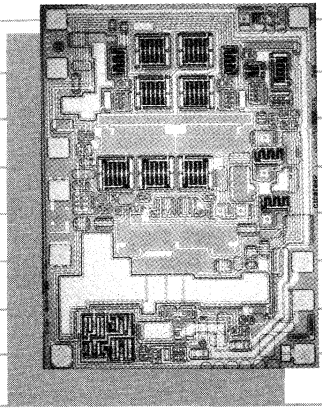

BURR-BROWN

integrated circuits data book supplement volume 33c

BURR-BROWN®

Operational Amplifiers
Instrumentation Amplifiers
Isolation Amplifiers
Analog Circuit Functions
D/A Converters
A/D Converters
Voltage-to-Frequency Converters
Digital Signal Processing
DC/DC Converters

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Individual product data sheets for models not listed here are available from your local Burr-Brown salesperson or representative. See the listing on the inside back cover.

How To Use This Book

If you know the **MODEL NUMBER,**	Use the Model Index on the **INSIDE FRONT COVER.**
If you know the **PRODUCT TYPE,**	Use the **TABBED TABLE OF CONTENTS** on page *v.* Or, use the **SELECTION GUIDE TABLES** at the front of each tabbed section.
If you want **NEW MODELS,**	Use the Model Index on the **INSIDE FRONT COVER** or the **SELECTION GUIDE TABLES** at the front of each tabbed section. All models contained in this supplement are shown in **boldface**; for other models see *Burr-Brown Integrated Circuits Data Book Volume 33*. Contact your local Burr-Brown salesperson or representative for information on new models.
If you want a **PRICE,**	If you are in the USA, see the **USA PRICE LIST,** Section 18. If you are outside the USA, contact your local Burr-Brown salesperson or representative.
If you want **MILITARY** components,	Contact your local Burr-Brown salesperson or representative. See **INSIDE BACK COVER.**
If you want **DIE,**	See **DIE INFORMATION AND SELECTION GUIDE,** Section 17, or contact your local Burr-Brown salesperson or representative.

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Burr-Brown Integrated Circuits Data Book Supplement

Volume 33c

NEW!
Data Book Supplement!

Use with IC Data Book Vol. 33

Replaces Vol. 33b

BURR-BROWN®

About Burr-Brown

Burr-Brown Corporation is a leading designer and manufacturer of precision microcircuits and microelectronic-based systems for use in data acquisition, signal conditioning, measurement, and control.

We make our products for customers who pursue business success in the same way we do — through worldwide competition based on high performance, high quality, and high value. Our customers include OEMs, sophisticated end-users, systems integrators, and VARs who demand an extra measure of performance for their products and operations.

COMPANY FACTS

- ✔ Founded in 1956.
- ✔ Corporate headquarters: Tucson, Arizona, USA.
- ✔ 1475 employees.
- ✔ 1000+ high-performance products.
- ✔ Manufacturing and technical facilities: Tucson, Arizona; Darmstadt, Germany; Livingston, Scotland; Atsugi, Japan.
- ✔ 13 North American direct sales offices, 29 sales representatives in 75+ locations.
- ✔ International sales and distribution subsidiaries in Austria, France, Germany, Italy, Japan, the Netherlands, Switzerland, and the United Kingdom; 25 sales representatives throughout the rest of the world.
- ✔ Over 250 sales and service staff worldwide.

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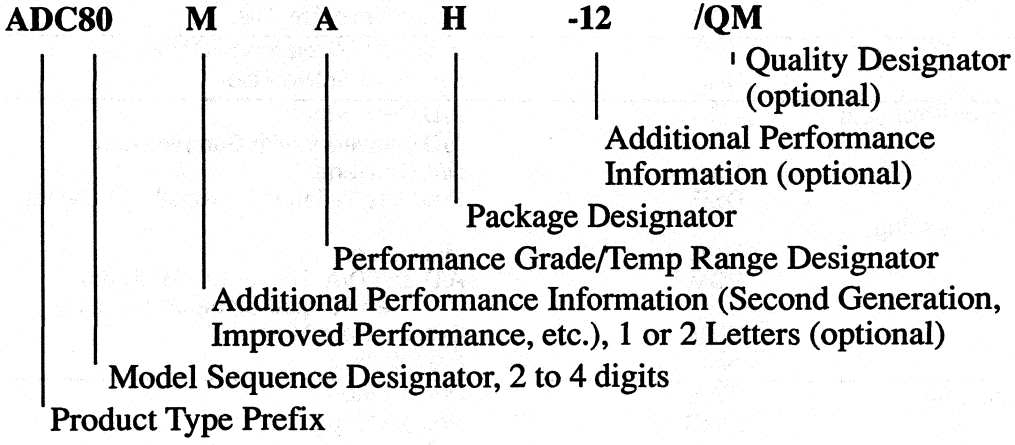
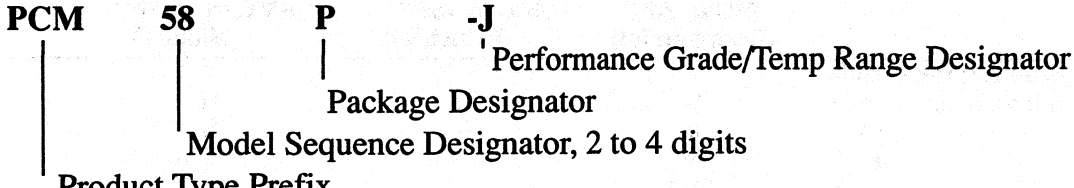
Understanding Component Model Numbers

Most Burr-Brown component products in this book have model numbers in the following form:



Exceptions: Second-source products are marked as similarly to the original vendor's part number as possible.

Some products designed for digital audio and signal processing applications have model numbers as follows:



Product Type Prefixes

Product Type	Prefix	Description
Amplifiers	OPA	Operational Amplifier
	INA	Instrumentation Amplifier
	PGA	Programmable Gain Amplifier
	ISO	Isolation Amplifier
Analog Circuit Functions	MFC	Multifunction Converter
	MPY	Multiplier
	DIV	Divider
	LOG	Logarithmic Amplifier
Frequency Products	VFC	Voltage-to-Frequency Converter
	UAF	Universal Active Filter
Conversion Products	ADC	A/D Converter
	ADS	A/D Converter with Sample/Hold
	DAC	D/A Converter
	DSP	Products Tailored Especially for Digital Signal Processing
	MPC	Multiplexer
	PCM	A/D and D/A Converters for Audio and Digital Signal Processing
	SDM	System Data Modules
	SHC	Sample/Hold
Miscellaneous	PWS	Power Supply
	PWR	Power Supply
	REF	Reference
	XTR	Transmitter
	RCV	Receiver

Performance Grade and Temperature Range Designators

	Temperature Range		
	0°C to 70°C (Commercial)	–25°C to +85°C [1] (Industrial)	–55°C to +125°C (Military)
Increasing Parametric Performance ↓	H	A	R
	J	B	S
	K	C (best)	T (best)
	L (best)		

NOTE: (1) For some industrial products this may be –40°C to 85°C.

Package Designators		Quality Designators	
M	Metal (hermetic)	Q	Burr-Brown's Q program
P	Plastic DIP (nonhermetic)	QM or /QM	Burr-Brown's Q program with Military Visual Criteria
G	Ceramic (hermetic or nonhermetic)	BI or B	Burn-in
U	SOIC		
N	PLCC		
L	Ceramic Leadless Chip Carrier		
D	Die		
H	Ceramic hermetic		

Where To Go From Here: Burr-Brown Sales & Service

The *Burr-Brown Integrated Circuits Data Book Supplement Vol. 33c* contains an extensive variety of new precision microcircuits. This new volume is a replacement for *Burr-Brown IC Data Book Supplement Vol. 33b*. You are urged to discard the old Vol. 33b and replace it with the new Vol. 33c. Many new products have been introduced since the January 1989 publication of the 1300-page *Burr-Brown Integrated Circuits Data Book Vol. 33*, which is available free upon request from your local salesperson or by calling **1-800-548-6132** (USA only). With both books, you will have an up-to-date collection of product data sheets on all commercial Burr-Brown IC parts.

ABOUT THIS BOOK

All Burr-Brown models are listed in Selection Guide tables at the beginning of each tabbed section. With these tables you can quickly compare specs among different models and choose the best part for your design. Complete product data sheets for items in **bold** are in this book, starting on the referenced page. Items not in bold are in the larger IC Data Book.

Data sheets are arranged alphanumerically, so if you know the name of the part you can find it quickly. Or, use the Model Index on the **inside front cover.** There you'll find models in this book in **bold** and arranged alphanumerically, along with models indexed from the larger IC Data Book. Throughout this book the prefix 'S' designates page numbers for the Data Book Supplement.

SUPERIOR CUSTOMER SERVICE

Burr-Brown gives you the best customer service in the industry — whether you need additional technical literature, technical assistance, to place an order, or to return products. For immediate assistance with any of the following, contact your local Burr-Brown salesperson or representative. See the **inside back cover.**

Technical Literature — In addition to individual data sheets, Burr-Brown has an extensive library of other useful publications. A brief summary: *IC Data Book, Vol. 33* (1/89); *Power Sources Handbook, Vol. 2* (8/90); reliability reports, application notes and handbook, *UPDATE, and Design Update*, our applications engineering newsletter. We also offer a comprehensive product selection guide on a PC diskette. The selection guide diskette is also available via our Electronic Bulletin Board Service (see below). For immediate assistance with technical literature, call our Product Information Center at **1-800-548-6132.**

Other Technical Information — Technical assistance is available during working hours to help you with product selection, literature requests, cross-reference, etc. Call the Product Information Center at **1-800-548-6132** (USA only).

Electronic Bulletin Board Service — Computer-based information system offers up-to-date product announcements, software/utilities (for example, SPICE models), technical support message center, and E-mail. Available 24 hours per day at no charge, except for toll call. Use these settings: 300/1200/2400 8-N-1; XMODEM file transfer. BBS number is (602) 741-3978.

Placing Orders — You can place orders via telephone, FAX, mail, TWX, or Telex with any authorized Burr-Brown field sales office, sales representative, or our Tucson headquarters. A complete list of sales offices is on the inside back cover of this book. For more information about placing an order, contact your local Burr-Brown salesperson or representative. See the **inside back cover.** Or, call customer service at **1-602-741-3930** (USA only).

If the products you want are readily available off the shelf, you can pay for them with your **VISA** or **MasterCard.** For more information, call customer service at **1-602-741-3930.**

Prices and Quotations — Prices in this book (USA only) are USA OEM prices and are subject to change. Price quotations made by Burr-Brown or its authorized field sales representatives are valid for 30 days. Delivery quotations are subject to reconfirmation at the time of order placement. For more information about pricing, contact your local Burr-Brown salesperson or representative. Or, call the Product Information Center at **1-800-548-6132** (USA only).

Returns and Warranty Service — When returning products for any reason, contact Burr-Brown prior to shipping for authorization and shipping instructions. For complete instructions, contact your local Burr-Brown sales office or representative. In the USA, call customer service at **1-602-741-3930.**

Please ship returned units prepaid and supply the original purchase order number and date, along with an explanation of the malfunction. Upon receipt of the returned unit and your RMA number, Burr-Brown will verify the malfunction and inform you of the warranty status, cost to repair or replace, credits, and status of replacement units where applicable.

2 Operational Amplifiers

Burr-Brown operational amplifiers are listed in eight applications groups described below. This helps you determine and select the best operational amplifier available for a design. Instrumentation amplifiers and isolation amplifiers are described in Sections 3 and 4 respectively.

The following Selection Guides show parameters for the high grade. Models shown in **boldface** are products included in this supplement.

LOW DRIFT

Low offset voltage drift vs temperature performance in both FET and bipolar input types is obtained by our sophisticated drift compensation techniques. First, the drift is measured and then special laser trim techniques are used to minimize the drift and the initial offset voltage at 25°C. Finally, "max drift" performance is retested for conformance with specifications.

LOW DRIFT OPERATIONAL AMPLIFIERS

Description	Model	Offset Voltage, max: At 25°C, (±mV)	Offset Voltage, max: Temp Drift, (±µV/°C)	Bias Current (25°C), max (nA)	Open Loop Gain, min (dB)	Frequency Response: Unity Gain (MHz)	Frequency Response: Slew Rate[3] (V/µs)	Rated Output, min: (±V)	Rated Output, min: (±mA)	Temp Range[1]	Pkg	Page No.
FET	**OPA627M**	**0.1**	**0.8**	**.005**	**112**	**16**	**55**	**11.5**	**45[3]**	**Ind**	**TO-99**	**S-2.121**
	OPA627P	**0.25**	**2**	**.005**	**112**	**16**	**55**	**11.5**	**45[3]**	**Ind**	**DIP**	**S-2.121**
	OPA627U	**0.5**	**2.5[3]**	**.01**	**106**	**16**	**55**	**11.5**	**45[3]**	**Ind**	**SOIC**	**S-2.121**
	OPA637M	**0.1**	**0.8**	**.005**	**112**	**80**	**135**	**11.5**	**45[3]**	**Ind**	**TO-99**	**S-2.121**
	OPA637P	**0.25**	**2**	**.005**	**112**	**80[4]**	**135**	**11.5**	**45[3]**	**Ind**	**DIP**	**S-2.121**
	OPA637U	**0.5**	**2.5[3]**	**.01**	**106**	**80[4]**	**135**	**11.5**	**45[3]**	**Ind**	**SOIC**	**S-2.121**
	OPA111M	0.25	1	±0.001	120	2	2	11	5.5	Ind	TO-99	2-55
	OPA671	**5.0**	**—**	**.05**	**74**	**35**	**107**	**10.5**	**50**	**Ind**	**DIP**	**S-2.159**
Wideband	OPA156M	2	5	0.05	94	6	14	10	5	Mil	TO-99	2-80
	OPA356M	2	5	0.05	94	6	14	10	5	Com	TO-99	2-80
	OPA602M	**0.25**	**2**	**±.001**	**92**	**6.5**	**35**	**11.5**	**15**	**Ind**	**TO-99**	**S-2.56**
	OPA602P	**1**	**5**	**±.002**	**88**	**6.5**	**35**	**11.5**	**15**	**Ind**	**DIP**	**S-2.56**
	OPA602U	**3**	**15**	**.01**	**75**	**6.5**	**35**	**11**	**15**	**Ind**	**SOIC**	**S-2.56**
	OPA606M	0.5	5	±0.01	100	13	35	12	5	Com	TO-99	2-158
	OPA606P	3	10[3]	.25	90	12	30	11	5	Com	DIP	2-158
	OPA671	**5.0**	**—**	**.05**	**74**	**35**	**107**	**10.5**	**50**	**Ind**	**DIP**	**S-2.159**
Dual FET	OPA2111M	0.5	2.8	±0.004	114	2	2	10	5	Ind, Mil	TO-99	2-195
	OPA2111P	2	15	.015	106	2	2	10	5	Com	DIP	2-195
	OPA2107M	**0.5**	**5**	**.005**	**84**	**4.5**	**18**	**11**	**5.5**	**Ind**	**TO-99**	**S-2.194**
	OPA2107P, U	**1**	**10**	**.01**	**82**	**4.5**	**18**	**11**	**5.5**	**Ind**	**DIP, SOIC**	**S-2.194**
Low Power (Dual) Single Supply Operation	**OPA1013M**	**0.15**	**2**	**20**	**120**	**0.6**	**.35**	**13**	**6.5**	**Com**	**TO-99**	**S-2.184**
	OPA1013P	**0.3**	**2.5**	**30**	**120**	**0.6**	**.35**	**12.5**	**6.25**	**Com**	**DIP**	**S-2.184**
Bipolar	**OPA177Z, P**	**0.01**	**0.1**	**1.5**	**134**	**0.6**	**0.3**	**12**	**12**	**Ind**	**DIP**	**S-2.11**
	OPA177S	**0.06**	**1.2**	**2.8**	**126**	**0.6**	**0.3**	**12**	**12**	**Ind**	**SOIC**	**S-2.11**
	OPA77Z, P	**0.025**	**0.3**	**2.0**	**134**	**0.6**	**0.3**	**12**	**12**	**Ind**	**DIP**	**S-2.11**
	OPA27J, Z	0.025	0.6	±40	120	8	1.9	12	16.7	Mil	TO-99, DIP	2-27 2-27
	OPA37J, Z	0.025	0.6	±40	120	63[2]	11.9	12	16.7	Mil	TO-99, DIP	2-27 2-27
	OPA27P, U	0.100	1.8	±80	117	8	1.9	12	16.7	Com	DIP, SOIC	2-27
	OPA37P, U	0.100	1.8	±80	117	63[2]	11.9	12	16.7	Com	DIP, SOIC	2-27

NOTES: (1) Com = 0°C to +70°C, Ind = –25°C to +85°C, Mil = –55°C to +125°C. (2) Gain BW Product at G = 5. (3) Typical. (4) Gain BW Product at G = 10.

LOW BIAS CURRENT

Our many years of experience in designing, manufacturing and testing FET amplifiers give us unique abilities in providing low and ultra-low bias current op amps. These amplifiers offer bias currents as low as 75fA (75 x 10^{-15}A) and voltage drift as low as 1µV/°C. With offset voltage laser-trimmed to as low as 250µV, the need for expensive trim pot adjustments is eliminated.

LOW BIAS CURRENT OPERATIONAL AMPLIFIERS

Description	Model	Offset Voltage, max: At 25°C, (±mV)	Offset Voltage, max: Temp Drift, (±µV/°C)	Bias Current (25°C), max (pA)	Open Loop Gain, min (dB)	Frequency Response: Unity Gain (MHz)	Frequency Response: Slew Rate[2] (V/µs)	Rated Output, min: (±V)	Rated Output, min: (±mA)	Temp Range[1]	Pkg	Page No.
FET	OPA111M	0.25	1	±1	120	2	2	11	5.5	Ind	TO-99	2-55
	OPA627M	**0.1**	**0.8**	**5**	**112**	**16**	**55**	**11.5**	**45[2]**	**Ind**	**TO-99**	**S-2.121**
	OPA627P	**0.25**	**2**	**5**	**112**	**16**	**55**	**11.5**	**45[2]**	**Ind**	**DIP**	**S-2.121**
	OPA627U	**0.5**	**2.5[2]**	**10**	**106**	**16**	**55**	**11.5**	**45[2]**	**Ind**	**SOIC**	**S-2.121**
	OPA637M	**0.1**	**0.8**	**5**	**112**	**80[4]**	**135**	**11.5**	**45[2]**	**Ind**	**TO-99**	**S-2.121**
	OPA637P	**0.25**	**2**	**5**	**112**	**80[4]**	**135**	**11.5**	**45[2]**	**Ind**	**DIP**	**S-2.121**
	OPA637U	**0.5**	**2.5[2]**	**10**	**106**	**80[4]**	**135**	**11.5**	**45[2]**	**Ind**	**SOIC**	**S-2.121**
	OPA671	**5.0**	**—**	**.05**	**74**	**35**	**107**	**10.5**	**50**	**Ind**	**DIP**	**S-2.159**
Low Noise	OPA101M	0.25	5	–10	94	10	6.5	12	12	Ind	TO-99	2-43
	OPA102M	0.25	5	–10	94	10[3]	14	12	12	Ind	TO-99	2-43
Ultra-Low Bias Current	OPA128M	0.5	5	±0.075	110	1	3	10	5	Com	TO-99	2-72
	AD515H	1	25	0.075	88	0.35	1	10	5	Com	TO-99	2-13
Dual FET	OPA2111M	0.5	2.8	±4	114	2	2	10	5	Ind	TO-99	2-195
	OPA2111P	2	15	±15	106	2	2	10	5	Com	DIP	2-195
	OPA2107M	**0.5**	**5**	**5**	**84**	**4.5**	**18**	**11**	**5.5**	**Ind**	**TO-99**	**S-2-194**
	OPA2107P, U	**1**	**10**	**10**	**82**	**4.5**	**18**	**11**	**5.5**	**Ind**	**DIP, SOIC**	**S-2-194**
Quad FET	**OPA404G**	**0.75**	**3[2]**	**±4**	**92**	**6.4**	**35**	**11.5**	**5**	**Ind**	**DIP**	**S-2.20**
	OPA404P, U	**2.5**	**5[2]**	**±12**	**88**	**6.4**	**35**	**11.5**	**5**	**Com**	**DIP, SOIC**	**S-2.20**
Low Cost	OPA121M	2	10	±5	110	2	2	11	5.5	Com	TO-99	2-66
	OPA121P, U	3	10	±10	106	2	2	11	5.5	Com	DIP, SOIC	2-66
	OPA602M	**0.25**	**2**	**1**	**92**	**6.5**	**35**	**11.5**	**15**	**Ind**	**TO-99**	**S-2.56**
	OPA602P	**1**	**5**	**2**	**88**	**6.5**	**35**	**11.5**	**15**	**Ind**	**DIP**	**S-2.56**
	OPA602U	**3**	**15**	**10**	**75**	**6.5**	**35**	**11**	**15**	**Com**	**SOIC**	**S-2.56**
Wideband	OPA606M	0.5	5	±10	100	13	35	12	5	Com	TO-99	2-158
	OPA606P	3	10[2]	±25	90	12	30	11	5	Com	DIP	2-158
	OPA654M	**3**	**40[2]**	**50**	**94[2]**	**32**	**750**	**11**	**200[2]**	**Ind**	**TO-3**	**S-2.135**
	OPA671	**5.0**	**—**	**.05**	**74**	**35**	**107**	**10.5**	**50**	**Ind**	**DIP**	**S-2.159**

NOTES: (1) Com = 0°C to +70°C, Ind = –25°C to +85°C, Mil = –55°C to +125°C. (2) Typical. (3) Gain = 3V/V. (4) Gain BW Product at G = 10.

LOW NOISE

Now both FET and bipolar input op amps are offered with guaranteed low noise specifications. Until now the designer had to rely on "typical" specs for his demanding low noise designs. These fully characterized parts allow a truly complete error budget calculation.

LOW NOISE OPERATIONAL AMPLIFIERS

Description	Model	Noise Voltage at 10kHz, max (nV/√Hz)	Bias Current (25°C), max (pA)	Offset Voltage, max: at 25°C (±mV)	Offset Voltage, max: Temp Drift (±µV/°C)	Open Loop Gain, min (dB)	Frequency Response: Gain BW (MHz)	Frequency Response: Slew Rate, min (V/µs)	Rated Output, min: (±V)	Rated Output, min: (±mA)	Temp Range[1]	Pkg	Page No.
Bipolar	OPA27J, Z	3.8	±40nA	0.025	0.6	120	8	1.7	12	16.7	Mil	TO-99, DIP	2-27

LOW NOISE OPERATIONAL AMPLIFIERS (Continued) — **Boldface = NEW**

Description	Model	Noise Voltage at 10kHz, max (nV/√Hz)	Bias Current (25°C), max (pA)	Offset Voltage, max at 25°C (±mV)	Offset Voltage, max Temp Drift (±µV/°C)	Open Loop Gain, min (dB)	Frequency Response Gain BW (MHz)	Frequency Response Slew Rate, min (V/µs)	Rated Output, min (±V)	Rated Output, min (±mA)	Temp Range[1]	Pkg	Page No.
	OPA37J, Z	3.8	±40nA	0.025	0.6	120	63	11	12	16.7	Mil	TO-99, DIP	2-27
	OPA177Z, P	**10[2]**	**1.5nA**	**0.01**	**0.1**	**134**	**0.6**	**0.1**	**12**	**12**	**Ind**	**DIP**	**S-2.11**
	OPA177S	**10**	**2.8nA**	**0.06**	**1.2**	**126**	**0.6**	**0.1**	**12**	**12**	**Ind**	**SOIC**	**S-2.11**
	OPA77Z, P	**11**	**2.0nA**	**0.025**	**0.3**	**134**	**0.6**	**0.1**	**12**	**12**	**Ind**	**DIP**	**S-2.11**
Wide Bandwidth	OPA101M	8	–10	0.25	5	94	20	5	12	12	Ind	TO-99	2-43
	OPA102M	8	–10	0.25	5	94	40	10	12	12	Ind	TO-99	2-43
FET	OPA111M	8	±1	0.25	1	120	2	1	11	5.5	Ind	TO-99	2-55
	OPA602M	**12[2]**	**1**	**0.25**	**2**	**92**	**6.5**	**28**	**11.5**	**15**	**Ind**	**TO-99**	**S-2.56**
	OPA602P	**12[2]**	**2**	**1**	**5**	**88**	**6.5**	**24**	**11.5**	**15**	**Ind**	**DIP**	**S-2.56**
	OPA602U	**12[2]**	**10**	**3**	**15**	**75**	**6.5**	**20**	**11**	**15**	**Ind**	**SOIC**	**S-2.56**
	OPA627M	**6**	**5**	**0.1**	**0.8**	**112**	**16**	**40**	**11.5**	**45[2]**	**Ind**	**TO-99**	**S-2.121**
	OPA627P	**6**	**5**	**0.25**	**2**	**112**	**16**	**40**	**11.5**	**45[2]**	**Ind**	**DIP**	**S-2.121**
	OPA627U	**4.8[2]**	**10**	**0.5**	**2.5[2]**	**106**	**16**	**40**	**11.5**	**45[2]**	**Ind**	**SOIC**	**S-2.121**
	OPA637M	**6**	**5**	**1**	**0.8**	**112**	**80**	**100**	**11.5**	**45[2]**	**Ind**	**TO-99**	**S-2.121**
	OPA637P	**6**	**5**	**0.25**	**2**	**112**	**80**	**100**	**11.5**	**45[2]**	**Ind**	**DIP**	**S-2.121**
	OPA637U	**4.8[2]**	**10**	**0.5**	**2.5[2]**	**106**	**80**	**40**	**11.5**	**45[2]**	**Ind**	**SOIC**	**S-2.121**
Low Cost	OPA27P, U	4.5	±80nA	0.100	1.8	117	8	1.7	12	16.7	Com	DIP, SOIC	2-27
	OPA37P, U	4.5	±80nA	0.100	1.8	117	63	11	12	16.7	Com	DIP, SOIC	2-27
Dual FET	OPA2111M	8	±4	0.5	2.8	114	2	1	10	5	Ind	TO-99	2-195
	OPA2111P	6[2]	±15	2	15	106	2	2[2]	10	5	Com	DIP	2-195
Dual Audio Op Amp	**OPA2604P,U**	**10[2]**	**100[2]**	**3**	**8[2]**	**80**	**20**	**15**	**11**	**35[2]**	**Ind**	**DIP, SOIC**	**S-2.210 S-2.210**

NOTES: (1) Ind = –25°C to +85°C, Mil = –55°C to +125°C, Com = 0°C to +70°C. (2) Typical.

UNITY-GAIN BUFFER (POWER BOOSTER)

These versatile amplifiers boost the ouput current capability of another amplifier; buffer an impedance that might load a critical circuit; and may be used inside the feedback loop of another op amp to form a current-boosted, composite amplifier. Currents as high as ±200mA are available with speeds of 2000V/µs.

UNITY-GAIN BUFFER OPERATIONAL AMPLIFIERS — **Boldface = NEW**

Description	Model	Rated Output, min (±V)	Rated Output, min (±mA)	Frequency Responses –3dB (MHz)	Frequency Responses Full Power (MHz)	Frequency Responses SlewRt (V/µs)	Gain (V/V)	Input Impedance (Ω)	Temp Range[1]	Pkg	Page No.
High Performance	3553	10	200	300	32	2000	≈1	10^{11}	Ind	TO-3	2-225
Low Cost	OPA633	11	80	275	65	2500	≈1	1.5×10^6	Ind	DIP	2-176
Transconductance Amp and Buffer	**OPA660**	**4**	**8**	**700**	**550**	**2000**	**≈1**	**10^6**	**Ind**	**DIP, SOIC**	**S-2.143**
High Slew Rate	**BUF600**	**±3.35**	**±20**	**650**	**320**	**3400**	**≈1**	**4.8M**	**Ind**	**DIP/SO**	**S-2.7**
	BUF601	**±3.35**	**±20**	**300**	**320**	**3600**	**≈1**	**2.5M**	**Ind**	**DIP/SO**	**S-2.7**

NOTE: (1) Ind = –25°C to +85°C.

WIDE BANDWIDTH

Design expertise in wideband circuits combines with our fully developed technology to create cost-effective wideband op amps. Burr-Brown high-speed amplifiers also offer outstanding DC performance specifications.

WIDE BANDWIDTH OPERATIONAL AMPLIFIERS — **Boldface = NEW**

Description	Model	Frequency Response: Gain BW (MHz)	Slew Rate min (V/µs)	t_s ±0.1% (ns)	Comp	Rated Output, min (±V)	Rated Output, min (±mA)	Offset Voltage, max: At 25°C (±mV)	Offset Voltage, max: Temp Drift (±µV/°C)	Open Loop Gain, min (dB)	Temp Range[1]	Pkg	Page No.
FET	OPA156M	6	10	1.5µs	int	10	5	2	5	94	Mil	TO-99	2-80
	OPA356M	6	10	1.5µs	int	10	5	2	5	94	Com	TO-99	2-80
	OPA602M	**6.5**	**28**	**600**	**int**	**11.5**	**15**	**0.25**	**2**	**92**	**Ind**	**TO-99**	**S-2.56**
	OPA602P	**6.5**	**24**	**600**	**int**	**11.5**	**15**	**0.5**	**5**	**88**	**Ind**	**DIP**	**S-2.56**
	OPA602U	**6.5**	**20**	**600**	**int**	**11**	**15**	**3**	**15**	**75**	**Ind**	**SOIC**	**S-2.56**
	OPA654M	**500**	**750[2]**	**150**	**ext**	**11**	**200[2]**	**3**	**40[2]**	**94[2]**	**Ind**	**TO-3**	**S-2.135**
	OPA671	**30**	**120[2]**	**150**	**int**	**10**	**50[2]**	**5**	**5[2]**	**74[2]**	**Ind**	**DIP**	**S-2.159**
Dual	**OPA2107M**	**4.5**	**13**	**1.5µs**	**int**	**11**	**5.5**	**0.5**	**5**	**84**	**Ind, Mil**	**TO-99**	**S-2.194**
	OPA2107P, U	**4.5**	**13**	**1.5µs**	**int**	**11**	**5.5**	**1**	**10**	**82**	**Ind**	**DIP, SOIC**	**S-2.194 S-2.194**
Dual Audio	**OPA2604P, U**	**20**	**15**	**1µs**	**int**	**11**	**35[2]**	**3**	**8[2]**	**80**	**Ind**	**DIP, SOIC**	**S-2.210 S-2.210**
Op Amp	OPA605M	200, A=1000	300[4]	230	ext	10	30	0.5	5	80[3]	Ind	DIP	2-152
	OPA606M	13	25	1µs	int	12	5	0.5	5	100	Com	TO-99	2-158
	OPA606P	12	20	1µs	int	11	5	3	10[2]	90	Com	TO-99	2-158
	OPA627M	**16**	**40**	**450**	**int**	**11.5**	**45[2]**	**0.1**	**0.8**	**112**	**Ind**	**TO-99**	**S-2.121**
	OPA627P	**16**	**40**	**450**	**int**	**11.5**	**45[2]**	**0.25**	**2**	**112**	**Ind**	**DIP**	**S-2.121**
	OPA627U	**80**	**40**	**450**	**int**	**11.5**	**45[2]**	**0.5**	**2.5[2]**	**106**	**Ind**	**SOIC**	**S-2.121**
	OPA637M	**80**	**100**	**300**	**G>5**	**11.5**	**45[2]**	**0.1**	**0.8**	**112**	**Ind**	**TO-99**	**S-2.121**
	OPA637P	**80**	**100**	**300**	**G>5**	**11.5**	**45[2]**	**0.25**	**2**	**112**	**Ind**	**DIP**	**S-2.121**
	OPA637U	**80**	**100**	**300**	**675**	**11.5**	**45**	**0.5**	**2.5[2]**	**106**	**Ind**	**SOIC**	**S-2.121**
	3554M	1700, A=1000	1000	120	ext	10	100	1	15	100	Ind	TO-3	2-229
Bipolar	3507	20, A=10	80	200	ext	10	10	10	30[2]	83	Com	TO-99	2-213
Current-Feedback	**OPA603P**	**50 (G=1 to 50)**	**1000**	**50**	**NA**	**10**	**75**	**5**	**8 typ**	**NA**	**Ind**	**DIP**	**S-2.66**
Low Power High Slew Rate	**OPA623**	**280**	**2000**	**TBD**	**NA**	**±3.3**	**±70**	**2**	**50**	**NA**	**Ind**	**DIP/SO**	**S-2.117**
Transconductance Amp and Buffer	**OPA660**	**700**	**2000**	**25**	**NA**	**4.0**	**20**	**20**	**50**	**NA**	**Ind**	**DIP,SOIC**	**S-2.143**
Dual Transconductance Amp	**OPA2662**	**200**	**2000**	**TBD**	**NA**	**±4**	**±75**	**±7**	**50**	**TBD**	**Ind**	**DIP/SO**	**S-2.222**
Quad FET	**OPA404G**	**6.4**	**28**	**600**	**int**	**11.5**	**5**	**0.75**	**3[2]**	**92**	**Ind**	**DIP**	**S-2.20**
	OPA404P, U	**6.4**	**24**	**600**	**Int**	**11.5**	**5**	**2.5**	**5[2]**	**88**	**Com**	**DIP, SOIC**	**S-2.20**
Low Noise Bipolar	OPA27J, Z	8,A=1	1.7	—	int	12	16.7	0.025	0.6	120	Mil	TO-99, DIP	2-27
	OPA37J, Z	63,A=5	11	—	int[3]	12	16.7	0.025	0.6	120	Mil	TO-99, DIP	2-27
Low Noise FET	OPA101M	20, A=100	5	2.5µs	int	12	12	0.25	5	94	Ind	TO-99	2-43
	OPA102M	40, A=100	10	1.5µs	int	12	12	0.25	5	94	Ind	TO-99	2-43

WIDE BANDWIDTH OPERATIONAL AMPLIFIERS (Continued)

Boldface = NEW

Description	Model	Frequency Response: Gain BW (MHz)	Frequency Response: Slew Rate min (V/µs)	Frequency Response: t_s ±0.1% (ns)	Comp	Rated Output, min: (±V)	Rated Output, min: (±mA)	Offset Voltage, max: At 25°C (±mV)	Offset Voltage, max: Temp Drift (±µV/°C)	Open Loop Gain, min (dB)	Temp Range[1]	Pkg	Page No.
Very Fast	**OPA620**	**200**	**175[2]**	**10**	**int**	**3**	**150[2]**	**0.5**	**8[2]**	**55**	**Com, Mil**	**DIP, SOIC**	**S-2.79 S-2.79**
	OPA622	**150**	**1600**	**TBD**	**NA**	**±3.5**	**±70**	**±0.5**	**50**	**NA**	**Ind**	**DIP/SO**	**S-2.112**
Settling Precision	**OPA621**	**500, A=10**	**350[2]**	**15**	**int**	**3**	**150[2]**	**0.5**	**12[2]**	**55**	**Com, Mil**	**DIP, SOIC**	**S-2.96 S-2.96**
	OPA600	**5000, A=1000**	**500**	**80**	**ext**	**9**	**180**	**4**	**40**	**86**	**Ind**	**DIP**	**S-2.47**
Very Fast Settling Switched Input	**OPA675G**	**3000, A=16**	**240**	**15**	**ext**	**2.1**	**30[2]**	**1**	**5**	**65**	**Com, Mil**	**DIP**	**S-2.166**
	OPA676G	**3000, A=16**	**240**	**15**	**ext**	**2.1**	**30[2]**	**1**	**5**	**65**	**Com, Mil**	**DIP**	**S-2.166**
	OPA678U, G	**200 A=1**	**350[2]**	**15**	**ext**	**2.5**	**40[2]**	**1**	**5**	**50**	**Ind, Mil**	**DIP SOIC**	**S-2.179 S-2.179**
Low Cost	OPA27P, U	8, A=1	1.7	—	int	12	16.7	0.100	1.8	117	Com	DIP, SOIC	2-27
	OPA37P, U	63, A=5	11	—	int[3]	12	16.7	0.100	1.8	117	Com	DIP, SOIC	2-27
Current Fdbk FET Input	**OPA603**	**100**	**1000[2]**	**50**	**int**	**12**	**150[2]**	**5**	**8[2]**	**440kΩ**	**Ind**	**DIP**	**S-2.66**
	OPA671	**30**	**120[2]**	**150**	**int**	**10**	**50[2]**	**5**	**5[2]**	**74[2]**	**Ind**	**DIP, SOIC**	**S-2.159**

NOTES: (1) Com = 0°C to +70°C, Ind = –25°C to +85°C, Mil = –55°C to +125°C. (2) Typical. (3) G = 5 min. (4) Typical G ≥ 50.

HIGH VOLTAGE, HIGH CURRENT OPERATIONAL AMPLIFIERS

Boldface = NEW

Description	Model	Rated Output, min: (±V)	Rated Output, min: (±mA)	Offset Voltage, max: At 25°C (±mV)	Offset Voltage, max: Temp Drift (±µV/°C)	Bias Current (25°C), max (pA)	Frequency Response: Unity Gain (MHz)	Frequency Response: Slew Rate (V/µs)	Open Loop Gain (dB)	Temp Range[1]	Pkg	Page No.
High Power	OPA501	26	10A	5	40	20nA	1	1.35	98	Ind	TO-3	2-109
	OPA511	22	5A	10	65	40	1	1	91	Ind	TO-3	2-117
	OPA512	35	10A	6	65	30	4	2.5	110	Ind	TO-3	2-122
		35	15A	3	40	20	4	2.5	110	Mil	TO-3	2-122
	OPA541	**35**	**5A**	**1**	**30**	**50**	**1.6**	**6**	**90**	**Ind**	**TO-3**	**S-2.39**
		30	**5A**	**10**	**40**	**50**	**1.6**	**6**	**90**	**Ind**	**Power Plastic**	**S-2.39**
(Dual)	**OPA2541**	**35**	**5A**	**1**	**30**	**50**	**1.6**	**8**	**90**	**Ind**	**TO-3**	**S-2-202**
	3573	20	2A[4]	10	65	40nA	1	2.6	94	Ind	TO-3	2-243
Wideband	3554M	10	100	1	15	–50	1700[2]	1200	100	Ind	TO-3	2-229
	OPA654M	**11**	**200[5]**	**3**	**40[5]**	**50**	**32**	**750**	**94**	**Ind**	**TO-3**	**S-2.135**
High Voltage	3584	145	15	3	25	20	20[2]	150	126	Com	TO-3	2-255
	3583	140	75	3	25	20	5	30	118	Ind	TO-3	2-251
	3582	145	15	3	25	20	5	20	118	Com	TO-3	2-247
	3581	70	30	3	25	20	5	20	112	Com	TO-3	2-247
	3580	30	60	10	30	50	5	15	106	Com	TO-3	2-247
	OPA445	**35**	**15**	**3**	**10**	**50**	**2**	**10**	**100**	**Ind**	**TO-99,DIP**	**S-2.32**
Buffer	3553	10	200	50	300[5]	200	300	2000	NA	Ind	TO-3	2-225
	OPA633	11	80	15	33[5]	35µA	275[5]	2500	NA	Ind	DIP	2-176

NOTES: (1) Com = 0°C to +70°C, Ind = –25°C to +85°C, Mil = –55°C to +125°C. (2) Gain-bandwidth product. (3) 2A peak. (4) 5A peak. (5) Typical.

SPECIAL PURPOSE

These op amps offer specialized performance or function, including devices with switched inputs (OPA675/676) and wideband voltage controlled amplifiers (VCA610.)

SPECIAL PURPOSE OPERATIONAL AMPLIFIERS — **Boldface = NEW**

Description	Model	Offset Voltage, max: At 25°C, (±mV)	Offset Voltage, max: Temp Drift, (±µV/°C)	Bias Current (25°C), max (µA)	Open Loop Gain, min (dB)	Frequency Response: Unity Gain (MHz)	Frequency Response: Slew Rate (V/µs)	Rated Output, min: (±V)	Rated Output, min: (±mA)	Temp Range[1]	Pkg	Page No.
Very Fast	**OPA675G**	**1**	**5**	**35**	**65**	**185[2]**	**350**	**2.1**	**30**	**Com, Mil**	**DIP**	**S-2.166**
Settling	**OPA676G**	**1**	**5**	**35**	**65**	**185[2]**	**350**	**2.1**	**30**	**Com, Mil**	**DIP**	**S-2.166**
Voltage	**OPA678**	**1.5**	**20**	**50**	**50**	**200**	**350**	**2.5**	**30**	**Com, Mil**	**DIP, SOIC**	**S-2.179**
Controlled Gain	**VCA610**	**—**	**—**	**12[3]**	**[4]**	**35[5]**	**100**	**3.0[6]**	**8**	**Com**	**DIP, SOIC**	**S-2.227**

NOTES: (1) Com = 0°C to +70°C, Mil = –55°C to +125°C. (2) –3dB BW at Gain of +10V/V. (3) Typical. (4) C/L Gain range: –40 to +40dB. (5) Gain = 40dB. (6) Vp-p.

Models STILL available but not listed on the cover of this book

Model	Description	Recommended Newer Model	Equivalency[1]
3550	Fast Settling FET Op Amp	OPA671A	F/E
3551	Wideband and Fast Settling FET Op Amp	OPA671AP	F/E

NOTES: (1) F/E = Functional Equivalent. Very similar function, very similar performance, but not pin for pin.

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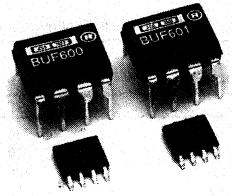


BUF600/601

ADVANCE INFORMATION
SUBJECT TO CHANGE

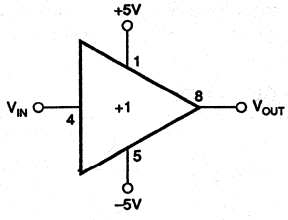
HIGH-SPEED BUFFER AMPLIFIER

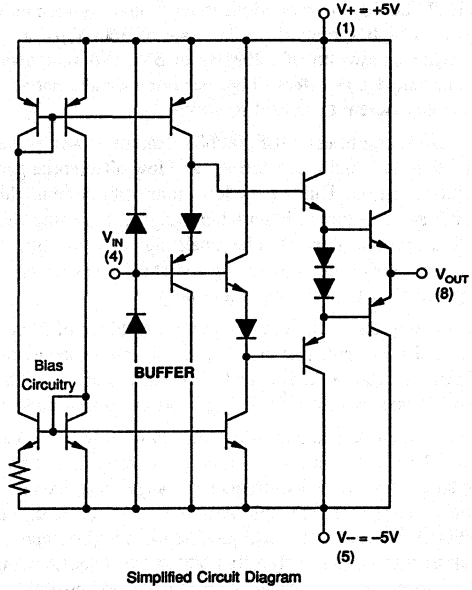
FEATURES

- OUTSTANDING AC-PERFORMANCE
- EXCELLENT FORWARD AND VERY LOW REVERSE GAIN
- OPEN LOOP BUFFER
- HIGH-SLEW RATE: 3600V/μs, 5.0Vp-p
- LARGE SIGNAL BANDWIDTH: 320MHz, 5Vp-p
- LOW INPUT BIAS CURRENT: 1μA/2μA
- LOW QUIESCENT CURRENT: 3mA/6mA
- REPLACES DISCRETE/HYBRID SOLUTIONS
- SAVES BOARD SPACE AND CONSERVES POWER
- IMPROVED PERFORMANCE
- SIGNAL FIDELITY

APPLICATIONS

- VIDEO BUFFER/LINE DRIVER
- INPUT/OUTPUT AMPLIFIER FOR MEASUREMENT EQUIPMENT
- PORTABLE SYSTEMS
- TRANSMISSION SYSTEMS
- TELECOMMUNICATIONS
- HIGH-SPEED ANALOG SIGNAL PROCESSING





Simplified Circuit Diagram

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SPECIFICATIONS

ELECTRICAL

At V_{CC} = ±5VDC, R_{LOAD} = 100Ω (BUF601), R_{LOAD} = 200Ω (BUF600), and T_A = 25°C unless otherwise noted.

PARAMETER	CONDITIONS	BUF600	BUF601	UNITS
AC-PERFORMANCE		TYP	TYP	
Small Signal Bandwidth	V_{OUT} = 0.2Vp-p	650	820	MHz
Large Signal Bandwidth	V_{OUT} = 5.0Vp-p	320	320	MHz
	V_{OUT} = 2.8Vp-p	435	400	MHz
	V_{OUT} = 1.4Vp-p	710	700	MHz
Slew Rate	V_{IN} = 5.0Vp-p	3400	3600	V/µs
	V_{IN} = 2.8Vp-p	2400	2400	V/µs
	V_{IN} = 1.4Vp-p	1500	1500	V/µs
Group Delay Time			<200	ps
Differential Phase	f = 4.43MHz, V_{IN} = 0.3Vp-p, VDC = 0V to 0.7V	0.02	0.025	deg
Differential Gain	f = 4.43MHz, V_{IN} = 0.3Vp-p, VDC = 0V to 0.7V	0.5	0.4	%
DC -PERFORMANCE				
OUTPUT CHARACTERISTICS				
Voltage Output		±3.35	±3.35	V
Current Output	DC	20	20	mA
	AC	50	50	mA
Output Impedance		10	5	Ω
Offset Voltage	Initial	3	3	mV
TRANSFER CHARACTERISTICS				
Gain	R_L = 1kΩ		0.9902	V/V
	R_L = 2kΩ		0.9922	V/V
	R_L = 5kΩ		0.9936	V/V
INPUT CHARACTERISTICS				
Noise Voltage			4	nV/√Hz
Impedance			2.5 ‖ 0.65	MΩ ‖ pF
POWER SUPPLY				
Rated Voltage		±5	±5	V
Quiescent Current		3	6	mA

DESCRIPTION

The BUF600/601 are monolithic open-loop unity-gain buffers with a high symmetrical slew rate of 3600V/µs and a very wide bandwidth of 320MHz at 5Vp-p output level. Their unique design offers a high-performance alternative to expensive discrete or hybrid solutions.

The buffer amplifiers BUF600/601 feature lower power dissipation, low input bias current, and low differential gain and phase errors. Due to its low quiescent current, this circuit is suitable for use in portable equipment or equipment supplied by solar current. The small signal delay time of 300/200ps allows very fast analog signal transmission and a low phase shift between input and output.

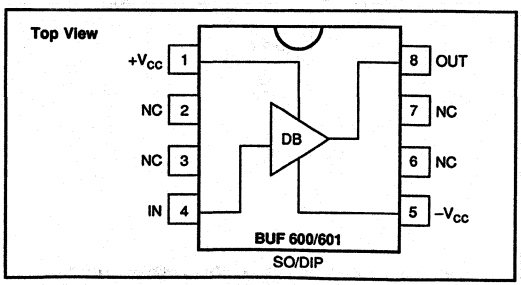
With its long-term DC output current capability of 20mA, 50mA pulse current, and stability to capacitive loads, the BUF601 can also drive 50Ω and 75Ω systems or lines. This capability makes it ideal for RF, IF, and video applications.

Due to its small-signal delay time and phase shift, low offset voltage between input and output, constant low output impedance over a broad frequency range, and excellent relation between bandwidth and quiescent current, the BUF600 is well-suited for operation between high-frequency signal processing stages. The BUF600 shows its outstanding performance even in feedback loops of wideband operational amplifiers. This type of open-loop buffer is a new and easy-to-use step to prevent an interaction between two points in complex high-speed analog circuitry.

The broad range of analog and digital applications extends from high-resolution graphic cards, graphic terminal R-G-B or composite video line drivers, and impedance transformation, to flash ADC input buffers, and analog and digital oscilloscope input stages.

All performance is specified and rated for operation with supplies of ±5V, reducing power consumption compared with traditional ±15V designs. The BUF600/601 are available in a space-saving SO package and a low-cost plastic DIP package, both for operation over the industrial (–40°C to +85°C) range.

PIN CONFIGURATION



DISCUSSION OF PERFORMANCE

The open-loop buffer amplifiers BUF600/601 use a complementary bipolar IC process which incorporates pn-junction isolated high-frequency NPN and PNP transistors to achieve excellent high-frequency performance unattainable with conventional integrated circuit technology. The two buffer amplifiers provide a level of full power bandwidth previously not possible in monolithic form, much less in hybrid form.

In addition, the circuit shows the excellent AC and DC performance parameters, as shown in the specification table, with a drastically reduced quiescent current and lower input bias current.

These two factors, along with decreased board space, are very important in an increasingly complex electronic environment and for portable telecommunications equipment.

The BUF600/601 are 3-stage buffers with an implemented boost circuit in the input stage responsible for the high slew rates and wide large-signal bandwidth. The cross current in the input stage can be kept to about 100µA, which results in a low input bias current of 2µA.

The second stage drives the output transistors and reduces the feedthrough from the output to the input when driving (RLC) loads.

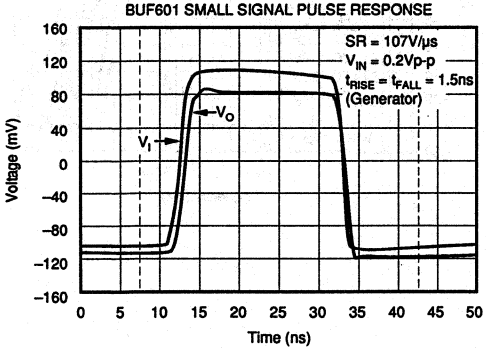
An ideal buffer has an exact unity gain from input to output, irrespective of the load. The characteristic of the unity gain is called "forward gain." An ideal buffer also allows a variety of complex loads to be driven at the output without modifying the existing input condition. This characteristic is called "reverse gain" and should be zero.

Because of the wideband nature of the BUF600/601, forward and reverse gain are specified in S-parameters. They are reflection and transmission coefficients, which are used to describe a linear two-port network in the same way as Y, Z, or H parameters. Short or open circuits are misnomers in RF circles. Instead, the network is defined in terms of incident and reflected waveforms. Waveforms are easier to measure and the results are more realistic above 100MHz.

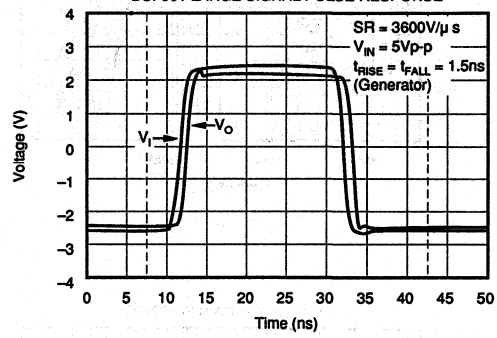
TYPICAL PERFORMANCE CURVES

At V_{CC} = ±5VDC, R_{LOAD} = 100Ω (BUF601), R_{LOAD} = 200Ω (BUF600), and T_A = 25°C unless otherwise noted.

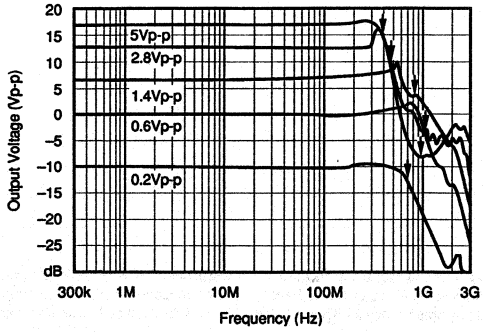
BUF601 SMALL SIGNAL PULSE RESPONSE



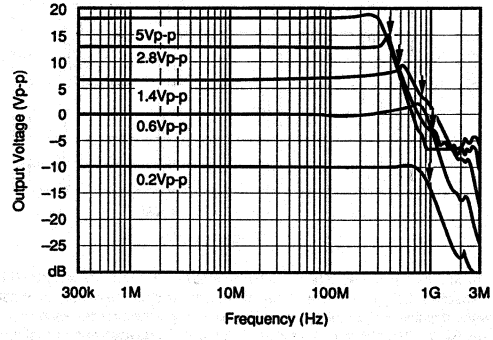
BUF601 LARGE SIGNAL PULSE RESPONSE



BUF600 BANDWIDTH vs OUTPUT VOLTAGE



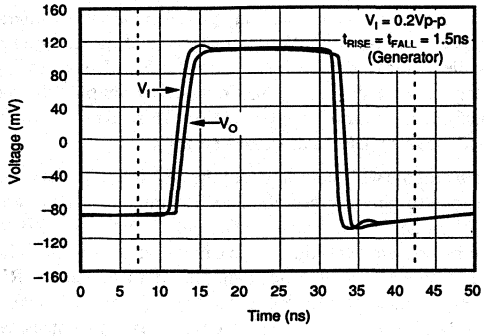
BUF601 BANDWIDTH vs OUTPUT VOLTAGE



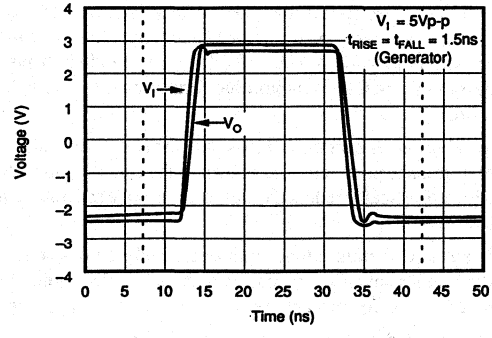
TYPICAL PERFORMANCE CURVES (CONT)

At V_{CC} = ±5VDC, R_{LOAD} = 100Ω (BUF601), R_{LOAD} = 200Ω (BUF600), and T_A = 25°C unless otherwise noted.

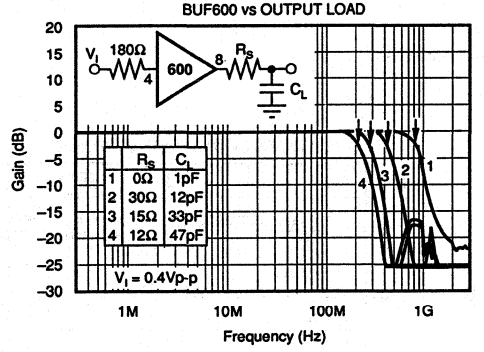
BUF600 SMALL SIGNAL PULSE RESPONSE



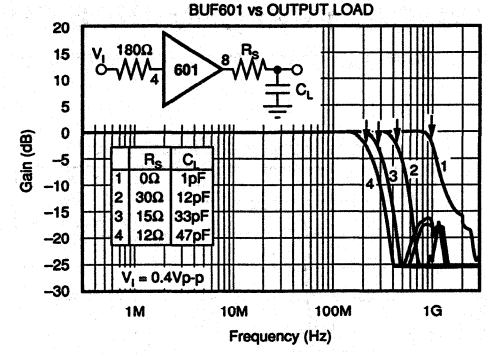
BUF600 LARGE SIGNAL PULSE RESPONSE



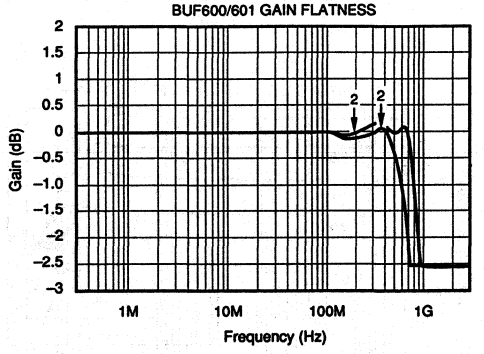
BUF600 vs OUTPUT LOAD



BUF601 vs OUTPUT LOAD



BUF600/601 GAIN FLATNESS



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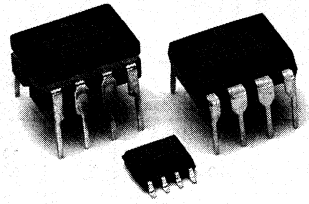


OPA177
OPA77

AVAILABLE IN DIE

Precision OPERATIONAL AMPLIFIER

FEATURES

- LOW OFFSET VOLTAGE: 10μV max
- LOW DRIFT: 0.1μV/°C
- HIGH OPEN-LOOP GAIN: 130dB min
- LOW QUIESCENT CURRENT: 1.5mA typ
- REPLACES INDUSTRY-STANDARD OP AMPS: OP-07, OP-77, OP-177, AD707, ETC.

APPLICATIONS

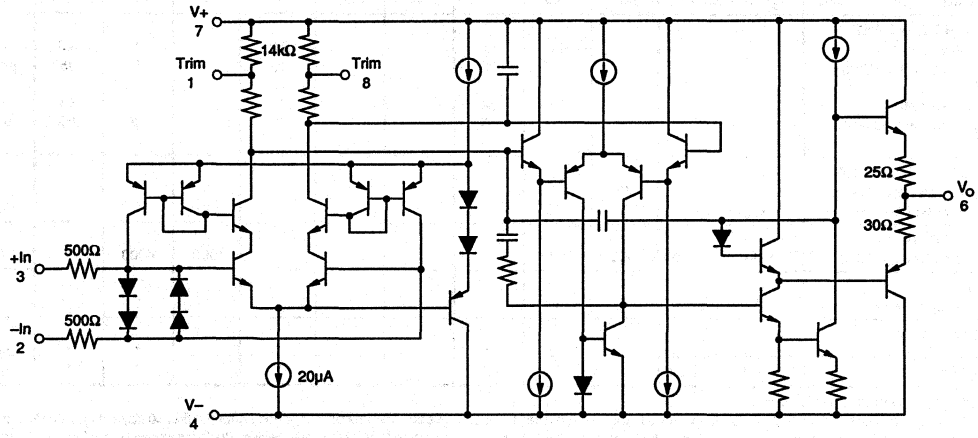
- PRECISION INSTRUMENTATION
- DATA ACQUISITION
- TEST EQUIPMENT
- BRIDGE AMPLIFIER
- THERMOCOUPLE AMPLIFIER

DESCRIPTION

The OPA177 and OPA77 precision bipolar op amps feature very low offset voltage and drift. Laser-trimmed offset, drift and input bias current virtually eliminate the need for costly external trimming. Their high performance and low cost make them ideally suited to a wide range of precision instrumentation.

The low quiescent current of the OPA177 and OPA77 dramatically reduce warm-up drift and errors due to thermoelectric effects in input interconnections. They provide an effective alternative to chopper-stabilized amplifiers. The low noise of the OPA177 and OPA77 maintains accuracy.

OPA177 and OPA77 performance gradeouts are available. Packaging options include 8-pin plastic DIP, 8-pin ceramic DIP, and SO-8 surface-mount packages.



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OPA177 SPECIFICATIONS

ELECTRICAL

At V_S = ±15V, T_A = +25°C unless otherwise noted.

PARAMETER	CONDITION	OPA177E			OPA177F			OPA177G			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
OFFSET VOLTAGE											
Input Offset Voltage			4	10		10	25		20	60	µV
Long-Term Input Offset[1]			0.2			0.3			0.4		µV/Mo
Voltage Stability											
Offset Adjustment Range	R_P = 20kΩ		±3			•			•		mV
Power Supply Rejection Ratio	V_S = ±3V to ±18V	120	125		115	•		110	120		dB
INPUT BIAS CURRENT											
Input Offset Current			0.3	1		•	1.5		•	2.8	nA
Input Bias Current			0.5	±1.5		•	±2		•	±2.8	nA
NOISE											
Input Noise Voltage	1Hz to 100Hz[2]		85	150		•	•		•	•	nVrms
Input Noise Current	1Hz to 100Hz		4.5			•			•		pArms
INPUT IMPEDANCE											
Input Resistance	Differential Mode[3]	26	45		•	•		18.5	•		MΩ
	Common Mode		200			•			•		GΩ
INPUT VOLTAGE RANGE											
Common-Mode Input Range[4]		±13	±14		•	•		•	•		V
Common-Mode Rejection	V_{CM} = ±13V	130	140		•	•		115	•		dB
OPEN-LOOP GAIN	R_L ≥ 2kΩ										
Large-Signal Voltage Gain	V_O = ±10V[5]	5000	12000		•	•		2000	6000		V/mV
OUTPUT											
Output Voltage Swing	R_L ≥ 10kΩ	±13.5	±14		•	•		•	•		V
	R_L ≥ 2kΩ	±12.5	±13		•	•		•	•		V
	R_L ≥ 1kΩ	±12	±12.5		•	•		•	•		V
Open-Loop Output Resistance			60			•			•		Ω
FREQUENCY RESPONSE											
Slew Rate	R_L ≥ 2kΩ	0.1	0.3		•	•		•	•		V/µs
Closed-Loop Bandwidth	G = +1	0.4	0.6		•	•		•	•		MHz
POWER SUPPLY											
Power Consumption	V_S = ±15V, No Load		40	60		•	•		•	•	mW
	V_S = ±3V, No Load		3.5	4.5		•	•		•	•	mW
Supply Current	V_S = ±15V, No Load		1.3	2		•	•		•	•	mA

ELECTRICAL

At V_S = ±15V, –40°C ≤ T_A ≤ +85°C, unless otherwise noted.

OFFSET VOLTAGE											
Input Offset Voltage			10	20		15	40		20	100	µV
Average Input Offset			0.03	0.1		0.1	0.3		0.7	1.2	µV/°C
Voltage Drift[6]											
Power Supply Rejection Ratio	V_S = ±3V to ±18V	120	125		110	120		106	115		dB
INPUT BIAS CURRENT											
Input Offset Current			0.5	1.5		•	2.2		•	4.5	nA
Average Input Offset Current			1.5	25		•	40		•	85	pA/°C
Drift[7]											
Input Bias Current			0.5	±4		•	•		•	±6	nA
Average Input Bias Current			8	25		•	40		15	60	pA/°C
Drift[7]											
INPUT VOLTAGE RANGE											
Common-Mode Input Range		±13	±13.5		•	•		•	•		V
Common-Mode Rejection	V_{CM} = ±13V	120	140		•	•		110	•		dB
OPEN-LOOP GAIN											
Large-Signal Voltage Gain	R_L ≥ 2kΩ, V_O = ±10V	2000	6000		•	•		1000	4000		V/mV
OUTPUT											
Output Voltage Swing	R_L ≥ 2kΩ	±12	±13		•	•		•	•		V
POWER SUPPLY											
Power Consumption	V_S = ±15V, No Load		60	75		•	•		•	•	mW
Supply Current	V_S = ±15V, No Load		2	2.5		•	•		•	•	mA

* Same as specifcation for product to left.

NOTES: (1) Long-Term Input Offset Voltage Stability refers to the averaged trend line of V_{OS} vs time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically less than 2µV. (2) Sample tested. (3) Guaranteed by design. (4) Guaranteed by CMRR test condition. (5) To insure high open-loop gain throughout the ±10V output range, A_{OL} is tested at –10V ≤ V_O ≤ 0V, 0V ≤ V_O ≤ +10V, and –10V ≤ V_O ≤ +10V. (6) OP177EZ and OP177FZ: TCV_{OS} is 100% tested. (7) Guaranteed by end-point limits.

OPA77 SPECIFICATIONS

ELECTRICAL

At V_S = ±15V, T_A = +25°C unless otherwise noted.

PARAMETER	CONDITION	OPA77E			OPA77F			OPA77G			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
OFFSET VOLTAGE											
Input Offset Voltage			10	25		20	60		50	100	µV
Long-Term Input Offset Voltage Stability[1]			0.3			0.4			*		µV/Mo
Offset Adjustment Range	R_{TRIM} = 20kΩ		±3			*			*		mV
Power Supply Rejection Ratio	V_S = ±3V to ±18V		0.7	3		*	*		*	*	µV/V
INPUT BIAS CURRENT											
Input Offset Current			0.3	1.5		*	2.8		*	*	nA
Input Bias Current			1.2	±2		*	±2.8		*	*	nA
NOISE											
Input Noise Voltage	0.1Hz to 10Hz[2]		0.35	0.6		0.38	0.65		*	*	µVp-p
Input Noise Voltage Density	f = 10Hz[2]		8.5	18		*	20		*	*	nV/√Hz
	f = 100Hz[2]		7.5	13		*	13.5		*	*	nV/√Hz
	f = 1000Hz[2]		7.5	11		*	11.5		*	*	nV/√Hz
Input Noise Current	0.1Hz to 10Hz		35			*			*		pAp-p
Input Noise Current Density	f = 10Hz		0.73			*			*		pA/√Hz
	f = 100Hz		0.26			*			*		pA/√Hz
	f = 1000Hz		0.22			*			*		pA/√Hz
INPUT RESISTANCE											
Differential Input Resistance[3]		26	45		18.5	*		*	*		MΩ
Common-mode Input Resistance			200			*			*		GΩ
INPUT VOLTAGE RANGE											
Common Mode Input Range		±13	±14		*	*		*	*		V
Common-Mode Rejection	V_{CM} = ±13V		0.1	1		*	1.6		*	*	µV/V
OPEN-LOOP GAIN											
Large-Signal Voltage Gain	R_L ≥ 2kΩ, V_O = ±10V	5000	12000		2000	6000		*	*		V/mV
OUTPUT											
Output Voltage Swing	R_L ≥ 10kΩ	±13.5	±14		*	*		*	*		V
	R_L ≥ 2kΩ	±12.5	±13		*	*		*	*		V
	R_L ≥ 1kΩ	±12	±12.5		*	*		*	*		V
Open-Loop Output Resistance			60			*			*		Ω
FREQUENCY RESPONSE											
Slew Rate	R_L ≥ 2kΩ	0.1	0.3		*	*		*	*		V/µs
Closed-Loop Bandwidth	AVCL = +1	0.4	0.6		*	*		*	*		MHz
POWER SUPPLY											
Power Consumption	V_S = ±15V, No Load		50	60		*	*		*	*	mW
	V_S = ±3V, No Load		3.5	4.5		*	*		*	*	mW

ELECTRICAL

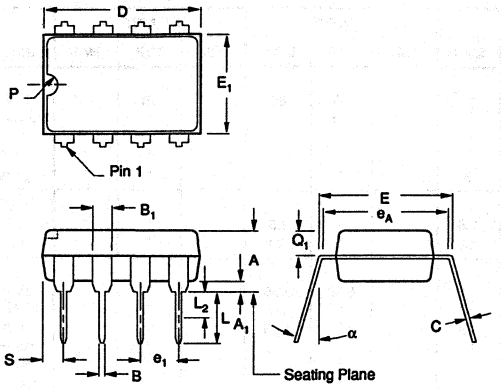
At V_S = ±15V, –25°C ≤ T_A ≤ +85°C for OPA77EZ and OPA77FZ, 0°C ≤ T_A ≤ +70°C for OPA77FP and OPA77GP, unless otherwise noted.

OFFSET VOLTAGE											
Input Offset Voltage	Z Package		10	45		20	100		*	*	µV
	P Package		10	55		20	100		80	150	µV
Average Input Offset[4]	Z Package		0.1	0.3		0.2	0.6		*	*	µV/°C
Voltage Drift	P Package		0.3	0.6		0.4	1		0.7	1.2	µV/°C
Power Supply Rejection Ratio	V_S = ±3V to ±18V		1	3		*	5		*	*	µV/V
INPUT BIAS CURRENT											
Input Offset Current			0.5	2.2		*	4.5		*	*	nA
Avg Input Offset Current Drift[5]			1.5	40		*	85		*	*	pA/°C
Input Bias Current			2.4	±4		*	±6		*	*	nA
Avg Input Bias Current Drift[5]			8	40		15	60		*	*	pA/°C
INPUT VOLTAGE RANGE											
Common Mode Input Range		±13	±13.5		*	*		*	*		V
Common-Mode Rejection	V_{CM} = ±13V		0.1	1		*	3		*	*	µV/V
OPEN-LOOP GAIN											
Large-Signal Voltage Gain	R_L ≥ 2kΩ, V_O = ±10V	2000	6000		1000	4000		*	*		V/mV
OUTPUT											
Output Voltage Swing	R_L ≥ 2kΩ	±12	±13		*	*		*	*		V
POWER SUPPLY											
Power Consumption	V_S = ±15V, No Load		60	75		*	*		*	*	mW

* Same as specification for product to left. NOTES: (1) Long-Term Input Offset Voltage Stability refers to the averaged trend line of V_{OS} vs time over extended period after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically 2.5µV. (2) Sample tested. (3) Guaranteed by design. (4) OPA77E: TCV_{OS} is 100% tested on Z package. (5) Guaranteed by end-point limits.

MECHANICAL

P Package — 8-Pin Plastic DIP

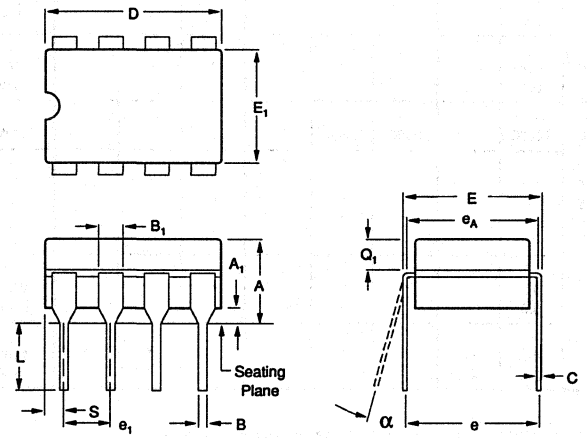


DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.155	.200	3.94	5.08
A1	.020	.050	0.51	1.27
B	.014	.020	0.36	0.51
B1	.045	.065	1.14	1.65
C	.008	.012	0.20	0.30
D (1)	.370	.400	9.40	10.16
E	.300	.325	7.62	8.26
E1	.240	.260	6.10	6.60
e1	.100 BASIC		2.54 BASIC	
eA	.300 BASIC		7.62 BASIC	
L	.125	.150	3.18	3.81

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
L2 (2)	0	.030	0.00	0.76
α	0°	15°	0°	15°
P	.015	.050	0.38	1.270
Q1	.040	.075	1.02	1.91
S (1)	.015	.050	0.38	1.27

(1) Not JEDEC Std.
(2) e_1 and e_A apply in zone L_2 when unit installed.
NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

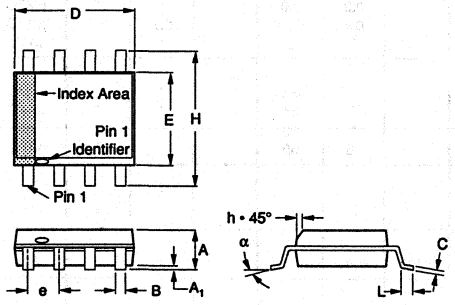
Z Package — 8-Pin SSI Ceramic DIP



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.160	.214	4.07	5.44
A1	.009	.060	0.23	1.52
B	.015	.021	.38	.54
B1	.045	.060	1.14	1.52
C	.008	.012	0.20	0.30
D	.365	.395	9.27	10.03
E	.290	.320	7.37	8.13
E1	.245	.255	6.22	6.48
e1	.100 BASIC		2.54 BASIC	
eA	.268	.288	6.81	7.31
L	.125	.175	3.18	4.45
α	0°	15°	0°	15°
Q1	.180	.220	4.57	5.59
S	—	.098	—	2.49
e	.290	.320	7.37	8.13

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

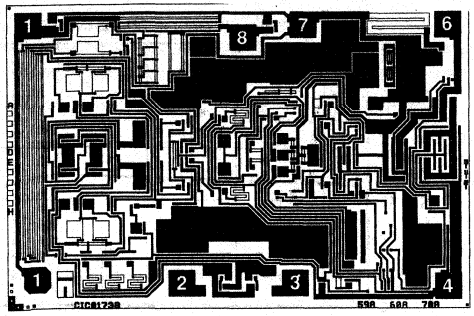
U Package — 8-Pin SO-8 Surface Mount



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.054	.068	1.37	1.73
A1	.004	.009	0.10	0.23
B	.014	.019	0.36	0.48
C	.008	.0098	0.20	0.25
D	.189	.196	4.80	4.98
E	.150	.157	3.81	3.99
e	.050 BASIC		1.27 BASIC	
H	.229	.244	5.82	6.20
h	.010	.019	0.25	0.48
L	.016	.050	0.41	1.27
N	8		8	
α	0°	8°	0°	8°

NOTES:
1. Dimensioning and tolerancing per ANSI Y14.5M–1982.
2. "D" and "E" are reference datums and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm (.086 in.)
3. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the cross-hatched area.
4. "L" is the length of the terminal for soldering to a substrate.
5. "N" is the number of terminal positions.

DICE INFORMATION



OPA177/77 DIE TOPOGRAPHY

PAD	FUNCTION
1	Offset Trim
2	–In
3	+In
4	V–
5	NC
6	V_O
7	V+
8	Offset Trim

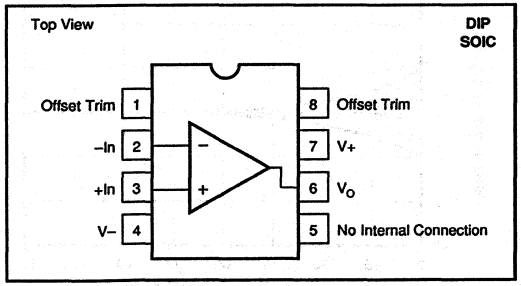
Substrate Bias: $-V_S$
NC: No Connection.

MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	63 x 92 ±5	1.60 x 2.34 ±0.13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.10 x 0.10
Backing	Gold	

See "DICE PRODUCTS" Section 17 in Data Book Supplement Volume 33c, or contact Burr-Brown for current information.

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage	±22V
Differential Input Voltage	±30V
Input Voltage	$\pm V_S$
Output Short Circuit	Continuous
Operating Temperature:	
Ceramic DIP (Z)	–55°C to +125°C
Plastic DIP (P), SO-8 (S)	–40°C to +85°C
Storage Temperature:	
Ceramic DIP (Z)	–65°C to +150°C
Plastic DIP (P), SO-8 (S)	–65°C to +125°C
Junction Temperature	+150°C
Lead Temperature (soldering, 10s) P, Z packages	+300°C
(soldering, 3s) S package	+260°C

ORDERING INFORMATION

MODEL	PACKAGE	TEMP. RANGE
OPA177FP	8-Pin Plastic DIP	–40°C to +85°C
OPA177GP	8-Pin Plastic DIP	–40°C to +85°C
OPA177GS	SO-8 Surface-Mount	–40°C to +85°C
OPA177EZ	8-Pin Ceramic DIP	–40°C to +85°C
OPA177FZ	8-Pin Ceramic DIP	–40°C to +85°C
OPA177GZ	8-Pin Ceramic DIP	–40°C to +85°C
OPA77FP	8-Pin Plastic DIP	0°C to +70°C
OPA77GP	8-Pin Plastic DIP	0°C to +70°C
OPA77EZ	8-Pin Ceramic DIP	–25°C to +85°C
OPA77FZ	8-Pin Ceramic DIP	–25°C to +85°C

ELECTROSTATIC DISCHARGE SENSITIVITY

Any integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. ESD can cause damage ranging from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

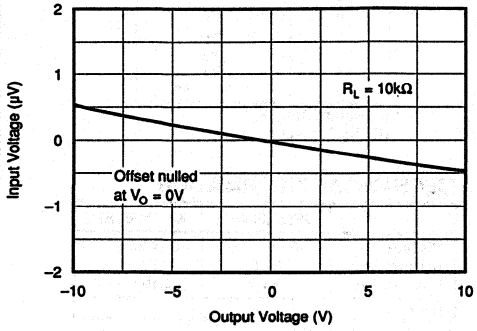
Burr-Brown's standard ESD test method consists of five 1000V positive and negative discharges (100pF in series with 1.5kΩ) applied to each pin.

Failure to observe proper handling procedures could result in small changes to the OPA177's input bias current.

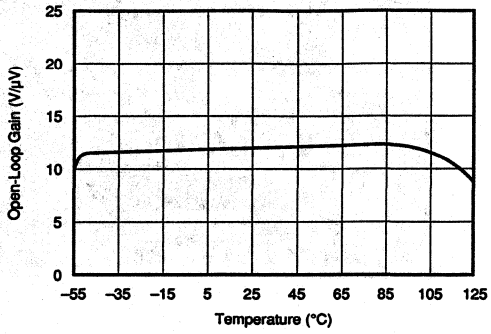
TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_S = ±15V unless otherwise noted.

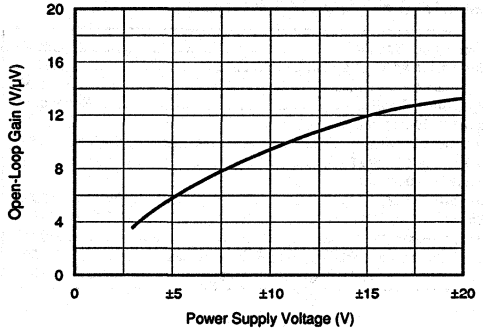
GAIN LINEARITY
(NORMALIZED INPUT VOLTAGE vs OUTPUT VOLTAGE)



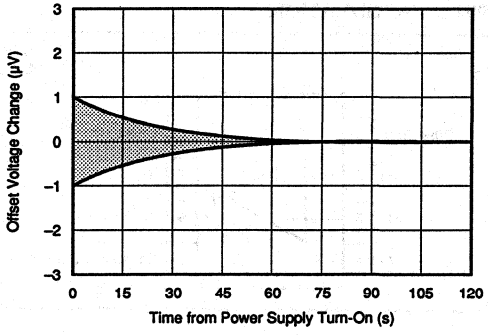
OPEN-LOOP GAIN vs TEMPERATURE



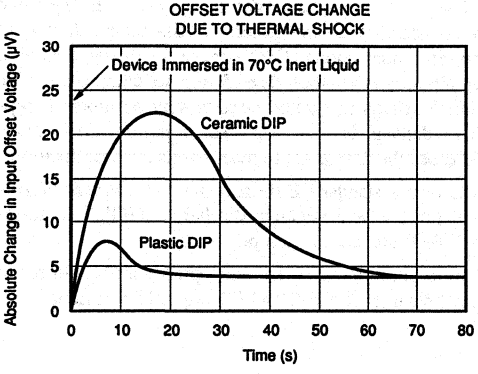
OPEN-LOOP GAIN vs POWER SUPPLY VOLTAGE



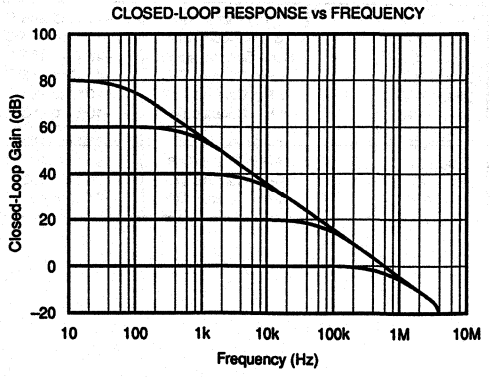
WARM-UP OFFSET VOLTAGE DRIFT



OFFSET VOLTAGE CHANGE
DUE TO THERMAL SHOCK



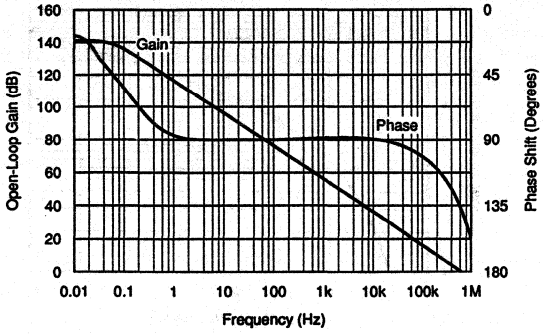
CLOSED-LOOP RESPONSE vs FREQUENCY



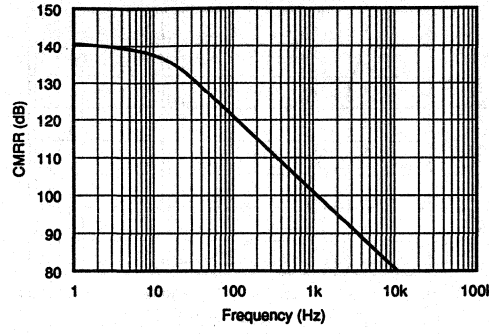
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_S = ±15V unless otherwise noted.

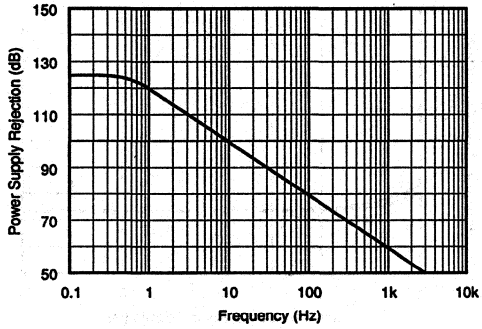
OPEN-LOOP GAIN/PHASE vs FREQUENCY



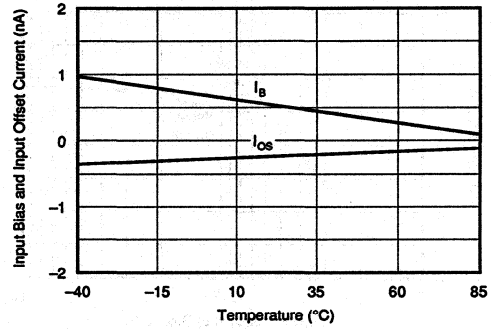
CMRR vs FREQUENCY



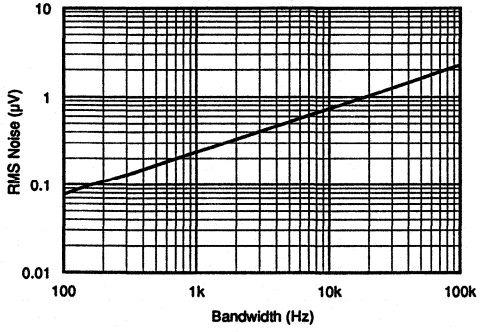
POWER SUPPLY REJECTION vs FREQUENCY



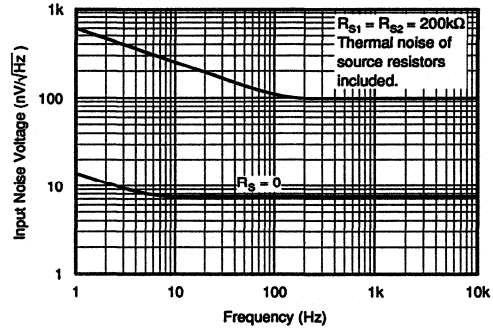
INPUT BIAS AND INPUT OFFSET CURRENT vs TEMPERATURE



TOTAL NOISE vs BANDWIDTH (0.1Hz to Frequency Indicated)



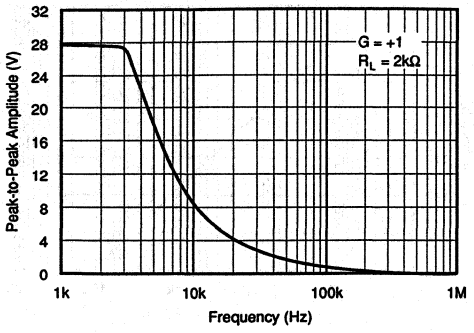
INPUT NOISE VOLTAGE DENSITY vs FREQUENCY



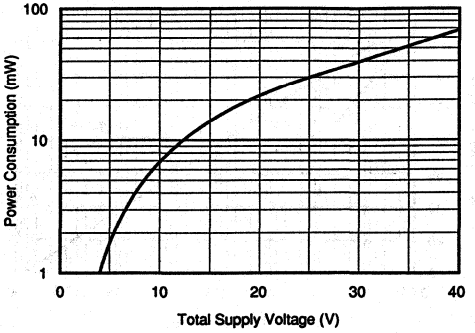
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_S = ±15V unless otherwise noted.

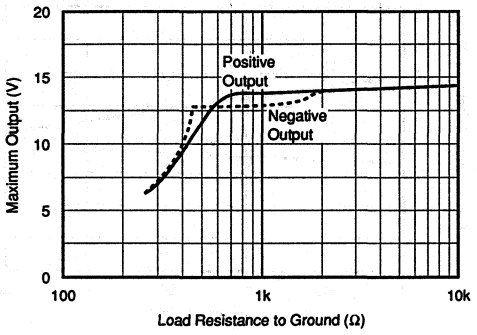
MAXIMUM OUTPUT SWING vs FREQUENCY



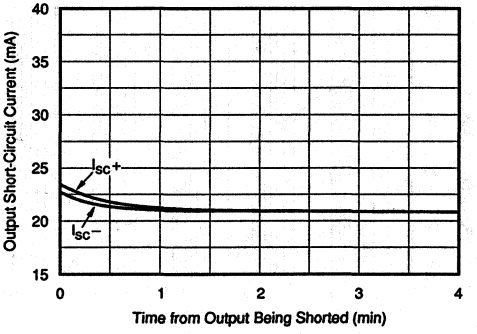
POWER CONSUMPTION vs POWER SUPPLY



MAXIMUM OUTPUT VOLTAGE vs LOAD RESISTANCE



OUTPUT SHORT-CIRCUIT CURRENT vs TIME



APPLICATIONS INFORMATION

The OPA177 is unity-gain stable, making it easy to use and free from oscillations in the widest range of circuitry. Applications with noisy or high impedance power supply lines may require decoupling capacitors close to the device pins. In most cases 0.1µF ceramic capacitors are adequate.

The OPA177 has very low offset voltage and drift. To achieve highest performance, circuit layout and mechanical conditions must be optimized. Offset voltage and drift can be degraded by small thermoelectric potentials at the op amp inputs. Connections of dissimilar metals will generate thermal potential which can mask the ultimate performance of the OPA177. These thermal potentials can be made to cancel by assuring that they are equal in both input terminals.

1. Keep connections made to the two input terminals close together.
2. Locate heat sources as far as possible from the critical input circuitry.
3. Shield the op amp and input circuitry from air currents such as cooling fans.

OFFSET VOLTAGE ADJUSTMENT

The OPA177 and OPA77 have been laser-trimmed for low offset voltage and drift so most circuits will not require external adjustment. Figure 1 shows the optional connection of an external potentiometer to adjust offset voltage. This adjustment should not be used to compensate for offsets created elsewhere in a system since this can introduce excessive temperature drift.

INPUT PROTECTION

The inputs of the OPA177 and OPA77 are protected with 500Ω series input resistors and diode clamps as shown in the simplified circuit diagram. The inputs can withstand ±30V differential inputs without damage. The protection diodes will, of course, conduct current when the inputs are overdriven. This may disturb the slewing behavior of unity-gain follower applications, but will not damage the op amp.

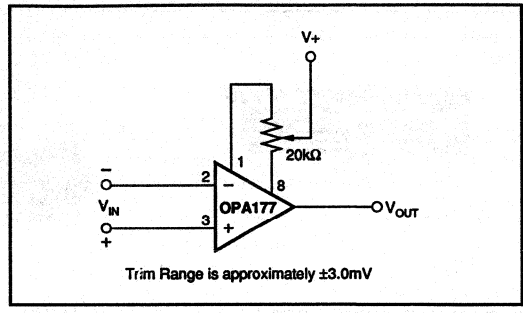


FIGURE 1. Optional Offset Nulling Circuit.

NOISE PERFORMANCE

The noise performance of the OPA177 and OPA77 is optimized for circuit impedances in the range of 2kΩ to 50kΩ. Total noise in an application is a combination of the op amp's input voltage noise and input bias current noise reacting with circuit impedances. For applications with higher source impedance, the OPA627 FET-input op amp will generally provide lower noise. For very low impedance applications, the OPA27 will provide lower noise.

INPUT BIAS CURRENT CANCELLATION

The input stage base current of the OPA177 is internally compensated with an equal and opposite cancellation current. The resulting input bias current is the difference between the input stage base current and the cancellation current. This residual input bias current can be positive or negative.

When the bias current is cancelled in this manner, the input bias current and input offset current are approximately the same magnitude. As a result, it is not necessary to balance the DC resistance seen at the two input terminals (Figure 2). A resistor added to balance the input resistances may actually increase offset and noise.

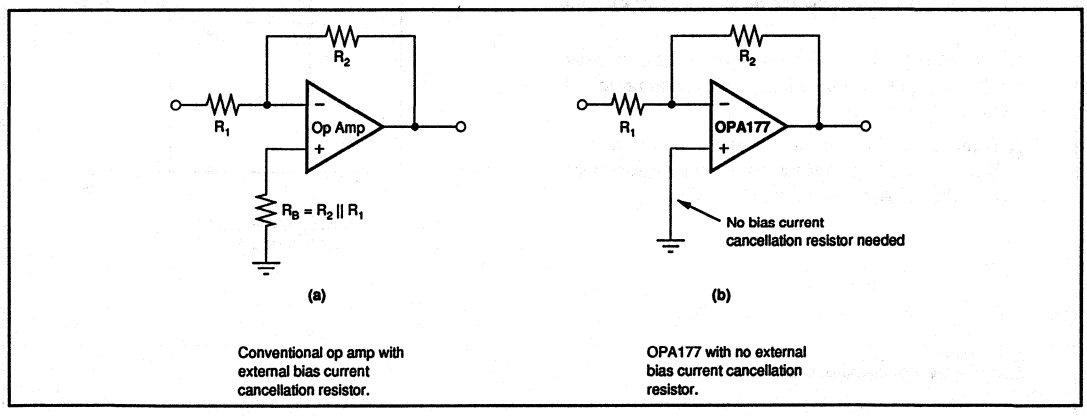
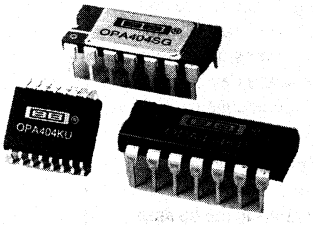


FIGURE 2. Input Bias Current Cancellation.

BURR-BROWN®



OPA404

AVAILABLE IN DIE

Quad High-Speed Precision *Difet*® OPERATIONAL AMPLIFIER

FEATURES

- WIDE BANDWIDTH: 6.4MHz
- HIGH SLEW RATE: 35V/µs
- LOW OFFSET: ±750µV max
- LOW BIAS CURRENT: ±4pA max
- LOW SETTLING: 1.5µs to 0.01%
- STANDARD QUAD PINOUT

APPLICATIONS

- PRECISION INSTRUMENTATION
- OPTOELECTRONICS
- SONAR, ULTRASOUND
- PROFESSIONAL AUDIO EQUIPMENT
- MEDICAL EQUIPMENT
- DETECTOR ARRAYS

DESCRIPTION

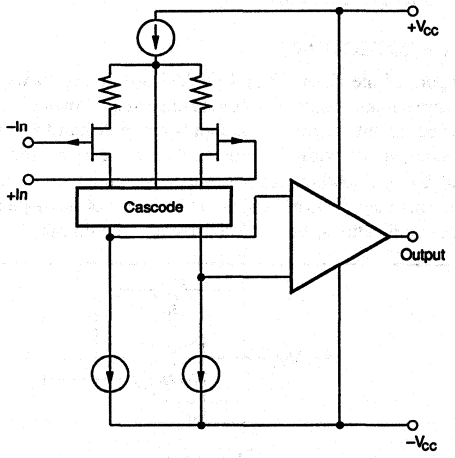
The OPA404 is a high performance monolithic ***Difet***® (dielectrically-isolated FET) quad operational amplifier. It offers an unusual combination of very-low bias curent together with wide bandwidth and fast slew rate.

Noise, bias current, voltage offset, drift, and speed are superior to BIFET® amplifiers.

Laser-trimming of thin-film resistors gives very low offset and drift—the best available in a quad FET op amp.

The OPA404's input cascode design allows high precision input specifications and uncompromised high-speed performance.

Standard quad op amp pin configuration allows upgrading of existing designs to higher performance levels. The OPA404 is unity-gain stable.



OPA404 Simplified Circuit
(Each Amplifier)

Difet®, Burr-Brown Corp.
BIFET®, National Semiconductor Corp.

International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL

At V_{CC} = ±15VDC and T_A = +25°C unless otherwise noted.

PARAMETER	CONDITIONS	OPA404AG, KP, KU			OPA404BG			OPA404SG			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
INPUT											
NOISE[1]											
Voltage: f_O = 10Hz			32			*			*		nV/√Hz
f_O = 100Hz			19			*			*		nV/√Hz
f_O = 1kHz			15			*			*		nV/√Hz
f_O = 10kHz			12			*			*		nV/√Hz
f_B = 10Hz to 10kHz			1.4			*			*		µVrms
f_B = 0.1Hz to 10Hz			0.95			*			*		µVp-p
Current: f_B = 0.1Hz to 10Hz			12			*			*		fA, p-p
f_O = 0.1Hz thru 20kHz			0.6			*			*		fA/√Hz
OFFSET VOLTAGE											
Input Offset Voltage	V_{CM} = 0VDC		±260	±1mV		*	±750		*	*	µV
KP, KU			±750	±2.5mV							µV
Average Drift	$T_A = T_{MIN}$ to T_{MAX}		±3			*			*		µV/°C
KP, KU			±5								µV/°C
Supply Rejection	±V_{CC} = 12V to 18V	80	100		86	*		*	*		dB
KP, KU		76	100								dB
Channel Separation	100Hz, R_L = 2kΩ		125			*			*		dB
BIAS CURRENT											
Input Bias Current	V_{CM} = 0VDC		±1	±8		*	±4		*	*	pA
KP, KU			±1	±12							pA
OFFSET CURRENT											
Input Offset Current	V_{CM} = 0VDC		0.5	8		*	4		*	*	pA
KP, KU			0.5	12							pA
IMPEDANCE											
Differential			10^{13} || 1			*			*		Ω || pF
Common-Mode			10^{14} || 3			*			*		Ω || pF
VOTAGE RANGE											
Common-Mode Input Range		±10.5	+13, –11		*	*		*	*		V
Common-Mode Rejection	V_{IN} = ±10VDC	88	100		92	*		*	*		dB
KP, KU		84	100								dB
OPEN-LOOP GAIN, DC											
Open-Loop Voltage Gain	R_L ≥ 2kΩ	88	100		92	*		*	*		dB
FREQUENCY RESPONSE											
Gain Bandwidth	Gain = 100	4	6.4		5	*		*	*		MHz
Full Power Response	20Vp-p, R_L = 2kΩ		570			*			*		kHz
Slew Rate	V_O = ±10V, R_L = 2kΩ	24	35		28	*		*	*		V/µs
Settling Time: 0.1%	Gain = –1, R_L = 2kΩ		0.6			*			*		µs
0.01%	C_L = 100 pF, 10V Step		1.5			*			*		µs
RATED OUTPUT											
Voltage Output	R_L = 2kΩ	±11.5	+13.2, –13.8		*	*		*	*		V
Current Output	V_O = ±10VDC	±5	±10		*	*		*	*		mA
Output Resistance	1MHz, Open Loop		80			*			*		Ω
Load Capacitance Stability	Gain = +1		1000			*			*		pF
Short Circuit Current		±10	±18	±20	*	*	*	*	*	*	mA
POWER SUPPLY											
Rated Voltage			±15			*			*		VDC
Voltage Range, Derated Performance		±5		±18	*		*	*		*	VDC
Current, Quiescent	I_O = 0mADC		9	10		*	*		*	*	mA
TEMPERATURE RANGE											
Specification	Ambient Temperature	–25		+85	*		*	–55		+125	°C
KP, KU		0		+70							°C
Operating	Ambient Temperature	–55		+125	*		*	*		*	°C
KP, KU		–25		+85							°C
Storage	Ambient Temperature	–65		+150	*		*	*		*	°C
KP, KU		–40		+125							°C
θ Junction-Ambient			100			*			*		°C/W
KP, KU			120/100								°C/W

*Specificaions same as OPA404AG.

NOTE: (1) Noise testing available—inquire.

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ELECTRICAL (FULL TEMPERATURE RANGE SPECIFICATIONS)

At V_{CC} = ±15VDC and $T_A = T_{MIN}$ to T_{MAX} unless otherwise noted.

PARAMETER	CONDITIONS	OPA404AG, KP, KU			OPA404BG			OPA404SG			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
TEMPERATURE RANGE											
Specification Range	Ambient Temperature	–25		+85	*		*	–55		+125	°C
KP, KU		0		+70							°C
INPUT											
OFFSET VOLTAGE											
Input Offset Voltage	V_{CM} = 0VDC		±450	2mV		*	±1.5mV		±550	±2.5mV	µV
KP KU			±1	±3.5							mV
Average Drift			±3			*			*		µV/°C
KP, KU			±5								µV/°C
Supply Rejection		75	96		80	*		70	93		dB
BIAS CURRENT											
Input Bias Current	V_{CM} = 0VDC		±32	±200		*	±100		±500	±5nA	pA
OFFSET CURRENT											
Input Offset Current	V_{CM} = 0VDC		17	100		*	50		260	2.5nA	pA
VOLTAGE RANGE											
Common-Mode Input Range		±10	±12.7, –10.6		*	*		±10	+12.6, –10.5		V
Common-Mode Rejection	V_{IN} = ±10VDC	82	99		86	*		80	88		dB
KP, KU		80	99								dB
OPEN-LOOP GAIN, DC											
Open-Loop Voltage Gain	$R_L \geq 2k\Omega$	82	94		86	*		80	88		dB
RATED OUTPUT											
Voltage Output	R_L = 2kΩ	±11.5	±12.9, –13.8		*	*		±11	+12.7, –13.8		V
Current Output	V_O = ±10VDC	±5	±9		*	*		*	±8		mA
Short Circuit Current	V_O = 0VDC	±5	±12	±30	*	*	*	±8	±10	*	mA
POWER SUPPLY											
Current, Quiescent	I_O = 0mADC		9.3	10.5		*	*		9.4	11	mA

NOTE: Specification same as OPA404AG.

ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE
OPA404KP	14-Pin Plastic DIP	0°C to +70°C
OPA404KU	16-Pin Plastic SOIC	0°C to +70°C
OPA404AG	14-Pin Ceramic DIP	–25°C to +85°C
OPA404BG	14-Pin Ceramic DIP	–25°C to +85°C
OPA404SG	14-Pin Ceramic DIP	–55°C to +125°C

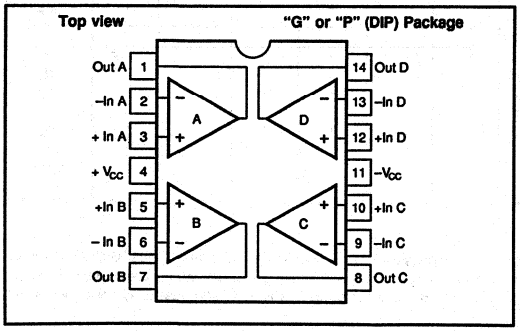
ABSOLUTE MAXIMUM RATINGS

Supply ..... ±18VDC
Internal Power Dissipation[1] 1000mW
Differential Input Voltage[2] ..... ±36VDC
Input Voltage Range[2] ..... ±18VDC
Storage Temperature Range ..... P, U = –40/+125°C, G = –65°C / +150°C
Operating Temperature Range ..... P, U = –25/+85°C, G = –55°C / +125°C
Lead Temperature (soldering, 10s) ..... 300°C
SOIC (soldering, 3s) ..... +260°C
Output Short-Circuit Duration[3] ..... Continuous
Junction Temperature ..... +175°C

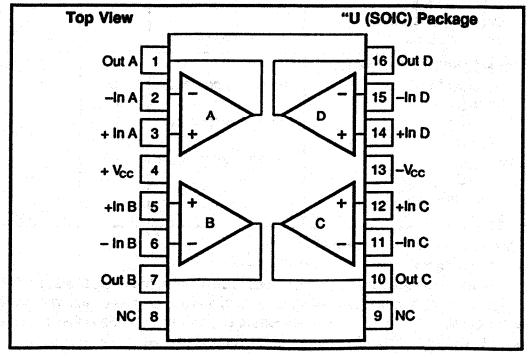
NOTES:(1) Packages must be derated based on θ_{JC} = 30°C/W or θ_{JA} = 120°C/W. (2) For supply voltages less than ±18VDC the absolute maximum input voltage is equal to: 18V > V_{IN} > $-V_{CC}$ – 8V. See Figure 2. (3) Short circuit may be to power supply common only. Rating applies to +25°C ambient. Observe dissipation limit and T_J.

PIN CONFIGURATION

Top view "G" or "P" (DIP) Package

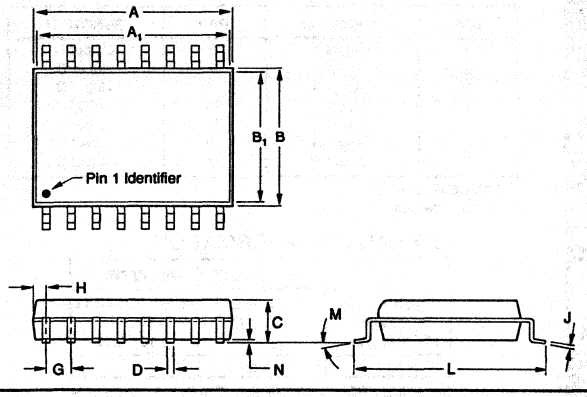


Top View "U (SOIC) Package



MECHANICAL

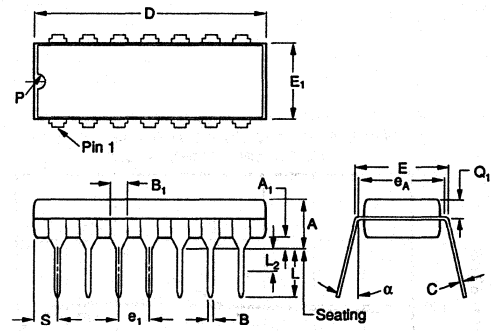
U Package — 16-Pin SOIC



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.400	.416	10.16	10.57
A1	.388	.412	9.86	10.46
B	.286	.302	7.26	7.67
B1	.268	.286	6.81	7.26
C	.093	.109	2.36	2.77
D	.015	.020	0.38	0.51
G	.050 BASIC		1.27 BASIC	
H	.022	.038	0.56	0.97
J	.008	.012	0.20	0.30
L	.391	.421	9.93	10.69
M	5° TYP		5° TYP	
N	.000	.012	0.00	0.30

NOTE: Leads in true position within 0.010" (0.25mm) R at MMC at seating plane.

P Package — 14-Pin Plastic DIP



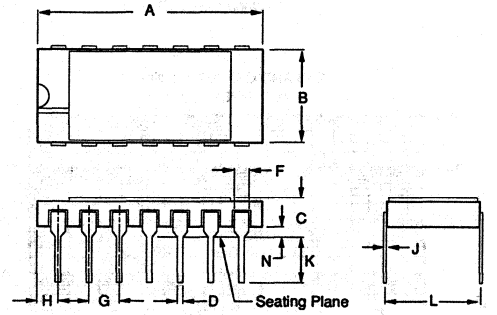
DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.120	.160	3.048	4.064
A1	.015	.065	.381	1.651
B	.014	.020	.355	.508
B1	.050	.065	1.270	1.651
C	.008	.012	.203	.304
D	.745	.770	18.923	19.558
E	.300	.325	7.620	8.255
E1	.240	.260	6.096	6.604
e1	.100 BASIC		2.540 BASIC	
eA	.300 BASIC		7.620 BASIC	
L	.125	.150	3.175	3.810

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
L2 (4)	0	.030	0	.762
α	0°	15°	0°	15°
N (1)	14		14	
N1 (2)	0		0	
P	—	.050	—	1.270
Q1	.050	.085	1.270	2.159
S (3)	.065	.090	1.651	2.286

(1) N = Total number of pins.
(2) N_1 = Total number of missing pins.
(3) Not per JEDEC Std.
(4) e_1 and e_A applies in zone L_2 when unit installed.

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

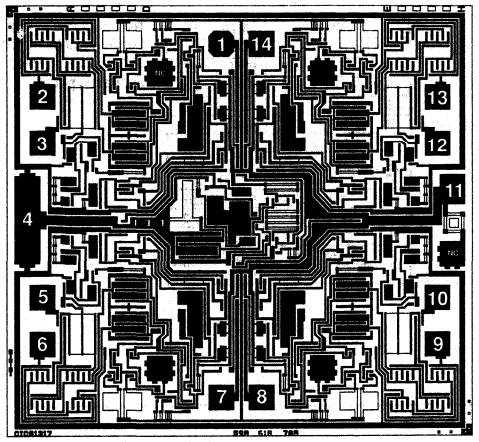
G Package — 14-Pin Ceramic DIP



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.692	.708	17.58	17.98
B	.300	.320	7.62	8.13
C	.102	.138	2.59	3.51
D	.016	.020	0.41	0.51
F	.042	.052	1.07	1.32
G	.100 BASIC		2.54 BASIC	
H	.052	.058	1.32	1.47
J	.008	.012	0.20	0.30
K	.125	.180	3.18	4.57
L	.300 BASIC		7.62 BASIC	
N	.025	.046	0.64	1.14

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

DICE INFORMATION



OPA404 DIE TOPOGRAPHY

PAD	FUNCTION	PAD	FUNCTION
1	Output A	8	Output C
2	–Input A	9	–Input C
3	+Input A	10	+Input C
4	$+V_{CC}$	11	$-V_{CC}$
5	+Input B	12	+Input D
6	–Input B	13	–Input D
7	Output B	14	Output D

Substrate Bias: $-V_{CC}$
NC: No connection

MECHANICAL INFORMATION

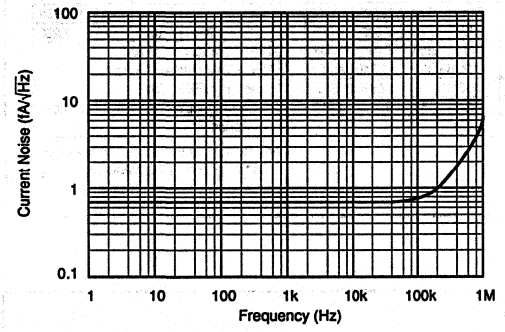
	MILS (0.001")	MILLIMETERS
Die Size	97 x 91 ±5	2.46 x 2.31 ±0.13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.10 x 0.10
Backing	None	

See "DICE PRODUCTS" Section 17 in Data Book Supplement Volume 33c, or contact Burr-Brown for current information.

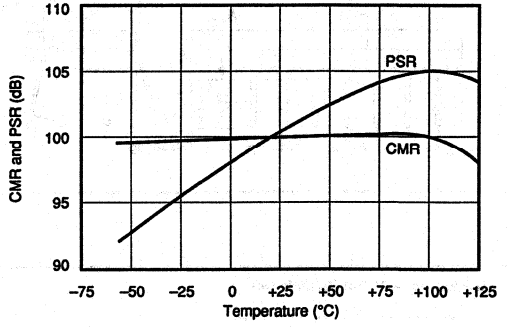
TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_{CC} = ±15VDC unless otherwise noted.

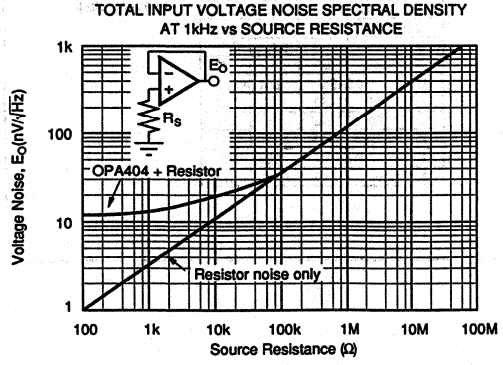
INPUT VOLTAGE NOISE SPECTRAL DENSITY



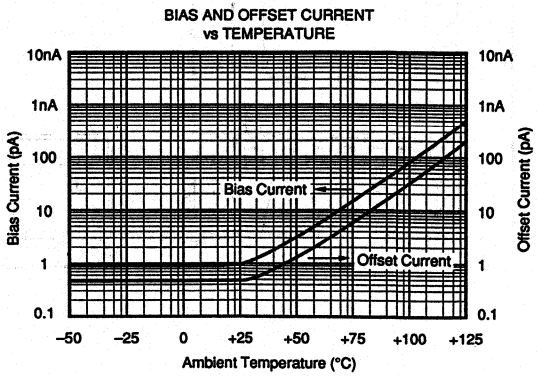
POWER SUPPLY REJECTION AND COMMON-MODE REJECTION vs TEMPERATURE



TOTAL INPUT VOLTAGE NOISE SPECTRAL DENSITY AT 1kHz vs SOURCE RESISTANCE



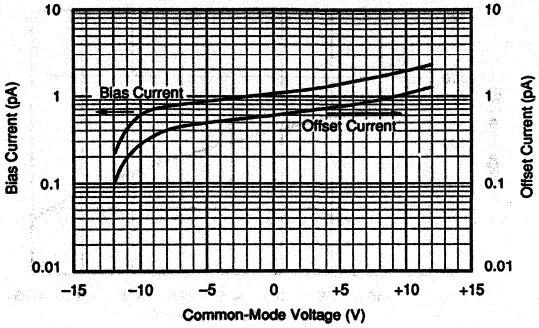
BIAS AND OFFSET CURRENT vs TEMPERATURE



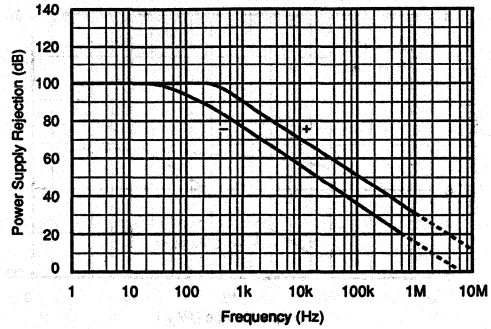
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_{CC} = ±15VDC unless otherwise noted.

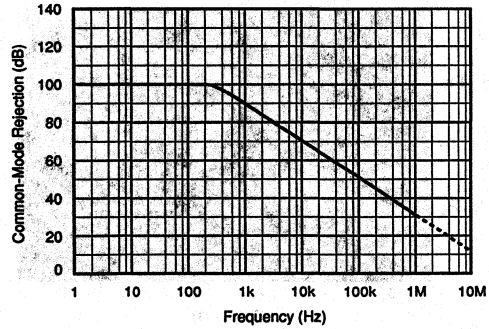
BIAS AND OFFSET CURRENT
vs INPUT COMMON-MODE VOLTAGE



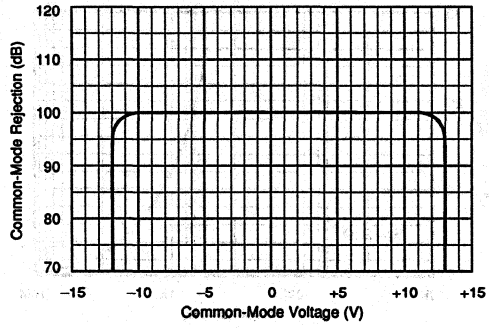
POWER SUPPLY REJECTION
vs FREQUENCY



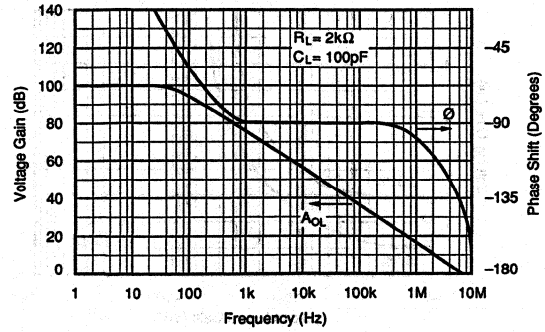
COMMON-MODE REJECTION
vs FREQUENCY



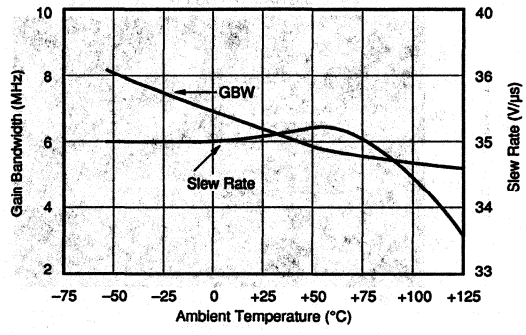
COMMON-MODE REJECTION
vs INPUT COMMON-MODE VOLTAGE



OPEN-LOOP FREQUENCY RESPONSE



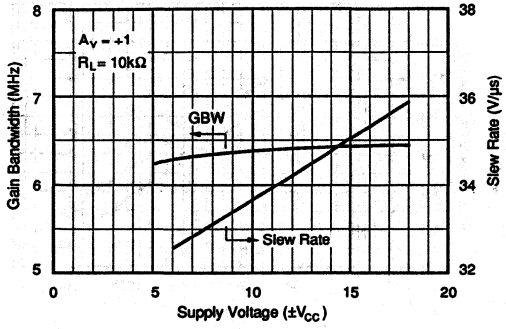
GAIN-BANDWIDTH AND SLEW RATE
vs TEMPERATURE



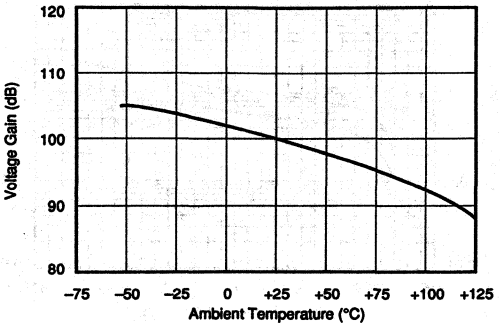
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_{CC} = ±15VDC unless otherwise noted.

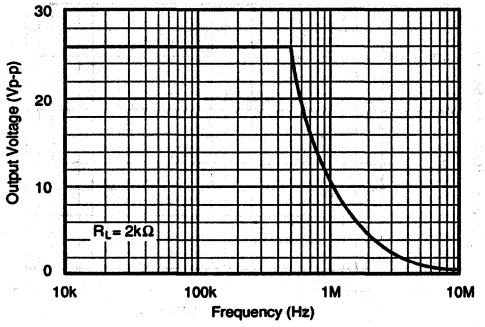
GAIN-BANDWIDTH AND SLEW RATE vs SUPPLY VOLTAGE



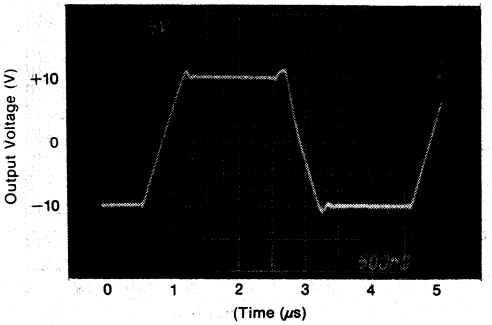
OPEN-LOOP GAIN vs TEMPERATURE



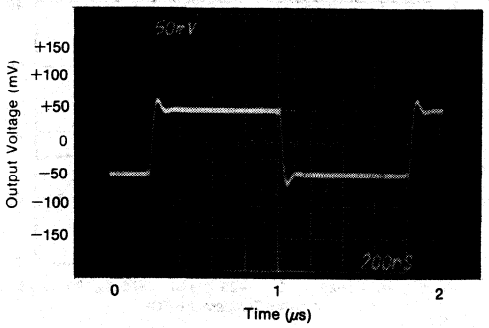
MAXIMUM OUTPUT VOTAGE SWING vs FREQUENCY



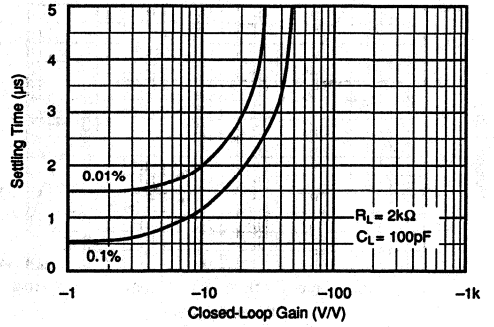
LARGE SIGNAL TRANSIENT RESPONSE



SMALL SIGNAL TRANSIENT RESPONSE



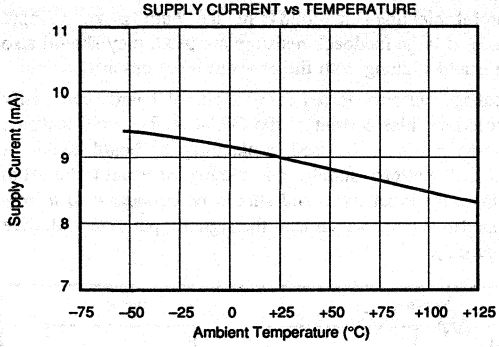
SETTLING TIME vs CLOSED-LOOP GAIN



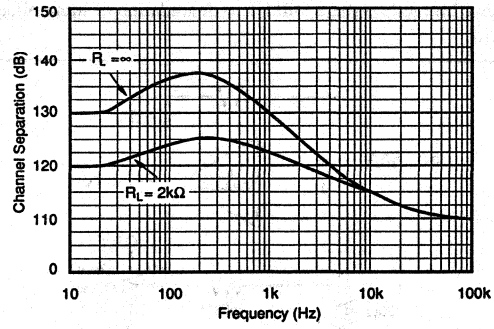
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_{CC} = ±15VDC unless otherwise noted.

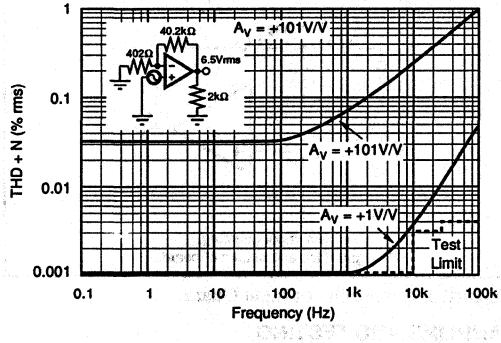
SUPPLY CURRENT vs TEMPERATURE



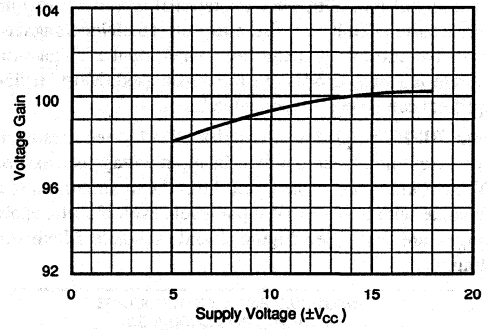
CHANNEL SEPARATION vs FREQUENCY



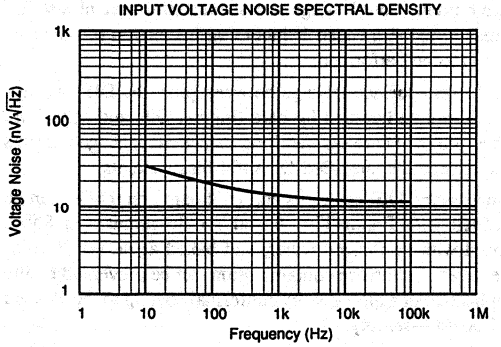
TOTAL HARMONIC DISTORTION vs FREQUENCY



OPEN-LOOP GAIN vs SUPPLY VOLTAGE



INPUT VOLTAGE NOISE SPECTRAL DENSITY



APPLICATIONS INFORMATION

OFFSET VOLTAGE ADJUSTMENT

The OPA404 offset voltage is laser-trimmed and will require no further trim for most applications. If desired, offset voltage can be trimmed by summing (see Figure 1). With this trim method there will be no degradation of input offset drift.

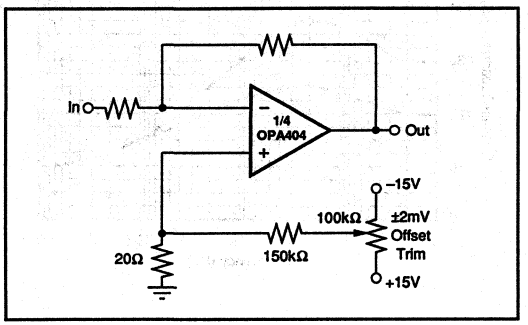


FIGURE 1. Offset Voltage Trim.

INPUT PROTECTION

Conventional monlithic FET operational amplifiers require external current-limiting resistors to protect their inputs against destructive currents that can flow when input FET gate-to-substrate isolation diodes are forward-biased. Most BIFET amplifiers can be destroyed by the loss of $-V_{CC}$.

Unlike BIFET amplifiers, the ***Difet*** OPA404 requires input current limiting resistors only if its input voltage can exceed –8V. A 10kΩ series resistor will limit the input current to a safe value with up to ±15V input levels even if both supply voltages are lost. (See Figure 2 and Absolute Maximum Ratings).

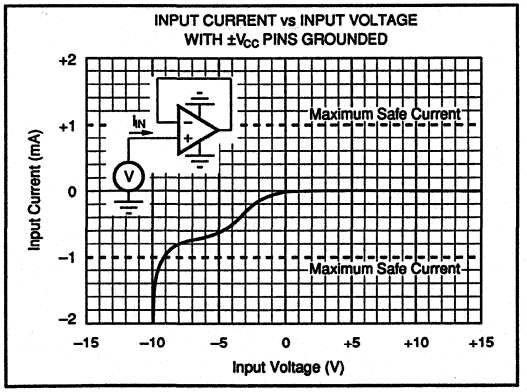


FIGURE 2. Input Current vs Input Voltage with $\pm V_{CC}$ Pins Grounded.

Static damage can cause subtle changes in amplifier input characteristics without necessarily destroying the device. In precision operational amplifiers (both bipolar and FET types), this may cause a noticeable degradation of offset voltage and drift.

Static protection is recommended when handling any precision IC operational amplifier.

GUARDING AND SHIELDING

As in any situation where high impedances are involved, careful shielding is required to reduce "hum" pickup in input leads. If large feedback resistors are used, they should also be shielded along with the external input circuitry.

Leakage currents across printed circuit boards can easily exceed the bias current of the OPA404. To avoid leakage, utmost care must be used in planning the board layout. A "guard" pattern should completely surround the high impedance input leads and should be connected to a low-impedance point which is at the signal input potential. (See Figure 3).

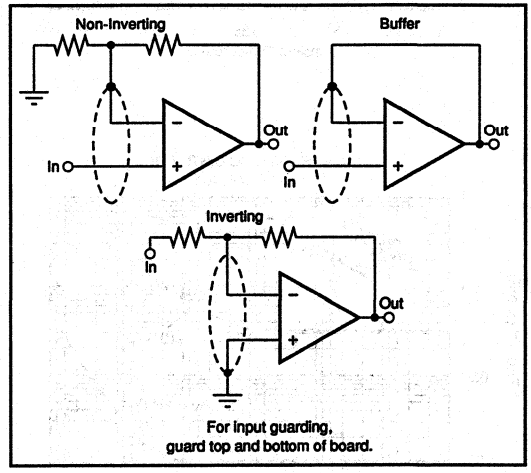


FIGURE 3. Connection of Input Guard.

HANDLING AND TESTING

Measuring the unusually low bias current of the OPA404 is difficult without specialized test equipment; most commercial benchtop testers cannot accurately measure the OPA404 bias current. Low-leakage test sockets and special test fixtures are recommended if incoming inspection of bias current is to be performed.

To prevent surface leakage between pins, the DIP package should not be handled by bare fingers. Oils and salts from fingerprints or careless handling can create leakage currents that exceed the specified OPA404 bias currents.

If necessary, DIP packages and PC board assemblies can be cleaned with Freon TF®, baked for 30 minutes at 85°C, rinsed with de-ionized water, and baked again for 30 minutes at 85°C. Surface contamination can be prevented by the application of a high-quality conformal coating to the cleaned PC board assembly.

BIAS CURRENT CHANGE VERSUS COMMON-MODE VOLTAGE

The input bias currents of most popular BIFET operational amplifiers are affected by common-mode voltage (Figure 4). Higher input FET gate-to-drain voltage causes leakage and ionization (bias) currents to increase. Due to its cascode input stage, the extremely-low bias current of the OPA404 is not compromised by common-mode voltage.

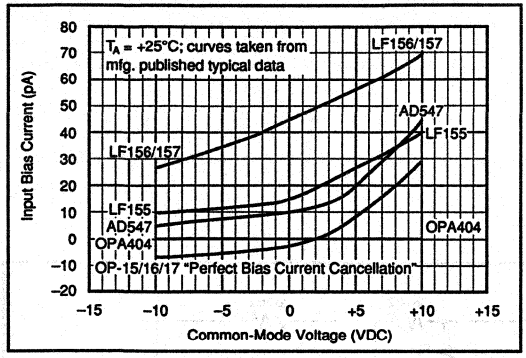


FIGURE 4. Input Bias Current vs Common-Mode Voltage.

APPLICATIONS CIRCUITS

Figures 5 through 11 are circuit diagrams of various applications for the OPA404.

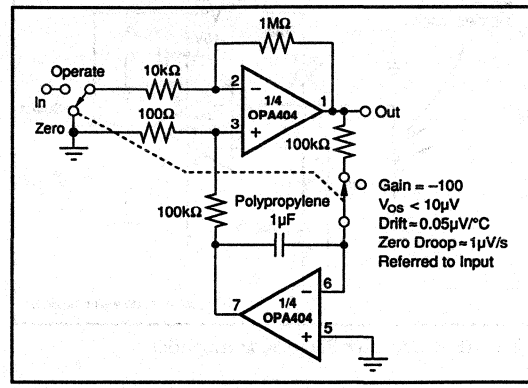


FIGURE 5. Auto-Zero Amplifier.

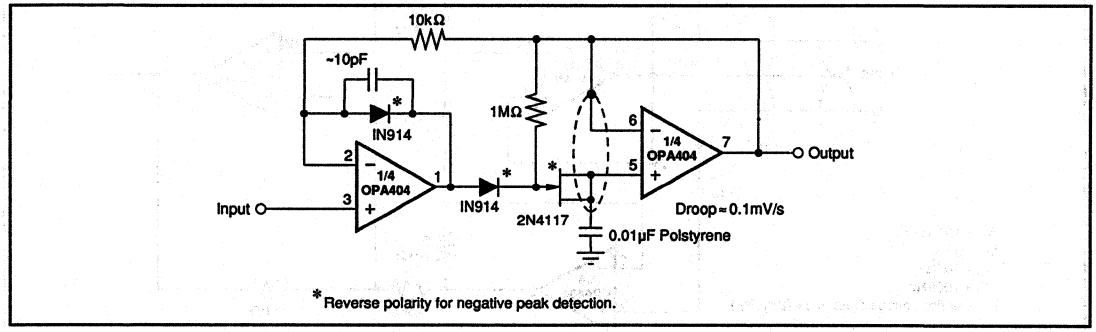


FIGURE 6. Low-Droop Positive Peak Detector.

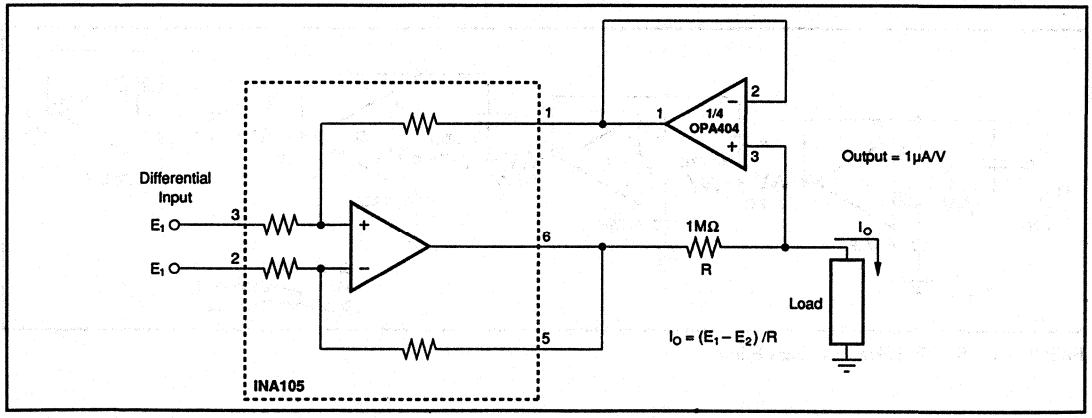


FIGURE 7. Voltage-Controlled Microamp Current Source.

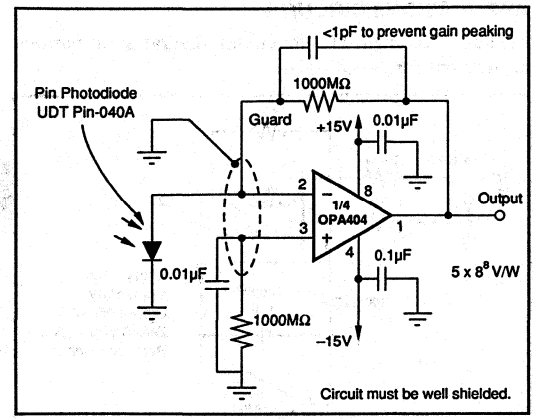


FIGURE 8. Sensitive Photodiode Amplifier.

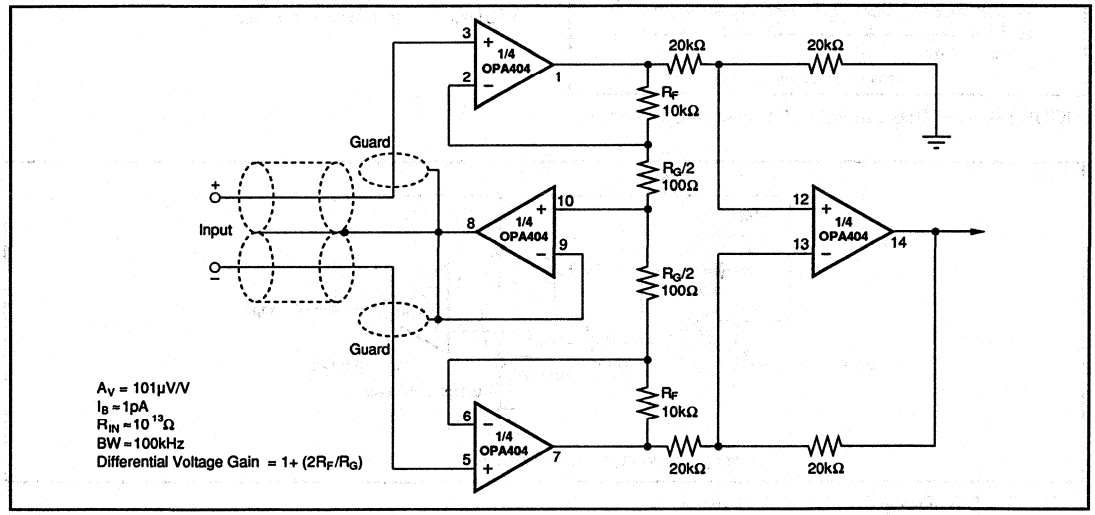


FIGURE 9. FET Instrumentation Amplifier with Shield Driver.

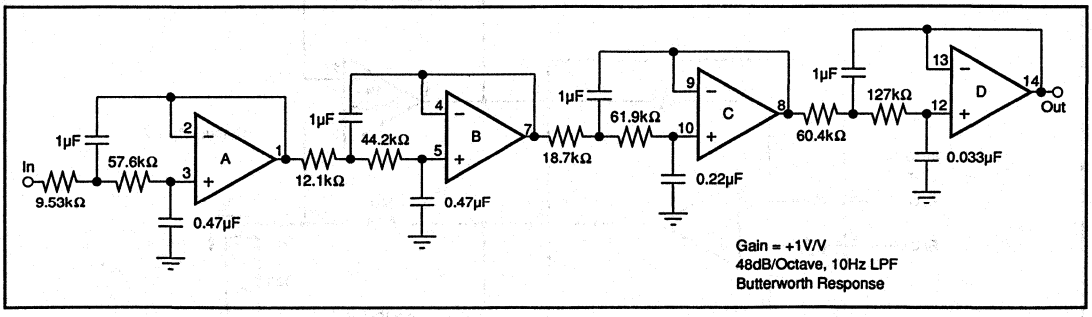


FIGURE 10. 8-Pole 10Hz Low-Pass Filter.

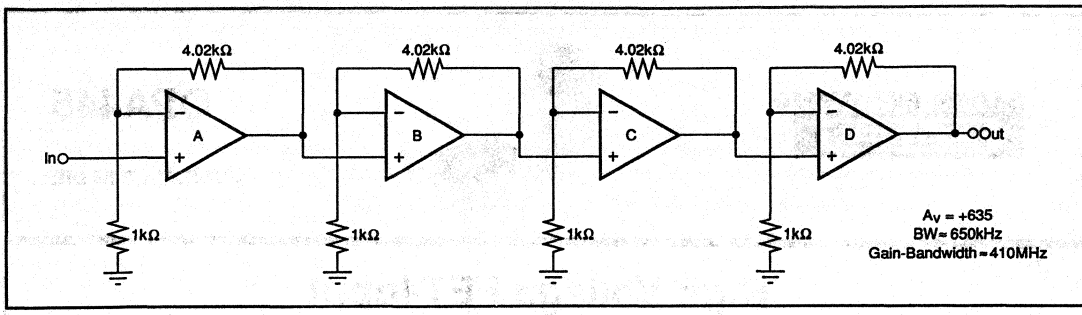
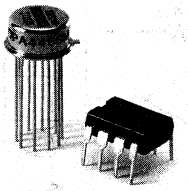


FIGURE 11. Wide-Band Amplifier.

BURR-BROWN®



OPA445

AVAILABLE IN DIE

High Voltage FET-Input OPERATIONAL AMPLIFIER

FEATURES

- WIDE POWER SUPPLY RANGE: ±10V to ±45V
- HIGH SLEW RATE: 10V/µs
- LOW INPUT BIAS CURRENT: 50pA max
- STANDARD-PINOUT TO-99 AND DIP PACKAGES

APPLICATIONS

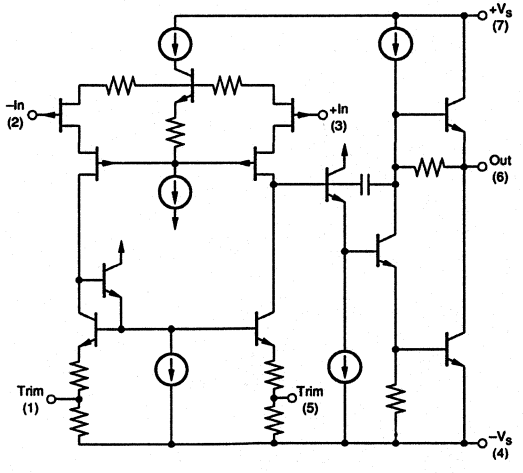
- TEST EQUIPMENT
- HIGH VOLTAGE REGULATORS
- POWER AMPLIFIERS
- DATA ACQUISITION
- SIGNAL CONDITIONING

DESCRIPTION

The OPA445 is a monolithic operational amplifier capable of operation from power supplies up to ±45V and output currents of 15mA. It is useful in a wide variety of applications requiring high output voltage or large common-mode voltage swings.

The OPA445's high slew rate provides wide power-bandwidth response, which is often required for high voltage applications. FET input circuitry allows the use of high impedance feedback networks, thus minimizing their output loading effects. Laser trimming of the input circuitry yields low input offset voltage and drift.

The OPA445 is unity-gain stable and requires no external compensation components. It is available in both industrial (–25°C to +85°C) and military (–55°C to +125°C) temperature ranges.



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Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

PDS-754B

SPECIFICATIONS

ELECTRICAL

At V_S = ±40°C and T_A = +25°C, unless otherwise specified.

PARAMETER	CONDITIONS	OPA445SM			OPA445BM			OPA445AP			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
INPUT											
OFFSET VOLTAGE											
Input Offset Voltage	V_{CM} = 0V		0.5	1.0		1.0	3.0		2.0	5.0	mV
Average Drift	$T_A = T_{MIN}$ to T_{MAX}		*			10			15		µV/°C
Supply Rejection	V_S = ±10V to ±50V	*	*		80	110		*	*		dB
BIAS CURRENT											
Input Bias Current	V_{CM} = 0V		*	*		20	50		50	100	pA
Over Temperature				100			10			20	nA
OFFSET CURRENT											
Input Offset Current	V_{CM} = 0V		*	*		4	10		20	40	pA
Over Temperature				50			5			10	nA
IMPEDANCE											
Differential			*			10^{13} || 1			*		Ω || pF
Common-Mode			*			10^{14} || 3			*		Ω || pF
VOLTAGE RANGE											
Common-Mode Input Range		*			±35			*			V
Common-Mode Rejection	V_{IN} = ±30V,										
	Over Temp.	*	*		80	95		*	*		dB
OPEN-LOOP GAIN, DC											
Open-Loop Voltage Gain	R_L =5kΩ	*	*		100	105		*	*		dB
Over Temperature		*			97			*			dB
FREQUENCY RESPONSE											
Gain Bandwidth	Small Signal		*			2			*		MHz
Full Power Response	35Vp-p, R_L = 5kΩ	*	*		45	55		*	*		kHz
DYNAMIC RESPONSE											
Slew Rate	V_O = ±35V,										
	R_L = 5kΩ	*	*		5	10		*	*		V/µs
Rise Time	V_O = ±200mV		*			100			*		ns
Overshoot	A_V = +1										
	Z_L = 5kΩ || 50pF		*			30			*		%
RATE OUTPUT											
Voltage Output, Over Temp.	R_L = 5kΩ	*			±35			*			V
Current Output	V_O = ±28V	*			±15			*			mA
Output Resistance	DC, Open Loop		*			220			*		Ω
Short Circuit Current			*			±26			*		mA
POWER SUPPLY											
Rated Voltage, $±V_S$			*			±40			*		V
Voltage Range, $±V_S$											
Derated Performance	Over Temperature	*		*	±10		±45	*		*	V
Current, Quiescent	I_O = 0mA		*	*		3.8	4.5		*	*	mA
TEMPERATURE RANGE											
Specification		–55		+125	–25		+85	*		*	°C
Operating	Ambient Temperature	*		*	–55		+125	–25		+85	°C
θ Junction-Ambient			*			200			100		°C/W

*Specifications same as OPA445BM.

ORDERING INFORMATION

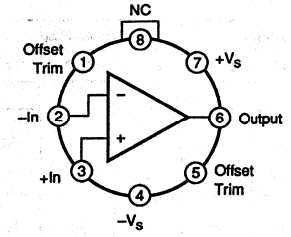
MODEL	PACKAGE	TEMPERATURE RANGE
OPA445AP	8-pin plastic DIP	–25°C to +85°C
OPA445BM	8-pin TO-99	–25°C to +85°C
OPA445SM	8-pin TO-99	–55°C to +125°C

ABSOLUTE MAXIMUM RATINGS

Power Supply	±50V
Internal Power Dissipation	680mW
Differential Input Voltage	±80V
Input Voltage Range	$\|±V_S\|$ –3V
Storage Temperature Range: M	–65°C to +150°C
P	–40°C to +85°C
Operating Temperature Range: M	–55°C to +125°C
P	–40°C to +85°C
Lead Temperature (soldering, 10s)	+300°C
Output Short-Circuit to Ground (T_A = +25°C)	Continuous
Junction Temperature	+175°C

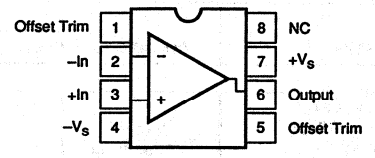
CONNECTION DIAGRAMS

Top View — TO-99



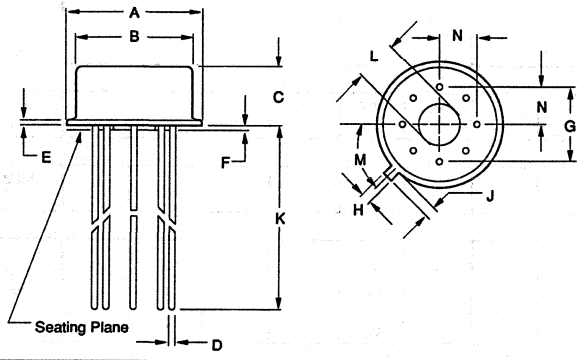
Case is connected to $-V_S$

Top View — DIP



MECHANICALS

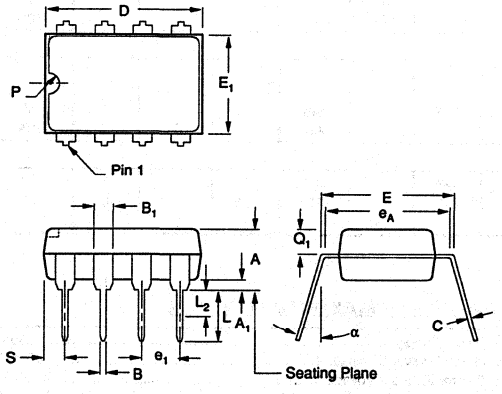
M Package — Metal TO-99



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.335	.370	8.51	9.40
B	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.200 BASIC		5.08 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500	—	12.7	—
L	.110	.160	2.79	4.06
M	45° BASIC		45° BASIC	
N	.095	.105	2.41	2.67

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Tab is pin 8.

P Package — 8-Pin Plastic DIP



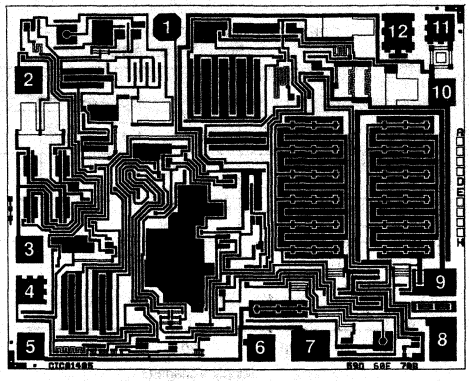
DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.155	.200	3.94	5.08
A1	.020	.050	0.51	1.27
B	.014	.020	0.36	0.51
B1	.045	.065	1.14	1.65
C	.008	.012	0.20	0.30
D (1)	.370	.400	9.40	10.16
E	.300	.325	7.62	8.26
E1	.240	.260	6.10	6.60
e1	.100 BASIC		2.54 BASIC	
eA	.300 BASIC		7.62 BASIC	
L	.125	.150	3.18	3.81

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
L2 (2)	0	.030	0.00	0.76
α	0°	15°	0°	15°
P	.015	.050	0.38	1.270
Q1	.040	.075	1.02	1.91
S (1)	.015	.050	0.38	1.27

(1) Not JEDEC Std.
(2) e_1 and e_A apply in zone L_2 when unit installed.
NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

DICE INFORMATION



OPA445 DIE TOPOGRAPHY

PAD	FUNCTION	PAD	FUNCTION
1	Offset Trim	7	$-V_S$
2	–In	8	(Compensation)
3	+In	9	Output
4	NC	10	$+V_S$
5	$-V_S$	11	NC
6	Offset Trim	12	NC

Substrate Bias: Electrically connected to $-V_S$ supply.
NC: No Connection.

MECHANICAL INFORMATION

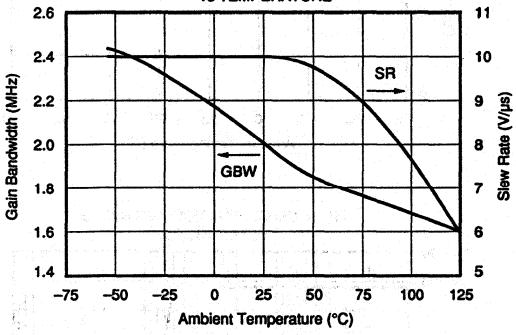
	MILS (0.001")	MILLIMETERS
Die Size	88 x 72 ±5	2.24 x 1.83 ±0.13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.1 x 0.1
Backing:	Chromium-Silver	

See "DICE PRODUCTS" Section 17 in Data Book Supplement Volume 33c, or contact Burr-Brown for current information.

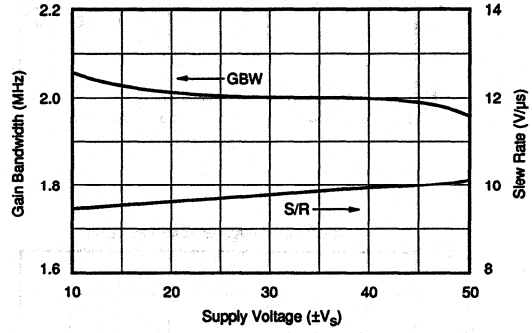
TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_S = ±40VDC, unless otherwise noted.

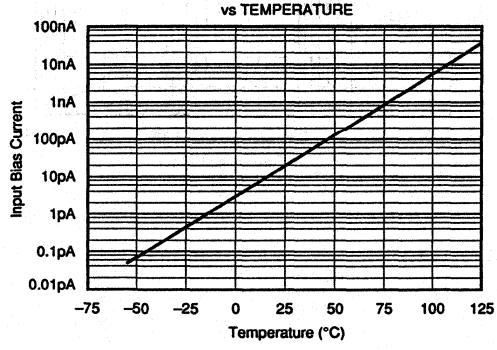
GAIN BANDWIDTH AND SLEW RATE vs TEMPERATURE



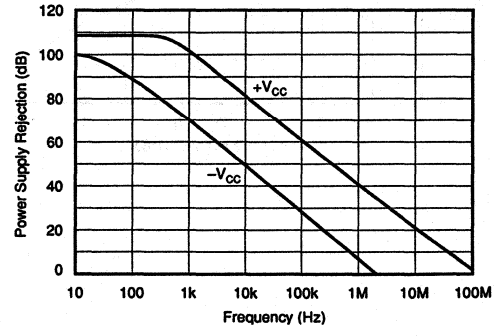
GAIN BANDWIDTH AND SLEW RATE vs SUPPLY VOLTAGE



INPUT BIAS CURRENT vs TEMPERATURE



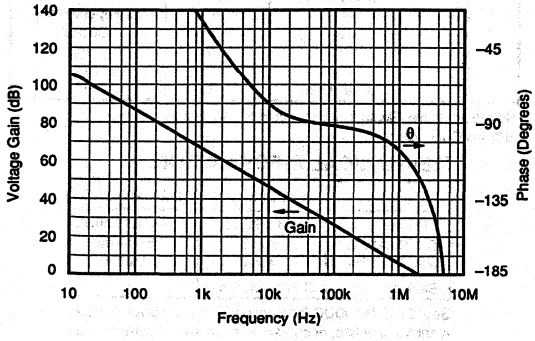
POWER SUPPLY REJECTION vs TEMPERATURE



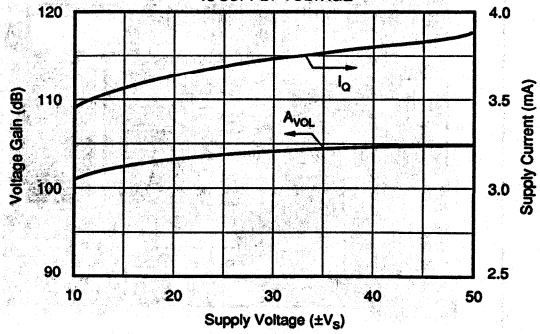
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_S = ±15VDC unless otherwise noted.

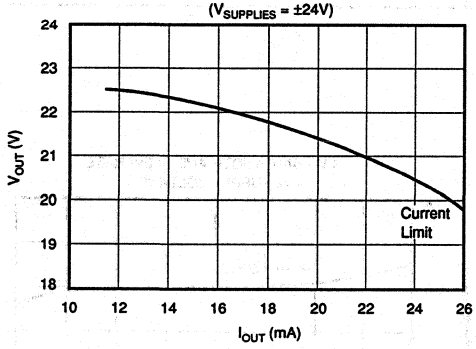
OPEN-LOOP FREQUENCY RESPONSE



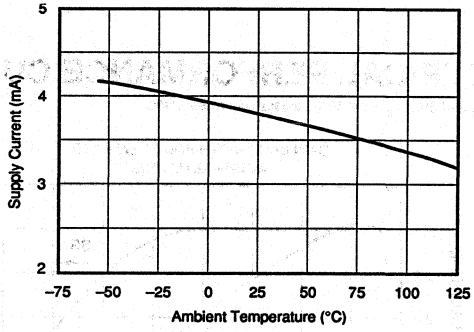
OPEN-LOOP GAIN AND SUPPLY CURRENT vs SUPPLY VOLTAGE



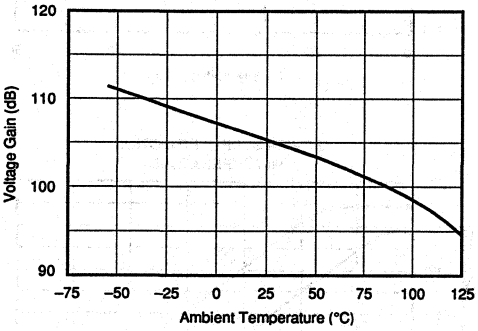
OUTPUT VOLTAGE vs OUTPUT CURRENT ($V_{SUPPLIES}$ = ±24V)



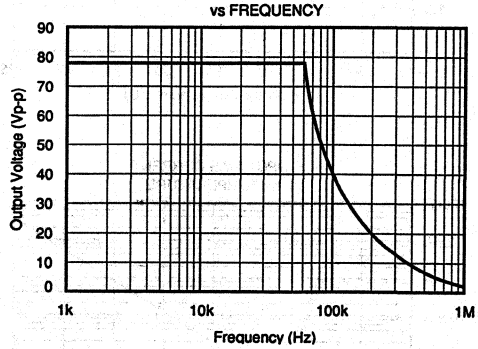
SUPPLY CURRENT vs TEMPERATURE



OPEN-LOOP GAIN vs TEMPERATURE



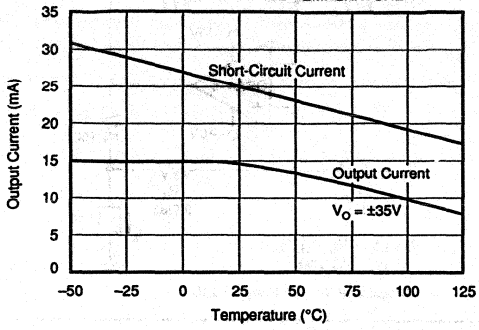
MAXIMUM OUTPUT VOLTAGE SWING vs FREQUENCY



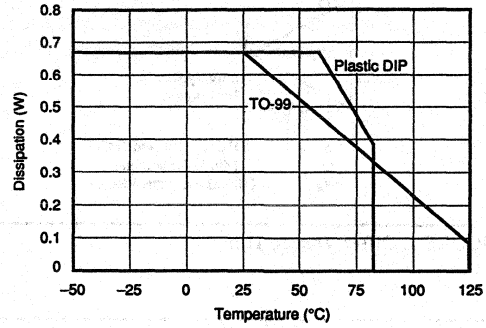
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_S = ±15VDC unless otherwise noted.

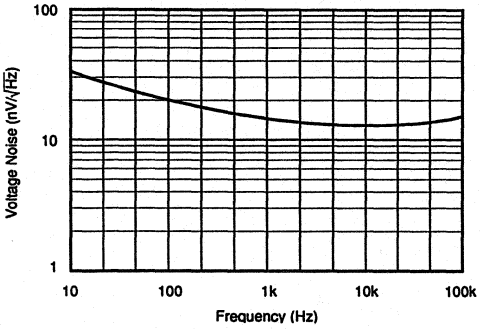
OUTPUT CURRENT vs TEMPERATURE



MAXIMUM POWER DISSIPATION vs TEMPERATURE



INPUT VOLTAGE NOISE SPECTRAL DENSITY



INSTALLATION AND OPERATING INSTRUCTIONS

The OPA445 may be operated from power supplies up to ±45V or a total of 90V. Power supplies should be bypassed with 0.022µF capacitors, or greater, near the power supply pins. Be sure that the capacitors are appropriately rated for the supply voltage used.

The OPA445 can supply output currents of 15mA and larger. This would present no problem for a standard op amp operating from ±15V supplies. With high supply voltages, however, internal power dissipation of the op amp can be quite large. Operation from a single power supply (or unbalanced power supplies) can produce even larger power dissipation since a larger voltage is impressed across the conducting output transistor.

Dissipation should be limited to 680mW at 25°C. At temperatures above 25°C, the maximum dissipation should be derated according to the thermal resistance of the package type used.

Package thermal resistance, θ_{JC}, is affected by mounting techniques and environments. The figures provided are typical for common mounting configurations with convection air flow. Poor air circulation and use of sockets can significantly increase thermal resistance. Best thermal performance is achieved by soldering the op amp into a circuit board with wide printed circuit traces to allow greater conduction through the op amp leads. Simple clip-on heat sinks can reduce the thermal resistance of the TO-99 metal package by as much as 50°C/W.

A short-circuit to ground will produce a typical output current of 25mA. With ±40V power supplies, this creates an internal power dissipation of 1.0W. This exceeds the maximum rating for the device, and is not recommended. Permanent damage is unlikely, however, since the short-circuit output current will diminish as the junction temperature rises.

TYPICAL APPLICATIONS

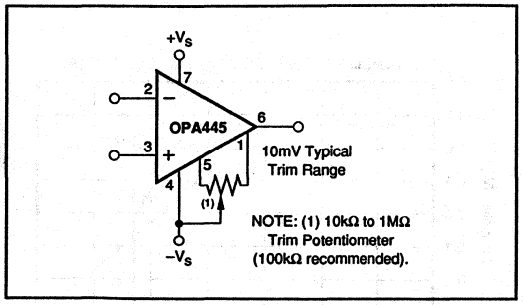


FIGURE 1. Offset Voltage Trim.

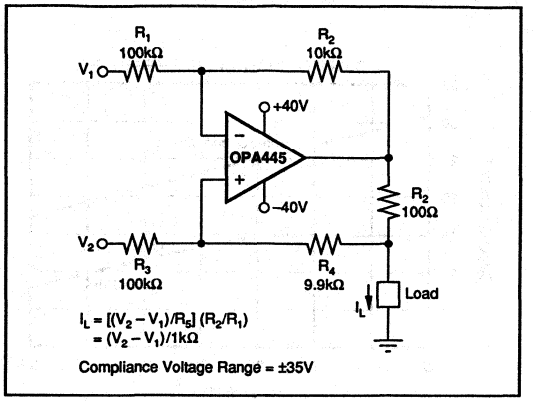


FIGURE 2. Voltage-to-Current Converter.

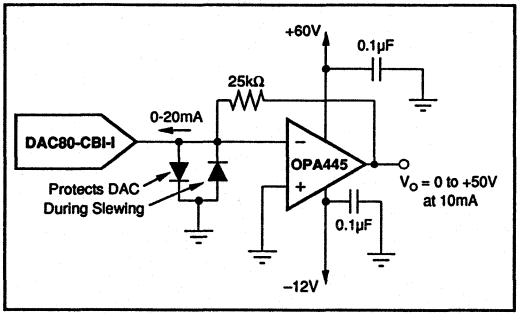


FIGURE 3. Programmable Voltage Source.

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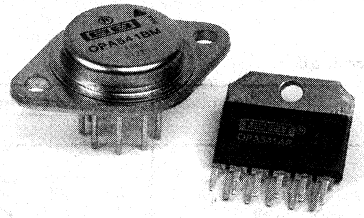


OPA541

AVAILABLE IN DIE

High Power Monolithic OPERATIONAL AMPLIFIER

FEATURES

- POWER SUPPLIES TO ±40V
- OUTPUT CURRENT TO 10A PEAK
- PROGRAMMABLE CURRENT LIMIT
- INDUSTRY-STANDARD PIN OUT
- FET INPUT
- TO-3 AND LOW-COST POWER PLASTIC PACKAGES

APPLICATIONS

- MOTOR DRIVER
- SERVO AMPLIFIER
- SYNCHRO EXCITATION
- AUDIO AMPLIFIER
- PROGRAMMABLE POWER SUPPLY

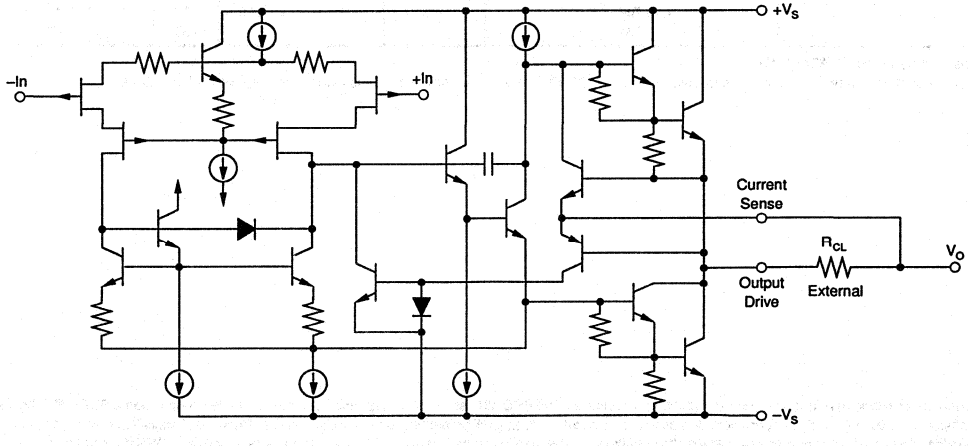
DESCRIPTION

The OPA541 is a power operational amplifier capable of operation from power supplies up to ±40V and delivering continuous output currents up to 5A. Internal current limit circuitry can be user-programmed with a single external resistor, protecting the amplifier and load from fault conditions. The OPA541 is fabricated using a proprietary bipolar/FET process.

Pinout is compatible with popular hybrid power amplifiers such as the OPA511, OPA512 and the 3573.

The OPA541 uses a single current-limit resistor to set both the positive and negative current limits. Applications currently using hybrid power amplifiers requiring two current-limit resistors need not be modified.

The OPA541 is available in an 11-pin power plastic package and an industry-standard 8-pin TO-3 hermetic package. The power plastic package has a copper-lead frame to maximize heat transfer. The TO-3 package is isolated from all circuitry, allowing it to be mounted directly to a heat sink without special insulators.



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Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL

At T_C = +25°C and V_S = ±35VDC unless otherwise noted.

PARAMETER	CONDITIONS	OPA541AM/AP			OPA541BM/SM			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
INPUT OFFSET VOLTAGE								
V_{OS}			±2	±10		±0.1	±1	mV
vs Temperature	Specified Temperature Range		±20	±40		±15	±30	µV/°C
vs Supply Voltage	V_S = ±10V to ±V_{MAX}		±2.5	±10		*	*	µV/V
vs Power			±20	±60		*	*	µV/W
INPUT BIAS CURRENT								
I_B			4	50		*	*	pA
INPUT OFFSET CURRENT								
I_{OS}			±1	±30		*	*	pA
	Specified Temperature Range			5		*		nA
INPUT CHARACTERISTICS								
Common-Mode Voltage Range	Specified Temperature Range	±(|V_S| – 6)	±(|V_S| – 3)		*	*		V
Common-Mode Rejection	V_{CM} = (±V_S – 6V)	95	113		*	*		dB
Input Capacitance			5			*		pF
Input Impedance, DC			1			*		TΩ
GAIN CHARACTERISTICS								
Open Loop Gain at 10Hz	R_L = 6Ω	90	97		*	*		dB
Gain-Bandwidth Product			1.6			*		MHz
OUTPUT								
Voltage Swing	I_O = 5A, Continuous	±(|V_S| – 5.5)	±(|V_S| – 4.5)		*	*		V
	I_O = 2A	±(|V_S| – 4.5)	±(|V_S| – 3.6)		*	*		V
	I_O = 0.5A	±(|V_S| – 4)	±(|V_S| – 3.2)		*	*		V
Current, Peak		9	10		*	*		A
AC PERFORMANCE								
Slew Rate		6	10		*	*		V/µs
Power Bandwidth	R_L = 8Ω, V_O = 20Vrms	45	55		*	*		kHz
Settling Time to 0.1%	2V Step		2			*		µs
Capacitive Load	Specified Temperature Range, G = 1	3.3					*	nF
	Specified Temperature Range, G >10			SOA[1]			*	
Phase Margin	Specified Temperature Range, R_L = 8Ω		40			*		Degrees
POWER SUPPLY								
Power Supply Voltage, ±V_S	Specified Temperature Range	±10	±30	±35	*	±35	±40	V
Current, Quiescent			20	25		*	*	mA
THERMAL RESISTANCE								
θ_{JC} (Junction-to-Case)[2]	AC Output f > 60Hz		2.5					°C/W
θ_{JC}[2]	DC Output		3					°C/W
θ_{JA} (Junction-to-Ambient)	No Heat Sink		40					°C/W
OPA541AP (Plastic)			40					°C/W
TEMPERATURE RANGE								
T_{CASE}	AM, BM, AP	–25		+85	*		*	°C
	SM				–55		+125	°C

* Specification same as OPA541AM/AP.

NOTE: (1) SOA is the Safe Operating Area shown in Figure 1. (2) Plastic package may require insulator which typically adds 1°C/W.

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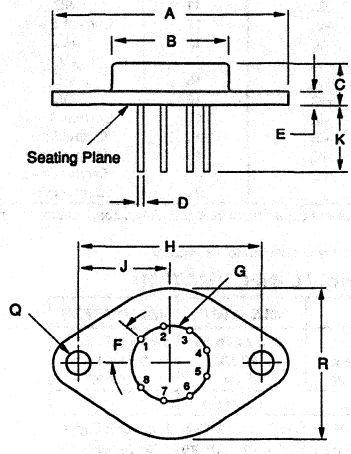
MECHANICAL

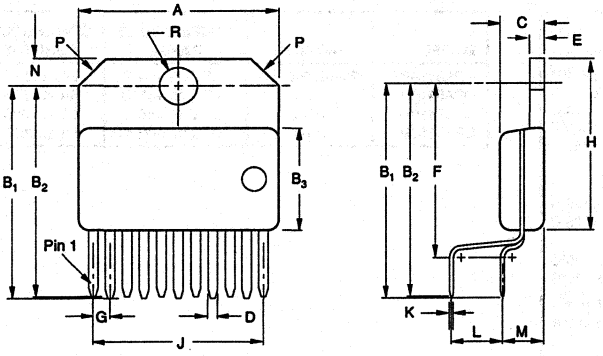
M Package — 8-Pin Metal TO-3



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.510	1.550	38.35	39.37
B	.745	.770	18.92	19.56
C	.260	.300	6.60	7.62
D	.038	.042	0.97	1.07
E	.080	.105	2.03	2.67
F	40° BASIC		40° BASIC	
G	.500 BASIC		12.70 BASIC	
H	1.182	1.192	30.02	30.28
J	.591	.596	15.01	15.14
K	.400	.500	10.16	12.70
Q	.151	.161	3.84	4.09
R	.980	1.020	24.89	25.91

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.

P Package — 11-Pin Plastic SIP

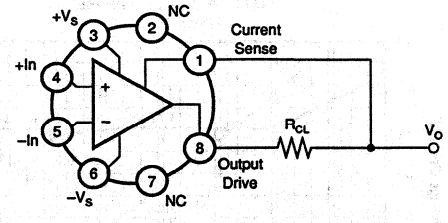


DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.778	.798	19.76	20.27
B_1	.846	.886	21.49	22.50
B_2	.840	.880	21.34	22.35
B_3	.400	.420	10.16	10.67
C	.172	.182	4.37	4.62
D	.033	.043	0.84	1.09
E	.057	.063	1.45	1.60
F	.690	.710	17.53	18.03
G	.057	.077	1.45	1.96
H	.675	.705	17.15	17.91
J	.660	.680	16.76	17.27
K	.014	.018	0.36	0.46
L	.190	.210	4.83	5.33
M	.159	.179	4.04	4.55
N	.105	.115	2.67	2.92
P	45° x .120		45° x 3.05	
R	.148 D	.152 D	3.76 D	3.86 D

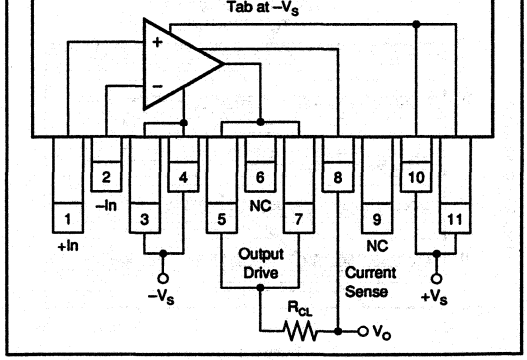
NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

CONNECTION DIAGRAMS

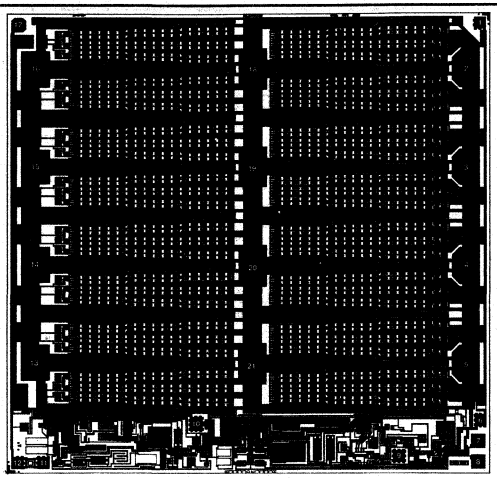
M Package Top View



P Package Top View



DICE INFORMATION



OPA541 DIE TOPOGRAPHY

PAD	FUNCTION	PAD	FUNCTION
1	NC	11	NC
2	$-V_S$	12	Current Sense
3	$-V_S$	13	$+V_S$
4	$-V_S$	14	$+V_S$
5	$-V_S$	15	$+V_S$
6	NC	16	$+V_S$
7	–In	17	Current Sense
8	+In	18	Output Drive
9	NC	19	Output Drive
10	NC	20	Output Drive
		21	Output Drive

NOTE: For full output current capability, wire-bond all like connections of $+V_S$, $-V_S$ and Output Drive.

Substrate Bias: Electrically connected to $-V_S$ supply.

MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	213 x 205 ±5	5.41 x 5.21 ±0.13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.1 x 0.1
Backing:	Chromium-Silver	

See "DICE PRODUCTS" Section 17 in Data Book Supplement Volume 33c, or contact Burr-Brown for current information.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, $+V_S$ to $-V_S$ 80V
Output Current ..... see SOA
Power Dissipation, Internal[1] 125W
Input Voltage: Differential ..... $\pm V_S$
Common-mode ..... $\pm V_S$
Temperature: Pin solder, 10s ..... +300°C
Junction[1] ..... +150°C
Temperature Range:
AM, BM SM
Storage ..... –65°C to +150°C
Operating (case) ..... –55°C to +125°C
AP
Storage ..... –40°C to +85°C
Operating (case) ..... –25°C to +85°C

NOTE: (1) Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF.

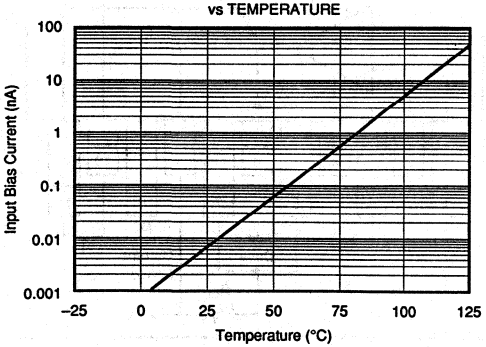
ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE	CONTINUOUS CURRENT
OPA541AP	Power Plastic	–25°C to +85°C	5A at 25°C
OPA541AM	TO-3	–25°C to +85°C	5A at 25°C
OPA541BM	TO-3	–25°C to +85°C	5A at 25°C
OPA541SM	TO-3	–55°C to +125°C	5A at 25°C

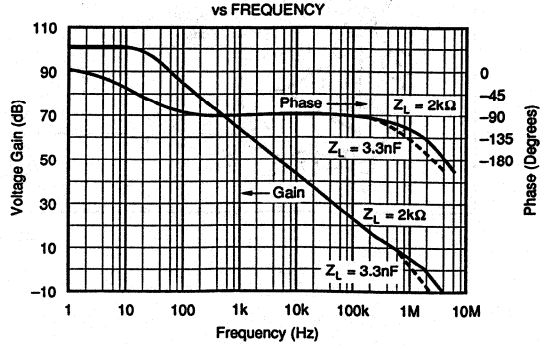
TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_S = ±35VDC unless otherwise noted.

INPUT BIAS CURRENT vs TEMPERATURE



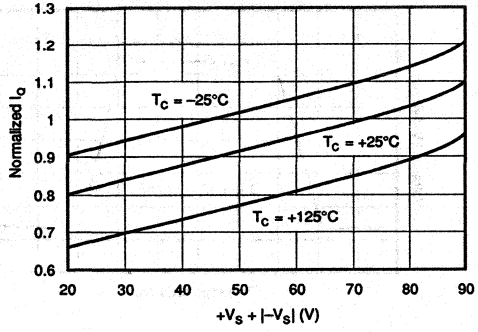
OPEN-LOOP GAIN AND PHASE vs FREQUENCY



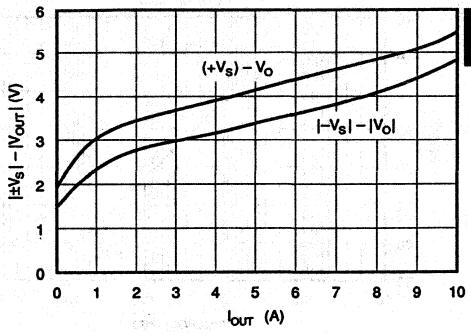
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_S = ±35VDC unless otherwise noted.

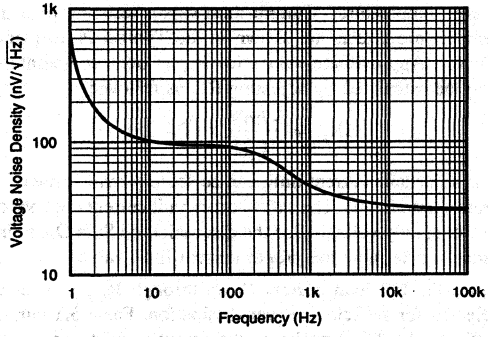
NORMALIZED QUIESCENT CURRENT vs TOTAL POWER SUPPLY VOLTAGE



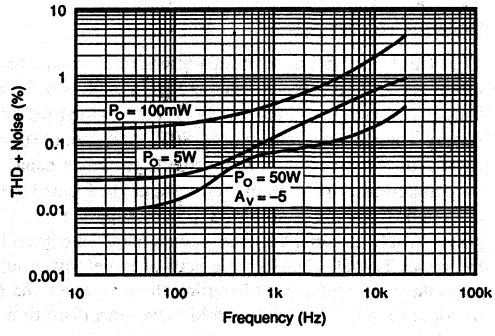
OUTPUT VOLTAGE SWING vs OUTPUT CURRENT



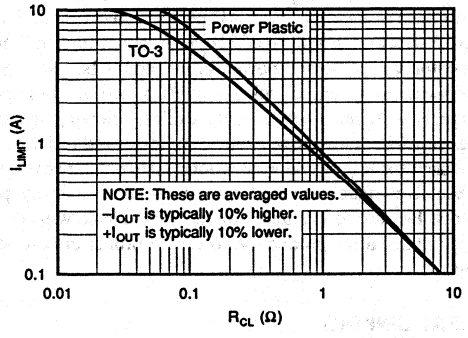
VOLTAGE NOISE DENSITY vs FREQUENCY



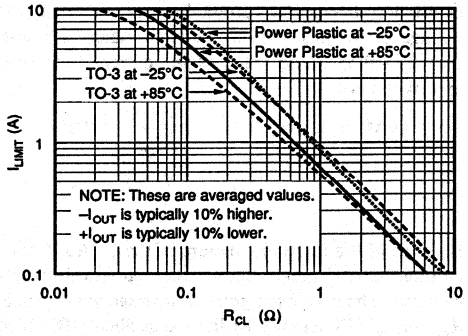
TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY



CURRENT LIMIT vs RESISTANCE LIMIT

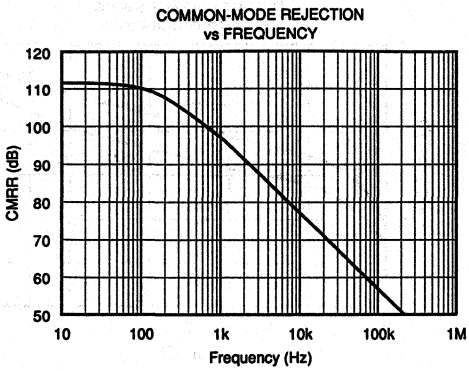


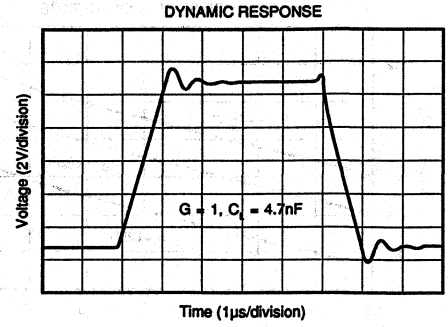
CURRENT LIMIT vs RESISTANCE LIMIT vs TEMPERATURE



TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_S = ±35VDC unless otherwise noted.





INSTALLATION INSTRUCTIONS

POWER SUPPLIES

The OPA541 is specified for operation from power supplies up to ±40V. It can also be operated from unbalanced power supplies or a single power supply, as long as the total power supply voltage does not exceed 80V. The power supplies should be bypassed with low series impedance capacitors such as ceramic or tantalum. These should be located as near as practical to the amplifier's power supply pins. Good power amplifier circuit layout is, in general, like good high frequency layout. Consider the path of large power supply and output currents. Avoid routing these connections near low-level input circuitry to avoid waveform distortion and oscillations.

CURRENT LIMIT

Internal current limit circuitry is controlled by a single external resistor, R_{CL}. Output load current flows through this external resistor. The current limit is activated when the voltage across this resistor is approximately a base-emitter turn-on voltage. The value of the current limit resistor is approximately:

$$\text{(AM, BM, SM)} \quad R_{CL} = \frac{0.809}{|I_{LIM}|} - 0.057$$

$$\text{(AP)} \quad R_{CL} = \frac{0.813}{|I_{LIM}|} - 0.02$$

Because of the internal structure of the OPA541, the actual current limit depends on whether current is positive or negative. The above R_{CL} gives an average value. For a given R_{CL}, $+I_{OUT}$ will actually be limited at about 10% below the expected level, while $-I_{OUT}$ will be limited about 10% above the expected level.

The current limit value decreases with increasing temperature due to the temperature coefficient of a base-emitter junction voltage. Similarly, the current limit value increases at low temperatures. Current limit versus resistor value and temperature effects are shown in the Typical Performance Curves. Approximate values for R_{CL} at other temperatures may be calculated by adjusting R_{CL} as follows:

$$\Delta R_{CL} = \frac{-2mV}{|I_{LIM}|} \times (T - 25)$$

The adjustable current limit can be set to provide protection from short circuits. The safe short-circuit current depends on power supply voltage. See the discussion on Safe Operating Area to determine the proper current limit value.

Since the full load current flows through R_{CL}, it must be selected for sufficient power dissipation. For a 5A current limit on the TO-3 package, the formula yields an R_{CL} of 0.105Ω (0.143Ω on the power plastic package due to different internal resistances). A continuous 5A through 0.105Ω would require an R_{CL} that can dissipate 2.625W.

Sinusoidal outputs create dissipation according to rms load current. For the same R_{CL}, AC peaks would still be limited to 5A, but rms current would be 3.5A, and a current limiting resistor with a lower power rating could be used. Some applications (such as voice amplification) are assured of signals with much lower duty cycles, allowing a current resistor with a low power rating. Wire-wound resistors may be used for R_{CL}. Some wire-wound resistors, however, have excessive inductance and may cause loop-stability problems. Be sure to evaluate circuit performance with resistor type planned for production to assure proper circuit operation.

HEAT SINKING

Power amplifiers are rated by case temperature, not ambient temperature as with signal op amps. Sufficient heat sinking must be provided to keep the case temperature within rated

limits for the maximum ambient temperature and power dissipation. The thermal resistance of the heat sink required may be calculated by:

$$\theta_{HS} = \frac{T_{CASE} - T_{AMBIENT}}{P_D \text{ (max)}}$$

Commercially available heat sinks often specify their thermal resistance. These ratings are often suspect, however, since they depend greatly on the mounting environment and air flow conditions. Actual thermal performance should be verified by measurement of case temperature under the required load and environmental conditions.

No insulating hardware is required when using the TO-3 package. Since mica and other similar insulators typically add approximately 0.7°C/W thermal resistance, their elimination significantly improves thermal performance. See Burr-Brown Application Note AN-83 for further details on heat sinking. On the power plastic package, the metal tab is connected to $-V_S$, and appropriate actions should be taken when mounting on a heat sink or chassis.

SAFE OPERATING AREA

The safe operating area (SOA) plot provides comprehensive information on the power handling abilities of the OPA541. It shows the allowable output current as a function of the voltage across the conducting output transistor (see Figure 1). This voltage is equal to the power supply voltage minus the output voltage. For example, as the amplifier output swings near the positive power supply voltage, the voltage across the output transistor decreases and the device can safely provide large output currents demanded by the load.

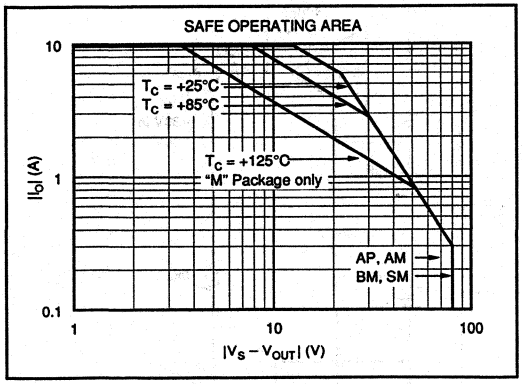


FIGURE 1. Safe Operating Area.

Short circuit protection requires evaluation of SOA. When the amplifier output is shorted to ground, the full power supply voltage is impressed across the conducting output transistor. The current limit must be set to a value which is safe for the power supply voltage used. For instance, with V_S ±35V, a short to ground would force 35V across the conducting power transistor. A current limit of 1.8A would be safe.

Reactive, or EMF-generating, loads such as DC motors can present difficult SOA requirements. With a purely reactive load, output voltage and load current are 90° out of phase. Thus, peak output current occurs when the output voltage is zero and the voltage across the conducting transistor is equal to the full power supply voltage. See Burr-Brown Application Note AN-123 for further information on evaluating SOA.

REPLACING HYBRID POWER AMPLIFIERS

The OPA541 can be used in applications currently using various hybrid power amplifiers, including the OPA501, OPA511, OPA512, and 3573. Of course, the application must be evaluated to assure that the output capability and other performance attributes of the OPA541 meet the necessary requirement. These hybrid power amplifiers use two current limit resistors to independently set the positive and negative current limit value. Since the OPA541 uses only one current limit resistor to set both the positive and negative current limit, only one resistor (see Figure 4) need be installed. If installed, the resistor connected to pin 2 (TO-3 package) is superfluous, but it does no harm.

Because one resistor carries the current previously carried by two, the resistor may require a higher power rating. Minor adjustments may be required in the resistor value to achieve the same current limit value. Often, however, the

APPLICATIONS CIRCUITS

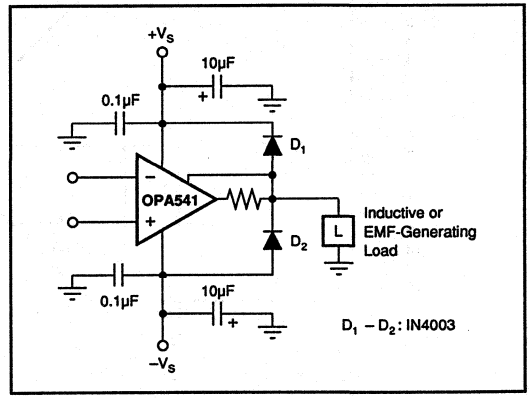


FIGURE 2. Clamping Output for EMF-Generating Loads.

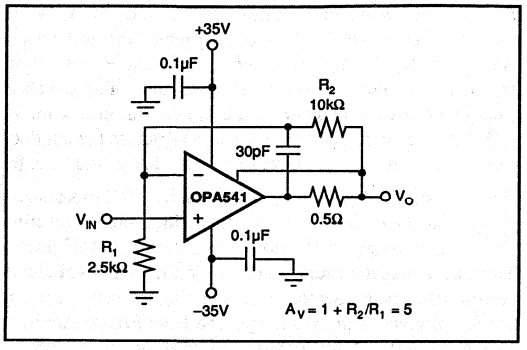


FIGURE 3. Isolating Capacitive Loads.

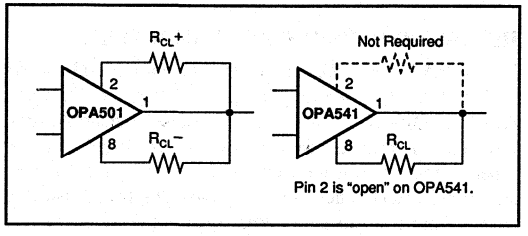


FIGURE 4. Replacing OPA501 with OPA541.

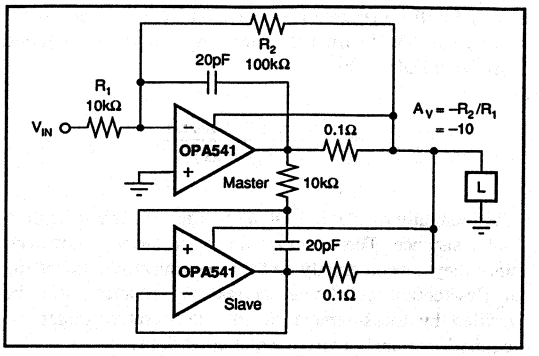


FIGURE 5. Paralleled Operation, Extended SOA.

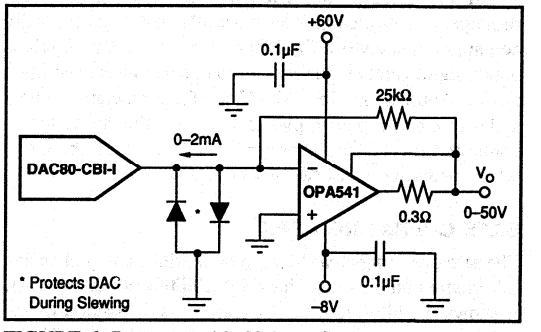


FIGURE 6. Programmable Voltage Source.

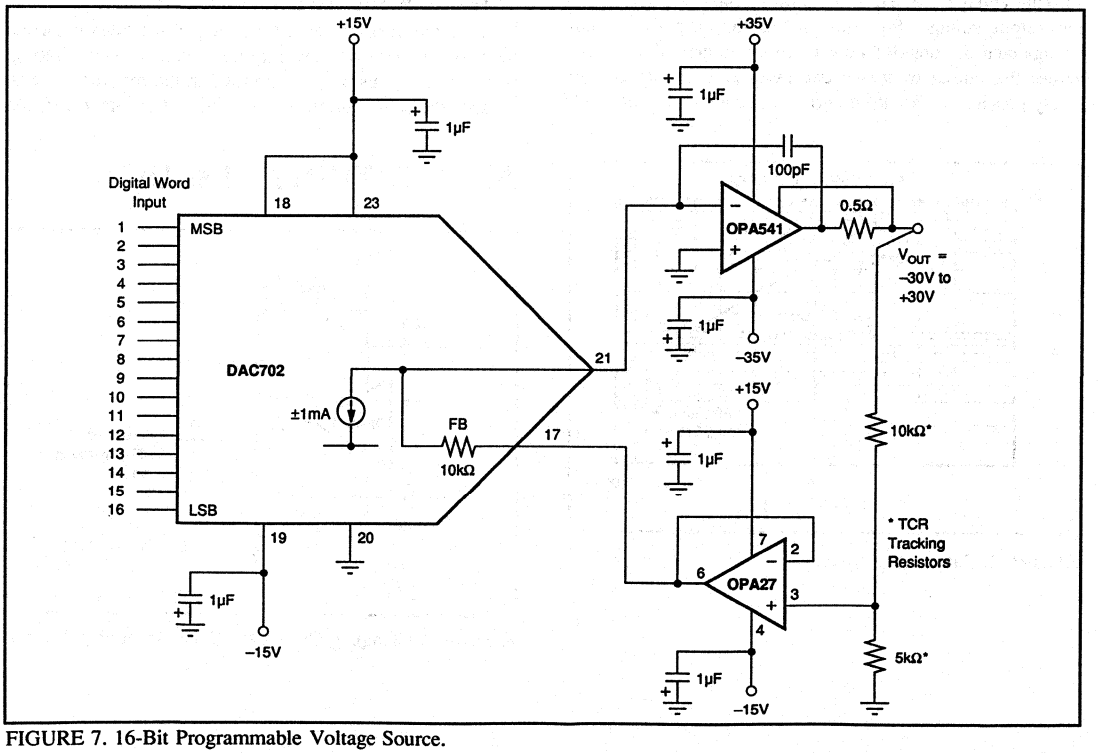


FIGURE 7. 16-Bit Programmable Voltage Source.

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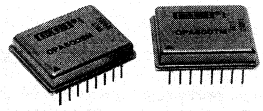


OPA600

Fast-Settling Wideband OPERATIONAL AMPLIFIER

FEATURES

- FAST SETTLING: 80ns to ±0.1%
  100ns to ±0.01%
- FULL DIFFERENTIAL FET INPUT
- –25°C to +85°C AND –55°C to +125°C TEMPERATURE RANGES
- ±10V OUTPUT: 200mA
- GAIN BANDWIDTH PRODUCT: 5GHz

APPLICATIONS

- VOLTAGE CONTROLLED OSCILLATOR DRIVER
- LARGE SIGNAL, WIDEBAND DRIVERS
- HIGH SPEED D/A CONVERTER OUTPUT AMPLIFIER
- VIDEO PULSE AMPLIFIER

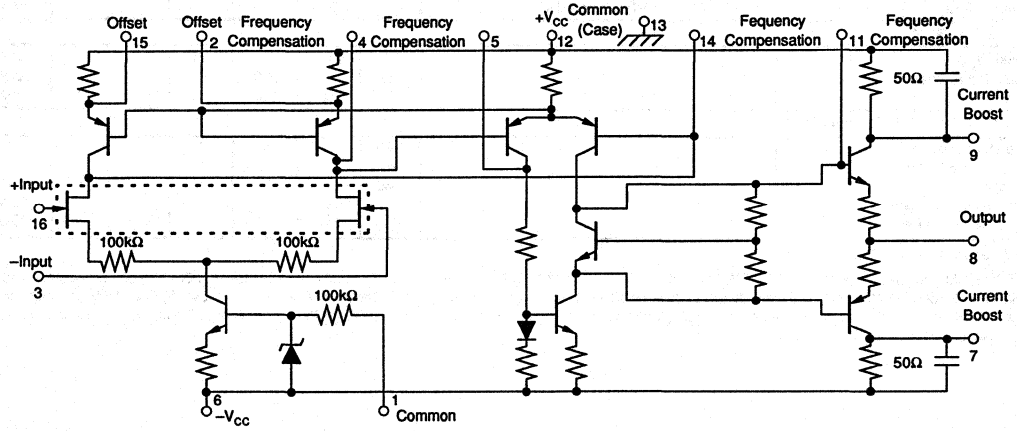
DESCRIPTION

The OPA600 is a wideband operational amplifier specifically designed for fast settling to ±0.01% accuracy. It is stable, easy to use, has good phase margin with minimum overshoot, and it has excellent DC performance. It utilizes an FET input stage to give low input bias current. Its DC stability over temperature is outstanding. The slew rate exceeds 400V/µs. All of this combines to form an outstanding amplifier for large and small signals.

High accuracy with fast settling time is achieved by using a high open-loop gain which provides the accuracy at high frequencies. The thermally balanced design maintains this accuracy without droop or thermal tail. External frequency compensation allows the user to optimize the settling time for various gains and load conditions.

The OPA600 is useful in a broad range of video, high speed test circuits and ECM applications. It is particularly well suited to operate as a voltage controlled oscillator (VCO) driver. It makes an excellent digital-to-analog converter output amplifier. It is a workhorse in test equipment where fast pulses, large signals, and 50Ω drive are important. It is a good choice for sample/holds, integrators, fast waveform generators, and multiplexers.

The OPA600 is specified over the industrial temperature range (OPA600BM, CM) and military temperature range (OPA600SM, TM). The OPA600 is housed in a welded, hermetic metal package.



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Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL

At V_{CC} = ±15VDC and T_A = +25°C unless otherwise noted.

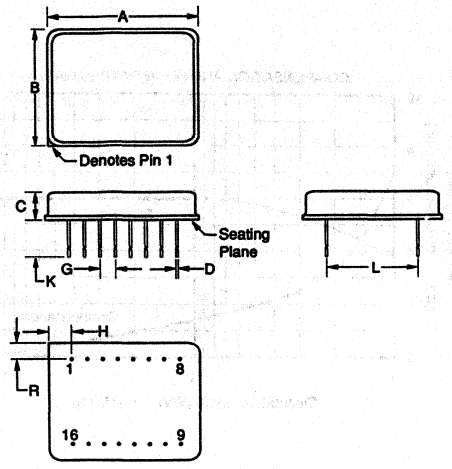
PARAMETER	CONDITIONS	OPA600CM,TM[1] MIN	OPA600CM,TM[1] TYP	OPA600CM,TM[1] MAX	OPA600BM,SM MIN	OPA600BM,SM TYP	OPA600BM,SM MAX	UNITS
OUTPUT								
Voltage	R_L = 2kΩ	±10			*			V
	R_L = 50Ω[2]	±9			*			V
Current	R_L = 50Ω[2]	±180	±200		*	*		mA
Current Pulse	R_L = 50Ω[3]	±180	±200		*	*		mA
Resistance	Open Loop DC		75			*		Ω
Short-Circuit Current	To COMMON Only, t_{MAX} = 1s[4]		250	300		*	*	mA
DYNAMIC RESPONSE								
Settling Time[5]: to ±0.01% (±1mV)	ΔV_{OUT} = 10V		100	125		*	*	ns
to ±0.1% (±10mV)	ΔV_{OUT} = 10V		80	105		*	*	ns
to ±1% (±100mV)	ΔV_{OUT} = 10V		70	95		*	*	ns
Gain-Bandwidth Product (open-loop)	C_C = 0pF, G = 1V/V		150			*		MHz
	C_C = 0pF, G = 10V/V		500			*		MHz
	C_C = 0pF, G = 100V/V		1.5			*		GHz
	C_C = 0pF, G = 1000V/V		5			*		GHz
	C_C = 0pF, G = 10,000V/V		10			*		GHz
Bandwidth (–3dB small signal)[6]	G = +1V/V		125			*		MHz
	G = –1V/V		90			*		MHz
	G = –10V/V		95			*		MHz
	G = –100V/V		20			*		MHz
	G = –1000V/V		6			*		MHz
Full Power Bandwidth	V_{OUT} = ±5V, G = –1V/V, C_C = 3.3pF, R_L = 100Ω		16			*		MHz
Slew Rate	V_{OUT} = ±5V, G = –1000V/V, C_C = 0pF, R_L = 100Ω		500			*		V/µs
	V_{OUT} = ±5V,G = –1V/V[4]	400	440		*	*		V/µs
Phase Margin	G = –1V/V, C_C = 3.3pF		40			*		Degrees
GAIN								
Open-Loop Voltage Gain	f = DC, R_L = 2kΩ, T_A = +25°C	86	94		*	*		dB
INPUT								
Offset Voltage[7]	T_A = +25°C		±1	±4		±2	±5	mV
	T_A = –25°C to +85°C			±5			±10	mV
	T_A = –55°C to +125°C			±6			±15	mV
Offset Voltage Drift	T_A = –25°C to +85°C			±20			±80	µV/°C
	T_A = –55°C to +125°C			±20			±100	µV/°C
Bias Current	T_A = +25°C		–20	–100		*	*	pA
	T_A = –25°C to +125°C		–20	–100		*	*	nA
Offset Current	T_A = +25°C		20			*		pA
	T_A = –55°C to +125°C		20			*		nA
Power Supply Rejection Ratio	V_{CC} = ±15V, ±1V		200	500		*	*	µV/V
Common-Mode Voltage Range		–10		+7	*		*	V
Common-Mode Rejection Ratio	V_{CM} = –5V to +5V	60	80		*	*		dB
Impedance	Differential and Common-Mode		10^{11} || 2			*		Ω || pF
Voltage Noise	10kHz Bandwidth		20			*		nV/√Hz
POWER SUPPLY								
Rated (V_{CC})			±15			*		VDC
Operating Range		±9		±16	*		*	VDC
Quiescent Current			±30	±38		*	*	mA
TEMPERATURE RANGE (Ambient)								
Operating: BM, CM		–25		+85	*		*	°C
SM, TM		–55		+125	*		*	°C
Storage		–65		+150	*		*	°C
θ_{JC} ,(junction-to-case)			30			*		°C/W
θ_{CA} , (case-to-ambient)			35			*		°C/W

*Specification same as OPA600CM, TM.

NOTES: (1) BM, CM grades: –25°C to +85°C. SM, TM grades: –55°C to +125°C. (2) Pin 9 connected to +V_{CC}, pin 7 connected to –V_{CC}. Observe power dissipation ratings. (3) Pin 9 and 7 open. Single pulse t = 100ns. Observe power dissipation ratings. (4) Pin 9 and 7 open. See section on Current Boost. (5) G = –1V/V. Optimum settling time and slew rate achieved by individually compensating each device. Refer to section on Compensation. (6) Frequency compensation as discussed in section on Compensation. (7) Adjustable to zero.

MECHANICAL

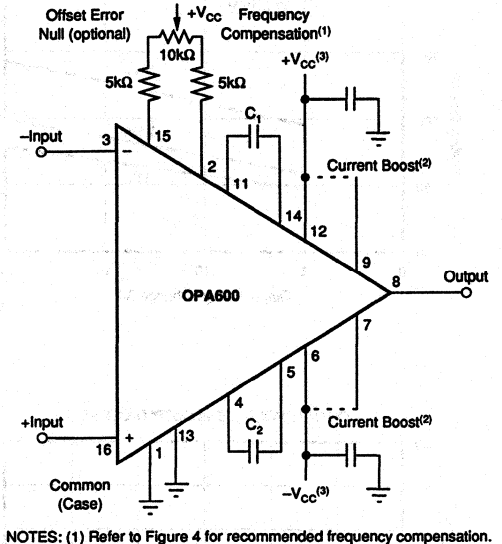
M Package — 16-Pin



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.963	.980	24.46	24.89
B	.760	.805	19.30	20.45
C	.175	.190	4.45	4.83
D	.014	.022	0.36	0.56
G	.100 BASIC		2.54 BASIC	
H	.135	.155	3.43	3.94
K	.230	.270	5.84	6.86
L	.600 BASIC		15.24 BASIC	
R	.095	.115	2.41	2.92

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only.

CONNECTION DIAGRAM



NOTES: (1) Refer to Figure 4 for recommended frequency compensation. (2) connect pin 9 to pin 12 and connect pin 7 to pin 6 for maximum output current. See Application Information for further information. (3) Bypass each power supply lead as close as possible to the amplifier pins. A 1µF CS13 tantalum capacitor is recommended. (4)There is no internal conenction. An external connection may be made. (5) It is recommended that the amplifier be mounted with the case in contact with a ground plane for good thermal transfer and optimum AC performance.

ABSOLUTE MAXIMUM RATINGS(1)

Supply Voltage, $+V_{CC}$ to $-V_{CC}$	±17V
Power Dissipation, At T_{CASE} +125°C(2)	1.6W
Input Voltage: Differential	$\pm V_{CC}$
Common-Mode	$\pm V_{CC}$
Output Short Circuit Duration to Common	<5s
Temperature: pin (soldering, 20s)	+300°C
Junction(1), T_J	+175°C
Temperature Range: Storage	–65°C to +150°C
Operating (case)	–55°C to +125°C

NOTES: (1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability. (2) Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF.

ORDERING INFORMATION

MODEL	TEMPERATURE RANGE (°C)	VOLTAGE OFFSET DRIFT (µV/°C)
OPA600BM	–25 to +85	±80
OPA600CM	–25 to +85	±20
OPA600SM	–55 to +125	±100
OPA600TM	–25 to +125	±20

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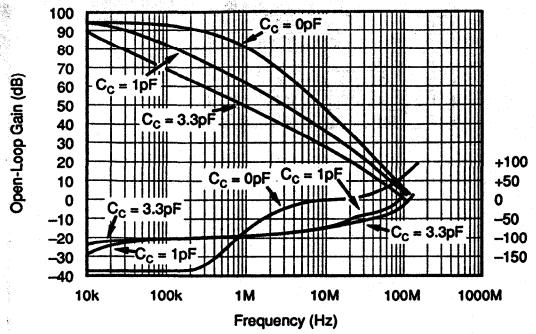
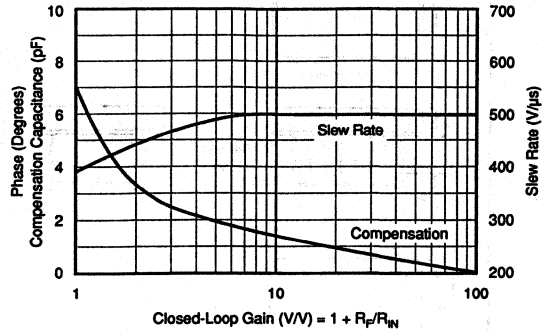
TYPICAL PERFORMANCE CURVES

Typical at T_A = +25°C and $\pm V_{CC}$ = 15VDC, unless otherwise specified.

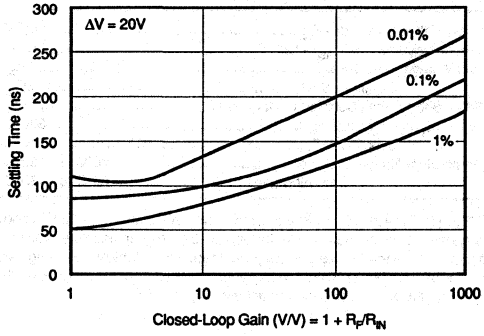
BODE PLOT



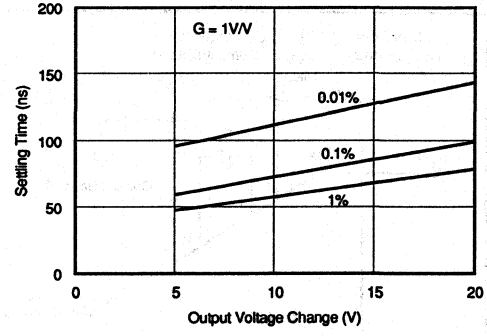
COMPENSATION AND SLEW RATE vs GAIN



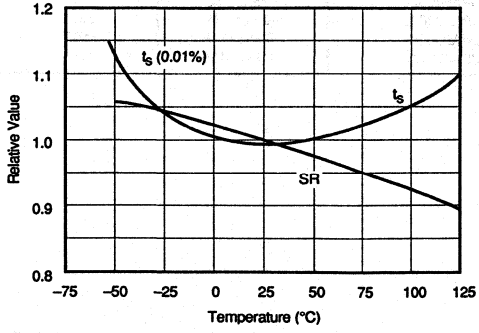
SETTLING TIME vs GAIN



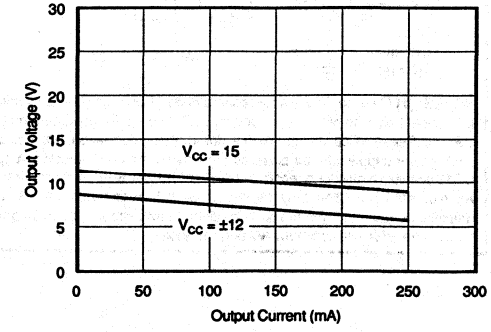
SETTLING TIME vs OUTPUT VOLTAGE CHANGE



SETTLING TIME AND SLEW RATE vs TEMPERATURE



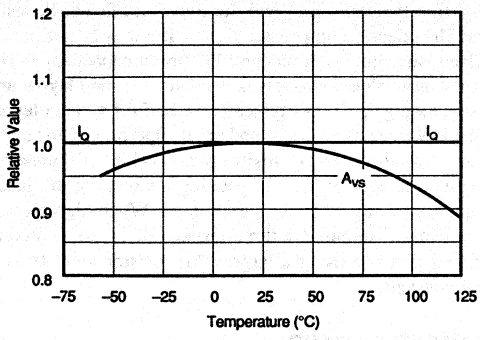
OUTPUT VOLTAGE vs OUTPUT CURRENT



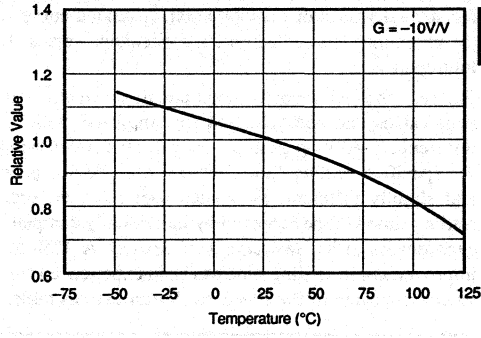
TYPICAL PERFORMANCE CURVES (CONT)

Typical at T_A = +25°C, $\pm V_{CC}$ = 15VDC unless otherwise specified.

OPEN-LOOP GAIN AND QUIESCENT CURRENT vs TEMPERATURE



BANDWIDTH



INSTALLATION AND OPERATION

WIRING PRECAUTIONS

The OPA600 is a wideband, high frequency operational amplifier with a gain-bandwidth product exceeding 5GHz. This capability can be realized by observing a few wiring precautions and using high frequency layout techniques. In general, all printed circuit board conductors should be wide to provide low resistance, low impedance signal paths and should be as short as possible. The entire physical circuit should be as small as is practical. Stray capacitances should be minimized, especially at high impedance nodes, such as the input terminals of the amplifier and compensation pins. Stray signal coupling from the output to the input should be minimized. All circuit element leads should be as short as possible and low values of resistance should be used. This will give the best circuit performance as it will minimize the time constants formed with the circuit capacitances and will eliminate stray, unwanted tuned circuits.

Grounding is the most important application consideration for the OPA600, as it is with all high frequency circuits. Ultra-high frequency transistors are used in the design of the OPA600 and oscillations at frequencies of 500MHz and above can be stimulated if good grounding techniques are not used. A ground plane is highly recommended. It should connect all areas of the pattern side of the printed circuit that are not otherwise used. The ground plane provides a low resistance, low inductance common return path for all signal and power returns. The ground plane also reduces stray signal pickup.

Point-to-point wiring is not recommended. However, if point-to-point wiring is used, a single-point ground should be used. The input signal return, the load signal return and the power supply common should all be connected at the same physical point. This eliminates common current paths or ground loops which can cause unwanted feedback.

Each power supply lead should be bypassed to ground as near as possible to the amplifier pins. A 1µF CS13 tantalum capacitor is recommended. A parallel 0.01µF ceramic may be added if desired. This is especially important when driving high current loads. Properly bypassed and modulation-free power supply lines allow full amplifier output and optimum settling time performance.

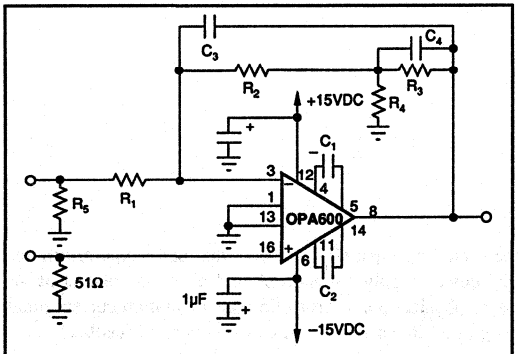
OPA600 circuit common is connected to pins 1 and 13; these pins should be connected to the ground plane. The input signal return, load return, and power supply common should also be connected to the ground plane.

The case of the OPA600 is internally connected to circuit common, and as indicated above, pins 1 and 13 should be connected to the ground plane. Ideally, the case should be mechanically connected to the ground plane for good thermal transfer, but because this is difficult in practice, the OPA600 should be fully inserted into the printed circuit board with the case very close to the ground plane to make the best possible thermal connection. If the case and ground plane are physically connected or are in close thermal proximity, the ground plane will provide heat sinking which will reduce the case temperature rise. The minimum OPA600 pin length will minimize lead inductance, thereby maximizing performance.

COMPENSATION

The OPA600 uses external frequency compensation so that the user may optimize the bandwidth or settling time for his particular application. Several performance curves aid in the selection of the correct compensation's capacitance value. The Bode plot shows amplitude and phase versus frequency for several values of compensation. A related curve shows the recommended compensation capacitance versus closed-loop gain.

Figure 1 shows a recommended circuit schematic. Component values and compensation for amplifiers with several different closed-loop gains are shown. This circuit will yield the specified settling time. Because each device is unique and slightly different, as is each user's circuit, optimum settling time will be achieved by individually compensating each device in its own circuit, if desired. A 10% to 20% improvement in settling time has been experienced from the values indicated in the Electrical Specifications table.



Closed Loop Gain	R_1	R_2	R_3	R_4	C_1, C_2	C_3	C_4	R_5
+1	open	100	short	open	6.8	0	0	–
–1	620	620	short	open	3.3	4.7	0	56
–10	100	1k	short	open	1	2.2	0	100
–100	100	3.3k	3.3k	3.2k	0	1	0	100
–1000	100	3.3k	3.3k	116	0	0	4.7	100

FIGURE 1. Recommended Amplifier Circuits and Frequency Compensation.

The primary compensation capacitors are C_1 and C_2 (see Figure 1). They are connected between pins 4 and 5 and between pins 11 and 14. Both C_1 and C_2 should be the same value. As Figure 1 and the performance curves show, larger closed-loop configurations require less capacitance, and improved gain-bandwidth product can be realized. Note that no compensation capacitor is required for closed-loop gains equal to or above 100V/V. If upon initial application the user's circuit is unstable, and remains so after checking for proper bypassing, grounding, etc., it may be necessary to increase the compensation slightly to eliminate oscillations. Do not over compensate. It should not be necessary to increase C_1 and C_2 beyond 10pF to 15pF. It may also be necessary to individually optimize C_1 and C_2 for improved performance.

The flat high frequency response of the OPA600 is preserved and high frequency peaking is minimized by connecting a small capacitor in parallel with the feedback resistor (see Figure 1). This capacitor compensates for the closed-loop, high frequency, transfer function zero that results from the time constant formed by the input capacitance of the amplifier, typically 2pF, and the input and feedback resistors. The selected compensation capacitor may be a trimmer, a fixed capacitor, or a planned PC board capacitance. The capacitance value is strongly dependent on circuit layout and closed-loop gain. It will typically be 2pF for a clean layout using low resistances (1kΩ) and up to 10pF for circuits using larger resistances. Using small resistor values will preserve the phase margin and avoid peaking by keeping the break frequency of this zero sufficiently high. When high closed-loop gains are required, a three-resistor attenuator is recommended to avoid using a large value resistor with its long time constant.

CAPACITIVE LOADS

The OPA600 will drive large capacitive loads (up to 100pF) when properly compensated and settling times of under 150ns are achievable. The effect of a capacitive load is to decrease the phase margin of the amplifier, which may cause high frequency peaking or oscillations. A solution is to increase the compensation capacitance, somewhat slowing the amplifier's ability to respond. The recommended compensation capacitance value as a function of load capacitance is shown in Figure 2. (Use two capacitors, each with the value indicated.) Alternately, without increasing the OPA600's compensation capacitance, the capacitive load may be buffered by connecting a small resistance, usually 5Ω to 50Ω, in series with the Output, pin 8.

For very-large capacitive loads, greater than 100pF, it will be necessary to use doublet compensation. Refer to Figure 3 and discussion on slew rate. This places the dominant pole at the input stage. Settling time will be approximately 50% slower; slew rate should increase. Load capacitance should be minimized for optimum high frequency performance.

Because of its large output capability, the OPA600 is particularly well suited for driving loads via coaxial cables. Note that the capacitance of coaxial cable (29pF/foot of length for RG-58) will not load the amplifier when the coaxial cable or transmission line is terminated in its characteristic impedance.

SETTLING TIME

Settling time is defined as the total time required, from the input signal step, for the output to settle within the specified error band around the final value. This error band is expressed as a percentage of the magnitude of the output transition, a 10V step.

Settling time is a complete dynamic measure of the OPA600's total performance. It includes the slew rate time, a large signal dynamic parameter, and the time to accurately reach the final value, a small signal parameter that is a function of bandwidth and open-loop gain. Performance curves show

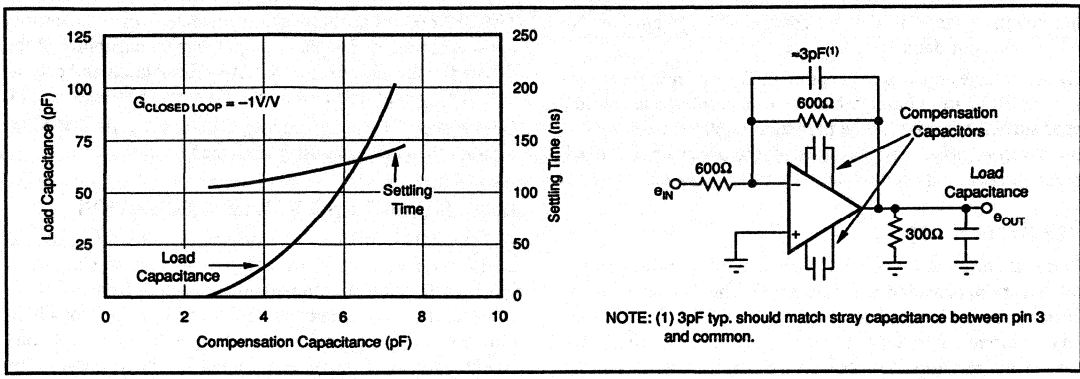


FIGURE 2. Capacitive Load Compensation and Response.

the OPA600 settling time to ±1%, ±0.1%, and ±0.01%. The best settling time is achieved in low closed-loop gain circuits.

Settling time is dependent upon compensation. Under-compensation will result in small phase margin, overshoot or instability. Over-compensation will result in poor settling time.

Figure 1 shows the recommended compensation to yield the specified settling time. Improved or optimum settling time may be achieved by individually compensating each device in the user's circuit since individual devices vary slightly from one to another, as do user's circuits.

SLEW RATE

Slew rate is primarily an output, large signal parameter. It has virtually no dependence upon the closed-loop gain or small signal bandwidth. Slew rate is dependent upon compensation and decreasing the compensation capacitor value will increase the available slew rate as shown in the performance curve.

The OPA600 slew rate may be increased by using an alternate compensation as shown in Figure 3. The slew rate will increase between 700 and 800V/µs typical, with 0.01% settling time increasing to between 175 and 190ns typical, and 0.1% settling time increasing to between 110 and 120ns typical.

For alternate doublet compensation refer to Figure 3. For a closed-loop gain equal to –1, delete C_1 and C_2 and add a series RC circuit (R = 22Ω, C = 0.01µF) Between pins 14 and 4. Make no connections to pins 11 and 5. Absolutely minimize the capacitance to these pins. If a connector is used for the OPA600, it is recommended that sockets for pins 11 and 5 be removed. For a PC board mount, it is recommended that the PC board holes be overdrilled for pins 11 and 5 and adjacent ground plane copper be removed. Effectively, this compensation places the dominant pole at the input stage, allowing the output stage to have no compensation and to slew as fast as possible. Bandwidth and settling time are impaired only slightly. For closed-loop gains other than –1, different values of R and C may be required.

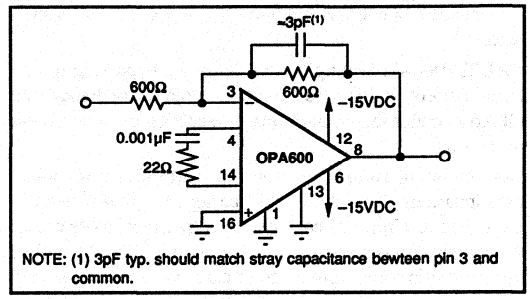


FIGURE 3. Amplifier Circuit for Increased Slew Rate.

OFFSET ADJUSTMENT

The offset voltage of the OPA600 may be adjusted to zero by connecting a 5kΩ resistor in series with a 10kΩ linear potentiometer in series with another 5kΩ resistor between pins 2 and 15, as shown in Figure 4. It is important that one end of each of the two resistors be located very close to pins 2 and 15 to isolate and avoid loading these sensitive terminals. The potentiometer should be a small noninductive type with the wiper connected to the positive supply. The leads connecting these components should be short, no longer than 0.5-inch, to avoid stray capacitance and stray signal pick-up. If the potentiometer must be located away from the immediate vicinity of the OPA600, extreme care must be observed with the sensitive leads. Locate the two 5kΩ resistors very close to pins 2 and 15.

Never connect $+V_{CC}$ directly to pin 2 or 15. Do not attempt to eliminate the 5kΩ resistors because at extreme rotation,

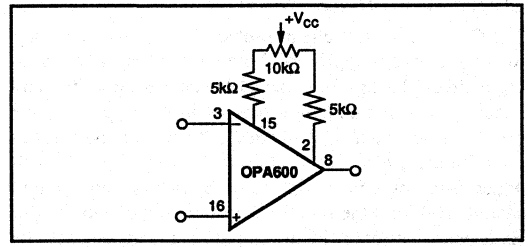


FIGURE 4. Offset Null Circuit.

the potentiometer will directly connect $+V_{CC}$ to pin 2 or 15 and permanent damage will result.

Offset voltage adjustment is optional. The potentiometer and two resistors are omitted when the offset voltage is considered sufficiently low for the particular application. For each microvolt of offset voltage adjusted, the offset voltage temperature sensitivity will change by ±0.004µV/°C.

CURRENT BOOST

External ability to bypass the internal current limiting resistors has been provided in the OPA600. This is referred to as current boost. Current boost enables the OPA600 to deliver large currents into heavy loads (±200mA at ±10V). To bypass the resistors and activate the current boost, connect pin 7 to $-V_{CC}$ at pin 6 with a short lead to minimize lead inductance and connect pin 9 to $+V_{CC}$ at pin 12 with a short lead.

CAUTION—Activating current boost by bypassing the internal current limiting resistors can permanently damage the OPA600 under fault conditions. See section on short circuit protection.

Not activating current boost is especially useful for initial breadboarding. The 50Ω (±5%) current limiting resistor in the collector circuit of each of the output transistors causes the output transistors to saturate; this limits the power dissipation in the output stage in case of a fault. Operating with the current boost not activated may also be desirable with small-signal outputs (i.e., ±1V) or when the load current is small.

Each resistor is internally capacitively-bypassed (0.01µF, ±20%) to allow the amplifier to deliver large pulses of current, such as to charge diode junctions or circuit capacitance and still respond quickly. The length of time that the OPA600 can deliver these current pulses is limited by the RC time constant.

The internal voltage drops, output voltage available, power dissipation, and maximum output current can be determined for the user's application by knowing the load resistance and computing:

$$V_{OUT} = 14\ [R_{LOAD} \div (50 + R_{LOAD})]$$

This applies for R_{LOAD} less than 100Ω and the current boost not activated. When R_{LOAD} is large, the peak output voltage is typically ±11V, which is determined by other factors within the OPA600.

SHORT-CIRCUIT PROTECTION

The OPA600 is short-circuit-protected for momentary short to common (<5s), typical of those encountered when probing a circuit during experimental breadboarding or troubleshooting. This is true only if pins 7 and 9 are open (current boost not activated.) An internal 50Ω resistor is in series with the collector of each of the output transistors, which under fault conditions will cause the output transistors to saturate and limit the power dissipation in the output stage. Extended application of an output short can damage the amplifier due to excessive power dissipation.

The OPA600 is not short-circuit-protected when the current boost is activated. The large output current capability of the OPA600 will cause excessive power dissipation and permanent damage will result even for momentary shorts to ground.

Output shorts to either supply will destroy the OPA600 whether the current boost is activated or not.

HEAT SINKING AND POWER DISSIPATION

The OPA600 is intended as a printed circuit board mounted device, and as such does not require a heat sink. It is specified for ambient temperature operation from –55°C to +125°C. However, the power dissipation must be kept within safe limits. At extreme temperature and under full load conditions, some form of heat sinking will be necessary. The use of a heat sink, or other heat dissipating means such as proximity to the ground plane, will result in cooler operating temperatures, better temperature performance, and improved reliability.

It may be necessary to physically connect the OPA600 to the printed circuit board ground plane, attach fins, tabs, etc., to dissipate the generated heat. Because of the wide variety of possibilities, this task is left to the user. For all applications it is recommended that the OPA600 be fully inserted into the printed circuit board and that the pin length be short. Heat will be dissipated through the ground plane and the AC performance will be its best.

With a maximum case temperature of +125°C and not exceeding the maximum junction of +175°C, a maximum power dissipation of 600mW is allowed in either output transistor.

TESTING

For static and low frequency dynamic measurements, the OPA600 may be tested in conventional operational amplifier test circuits, provided proper ground techniques are observed, excessive lead lengths are avoided, and care is maintained to avoid parasitic oscillations. The circuit in Figure 3 is recommended for low frequency functional testing, incoming inspection, etc. This circuit is less susceptible to stray capacitance, excessive lead length, parasitic tuned circuits, changing capacitive loads, etc. It does not yield optimum settling time. We recommend placing a resistor (approximately 300Ω) in series with each piece of test equipment, such as a DVM, to isolate loading effects on the OPA600.

To realize the full performance capabilities of the OPA600, high frequency techniques must be employed and the test fixture must not limit the amplifier. Settling time is the most critical dynamic test and Figure 5 shows a recommended OPA600 settling time test circuit schematic. Good grounding, truly square drive signals, minimum stray coupling, and small physical size are important.

The input pulse generator must have a flat topped, fast settling pulse to measure the true settling time of the amplifier. A circuit that generates a ±5V flat topped pulse is shown in Figure 6.

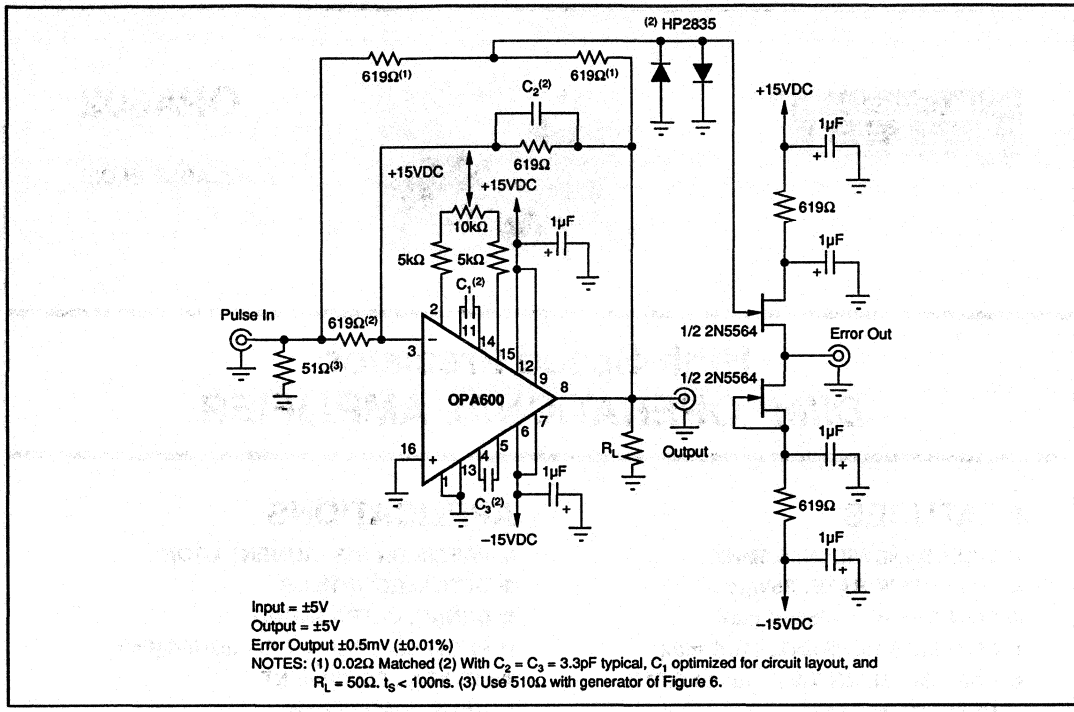


FIGURE 5. Settling Time and Slew Rate Test Circuit.

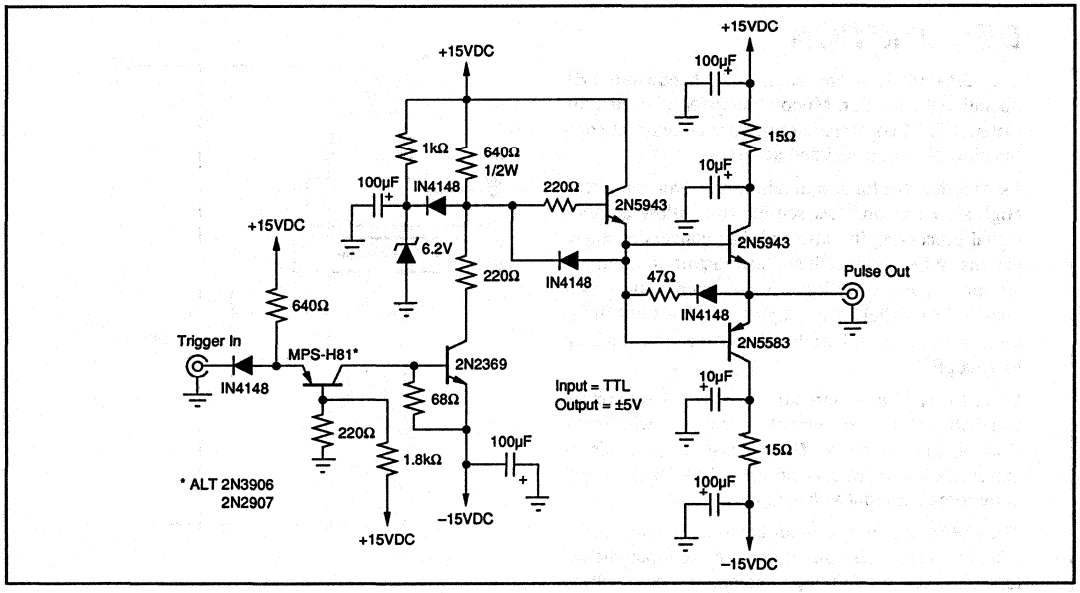


FIGURE 6. Flat Top Pulse Generator.

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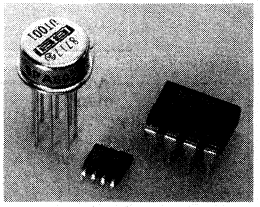


OPA602

AVAILABLE IN DIE

High-Speed Precision *Difet*® OPERATIONAL AMPLIFIER

FEATURES

- WIDE BANDWIDTH: 6.5MHz
- HIGH SLEW RATE: 35V/µs
- LOW OFFSET: ±250µV max
- LOW BIAS CURRENT: ±1pA max
- FAST SETTLING TIME: 1µs to 0.01%
- UNITY-GAIN STABLE

APPLICATIONS

- PRECISION INSTRUMENTATION
- OPTOELECTRONICS
- SONAR, ULTRASOUND
- PROFESSIONAL AUDIO EQUIPMENT
- MEDICAL EQUIPMENT
- DATA CONVERSION

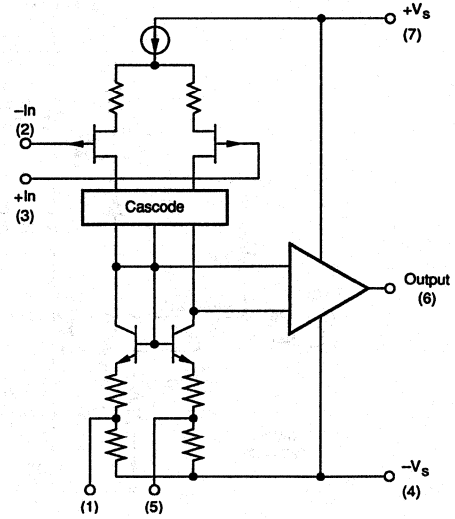
DESCRIPTION

The OPA602 is a precision, wide bandwidth FET operational amplifier. Monolithic ***Difet*** (dielectrically isolated FET) construction provides an unusual combination of high speed and accuracy.

Its wide-bandwidth design minimizes dynamic errors. High slew rate and fast settling time allow accurate signal processing in pulse and data conversion applications. Wide bandwidth and low distortion minimize AC errors. All specifications are rated with a 1kΩ resistor in parallel with 500pF load. The OPA602 is unity-gain stable and easily drives capacitive loads up to 1500pF.

Laser-trimmed input circuitry provides offset voltage and drift performance normally associated with precision bipolar op amps. ***Difet*** construction achieves extremely low input bias currents (1pA max) without compromising input voltage noise.

The OPA602's unique input cascode circuitry maintains low input bias current and precise input characteristics over its full input common-mode voltage range.



Difet® Burr-Brown Corp.

International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL

At V_S = ±15VDC and T_A = +25°C unless otherwise noted.

PARAMETER	CONDITIONS	OPA602AM/AP/AU			OPA602BM/SM/BP			OPA602CM			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
INPUT NOISE											
Voltage: f_O = 10Hz			*			23			*		nV/√Hz
f_O = 100Hz			*			19			*		nV/√Hz
f_O = 1kHz			*			13			*		nV/√Hz
f_O = 10kHz			*			12			*		nV/√Hz
f_B = 10Hz to 10kHz			*			1.4			*		µVrms
f_B = 0.1Hz to 10Hz			*			0.95			*		µVp-p
Current: f_B = 0.1Hz to 10Hz			*			12			*		fAp-p
f_O = 0.1Hz to 20kHz			*			0.6			*		fA/√Hz
OFFSET VOLTAGE											
Input Offset Voltage:											
M Package	V_{CM} = 0VDC		±300	±1000		±150	±500		±100	±250	µV
P Package			1	2		0.5	1				mV
U Package			1	3							mV
Over Specified Temperature											
M Package			±550			±250	±1000		±200	±500	µV
P, U Packages			±1.5			±0.75	±1.5				mV
Average Drift	T_A = T_{MIN} to T_{MAX}		*	±15		±3	±5		*	±2	µV/°C
Supply Rejection	±V_S = 12V to 18V	70	*		80	100		86	*		dB
BIAS CURRENT											
Input Bias Current	V_{CM} = 0VDC		±2	±10		±1	±2		±0.5	±1	pA
Over Specified Temperature			±20	±500		±20	±200		±10	±100	pA
SM Grade						±200	±2000				pA
OFFSET CURRENT											
Input Offset Current	V_{CM} = 0VDC		1	10		0.5	2		0.5	1	pA
Over Specified Temperature			20	500		20	200		10	100	pA
SM Grade						200	1000				pA
INPUT IMPEDANCE											
Differential			*			10^{13} ‖ 1			*		Ω ‖ pF
Common-Mode			*			10^{14} ‖ 3			*		Ω ‖ pF
INPUT VOLTAGE RANGE											
Common-Mode Input Range		*	*		±10.2	+13, −11		*	*		V
Common-Mode Rejection	V_{IN} = ±10VDC	75	*		88	100		92	*		dB
OPEN-LOOP GAIN, DC											
Open-Loop Voltage Gain	R_L ≥ 1kΩ	75	*		88	100		92	*		dB
FREQUENCY RESPONSE											
Gain Bandwidth	Gain = 100	3.5	*		4	6.5		5	*		MHz
Full Power Response	20Vp-p, R_L = 1kΩ		*			570			*		kHz
Slew Rate	V_O = ±10V, R_L = 1kΩ	20	*		24	35		28	*		V/µs
Settling Time: 0.1%	Gain = −1, R_L = 1kΩ		*			0.6			*		µs
0.01%	C_L = 500pF, 10V Step		*			1.0			*		µs
RATED OUTPUT											
Voltage Output	R_L = 1kΩ	±11	*		±11.5	+12.9, −13.8		*	*		V
Current Output	V_O = ±10VDC	*	*		±15	±20		*	*		mA
Output Resistance	1MHz, Open Loop		*			80			*		Ω
Load Capacitance Stability	Gain = +1		*			1500			*		pF
Short Circuit Current		±25	*		±30	±50		*	*		mA
POWER SUPPLY											
Rated Voltage			*			±15			*		VDC
Voltage Range,											
Derated Performance		*		*	±5		±18	*		*	VDC
Current, Quiescent	I_O = 0mADC		*	*		3	4		*	*	mA
Over Specified Temperature			*	*		3.5	4.5		*	*	mA
TEMPERATURE RANGE											
Specification	Ambient Temperature	*		*	−25		+85	*		*	°C
SM Grade					−55		+125				°C
Operating: M Package	Ambient Temperature	*		*	−55		+125	*		*	°C
P, U Packages		−25		+85	−25		+85				°C
Storage: M Package	Ambient Temperature	*		*	−65		+150	*		*	°C
P, U Packages		−40		+125	−40		+125				°C
θ_{JA}			*			200			*		°C/W

* Same specifications as OPA602BM.

ABSOLUTE MAXIMUM RATINGS

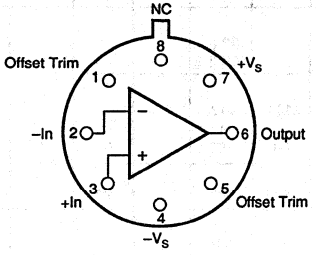
Supply Voltage	±18VDC
Internal Power Dissipation ($T_J \leq +175°C$)	1000mW
Differential Input Voltage	Total V_S
Input Voltage Range	$\pm V_S$
Storage Temperature Range	
M Package	–65°C to +150°C
P and U Packages	–40°C to +125°C
Operating Temperature Range	
M Package	–55°C to +125°C
P and U Packages	–25°C to + 85°C
Lead Temperature	
M and P Packages (soldering, 10s)	+300°C
U Package, SOIC (3s)	+260°C
Output Short Circuit to Ground (+25°C)	Continuous
Junction Temperature	+175°C

ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE	OFFSET VOLTAGE MAX (µV) AT 25°C
OPA602AM	TO-99	–25 to +85°C	±1000
OPA602BM	TO-99	–25 to +85°C	±500
OPA602CM	TO-99	–25 to +85°C	±250
OPA602SM	TO-99	–55 to +125°C	±500
OPA602AP	Plastic DIP	–25 to +85°C	±2000
OPA602BP	Plastic DIP	–25 to +85°C	±1000
OPA602AU	Plastic SOIC	–25 to +85°C	±3000

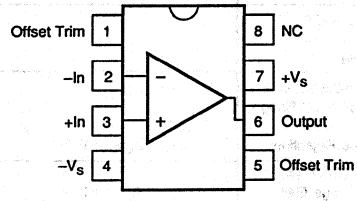
PIN CONFIGURATIONS

Top View — TO-99

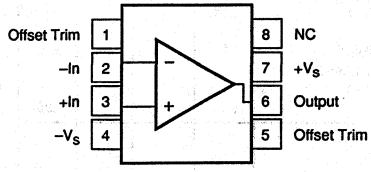


Case Connected to $+V_S$.

Top View — DIP



Top View — SOIC



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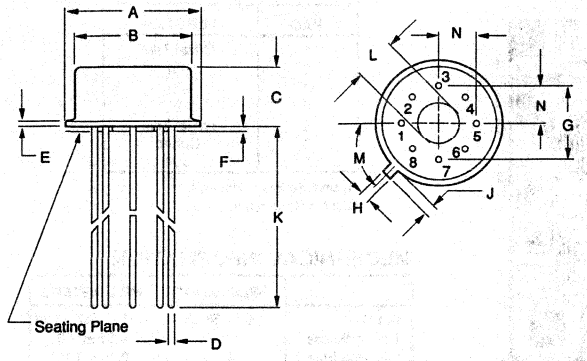
MECHANICAL

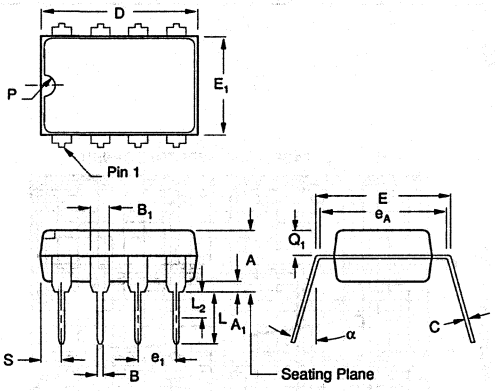
M Package — Metal TO-99



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.335	.370	8.51	9.40
B	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.200 BASIC		5.08 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500	—	12.7	—
L	.110	.160	2.79	4.06
M	45° BASIC		45° BASIC	
N	.095	.105	2.41	2.67

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.

P Package — 8-Pin Plastic DIP

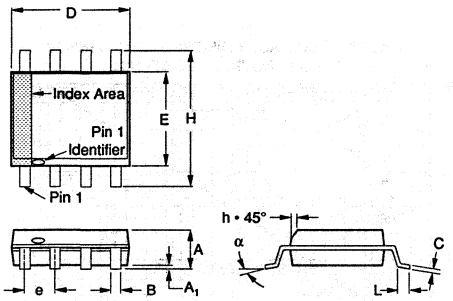


DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.155	.200	3.94	5.08
A_1	.020	.050	0.51	1.27
B	.014	.020	0.36	0.51
B_1	.045	.065	1.14	1.65
C	.008	.012	0.20	0.30
D (1)	.370	.400	9.40	10.16
E	.300	.325	7.62	8.26
E_1	.240	.260	6.10	6.60
e_1	.100 BASIC		2.54 BASIC	
e_A	.300 BASIC		7.62 BASIC	
L	.125	.150	3.18	3.81

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
L_2 (2)	0	.030	0.00	0.76
α	0°	15°	0°	15°
P	.015	.050	0.38	1.270
Q_1	.040	.075	1.02	1.91
S (1)	.015	.050	0.38	1.27

(1) Not JEDEC Std.
(2) e_1 and e_A apply in zone L_2 when unit installed.
NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

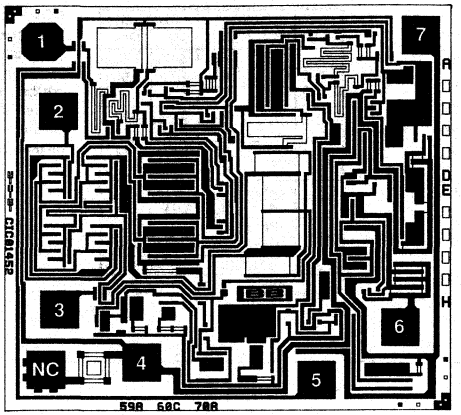
U Package — 8-Pin SO-8 Surface Mount



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.054	.068	1.37	1.73
A_1	.004	.009	0.10	0.23
B	.014	.019	0.36	0.48
C	.008	.0098	0.20	0.25
D	.189	.196	4.80	4.98
E	.150	.157	3.81	3.99
e	.050 BASIC		1.27 BASIC	
H	.229	.244	5.82	6.20
h	.010	.019	0.25	0.48
L	.016	.050	0.41	1.27
N	8		8	
α	0°	8°	0°	8°

NOTES:
1. Dimensioning and tolerancing per ANSI Y14.5M–1982.
2. "D" and "E" are reference datums and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm (.086 in.)
3. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the cross-hatched area.
4. "L" is the length of the terminal for soldering to a substrate.
5. "N" is the number of terminal positions.

DICE INFORMATION



OPA602 DIE TOPOGRAPHY

PAD	FUNCTION
1	Offset Trim
2	–In
3	+In
4	$-V_S$
5	Offset Trim
6	Output
7	$+V^S$

Substrate Bias: Isolated.
NC: No Connection.

MECHANICAL INFORMATION

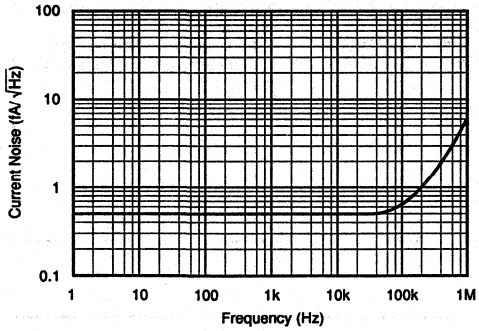
	MILS (0.001")	MILLIMETERS
Die Size	63 x 58 ±5	1.60 x 1.47 ±0.13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.10 x 0.10
Backing:	None	

See "DICE PRODUCTS" Section 17 in Data Book Supplement Volume 33c, or contact Burr-Brown for current information.

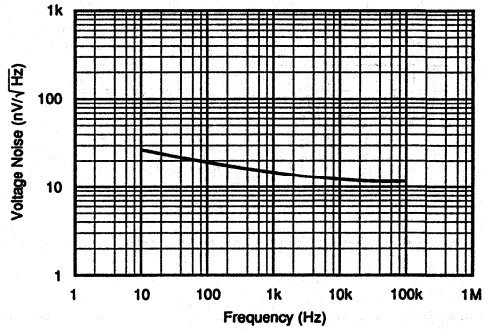
TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_S = ±15VDC unless otherwise noted.

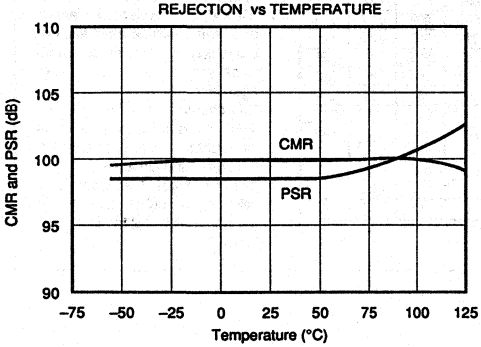
INPUT CURRENT NOISE SPECTRAL DENSITY



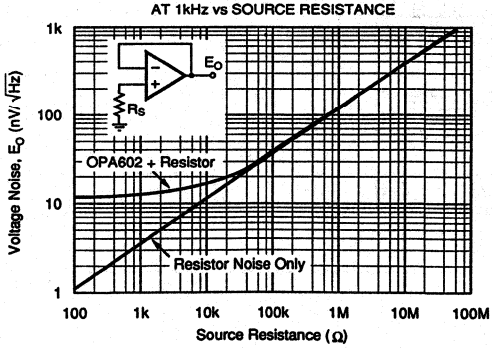
INPUT VOLTAGE NOISE SPECTRAL DENSITY



POWER SUPPLY REJECTION AND COMMON-MODE REJECTION vs TEMPERATURE



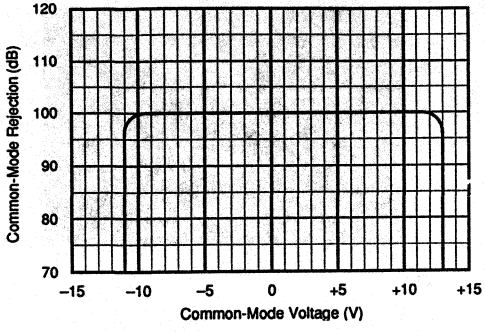
TOTAL INPUT VOLTAGE NOISE SPECTRAL DENSITY AT 1kHz vs SOURCE RESISTANCE



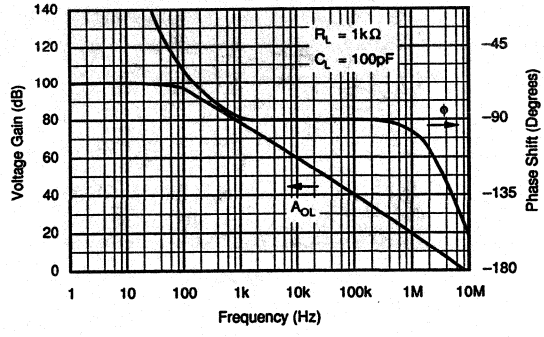
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_S = ±15VDC unless otherwise noted.

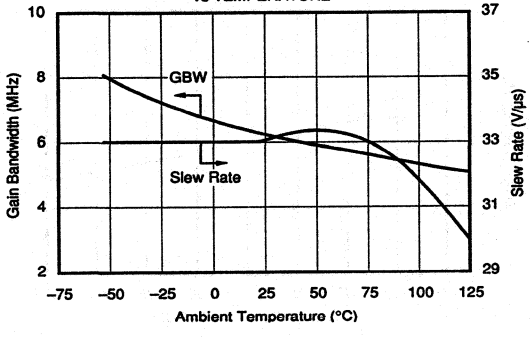
COMMON-MODE REJECTION
vs INPUT COMMON-MODE VOLTAGE



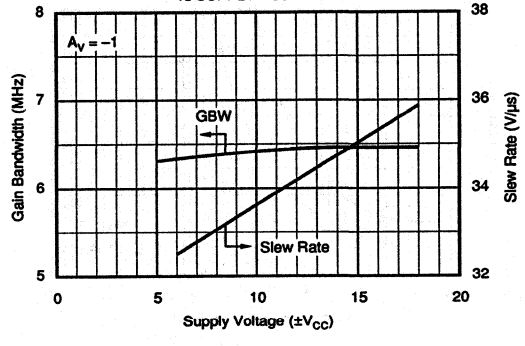
OPEN-LOOP FREQUENCY RESPONSE



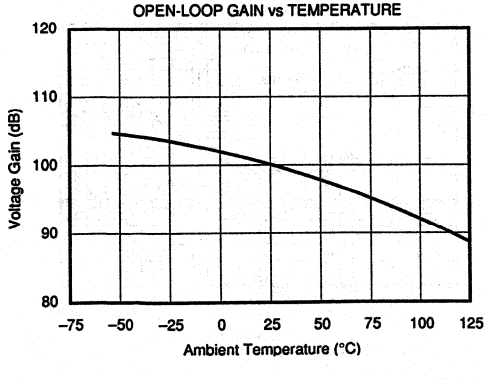
GAIN BANDWIDTH AND SLEW RATE
vs TEMPERATURE



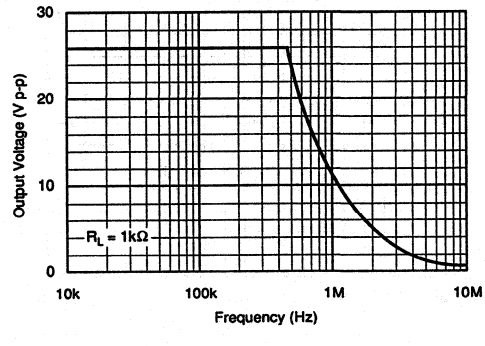
GAIN BANDWIDTH AND SLEW RATE
vs SUPPLY VOLTAGE



OPEN-LOOP GAIN vs TEMPERATURE



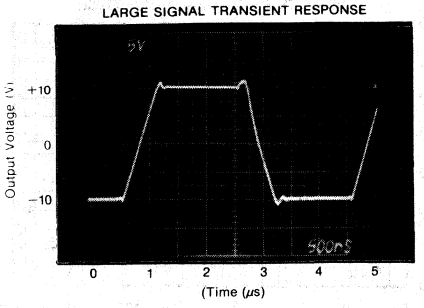
MAXIMUM OUTPUT VOLTAGE SWING
vs FREQUENCY



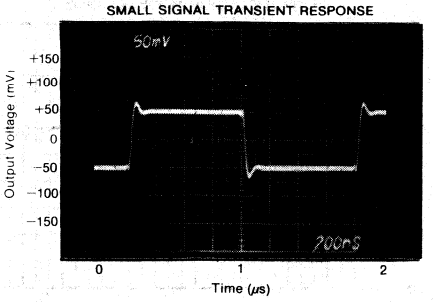
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_S = ±15VDC unless otherwise noted.

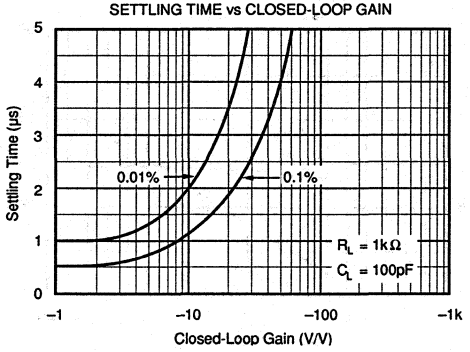
LARGE SIGNAL TRANSIENT RESPONSE



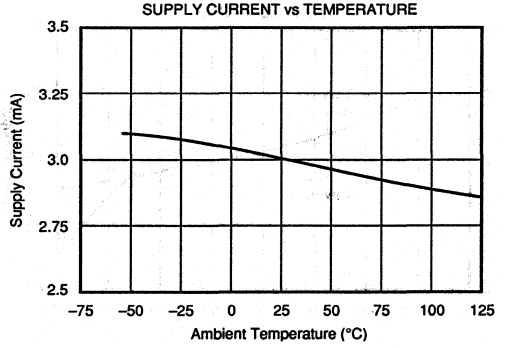
SMALL SIGNAL TRANSIENT RESPONSE



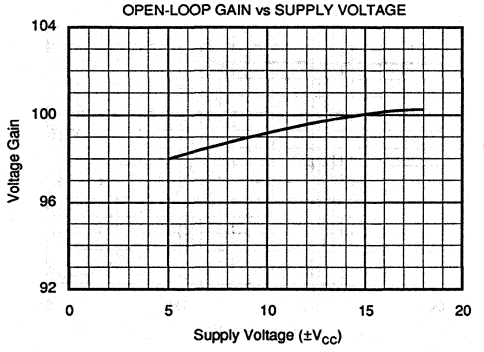
SETTLING TIME vs CLOSED-LOOP GAIN



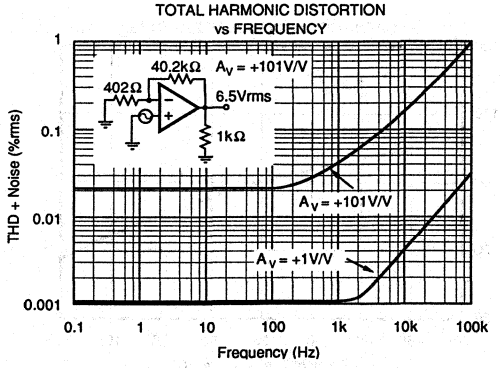
SUPPLY CURRENT vs TEMPERATURE



OPEN-LOOP GAIN vs SUPPLY VOLTAGE



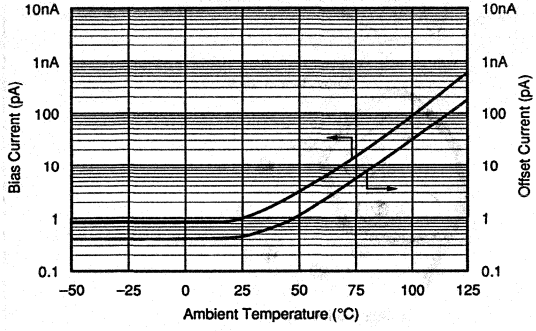
TOTAL HARMONIC DISTORTION vs FREQUENCY



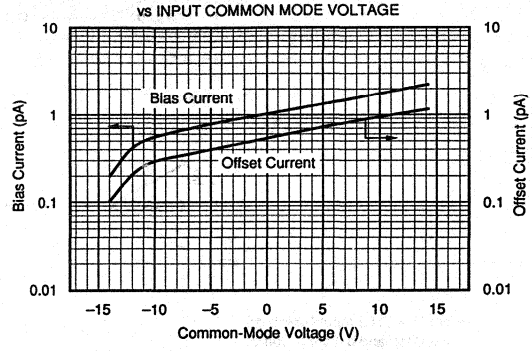
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_S = ±15VDC unless otherwise noted.

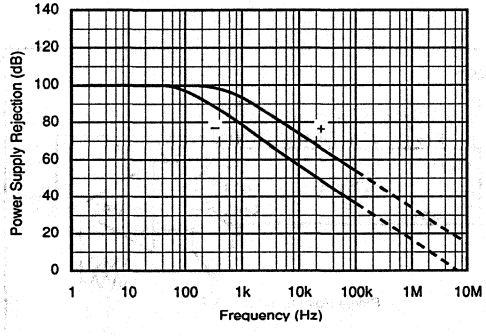
BIAS AND OFFSET CURRENT vs TEMPERATURE



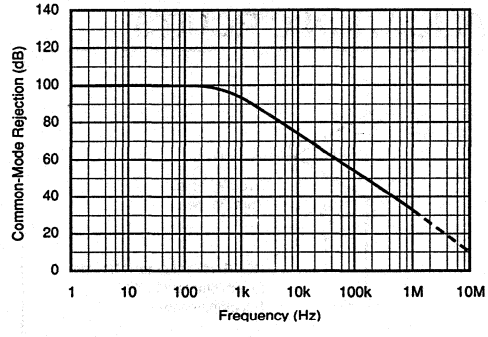
BIAS AND OFFSET CURRENT vs INPUT COMMON MODE VOLTAGE



POWER SUPPLY REJECTION vs FREQUENCY



COMMON-MODE REJECTION vs FREQUENCY



APPLICATIONS INFORMATION

Unity-gain stability with good phase margin and excellent output drive characteristics bring freedom from the subtle problems associated with other high speed amplifiers. But with any high speed, wide bandwidth circuitry, careful circuit layout will ensure best performance. Make short, direct interconnections and avoid stray wiring capacitance—especially at the inverting input pin.

Power supplies should be bypassed with good high frequency capacitors positioned close to the op amp pins. In most cases 0.1µF ceramic capacitors are adequate. Applications with heavier loads and fast transient waveforms may benefit from use of additional 1.0µF tantalum bypass capacitors.

INPUT BIAS CURRENT GUARDING

Leakage currents across printed circuit boards can easily exceed the input bias current of the OPA602. A circuit board "guard" pattern (Figure 1) is an effective solution to difficult leakage problems. This guard pattern must be repeated on all layers of a multilayer board. By surrounding critical high impedance input circuitry with a low impedance circuit connection at the same potential, leakage currents will flow harmlessly to the low impedance node.

Input bias current may also be degraded by improper handling or cleaning. Contamination from handling parts and circuit boards may be cleaned with appropriate solvents and de-ionized water. Each rinsing operation should be followed by a 30-minute bake at +85°C.

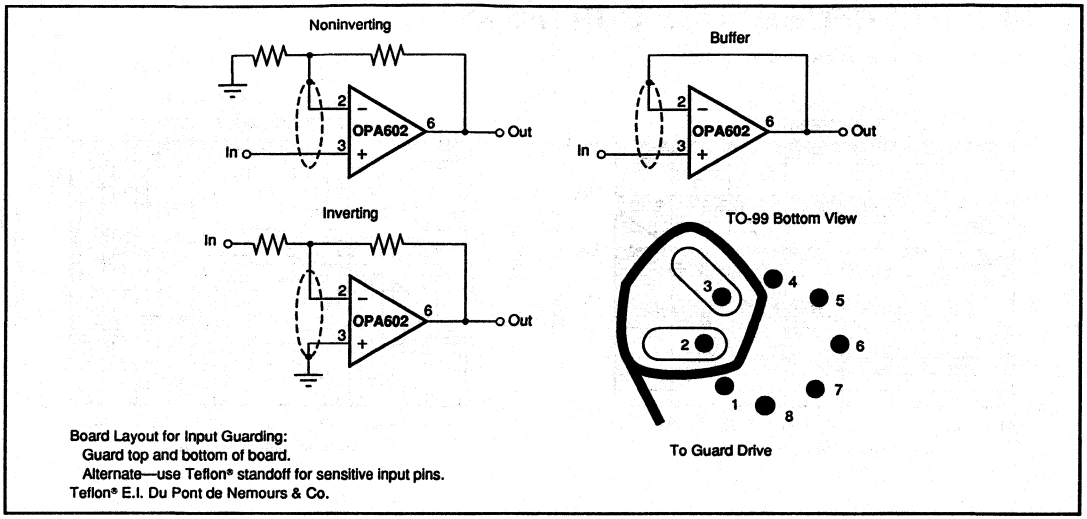


FIGURE 1. Connection of Input Guard.

APPLICATION CIRCUITS

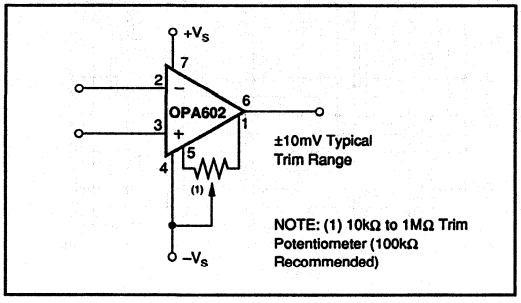


FIGURE 2. Offset Voltage Trim.

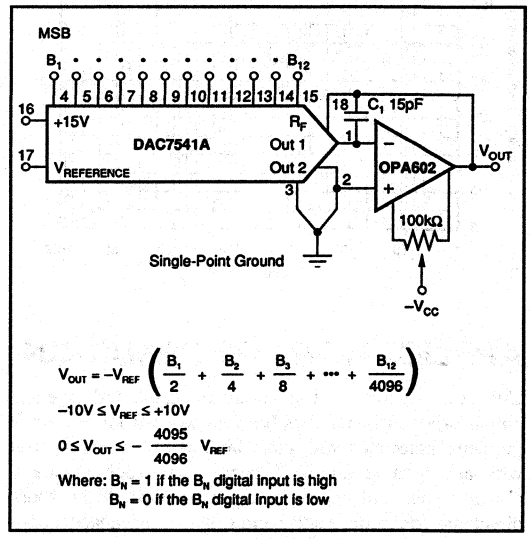


FIGURE 3. Voltage Output D/A Converter.

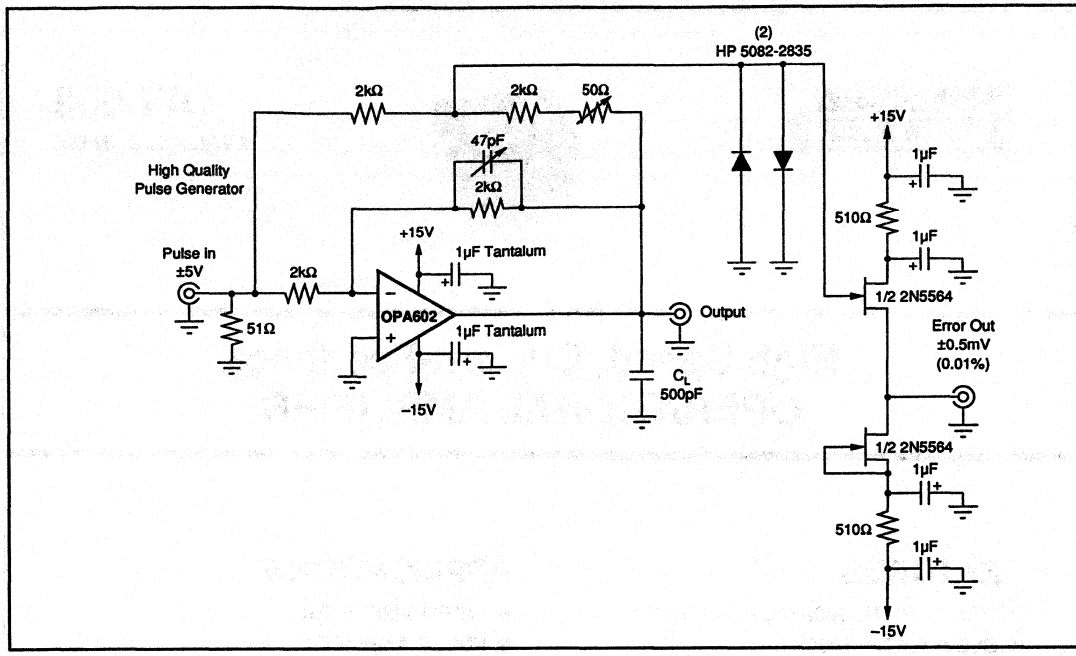


FIGURE 4. Settling Time and Slew Rate Test Circuit.

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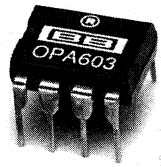


OPA603

AVAILABLE IN DIE

High Speed, Current-Feedback OPERATIONAL AMPLIFIER

FEATURES

- BANDWIDTH: 100MHz, G = 1 to 10
- SLEW RATE: 1000V/μs
- FAST SETTLING TIME: 50ns to 0.1%
- WIDE SUPPLY RANGE: ±4.5 to ±18V
- HIGH OUTPUT CURRENT: ±150mA peak
- 8-PIN PLASTIC MINI-DIP PACKAGE
- SOL-16 SURFACE-MOUNT PACKAGE

APPLICATIONS

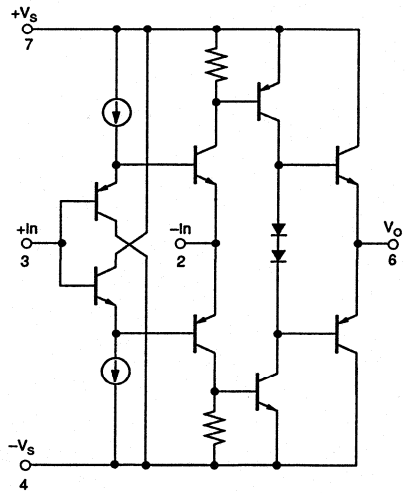
- VIDEO AMPLIFIER
- PULSE AMPLIFIER
- SONAR, ULTRASOUND CIRCUITRY
- ATE PIN DRIVERS
- LINE DRIVERS
- FAST DATA ACQUISTION
- WAVEFORM GENERATORS

DESCRIPTION

The OPA603 is a high-speed current-feedback op amp with guaranteed specifications at both ±5V and ±15V power supplies. It can deliver full ±10V signals into 150Ω loads with up to 1000V/μs slew rate. This allows it to drive terminated 75Ω cables. With 150mA peak output current capability it is suitable for driving load capacitance or long lines at high speed.

In contrast with conventional op amps, the current-feedback approach provides nearly constant bandwidth and settling time over a wide range of closed-loop voltage gains.

The OPA603 is available in a plastic 8-pin dual-in-line and SOL-16 surface-mount packages, specified for the industrial temperature range.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS, V_S = ±15V

ELECTRICAL

T_A = +25°C, R_L = 150Ω unless otherwise noted.

PARAMETER	CONDITIONS	OPA603AP/AU MIN	OPA603AP/AU TYP	OPA603AP/AU MAX	UNITS
INPUT OFFSET VOLTAGE					
Initial				5	mV
vs Temperature			8		µV/°C
vs Common-Mode Voltage	V_{CM} = ±10V	50	60		dB
vs Supply (tracking) Voltage	V_S = ±12V to ±18V	80	85		dB
vs Supply (non-tracking)[1]	$\|V_S\|$ = 12V to 18V	55	60		dB
+INPUT BIAS CURRENT					
Initial				5	µA
vs Temperature			30		nA/°C
vs Common-Mode	V_{CM} = ±10V		200	500	nA/V
vs Supply (tracking)	V_S = ±12V to ±18V		50	100	nA/V
vs Supply (non-tracking)[1]	$\|V_S\|$ = 12V to 18V		150	300	nA/V
–INPUT BIAS CURRENT					
Initial				25	µA
vs Temperature			300		nA/°C
vs Common-Mode	V_{CM} = ±10V		200	600	nA/V
vs Supply (tracking)	V_S = ±12V to ±18V		300	500	nA/V
vs Supply (non-tracking)[1]	$\|V_S\|$ = 12V to 18V		1500	2000	nA/V
INPUT IMPEDANCE					
+Input			5 || 2		MΩ || pF
–Input			30 || 2		Ω || pF
OPEN LOOP CHARACTERISTICS					
Transresistance	V_O = ±10V	300	440		kΩ
Transcapacitance			1.8		pF
OUTPUT CHARACTERISTICS					
Voltage	R_L = 150Ω	±10	±12		V
Peak Current			150		mA
Short-Circuit Current[2]	V_O = 0V		250		mA
Output Resistance, Open-Loop			70		Ω
FREQUENCY RESPONSE	G = +2				
Small-Signal Bandwidth[3]		70	160		MHz
Gain Flatness, ±0.5dB		35	75		MHz
Full-Power Bandwidth	V_O = 20Vp-p		10		MHz
Differential Gain	f = 4.43MHz, V_O = 1V		0.03		%
Differential Phase	f = 4.43MHz, V_O = 1V		0.025		Degrees
TIME DOMAIN RESPONSE	G = +2				
Propagation Delay			10		ns
Rise and Fall Time			10		ns
Settling Time to 0.10%	10V Step		50		ns
Slew Rate			1000		V/µs
DISTORTION	G = +2, R_L = 100Ω, f = 10MHz				
2nd Harmonic Distortion	V_O = 0.2Vp-p	–60	–65		dBc
3rd Harmonic Distortion	V_O = 0.2Vp-p	–70	–90		dBc
POWER SUPPLY					
Specified Operating Voltage			±15		V
Operating Voltage Range		±4.5		±18	V
Current			±21	±25	mA
TEMPERATURE RANGE					
Specification		–25		+85	°C
Storage		–40		+150	°C
THERMAL RESISTANCE, $\theta_{JUNCTION-AMBIENT}$	Soldered to Printed Circuit		90		°C/W

NOTES: (1) One power supply fixed at 15V; the other supply varied from 12V to 18V. (2) Observe power derating curve. (3) See bandwidth versus gain curve, Figure 5.

SPECIFICATIONS, $V_S = \pm 5V$

ELECTRICAL

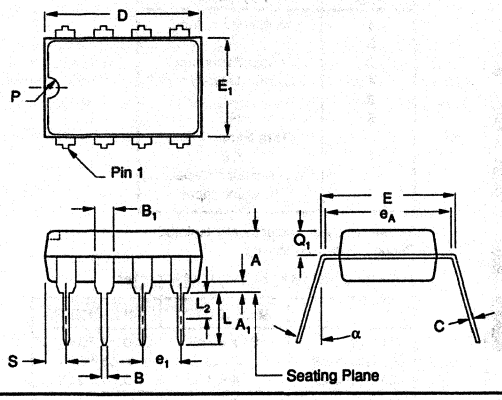
T_A = +25°C, R_L = 75Ω unless otherwise noted.

PARAMETER	CONDITIONS	OPA603AP/AU MIN	OPA603AP/AU TYP	OPA603AP/AU MAX	UNITS
INPUT OFFSET VOLTAGE					
Initial				6	mV
vs Temperature			8		µV/°C
vs Common-Mode	V_{CM} = ±3V	50	55		dB
vs Supply (tracking)	V_S = ±4V to ±6V	75	80		dB
vs Supply (non-tracking)(1)	$\|V_S\|$ = 4V to 6V	55	60		dB
+INPUT BIAS CURRENT					
Initial				5	µA
vs Temperature			30		nA/°C
vs Common-Mode	V_{CM} = ±3V		350	600	nA/V
vs Supply (tracking)	V_S = ±4V to ±6V		100	200	nA/V
vs Supply (non-tracking)(1)	$\|V_S\|$ = 4V to 6V		200	300	nA/V
–INPUT BIAS CURRENT					
Initial				25	µA
vs Temperature			300		nA/°C
vs Common-Mode	V_{CM} = ±3V		300	600	nA/V
vs Supply (tracking)	V_S = ±4V to ±6V		500	700	nA/V
vs Supply (non-tracking)(1)	$\|V_S\|$ = 4V to 6V		2500	3000	nA/V
INPUT IMPEDANCE					
+Input			3.3 || 2		MΩ || pF
–Input			30 || 2		Ω || pF
OPEN LOOP CHARACTERISTICS					
Transresistance	V_O = ±2V	225	330		kΩ
Transcapacitance			2.4		pF
OUTPUT CHARACTERISTICS					
Voltage	R_L = 75Ω	±2	±2.75		V
Peak Current			150		mA
Short-Circuit Current(2)	V_O = 0V		250		mA
Output Resistance, Open-Loop			80		Ω
FREQUENCY RESPONSE	G = +2				
Small-Signal Bandwidth(3)			140		MHz
Gain Flatness, ±0.5dB			65		MHz
Full-Power Bandwidth			20		MHz
Differential Gain	f = 4.43MHz, V_O = 1V, R_L = 150Ω		0.03		%
Differential Phase	f = 4.43MHz, V_O = 1V, R_L = 150Ω		0.025		Degrees
TIME DOMAIN RESPONSE	G = +2, R_L = 100Ω				
Propagation Delay			15		ns
Rise and Fall Time			20		ns
Settling Time to 0.10%			60		ns
Slew Rate			750		V/µs
DISTORTION	G = +2, R_L = 100Ω, f = 10MHz				
2nd Harmonic Distortion	V_O = 0.2Vp-p		–67		dBc
3rd Harmonic Distortion	V_O = 0.2Vp-p		–78		dBc
POWER SUPPLY					
Specified Operating Voltage			±5		V
Operating Voltage Range		±4.5		±18	V
Current			±21	±25	mA
TEMPERATURE RANGE					
Specification		–25		+85	°C
Storage		–40		+150	°C
THERMAL RESISTANCE, $\theta_{JUNCTION\text{-}AMBIENT}$	Soldered to Printed Circuit		90		°C/W

NOTES: (1) One power supply fixed at 5V; the other supply varied from 4V to 6V. (2) Observe power derating curve. (3) See bandwidth versus gain curves, Figure 5.

MECHANICAL

P Package — 8-Pin Plastic DIP

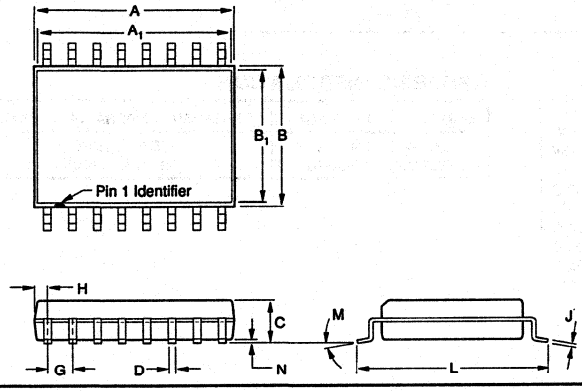


DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.155	.200	3.94	5.08
A1	.020	.050	0.51	1.27
B	.014	.020	0.36	0.51
B1	.045	.065	1.14	1.65
C	.008	.012	0.20	0.30
D(1)	.370	.400	9.40	10.16
E	.300	.325	7.62	8.26
E1	.240	.260	6.10	6.60
e1	.100 BASIC		2.54 BASIC	
eA	.300 BASIC		7.62 BASIC	
L	.125	.150	3.18	3.81

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
L2(2)	0	.030	0.00	0.76
α	0°	15°	0°	15°
P	.015	.050	0.38	1.270
Q1	.040	.075	1.02	1.91
S(1)	.015	.050	0.38	1.27

(1) Not JEDEC Std.
(2) e_1 and e_A apply in zone L_2 when unit installed.
NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

U Package — 16-Pin SOIC

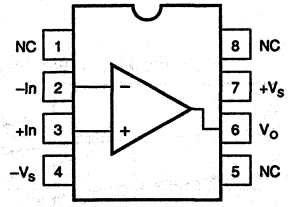


DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.400	.416	10.16	10.57
A1	.388	.412	9.86	10.46
B	.286	.302	7.26	7.67
B1	.268	.286	6.81	7.26
C	.093	.109	2.36	2.77
D	.015	.020	0.38	0.51
G	.050 BASIC		1.27 BASIC	
H	.022	.038	0.56	0.97
J	.008	.012	0.20	0.30
L	.391	.421	9.93	10.69
M	5° TYP		5° TYP	
N	.000	.012	0.00	0.30

NOTE: Leads in true position within 0.010" (0.25mm) R at MMC at seating plane.

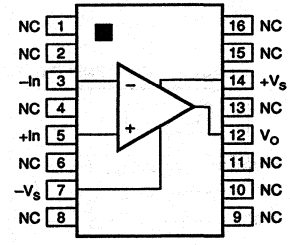
PIN CONFIGURATION

Top View — DIP



NC: No Internal Connection.
Solder to ground plane for improved heat dissipation.

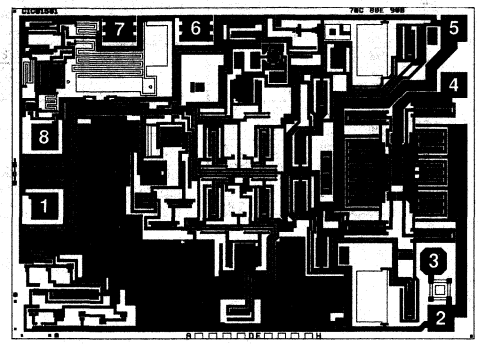
Top View — SOL-16



NC: No Internal Connection.
Solder to ground plane for improved heat dissipation.

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

DICE INFORMATION



OPA603 DIE TOPOGRAPHY

PAD	FUNCTION
1	Noninverting Input
2	$-V_S$
3	Laser Alignment
4	V_O (Output)
5	$+V_S$
6	RT (Trim Sense Point)
7	CE (Compensation Capacitor)
8	Inverting Input

Substrate Bias: Dielectrically Isolated. Recommend tying to $+V_S$.

MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	94 x 69 ±5	2.39 x 1.75 ±0.13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.10 x 0.10
Backing	Gold	

See "DICE PRODUCTS" Section 17 in Data Book Supplement Volume 33c, or contact Burr-Brown for current information.

ABSOLUTE MAXIMUM RATINGS

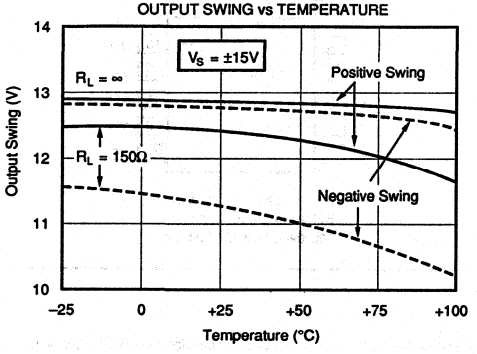
Supply Voltage	±18V
Input Voltage Range	$\pm V_S$
Differential Input Voltage	±6V
Power Dissipation	See derating curve
Operating Temperature	+100°C
Storage Temperature	+150°C
Junction Temperature	+150°C
Lead Temperature (soldering, 10s)	+300°C
(soldering SOL-16 package, 3s)	+260°C

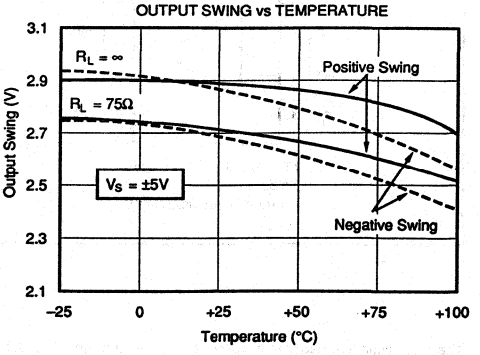
ORDERING INFORMATION

MODEL	PACKAGE	SPECIFIED TEMPERATURE RANGE
OPA603AP	Plastic DIP	–25°C to +85°C
OPA603AU	SOL-16	–25°C to +85°C

TYPICAL PERFORMANCE CURVES

T_A = +25°C unless otherwise noted.

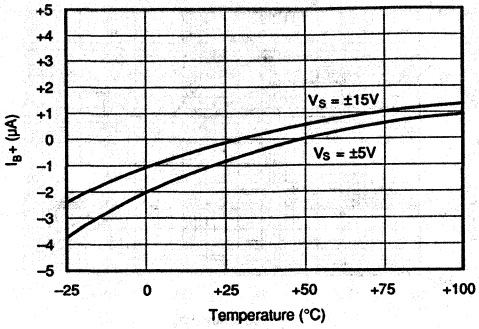




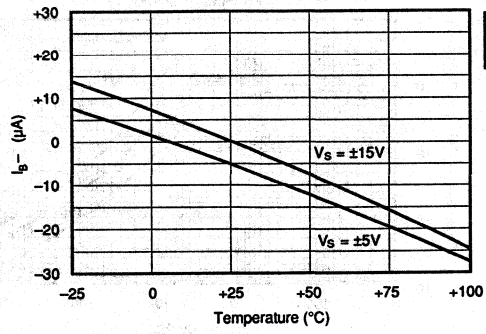
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C unless otherwise noted.

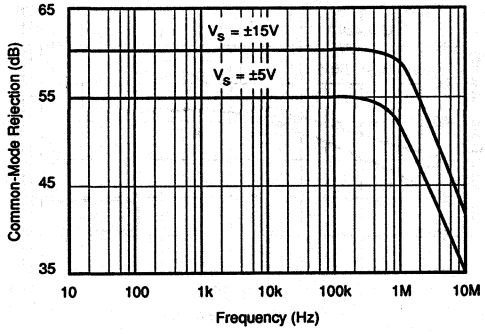
NONINVERTING INPUT BIAS CURRENT vs TEMPERATURE



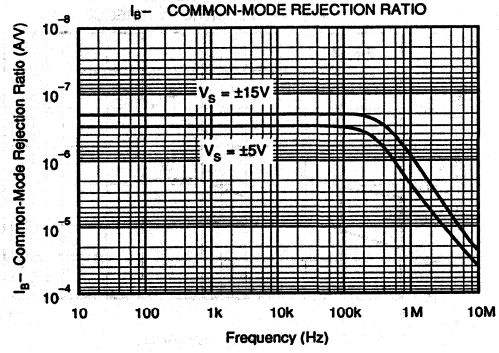
INVERTING INPUT BIAS CURRENT vs TEMPERATURE



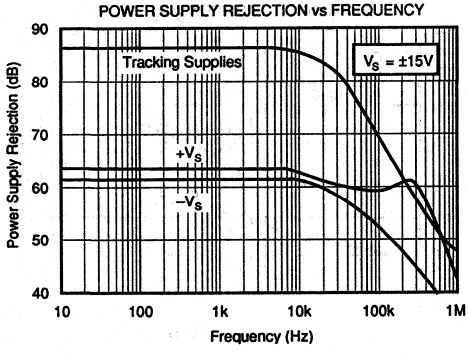
COMMON-MODE REJECTION vs FREQUENCY



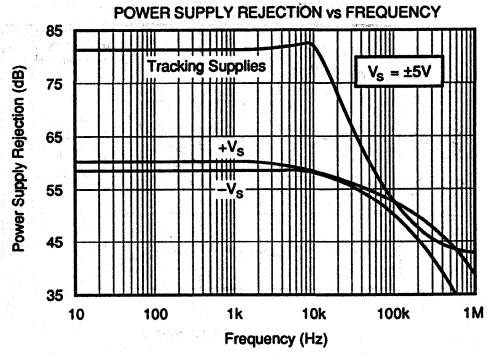
I_B– COMMON-MODE REJECTION RATIO



POWER SUPPLY REJECTION vs FREQUENCY

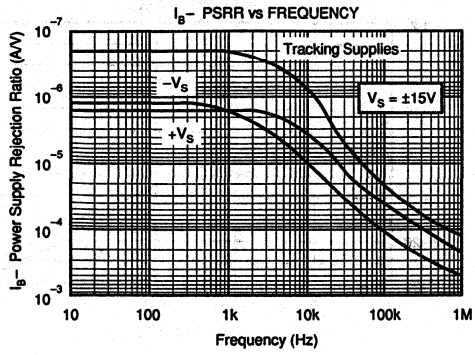


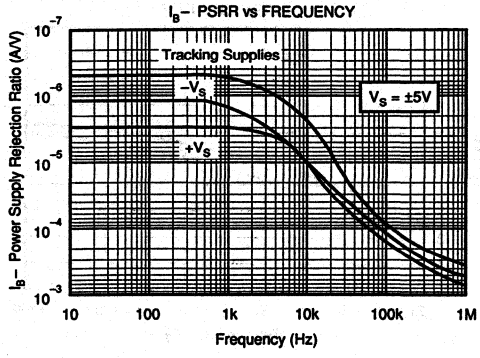
POWER SUPPLY REJECTION vs FREQUENCY

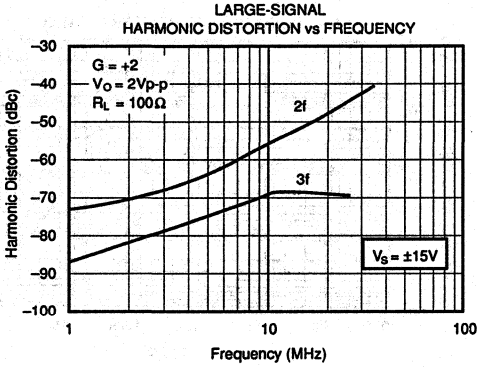


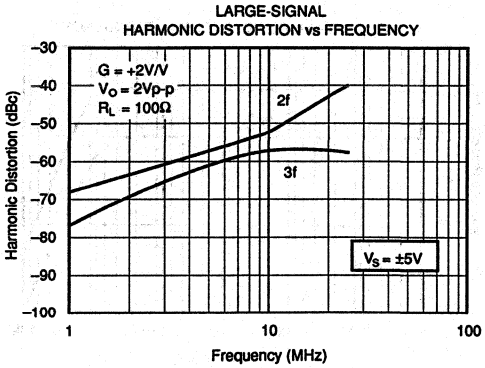
TYPICAL PERFORMANCE CURVES (CONT)

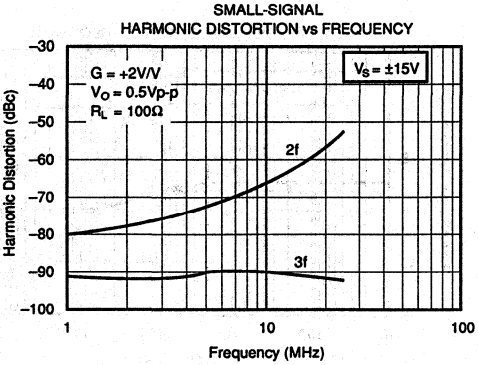
T_A = +25°C unless otherwise noted.

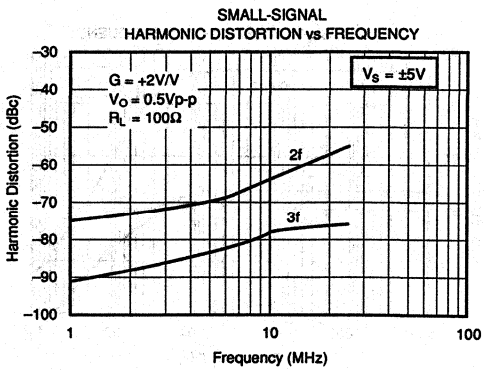








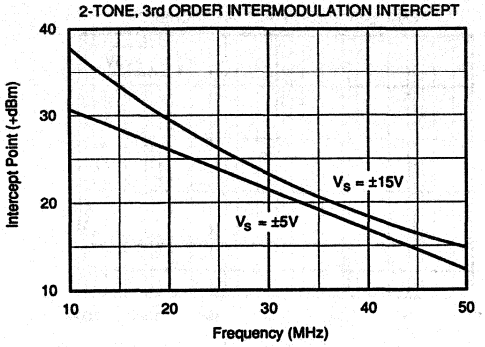




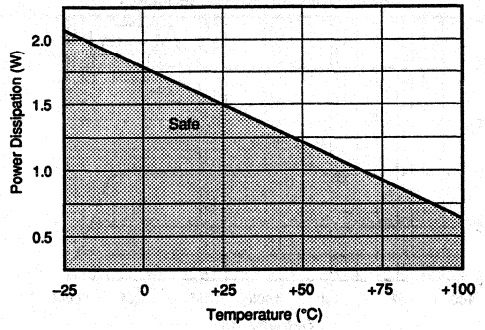
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C unless otherwise noted.

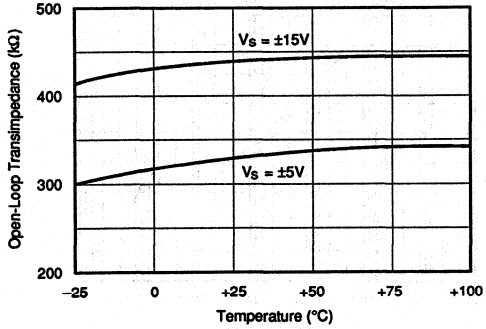
2-TONE, 3rd ORDER INTERMODULATION INTERCEPT



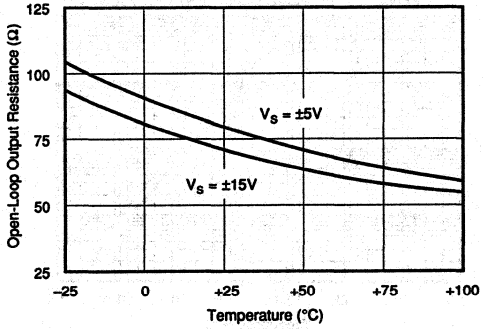
MAXIMUM POWER DISSIPATION vs TEMPERATURE



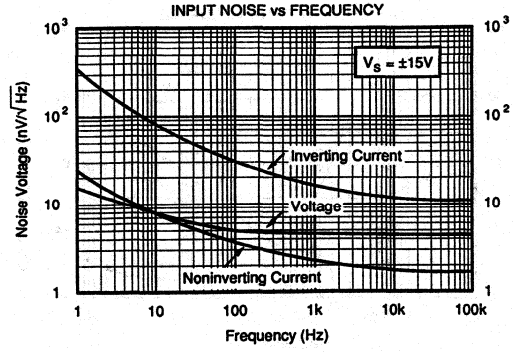
OPEN-LOOP TRANSIMPEDANCE vs TEMPERATURE



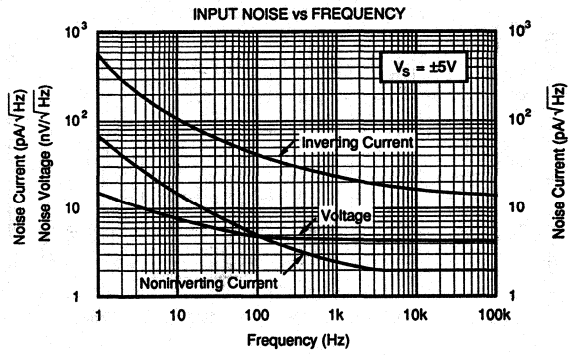
OPEN-LOOP OUTPUT RESISTANCE vs TEMPERATURE



INPUT NOISE vs FREQUENCY



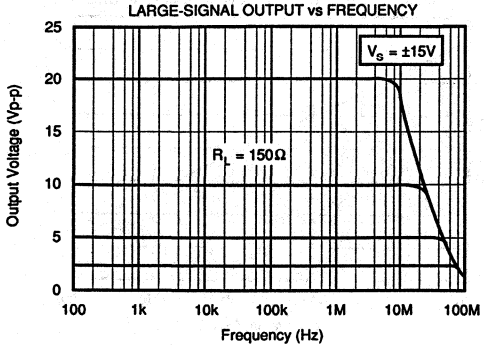
INPUT NOISE vs FREQUENCY



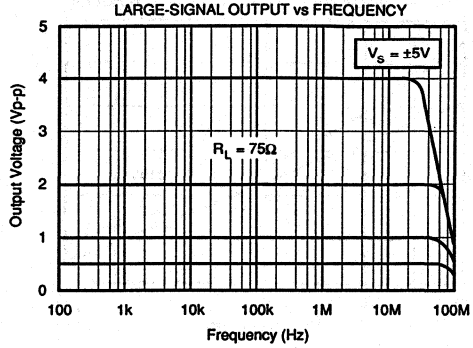
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C unless otherwise noted.

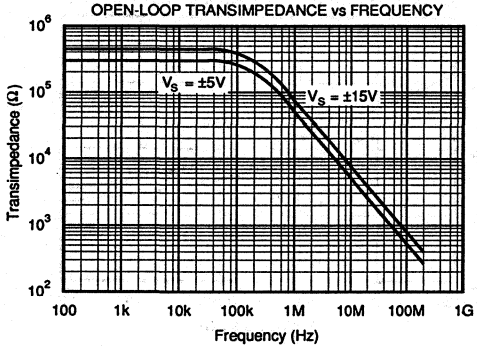
LARGE-SIGNAL OUTPUT vs FREQUENCY



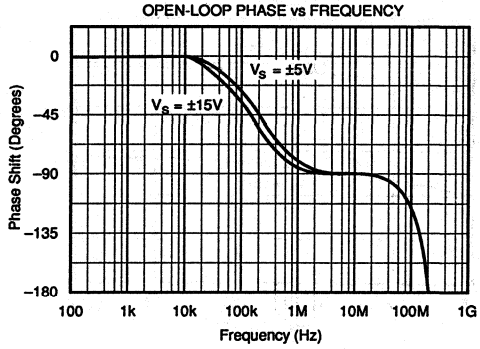
LARGE-SIGNAL OUTPUT vs FREQUENCY



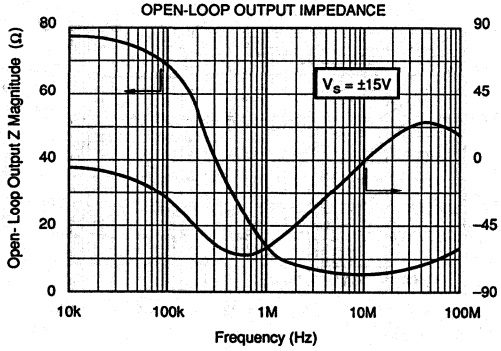
OPEN-LOOP TRANSIMPEDANCE vs FREQUENCY



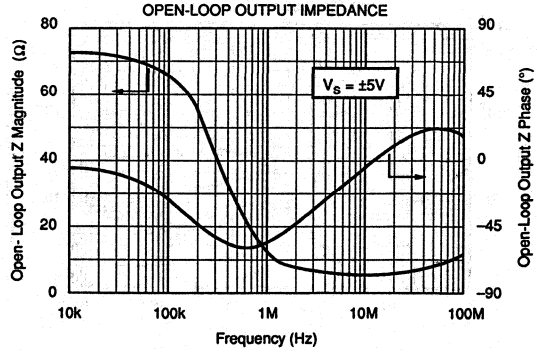
OPEN-LOOP PHASE vs FREQUENCY



OPEN-LOOP OUTPUT IMPEDANCE



OPEN-LOOP OUTPUT IMPEDANCE



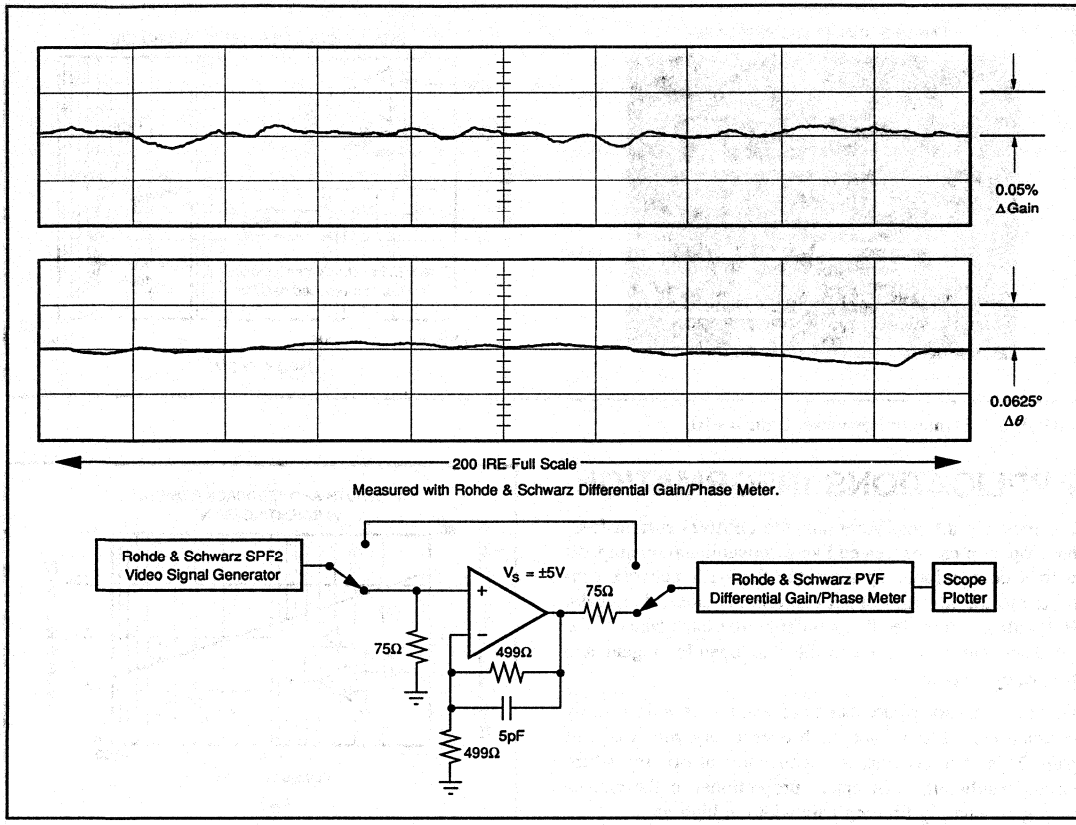


FIGURE 1. Video Differential Gain/Phase Performance.

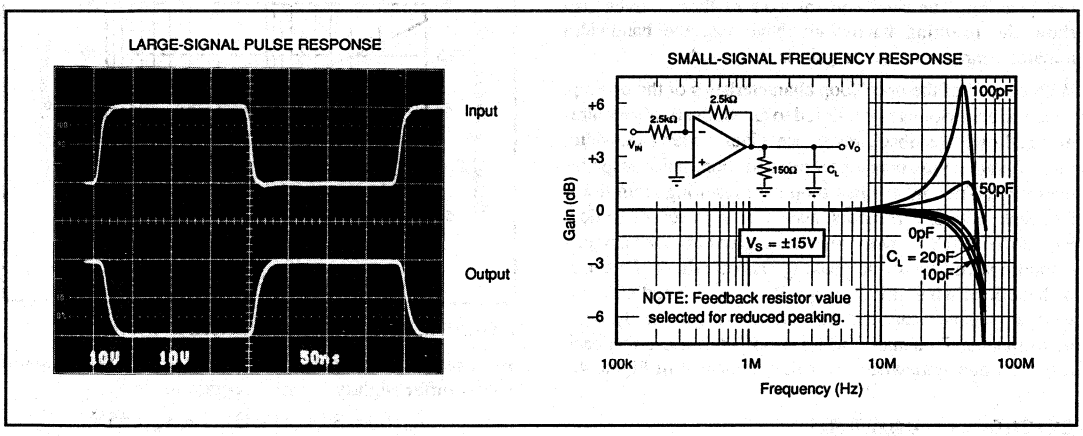


FIGURE 2. Dynamic Response, Inverting Unity-Gain.

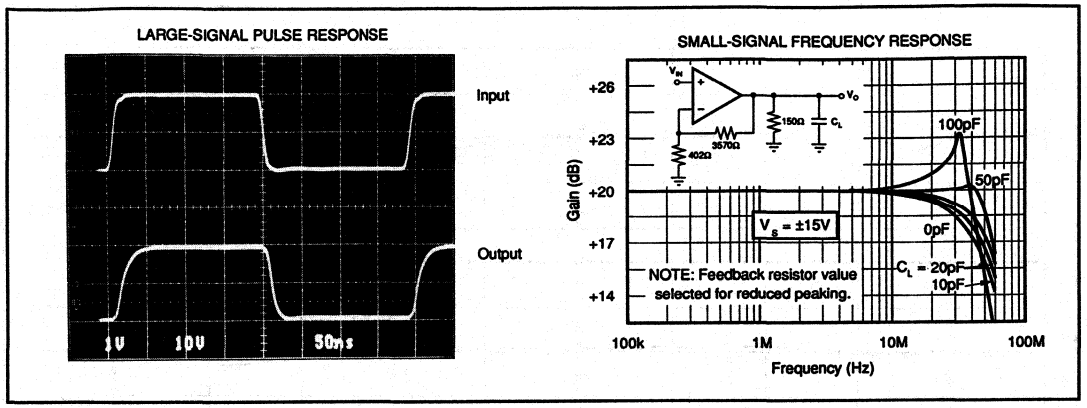


FIGURE 3. Dynamic Response, Gain = +10.

APPLICATIONS INFORMATION

For most circuit configurations, the OPA603 current-feedback op amp can be treated like a conventional op amp. As with a conventional op amp, the feedback network connected to the inverting input controls the closed-loop gain. But with a current-feedback op amp, the impedance of the feedback network also controls the open-loop gain and frequency response.

Feedback resistor values can be selected to provide a nearly constant closed-loop bandwidth over a very wide range of gain. This is in contrast to a conventional op amp where circuit bandwidth is inversely proportional to the closed-loop gain, sharply limiting bandwidth at high gain.

Figures 4a and 4b show appropriate feedback resistor values versus closed-loop gain for maximum bandwidth with minimal peaking. The dual vertical axes of these curves also show the resulting bandwidth. Note that the bandwidth remains nearly constant as gain is increased.

With control of the open-loop characteristics of the op amp, dynamic behavior can be tailored to an application's requirements. Lower feedback resistance gives wider bandwidth, more frequency-response peaking and more pulse response overshoot. The higher open-loop gain resulting from lower feedback network resistors also yields lower distortion. Higher feedback network resistance gives an over-damped response with little or no peaking and overshoot. This may be beneficial when driving capacitive loads. Feedback network impedance can also be varied to optimize dynamic performance. To achieve wider bandwidth, use a feedback resistor value somewhat lower than indicated in Figure 4.

EXTENDING BANDWIDTH

For gains less than approximately 20, bandwidth can be extended by adding a capacitor, C_F, in parallel with a lower value for R_F. The optimum gain-setting resistor value in this case is far lower than those shown in Figure 1. For ±15V operation, select R_F with the following equation:

$$R_F\ (\Omega) = 30 \cdot (30 - G) \quad \text{for } V_S = \pm 15V$$

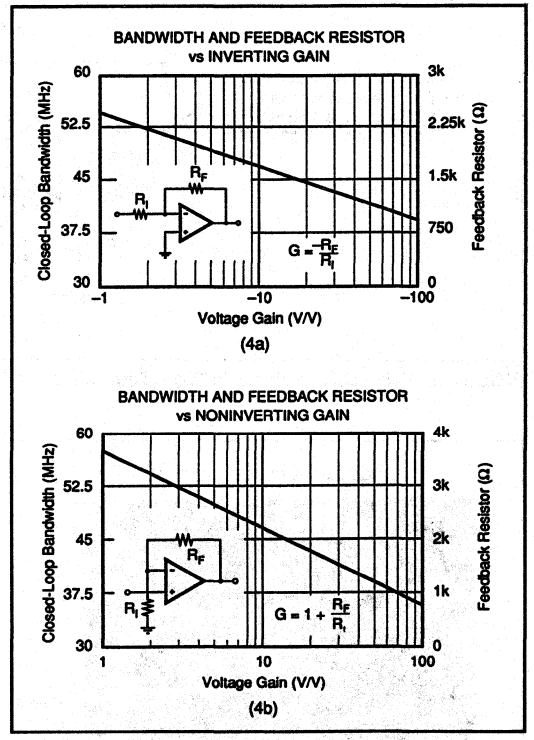


FIGURE 4. Feedback Resistor Selection Curves.

For example, for a gain of 10, use R_F = 600Ω. Optimum values differ slightly for ±5V operation:

$$R_F\ (\Omega) = 30 \cdot (23 - G) \quad \text{for } V_S = \pm 5V$$

C_F will range from 1pF to 10pF depending on the selected gain, load, and circuit layout. Adjust C_F to optimize bandwidth and minimize peaking. Figure 5 shows bandwidth which can be acheived using this technique.

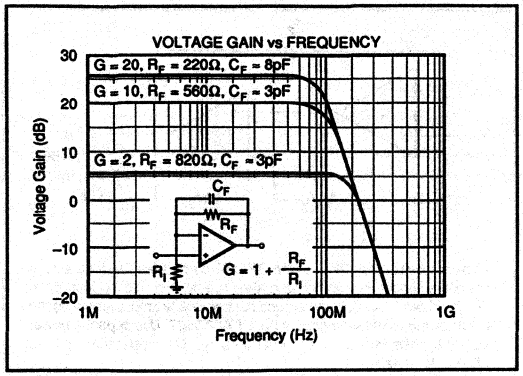


FIGURE 5. Bandwidth Results with Added Capacitor C_F.

Typical values for this capacitor range from 1pF to 10pF depending on closed-loop gain and load characteristics. Too large a value of C_F can cause instability.

UNITY-GAIN OPERATION

As Figure 4b indicates, the OPA603 can be operated in unity gain. A feedback resistor (approximately 2.8kΩ) sets the appropriate open-loop characteristics and resistor R_I is omitted. Just as with gains greater than one, the value of the feedback resistor (and capacitor if used) can be optimized for the desired dynamic response and load characteristics.

Care should be exercised not to exceed the maximum differential input voltage rating of ±6V. Large input voltage steps which exceed the device's slew rate of 1000V/µs can apply excessive differential input voltage.

CIRCUIT LAYOUT

With any high-speed, wide-bandwidth circuitry, careful circuit layout will ensure best performance. Make short, direct circuit interconnections and avoid stray wiring capacitance—especially at the inverting input pin. A component-side ground plane will help ensure low ground impedance. Do not place the ground plane under or near the inputs and feedback network.

Power supplies should be bypassed with good high-frequency capacitors positioned close to the op amp pins. In most cases, a 0.01µF ceramic capacitor in parallel with a 2.2µF solid tantalum capacitor at each power supply pin is adequate. The OPA603 can deliver high load current—up to 150mA peak. Applications with low impedance or capacitive loads demand large current transients from the power supplies. It is the power supply bypass capacitors which must supply these current transients. Larger bypass capacitors such as 10µF solid tantalum capacitors may improve performance in these applications.

POWER DISSIPATION

High output current causes increased internal power dissipation in the OPA603. Copper leadframe construction maximizes heat dissipation compared to conventional plastic packages. To achieve best heat dissipation, solder the device directly to the circuit board and use wide circuit board traces. Solder the unused pins, (1, 5 and 8) to a top-side ground plane for improved power dissipation. Limit the load and signal conditions depending on maximum ambient temperature to assure operation within the power derating curve.

The OPA603 may be operated at reduced power supply voltage to minimize power dissipation. Detailed specifications are provided for both ±15V and ±5V operation.

APPLICATIONS CIRCUITS

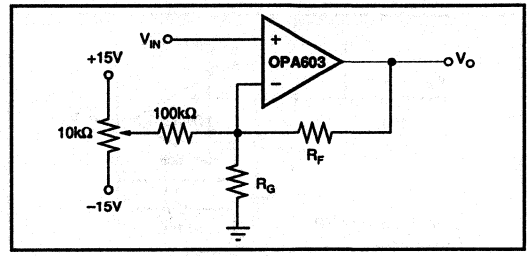


FIGURE 6. Offset Voltage Adjustment.

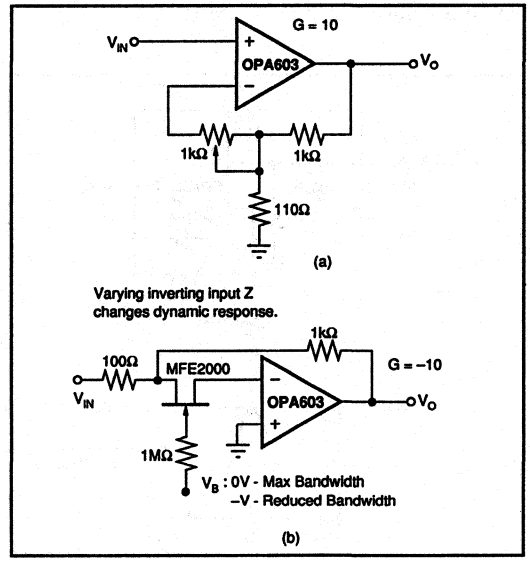


FIGURE 7. Controlling Dynamic Performance.

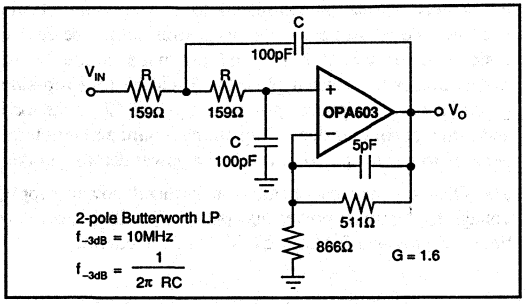


FIGURE 8. Low-Pass Filter — 10MHz.

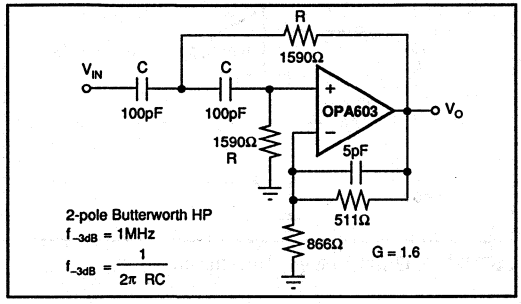


FIGURE 9. High-Pass Filter — 1MHz.

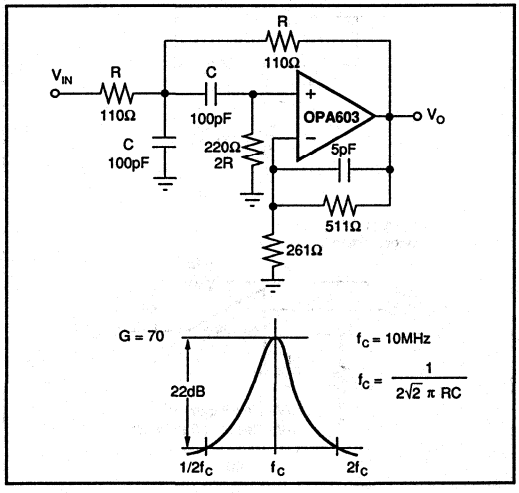
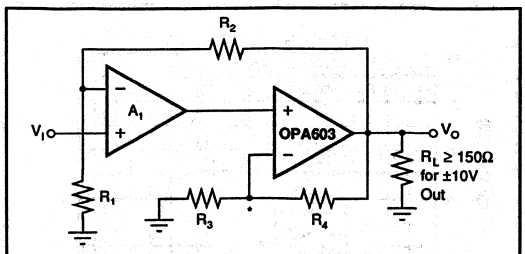


FIGURE 10. Bandpass Filter — 10MHz.



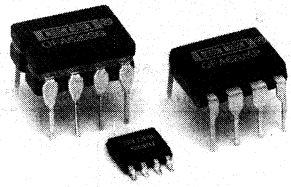
This composite amplifier uses the OPA603 current-feedback op amp to provide extended bandwidth and slew rate at high closed-loop gain. The feedback loop is closed around the composite amp, preserving the precision input characteristics of the OPA627/637. Use separate power supply bypass capacitors for each op amp. See Application Bulletin AB-007 for details.

* Minimize capacitance at this node.

GAIN (V/V)	A_1 OP AMP	R_1 (Ω)	R_2 (kΩ)	R_3 (Ω)	R_4 (kΩ)	–3dB (MHz)	SLEW RATE (V/µs)
100	OPA627	50.5(1)	4.99	20	1	15	700
1000	OPA637	49.9	4.99	12	1	11	500
NOTE: (1) Closest 1/2% value.							

FIGURE 11. Precision-Input Composite Amplifier.

BURR-BROWN®



OPA620

AVAILABLE IN DIE

Wideband Precision OPERATIONAL AMPLIFIER

FEATURES

- LOW NOISE
- 8-PIN DIP, SOIC PACKAGES AND DIE
- FAST SETTLING: 25ns (0.01%)
- GAIN-BANDWIDTH: 200MHz
- UNITY-GAIN STABLE
- LOW OFFSET VOLTAGE: ±100µV
- SLEW RATE: 250V/µs
- LOW DIFFERENTIAL GAIN/PHASE ERROR

APPLICATIONS

- LOW NOISE PREAMPLIFIER
- LOW NOISE DIFFERENTIAL AMPLIFIER
- HIGH-RESOLUTION VIDEO
- HIGH-SPEED DIGNAL PROCESSING
- ADC/DAC BUFFER
- ULTRASOUND
- PULSE/RF AMPLIFIERS
- ACTIVE FILTERS

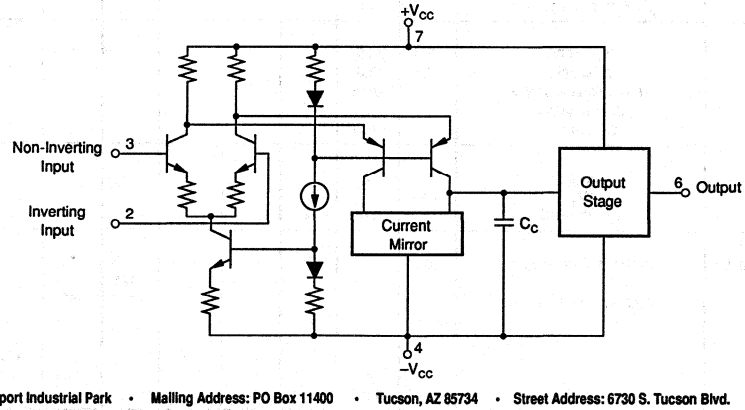
DESCRIPTION

The OPA620 is a precision wideband monolithic operational amplifier featuring very fast settling time, low differential gain and phase error, and high output current drive capability.

The OPA620 is internally compensated for unity-gain stability. This amplifier has a very low offset, fully symmetrical differential input due to its "classical" operational amplifier circuit architecture. Unlike "current-feedback" amplifier designs, the OPA620 may be used in all op amp applications requiring high speed and precision.

Low noise and distortion, wide bandwidth, and high linearity make this amplifier suitable for RF and video applications. Short-circuit protection is provided by an internal current-limiting circuit.

The OPA620 is available in plastic, ceramic, SOIC packages, and die form. Two temperature ranges are offered: 0°C to +70°C and –55°C to +125°C.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL

At V_{CC} = ±5VDC, R_L = 100Ω, and T_A = +25°C unless otherwise noted.

PARAMETER	CONDITIONS	OPA620KP/KU MIN	OPA620KP/KU TYP	OPA620KP/KU MAX	OPA620KG/SG MIN	OPA620KG/SG TYP	OPA620KG/SG MAX	OPA620LG MIN	OPA620LG TYP	OPA620LG MAX	UNITS
INPUT NOISE											
Voltage: f_O = 100Hz	R_S = 0Ω		10			*			*		nV/√Hz
f_O = 1kHz			5.5			*			*		nV/√Hz
f_O = 10kHz			3.3			*			*		nV/√Hz
f_O = 100kHz			2.5			*			*		nV/√Hz
f_O = 1MHz to 100MHz			2.3			*			*		nV/√Hz
f_B = 100Hz to 10MHz			8.0			*			*		µV, rms
Current: f_O = 10kHz to 100MHz			2.3			*			*		pA/√Hz
OFFSET VOLTAGE[1]											
Input Offset Voltage	V_{CM} = 0VDC		±200	±1mV		*	*		±100	±500	µV
Average Drift	$T_A = T_{MIN}$ to T_{MAX}		±8			*			*		µV/°C
Supply Rejection	$\pm V_{CC}$ = 4.5V to 5.5V	50	60		*	*		55	*		dB
BIAS CURRENT											
Input Bias Current	V_{CM} = 0VDC		15	30		*	*		*	25	µA
OFFSET CURRENT											
Input Offset Current	V_{CM} = 0VDC		0.2	2		*	*		*	*	µA
INPUT IMPEDANCE											
Differential	Open-Loop		15 ‖ 1			*			*		kΩ ‖ pF
Common-Mode			1 ‖ 1			*			*		MΩ ‖ pF
INPUT VOLTAGE RANGE											
Common-Mode Input Range		±3.0	±3.5		*	*		*	*		V
Common-Mode Rejection	V_{IN} = ±2.5VDC, V_O = 0VDC	65	75		*	*		70	*		dB
OPEN-LOOP GAIN, DC											
Open-Loop Voltage Gain	R_L = 100Ω	50	60		*	*		55	*		dB
	R_L = 50Ω	48	58		*	*		53	*		dB
FREQUENCY RESPONSE											
Closed-Loop Bandwidth	Gain = +1V/V		300			*			*		MHz
(–3dB)	Gain = +2V/V		100			*			*		MHz
	Gain = +5V/V		40			*			*		MHz
	Gain = +10V/V		20			*			*		MHz
Gain-Bandwidth	Gain = +10V/V		200			*			*		MHz
Differential Gain	3.58MHz, G = +1V/V		0.05			*			*		%
Differential Phase	3.58MHz, G = +1V/V		0.05			*			*		Degrees
Harmonic Distortion[2]	G = +2V/V, f = 10MHz, V_O = 2Vp-p										
	Second Harmonic		–61	–50		*	*		*	*	dBc[3]
	Third Harmonic		–65	–55		*	*		*	*	dBc
Full Power Response[2]	V_O = 5Vp-p, Gain = +1V/V	11	16		*	*		*	*		MHz
	V_O = 2Vp-p, Gain = +1V/V	27	40		*	*		*	*		MHz
Slew Rate[2]	2V Step, Gain = –1V/V	175	250		*	*		*	*		V/µs
Overshoot	2V Step, Gain = –1V/V		10			*			*		%
Settling Time: 0.1%	2V Step, Gain = –1V/V		13			*			*		ns
0.01%			25			*			*		ns
Phase Margin	Gain = +1V/V		60			*			*		Degrees
Rise Time	Gain = +1V/V, 10% to 90%								*		
	V_O = 100mVp-p; Small Signal		2			*			*		ns
	V_O = 6Vp-p; Large Signal		22			*			*		ns
RATED OUTPUT											
Voltage Output	R_L = 100Ω	±3.0	±3.5		*	*		*	*		V
	R_L = 50Ω	±2.5	±3.0		*	*		*	*		V
Output Resistance	1MHz, Gain = +1V/V		0.015			*			*		Ω
Load Capacitance Stability	Gain = +1V/V		20			*			*		pF
Short Circuit Current	Continuous		±150			*			*		mA
POWER SUPPLY											
Rated Voltage	$\pm V_{CC}$		5			*			*		VDC
Derated Performance	$\pm V_{CC}$	4.0		6.0	*		*	*		*	VDC
Current, Quiescent	I_O = 0mADC		21	23		*	*		*	*	mA
TEMPERATURE RANGE											
Specification: KP, KU, KG, LG	Ambient Temperature	0		+70	*		*	*		*	°C
SG					–55		+125				°C
Operating: KG, LG, SG	Ambient Temperature				–55		+125	–55		+125	°C
KP, KU		–25		+85							°C
θ_{JA}											
KG, LG, SG						125			125		°C/W
KP			90								°C/W
KU			100								°C/W

* Same specifications as for KP/KU.

SPECIFICATIONS (CONT)

ELECTRICAL (FULL TEMPERATURE RANGE SPECIFICATIONS)

At V_{CC} = ±5VDC, R_L = 100Ω, and T_A = T_{MIN} to T_{MAX} unless otherwise noted.

PARAMETER	CONDITIONS	OPA620AKP/KU			OPA620KG/SG			OPA620LG			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
TEMPERATURE RANGE											
Specification: KP, KU, KG, LG	Ambient Temperature	0		+70	•		•	•		•	°C
SG					–55		+125				°C
OFFSET VOLTAGE[1]											
Average Drift	T_A = T_{MIN} to T_{MAX}		±8			•			•		µV/°C
Supply Rejection	±V_{CC} = 4.5V to 5.5V	45	60		•	•		50	•		dB
BIAS CURRENT											
Input Bias Current	V_{CM} = 0VDC		15	40		•	•		•	35	µA
OFFSET CURRENT											
Input Offset Current	V_{CM} = 0VDC		0.2	5		•	•		•	•	µA
INPUT VOLTAGE RANGE											
Common-Mode Input Range		±2.5	±3.0		•	•		•	•		V
Common-Mode Rejection	V_{IN} = ±2.5VDC, V_O = 0VDC	60	75		•	•		65	•		dB
OPEN LOOP GAIN, DC											
Open-Loop Voltage Gain	R_L = 100Ω	46	60		•	•		52	•		dB
	R_L = 50Ω	44	58		•	•		50	•		dB
RATED OUTPUT											
Voltage Output	R_L = 100Ω	±3.0	±3.5		•	•		•	•		V
	R_L = 50Ω	±2.5	±3.0		•	•		•	•		V
POWER SUPPLY											
Current, Quiescent	I_O = 0mADC		21	25		•	•		•	•	mA

* Same specifications as for KP/KU.

NOTES: (1) Offset Voltage specifications are also guaranteed with units fully warmed up. (2) Parameter is sample tested. (3) dBc = dB refered to carrier-input signal.

ORDERING INFORMATION

OPA620 ( )( )

- Basic Model Number
- Performance Grade Code
  - K,L = 0°C to +70°C
  - S = –55°C to +125°C
- Package Code
  - G = 8-pin Ceramic DIP
  - P = 8-pin Plastic DIP
  - U = 8-pin Plastic SOIC

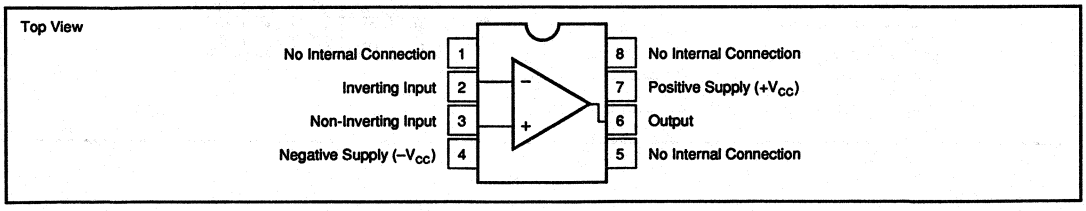
ABSOLUTE MAXIMUM RATINGS

Supply	±7VDC
Internal Power Dissipation[4]	See Applications Information
Differential Input Voltage	Total V_{CC}
Input Voltage Range	See Applications Information
Storage Temperature Range: KG, LG, SG	–65°C to +150°C
KP, KU	–40°C to +125°C
Lead Temperature (soldering, 10s)	+300°C
(soldering, SOIC 3s)	+260°C
Output Short Circuit to Ground (+25°C)	Continuous to Ground
Junction Temperature (T_J)	+175°C

NOTE: (4) Packages must be derated based on specified θ_{JA}. Maximum T_J must be observed.

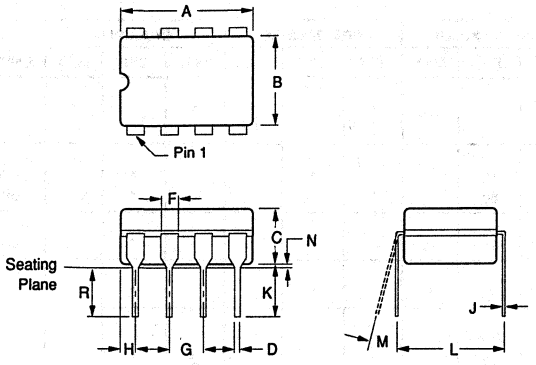
The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

PIN CONFIGURATION (8-PIN DIP)



MECHANICAL

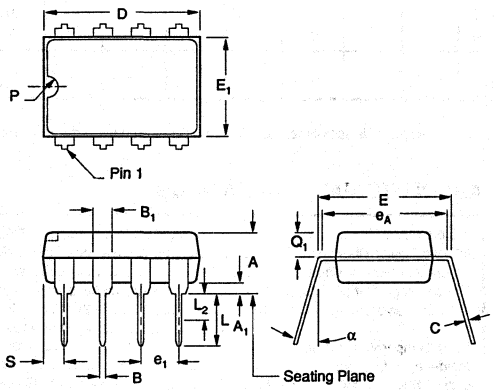
G Package — 8-Pin Ceramic



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.375	.405	9.53	10.28
B	.245	.251	6.22	6.38
C	.140	.170	3.56	4.32
D	.015	.021	0.38	0.53
F	.045	.060	1.14	1.52
G	.100 BASIC		2.54 BASIC	
H	—	.098	—	2.49
J	.008	.012	0.20	0.30
K	.150	—	3.80	—
L	.290	.320	7.37	8.13
M	0°	15°	0°	15°
N	.009	.060	0.23	1.52
R	.125	.175	3.18	4.45

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

P Package — 8-Pin Plastic DIP

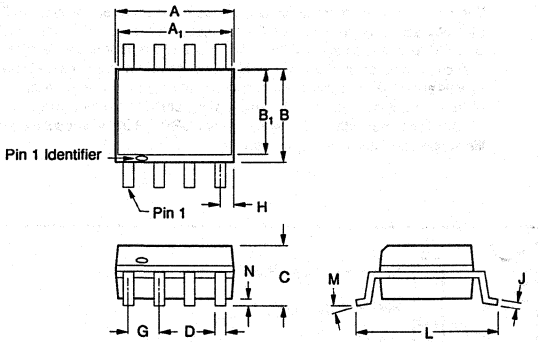


DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.155	.200	3.94	5.08
A1	.020	.050	0.51	1.27
B	.014	.020	0.36	0.51
B1	.045	.065	1.14	1.65
C	.008	.012	0.20	0.30
D (1)	.370	.400	9.40	10.16
E	.300	.325	7.62	8.26
E1	.240	.260	6.10	6.60
e1	.100 BASIC		2.54 BASIC	
eA	.300 BASIC		7.62 BASIC	
L	.125	.150	3.18	3.81

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
L2(2)	0	.030	0.00	0.76
α	0°	15°	0°	15°
P	.015	.050	0.38	1.270
Q1	.040	.075	1.02	1.91
S (1)	.015	.050	0.38	1.27

(1) Not JEDEC Std.
(2) e_1 and e_A applies in zone L_2 when unit installed.
NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

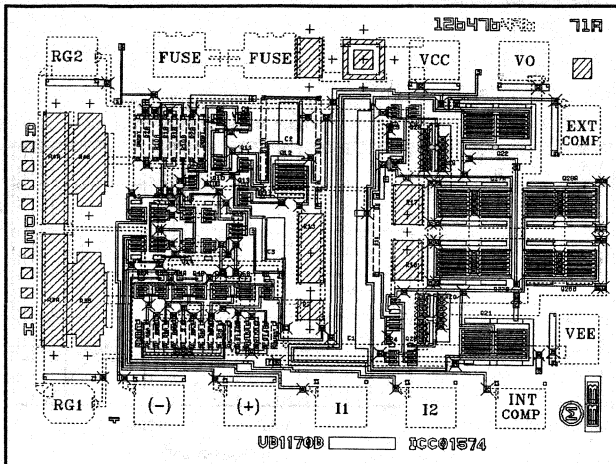
U Package — 8-Pin SOIC



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.185	.201	4.70	5.11
A1	.178	.201	4.52	5.11
B	.146	.162	3.71	4.11
B1	.130	.149	3.30	3.78
C	.054	.145	1.37	3.69
D	.015	.019	0.38	0.48
G	.050 BASIC		1.27 BASIC	
H	.018	.026	0.46	0.66
J	.008	.012	0.20	0.30
L	.220	.252	5.59	6.40
M	0°	10°	0°	10°
N	.000	.012	0.00	0.30

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

DICE INFORMATION



OPA620 DIE TOPOGRAPHY

PAD	FUNCTION	PAD	FUNCTION
1	NC	7	$-V_{CC}$
2	–Input	8	NC
3	+Input	9	V_{OUT}
4	NC	10	$+V_{CC}$
5	NC	11	NC
6	NC	12	NC
		13	NC

Substrate Bias: Negative Supply $-V_{CC}$.

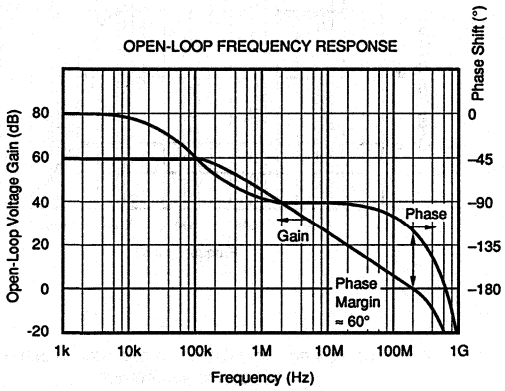
MECHANICAL INFORMATION

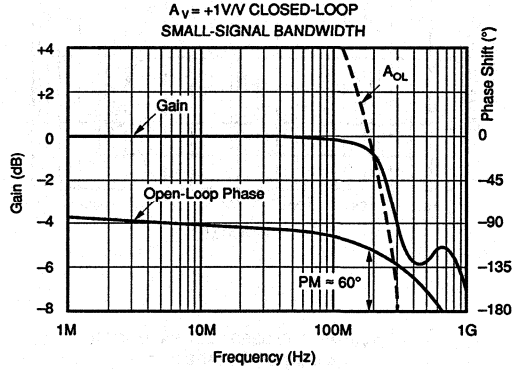
	MILS (0.001")	MILLIMETERS
Die Size	63 x 47 ±5	1.22 x 1.83 ±0.13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.10 x 0.10
Backing	Gold	
Metalization	Gold	

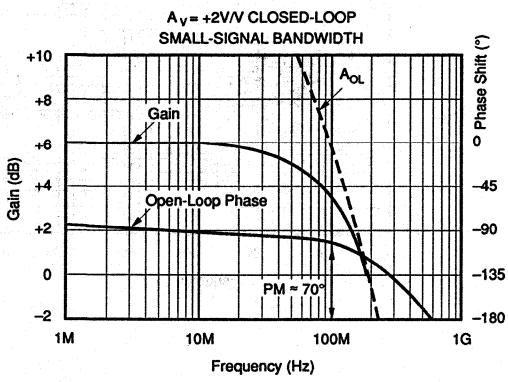
See "DICE PRODUCTS" Section 17 in Data Book Supplement Volume 33c, or contact Burr-Brown for current information.

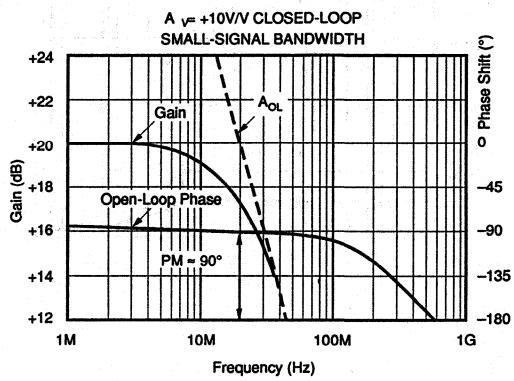
TYPICAL PERFORMANCE CURVES

At V_{CC} = ±5VDC, R_L = 100Ω, and T_A = +25°C unless otherwise noted.





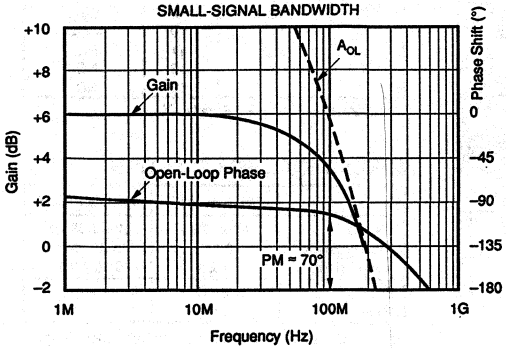




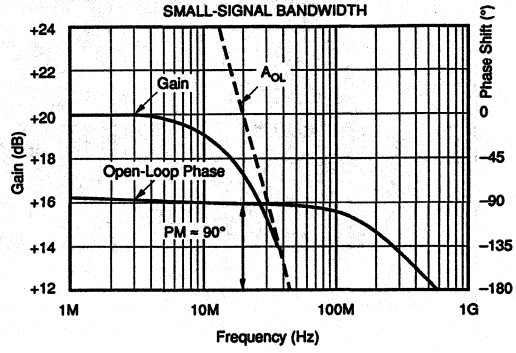
TYPICAL PERFORMANCE CURVES (CONT)

At V_{CC} = ±5VDC, R_L = 100Ω, and T_A = +25°C unless otherwise noted.

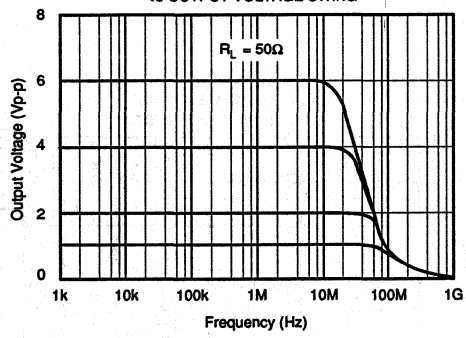
A_V = +2V/V CLOSED-LOOP
SMALL-SIGNAL BANDWIDTH



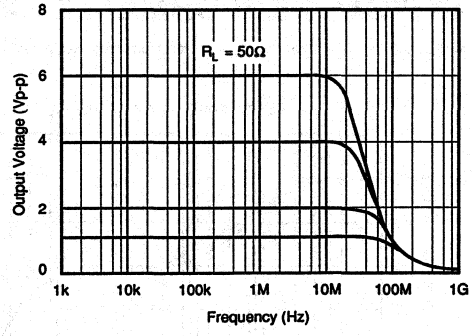
A_V = +10V/V CLOSED-LOOP
SMALL-SIGNAL BANDWIDTH



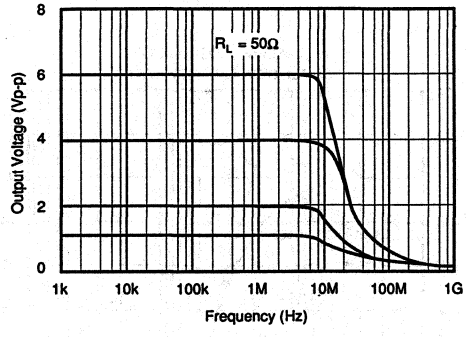
A_V = +1V/V CLOSED-LOOP BANDWIDTH
vs OUTPUT VOLTAGE SWING



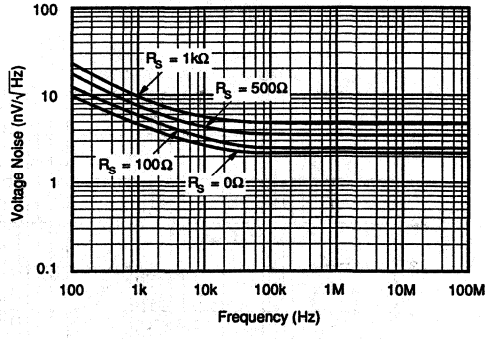
A_V = +2V/V CLOSED-LOOP BANDWIDTH
vs OUTPUT VOLTAGE SWING



A_V = +10V/V CLOSED-LOOP BANDWIDTH
vs OUTPUT VOLTAGE SWING



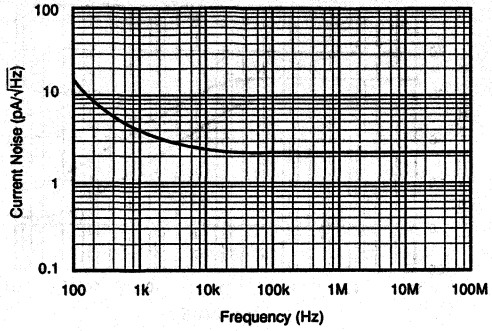
TOTAL INPUT VOLTAGE NOISE SPECTRAL DENSITY
vs SOURCE RESISTANCE



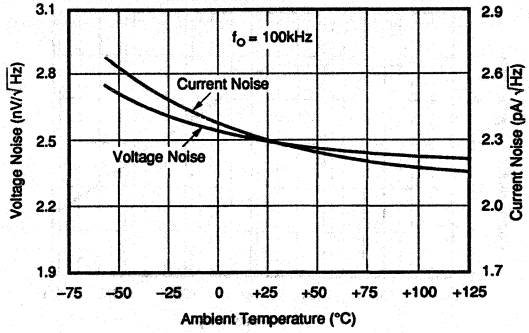
TYPICAL PERFORMANCE CURVES (CONT)

At V_{CC} = ±5VDC, R_L = 100Ω, and T_A = +25°C unless otherwise noted.

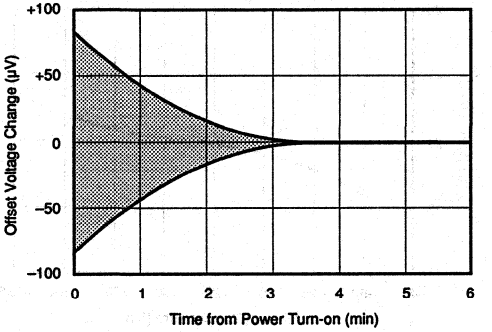
INPUT CURRENT NOISE SPECTRAL DENSITY



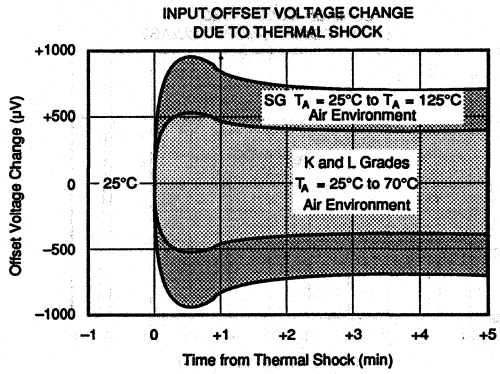
VOLTAGE AND CURRENT NOISE SPECTRAL DENSITY vs TEMPERATURE



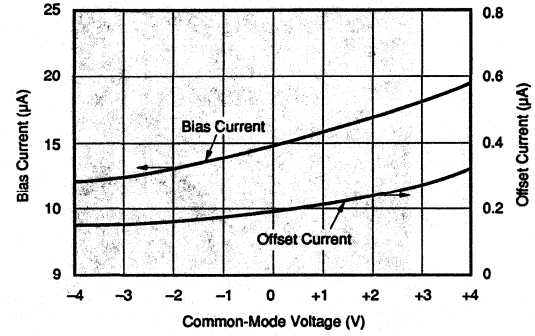
INPUT OFFSET VOLTAGE WARM-UP DRIFT



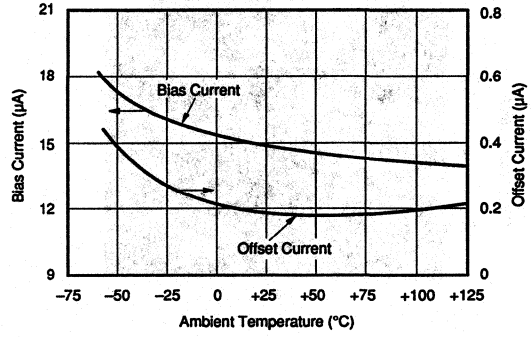
INPUT OFFSET VOLTAGE CHANGE DUE TO THERMAL SHOCK



BIAS AND OFFSET CURRENT vs INPUT COMMON-MODE VOLTAGE



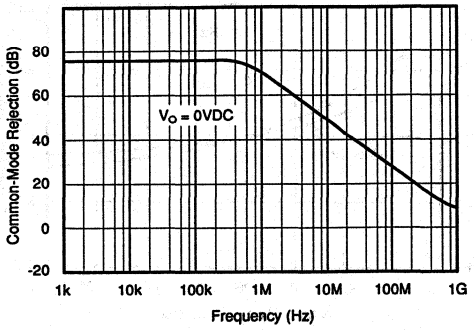
BIAS AND OFFSET CURRENT vs TEMPERATURE



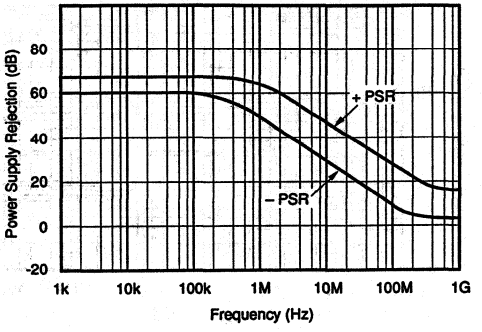
TYPICAL PERFORMANCE CURVES (CONT)

At V_{CC} = ±5VDC, R_L = 100Ω, and T_A = +25°C unless otherwise noted.

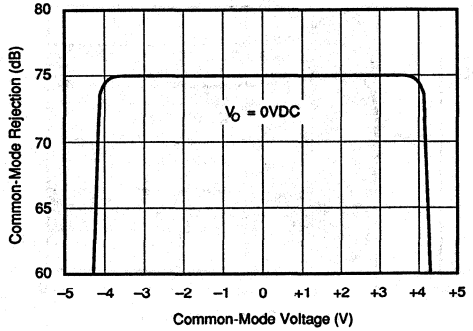
COMMON-MODE REJECTION vs FREQUENCY



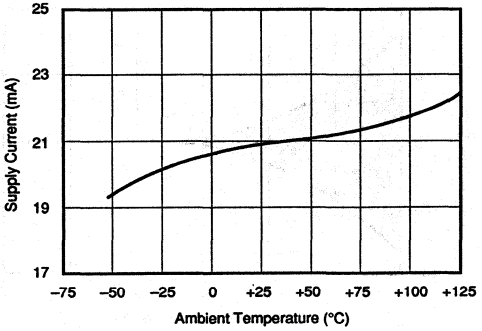
POWER SUPPLY REJECTION vs FREQUENCY



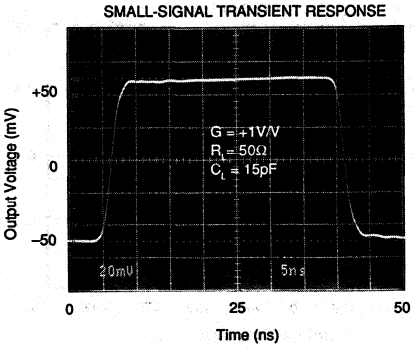
COMMON-MODE REJECTION vs INPUT COMMON-MODE VOLTAGE



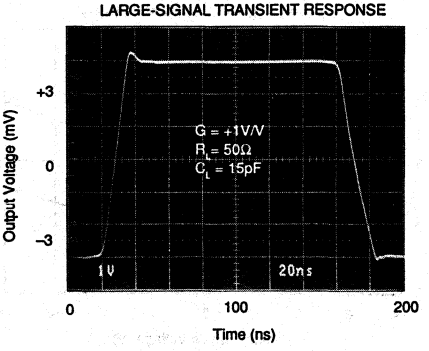
SUPPLY CURRENT vs TEMPERATURE



SMALL-SIGNAL TRANSIENT RESPONSE



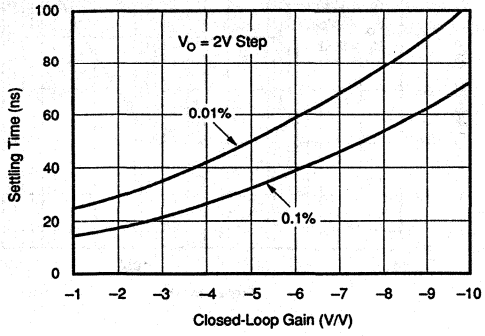
LARGE-SIGNAL TRANSIENT RESPONSE



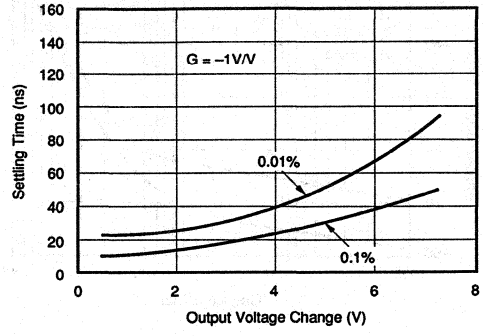
TYPICAL PERFORMANCE CURVES (CONT)

At V_{CC} = ±5VDC, R_L = 100Ω, and T_A = +25°C unless otherwise noted.

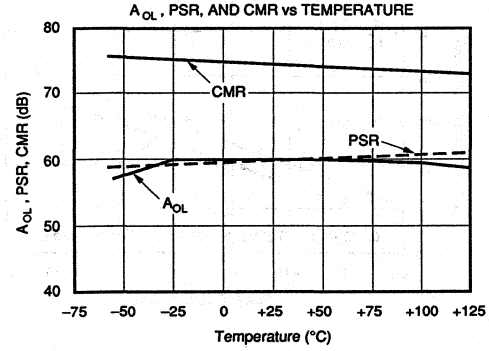
SETTLING TIME vs CLOSED-LOOP GAIN



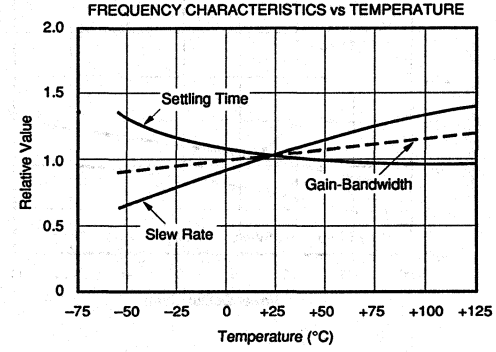
SETTLING TIME vs OUTPUT VOLTAGE CHANGE



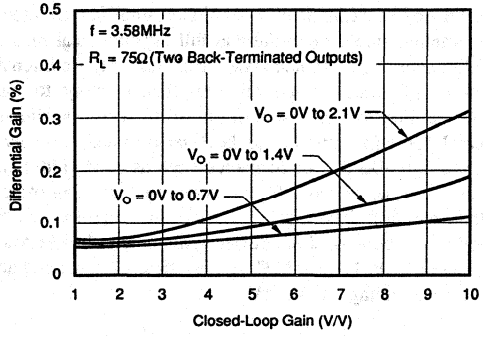
A_{OL}, PSR, AND CMR vs TEMPERATURE



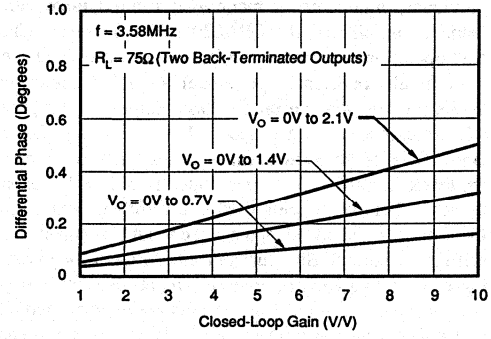
FREQUENCY CHARACTERISTICS vs TEMPERATURE



NTSC DIFFERENTIAL GAIN vs CLOSED-LOOP GAIN



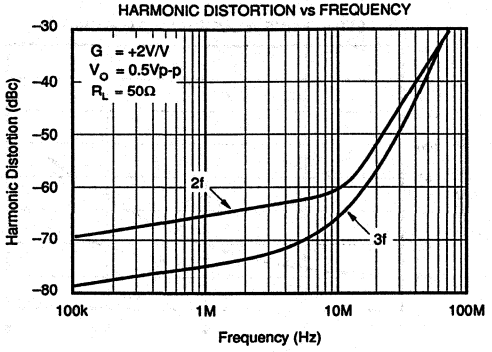
NTSC DIFFERENTIAL PHASE vs CLOSED-LOOP GAIN



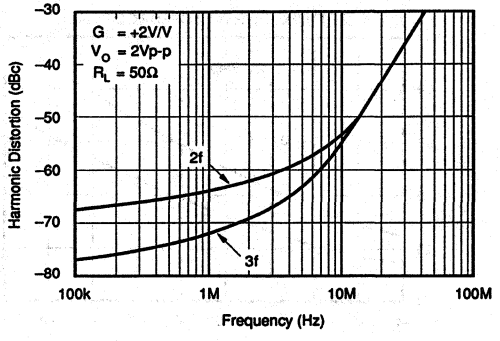
TYPICAL PERFORMANCE CURVES (CONT)

At V_{CC} = ±5VDC, R_L = 100Ω, and T_A = +25°C unless otherwise noted.

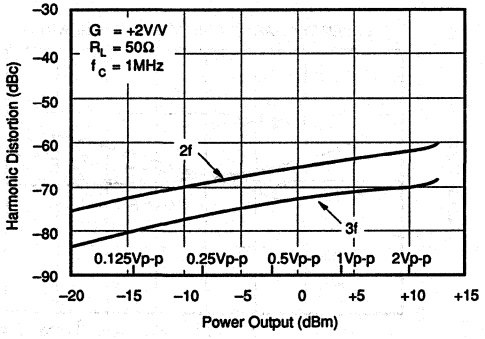
SMALL-SIGNAL
HARMONIC DISTORTION vs FREQUENCY



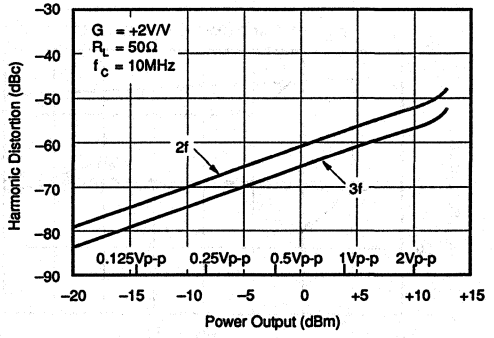
LARGE-SIGNAL
HARMONIC DISTORTION vs FREQUENCY



1MHz HARMONIC DISTORTION
vs POWER OUTPUT



10MHz HARMONIC DISTORTION
vs POWER OUTPUT



APPLICATIONS INFORMATION

DISCUSSION OF PERFORMANCE

The OPA620 provides a level of speed and precision not previously attainable in monolithic form. Unlike current feedback amplifiers, the OPA620's design uses a "Classical" operational amplifier architecture and can therefore be used in all traditional operational amplifier applications. While it is true that current feedback amplifiers can provide wider bandwidth at higher gains, they offer many disadvantages. The asymmetrical input characteristics of current feedback amplifiers (i.e. one input is a low impedance) prevents them from being used in a variety of applications. In addition, unbalanced inputs make input bias current errors difficult to correct. Bias current cancellation through matching of inverting and non-inverting input resistors is impossible because the input bias currents are uncorrelated. Current noise is also asymmetrical and is usually significantly higher on the inverting input. Perhaps most important, settling time to 0.01% is often extremely poor due to internal design tradeoffs. Many current feedback designs exhibit settling times to 0.01% in excess of 10 *microseconds* even though 0.1% settling times are reasonable. Such amplifiers are completely inadequate for fast settling 12-bit applications.

The OPA620's "Classical" operational amplifier architecture employs true differential and fully symmetrical inputs to eliminate these troublesome problems. All traditional circuit configurations and op amp theory apply to the OPA620. The use of low-drift thin-film resistors allows internal operating currents to be laser-trimmed at wafer-level to optimize AC performance such as bandwidth and settling time, as well as DC parameters such as input offset voltage and drift. The result is a wideband, high-frequency monolithic operational amplifier with a gain-bandwidth product of 200MHz, a 0.01% settling time of 25ns, and an input offset voltage of 100µV.

WIRING PRECAUTIONS

Maximizing the OPA620's capability requires some wiring precautions and high-frequency layout techniques. Oscilla-

tion, ringing, poor bandwidth and settling, gain peaking, and instability are typical problems plaguing all high-speed amplifiers when they are improperly used. In general, all printed circuit board conductors should be wide to provide low resistance, low impedance signal paths. They should also be as short as possible. The entire physical circuit should be as small as practical. Stray capacitances should be minimized, especially at high impedance nodes, such as the amplifier's input terminals. Stray signal coupling from the output or power supplies to the inputs should be minimized. All circuit element leads should be no longer than 1/4 inch (6mm) to minimize lead inductance, and low values of resistance should be used. This will minimize time constants formed with the circuit capacitances and will eliminate stray, parasitic circuits.

Grounding is the most important application consideration for the OPA620, as it is with all high-frequency circuits. Oscillations at frequencies of 200MHz and above can easily occur if good grounding techniques are not used. A heavy ground plane (2oz copper recommended) should connect all unused areas on the component side. Good ground planes can reduce stray signal pickup, provide a low resistance, low inductance common return path for signal and power, and can conduct heat from active circuit package pins into ambient air by convection.

Supply bypassing is extremely critical and must *always* be used, especially when driving high current loads. Both power supply leads should be bypassed to ground as close as possible to the amplifier pins. Tantalum capacitors (1µF to 10µF) with very short leads are recommended. Although not required, a parallel 0.01µF ceramic may be added if desired. Surface mount bypass capacitors will produce excellent results due to their low lead inductance. Additionally, suppression filters can be used to isolate noisy supply lines. Properly bypassed and modulation-free power supply lines allow full amplifier output and optimum settling time performance.

Points to Remember

1) Don't use point-to-point wiring as the increase in wiring inductance will be detrimental to AC performance. However, if it must be used, very short, direct signal paths are required. The input signal ground return, the load ground return, and the power supply common should all be connected to the same physical point to eliminate ground loops, which can cause unwanted feedback.

2) Good component selection is essential. Capacitors used in critical locations should be a low inductance type with a high quality dielectric material. Likewise, diodes used in critical locations should be Schottky barrier types, such as HP5082-2835 for fast recovery and minimum charge storage. Ordinary diodes will not be suitable in RF circuits.

3) Whenever possible, solder the OPA620 directly into the PC board without using a socket. Sockets add parasitic capacitance and inductance, which can seriously degrade AC performance or produce oscillations. If sockets must be used, consider using zero-profile solderless sockets such as Augat part number 8134-HC-5P2. Alternately, Teflon® standoffs located close to the amplifier's pins can be used to mount feedback components.

4) Resistors used in feedback networks should have values of a few hundred ohms for best performance. Shunt capacitance problems limit the acceptable resistance range to about 1kΩ on the high end and to a value that is within the amplifier's output drive limits on the low end. Metal film and carbon resistors will be satisfactory, but wirewound resistors (even "non-inductive" types) are absolutely *unacceptable* in high-frequency circuits.

5) Surface mount components (chip resistors, capacitors, etc) have low lead inductance and are therefore strongly recommended. Circuits using all surface mount components with the OPA620KU (SOIC package) will offer the best AC performance. The parasitic package inductance and capacitance for the SOIC is lower than the both the Cerdip and 8-lead Plastic DIP.

6) Avoid overloading the output. Remember that output current must be provided by the amplifier to drive its own feedback network as well as to drive its load. Lowest distortion is achieved with high impedance loads.

7) Don't forget that these amplifiers use ±5V supplies. Although they will operate perfectly well with +5V and –5.2V, use of ±15V supplies will destroy the part.

8) Standard commercial test equipment has not been designed to test devices in the OPA620's speed range. Benchtop op amp testers and ATE systems will require a special test head to successfully test these amplifiers.

9) Terminate transmission line loads. Unterminated lines, such as coaxial cable, can appear to the amplifier to be a capacitive or inductive load. By terminating a transmission line with its characteristic impedance, the amplifier's load then appears purely resistive.

10) Plug-in prototype boards and wire-wrap boards will not be satisfactory. A clean layout using RF techniques is essential; there are no shortcuts.

OFFSET VOLTAGE ADJUSTMENT

The OPA620's input offset voltage is laser-trimmed and will require no further adjustment for most applications. However, if additional adjustment is needed, the circuit in Figure 1 can be used without degrading offset drift with temperature. Avoid external adjustment whenever possible since extraneous noise, such as power supply noise, can be inadvertently coupled into the amplifier's inverting input terminal. Remember that additional offset errors can be created by the amplifier's input bias currents. Whenever possible, match the impedance seen by both inputs as is shown with R_3. This will reduce input bias current errors to the amplifier's offset current, which is typically only 0.2µA.

INPUT PROTECTION

Static damage has been well recognized for MOSFET devices, but any semiconductor device deserves protection from this potentially damaging source. The OPA620 incorporates on-chip ESD protection diodes as shown in Figure 2.

Teflon® E. I. Du Pont de Nemours & Co.

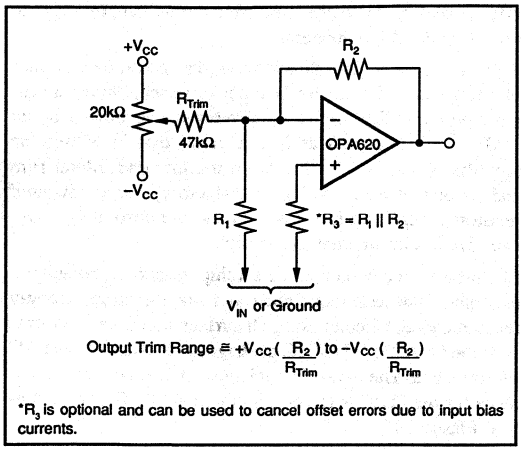


FIGURE 1. Offset Voltage Trim.

This eliminates the need for the user to add external protection diodes, which can add capacitance and degrade AC performance.

All pins on the OPA620 are internally protected from ESD by means of a pair of back-to-back reverse-biased diodes to either power supply as shown. These diodes will begin to conduct when the input voltage exceeds either power supply by about 0.7V. This situation can occur with loss of the amplifier's power supplies while a signal source is still present. The diodes can typically withstand a continuous current of 30mA without destruction. To insure long term reliability, however, diode current should be externally limited to 10mA or so whenever possible.

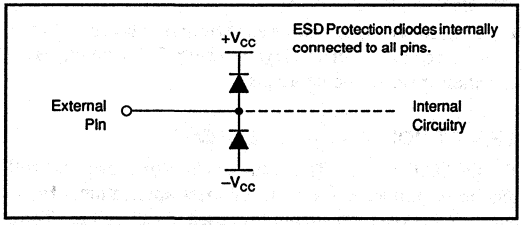


FIGURE 2. Internal ESD Protection.

The internal protection diodes are designed to withstand 2.5kV (using Human Body Model) and will provide adequate ESD protection for most normal handling procedures. However, static damage can cause subtle changes in amplifier input characteristics without necessarily destroying the device. In precision operational amplifiers, this may cause a noticeable degradation of offset voltage and drift. Therefore, static protection is strongly recommended when handling the OPA620.

OUTPUT DRIVE CAPABILITY

The OPA620's design uses large output devices and has been optimized to drive 50Ω and 75Ω resistive loads. The device can easily drive 6Vp-p into a 50Ω load. This high-output drive capability makes the OPA620 an ideal choice for a wide range of RF, IF, and video applications. In many cases, additional buffer amplifiers are unneeded.

Internal current-limiting circuitry limits output current to about 150mA at 25°C. This prevents destruction from accidental shorts to common and eliminates the need for external current-limiting circuitry. Although the device can withstand momentary shorts to either power supply, it is not recommended.

Many demanding high-speed applications such as ADC/DAC buffers require op amps with low wideband output impedance. For example, low output impedance is essential when driving the signal-dependent capacitances at the inputs of flash A/D converters. As shown in Figure 3, the OPA620 maintains very low closed-loop output impedance over frequency. Closed-loop output impedance increases with frequency since loop gain is decreasing with frequency.

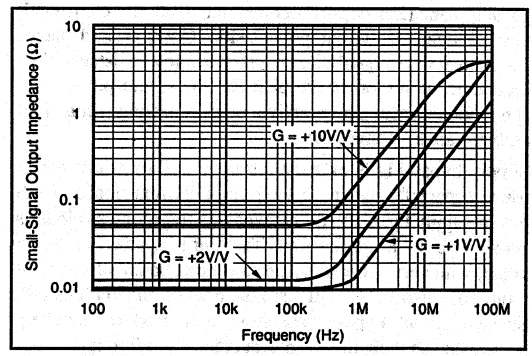


FIGURE 3. Small-Signal Output Impedance vs Frequency.

THERMAL CONSIDERATIONS

The OPA620 does not require a heat sink for operation in most environments. The use of a heat sink, however, will reduce the internal thermal rise and will result in cooler, more relaible operation. At extreme temperatures and under full load conditions a heat sink is necessary. See "Maximum Power Dissipation" curve, Figure 4.

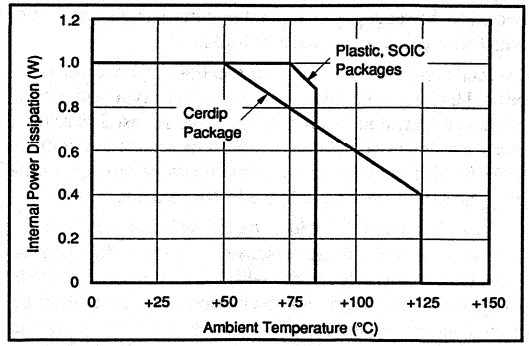


FIGURE 4. Maximum Power Dissipation.

The internal power dissipation is given by the equation $P_D = P_{DQ} + P_{DL}$, where P_{DQ} is the quiescent power dissipation and P_{DL} is the power dissipation in the output stage due to the load. (For $\pm V_{CC} = \pm 5V$, $P_{DQ} = 10V \times 23mA = 230mW$, max). For the case where the amplifier is driving a grounded load (R_L) with a DC voltage ($\pm V_{OUT}$) the maximum value of P_{DL} occurs at $\pm V_{OUT} = \pm V_{CC}/2$, and is equal to P_{DL}, max $= (\pm V_{CC})^2/4R_L$. Note that it is the voltage across the output transistor, and not the load, that determines the power dissipated in the output stage.

When the output is shorted to common $P_{DL} = 5V \times 150mA = 750mW$. Thus, $P_D = 230mW + 750mW \approx 1W$. Note that the short-circuit condition represents the maximum amount of internal power dissipation that can be generated. Thus, the "Maximum Power Dissipation" curve starts at 1W and is derated based on a 175°C maximum junction temperature and the junction-to-ambient thermal resistance, θ_{JA}, of each package. The variation of short-circuit current with temperature is shown in Figure 5.

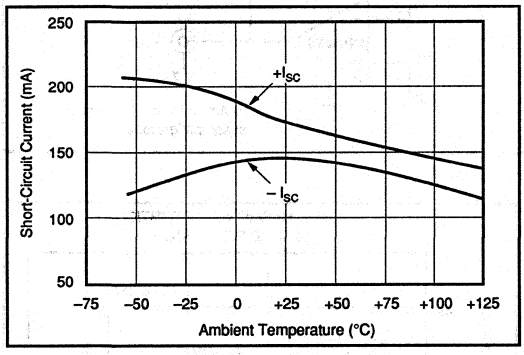


FIGURE 5. Short-Circuit Current vs Temperature.

CAPACITIVE LOADS

The OPA620's output stage has been optimized to drive resistive loads as low as 50Ω. Capacitive loads, however, will decrease the amplifier's phase margin which may cause high frequency peaking or oscillations. Capacitive loads greater than 20pF should be buffered by connecting a small resistance, usually 5Ω to 25Ω, in series with the output as shown in Figure 6. This is particularly important when driving high capacitance loads such as flash A/D converters.

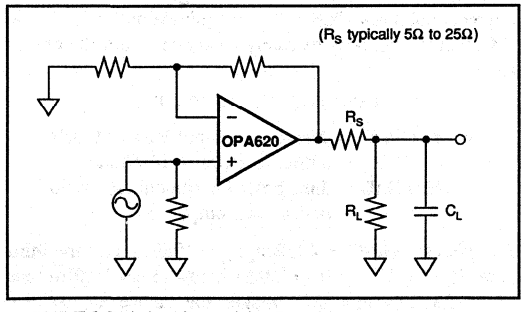


FIGURE6.DrivingCapacitiveLoads.

In general, capacitive loads should be minimized for optimum high frequency performance. Coax lines can be driven if the cable is properly terminated. The capacitance of coax cable (29pF/foot for RG-58) will not load the amplifier when the coaxial cable or transmission line is terminated in its characteristic impedance.

COMPENSATION

The OPA620 is internally compensated and is stable in unity gain with a phase margin of approximately 60°. However, the unity gain buffer is the most demanding circuit configuration for loop stability and oscillations are most likely to occur in this gain. If possible, use the device in a noise gain of two or greater to improve phase margin and reduce the susceptibility to oscillation. (Note that, from a stability standpoint, an inverting gain of –1V/V is equivalent to a noise gain of 2.) Gain and phase response for other gains are shown in the Typical Performance Curves.

The high-frequency response of the OPA620 in a good layout is very flat with frequency. However, some circuit configurations such as those where large feedback resistances are used, can produce high-frequency gain peaking. This peaking can be minimized by connecting a small capacitor in parallel with the feedback resistor. This capacitor compensates for the closed-loop, high frequency, transfer function zero that results from the time constant formed by the input capacitance of the amplifier (typically 2pF after PC board mounting), and the input and feedback resistors. The selected compensation capacitor may be a trimmer, a fixed capacitor, or a planned PC board capacitance. The capacitance value is strongly dependent on circuit layout and closed-loop gain. Using small resistor values will preserve the phase margin and avoid peaking by keeping the break frequency of this zero sufficiently high. When high closed-loop gains are required, a three-resistor attenuator (tee network) is recommended to avoid using large value resistors with large time constants.

SETTLING TIME

Settling time is defined as the total time required, from the input signal step, for the output to settle to within the specified error band around the final value. This error band is expressed as a percentage of the value of the output transition, a 2V step. Thus, settling time to 0.01% requires an error band of ±200µV centered around the final value of 2V.

Settling time, specified in an inverting gain of one, occurs in only 25ns to 0.01% for a 2V step, making the OPA620 one of the fastest settling monolithic amplifiers commercially available. Settling time increases with closed-loop gain and output voltage change as described in the Typical Performance Curves. Preserving settling time requires critical attention to the details as mentioned under "Wiring Precautions." The amplifier also recovers quickly from input overloads. Overload recovery time to linear operation from a 50% overload is typically only 30ns.

In practice, settling time measurements on the OPA620 prove to be very difficult to perform. Accurate measurement is next to impossible in all but the very best equipped labs. Among other things, a fast flat-top generator and high speed oscilloscope are needed. Unfortunately, fast flat-top generators, which settle to 0.01% in sufficient time, are scarce and expensive. Fast oscilloscopes, however, are more commonly available. For best results a sampling oscilloscope is recommended. Sampling scopes typically have bandwidths that are greater than 1GHz and very low capacitance inputs. They also exhibit faster settling times in response to signals that would tend to overload a real-time oscilloscope.

Figure 7 shows the test circuit used to measure settling time for the OPA620. This approach uses a 16-bit sampling oscilloscope to monitor the input and output pulses. These waveforms are captured by the sampling scope, averaged, and then subtracted from each other in software to produce the error signal. This technique eliminates the need for the traditional "false-summing junction," which adds extra parasitic capacitance. Note that instead of an additional flat-top generator, this technique uses the scope's built-in calibration source as the input signal.

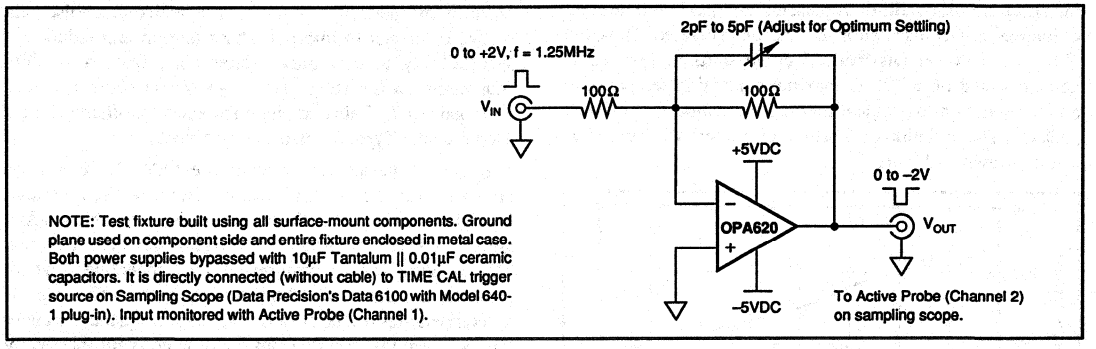


FIGURE 7. Settling Time Test Circuit.

DIFFERENTIAL GAIN AND PHASE

Differential Gain (DG) and Differential Phase (DP) are among the more important specifications for video applications. DG is defined as the percent change in closed-loop gain over a specified change in output voltage level. DP is defined as the change in degrees of the closed-loop phase over the same output voltage change. Both DG and DP are specified at the NTSC sub-carrier frequency of 3.58MHz. DG and DP increase with closed-loop gain and output voltage transition as shown in the Typical Performance Curves. All measurements were performed using a Tektronix model VM700 Video Measurement Set.

DISTORTION

The OPA620's Harmonic Distortion characteristics into a 50Ω load are shown vs frequency and power output in the Typical Performance Curves. Distortion can be further improved by increasing the load resistance as illustrated in Figure 8. Remember to include the contribution of the feedback resistance when calculating the effective load resistance seen by the amplifier.

Two-tone, third-order intermodulation distortion (IM) is an important parameter for many RF amplifier applications. Figure 9 shows the OPA620's two-tone, third-order IM intercept vs frequency. For these measurements, tones were spaced 1MHz apart. This curve is particularly useful for determining the magnitude of the third-order IM products as a function of frequency, load resistance, and gain. For example, assume that the application requires the OPA620 to operate in a gain of +2V/V and drive 2Vp-p into 50Ω at

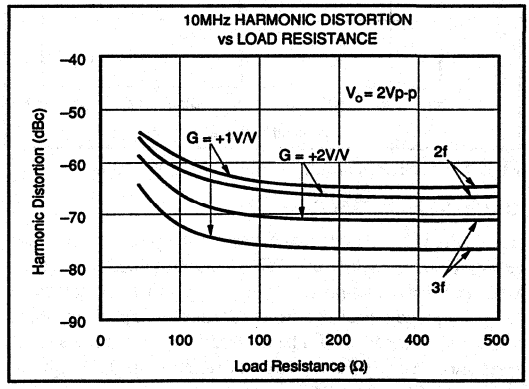


FIGURE 8. 10MHz Harmonic Distortion vs Load Resistance.

a frequency of 10MHz. Referring to Figure 9 we find that the intercept point is +40dBm. The magnitude of the third-order IM products can now be easily calculated from the expression:

$$\text{Third IMD} = 2(OPI^3P - P_O)$$

where OPI^3P = third-order output intercept, dBm
P_O = output level/tone, dBm/tone
Third IMD = third-order intermodulation ratio below each output tone, dB

For this case OPI^3P = 40dBm, P_O = 10dBm, and the third-order IMD = 2(40 – 10) = 60dB below either 10dBm tone. The OPA620's low IMD makes the device an excellent choice for a variety of RF signal processing applications.

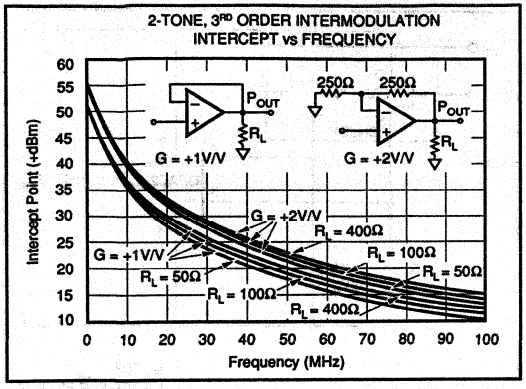


FIGURE 9. 2-Tone, 3rd Order Intermodulation Intercept vs Frequency.

NOISE FIGURE

The OPA620's voltage and current noise spectral densities are specified in the Typical Performance Curves. For RF applications, however, Noise Figure (NF) is often the preferred noise specification since it allows system noise performance to be more easily calculated. The OPA620's Noise Figure vs Source Resistance is shown in Figure 10.

SPICE MODELS

Computer simulation using SPICE is often useful when analyzing the performance of analog circuits and systems. This is particularly true for Video and RF amplifier circuits where parasitic capacitance and inductance can have a major effect on circuit performance. SPICE models using MicroSim Corporation's PSpice are available for the OPA620. Request Burr-Brown Application Note AN-167.

RELIABILITY DATA

Extensive reliability testing has been performed on the OPA620. Accelerated life testing (2000 hours) at maximum operating temperature was used to calculate MTTF at an ambient temperature of 25°C. These test results yield MTTF of: Cerdip package = 1.31E+9 Hours, Plastic DIP = 5.02E+7 Hours, and SOIC = 2.94E+7 Hours. Additional tests such as PCT have also been performed. Reliability reports are available upon request for each of the package options offered.

DEMONSTRATION BOARDS

Demonstration boards to speed prototyping are available. Request DEM1135 for 8-Pin DIP, and DEM1136 for SOIC package.

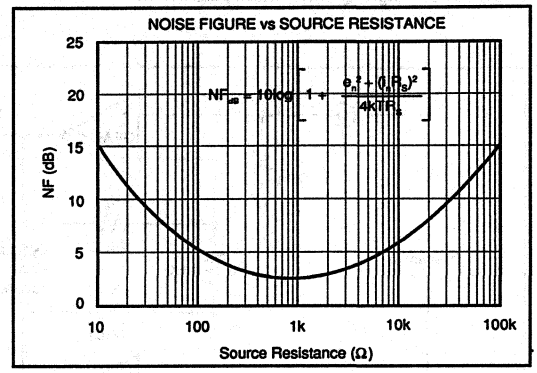


FIGURE 10. Noise Figure vs Source Resistance.

APPLICATIONS

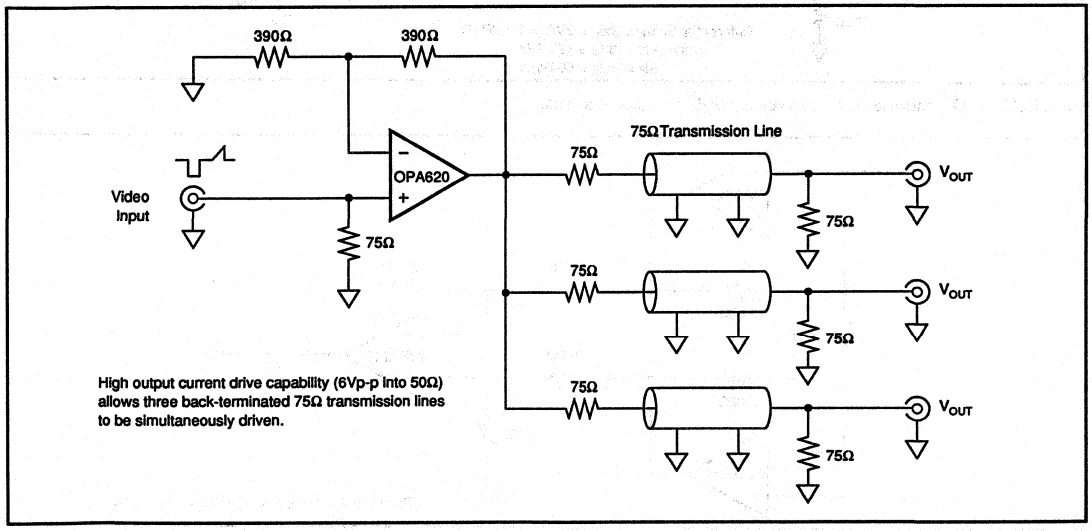


FIGURE 11. Video Distribution Amplifier.

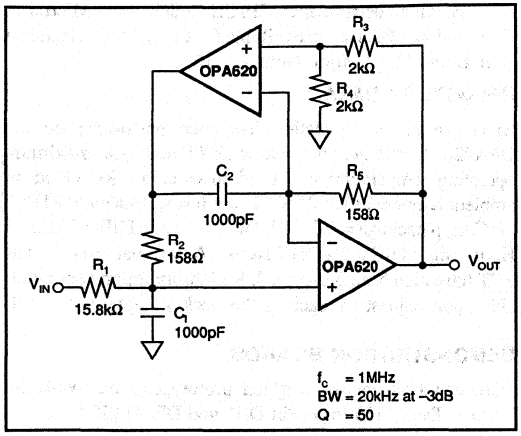


FIGURE 12. High-Q 1MHz Bandpass Filter.

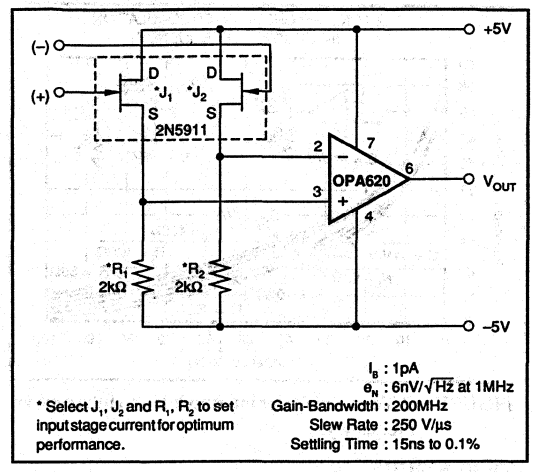


FIGURE 13. Low Noise, Wideband FET Input Op Amp.

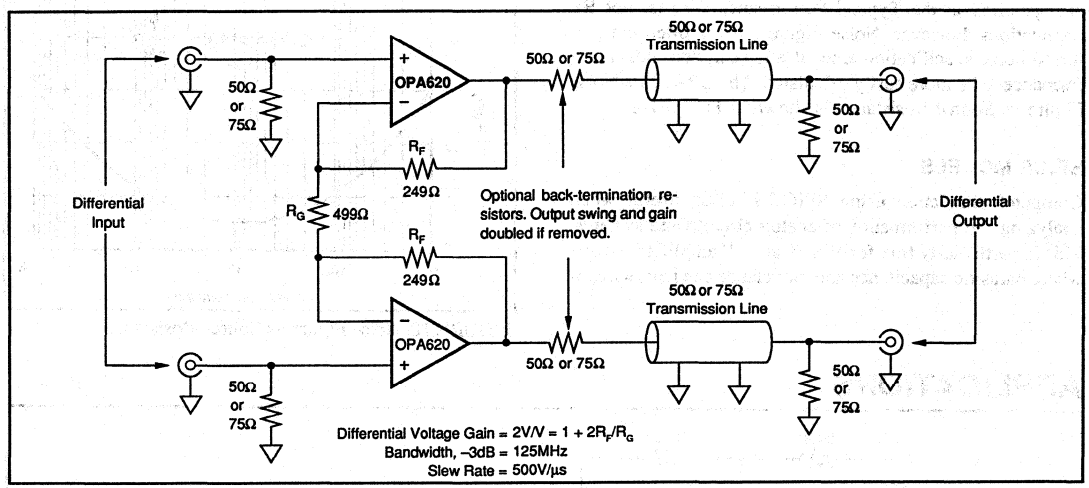


FIGURE 14. Differential Line Driver for 50Ω or 75Ω Systems.

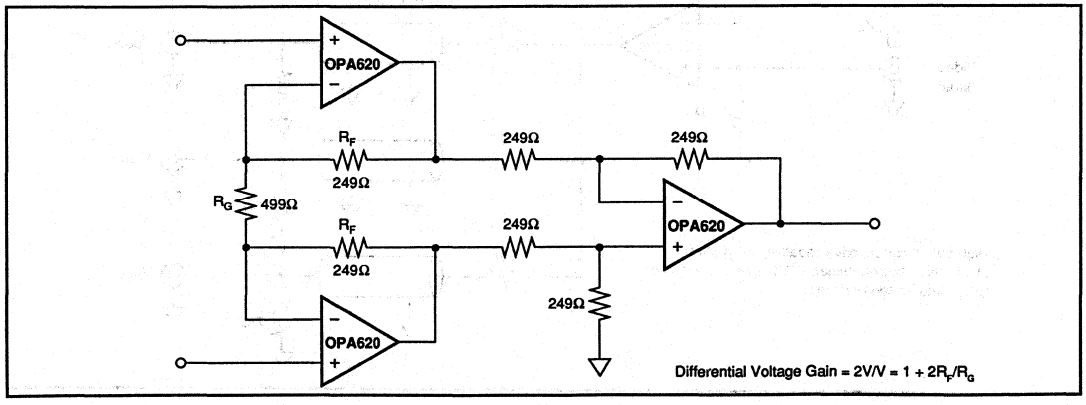


FIGURE 15. Wideband, Fast-Settling Instrumentation Amplifier.

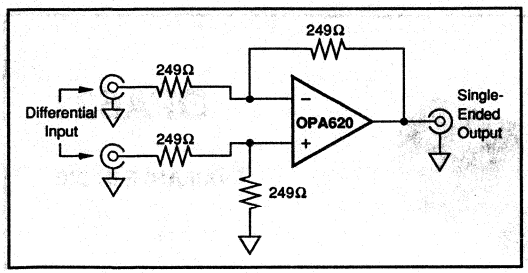


FIGURE 16. Unity Gain Difference Amplifier.

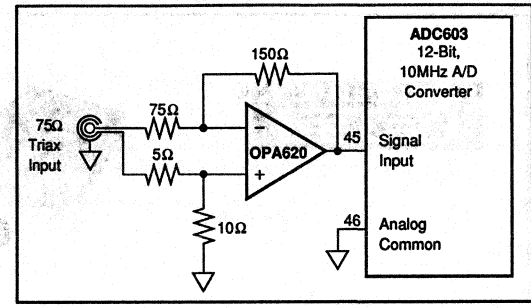


FIGURE 17. Differential Input Buffer Amplifier (G=–2V/V).

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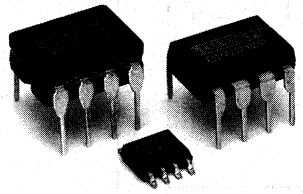


OPA621

AVAILABLE IN DIE

Wideband Precision OPERATIONAL AMPLIFIER

FEATURES

- LOW NOISE
- LOW DIFFERENTIAL GAIN/PHASE ERROR
- VERY LOW DISTORTION
- FAST SETTLING: 25ns (0.01%)
- GAIN-BANDWIDTH: 500MHz
- STABLE IN GAINS: ≥ ±2V/V
- LOW OFFSET VOLTAGE: ±100µV
- SLEW RATE: 500V/µs
- 8-PIN DIP, SOIC PACKAGES AND DIE

APPLICATIONS

- LOW NOISE PREAMPLIFIER
- LOW NOISE DIFFERENTIAL AMPLIFIER
- HIGH-RESOLUTION VIDEO
- HIGH-SPEED SIGNAL PROCESSING
- ADC/DAC BUFFER
- ULTRASOUND
- PULSE/RF AMPLIFIERS
- ACTIVE FILTERS

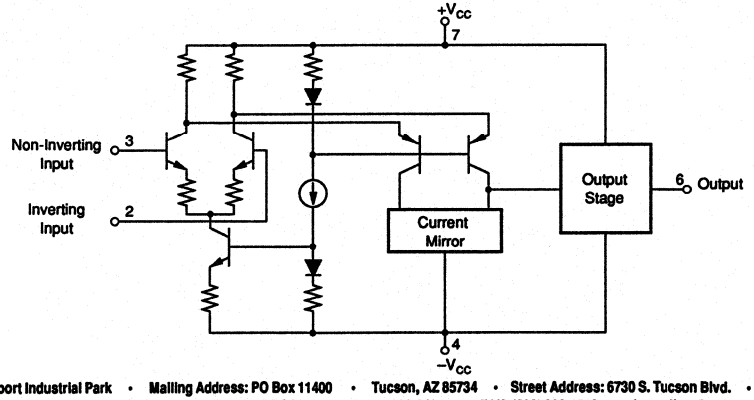
DESCRIPTION

The OPA621 is a precision wideband monolithic operational amplifier featuring very fast settling time, low differential gain and phase error, and high output current drive capability.

The OPA621 is stable in gains of ±2V/V or higher. This amplifier has a very low offset, fully symmetrical differential input due to its "classical" operational amplifier circuit architecture. Unlike "current-feedback" amplifier designs, the OPA621 may be used in all op amp applications requiring high speed and precision.

Low noise and distortion, wide bandwidth, and high linearity make this amplifier suitable for RF and video applications. Short circuit protection is provided by an internal current-limiting circuit.

The OPA621 is available in plastic, ceramic, SOIC packages, and die form. Two temperature ranges are offered: 0°C to 70°C and –55°C to +125°C.



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Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

PDS-939D

SPECIFICATIONS

ELECTRICAL

At V_{CC} = ±5VDC, R_L = 100Ω, and T_A = +25°C unless otherwise noted.

PARAMETER	CONDITIONS	OPA621KP/KU			OPA621KG/SG			OPA621LG			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
INPUT NOISE											
Voltage: f_o= 100Hz	R_S = 0Ω		10			*			*		nV/√Hz
f_o= 1kHz			5.5			*			*		nV/√Hz
f_o= 10kHz			3.3			*			*		nV/√Hz
f_o= 100kHz			2.5			*			*		nV/√Hz
f_o= 1MHz to 100MHz			2.3			*			*		nV/√Hz
f_B= 100Hz to 10MHz			8.0			*			*		µV, rms
Current: f_o= 10kHz to 100MHz			2.3			*			*		pA/√Hz
OFFSET VOLTAGE[1]											
Input Offset Voltage	V_{CM} = 0VDC		±200	±1mV		*	*		±100	±500	µV
Average Drift	T_A = T_{MIN} to T_{MAX}		±12			*			*		µV/°C
Supply Rejection	±V_{CC} = 4.5V to 5.5V	50	60		*	*		55	*		dB
BIAS CURRENT											
Input Bias Current	V_{CM} = 0VDC		18	30		*	*		*	25	µA
OFFSET CURRENT											
Input Offset Current	V_{CM} = 0VDC		0.2	2		*	*		*	*	µA
INPUT IMPEDANCE											
Differential	Open-Loop		15 || 1			*			*		kΩ || pF
Common-Mode			1 || 1			*			*		MΩ || pF
INPUT VOLTAGE RANGE											
Common-Mode Input Range		±3.0	±3.5		*	*		*	*		V
Common-Mode Rejection	V_{IN} = ±2.5VDC, V_O = 0VDC	65	75		*	*	-	70	*		dB
OPEN-LOOP GAIN, DC											
Open-Loop Voltage Gain	R_L = 100Ω	50	60		*	*		55	*		dB
	R_L = 50Ω	48	58		*	*		53	*		dB
FREQUENCY RESPONSE											
Closed-Loop Bandwidth											
(–3dB)	Gain = +2V/V		500			*			*		MHz
	Gain = +5V/V		100			*			*		MHz
	Gain = +10V/V		50			*			*		MHz
Gain-Bandwidth	Gain = +10V/V		500			*			*		MHz
Differential Gain	3.58MHz, G = +2V/V		0.05			*			*		%
Differential Phase	3.58MHz, G = +2V/V		0.05			*			*		Degrees
Harmonic Distortion[2]	G = +2V/V, f = 10MHz, V_O = 2Vp-p										
	f = 10MHz, Second Harmonic		–62	–50		*	*		*	*	dBc[3]
	Third Harmonic		–80	–70		*	*		*	*	dBc
Full Power Response[2]	V_O = 5Vp-p, Gain = +2V/V	22	32		*	*		*	*		MHz
	V_O = 2Vp-p, Gain = +2V/V	55	80		*	*		*	*		MHz
Slew Rate[2]	2V Step, Gain = –2V/V	350	500		*	*		*	*		V/µs
Overshoot	2V Step, Gain = –2V/V		15			*			*		%
Settling Time: 0.1%	2V Step, Gain = –2V/V		15			*			*		ns
0.01%			25			*			*		ns
Phase Margin	Gain = +2V/V		50			*			*		Degrees
Rise Time	Gain = +2V/V, 10% to 90%								*		
	V_O = 100mVp-p; Small Signal		1.8			*			*		ns
	V_O = 6Vp-p; Large Signal		8			*			*		ns
RATED OUTPUT											
Voltage Output	R_L = 100Ω	±3.0	±3.5		*	*		*	*		V
	R_L = 50Ω	±2.5	±3.0		*	*		*	*		V
Output Resistance	1MHz, Gain = +2V/V		0.015			*			*		Ω
Load Capacitance Stability	Gain = +2V/V		15			*			*		pF
Short Circuit Current	Continuous		±150			*			*		mA
POWER SUPPLY											
Rated Voltage	±V_{CC}		5			*			*		VDC
Derated Performance	±V_{CC}	4.0		6.0	*		*	*		*	VDC
Current, Quiescent	I_O = 0mADC		26	28		*	*		*	*	mA
TEMPERATURE RANGE											
Specification: KP, KU, KG, LG	Ambient Temperature	0		+70	*		*	*		*	°C
SG					–55		+125				°C
Operating: KG, LG, SG	Ambient Temperature				–55		+125	–55		+125	°C
KP, KU		–25		+85							°C
θ_{JA} KG, LG, SG						125			125		°C/W
KP			90								°C/W
KU			100								°C/W

* Same Specifications as for KP/KU.

SPECIFICATIONS (CONT)

ELECTRICAL (FULL TEMPERATURE RANGE SPECIFICATIONS)

At V_{CC} = ±5VDC, R_L = 100Ω, and T_A = T_{MIN} to T_{MAX} unless otherwise noted.

PARAMETER	CONDITIONS	OPA621KP/KU			OPA621KG/SG			OPA621LG			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
TEMPERATURE RANGE											
Specification: KP, KU, KG, LG	Ambient Temperature	0		+70	*		*	*		*	°C
SG					–55		+125				°C
OFFSET VOLTAGE[1]											
Average Drift	T_A = T_{MIN} to T_{MAX}		±12			*			*		µV/°C
Supply Rejection	±V_{CC} = 4.5V to 5.5V	45	60		*	*		50	*		dB
BIAS CURRENT											
Input Bias Current	V_{CM} = 0VDC		18	40		*	*		*	35	µA
OFFSET CURRENT											
Input Offset Current	V_{CM} = 0VDC		0.2	5		*	*		*	*	µA
INPUT VOLTAGE RANGE											
Common-Mode Input Range		±2.5	±3.0		*	*		*	*		V
Common-Mode Rejection	V_{IN} = ±2.5VDC, V_O = 0VDC	60	75		*	*		65	*		dB
OPEN LOOP GAIN, DC											
Open-Loop Voltage Gain	R_L = 100Ω	46	60		*	*		52	*		dB
	R_L = 50Ω	44	58		*	*		50	*		dB
RATED OUTPUT											
Voltage Output	R_L = 100Ω	±3.0	±3.5		*	*		*	*		V
	R_L = 50Ω	±2.5	±3.0		*	*		*	*		V
POWER SUPPLY											
Current, Quiescent	I_O = 0mADC		26	30		*	*		*	*	mA

* Same specifications as for KP/KU.

NOTES: (1) Offset Voltage specifications are also guaranteed with units fully warmed up. (2) Parameter is sample tested. (3) dBc = dB referred to carrier-input signal.

ORDERING INFORMATION

OPA621 ( )( )

- Basic Model Number
- Performance Grade Code
  - K, L = –25°C to +85°C
  - S = –55°C to +125°C
- Package Code
  - G = 8-pin Ceramic DIP
  - P = 8-pin Plastic DIP
  - U = 8-pin Plastic SOIC
- Reliability Screening

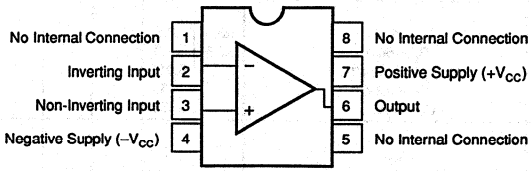
ABSOLUTE MAXIMUM RATINGS

Supply	±7VDC
Internal Power Dissipation[4]	See Applications Information
Differential Input Voltage	Total V_{CC}
Input Voltage Range	See Applications Information
Storage Temperature Range KG, LG, SG:	–65°C to +150°C
KP, KU:	–40°C to +125°C
Lead Temperature (soldering, 10s)	+300°C
(soldering, SOIC 3s)	+260°C
Output Short Circuit to Ground (+25°C)	Continuous to Ground
Junction Temperature (T_J)	+175°C

NOTE: (4) Packages must be derated based on specified θ_{JA}. Maximum T_J must be observed.

PIN CONFIGURATION (8-PIN DIP)

Top View



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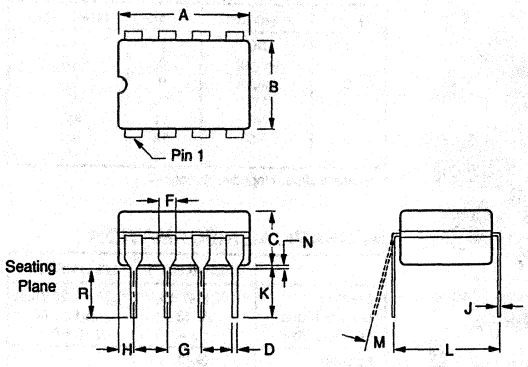
MECHANICAL

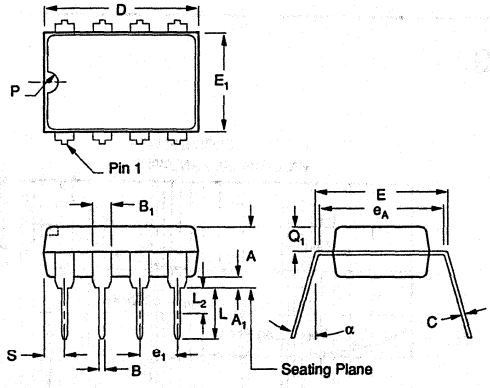
G Package — 8-Pin Ceramic



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.375	.405	9.53	10.28
B	.245	.251	6.22	6.38
C	.140	.170	3.56	4.32
D	.015	.021	0.38	0.53
F	.045	.060	1.14	1.52
G	.100 BASIC		2.54 BASIC	
H	—	.098	—	2.49
J	.008	.012	0.20	0.30
K	.150	—	3.80	—
L	.290	.320	7.37	8.13
M	0°	15°	0°	15°
N	.009	.060	0.23	1.52
R	.125	.175	3.18	4.45

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

P Package — 8-Pin Plastic DIP

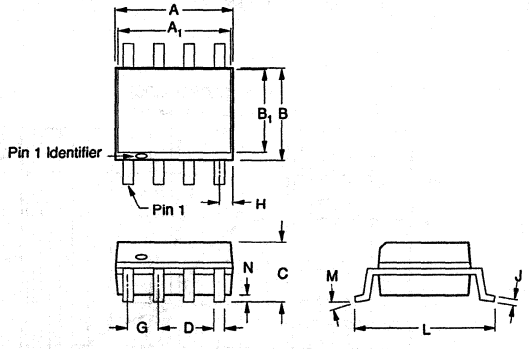


DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.155	.200	3.94	5.08
A1	.020	.050	0.51	1.27
B	.014	.020	0.36	0.51
B1	.045	.065	1.14	1.65
C	.008	.012	0.20	0.30
D (1)	.370	.400	9.40	10.16
E	.300	.325	7.62	8.26
E1	.240	.260	6.10	6.60
e1	.100 BASIC		2.54 BASIC	
eA	.300 BASIC		7.62 BASIC	
L	.125	.150	3.18	3.81

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
L2(2)	0	.030	0.00	0.76
α	0°	15°	0°	15°
P	.015	.050	0.38	1.270
Q1	.040	.075	1.02	1.91
S (1)	.015	.050	0.38	1.27

(1) Not JEDEC Std.
(2) e_1 and e_A applies in zone L_2 when unit installed.
NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

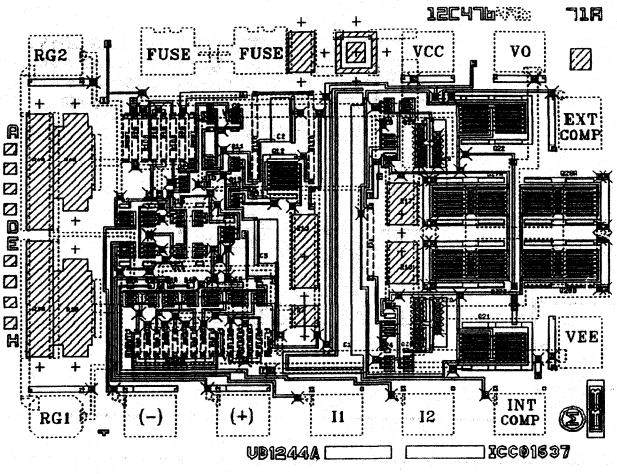
U Package — 8-Pin SOIC



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.185	.201	4.70	5.11
A1	.178	.201	4.52	5.11
B	.146	.162	3.71	4.11
B1	.130	.149	3.30	3.78
C	.054	.145	1.37	3.69
D	.015	.019	0.38	0.48
G	.050 BASIC		1.27 BASIC	
H	.018	.026	0.46	0.66
J	.008	.012	0.20	0.30
L	.220	.252	5.59	6.40
M	0°	10°	0°	10°
N	.000	.012	0.00	0.30

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

DICE INFORMATION



OPA621 DIE TOPOGRAPHY

PAD	FUNCTION	PAD	FUNCTION
1	NC	7	$-V_{CC}$
2	–Input	8	NC
3	+Input	9	V_{OUT}
4	NC	10	$+V_{CC}$
5	NC	11	NC
6	NC	12	NC
		13	NC

Substrate Bias: Negative Supply $-V_{CC}$.

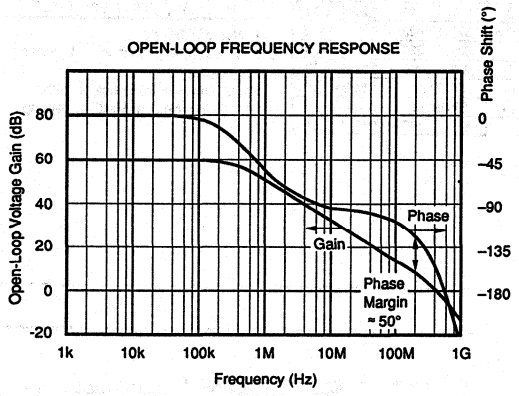
MECHANICAL INFORMATION

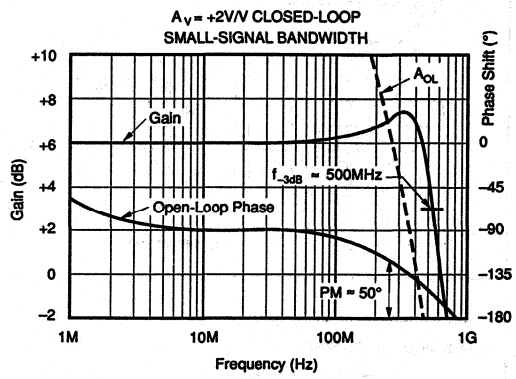
	MILS (0.001")	MILLIMETERS
Die Size	63 x 47 ±5	1.60 x 1.20 ±0.13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.10 x 0.10
Backing	Gold	
Top Metalization	Gold	

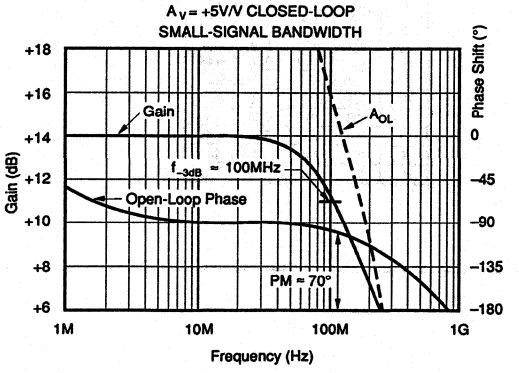
See "DICE PRODUCTS" Section 17 in Data Book Supplement Volume 33c, or contact Burr-Brown for current information.

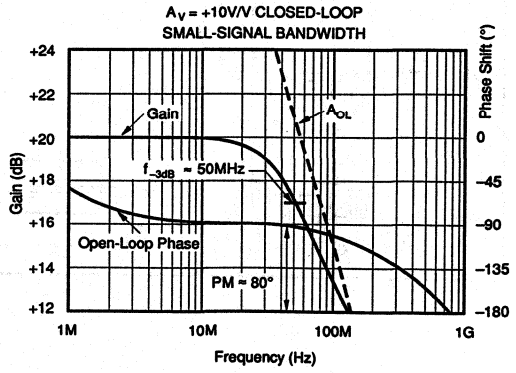
TYPICAL PERFORMANCE CURVES

At V_{CC} = ±5VDC, R_L = 100Ω, and T_A = +25°C unless otherwise noted.





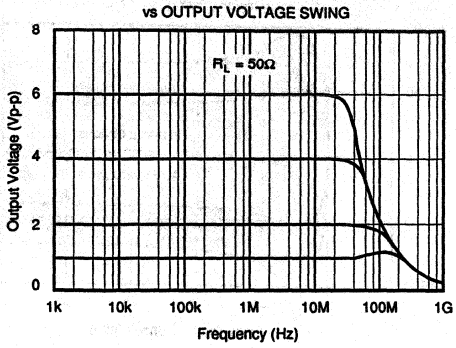




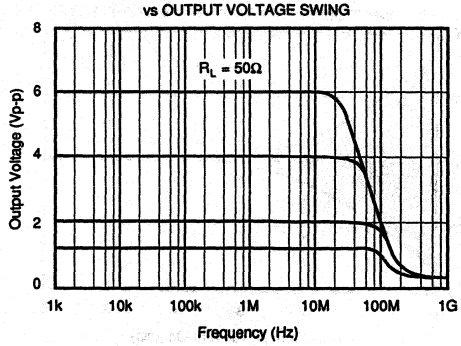
TYPICAL PERFORMANCE CURVES (CONT)

At V_{CC} = ±5VDC, R_L = 100Ω, and T_A = +25°C unless otherwise noted.

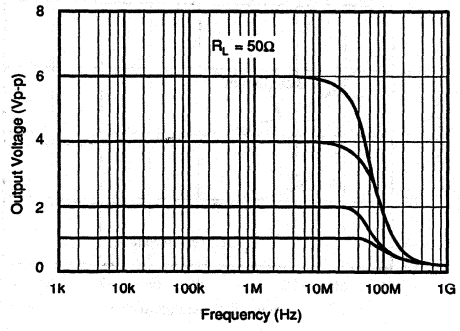
A_V = +2V/V CLOSED-LOOP BANDWIDTH vs OUTPUT VOLTAGE SWING



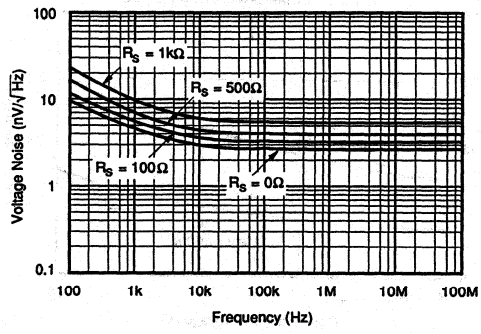
A_V = +5V/V CLOSED-LOOP BANDWIDTH vs OUTPUT VOLTAGE SWING



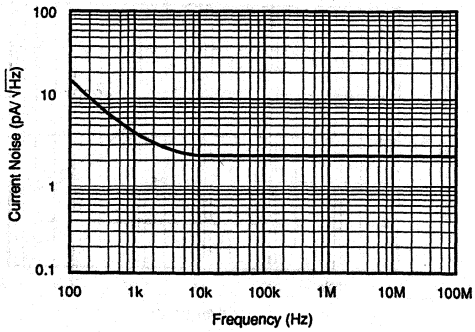
A_V = +10V/V CLOSED-LOOP BANDWIDTH vs OUTPUT VOLTAGE SWING



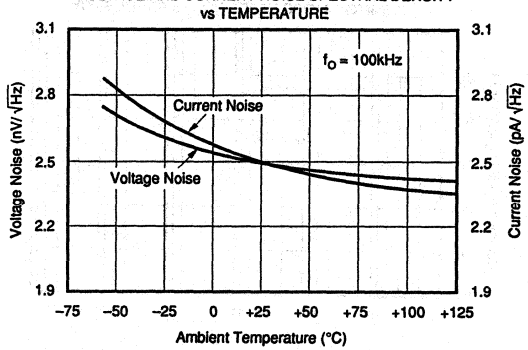
TOTAL INPUT VOLTAGE NOISE SPECTRAL DENSITY vs SOURCE RESISTANCE



INPUT CURRENT NOISE SPECTRAL DENSITY



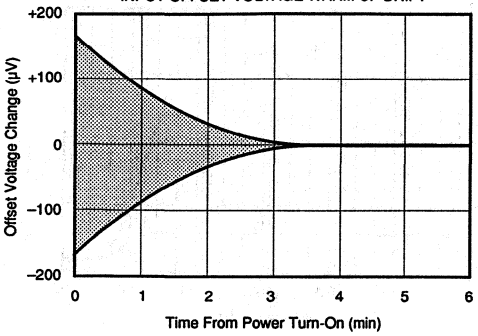
VOLTAGE AND CURRENT NOISE SPECTRAL DENSITY vs TEMPERATURE



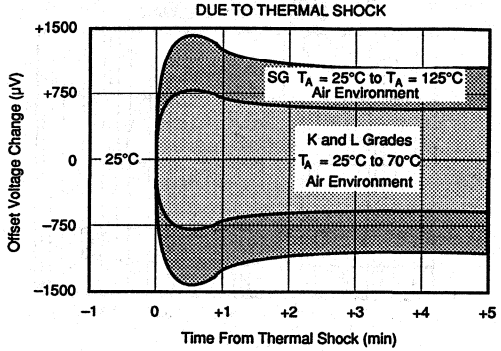
TYPICAL PERFORMANCE CURVES (CONT)

At V_{CC} = ±5VDC, R_L = 100Ω, and T_A = +25°C unless otherwise noted.

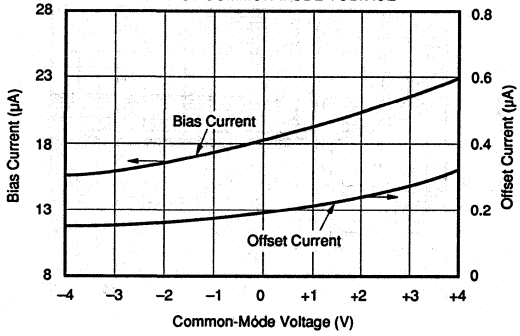
INPUT OFFSET VOLTAGE WARM-UP DRIFT



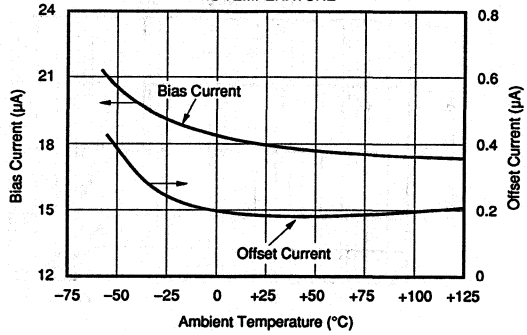
INPUT OFFSET VOLTAGE CHANGE DUE TO THERMAL SHOCK



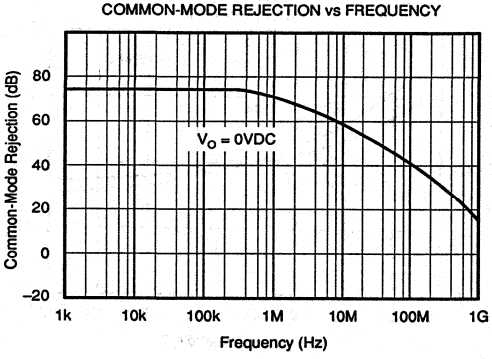
BIAS AND OFFSET CURRENT vs INPUT COMMON-MODE VOLTAGE



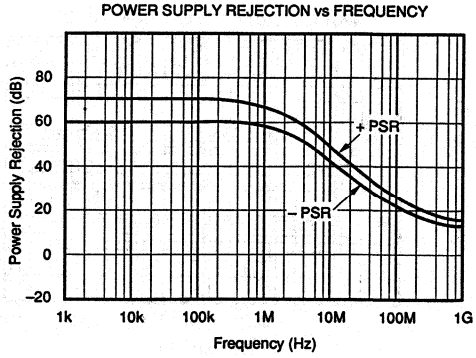
BIAS AND OFFSET CURRENT vs TEMPERATURE



COMMON-MODE REJECTION vs FREQUENCY



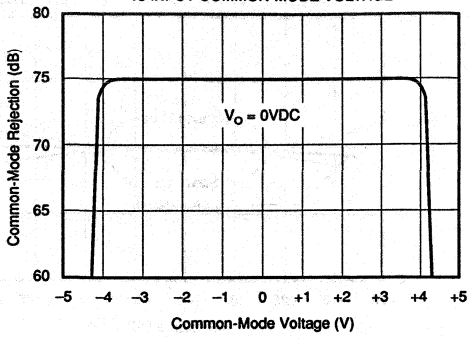
POWER SUPPLY REJECTION vs FREQUENCY



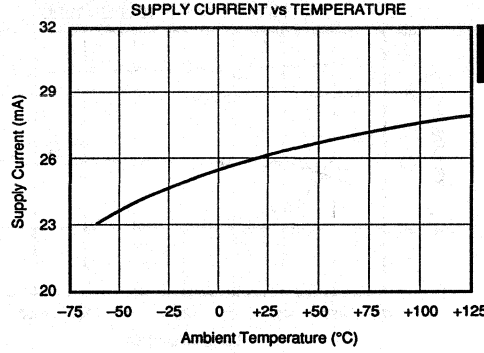
TYPICAL PERFORMANCE CURVES (CONT)

At V_{CC} = ±5VDC, R_L = 100Ω, and T_A = +25°C unless otherwise noted.

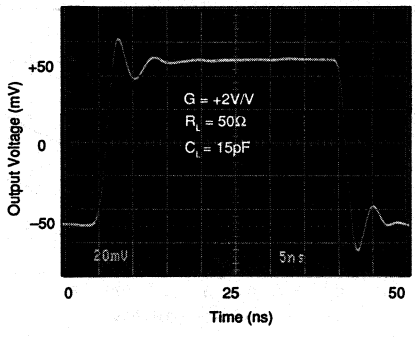
COMMON-MODE REJECTION
vs INPUT COMMON-MODE VOLTAGE



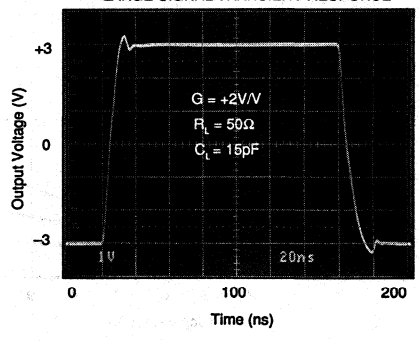
SUPPLY CURRENT vs TEMPERATURE



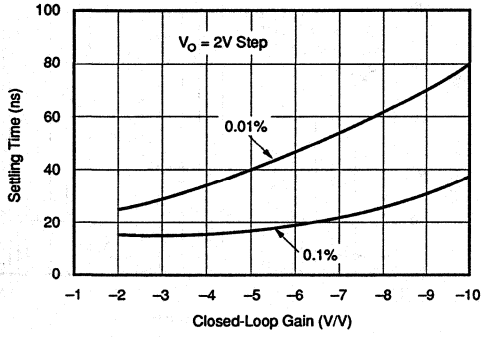
SMALL-SIGNAL TRANSIENT RESPONSE



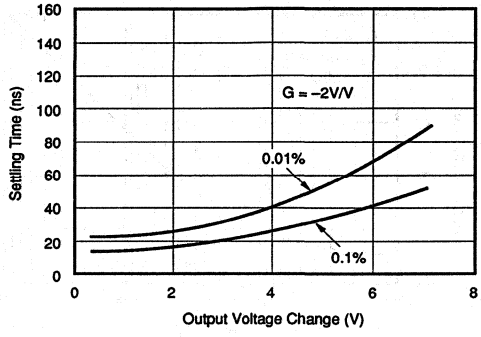
LARGE-SIGNAL TRANSIENT RESPONSE



SETTLING TIME vs CLOSED-LOOP GAIN



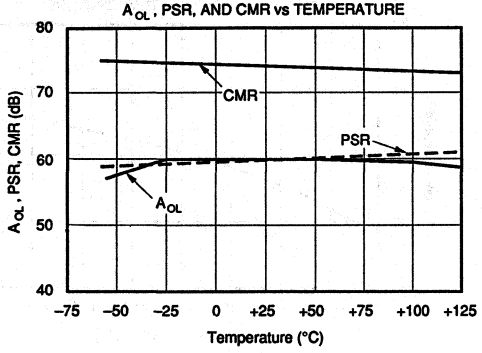
SETTLING TIME vs OUTPUT VOLTAGE CHANGE



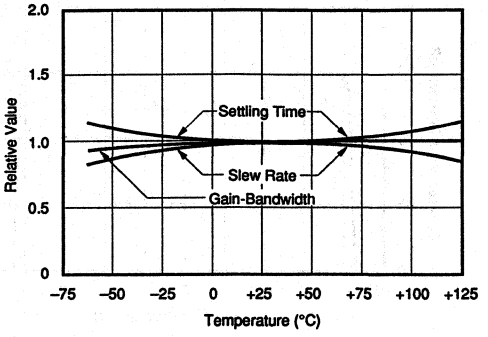
TYPICAL PERFORMANCE CURVES (CONT)

At V_{CC} = ±5VDC, R_L = 100Ω, and T_A = +25°C unless otherwise noted.

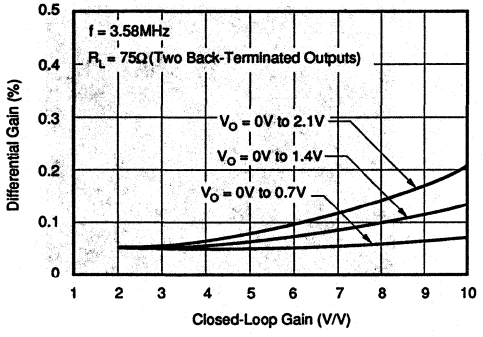
A_{OL}, PSR, AND CMR vs TEMPERATURE



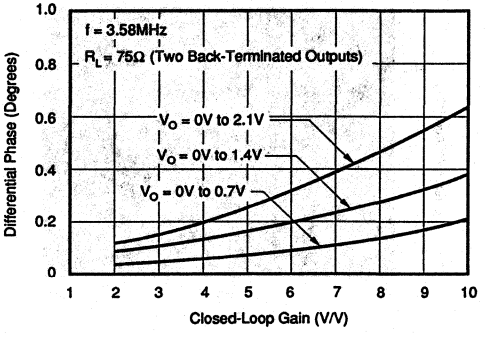
FREQUENCY CHARACTERISTICS vs TEMPERATURE



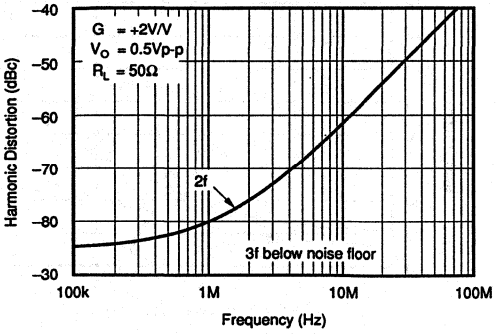
NTSC DIFFERENTIAL GAIN vs CLOSED-LOOP GAIN



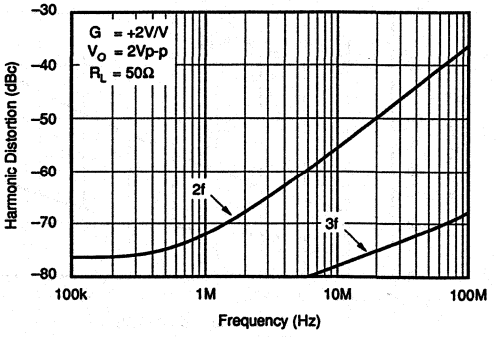
NTSC DIFFERENTIAL PHASE vs CLOSED-LOOP GAIN



SMALL-SIGNAL
HARMONIC DISTORTION vs FREQUENCY

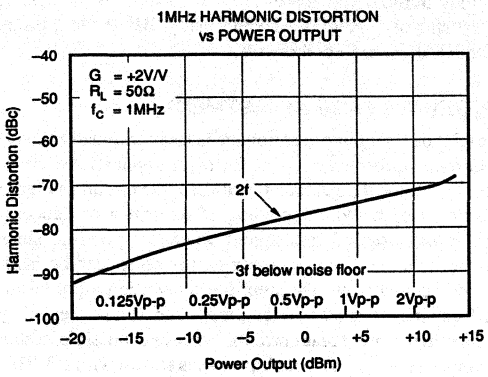


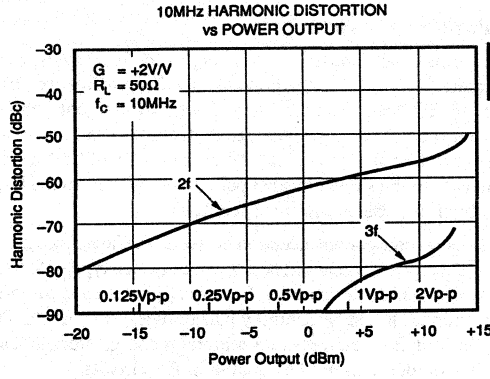
LARGE-SIGNAL
HARMONIC DISTORTION vs FREQUENCY



TYPICAL PERFORMANCE CURVES (CONT)

At V_{CC} = ±5VDC, R_L = 100Ω, and T_A = +25°C unless otherwise noted.





APPLICATIONS INFORMATION

DISCUSSION OF PERFORMANCE

The OPA621 provides a level of speed and precision not previously attainable in monolithic form. Unlike current feedback amplifiers, the OPA621's design uses a "Classical" operational amplifier architecture and can therefore be used in all traditional operational amplifier applications. While it is true that current feedback amplifiers can provide wider bandwidth at higher gains, they offer many disadvantages. The asymmetrical input characteristics of current feedback amplifiers (i.e. one input is a low impedance) prevents them from being used in a variety of applications. In addition, unbalanced inputs make input bias current errors difficult to correct. Bias current cancellation through matching of inverting and non-inverting input resistors is impossible because the input bias currents are uncorrelated. Current noise is also asymmetrical and is usually significantly higher on the inverting input. Perhaps most important, settling time to 0.01% is often extremely poor due to internal design tradeoffs. Many current feedback designs exhibit settling times to 0.01% in excess of 10 microseconds even though 0.1% settling times are reasonable. Such amplifiers are completely inadequate for fast settling 12-bit applications.

The OPA621's "Classical" operational amplifier architecture employs true differential and fully symmetrical inputs to eliminate these troublesome problems. All traditional circuit configurations and op amp theory apply to the OPA621. The use of low-drift thin-film resistors allows internal operating currents to be laser-trimmed at wafer-level to optimize AC performance such as bandwidth and settling time, as well as DC parameters such as input offset voltage and drift. The result is a wideband, high-frequency monolithic operational amplifier with a gain-bandwidth product of 500MHz, a 0.01% settling time of 25ns, and an input offset voltage of 100µV.

WIRING PRECAUTIONS

Maximizing the OPA621's capability requires some wiring precautions and high-frequency layout techniques. Oscillation, ringing, poor bandwidth and settling, gain peaking, and instability are typical problems plaguing all high-speed amplifiers when they are improperly used. In general, all printed circuit board conductors should be wide to provide low resistance, low impedance signal paths. They should also be as short as possible. The entire physical circuit should be as small as practical. Stray capacitances should be minimized, especially at high impedance nodes, such as the amplifier's input terminals. Stray signal coupling from the output or power supplies to the inputs should be minimized. All circuit element leads should be no longer than 1/4 inch (6mm) to minimize lead inductance, and low values of resistance should be used. This will minimize time constants formed with the circuit capacitances and will eliminate stray, parasitic circuits.

Grounding is the most important application consideration for the OPA621, as it is with all high-frequency circuits. Oscillations at frequencies of 500MHz and above can easily occur if good grounding techniques are not used. A heavy ground plane (2oz copper recommended) should connect all unused areas on the component side. Good ground planes can reduce stray signal pickup, provide a low resistance, low inductance common return path for signal and power, and can conduct heat from active circuit package pins into ambient air by convection.

Supply bypassing is extremely critical and must always be used, especially when driving high current loads. Both power supply leads should be bypassed to ground as close as possible to the amplifier pins. Tantalum capacitors (1µF to 10µF) with very short leads are recommended. Although not required, a parallel 0.01µF ceramic may be added if desired. Surface mount bypass capacitors will produce excellent results due to their low lead inductance. Additionally, sup-

pression filters can be used to isolate noisy supply lines. Properly bypassed and modulation-free power supply lines allow full amplifier output and optimum settling time performance.

Points to Remember

1) Don't use point-to-point wiring as the increase in wiring inductance will be detrimental to AC performance. However, if it must be used, very short, direct signal paths are required. The input signal ground return, the load ground return, and the power supply common should all be connected to the same physical point to eliminate ground loops, which can cause unwanted feedback.

2) Good component selection is essential. Capacitors used in critical locations should be a low inductance type with a high quality dielectric material. Likewise, diodes used in critical locations should be Schottky barrier types, such as HP5082-2835 for fast recovery and minimum charge storage. Ordinary diodes will not be suitable in RF circuits.

3) Whenever possible, solder the OPA621 directly into the PC board without using a socket. Sockets add parasitic capacitance and inductance, which can seriously degrade AC performance or produce oscillations. If sockets must be used, consider using zero-profile solderless sockets such as Augat part number 8134-HC-5P2. Alternately, Teflon® standoffs located close to the amplifier's pins can be used to mount feedback components.

4) Resistors used in feedback networks should have values of a few hundred ohms for best performance. Shunt capacitance problems limit the acceptable resistance range to about 1kΩ on the high end and to a value that is within the amplifier's output drive limits on the low end. Metal film and carbon resistors will be satisfactory, but wirewound resistors (even "non-inductive" types) are absolutely unacceptable in high-frequency circuits.

5) Surface mount components (chip resistors, capacitors, etc) have low lead inductance and are therefore strongly recommended. Circuits using all surface mount components with the OPA621AU (SOIC package) will offer the best AC performance. The parasitic package inductance and capacitance for the SOIC is lower than the both the Cerdip and 8-lead Plastic DIP.

6) Avoid overloading the output. Remember that output current must be provided by the amplifier to drive its own feedback network as well as to drive its load. Lowest distortion is achieved with high impedance loads.

7) Don't forget that these amplifiers use ±5V supplies. Although they will operate perfectly well with +5V and –5.2V, use of ±15V supplies will destroy the part.

8) Standard commercial test equipment has not been designed to test devices in the OPA621's speed range. Benchtop op amp testers and ATE systems will require a special test head to successfully test these amplifiers.

9) Terminate transmission line loads. Unterminated lines, such as coaxial cable, can appear to the amplifier to be a capacitive or inductive load. By terminating a transmission line with its characteristic impedance, the amplifier's load then appears purely resistive.

10) Plug-in prototype boards and wire-wrap boards will not be satisfactory. A clean layout using RF techniques is essential; there are no shortcuts.

Teflon® E. I. Du Pont de Nemours & Co.

OFFSET VOLTAGE ADJUSTMENT

The OPA621's input offset voltage is laser-trimmed and will require no further adjustment for most applications. However, if additional adjustment is needed, the circuit in Figure 1 can be used without degrading offset drift with temperature. Avoid external adjustment whenever possible since extraneous noise, such as power supply noise, can be inadvertently coupled into the amplifier's inverting input terminal. Remember that additional offset errors can be created by the amplifier's input bias currents. Whenever possible, match the impedance seen by both inputs as is shown with R3. This will reduce input bias current errors to the amplifier's offset current, which is typically only 0.2µA.

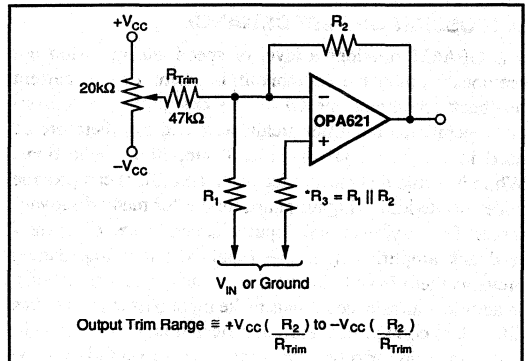


FIGURE 1. Offset Voltage Trim.

INPUT PROTECTION

Static damage has been well recognized for MOSFET devices, but any semiconductor device deserves protection from this potentially damaging source. The OPA621 incorporates on-chip ESD protection diodes as shown in Figure 2. This eliminates the need for the user to add external protection diodes, which can add capacitance and degrade AC performance.

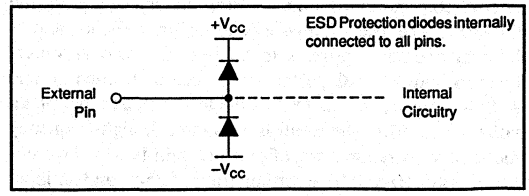


FIGURE 2. Internal ESD Protection.

All pins on the OPA621 are internally protected from ESD by means of a pair of back-to-back reverse-biased diodes to either power supply as shown. These diodes will begin to conduct when the input voltage exceeds either power supply by about 0.7V. This situation can occur with loss of the amplifier's power supplies while a signal source is still present. The diodes can typically withstand a continuous current of 30mA without destruction. To insure long term reliability, however, diode current should be externally limited to 10mA or so whenever possible.

The internal protection diodes are designed to withstand 2.5kV (using Human Body Model) and will provide adequate ESD protection for most normal handling procedures. However, static damage can cause subtle changes in amplifier input characteristics without necessarily destroying the device. In precision operational amplifiers, this may cause a noticeable degradation of offset voltage and drift. Therefore, static protection is strongly recommended when handling the OPA621.

OUTPUT DRIVE CAPABILITY

The OPA621's design uses large output devices and has been optimized to drive 50Ω and 75Ω resistive loads. The device can easily drive 6Vp-p into a 50Ω load. This high-output drive capability makes the OPA621 an ideal choice for a wide range of RF, IF, and video applications. In many cases, additional buffer amplifiers are unneeded.

Internal current-limiting circuitry limits output current to about 150mA at 25°C. This prevents destruction from accidental shorts to common and eliminates the need for external current-limiting circuitry. Although the device can withstand momentary shorts to either power supply, it is not recommended.

Many demanding high-speed applications such as ADC/DAC buffers require op amps with low wideband output impedance. For example, low output impedance is essential when driving the signal-dependent capacitances at the inputs of flash A/D converters. As shown in Figure 3, the OPA621 maintains very low closed-loop output impedance over frequency. Closed-loop output impedance increases with frequency since loop gain is decreasing with frequency.

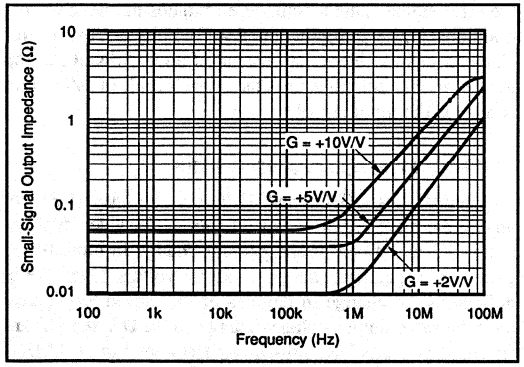


FIGURE 3. Small-Signal Output Impedance vs Frequency.

THERMAL CONSIDERATIONS

The OPA621 does not require a heat sink for operation in most environments. The use of a heat sink, however, will reduce the internal thermal rise and will result in cooler, more reliable operation. At extreme temperatures and under full load conditions a heat sink is necessary. See "Maximum Power Dissipation" curve, Figure 4.

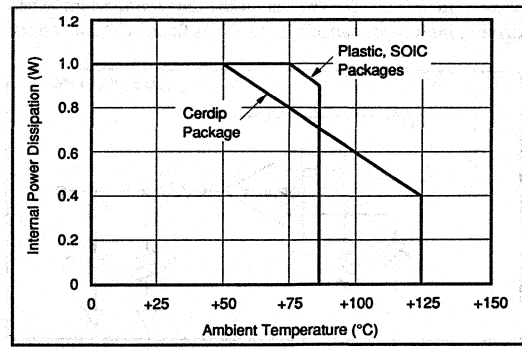


FIGURE 4. Maximum Power Dissipation.

The internal power dissipation is given by the equation $P_D = P_{DQ} + P_{DL}$, where P_{DQ} is the quiescent power dissipation and P_{DL} is the power dissipation in the output stage due to the load. (For $\pm V_{CC} = \pm 5V$, $P_{DQ} = 10V \times 28mA = 280mW$, max). For the case where the amplifier is driving a grounded load (R_L) with a DC voltage ($\pm V_{OUT}$) the maximum value of P_{DL} occurs at $\pm V_{OUT} = \pm V_{CC}/2$, and is equal to P_{DL}, max = $(\pm V_{CC})^2/4R_L$. Note that it is the voltage across the output transistor, and not the load, that determines the power dissipated in the output stage.

When the output is shorted to common $P_{DL} = 5V \times 150mA = 750mW$. Thus, $P_D = 280mW + 750mW \cong 1W$. Note that the short-circuit condition represents the maximum amount of internal power dissipation that can be generated. Thus, the "Maximum Power Dissipation" curve starts at 1W and is derated based on a 175°C maximum junction temperature and the junction-to-ambient thermal resistance, θ_{JA}, of each package. The variation of short-circuit current with temperature is shown in Figure 5.

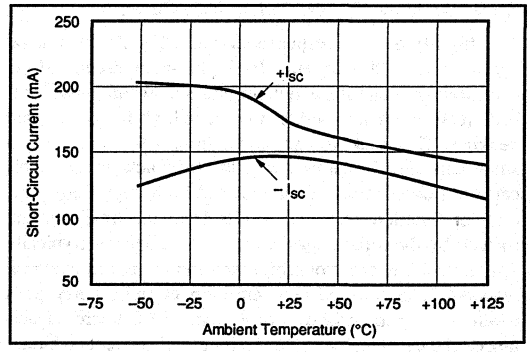


FIGURE 5. Short-Circuit Current vs Temperature.

CAPACITIVE LOADS

The OPA621's output stage has been optimized to drive resistive loads as low as 50Ω. Capacitive loads, however, will decrease the amplifier's phase margin which may cause high frequency peaking or oscillations. Capacitive loads greater than 15pF should be buffered by connecting a small resistance, usually 5Ω to 25Ω, in series with the output as shown in Figure 6. This is particularly important when driving high capacitance loads such as flash A/D converters.

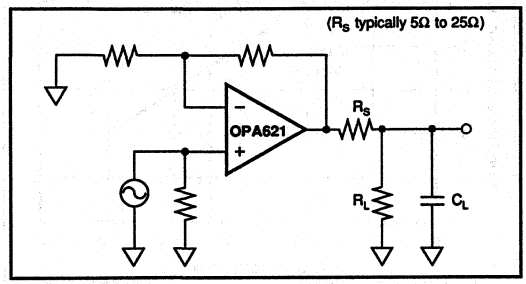


FIGURE 6. Driving Capacitive Loads.

In general, capacitive loads should be minimized for optimum high frequency performance. Coax lines can be driven if the cable is properly terminated. The capacitance of coax cable (29pF/foot for RG-58) will not load the amplifier when the coaxial cable or transmission line is terminated in its characteristic impedance.

COMPENSATION

The OPA621 is stable in inverting gains of ≥–2V/V and in non-inverting gains ≥+2V/V. Phase margin for both configurations is approximately 50°. Inverting and non-inverting gains of unity should be avoided. The minimum stable gains of +2V/V and –2V/V are the most demanding circuit configurations for loop stability and oscillations are most likely to occur in these gains. If possible, use the device in a noise gain greater than three to improve phase margin and reduce the susceptibility to oscillation. (Note that, from a stability standpoint, an inverting gain of –2V/V is equivalent to a noise gain of 3.) Gain and phase response for other gains are shown in the Typical Performance Curves.

The high-frequency response of the OPA621 in a good layout is flat with frequency for higher-gain circuits. However, low-gain circuits and configurations where large feedback resistances are used, can produce high-frequency gain peaking. This peaking can be minimized by connecting a small capacitor in parallel with the feedback resistor. This capacitor compensates for the closed-loop, high frequency, transfer function zero that results from the time constant formed by the input capacitance of the amplifier (typically 2pF after PC board mounting), and the input and feedback resistors. The selected compensation capacitor may be a trimmer, a fixed capacitor, or a planned PC board capacitance. The capacitance value is strongly dependent on circuit layout and closed-loop gain. Using small resistor values will preserve the phase margin and avoid peaking by keeping the break frequency of this zero sufficiently high. When high closed-loop gains are required, a three-resistor attenuator (tee network) is recommended to avoid using large value resistors with large time constants.

SETTLING TIME

Settling time is defined as the total time required, from the input signal step, for the output to settle to within the specified error band around the final value. This error band is expressed as a percentage of the value of the output transition, a 2V step. Thus, settling time to 0.01% requires an error band of ±200µV centered around the final value of 2V.

Settling time, specified in an inverting gain of two, occurs in only 25ns to 0.01% for a 2V step, making the OPA621 one of the fastest settling monolithic amplifiers commercially available. Settling time increases with closed-loop gain and output voltage change as described in the Typical Performance Curves. Preserving settling time requires critical attention to the details as mentioned under "Wiring Precautions." The amplifier also recovers quickly from input overloads. Overload recovery time to linear operation from a 50% overload is typically only 30ns.

In practice, settling time measurements on the OPA621 prove to be very difficult to perform. Accurate measurement is next to impossible in all but the very best equipped labs. Among other things, a fast flat-top generator and high speed oscilloscope are needed. Unfortunately, fast flat-top generators, which settle to 0.01% in sufficient time, are scarce and expensive. Fast oscilloscopes, however, are more commonly available. For best results a sampling oscilloscope is recommended. Sampling scopes typically have bandwidths that are greater than 1GHz and very low capacitance inputs. They also exhibit faster settling times in response to signals that would tend to overload a real-time oscilloscope.

Figure 7 shows the test circuit used to measure settling time for the OPA621. This approach uses a 16-bit sampling oscilloscope to monitor the input and output pulses. These waveforms are captured by the sampling scope, averaged, and then subtracted from each other in software to produce the error signal. This technique eliminates the need for the traditional "false-summing junction," which adds extra parasitic capacitance. Note that instead of an additional flat-top generator, this technique uses the scope's built-in calibration source as the input signal.

DIFFERENTIAL GAIN AND PHASE

Differential Gain (DG) and Differential Phase (DP) are among the more important specifications for video applications. DG is defined as the percent change in closed-loop gain over a specified change in output voltage level. DP is defined as the change in degrees of the closed-loop phase over the same output voltage change. Both DG and DP are specified at the NTSC sub-carrier frequency of 3.58MHz. DG and DP increase with closed-loop gain and output

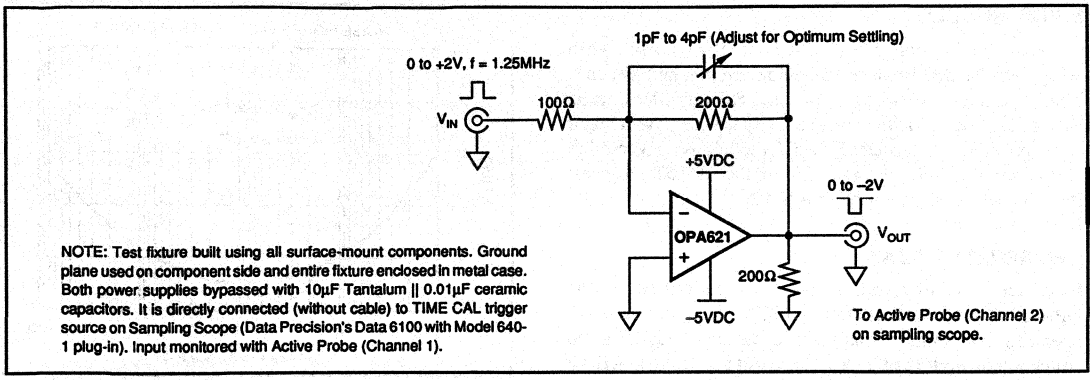


FIGURE 7. Settling Time Test Circuit.

voltage transition as shown in the Typical Performance Curves. All measurements were performed using a Tektronix model VM700 Video Measurement Set.

DISTORTION

The OPA621's Harmonic Distortion characteristics into a 50Ω load are shown vs frequency and power output in the Typical Performance Curves. Distortion can be further improved by increasing the load resistance as illustrated in Figure 8. Remember to include the contribution of the feedback resistance when calculating the effective load resistance seen by the amplifier.

Two-tone, third-order intermodulation distortion (IM) is an important parameter for many RF amplifier applications. Figure 9 shows the OPA621's two-tone, third-order IM intercept vs frequency. For these measurements, tones were spaced 1MHz apart. This curve is particularly useful for determining the magnitude of the third-order IM products as a function of frequency, load resistance, and gain. For example, assume that the application requires the OPA621 to operate in a gain of +2V/V and drive 2Vp-p into 50Ω at a frequency of 10MHz. Referring to Figure 9 we find that the intercept point is +47dBm. The magnitude of the third-order IM products can now be easily calculated from the expression:

$$\text{Third IMD} = 2(\text{OPI}^3\text{P} - P_O)$$

where OPI^3P = third-order output intercept, dBm
P_O = output level/tone, dBm/tone
Third IMD = third-order intermodulation ratio below each output tone, dB

For this case OPI^3P = 47dBm, P_O = 10dBm, and the third-order IMD = 2(47 – 10) = 74dB below either 10dBm tone. The OPA621's low IMD makes the device an excellent choice for a variety of RF signal processing applications.

NOISE FIGURE

The OPA621's voltage and current noise spectral densities are specified in the Typical Performance Curves. For RF applications, however, Noise Figure (NF) is often the preferred noise specification since it allows system noise performance to be more easily calculated. The OPA621's Noise Figure vs Source Resistance is shown in Figure 10.

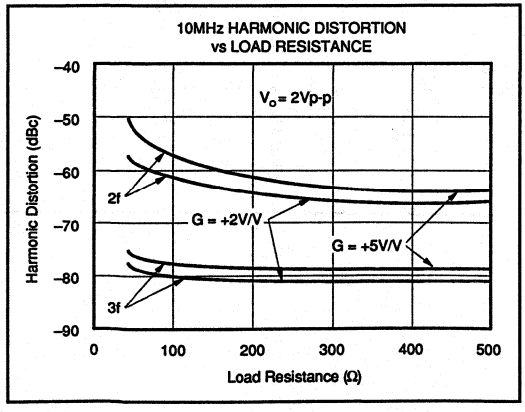


FIGURE 8. 10MHz Harmonic Distortion vs Load Resistance.

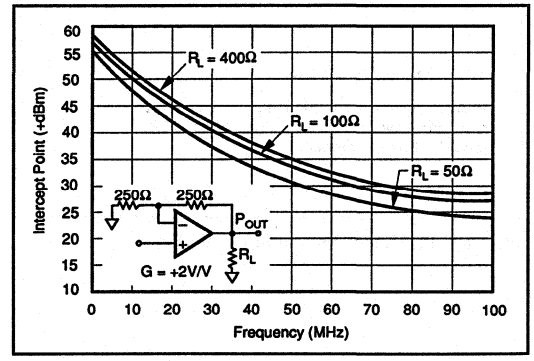


FIGURE 9. 2-Tone, 3rd Order Intermodulation Intercept vs Frequency.

SPICE MODELS

Computer simulation using SPICE is often useful when analyzing the performance of analog circuits and systems. This is particularly true for Video and RF amplifier circuits where parasitic capacitance and inductance can have a major effect on circuit performance. SPICE models using MicroSim Corporation's PSpice are available for the OPA621. Request Burr-Brown Application Note AN-167.

RELIABILITY DATA

Extensive reliability testing has been performed on the OPA621. Accelerated life testing (2000 hours) at maximum operating temperature was used to calculate MTTF at an ambient temperature of 25°C. These test results yield MTTF of: Cerdip package = 1.31E+9 Hours, Plastic DIP = 5.02E+7 Hours, and SOIC = 2.94E+7 Hours. Additional tests such as PCT have also been performed. Reliability reports are available upon request for each of the package options offered.

DEMONSTRATION BOARDS

Demonstration boards to speed prototyping are available. Request DEM1135 for 8-Pin DIP, and DEM1136 for SOIC package.

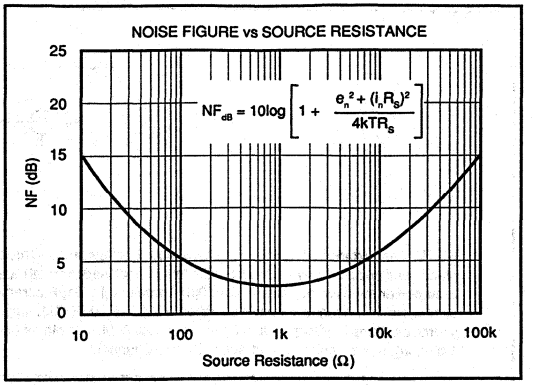


FIGURE 10. Noise Figure vs Source Resistance.

APPLICATIONS

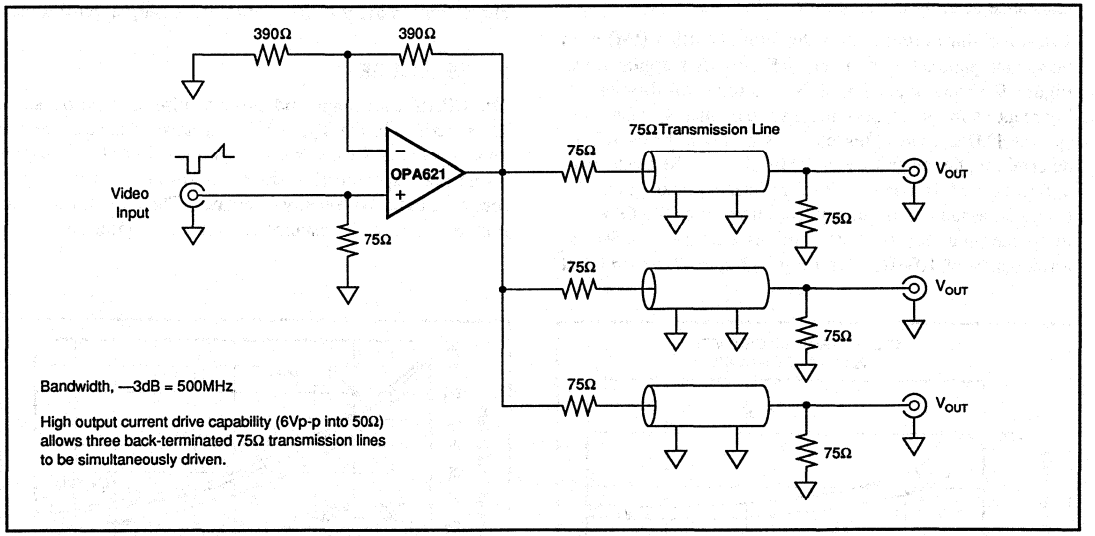


FIGURE 11. Video Distribution Amplifier.

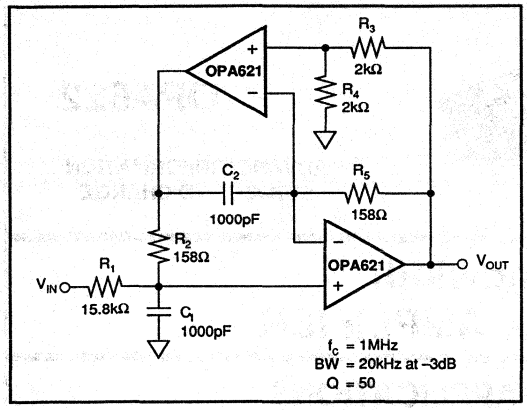


FIGURE 12. High-Q 1MHz Bandpass Filter

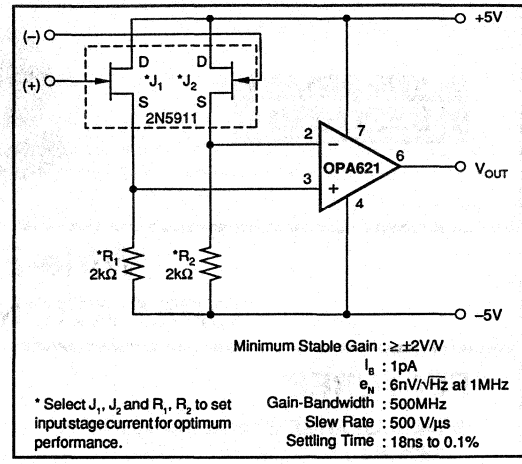


FIGURE 13. Low Noise, Wideband FET Input Op Amp.

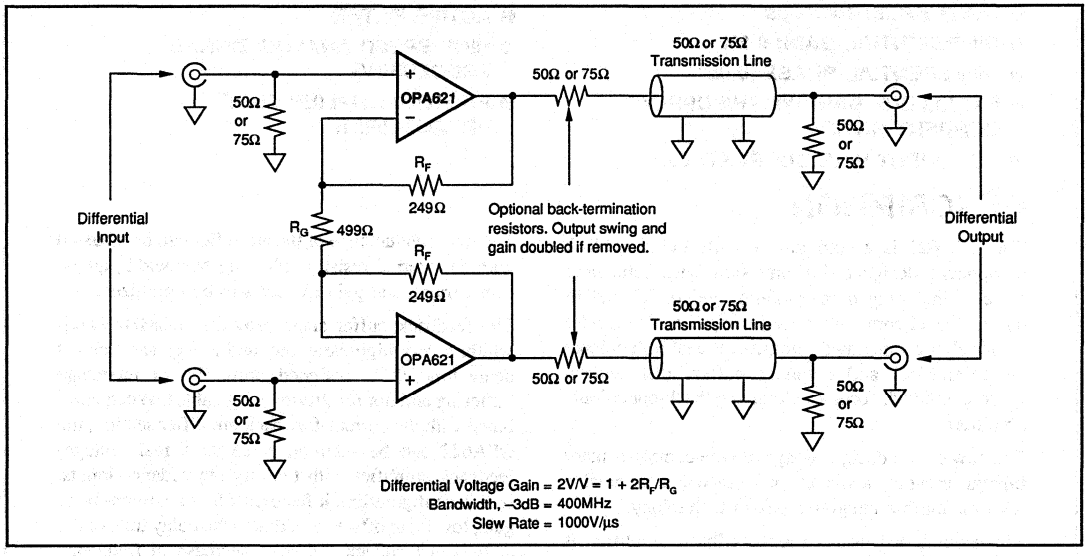


FIGURE 14. Differential Line Driver for 50Ω or 75Ω Systems.

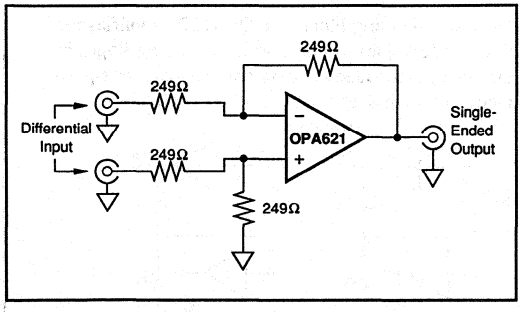


FIGURE 15. Unity Gain Difference Amplifier.

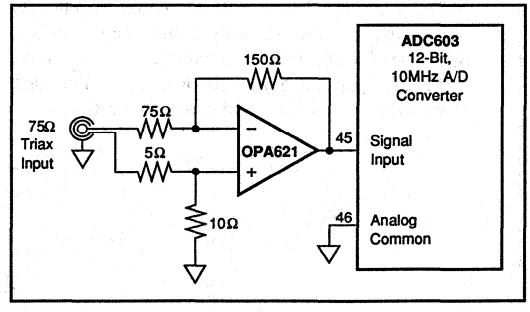
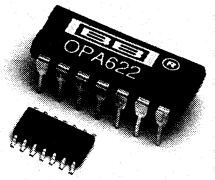


FIGURE 16. Differential Input Buffer Amplifier (G = –2V/V).

BURR-BROWN®



OPA622

ADVANCE INFORMATION
SUBJECT TO CHANGE

Wide-Bandwidth OPERATIONAL AMPLIFIER

FEATURES

- SMALL/LARGE SIGNAL BANDWIDTH: 180MHz
- HIGH OUTPUT CURRENT: ±70mA
- SLEW RATE: 1600V/µs
- DIFFERENTIAL GAIN: 0.2%
- DIFFERENTIAL PHASE: 0.05°
- EXCELLENT BANDWIDTH/SUPPLY CURRENT RATIO
- LOW INPUT BIAS CURRENT: 2µA

APPLICATIONS

- VIDEO EQUIPMENT
- COMMUNICATIONS
- PULSE/RF AMPLIFIERS
- ACTIVE FILTER
- HIGH SPEED ANALOG SIGNAL PROCESSING
- PHOTOMULTIPLIER TUBE PREAMPLIFIER

DESCRIPTION

The OPA622 is a common versatile building-block component designed for precision wide-bandwidth systems including high-resolution video, RF and IF circuitry, and communications equipment. It includes a monolithic integrated current-feedback operational amplifier block and a voltage buffer block, which, when combined, form a voltage-feedback operational amplifier.

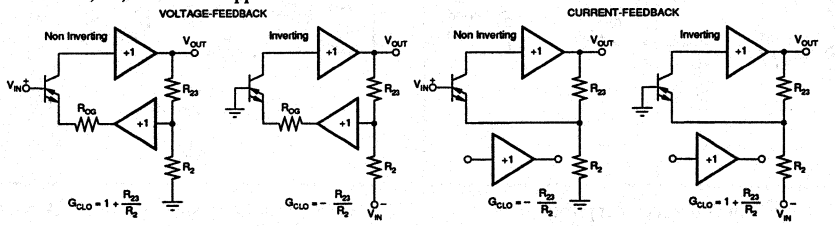
The new circuit design, along with the complementary bipolar process, achieves performance unattainable with monolithic integrated circuit technology.

When combined as a current-feedback amplifier, it provides a 280MHz large-signal bandwidth at ±2.5V output level and a 2500V/µs slew rate. The output buffer stage can deliver ±70mA output current. The high output current capability allows the OPA622 to drive two 50Ω or 75Ω lines with ±3V output swing, making it ideal along with the low differential gain/phase errors for RF, IF, and video applications.

The transconductance of the amplifier can be adjusted with an external resistor, allowing bandwidth, quiescent current, and gain tradeoffs to be optimized.

The feedback buffer stage provides 600MHz bandwidth, a very high slew rate, and a very short signal delay time. It is designed primarily for interstage buffering and not for driving long cables. When combined with the current-feedback amplifier section, the OPA622 can be interconnected as a real voltage-feedback amplifier with two high-impedance inputs. In this configuration, it features a low common-mode gain, low input offset, and, due to the delay time of the additional feedback buffer, a decrease in frequency bandwidth to 180MHz compared with the current-feedback configuration.

Used as a building block, the OPA622 simplifies the design of complex analog signal processing stages in high-resolution video systems, communications equipment, and high-speed data acquisition circuitry.



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Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

PDS-1131

SPECIFICATIONS

ELECTRICAL

AT V_{CC} = ±5VDC, R_{LOAD} = 100Ω, R_{SOURCE} = 50Ω, and T_A = +25°C unless otherwise specified.

DC-SPECIFICATION

PARAMETER	CONDITIONS	OPA622AP, AU MIN	OPA622AP, AU TYP	OPA622AP, AU MAX	UNITS
INPUT OFFSET VOLTAGE					
Initial			±0.5		mV
vs Temperature					µV/°C
vs Supply (tracking)	V_{CC} = ±4.5V to ±5.5V				dB
vs Supply (non-tracking)	V_{CC} = +4.5V to +5.5V				dB
vs Supply (non-tracking)	V_{CC} = −4.5V to −5.5V				dB
INPUT BIAS CURRENT					
Initial			2		µA
vs Temperature					nA/°C
vs Supply (tracking)	V_{CC} = ±4.5V to ±5.5V				nA/V
vs Supply (non-tracking)	V_{CC} = +4.5V to +5.5V				nA/V
vs Supply (non-tracking)	V_{CC} = −4.5V to 5.5V				nA/V
INPUT IMPEDANCE			2.7 || 1		MΩ || pF
INPUT NOISE					
Voltage Noise Density	f = 100kHz to 5MHz	14	15	16	nV/$\sqrt{Hz}$
Signal-to-Noise Ratio	S/N = 0.7/(Vn • $\sqrt{5MHz}$)		87		dB
RATED OUTPUT					
Voltage Output			±3.5		V
DC Current Output			70		mA
Output Impedance			0.3		Ω
POWER SUPPLY					
Rated Voltage			±5		VDC
Derated Performance		±4		±6	VDC
Quiescent Current	Useful Range		4...8		mA
Programmable 1 to 8mA					
Rejection Ratio					dB

AC-SPECIFICATION

PARAMETER	CONDITIONS	OPA622AP, AU MIN	OPA622AP, AU TYP	OPA622AP, AU MAX	UNITS
FREQUENCY DOMAIN					
Large Signal	V_O = 2.8Vp-p, Gain = +1V/V		230		MHz
Closed Loop Bandwidth	V_O = 2.8Vp-p, Gain = +2V/V		200		MHz
(−3dB)	V_O = 2.8Vp-p, Gain = +5V/V		185		MHz
	V_O = 2.8Vp-p, Gain = +10V/V		145		MHz
	V_O = 2.8Vp-p, Gain = −2V/V		220		MHz
SMALL SIGNAL BANDWIDTH	V_O = 0.2Vp-p, Gain = +2V/V		150		MHz
GROUP DELAY TIME			1500		ps
DIFFERENTIAL GAIN	f = 4.43MHz, V_O 1.4Vp-p		0.2		%
DIFFERENTIAL PHASE	f = 4.43MHz, V_O = 1.4Vp-p		0.05		Degrees
TIME DOMAIN					
Rise Time	Gain = +2V/V, 10% to 90%				
	C_1 = 2pF		2.2		ns
	C_1 = 22pF		2.5		ns
	C_1 = 47pF		3.1		ns
SLEW RATE	Gain = +2V/V, Rise Time = 2ns				
Positive	V_O = 6.2Vp-p		1600		V/µs
Negative	V_O = 6.2Vp-p		1400		V/µs

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage	±6V
Input Voltage[1]	±V_S to ±0.7V
Operating Temperature	−40°C to +85°C
Storage Temperature	−40°C to +125°C
Junction Temperature	+150°C
Lead Temperature (soldering, 10s)	+300°C

NOTE: (1) Inputs are internally diode-clamped to ±V_S.

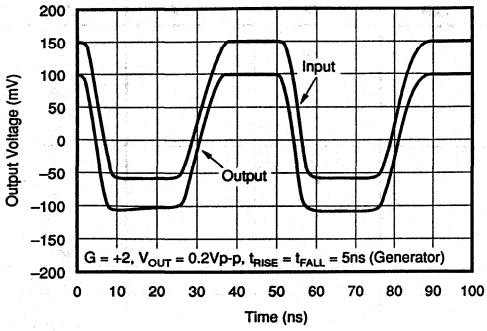
ORDERING INFORMATION

MODEL	DESCRIPTION	TEMPERATURE RANGE
OPA622AP	Plastic 14-Pin DIP	−40°C to +85°C
OPA622AU	SO-14 Surface-Mount	−40°C to +85°C

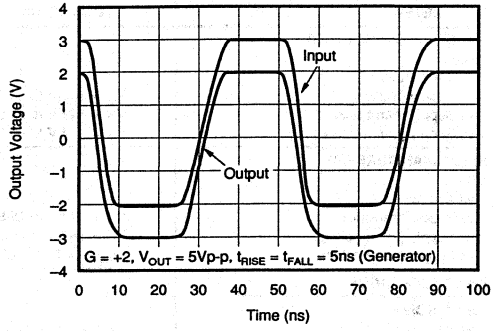
TYPICAL PERFORMANCE CURVES

I_O = 8mA, T_A = 25°C, V_{CC} = ±5VDC. R_L = 100Ω unless otherwise noted.

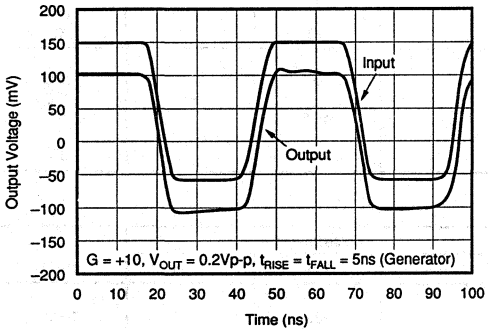
SMALL SIGNAL PULSE RESPONSE
VOLTAGE-FEEDBACK AMPLIFIER



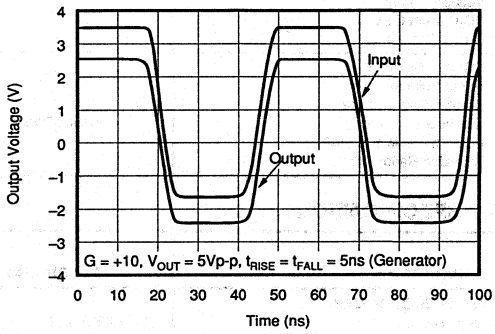
LARGE SIGNAL PULSE RESPONSE
VOLTAGE-FEEDBACK AMPLIFIER



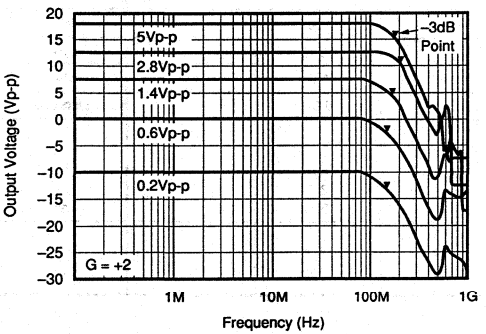
SMALL SIGNAL PULSE RESPONSE
VOLTAGE-FEEDBACK AMPLIFIER



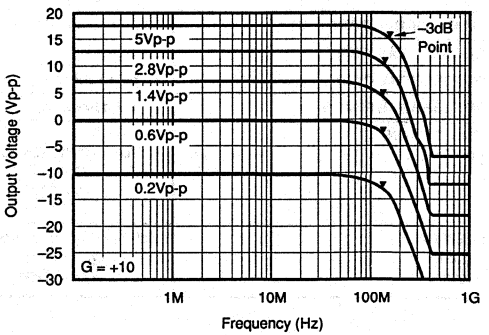
LARGE SIGNAL PULSE RESPONSE
VOLTAGE-FEEDBACK AMPLIFIER



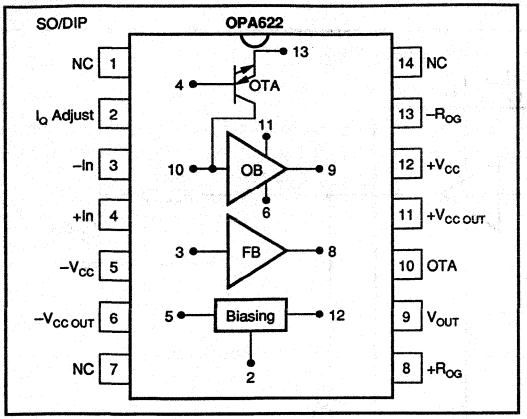
BANDWIDTH vs OUTPUT VOLTAGE
VOLTAGE-FEEDBACK AMPLIFIER



BANDWIDTH vs OUTPUT VOLTAGE
VOLTAGE-FEEDBACK AMPLIFIER



PIN CONFIGURATION



DISCUSSION OF PERFORMANCE

The OPA622 provides a level of full-power bandwidth previously unattainable in monolithic terms. In addition, the amplifier operates with reduced quiescent current and lower input bias current, which are very important factors in an increasingly complex electronic environment. The flexibility of the OPA622 design enables engineers to choose the speed advantages of a current-feedback amplifier or precision advantages such as two symmetrical inputs, low voltage offset, shorter settling times, and better CMMR of a voltage feedback amplifier. The programmable quiescent current feature also helps to adapt the amplifier to the particular design requirements.

VOLTAGE-FEEDBACK AMPLIFIER

The OPA622's design differs from a traditional "classical" operational amplifier structure, but it can nevertheless be used in all traditional operational amplifier applications. The "classical" differential input stage consists of two identical transistors with an emitter degeneration resistor, two current sources, and an active load diode. The classical configuration limits the current through the gain transistor to the current supplied by the current sources.

In the new design, a complementary push-pull buffer (emitter follower) replaces one side of the differential stage without the 0.7V V_{BE} offset. This buffer allows negative input signals without shutting off the input stage. A second complementary emitter follower and the open-loop gain resistor R_{OG} connected between the outputs recreate the differential stage without the disadvantages of the classical design. The current charging the parasitic capacitance on the base of the gain transistor is no longer limited to the fixed current of the current sources. This charging current is proportional to the input signal. This improvement results in a 10 times better slew rate.

The OPA622 is specified for the industrial temperature range (–40°C to +85°C) and is available in 14-pin plastic surface assembly or 14-pin plastic DIP.

The resistor R_{OG} sets the open-loop gain and corresponds to the emitter degeneration resistor in the classical differential stage already mentioned. Because the R_{OG} resistor can be varied, a flat frequency response can be achieved over a wide range of applications without the need to compensate the amplifier with a capacitor. In contrast to a current-feedback amplifier, it is possible to adjust the closed-loop gain using the feedback resistors or the open-loop gain using R_{OG} to optimize the frequency response.

The amplified current through the gain transistor of one of the buffers is mirrored and becomes the output current. The block consisting of the emitter follower and the current mirror can be viewed as an Operational Transconductance Amplifier—OTA. The high-impedance output of the OTA is now buffered by the high current output stage, which is designed for driving long cables or low-impedance loads at full power.

The two figures at the left on page 1 show the block diagram of a voltage-feedback configuration consisting of the described blocks (inverting and non-inverting.) Input offset is reduced to typically ±5µV using identical input buffers. Output offset is typically due to mismatch of the NPN and PNP transistors in the OTA mirror and the current output buffer ±500µV after trimming the output bias current.

CURRENT-FEEDBACK AMPLIFIER

The two figures at the right on page 1 show the current-feedback configuration. The feedback loop is now from the output to the emitter of the OTA section. The shorter feedback loop without the feedback buffer is the reason for the wider bandwidth of the current-feedback concept. The signal delay time through the buffer determines the difference between voltage and current feedback.

The specification data for offset voltage, CMMR, and settling time are the compromise parameters for the higher speed.

APPLICATIONS INFORMATION

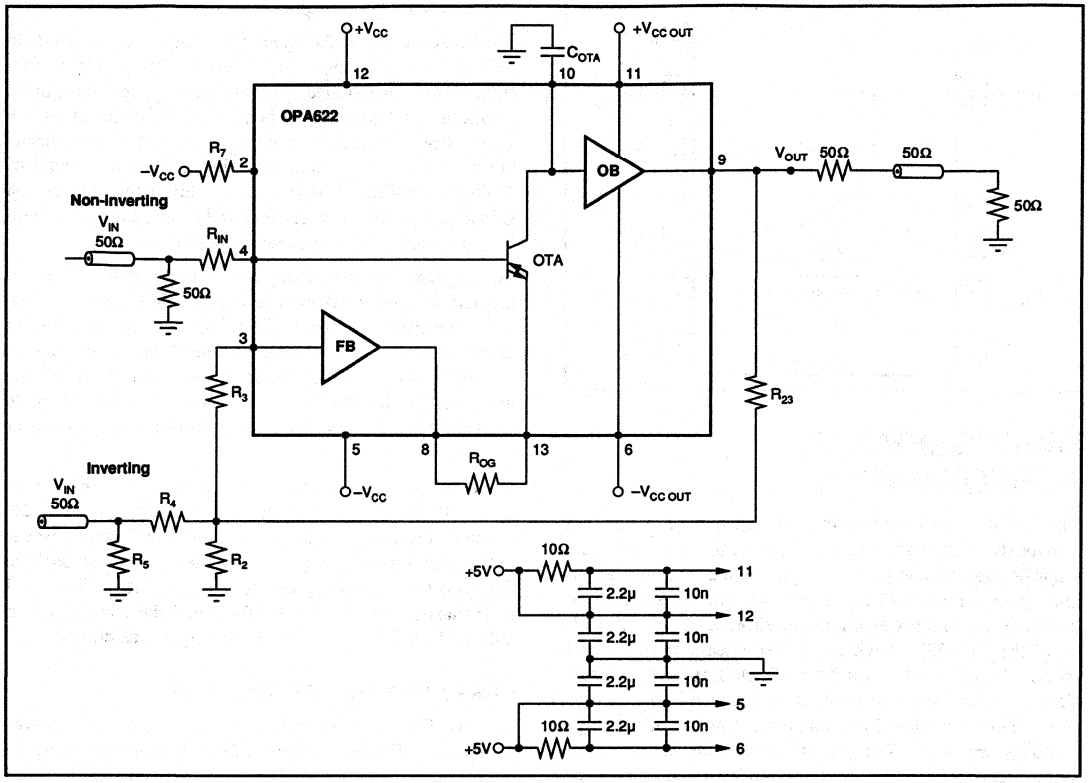


FIGURE 1. Voltage Feedback Amplifier.

OPA622AP	+1	+2	+5	+10	–1	–2	UNITS	OPA622AU	+1	+2	+5	+10	–1	–2	UNITS
R_{23}	0	300	330	390	270	270	Ω	R_{23}	200	270	300	180	180	240	Ω
R_2	∞	300	82	43			Ω	R_2	∞	270	75	20			Ω
R_3	300	0	0	0			Ω	R_3	0	0	0	0	0	0	Ω
R_{OG}	390	180	62	15	160	110	Ω	R_{OG}	330	160	39	4.7	150	110	Ω
C_{OTA}	15	1			1	1	pF	C_{OTA}	1.8	1.0	0.5	0.6	1.5	1.0	pF
R_{IN}	150	150	150	150	150	150	Ω	R_{IN}	150	150	150	150	150	150	Ω
R_4					270	130	Ω	R_4					180	120	Ω
R_5					56	68	Ω	R_5					68	82	Ω

TABLE 1. Recommended Components Values for Optimum Frequency Performance.

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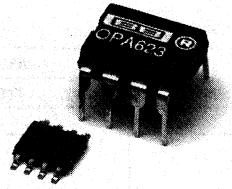


OPA623

ADVANCE INFORMATION
SUBJECT TO CHANGE

Wide Bandwidth, Current-Feedback OPERATIONAL AMPLIFIER

FEATURES

- SMALL/LARGE-SIGNAL BANDWIDTH: 280MHz
- HIGH OUTPUT CURRENT: ±70mA
- SLEW RATE: 2000V/µs, 5Vp-p
- DIFFERENTIAL GAIN: 0.05%
- DIFFERENTIAL PHASE: 0.05°
- LOW QUIESCENT CURRENT: ±4mA
- LOW INPUT BIAS CURRENT: 0.6µA

APPLICATIONS

- VIDEO EQUIPMENT
- COMMUNICATIONS
- PULSE/RF AMPLIFIER
- HIGH-SPEED ANALOG SIGNAL PROCESSING
- PHOTO MULTIPLIER TUBE PREAMPLIFIER

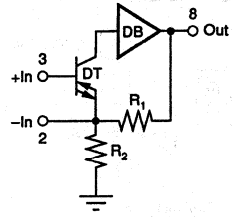
DESCRIPTION

The OPA623 is a common versatile building-block component designed for precision wide-bandwidth systems, including high-resolution video, RF and IF circuitry, and communications equipment. It includes a monolithic integrated current-feedback operational amplifier.

The new circuit design, together with the complementary bipolar process, achieves performance unattainable with monolithic integrated circuit technology.

The current-feedback amplifier is self-biased and bipolar. It provides a 280MHz large-signal bandwidth at ±2.5V output level as well as a 2000V/µs slew rate. The output buffer stage can deliver ±70mA output current. The high output current capability allows the OPA623 to drive 50Ω and 75Ω lines with ±3V output swing, making it ideal along with the low differential gain/phase errors for RF, IF, and video applications.

Used as a building block, the OPA623 simplifies the design of complex analog signal processing stages in high-resolution video systems, communications equipment, and high-speed data acquisition circuitry. The OPA623 is specified for the industrial temperature range (–40°C to +85°C) and is available in 8-pin plastic surface assembly, 8-pin plastic DIP.



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SPECIFICATIONS

ELECTRICAL

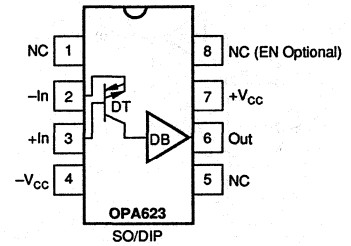
At V_{CC} = ±5VDC, R_{LOAD} = 100Ω, R_{SOURCE} = 50Ω, and T_A = +25°C unless otherwise noted.

PARAMETER	CONDITIONS	OPA623AP			OPA623AU			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
INPUT OFFSET VOLTAGE								
Initial			2			*		mV
vs Temperature								µV/°C
vs Supply (tracking)	V_{CC} = ±4.5V to ±5.5V							dB
vs Supply (non-tracking)	V_{CC} = +4.5V to +5.5V							dB
vs Supply (non-tracking)	V_{CC} = −4.5V to −5.5V							dB
INPUT BIAS CURRENT								
Initial			0.6			*		µA
vs Temperature								nA/°C
vs Supply (tracking)	V_{CC} = ±4.5V to ±5.5V							nA/V
vs Supply (non-tracking)	V_{CC} = +4.5V to +5.5V							nA/V
vs Supply (non-tracking)	V_{CC} = −4.5V to −5.5V							nA/V
INPUT IMPEDANCE			1.0 || 2.1			*		MΩ || pF
INPUT NOISE								
Voltage Noise Density	f = 100kHz to 100MHz		10			*		$nV/\sqrt{Hz}$
Signal to Noise Ratio	S/N = 0.7/(Vn • $\sqrt{5MHz}$)							dB
RATED OUTPUT								
Voltage Output			±3.3			*		V
DC Current Output			±70			*		mA
POWER SUPPLY								
Rated Voltage			±5			*		VDC
Derated Performance		±4.5		±5.5	*		*	VDC
Quiescent Current			4			*		mA
FREQUENCY DOMAIN								
Large Signal	V_O = 2.8Vp-p, Gain = +1V/V		380			*		MHz
Closed Loop Bandwidth	V_O = 2.8Vp-p, Gain = +2V/V		360			*		MHz
	V_O = 2.8Vp-p, Gain = +10V/V		170			*		MHz
	V_O = 2.8Vp-p, Gain = +20V/V		90			*		
SMALL SIGNAL BANDWIDTH	V_O = 0.2Vp-p, Gain = +2V/V		240			*		MHz
DIFFERENTIAL GAIN	f = 4.43MHz, V_O = 0.7Vp-p		0.05			*		%
DIFFERENTIAL PHASE	f = 4.43MHz, V_O = 0.7Vp-p		0.05			*		°
TIME DOMAIN								
Slew Rate	Gain = +2V/V, Rise Time = 2ns							
	V_O = 5.0Vp-p		2000			*		V/µs

*Specification same as OPA623AP.

PIN CONFIGURATION

Top View



ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage	±6V
Input Voltage[1]	$\pm V_S$ ±0.7V
Operating Temperature	−40°C to +85°C
Storage Temperature	−40°C to +125°C
Junction Temperature	+150°C
Lead Temperature (soldering, 10s)	+300°C

NOTE: (1) Inputs are internally diode-clamped to $\pm V_S$.

ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE
OPA623AP	Plastic 8-Pin DIP	−40°C to +85°C
OPA623AU	SO-8 Surface-Mount	−40°C to +85°C

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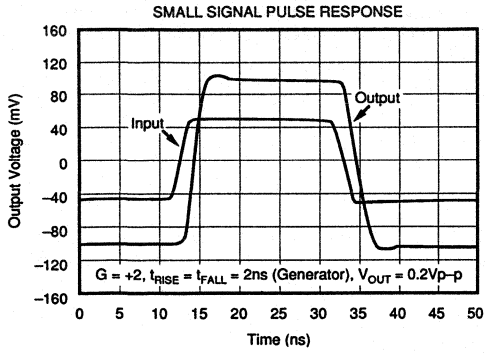
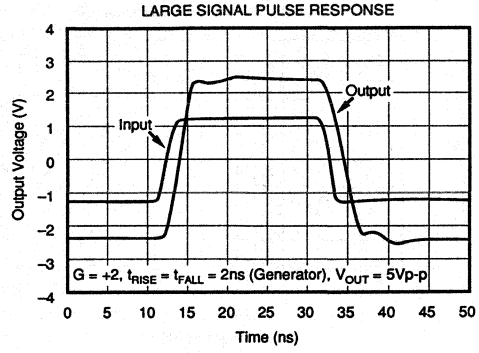
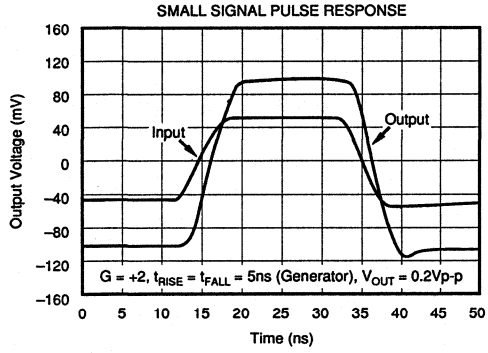
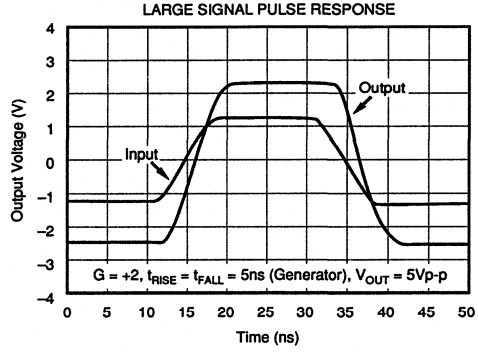
TYPICAL PERFORMANCE CURVES

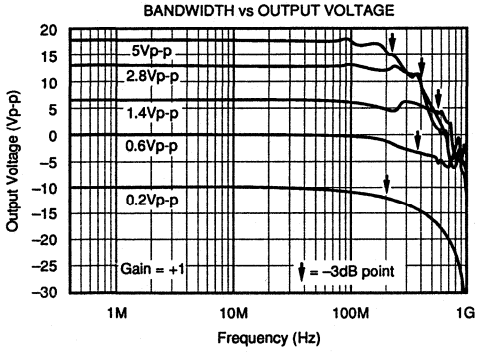
At V_{CC} = ±5VDC, R_{LOAD} = 100Ω, R_{SOURCE} = 50Ω, and T_A = +25°C unless otherwise noted.

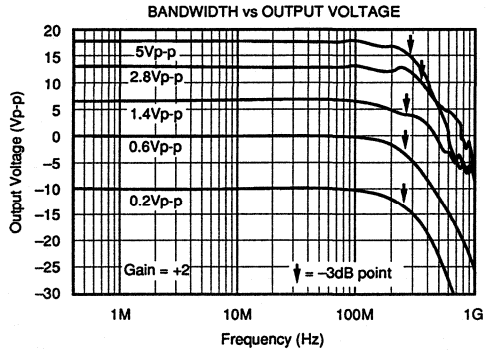








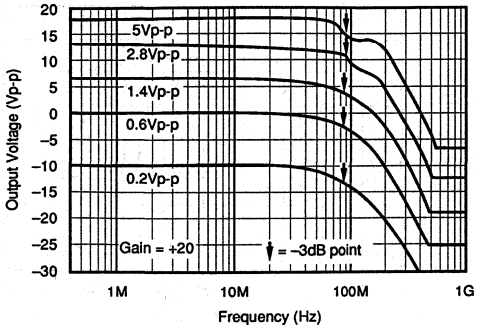




TYPICAL PERFORMANCE CURVES (CONT)

At V_{CC} = ±5VDC, R_{LOAD} = 100Ω, R_{SOURCE} = 50Ω, and T_A = +25°C unless otherwise noted.

BANDWIDTH vs OUTPUT VOLTAGE



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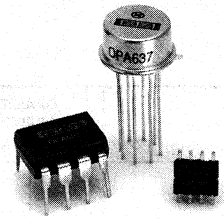


OPA627
OPA637

AVAILABLE IN DIE

Precision High-Speed *Difet*® OPERATIONAL AMPLIFIERS

FEATURES

- VERY LOW NOISE: 4.5nV/√Hz at 10kHz
- FAST SETTLING TIME:
  OPA627—550ns to 0.01%
  OPA637—450ns to 0.01%
- LOW V_{OS}: 100µV max
- LOW DRIFT: 0.8µV/°C max
- LOW I_B: 5pA max
- OPA627: Unity-Gain Stable
- OPA637: Stable in Gain ≥ 5

APPLICATIONS

- PRECISION INSTRUMENTATION
- FAST DATA ACQUISITION
- DAC OUTPUT AMPLIFIER
- OPTOELECTRONICS
- SONAR, ULTRASOUND
- HIGH-IMPEDANCE SENSOR AMPS
- HIGH-PERFORMANCE AUDIO CIRCUITRY
- ACTIVE FILTERS

DESCRIPTION

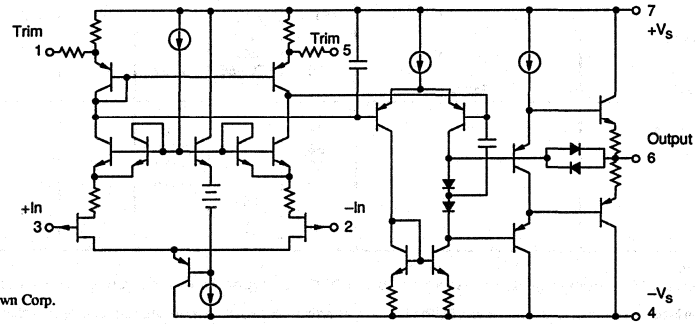
The OPA627 and OPA637 ***Difet*** operational amplifiers provide a new level of performance in a precision FET op amp. When compared to the popular OPA111 op amp, the OPA627/637 has lower noise, lower offset voltage, and much higher speed. It is useful in a broad range of precision and high speed analog circuitry.

The OPA627/637 is fabricated on a high-speed, dielectrically-isolated complementary NPN/PNP process. It operates over a wide range of power supply voltage—±4.5V to ±18V. Laser-trimmed ***Difet*** input circuitry provides high accuracy and low-noise performance comparable with the best bipolar-input op amps.

High frequency complementary transistors allow increased circuit bandwidth, attaining dynamic performance not possible with previous precision FET op amps. The OPA627 is unity-gain stable. The OPA637 is stable in gains equal to or greater than five.

Difet fabrication achieves extremely low input bias currents without compromising input voltage noise performance. Low input bias current is maintained over a wide input common-mode voltage range with unique cascode circuitry.

The OPA627/637 is available in plastic DIP, SOIC and metal TO-99 packages. Industrial and military temperature range models are available.



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SPECIFICATIONS

ELECTRICAL

T_A = +25°C, V_S = ±15V unless otherwise noted.

PARAMETER	CONDITIONS	OPA627BM/BP/SM OPA637BM/BP/SM MIN	TYP	MAX	OPA627AM/AP/AU OPA637AM/AP/AU MIN	TYP	MAX	UNITS
OFFSET VOLTAGE [1]								
Input Offset Voltage			40	100		130	250	µV
AP, BP, AU Grades			100	250		280	500	µV
Average Drift			0.4	0.8		1.2	2	µV/°C
AP, BP, AU Grades			0.8	2		2.5		µV/°C
Power Supply Rejection	V_S = ±4.5 to ±18V	106	120		100	116		dB
INPUT BIAS CURRENT [2]								
Input Bias Current	V_{CM} = 0V		1	5		2	10	pA
Over Specified Temperature	V_{CM} = 0V			1			2	nA
SM Grade	V_{CM} = 0V			50				nA
Over Common-Mode Voltage	V_{CM} = ±10V		1			2		pA
Input Offset Current	V_{CM} = 0V		0.5	5		1	10	pA
Over Specified Temperature	V_{CM} = 0V			1			2	nA
SM Grade				50				nA
NOISE								
Input Voltage Noise								
Noise Density: f = 10Hz			15	40		20		nV/√Hz
f = 100Hz			8	20		10		nV/√Hz
f = 1kHz			5.2	8		5.6		nV/√Hz
f = 10kHz			4.5	6		4.8		nV/√Hz
Voltage Noise, BW = 0.1 to 10Hz			0.6	1.6		0.8		µVp-p
Input Bias Current Noise								
Noise Density, f = 1kHz			1.6	2.5		2.5		fA/√Hz
Current Noise, BW = 0.1 to 10Hz			30	60		48		fAp-p
INPUT IMPEDANCE								
Differential			10^{13} || 8			*		Ω || pF
Common-Mode			10^{13} || 7			*		Ω || pF
INPUT VOLTAGE RANGE								
Common-Mode Input Range		±11	±11.5		*	*		V
Over Specified Temperature		±10.5	±11		*	*		V
Common-Mode Rejection	V_{CM} = ±10.5V	106	116		100	110		dB
OPEN-LOOP GAIN								
Open-Loop Voltage Gain	V_O = ±10V, R_L = 1kΩ	112	120		106	116		dB
Over Specified Temperature	V_O = ±10V, R_L = 1kΩ	106	117		100	110		dB
SM Grade	V_O = ±10V, R_L = 1kΩ	100	114					dB
FREQUENCY RESPONSE								
Slew Rate: OPA627	G = –1, 10V Step	40	55		*	*		V/µs
OPA637	G = –4, 10V Step	100	135		*	*		V/µs
Settling Time: OPA627 0.01%	G = –1, 10V Step		550			*		ns
0.1%	G = –1, 10V Step		450			*		ns
OPA637 0.01%	G = –4, 10V Step		450			*		ns
0.1%	G = –4, 10V Step		300			*		ns
Gain-Bandwidth Product: OPA627	G = 1		16			*		MHz
OPA637	G = 10		80			*		MHz
Total Harmonic Distortion + Noise	G = +1, f = 1kHz		0.00003			*		%
POWER SUPPLY								
Specified Operating Voltage			±15			*		V
Operating Voltage Range		±4.5		±18	*		*	V
Current			±7	±7.5		*	*	mA
OUTPUT								
Voltage Output	R_L = 1kΩ	±11.5	±12.3		*	*		
Over Specified Temperature		±11	±11.5		*	*		V
Current Output	V_O = ±10V		±45			*		mA
Short Circuit Current		±35	+70/–55	±100	*	*	*	mA
Output Impedance, Open-Loop	1MHz		55			*		Ω
TEMPERATURE RANGE								
Specification: AP, BP, AM, BM, AU		–25		+85	*		*	°C
SM		–55		+125				°C
Storage: AM, BM, SM		–60		+150	*		*	°C
AP, BP, AU		–40		+125	*		*	°C
θ_{JA}: AM, BM, SM			200			*		°C/W
AP, BP			100			*		°C/W
AU			160					°C/W

* Specifications same as "B" grade.

NOTES: (1) Offset voltage measured fully warmed-up. (2) High-speed test at T_J = 25°C. See Typical Performance Curves for warmed-up performance.

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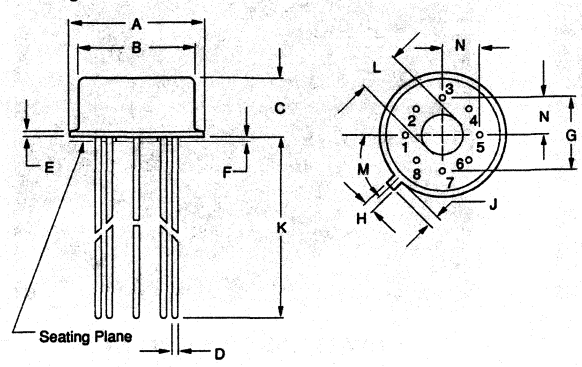
MECHANICAL

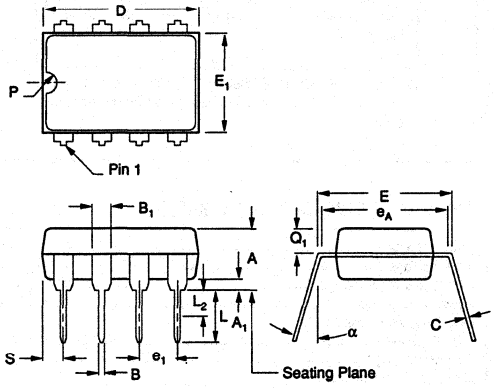
M Package — Metal TO-99



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.335	.370	8.51	9.40
B	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.200 BASIC		5.08 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500	—	12.7	—
L	.110	.160	2.79	4.06
M	45° BASIC		45° BASIC	
N	.095	.105	2.41	2.67

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.

P Package — 8-Pin Plastic DIP



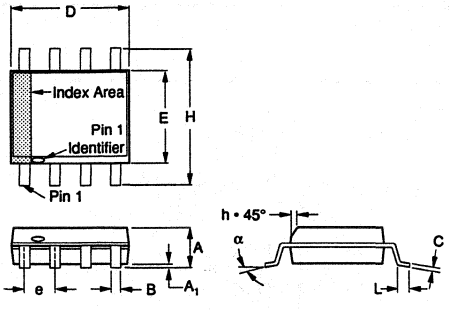
DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.155	.200	3.94	5.08
A1	.020	.050	0.51	1.27
B	.014	.020	0.36	0.51
B1	.045	.065	1.14	1.65
C	.008	.012	0.20	0.30
D (1)	.370	.400	9.40	10.16
E	.300	.325	7.62	8.26
E1	.240	.260	6.10	6.60
e1	.100 BASIC		2.54 BASIC	
eA	.300 BASIC		7.62 BASIC	
L	.125	.150	3.18	3.81

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
L2(2)	0	.030	0.00	0.76
α	0°	15°	0°	15°
P	.015	.050	0.38	1.270
Q1	.040	.075	1.02	1.91
S (1)	.015	.050	0.38	1.27

(1) Not JEDEC Std.
(2) e1 and e_A applies in zone L_2 when unit installed.

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

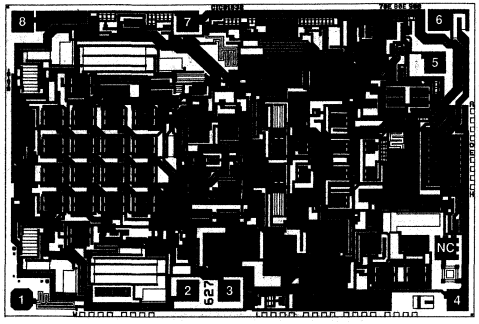
U Package — 8-Pin SO-8 Surface Mount



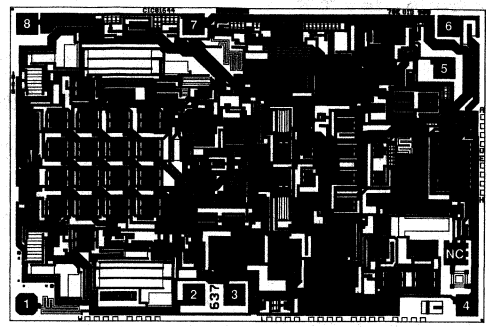
DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.054	.068	1.37	1.73
A1	.004	.009	0.10	0.23
B	.014	.019	0.36	0.48
C	.008	.0098	0.20	0.25
D	.189	.196	4.80	4.98
E	.150	.157	3.81	3.99
e	.050 BASIC		1.27 BASIC	
H	.229	.244	5.82	6.20
h	.010	.019	0.25	0.48
L	.016	.050	0.41	1.27
N	8		8	
α	0°	8°	0°	8°

NOTES:
1. Dimensioning and tolerancing per ANSI Y14.5M–1982.
2. "D" and "E" are reference datums and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm (.086 in.)
3. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the cross-hatched area.
4. "L" is the length of the terminal for soldering to a substrate.
5. "N" is the number of terminal positions.

DICE INFORMATION



OPA627 DIE TOPOGRAPHY



OPA637 DIE TOPOGRAPHY

PAD	FUNCTION	PAD	FUNCTION
1	Offset Trim	5	Offset Trim
2	–In	6	Output
3	+In	7	$+V_S$
4	$-V_S$	8	Substrate
		NC	No Connection

Substrate Bias: Dielectrically isolated. See data sheet for connection options.

MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	117 x 80 ±5	2.97 x 2.03 ±0.13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.10 x 0.10
Backing:	None	

See "DICE PRODUCTS" Section 17 in Data Book Supplement Volume 33c, or contact Burr-Brown for current information.

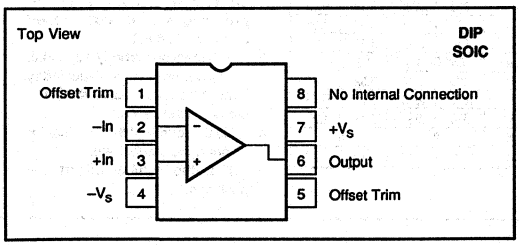
ORDERING INFORMATION

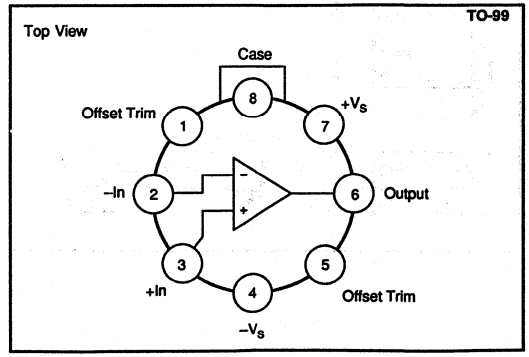
MODEL	PACKAGE	TEMPERATURE RANGE
OPA627AP	Plastic DIP	–25°C to +85°C
OPA627BP	Plastic DIP	–25°C to +85°C
OPA627AU	SOIC	–25°C to +85°C
OPA627AM	TO-99 Metal	–25°C to +85°C
OPA627BM	TO-99 Metal	–25°C to +85°C
OPA627SM	TO-99 Metal	–55°C to +125°C
OPA637AP	Plastic DIP	–25°C to +85°C
OPA637BP	Plastic DIP	–25°C to +85°C
OPA637AU	SOIC	–25°C to +85°C
OPA637AM	TO-99 Metal	–25°C to +85°C
OPA637BM	TO-99 Metal	–25°C to +85°C
OPA637SM	TO-99 Metal	–55°C to +125°C

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18V
Input Voltage Range	$+V_S$ + 2V to $-V_S$ – 2V
Differential Input Range	Total V_S + 4V
Power Dissipation	1000mW
Operating Temperature	
M Package	–55°C to +125°C
P, U Package	–40°C to +125°C
Storage Temperature	
M Package	–65°C to +150°C
P, U Package	–40°C to +125°C
Junction Temperature	
M Package	+175°C
P, U Package	+150°C
Lead Temperature (soldering, 10s)	+300°C

PIN CONFIGURATIONS

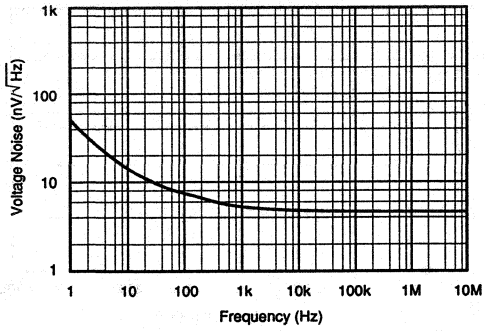




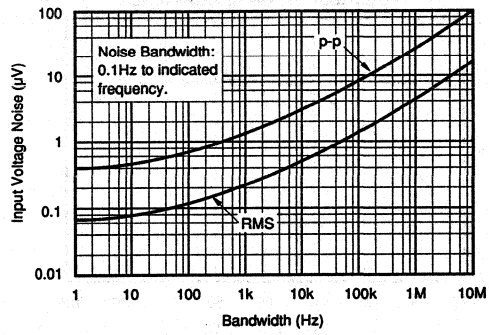
TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_S = ±15V unless otherwise noted.

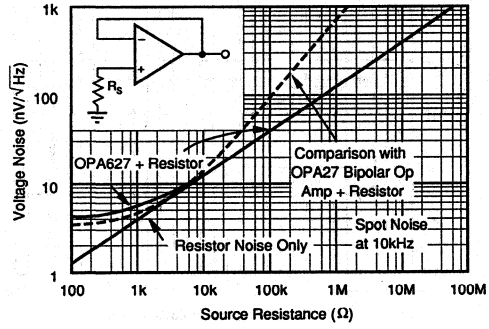
INPUT VOLTAGE NOISE SPECTRAL DENSITY



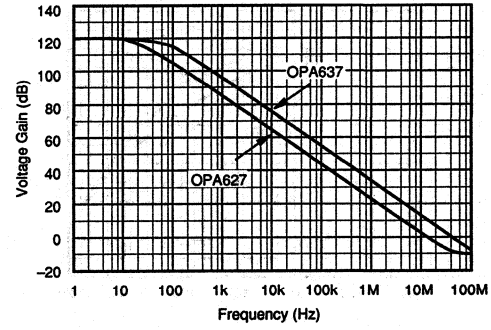
TOTAL INPUT VOLTAGE NOISE vs BANDWIDTH



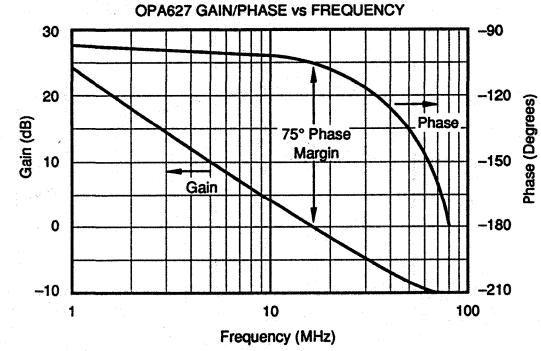
VOLTAGE NOISE vs SOURCE RESISTANCE



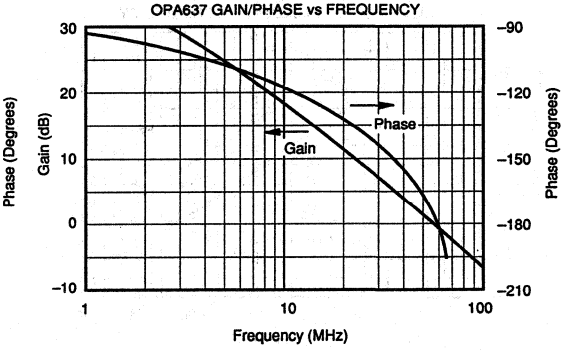
OPEN LOOP GAIN vs FREQUENCY



OPA627 GAIN/PHASE vs FREQUENCY



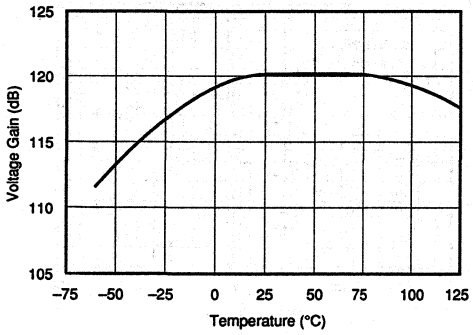
OPA637 GAIN/PHASE vs FREQUENCY



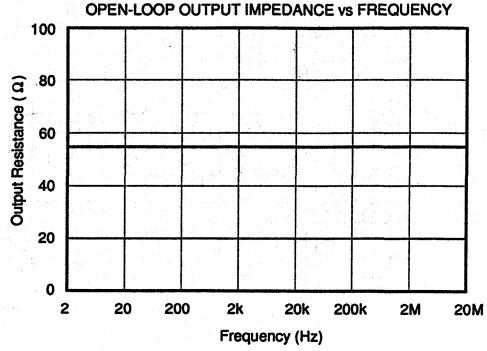
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_S = ±15V unless otherwise noted.

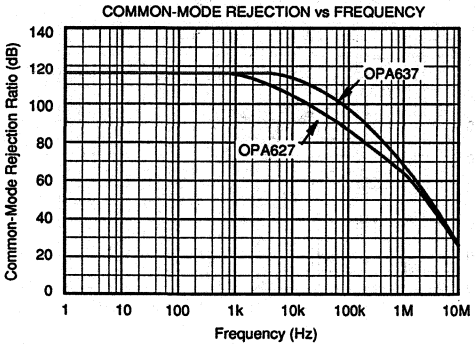
OPEN-LOOP GAIN vs TEMPERATURE



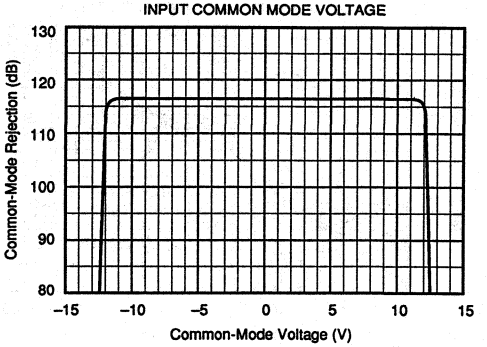
OPEN-LOOP OUTPUT IMPEDANCE vs FREQUENCY



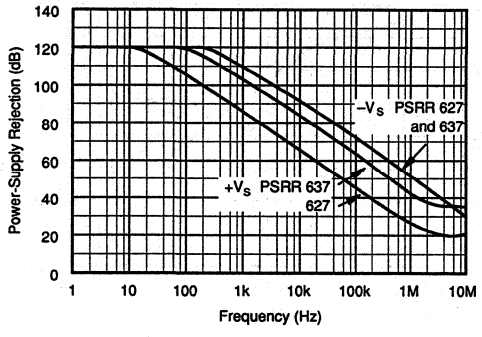
COMMON-MODE REJECTION vs FREQUENCY



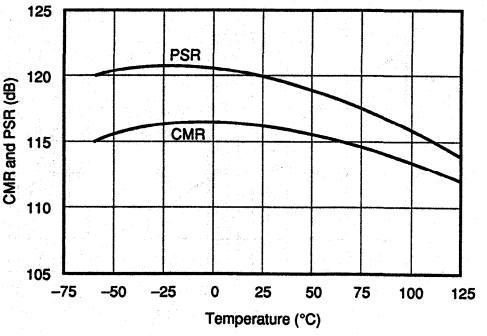
COMMON-MODE REJECTION vs INPUT COMMON MODE VOLTAGE



POWER-SUPPLY REJECTION vs FREQUENCY



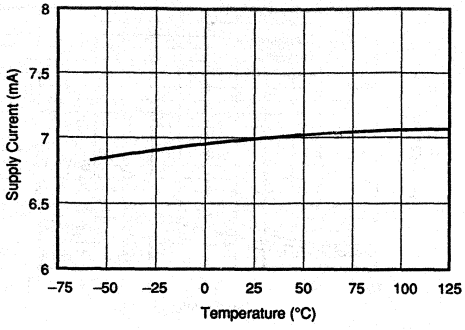
POWER-SUPPLY REJECTION AND COMMON-MODE REJECTION vs TEMPERATURE



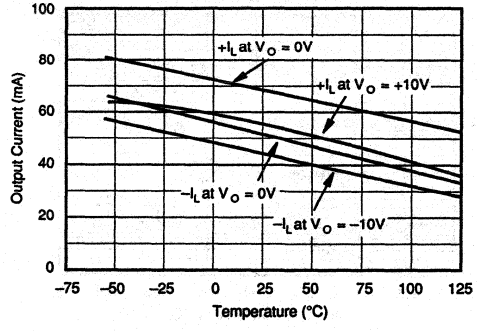
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_S = ±15V unless otherwise noted.

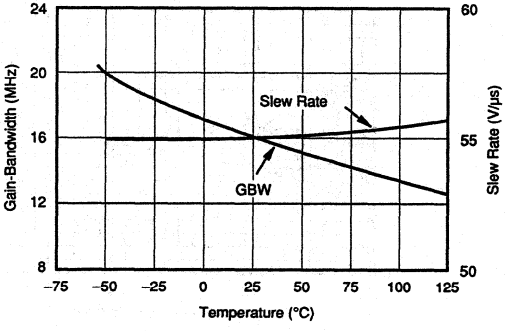
SUPPLY CURRENT vs TEMPERATURE



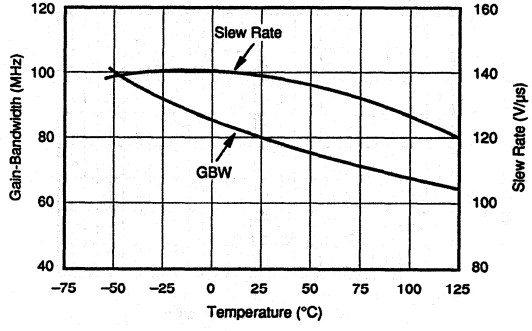
OUTPUT CURRENT LIMIT vs TEMPERATURE



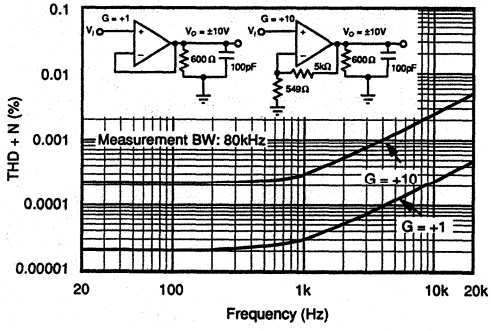
OPA627 GAIN-BANDWIDTH AND SLEW RATE vs TEMPERATURE



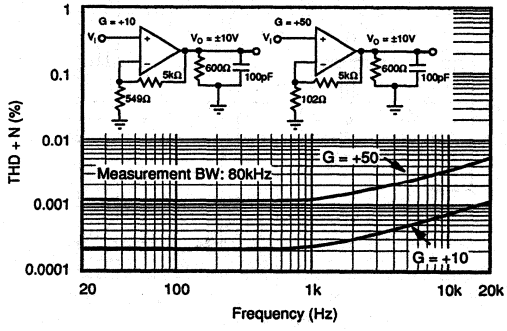
OPA637 GAIN-BANDWIDTH AND SLEW RATE vs TEMPERATURE



OPA627 TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY



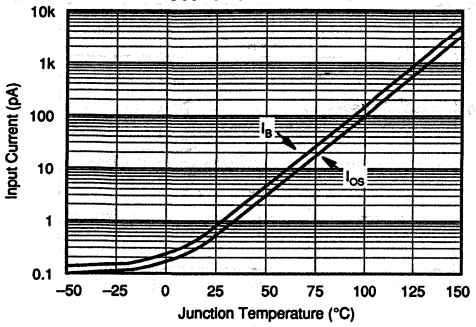
OPA637 TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY



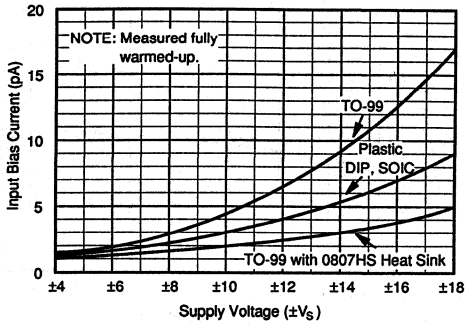
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_S = ±15V unless otherwise noted.

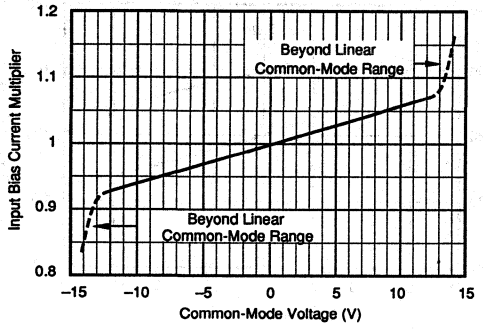
INPUT BIAS AND OFFSET CURRENT vs JUNCTION TEMPERATURE



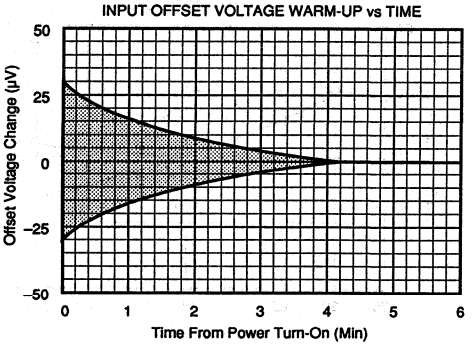
INPUT BIAS CURRENT vs POWER SUPPLY VOLTAGE



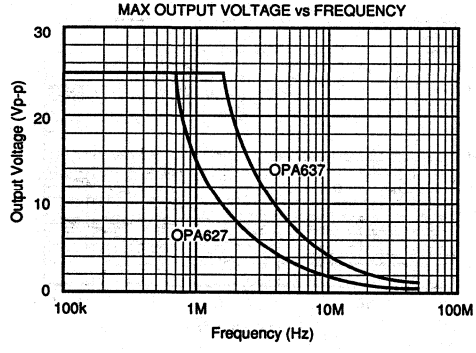
INPUT BIAS CURRENT vs COMMON-MODE VOLTAGE



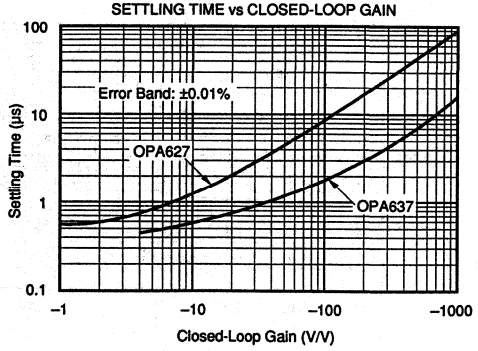
INPUT OFFSET VOLTAGE WARM-UP vs TIME



MAX OUTPUT VOLTAGE vs FREQUENCY

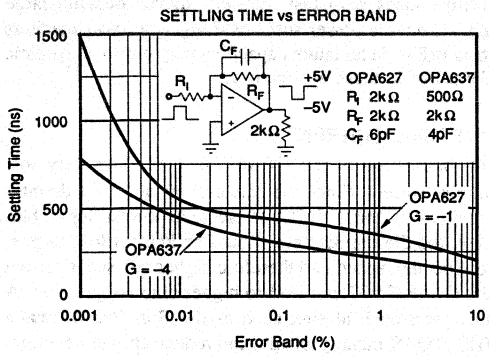


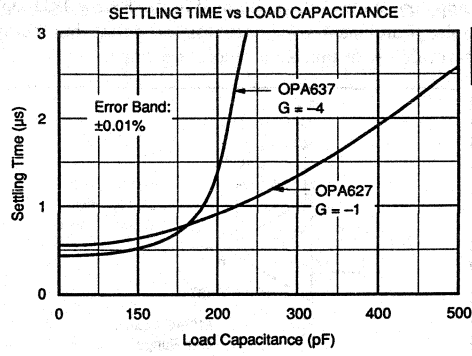
SETTLING TIME vs CLOSED-LOOP GAIN



TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_S = ±15V unless otherwise noted.





APPLICATIONS INFORMATION

The OPA627 is unity-gain stable. The OPA637 may be used to achieve higher speed and bandwidth in circuits with noise gain greater than five. Noise gain refers to the closed-loop gain of a circuit as if the non-inverting op amp input were being driven. For example, the OPA637 may be used in a non-inverting amplifier with gain greater than five, or an inverting amplifier of gain greater than four.

When choosing between the OPA627 or OPA637, it is important to consider the high frequency noise gain of your circuit configuration. Circuits with a feedback capacitor (Figure 1) place the op amp in unity noise-gain at high frequency. These applications must use the OPA627 for proper stability. An exception is the circuit in Figure 2, where a small feedback capacitance is used to compensate for the input capacitance at the op amp's inverting input. In this case, the closed-loop noise gain remains constant with frequency, so if the closed-loop gain is equal to five or greater, the OPA637 may be used.

OFFSET VOLTAGE ADJUSTMENT

The OPA627/637 is laser-trimmed for low offset voltage and drift, so many circuits will not require external adjustment. Figure 3 shows the optional connection of an external potentiometer to adjust offset voltage. This adjustment should not be used to compensate for offsets created elsewhere in a system (such as in later amplification stages or in an A/D converter) because this could introduce excessive temperature drift.

NOISE PERFORMANCE

Some bipolar op amps may provide lower voltage noise performance, but both voltage noise and bias current noise contribute to the total noise of a system. The OPA627/637 is unique in providing very low voltage noise and very low

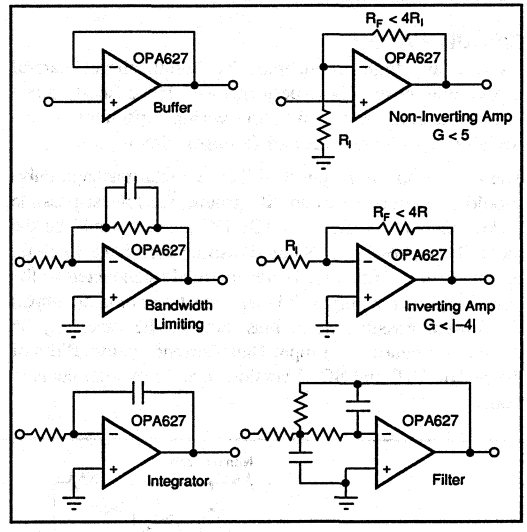


FIGURE 1. Circuits with Noise Gain Less than Five Require the OPA627 for Proper Stability.

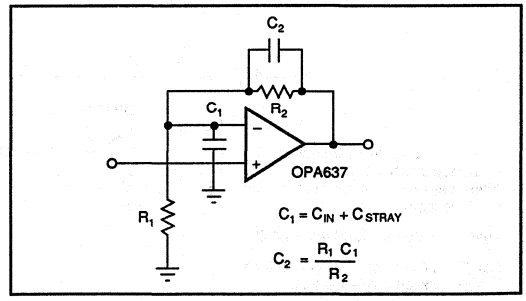


FIGURE 2. Circuits with Noise Gain Equal to or Greater than Five May Use the OPA637.

current noise. This provides optimum noise performance over a wide range of sources, including reactive source impedances. This can be seen in the performance curve showing the noise of a source resistor combined with the noise of an OPA627. Above a 2kΩ source resistance, the op amp contributes little additional noise. Below 1kΩ, op amp noise dominates over the resistor noise, but compares favorably with precision bipolar op amps.

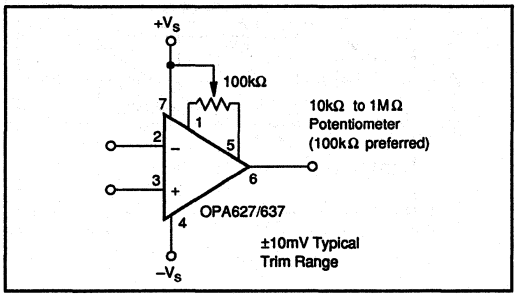


FIGURE 3. Optional Offset Voltage Trim Circuit.

CIRCUIT LAYOUT

As with any high speed, wide bandwidth circuit, careful layout will ensure best performance. Make short, direct interconnections and avoid stray wiring capacitance— especially at the input pins and feedback circuitry.

The case connection (pin 8 of TO-99 metal package only) should be connected to an AC ground for lowest possible pickup of external fields. While DC ground would be the most likely choice, pin 8 could also be connected to either power supply. (The case is not internally connected to the negative power supply as it is with most common op amps.) For lowest possible input bias current, the case may be driven as a guard—see Input Bias Current section. Pin 8 of the plastic DIP and SOIC versions has no internal connection.

Power supply connections should be bypassed with good high frequency capacitors positioned close to the op amp pins. In most cases 0.1µF ceramic capacitors are adequate. The OPA627/637 is capable of high output current (in excess of 45mA). Applications with low impedance loads or capacitive loads with fast transient signals demand large currents from the power supplies. Larger bypass capacitors such as 1µF solid tantalum capacitors may improve dynamic performance in these applications.

INPUT BIAS CURRENT

Difet fabrication of the OPA627/637 provides very low input bias current. Since the gate current of a FET doubles approximately every 10°C, to achieve lowest input bias current, the die temperature should be kept as low as possible. The high speed and therefore higher quiescent current of the OPA627/637 can lead to higher chip temperature. A simple press-on heat sink such as the Burr-Brown model 807HS (TO-99 metal package) can reduce chip temperature by approximately 15°C, lowering the I_B to one-third its warmed-up value. The 807HS heat sink can also reduce low-frequency voltage noise caused by air currents and thermoelectric effects. See the data sheet on the 807HS for details.

Temperature rise in the plastic DIP and SOIC packages can be minimized by soldering the device to the circuit board. Wide copper traces will also help dissipate heat.

The OPA627/637 may also be operated at reduced power supply voltage to minimize power dissipation and temperature rise. Using ±5V power supplies reduces power dissipation to one-third of that at ±15V. This reduces the I_B of TO-99 metal package devices to approximately one-fourth the value at ±15V.

Leakage currents between printed circuit board traces can easily exceed the input bias current of the OPA627/637. A circuit board "guard" pattern (Figure 4) reduces leakage effects. By surrounding critical high impedance input cir-

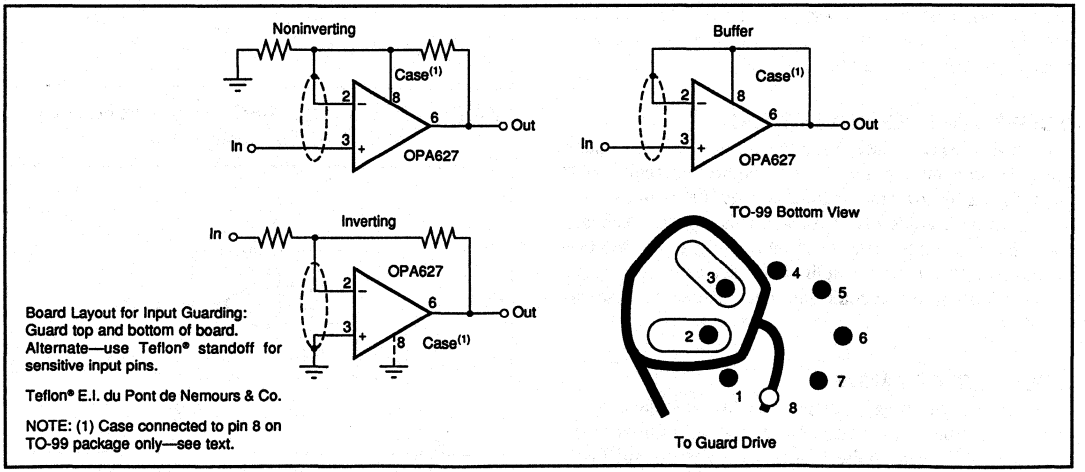


FIGURE 4. Connection of Input Guard for Lowest I_B.

cuitry with a low impedance circuit connection at the same potential, leakage current will flow harmlessly to the low-impedance node. The case connection (TO-99 metal package only) may also be driven at guard potential to minimize any leakage which might occur from the input pins to the case. The case is not internally connected to $-V_S$.

Input bias current may also be degraded by improper handling or cleaning. Contamination from handling parts and circuit boards may be removed with cleaning solvents and deionized water. Each rinsing operation should be followed by a 30-minute bake at 85°C.

Many FET-input op amps exhibit large changes in input bias current with changes in input voltage. Input stage cascode circuitry makes the input bias current of the OPA627/637 virtually constant with wide common-mode voltage changes. This is ideal for accurate high input-impedance buffer applications.

PHASE-REVERSAL PROTECTION

The OPA627/637 has internal phase-reversal protection. Many FET-input op amps exhibit a phase reversal when the input is driven beyond its linear common-mode range. This is most often encountered in non-inverting circuits when the input is driven below –12V, causing the output to reverse into the positive rail. The input circuitry of the OPA627/637 does not induce phase reversal with excessive common-mode voltage, so the output limits into the appropriate rail.

OUTPUT OVERLOAD

When the inputs to the OPA627/637 are overdriven, the output voltage of the OPA627/637 smoothly limits at approximately 2.5V from the positive and negative power supplies. If driven to the negative swing limit, recovery takes approximately 500ns. When the output is driven into the positive limit, recovery takes approximately 6µs. Output recovery of the OPA627 can be improved using the output clamp circuit shown in Figure 5. Diodes at the inverting input prevent degradation of input bias current.

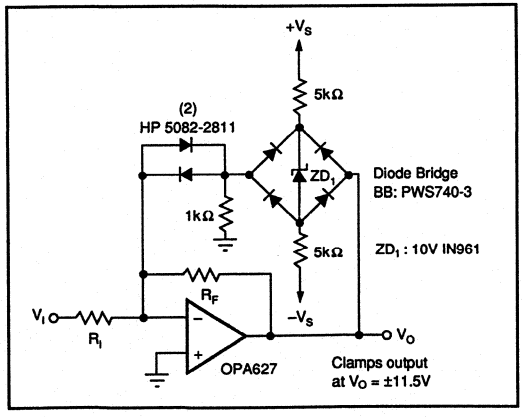


FIGURE 5. Clamp Circuit for Improved Overload Recovery.

CAPACITIVE LOADS

As with any high-speed op amp, best dynamic performance can be achieved by minimizing the capacitive load. Since a load capacitance presents a decreasing impedance at higher frequency, a load capacitance which is easily driven by a slow op amp can cause a high-speed op amp to perform poorly. See the typical curves showing settling times as a function of capacitive load. The lower bandwidth of the OPA627 makes it the better choice for driving large capacitive loads. Figure 6 shows a circuit for driving very large load capacitance. This circuit's two-pole response can also be used to sharply limit system bandwidth. This is often useful in reducing the noise of systems which do not require the full bandwidth of the OPA627.

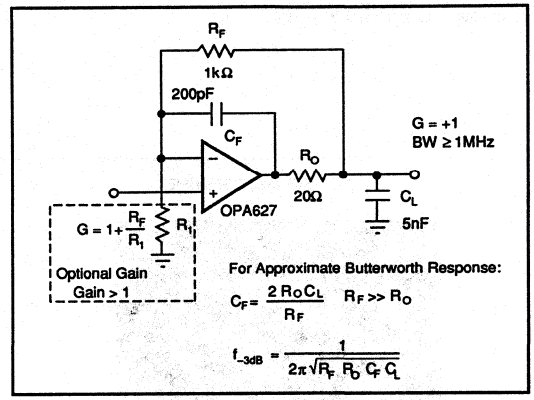


FIGURE 6. Driving Large Capacitive Loads.

INPUT PROTECTION

The inputs of the OPA627/637 are protected for voltages between $+V_S$ + 2V and $-V_S$ – 2V. If the input voltage can exceed these limits, the amplifier should be protected. The diode clamps shown in Figure 7a will prevent the input voltage from exceeding one forward diode voltage drop beyond the power supplies—well within the safe limits. If the input source can deliver current in excess of the maximum forward current of the protection diodes, use a series resistor, R_S, to limit the current. Be aware that adding resistance to the input will increase noise. The 4nV/√Hz theoretical thermal noise of a 1kΩ resistor will add to the 4.5nV/√Hz noise of the OPA627/637 (by the square-root of the sum of the squares), producing a total noise of 6nV/√Hz. Resistors below 100Ω add negligible noise.

Leakage current in the protection diodes can increase the total input bias current of the circuit. The specified maximum leakage current for commonly used diodes such as the 1N4148 is approximately 25nA—more than a thousand times larger than the input bias current of the OPA627/637. Leakage current of these diodes is typically much lower and may be adequate in many applications. Light falling on the junction of the protection diodes can dramatically increase leakage current, so common glass-packaged diodes should

be shielded from ambient light. Very low leakage can be achieved by using a diode-connected FET as shown. The 2N4117A is specified at 1pA and its metal case shields the junction from light.

Sometimes input protection is required on I/V converters of inverting amplifiers (Figure 7b). Although in normal operation, the voltage at the summing junction will be near zero (equal to the offset voltage of the amplifier), large input transients may cause this node to exceed 2V beyond the power supplies. In this case, the summing junction should be protected with diode clamps connected to ground. Even with the the low voltage present at the summing junction, common signal diodes may have excessive leakage current. Since the reverse voltage on these diodes is clamped, a diode-connected signal transistor can be used as an inexpensive low leakage diode (Figure 7b).

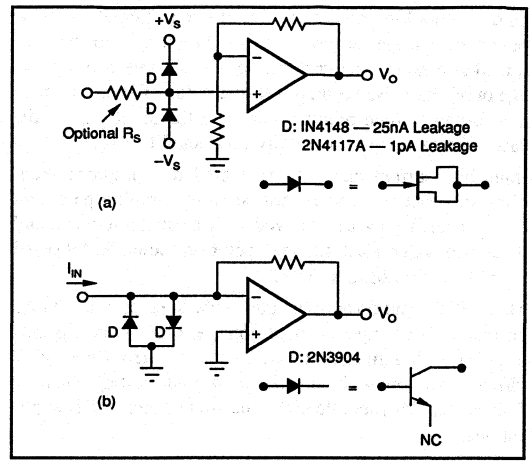


FIGURE 7. Input Protection Circuits.

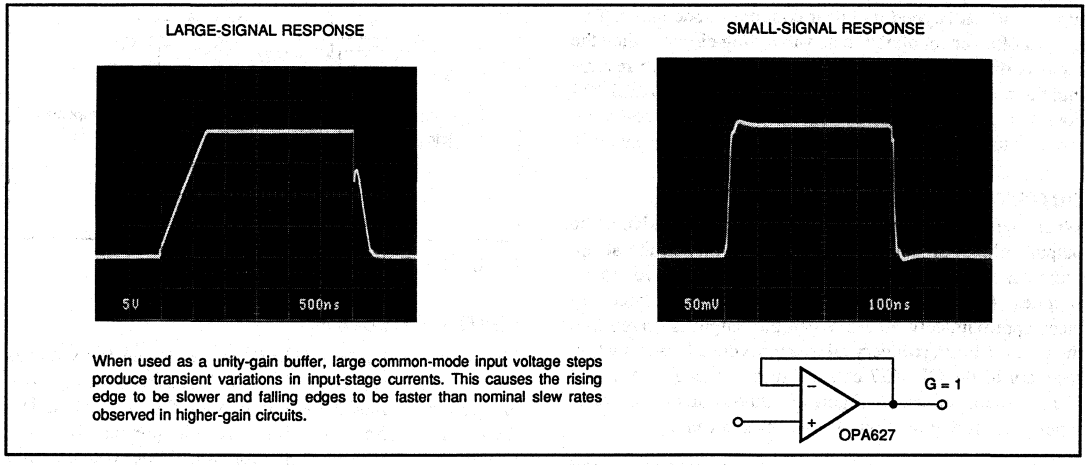


FIGURE 8. OPA627 Dynamic Performance, G = +1.

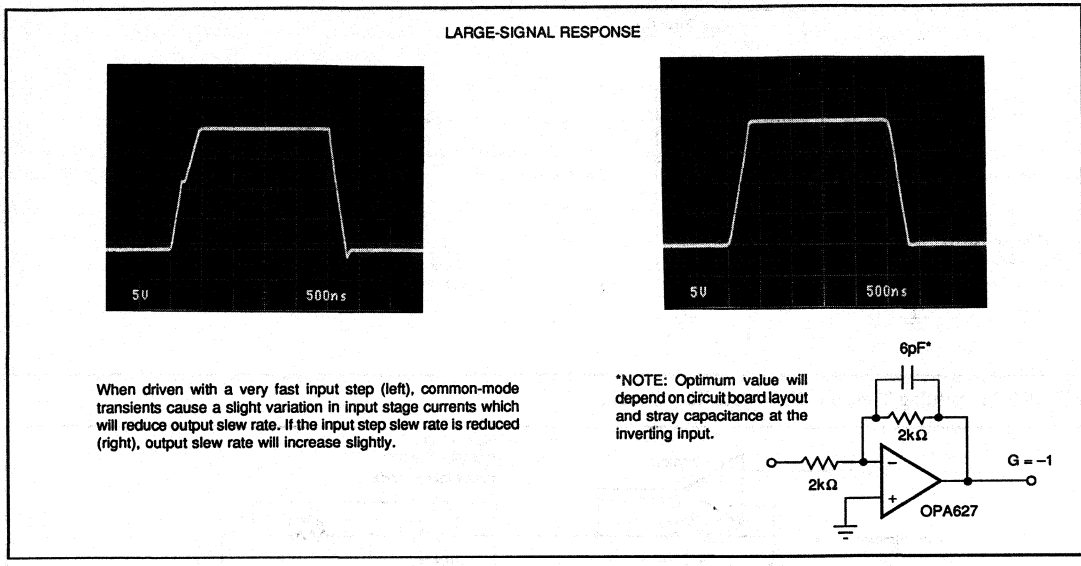


FIGURE 9. OPA627 Dynamic Performance, G = –1.

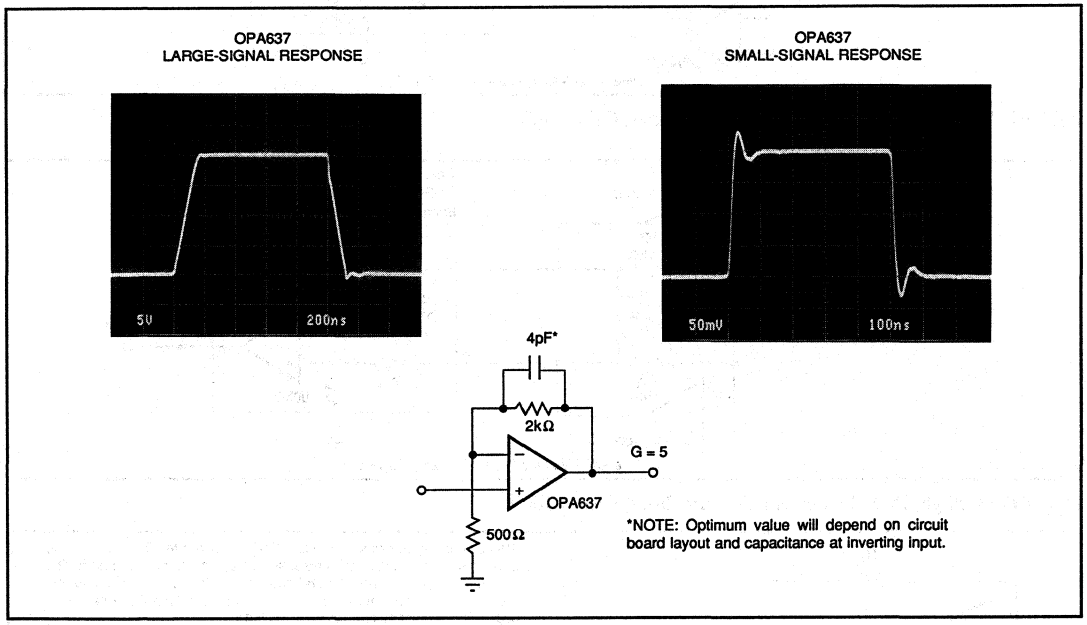
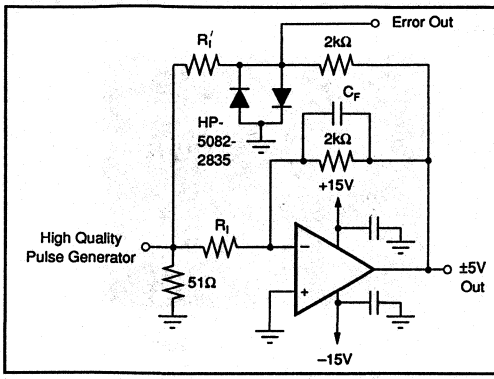


FIGURE 10. OPA637 Dynamic Response, G = 5.



	OPA627	OPA637
R_I, R_y	2kΩ	500Ω
C_F	6pF	4pF
Error Band (0.01%)	±0.5mV	±0.2mV

NOTE: C_F is selected for best settling time performance depending on test fixture layout. Once optimum value is determined, a fixed capacitor may be used.

FIGURE 11. Settling Time and Slew Rate Test Circuit.

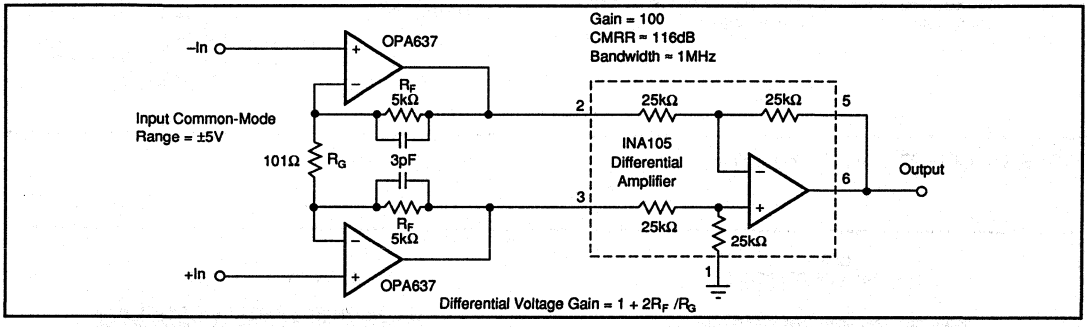


FIGURE 12. High Speed Instrumentation Amplifier, Gain = 100.

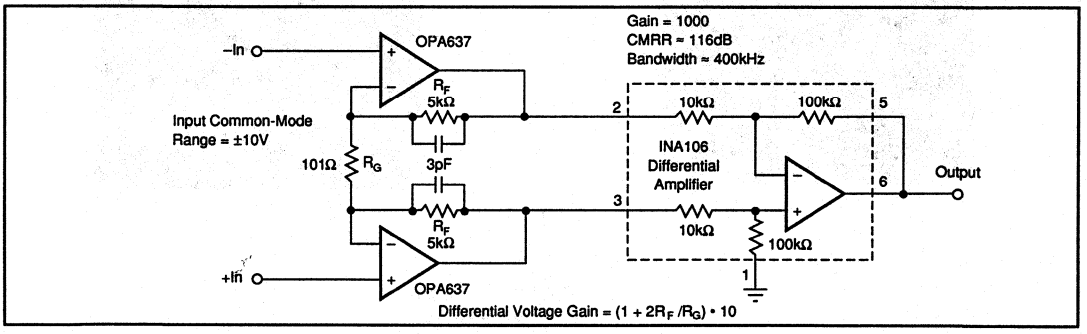
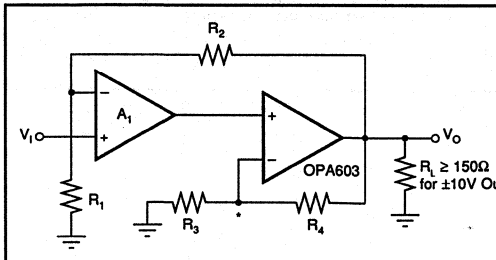


FIGURE 13. High Speed Instrumentation Amplifier, Gain = 1000.



This composite amplifier uses the OPA603 current-feedback op amp to provide extended bandwidth and slew rate at high closed-loop gain. The feedback loop is closed around the composite amp, preserving the precision input characteristics of the OPA627/637. Use separate power supply bypass capacitors for each op amp.

*Minimize capacitance at this node.

GAIN (V/V)	A_1 OP AMP	R_1 (Ω)	R_2 (kΩ)	R_3 (Ω)	R_4 (kΩ)	−3dB (MHz)	SLEW RATE (V/µs)
100	OPA627	50.5[1]	4.99	20	1	15	700
1000	OPA637	49.9	4.99	12	1	11	500

NOTE: (1) Closest 1/2% value.

FIGURE 14. Composite Amplifier for Wide Bandwidth.

BURR-BROWN®

OPA654

Wide Bandwidth, High Output Current *Difet*® OPERATIONAL AMPLIFIER

FEATURES

- HIGH SLEW RATE: 750V/µs
- HIGH OUTPUT CURRENT: 200mA
- WIDE GAIN-BANDWIDTH: 700MHz
- FAST SETTLING: 150ns to 0.1%
- FET INPUT: I_B = 50pA max

APPLICATIONS

- LINE DRIVERS
- PIN DRIVERS
- HIGH-SPEED DATA ACQUISITION
- WAVEFORM GENERATORS

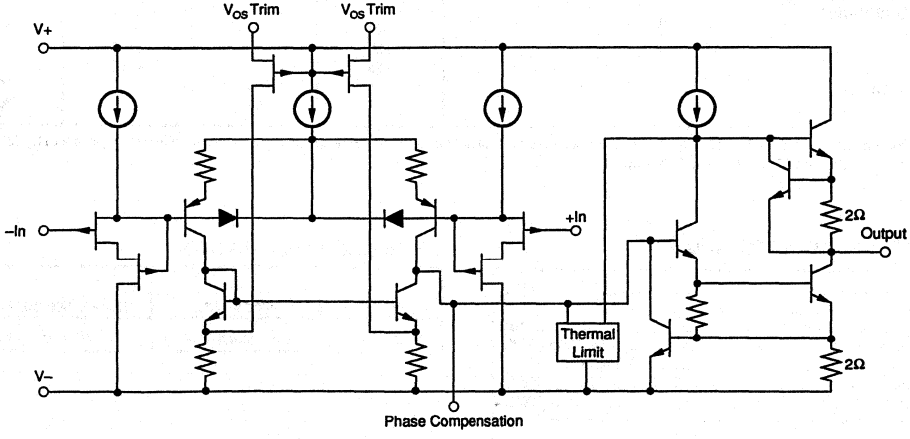
DESCRIPTION

The OPA654 is a high-speed monolithic operational amplifier featuring 200mA output current. Fabricated using Burr-Brown's Complementary-Bipolar, ***Difet*** process, it provides an excellent combination of high speed and high output current.

The OPA654 is versatile, operating from power supplies ranging from ±5V to ±18V. It can deliver up to ±10V signals into a 50Ω load at slew rates of 750V/µs. Its speed and output current make it useful for line driver and automatic test applications.

The OPA654 is externally compensated, allowing open-loop gain and phase characteristics to be optimized for the desired closed-loop gain, load and dynamic characteristics.

The OPA654 is available in an 8-pin metal TO-3 package that provides excellent thermal characteristics and is specified for the industrial temperature range.



Difet®, Burr-Brown Corp.

International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL

T_A = +25°C, V_S = ±15V unless otherwise noted.

PARAMETER	CONDITION	OPA654AM MIN	OPA654AM TYP	OPA654AM MAX	UNITS
OFFSET VOLTAGE					
Input Offset Voltage			±0.1	±3	mV
Average Drift			±40		µV/°C
Power Supply Rejection	V_S = ±5 to ±15V	72	82		dB
INPUT BIAS CURRENT(1)					
Input Bias Current	V_{CM} = 0V		3	50	pA
Input Offset Current	V_{CM} = 0V		2	25	pA
NOISE					
Input Voltage Noise					
Noise Density,	f = 10Hz		115		nV/√Hz
	f = 100Hz		37		nV/√Hz
	f = 1kHz		19		nV/√Hz
	f = 10kHz		14		nV/√Hz
Voltage Noise,	f_B = 10Hz to 1MHz		85		µVp-p
Input Bias Current Noise					
Current Noise Density, f = 0.1Hz to 20kHz			1		fA/√Hz
INPUT VOLTAGE RANGE					
Common-Mode Input Range		±12	±13		V
Common-Mode Rejection	V_{CM} = ±10V	70	76		dB
INPUT IMPEDANCE					
Differential			10^{12} || 2.5		Ω || pF
Common-Mode			10^{12} || 3.2		Ω || pF
OPEN-LOOP GAIN					
Open-Loop Voltage Gain	V_O = ±10V, R_L = 1kΩ		94		dB
	V_O = ±10V, R_L = 50Ω	80	82		dB
FREQUENCY RESPONSE					
Gain-Bandwidth Product (2)			See Typical Curve		
Slew Rate (2,3)	G = –1, 20V Step		750		V/µs
Settling Time (2) 0.01%	G = –1, 10V Step		240		ns
0.1%	G = –1, 10V Step		150		ns
1%	G = –1, 10V Step		85		ns
OUTPUT					
Voltage Output	R_L = 50Ω	±11	±12.3		V
Current Output	V_O = ±10V		200		mA
Short Circuit Current			325		mA
Output Resistance, Open-Loop	DC		800		Ω
POWER SUPPLY					
Specified Operating Voltage			±15		V
Operating Voltage Range		±5		±18	V
Quiescent Current			±38	±43	mA
TEMPERATURE RANGE					
Specification		–25		+85	°C
Operating		–55		+125	°C
Storage		–55		+150	°C
Thermal Resistance, θ_{JC}			15		°C/W
θ_{JA}			45		°C/W

NOTES: (1) High-speed test at T_J = 25°C. (2) Varies with external phase compensation, C_1. See typical curves for performance with other gains and C_1. (3) Slew rate is rate of change from 10% to 90% of output voltage step.

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage	±18V
Input Voltage	±V_S ±1V
Output Short Circuit (to ground)	10s
Operating Temperature	–40°C to +85°C
Storage Temperature	–40°C to +125°C
Junction Temperature	+165°C
Lead Temperature (soldering, 10s)	+300°C

ORDERING INFORMATION

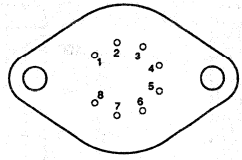
MODEL	PACKAGE	TEMPERATURE RANGE
OPA654AM	8-Pin Metal TO-3	–25°C to +85°C

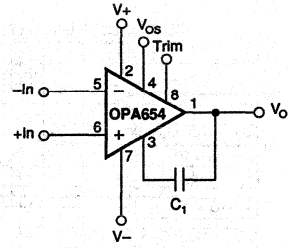
PIN CONFIGURATION

"M" TO-3 Metal Package

PIN LIST
1. V_O
2. V+
3. Compensation
4. V_{OS} Trim
5. –In
6. +In
7. V–
8. V_{OS} Trim

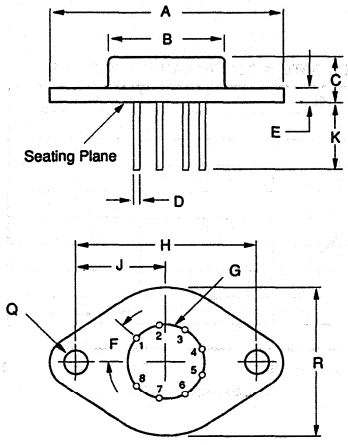
BOTTOM VIEW





Case is connected to IC substrate. Connect case to ground—see text.

M Package — 8-Pin Metal TO-3



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.510	1.550	38.35	39.37
B	.745	.770	18.92	19.56
C	.260	.340	6.60	8.64
D	.038	.042	0.97	1.07
E	.080	.105	2.03	2.67
F	40° BASIC		40° BASIC	
G	.500 BASIC		12.70 BASIC	
H	1.186 BASIC		30.12 BASIC	
J	.593 BASIC		15.06 BASIC	
K	.400	.500	10.16	12.70
Q	.151	.161	3.84	4.09
R	.980	1.020	24.89	25.91

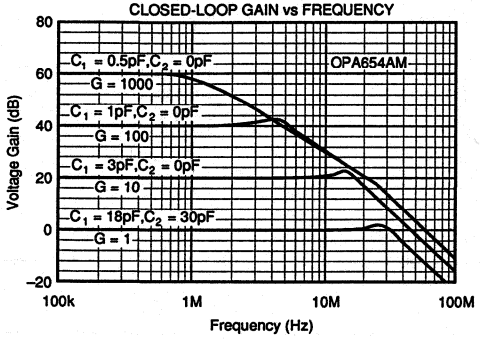
NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only.

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

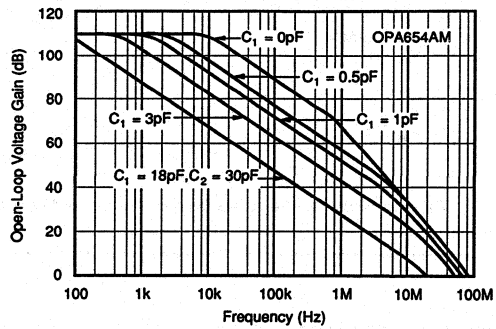
TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_S = ±15V unless otherwise noted.

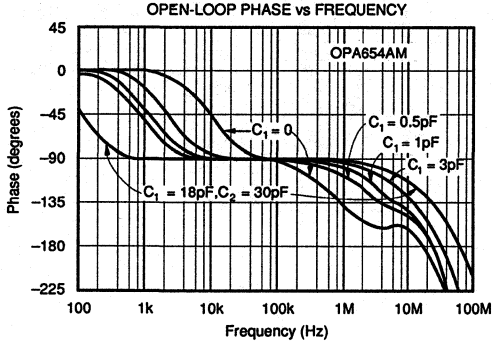
CLOSED-LOOP GAIN vs FREQUENCY



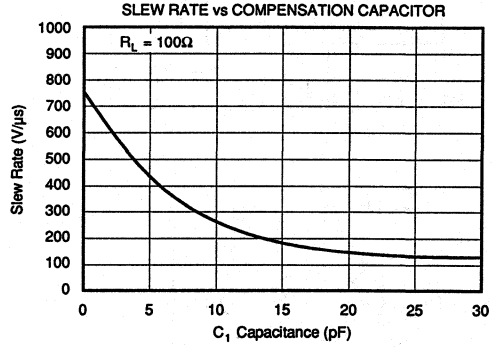
OPEN-LOOP GAIN vs FREQUENCY



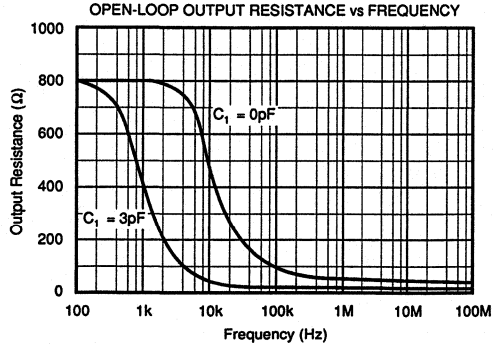
OPEN-LOOP PHASE vs FREQUENCY



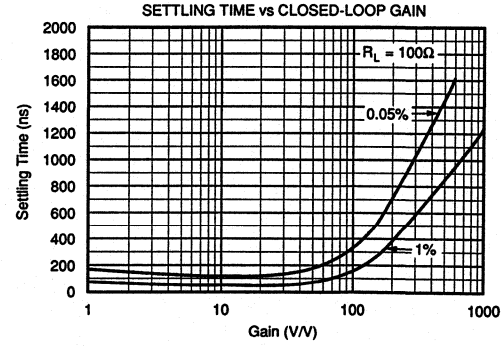
SLEW RATE vs COMPENSATION CAPACITOR



OPEN-LOOP OUTPUT RESISTANCE vs FREQUENCY



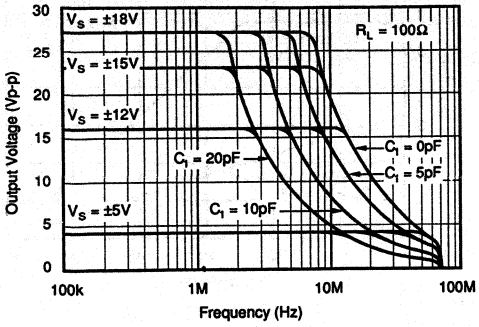
SETTLING TIME vs CLOSED-LOOP GAIN



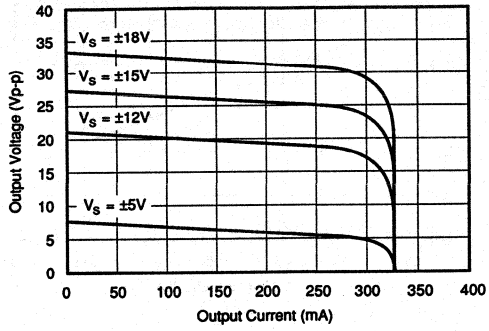
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_S = ±15V unless otherwise noted.

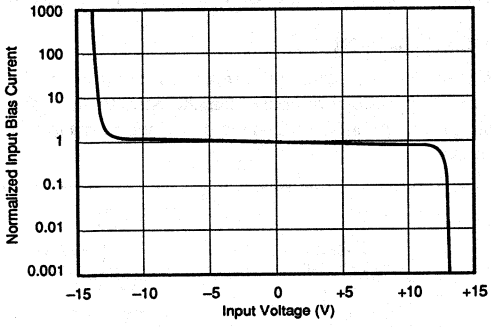
OUTPUT VOLTAGE vs FREQUENCY



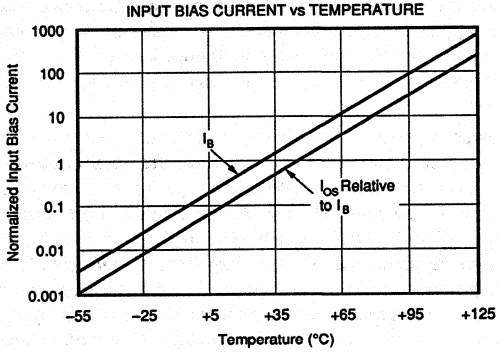
OUTPUT VOLTAGE vs OUTPUT CURRENT



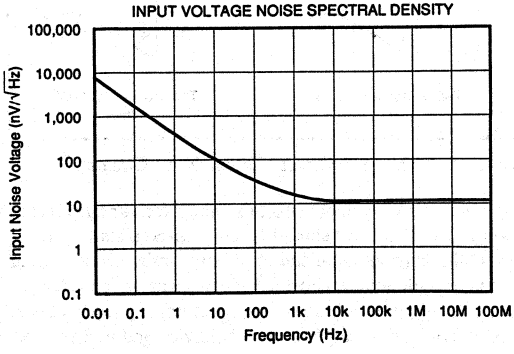
INPUT BIAS CURRENT



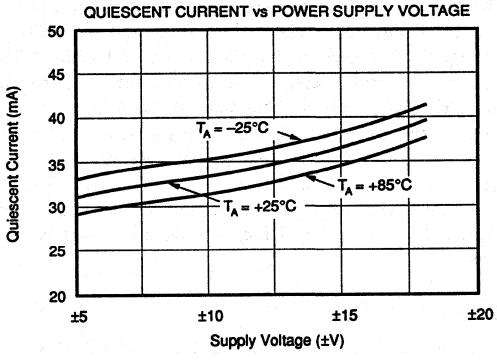
INPUT BIAS CURRENT vs TEMPERATURE



INPUT VOLTAGE NOISE SPECTRAL DENSITY

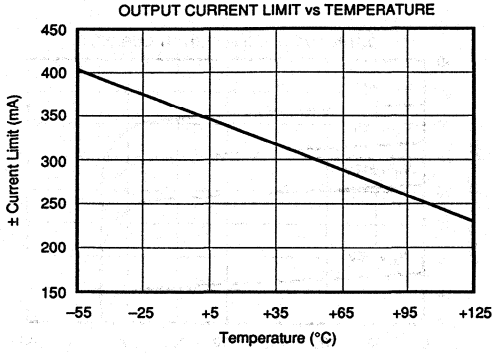


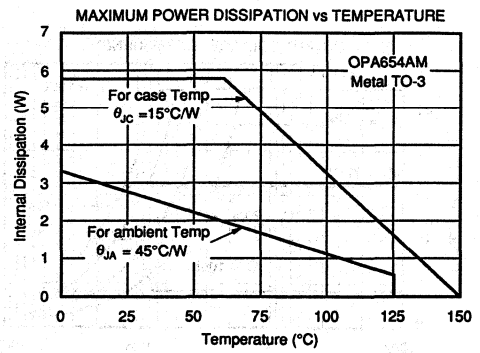
QUIESCENT CURRENT vs POWER SUPPLY VOLTAGE



TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_S = ±15V unless otherwise noted.





CIRCUIT LAYOUT

With any wide-bandwidth circuitry, careful circuit layout will ensure best performance. Make short, direct circuit interconnections and avoid stray wiring capacitance—especially at the inverting input pin. A component-side ground plane will help ensure low ground impedance. Do not place the ground plane under or near the inputs and feedback network.

Power supplies should be bypassed with good high-frequency capacitors positioned close to the op amp pins. In most cases, a 2.2µF solid tantalum capacitor for each power supply is adequate. The OPA654 can deliver load currents up to 200mA. Even if steady-state load currents are lower, signal transients may demand large current transients from the power supplies. It is the power supply bypass capacitors which must supply these current transients. Larger bypass capacitors such as 10µF solid tantalum capacitors may improve dynamic performance in these applications.

CASE CONNECTION

The case of the TO-3 metal package should be connected to ground. Failure to connect the case to ground will not damage the device but will degrade its AC performance. The case is internally connected to the substrate of the dielectrically isolated IC. This substrate is DC-neutral—it is not connected to the V– power supply as it would be with most analog ICs. In principle, it could be connected to any AC ground potential such as one of the power supplies, but DC ground is usually most convenient. Do not connect the case to DC potentials which exceed the power supply voltages, $\pm V_S$.

OFFSET ADJUSTMENT

Many applications require no external offset voltage adjustment. Figure 1a shows connection of an optional offset voltage trimming potentiometer. Use a small, non-inductive potentiometer with short connections to the trim pins. Avoid stray capacitance from the input or output nodes. The added resistors in Figure 1b help decouple the potentiometer from these sensitive nodes, making the type and location of the potentiometer less critical. This also reduces the trim range, providing more adjustment resolution. Do not use an offset voltage adjustment to correct for offsets produced in other circuitry since this can introduce large offset voltage drift.

COMPENSATION

The OPA654 uses external compensation capacitors. This tailors the open-loop response characteristics to the application. Its effect can be seen in the open-loop gain and phase curves.

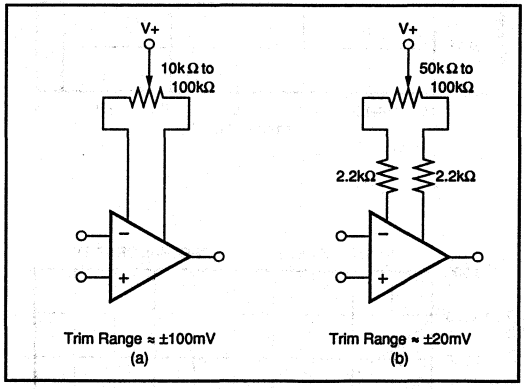
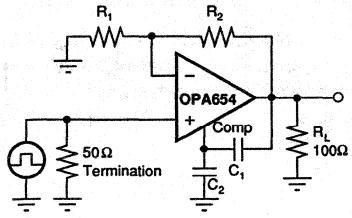
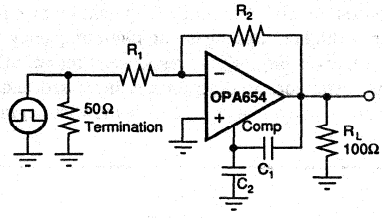


FIGURE 1. Optional Offset Voltage Trim Circuits.

Figures 2 shows typical capacitor values for various closed-loop gains. This chart should be considered a starting point for optimizing an application. Many variables including circuit layout, source and load characteristics, and desired dynamic behavior will affect the optimum capacitor values. Capacitive loads change op amp behavior and higher compensation capacitor values are generally required. Resistor R_S, shown in Figure 3, can improve the ability to drive a capacitive load. Typical values for R_S range from 5Ω to 50Ω, depending on the load and how much voltage drop can be tolerated.

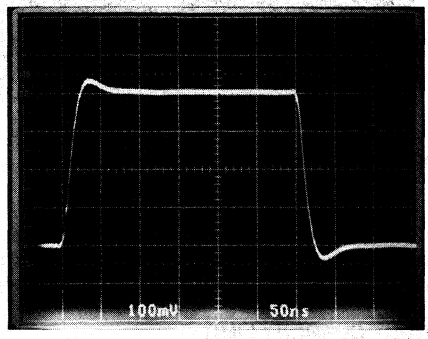




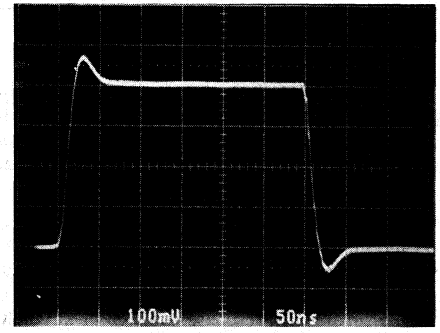
CLOSED-LOOP GAIN	METAL PACKAGE C_1	C_2	R_1	R_2
+1000	0.5pF	0	10Ω	10kΩ
+100	1pF	0	100Ω	10kΩ
+10	3pF	0	100Ω	900Ω
+1	18pF	30pF	—	0

CLOSED-LOOP GAIN	METAL PACKAGE C_1	C_2	R_1	R_2
−1000	0.5pF	0	10Ω	10kΩ
−100	1pF	0	100Ω	10kΩ
−10	3pF	0	100Ω	1kΩ
−1	18pF	20pF	1kΩ	1kΩ

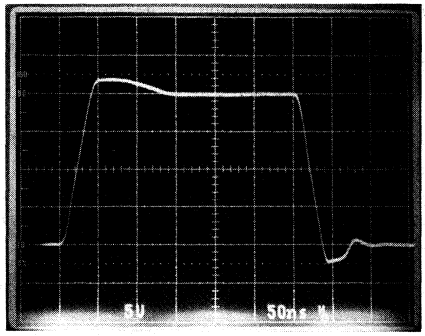
G = +10 SMALL-SIGNAL RESPONSE, R_L =100Ω



G = −10 SMALL-SIGNAL RESPONSE, R_L =100Ω



G = +10 LARGE-SIGNAL RESPONSE, R_L =100Ω



G = −10 LARGE-SIGNAL RESPONSE, R_L =100Ω

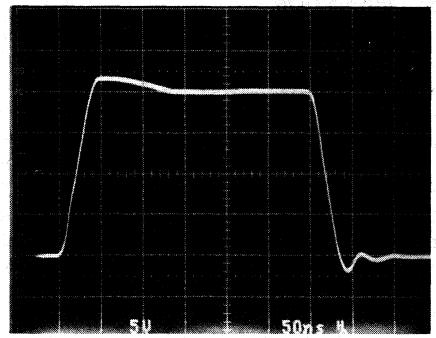


FIGURE 2. Basic Amplifier Circuits.

Figure 3 also demonstrates a compensation technique using an additional network, R_3-C_3. This allows use of a smaller value for C_1, producing a corresponding increase in slew rate. It reduces the high frequency loop gain by placing the op amp in a higher noise gain at high frequency. This technique improves large-signal response at the sacrifice of small-signal behavior. Settling time is increased and high frequency noise performance will be somewhat degraded.

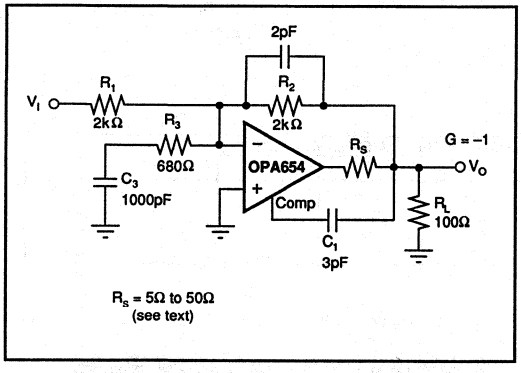


FIGURE 3. High Slew Rate Compensation Circuit.

Figure 4 shows an alternative compensation network for unity gain. This technique provides a small amount of positive feedback, reducing the net negative feedback factor. Large signal response and load driving capability is improved with this approach.

The compensation for a given application can be evaluated by observing amplifier pulse response. Both small-signal and large-signal response should be checked to assure that both are acceptable. Large overshoot or many cycles of ringing in the small-signal response is a sign of instability and the circuit may require further optimization. Good practice dictates a somewhat conservative approach to allow for device-to-device variation.

POWER DISSIPATION

Many applications do not require an external heat sink. However, with high ambient temperature or heavy load conditions, a heat sink may be required. The heat sink should be electrically connected to ground—see "Connections to Case". Operate within the power derating curve (Maximum Power Dissipation vs Temperature) shown in the typical performance curve section.

Exceeding the maximum die temperature of 165°C may activate the internal thermal limit circuitry, disabling the output stage. This thermal limit is set for a junction temperature of approximately 185°C.

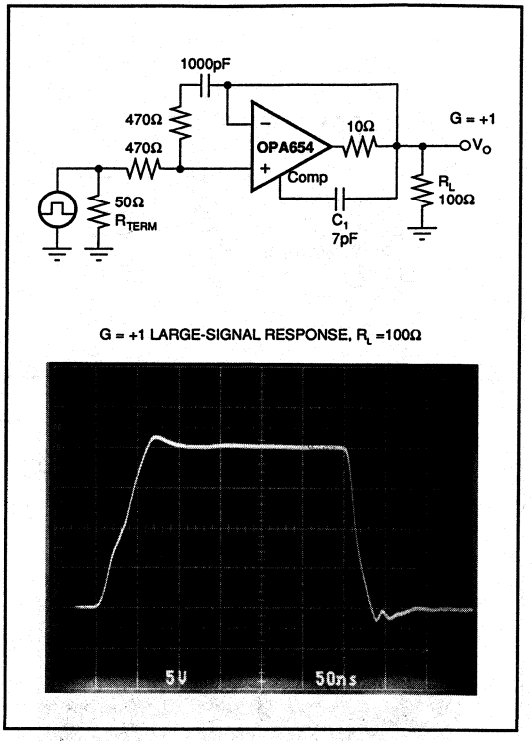


FIGURE 4. G = +1 Amplifier with Alternative Compensation.

The OPA654 may be operated at reduced power supply voltage, thus reducing internal power dissipation. This can eliminate the need for heat sinking in some applications.

OUTPUT CURRENT LIMIT

Output current is limited by internal circuitry to approximately 325mA at 25°C. The limit current decreases with increasing junction temperature as shown in the typical curves. The combination of current limit and thermal limit protects the device from short circuits to ground.

INPUT BIAS CURRENT

The OPA654 is fabricated with Burr-Brown's dielectrically isolated ***Difet*** process, giving it very low input bias current. Like other FET amplifiers, input bias current doubles for every 10°C increase in junction temperature. This increase can be minimized by providing a heat sink and, if possible, operating with reduced power supply voltage to minimize power dissipation.

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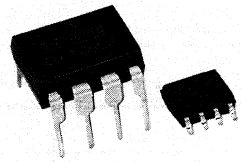


OPA660

Wide Bandwidth OPERATIONAL TRANSCONDUCTANCE AMPLIFIER AND BUFFER

FEATURES

- WIDE BANDWIDTH: 700MHz
- HIGH SLEW RATE: 3000V/µs
- LOW DIFFERENTIAL GAIN/PHASE ERROR
- VERSATILE CIRCUIT FUNCTION

APPLICATIONS

- VIDEO EQUIPMENT
- COMMUNICATIONS EQUIPMENT
- HIGH-SPEED DATA ACQUISITION

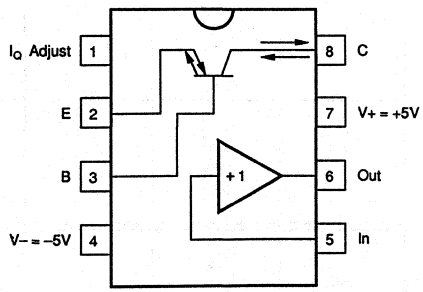
DESCRIPTION

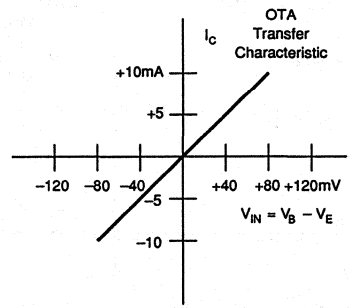
The OPA660 is a versatile monolithic component designed for wide-bandwidth systems including high performance video, RF and IF circuitry. It includes an integrated voltage-controlled current source and voltage buffer in an 8-pin package.

The voltage-controlled current source or Operational Transconductance Amplifier (OTA) can be viewed as an "ideal transistor." Like a transistor, it has three terminals—a high-impedance input (base), a low-impedance input/output (emitter), and the current output (collector). The OTA, however, is self-biased and bipolar. The output current is zero for zero differential input voltage. AC inputs centered about zero produce an output current which is bipolar and centered about zero. The transconductance of the OTA can be adjusted with an external resistor, allowing bandwidth, quiescent current and gain tradeoffs to be optimized.

The buffer stage provides 700MHz bandwidth and 3000V/µs slew rate. When combined with the OTA section, the OPA660 can be interconnected as a current-feedback amplifier. Used as a basic building block, the OPA660 can simplify the design of complex signal processing stages in video systems, communications equipment and high-speed data acquisition circuitry.

The OPA660 is packaged in SO-8 surface-mount, and 8-pin plastic DIP packages and is specified for the industrial temperature range.





International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

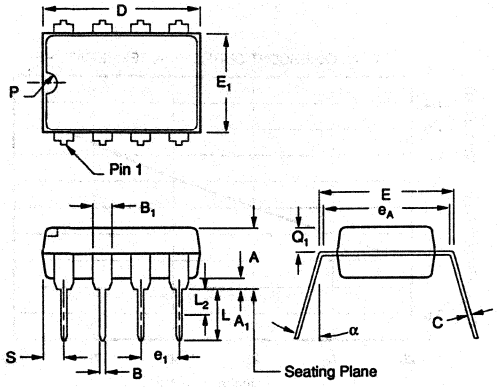
ELECTRICAL

Typical at I_O = 20mA, V_S = ±5VDC, T_A = +25°C, R_L = 500Ω unless otherwise specified.

PARAMETER	CONDITIONS	OPA660AP, AU MIN	OPA660AP, AU TYP	OPA660AP, AU MAX	UNITS
OTA TRANSCONDUCTANCE					
Transconductance	V_C = 0V	75	125	200	mA/V
OTA INPUT OFFSET VOLTAGE					
Initial			+7	±35	mV
vs Temperature			50		µV/°C
vs Supply (tracking)	V_S = ±4.5V to ±5.5V	55	60		dB
vs Supply (non-tracking)	V+ = 4.5V to 5.5V	40	45		dB
vs Supply (non-tracking)	V– = –4.5V to –5.5V	40	48		dB
OTA B-INPUT BIAS CURRENT					
Initial			–2.1	–2.2	µA
vs Temperature			5		nA/°C
vs Supply (tracking)	V_S = ±4.5V to ±5.5V			±750	nA/V
vs Supply (non-tracking)	V+ = 4.5V to 5.5V			±1500	nA/V
vs Supply (non-tracking)	V– = –4.5V to –5.5V			±500	nA/V
OTA OUTPUT BIAS CURRENT					
Output Bias Current	V_C = 0V		±10	±20	µA
vs Temperature			500		nA/°C
vs Supply (tracking)	V_S = ±4.5V to ±5.5V		±10	±25	µA/V
vs Supply (non-tracking)	V+ = 4.5V to 5.5V		±10	±25	µA/V
vs Supply (non-tracking)	V– = –4.5V to –5.5V		±10	±25	µA/V
OTA OUTPUT					
Output Current		±10	±15		mA
Output Voltage Compliance	I_C = ±1mA	±4.0	±4.7		V
Output Impedance			25k || 4.2		Ω || pF
Open Loop Gain	f = 1kHz		70		dB
BUFFER OFFSET VOLTAGE					
Initial			+7	±30	mV
vs Temperature			50		µV/°C
vs Supply (tracking)	V_S = ±4.5V to ±5.5V	55	60		dB
vs Supply (non-tracking)	V+ = 4.5V to 5.5V	40	45		dB
vs Supply (non-tracking)	V– = –4.5V to –5.5V	40	48		dB
BUFFER INPUT BIAS CURRENT					
Initial			–2.1	±5	µA
vs Temperature			5		nA/°C
vs Supply (tracking)	V_S = ±4.5V to ±5.5V			±750	nA/V
vs Supply (non-tracking)	V+ = 4.5V to 5.5V			±1500	nA/V
vs Supply (non-tracking)	V– = –4.5V to –5.5V			±500	nA/V
BUFFER INPUT IMPEDANCE					
Input Impedance			1.0 || 2.1		MΩ || pF
BUFFER INPUT NOISE					
Voltage Noise Density, f = 100kHz			4		nV/√Hz
BUFFER DYNAMIC RESPONSE					
Small Signal Bandwidth	V_O = ±100mV	700	850		MHz
Full Power Bandwidth	V_O = ±1.4V		800		MHz
	V_O = ±2.5V		570		MHz
Differential Gain Error	3.58MHz, at 0.7V		0.06		%
Differential Phase Error	3.58MHz, at 0.7V		0.02		Degrees
Harmonic Distortion, 2nd Harmonic	f = 10MHz, V_O = 0.5Vp-p		–68		dBc
Slew Rate	5V Step		3000		V/µs
Settling Time 0.1%	2V Step		25		ns
Rise Time (10% to 90%)	V_O = 100mVp-p		1		ns
	5V Step		1.5		ns
Group Delay Time			250		ps
BUFFER RATED OUTPUT					
Voltage Output	I_O = ±1mA	±3.7	±4.2		V
Current Output		±10	±15		mA
Gain		0.96	0.975		V/V
	R_L = 5kΩ		0.99		V/V
Output Impedance			7 || 2		Ω || pF
POWER SUPPLY					
Voltage, Rated			±5		V
Derated Performance		±4.5		±5.5	V
Quiescent Current (Programmable, Useful Range)		±3	±20	±26	mA

MECHANICAL

P Package — 8-Pin Plastic DIP

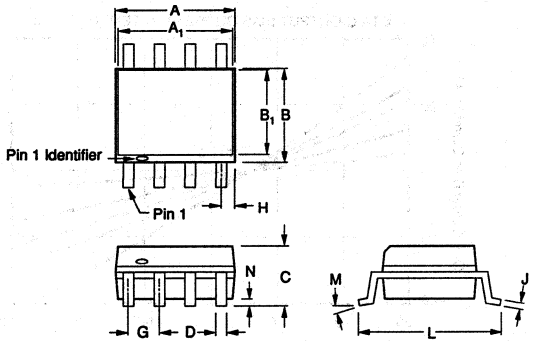


DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.155	.200	3.94	5.08
A1	.020	.050	0.51	1.27
B	.014	.020	0.36	0.51
B1	.045	.065	1.14	1.65
C	.008	.012	0.20	0.30
D (1)	.370	.400	9.40	10.16
E	.300	.325	7.62	8.26
E1	.240	.260	6.10	6.60
e1	.100 BASIC		2.54 BASIC	
eA	.300 BASIC		7.62 BASIC	
L	.125	.150	3.18	3.81

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
L2(2)	0	.030	0.00	0.76
α	0°	15°	0°	15°
P	.015	.050	0.38	1.270
Q1	.040	.075	1.02	1.91
S (1)	.015	.050	0.38	1.27

(1) Not JEDEC Std.
(2) e_1 and e_A apply in zone L_2 when unit installed.
NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

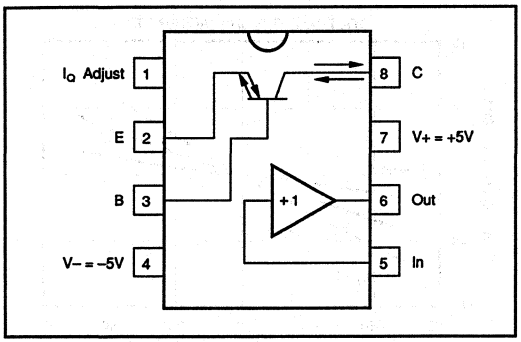
U Package — 8-Pin SOIC



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.185	.201	4.70	5.11
A1	.178	.201	4.52	5.11
B	.146	.162	3.71	4.11
B1	.130	.149	3.30	3.78
C	.054	.145	1.37	3.69
D	.015	.019	0.38	0.48
G	.050 BASIC		1.27 BASIC	
H	.018	.026	0.46	0.66
J	.008	.012	0.20	0.30
L	.220	.252	5.59	6.40
M	0°	10°	0°	10°
N	.000	.012	0.00	0.30

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only.

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage	±6V
Input Voltage (1)	$\pm V_S$ ±0.7V
Operating Temperature	–40°C to +85°C
Storage Temperature	–40°C to +125°C
Junction Temperature	+150°C
Lead Temperature (soldering, 10s)	+300°C

NOTE: (1) Inputs are internally diode-clamped to $\pm V_S$.

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

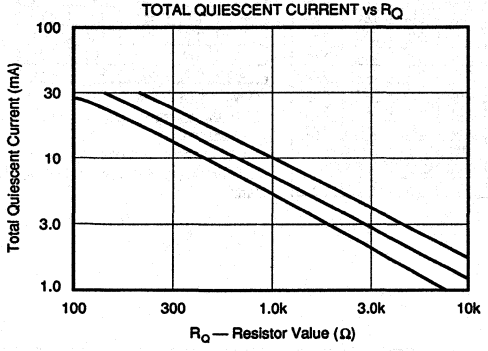
ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE
OPA660AP	Plastic 8-Pin DIP	–25°C to +85°C
OPA660AU	SO-8 Surface-Mount	–25°C to +85°C

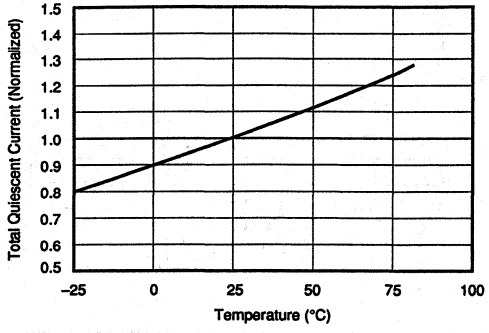
TYPICAL PERFORMANCE CURVES

I_Q = 20mA, T_A = +25°C, V_S = ±5V unless otherwise noted.

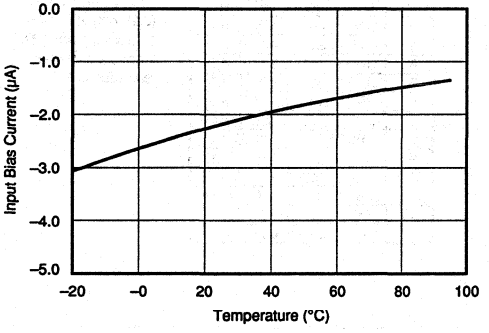
TOTAL QUIESCENT CURRENT vs R_Q



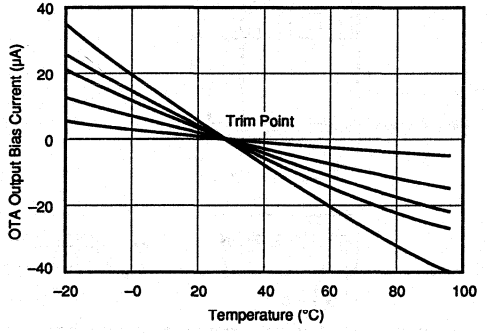
TOTAL QUIESCENT CURRENT vs TEMPERATURE



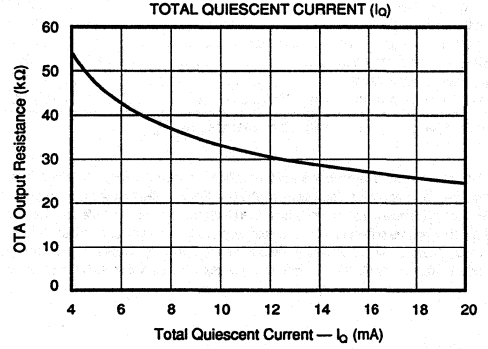
BUFFER and OTA B-INPUT BIAS CURRENT vs TEMPERTURE



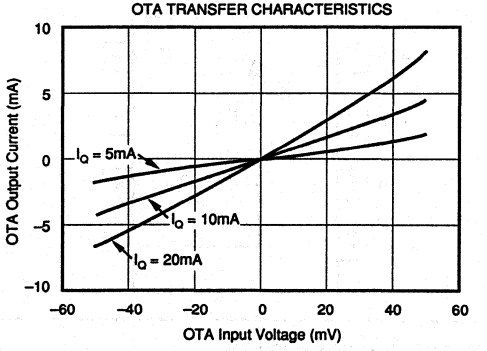
OTA C-OUTPUT BIAS CURRENT vs TEMPERATURE



OTA C-OUTPUT RESISTANCE vs TOTAL QUIESCENT CURRENT (I_Q)



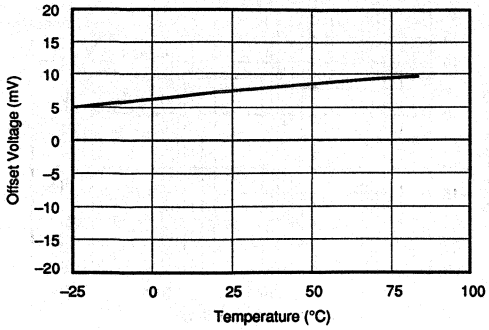
OTA TRANSFER CHARACTERISTICS



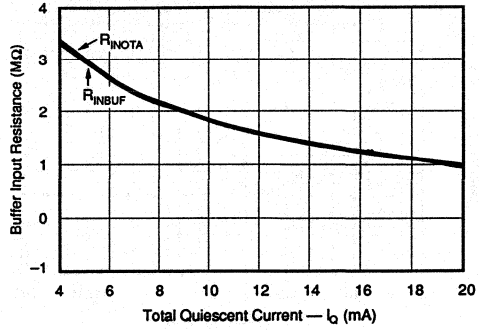
TYPICAL PERFORMANCE CURVES (CONT)

I_Q = 20mA, T_A = +25°C, V_S = ±5V unless otherwise noted.

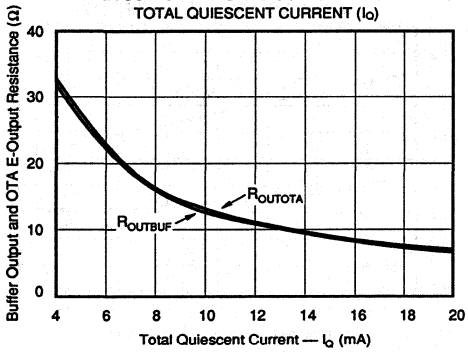
BUFFER AND OTA B-INPUT OFFSET VOLTAGE vs TEMPERATURE



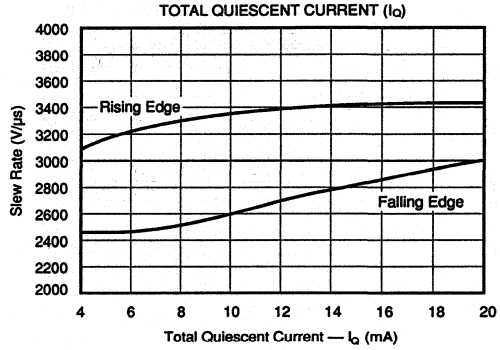
BUFFER AND OTA B-INPUT RESIBTANCE vs TOTAL QUIESCENT CURRENT (I_Q)



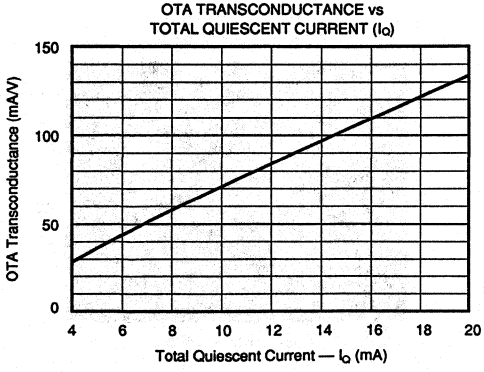
BUFFER OUTPUT AND OTA E-OUTPUT RESISTANCE vs TOTAL QUIESCENT CURRENT (I_Q)



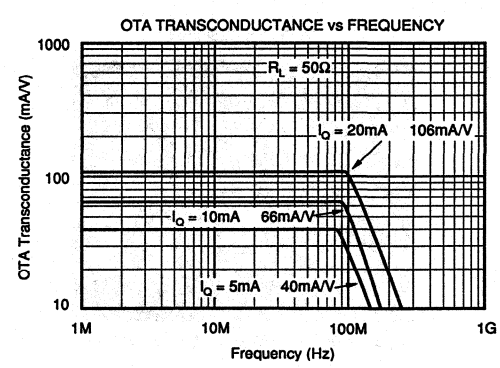
BUFFER SLEW RATE vs TOTAL QUIESCENT CURRENT (I_Q)



OTA TRANSCONDUCTANCE vs TOTAL QUIESCENT CURRENT (I_Q)



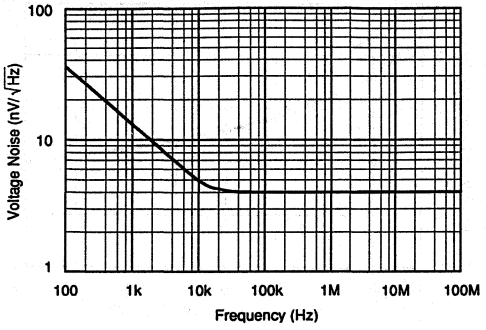
OTA TRANSCONDUCTANCE vs FREQUENCY



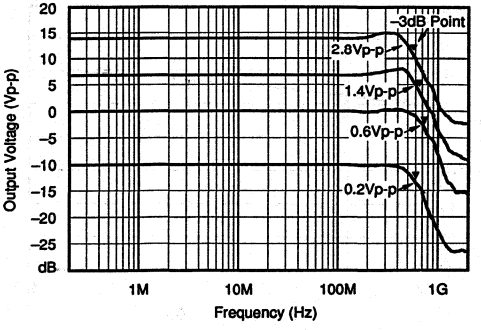
TYPICAL PERFORMANCE CURVES (CONT)

I_Q = 20mA, T_A = +25°C, V_S = ±5V unless otherwise noted.

BUFFER VOLTAGE NOISE SPECTRAL DENSITY

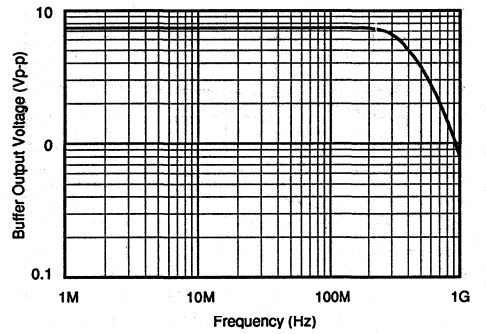


BUFFER FREQUENCY RESPONSE

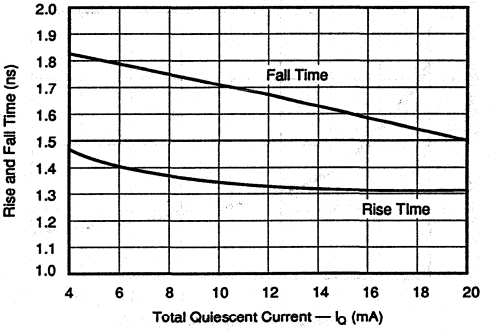


I_Q = 20mA R_{IN} = 160Ω R_L = 100Ω

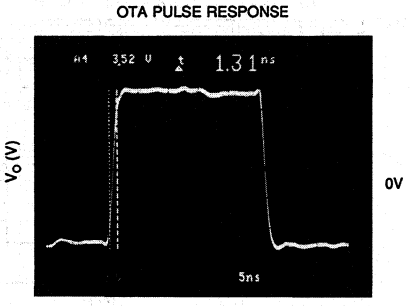
BUFFER MAX OUTPUT VOLTAGE vs FREQUENCY



BUFFER RISE AND FALL TIME vs TOTAL QUIESCENT CURRENT (I_Q)

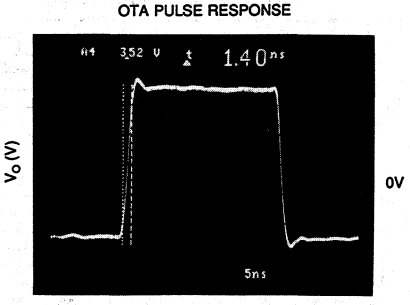


OTA PULSE RESPONSE



Input Voltage = 1.25Vp-p, t_r = t_f = 1ns, Gain = 4

OTA PULSE RESPONSE

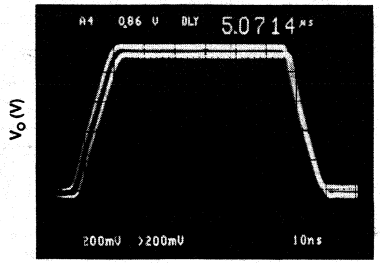


Output Voltage = 5Vp-p

TYPICAL PERFORMANCE CURVES (CONT)

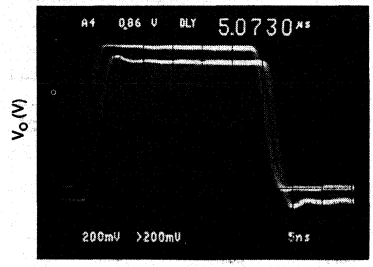
I_O = 20mA, T_A = +25°C, V_S = ±5V unless otherwise noted.

BUFFER LARGE SIGNAL PULSE RESPONSE

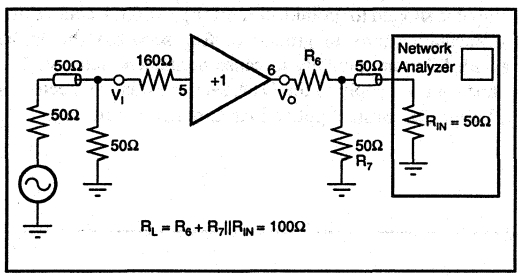


(HDTV Signal Pulse)

BUFFER LARGE SIGNAL PULSE RESPONSE

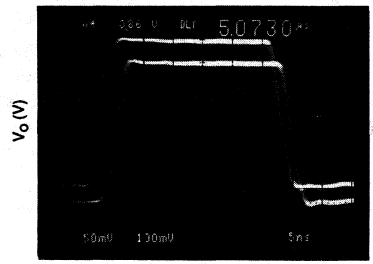


$t_r = t_f$ = 3ns



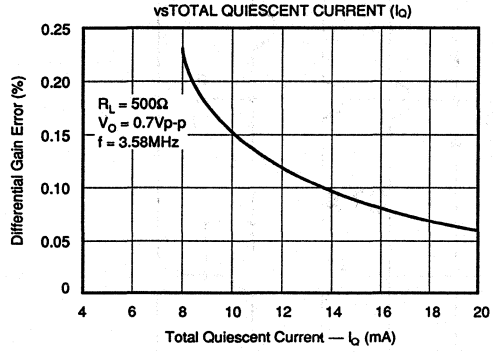
Test Circuit Buffer Pulse and Frequency Response

BUFFER SMALL SIGNAL PULSE RESPONSE

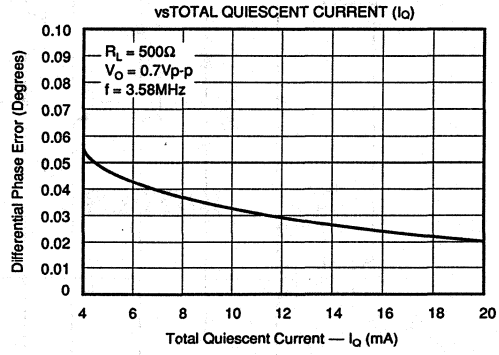


$t_r = t_f$ = 3ns

BUFFER DIFFERENTIAL GAIN ERROR vsTOTAL QUIESCENT CURRENT (I_O)

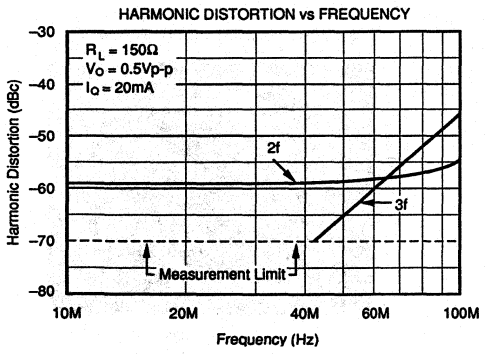


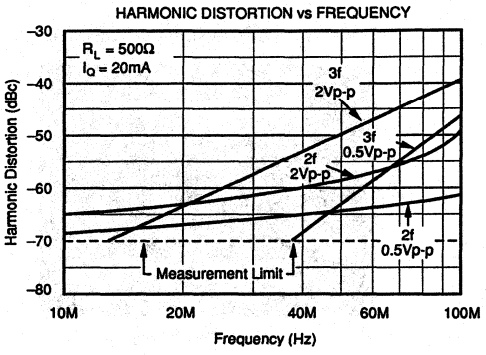
BUFFER DIFFERENTIAL PHASE ERROR vsTOTAL QUIESCENT CURRENT (I_O)



TYPICAL PERFORMANCE CURVES (CONT)

I_O = 20mA, T_A = +25°C, V_S = ±5V unless otherwise noted.





APPLICATIONS INFORMATION

The OPA660 operates from ±5V power supplies (±6V maximum). Do not attempt to operate with larger power supply voltages or permanent damage may occur.

Inputs of the OPA660 are protected with internal diode clamps as shown in the simplified schematic, Figure 1. These protection diodes can safely conduct 10mA, continuously (30mA peak). If input voltages can exceed the power supply voltages by 0.7V, the input signal current must be limited.

The buffer output is not current-limited or protected. If the output is shorted to ground, currents up to 60mA could flow. Momentary shorts to ground (a few seconds) should be avoided, but are unlikely to cause permanent damage. The same cautions apply to the OTA section when connected as a buffer (see Basic Applications Circuits, Figure 6b).

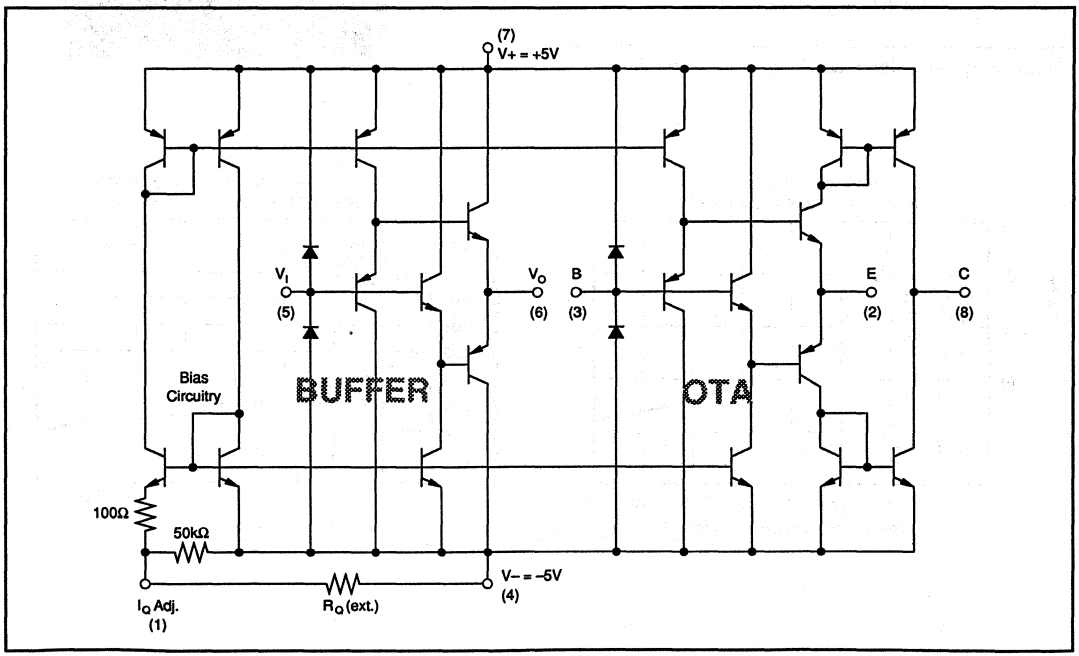


FIGURE 1. Simplified Circuit Diagram.

BUFFER SECTION—AN OVERVIEW

The buffer section of the OPA660 is an open-loop buffer consisting of complementary emitter-followers. It uses no feedback, so its low frequency gain is slightly less than unity and somewhat dependent on loading. It is designed primarily for interstage buffering. It is not designed for driving long cables or low impedance loads (although with small signals, it may be satisfactory for these applications).

TRANSCONDUCTANCE (OTA) SECTION—AN OVERVIEW

The symbol for the OTA section is similar to a transistor. Applications circuits for the OTA look and operate much like transistor circuits—the transistor, too, is a voltage-controlled current source. Not only does this simplify the understanding of applications circuits, but it aids the circuit optimization process. Many of the same intuitive techniques used with transistor designs apply to OTA circuits as well.

The three terminals of the OTA are labeled B, E and C. This calls attention to its similarity to a transistor, yet draws distinction for clarity.

While it is similar to a transistor, one essential difference is the sense of the C output current. It flows out the C terminal for positive B-to-E input voltage. The OTA offers many advantages over a discrete transistor. The OTA is self-biased, simplifying the design process and reducing component count. The OTA is far more linear than a transistor. Transconductance of a transistor is proportional to its collector current which is signal-dependent—this implies a fundamental nonlinearity.

BASIC CONNECTIONS

Figure 2 shows basic connections required for operation. These connections are not shown in subsequent circuit diagrams. Power supply bypass capacitors should be located as close as possible to the device pins. Solid tantalum capacitors are generally best. See "Circuit Layout" at the end of the applications discussion and Figure 26 for further suggestions on layout.

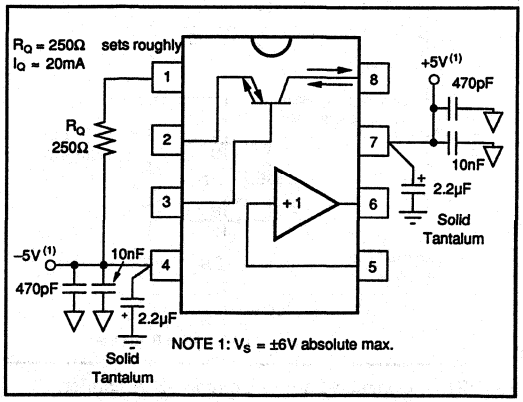


FIGURE 2. Basic Connections.

QUIESCENT CURRENT CONTROL PIN

The quiescent current of the OPA660 is set with a resistor, R_Q, connected from pin 1 to V–. It affects the operating currents of both the buffer and OTA sections. This controls the bandwidth and AC behavior as well as the transconductance of the OTA section.

R_Q = 250Ω sets approximately 20mA total quiescent current at 25°C. With a fixed 250Ω resistor, process variations could cause this current to vary from approximately 16mA to 26mA. It may be appropriate in some applications to trim this resistor to achieve the desired quiescent current or AC performance.

Applications circuits generally do not show resistor, R_Q, but it is required for proper operation.

With a fixed R_Q resistor, quiescent current increases with temperature (see typical performance curve, Quiescent Current vs Temperature). This variation of current with temperature holds the transconductance, gm, of the OTA relatively constant with temperature (another advantage over a transistor).

It is also possible to vary the quiescent current with a control signal. The control loop in Figure 3 shows a 1/2 of a REF200 current source used to develop 100mV on R_1. The loop forces 100mV to appear on R_2. Total quiescent current of the OPA660 is approximately 85 • I_1, where I_1 is the current made to flow out of pin 1.

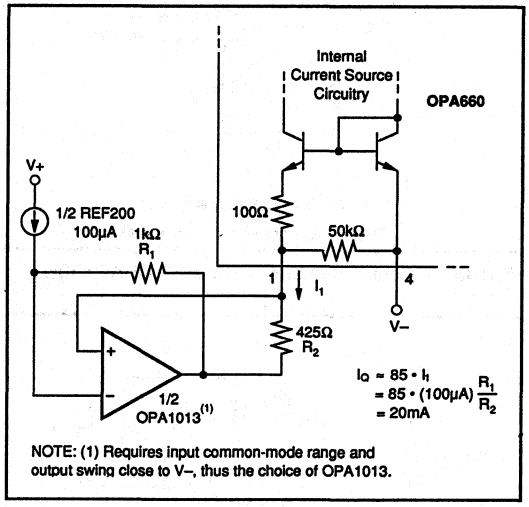


FIGURE 3. Optional Control Loop for Setting Quiescent Current.

With this control loop, quiescent current will be nearly constant with temperature. Since this differs from the temperature-dependent behavior of the internal current source, other temperature-dependent behavior may differ from that shown in typical performance curves.

The circuit of Figure 3 will control the I_Q of the OPA660 somewhat more accurately than with a fixed external resis-

tor, R_Q. Otherwise, there is no fundamental advantage to using this more complex biasing circuitry. It does, however, demonstrate the possibility of signal-controlled quiescent current. This may suggest other possibilities such as AGC, dynamic control of AC behavior or VCO.

Figure 4 shows logic control of pin 1 used to disable the OPA660. Zero/5V logic levels are converted to a 1mA/0mA current connected to pin 1. The the 1mA current flowing in RQ increases the voltage at pin 1 to approximately 1V above the –5V rail. This will reduce IQ to near zero, disabling the OPA660.

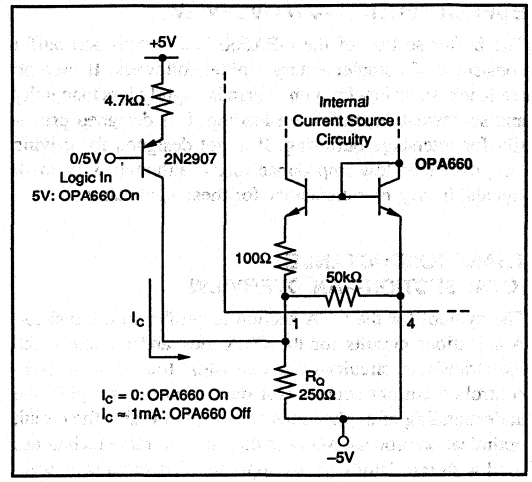


FIGURE 4. Logic-Controlled Disable Circuit.

BASIC APPLICATIONS CIRCUITS

Most applications circuits for the OTA section consist of a few basic types which are best understood by analogy to a transistor. Just as the transistor has three basic operating modes—common emitter, common base, and common collector—the OTA has three equivalent operating modes common-E, common-B, and common-C. See Figures 5, 6 and 7.

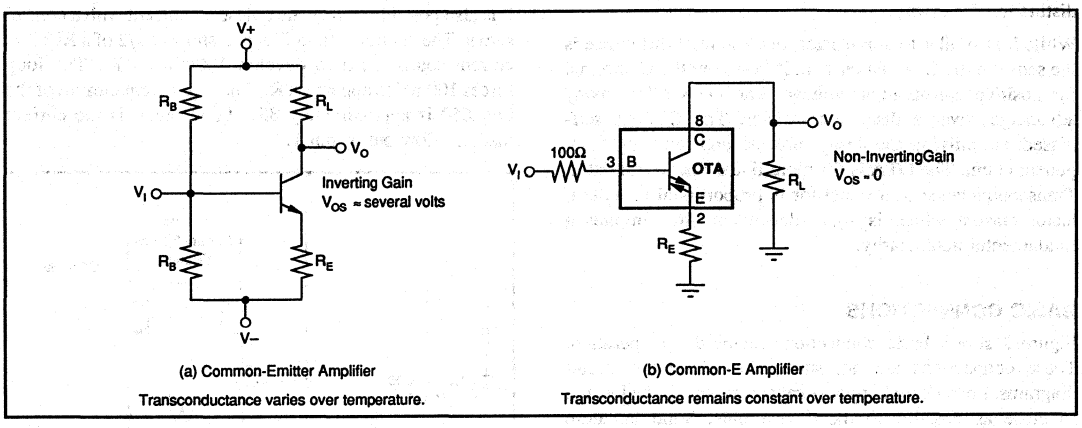


FIGURE 5. Common-Emitter vs Common-E Amplifier.

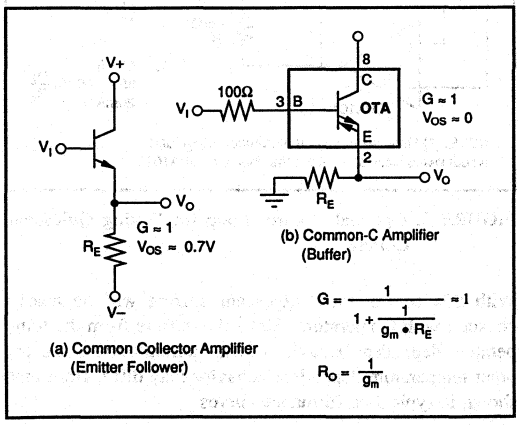


FIGURE 6. Common Collector vs Common-C Amplifier.

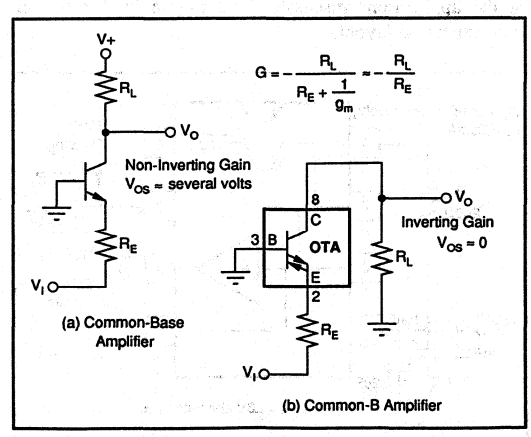


FIGURE 7. Common-Base vs Common-B Amplifier.

A positive voltage at the B, pin 3, causes a positive current to flow *out* of the C, pin 8. Figure 5b shows an amplifier connection of the OTA, the equivalent of a common-emitter transistor amplifier. Input and output can be ground-referenced without any biasing. Due to the sense of the output current, the amplifier is non-inverting. Figure 8 shows amplifier with various gains and output voltages using this configuration.

Just as transistor circuits often use emitter degeneration, OTA circuits may also use degeneration. This can be used to reduce the effect that offset voltage and offset current might otherwise have on the DC operating point of the OTA. The E-degeneration resistor may be bypassed with a large capacitor to maintain high AC gain. Other circumstances may suggest a smaller value capacitor used to extend or optimize high frequency performance.

The transconductance of the OTA with degeneration can be calculated by—

$$g_m' = \frac{1}{\frac{1}{g_m} + R_E}$$

Figure 6b shows the OTA connected as an E-follower—a voltage buffer. The buffer formed by this connection performs virtually the same as the buffer section of the OPA660 (the actual signal path is identical). A difference between the two, however, is that load current in pin 2 is replicated in the C terminal, pin 8. Since the C current comes from the power supplies, it is wasted. Twice the load current is drawn from the supplies. Load currents are often small compared to the quiescent current, making this entirely acceptable.

Many OTA and buffer circuits are improved by adding a low value resistor in series with the B input. This can reduce any tendency to oscillate and control frequency response peaking. Values from 25Ω to 200Ω are typical.

Figure 7 shows the Common-B amplifier. This configuration produces an inverting gain.

CIRCUIT LAYOUT

The high frequency performance of the OPA660 can be greatly affected by the physical layout of the circuit. The following tips are offered as suggestions, not dogma.

- Bypass power supplies very close to the device pins. Use a combination between tantalum capacitors (approximately 2.2µF) and polyester capacitors. Surface-mount types are best because they provide lowest inductance.
- Make short, wide interconnection traces to minimize series inductance.
- Use a large ground plane to assure that a low impedance ground is available throughout the layout.

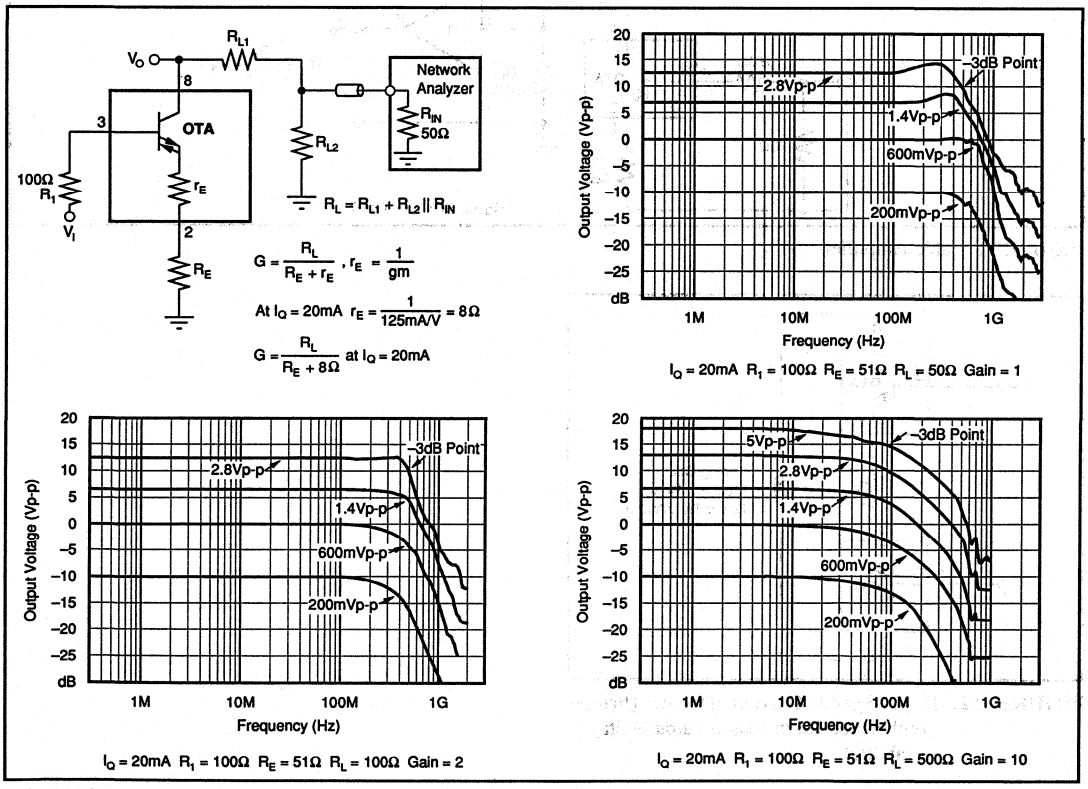


FIGURE 8. Common-E Amplifier Performance.

- Do not extend the ground plane under high impedance nodes sensitive to stray capacitance.
- Sockets are not recommended because they add significant inductance.
- Use low inductance components. Some film resistors are trimmed with spiral cuts which increase inductance.
- Use surface-mount components—they generally provide the lowest inductance.
- A resistor (25Ω to 200Ω) in series with the buffer and/or B input may help reduce oscillations and peaking.
- Use series resistors in the supply lines to decouple multiple devices.

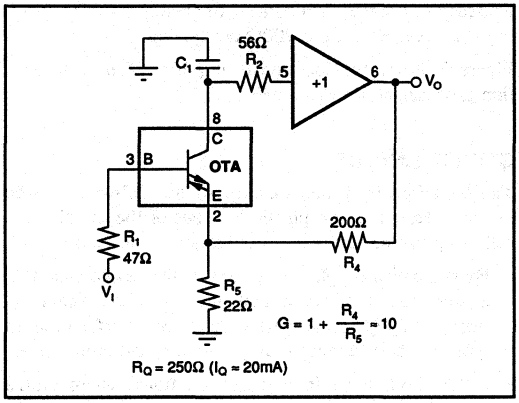


FIGURE 9. Current-Feedback Amplifier.

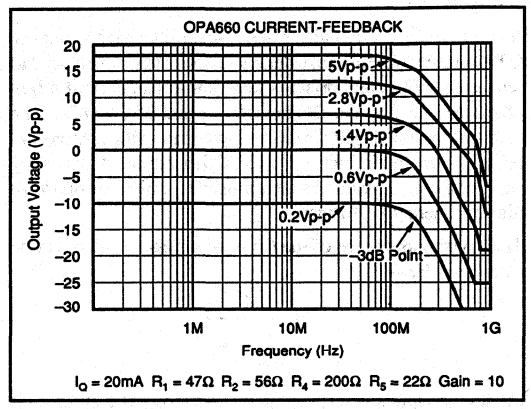


FIGURE 10. Current-Feedback Amplifier Frequency Response, G = 10.

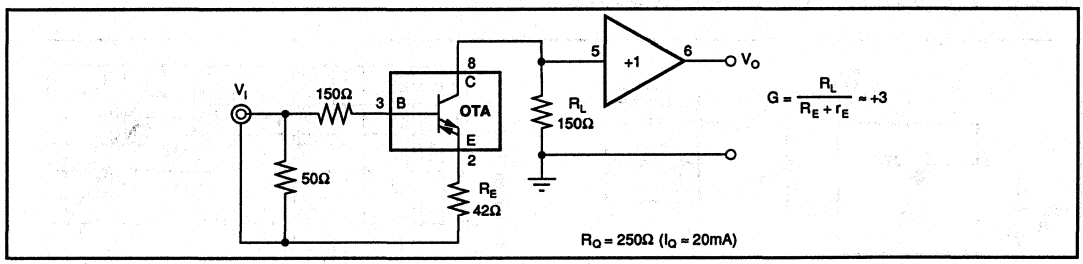


FIGURE 11. Cable Amplifier.

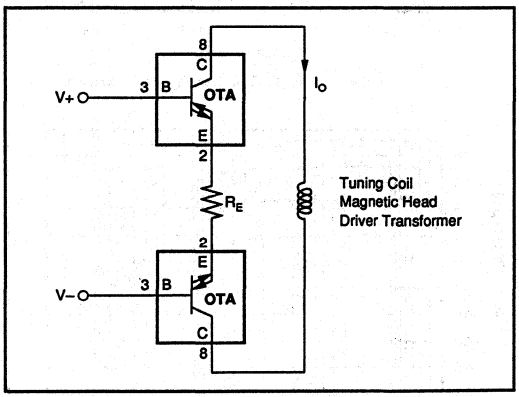


FIGURE 12. High Speed Current Driver (bridge combination for increased output voltage capability).

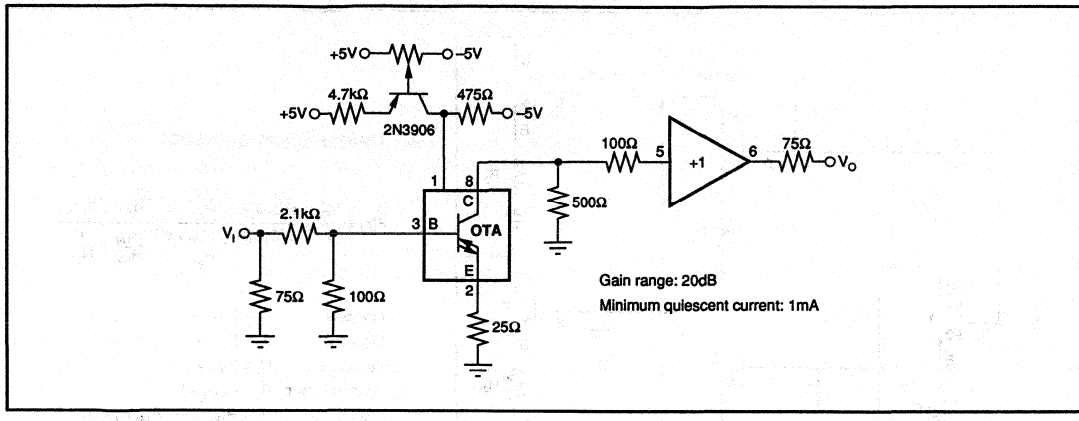


FIGURE 13. Variable Gain Amplifier (Luminance).

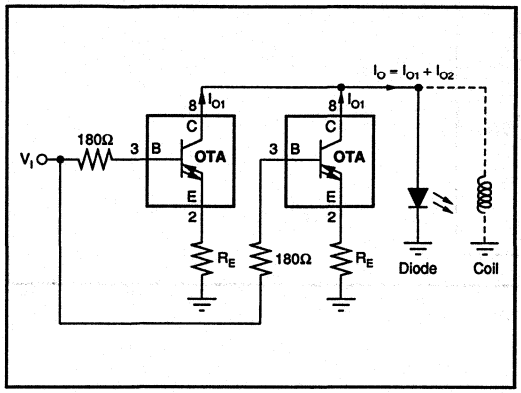


FIGURE 14. High Speed Current Driver (parallel combination for increased output current).

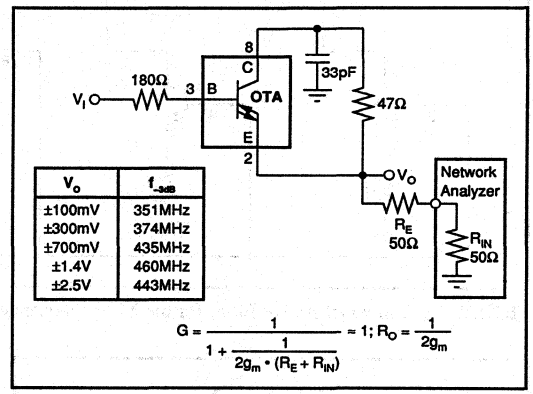


FIGURE 15. Voltage Buffer with Doubled Output Current.

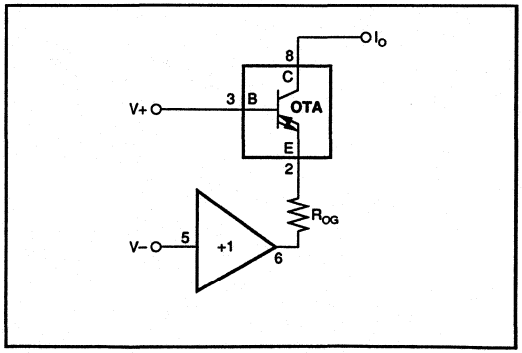


FIGURE 16. Operational Transconductance Amplifier.

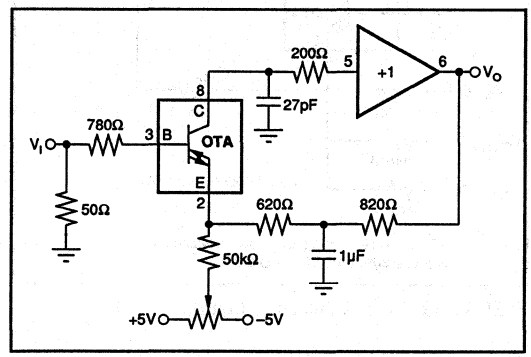


FIGURE 17. Integrator for ns-pulses.

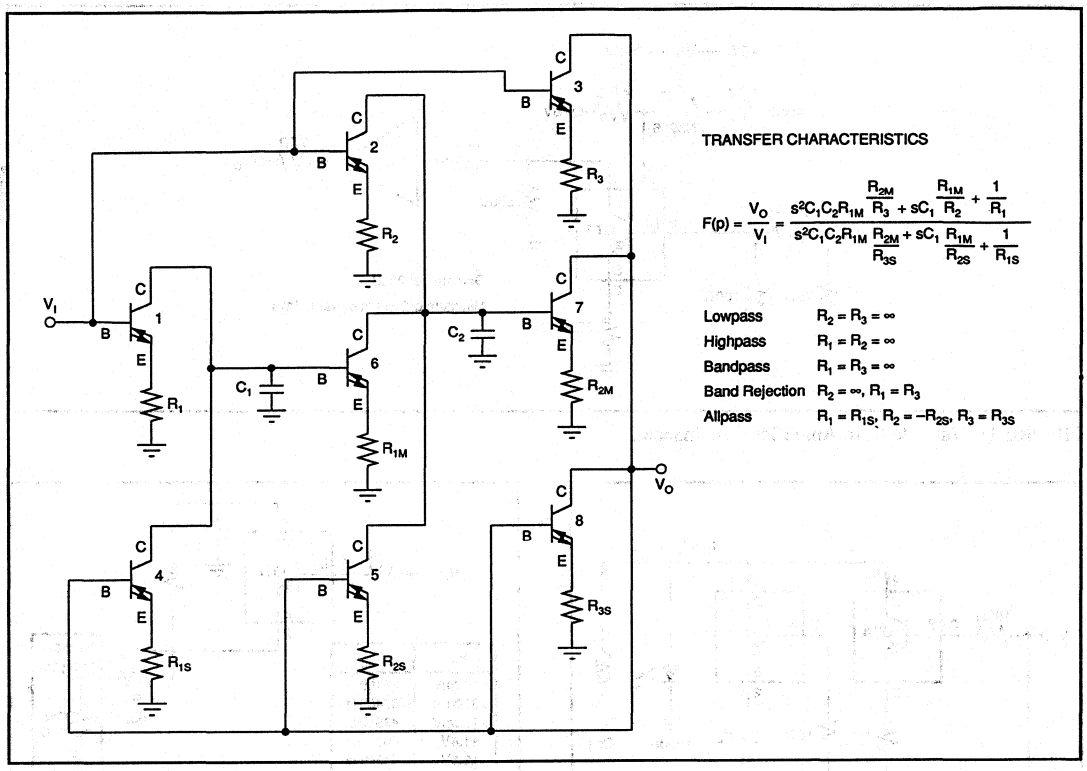


FIGURE 18. Universal Active Filter for the MHz Frequency Range.

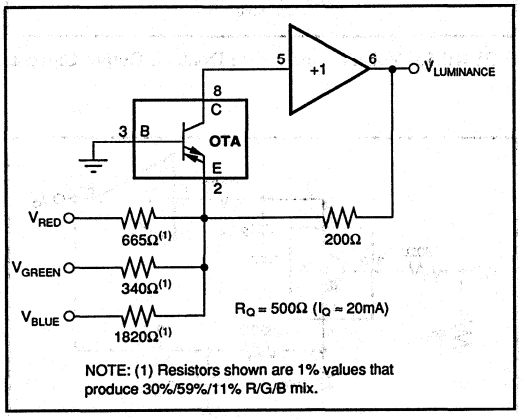


FIGURE 19. Video Luminance Matrix.

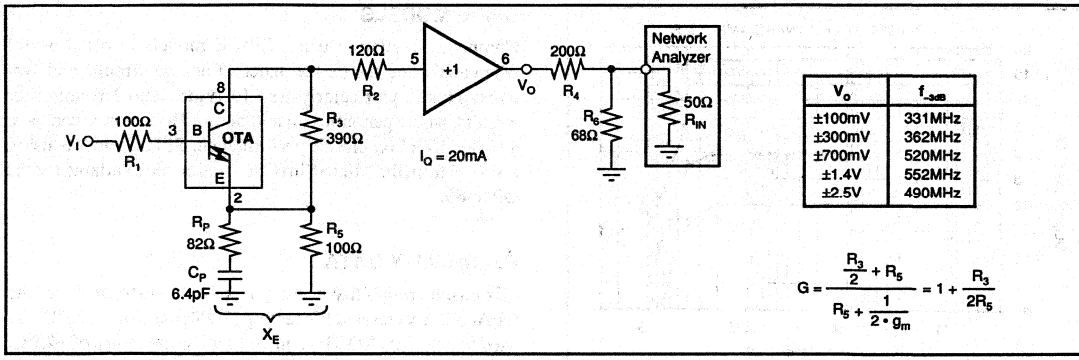


FIGURE 20. Direct-Feedback Amplifier.

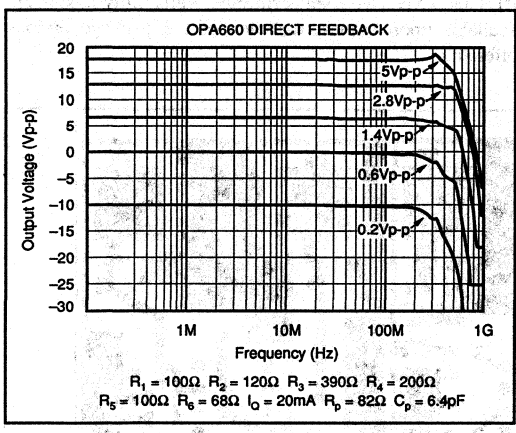


FIGURE 21. Frequency Response Direct-Feedback Amplifier.

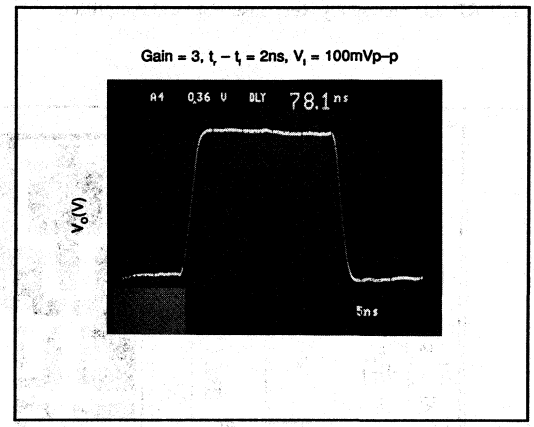


FIGURE 22. Direct-Feedback Amplifier Small-Signal Pulse Response.

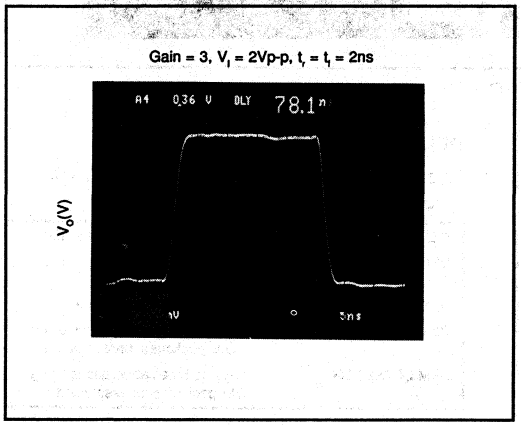


FIGURE 23. Direct-Feedback Amplifier Large-Signal Pulse Response.

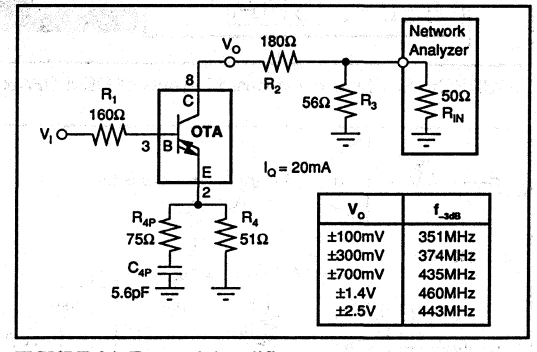


FIGURE 24. Forward Amplifier.

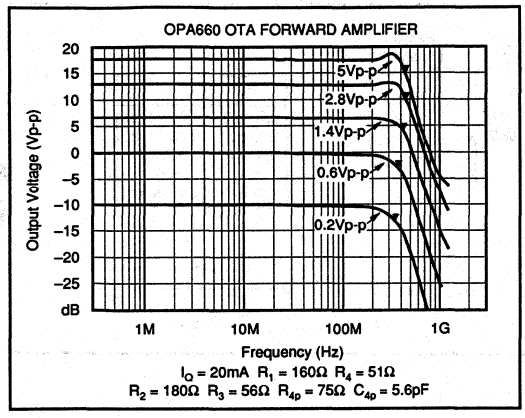


FIGURE 25. Frequency Response Forward Amplifier.

SPICE MODELS

Computer simulation using SPICE models is often useful when analyzing the performance of analog circuits and systems. This is particularly true for video and RF amplifier circuits, where parasitic capacitance and inductance can have a major effect on circuit performance. SPICE models using PSPICE from the Micro Sim Corporation are available for the OPA660.

RELIABILITY DATA

Extensive reliability testing has been performed on the OPA660. Accelerated life testing (1000 hours) at +125°C was used to calculate MTTF at an ambient temperature of +25°C. These test results yield a MTTF of: SO-package = 1.59E+07, and plastic DIP = 1.59E + 07 hours. Additional tests such as PTH and ESD have been performed. Reliablility reports are available upon request for each of the package options offered.

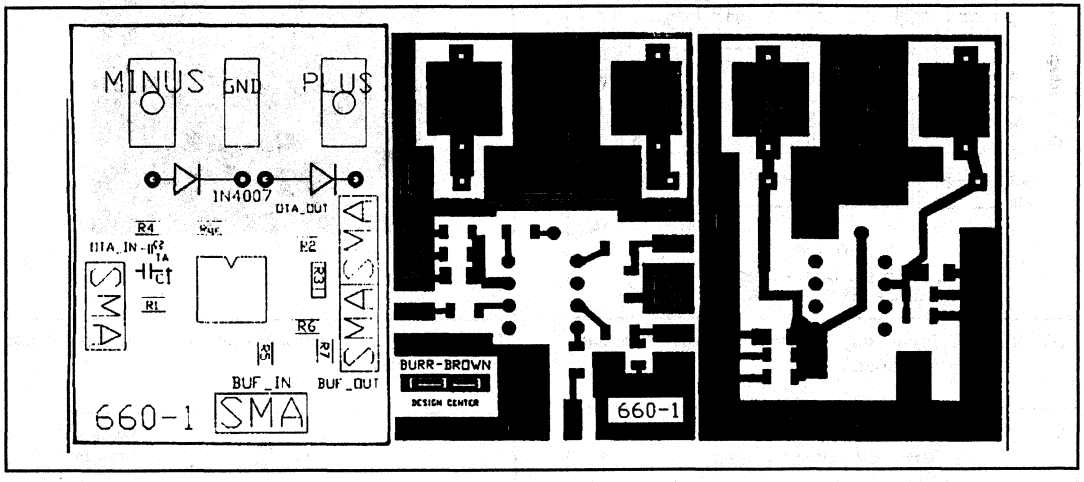


FIGURE 26. Silk Screen and Board Layouts of DEM OPA660-1GC.

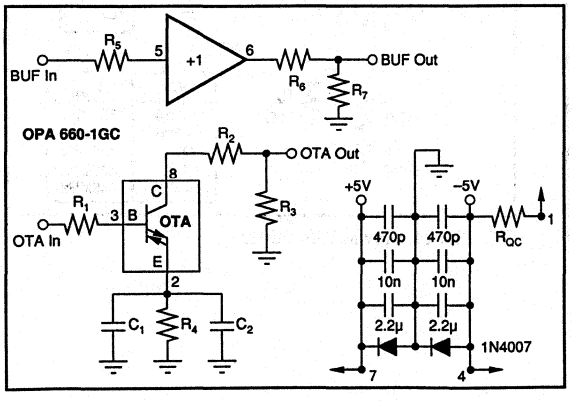


FIGURE 27. Circuit Diagram DEM OPA660-1GC.

DEMONSTRATION BOARDS

Five different demonstration boards are available to speed prototyping.

DEM OPA660-1GC	Diamond Transistor and Buffer
DEM OPA660-2GC	Current-Feedback Operational Amplifier
DEM OPA660-3GC	Direct-Feedback Amplifier
DEM OPA660-4G	Layouts for all applications using SOIC packages, unassembled
DEM OPA660-5G	Layouts for all applications using DIP packages, unassembled

BURR-BROWN®

OPA671

AVAILABLE IN DIE

Wide Bandwidth, Fast Settling *Difet*® OPERATIONAL AMPLIFIER

FEATURES

- WIDE GAIN-BANDWIDTH: 35MHz
- HIGH SLEW RATE: 100V/µs
- FAST SETTLING: 240ns to 0.01%
- FET INPUT: I_B = 50pA max
- HIGH OUTPUT CURRENT: 50mA
- WIDE SUPPLY RANGE: V_S = ±4.5 to ±18V

APPLICATIONS

- HIGH-SPEED DATA ACQUISITION
- OPTOELECTRONICS
- TRANSIMPEDANCE AMPLIFIER
- LINE DRIVER

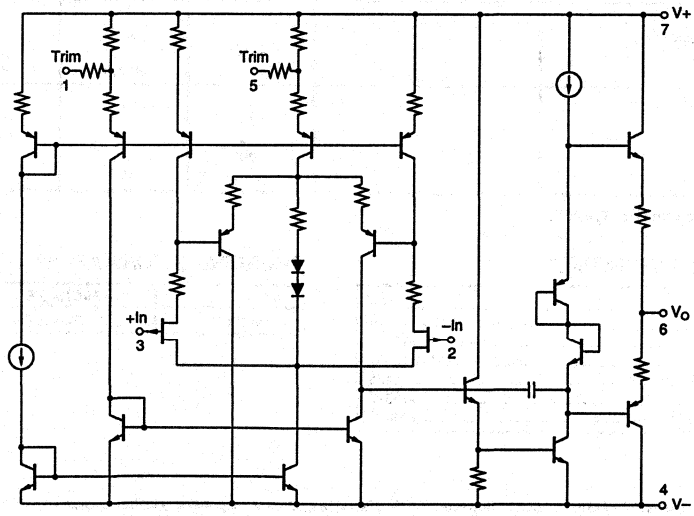
DESCRIPTION

The OPA671 is a FET-input monolithic operational amplifier featuring wide bandwidth and fast settling time. Fabricated using Burr-Brown's ***Difet***, complementary bipolar process, it provides an excellent combination of high speed, accuracy, and high output current.

The OPA671 is versatile, operating from ±4.5V to ±18V power supplies. It can deliver ±10V signals into a 200Ω load at slew rates of 100V/µs. OPA671's ***Difet*** input provides input bias current thousands of times lower than bipolar-input wideband op amps.

The OPA671 is internally compensated and is unity-gain stable, allowing use in the widest range of applications.

The OPA671 is available in an 8-pin plastic DIP, rated for the industrial temperature range.



Difet® Burr-Brown Corporation

International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

At T_A = +25°C, V_S = ±15V unless otherwise noted.

PARAMETER	CONDITION	OPA671AP MIN	OPA671AP TYP	OPA671AP MAX	UNITS
OFFSET VOLTAGE					
Input Offset Voltage			±0.5	±5	mV
Average Drift			±10		µV/°C
Power Supply Rejection	V_S = ±4.5 to ±16.5V	72	94		dB
INPUT BIAS CURRENT(1)					
Input Bias Current	V_{CM} = 0V		5	50	pA
Input Offset Current	V_{CM} = 0V		2		pA
NOISE					
Input Voltage Noise					
Noise Density, f = 100Hz			24		nV/√Hz
f = 1kHz			15		nV/√Hz
f = 10kHz			12		nV/√Hz
f = 100kHz			10		nV/√Hz
Voltage Noise, BW = 10Hz to 1MHz			60		µVp-p
Input Bias Current Noise					
Current Noise Density, f = 10Hz to 1MHz			2		fA/√Hz
INPUT VOLTAGE RANGE					
Common-Mode Input Range		±12	±13		V
Common-Mode Rejection	V_{CM} = ±10V	74	92		dB
INPUT IMPEDANCE					
Differential			10^{12} || 4.5		Ω || pF
Common-Mode			10^{12} || 6		Ω || pF
OPEN-LOOP GAIN					
Open-Loop Voltage Gain	V_O = ±10V, R_L = 1kΩ		80		dB
	V_O = ±10V, R_L = 200Ω	74	78		dB
FREQUENCY RESPONSE					
Gain-Bandwidth Product			35		MHz
Slew Rate	G = –1, 10V Step		107		V/µs
Settling Time 0.01%	G = –1, 10V Step		240		ns
0.1%	G = –1, 10V Step		150		ns
1%	G = –1, 10V Step		85		ns
Total Harmonic Distortion	G = 1, f = 100kHz V_O = 3V, R_L = 200Ω		0.0006		%
OUTPUT					
Voltage Output	R_L = 200Ω	±10.5	±11.5		V
Current Output	V_O = ±10V		50		mA
Short Circuit Current			–90/+105		mA
Output Resistance, Open-Loop	DC		20		Ω
POWER SUPPLY					
Specified Operating Voltage			±15		V
Operating Voltage Range		±4.5		±18	V
Quiescent Current			±14.8	±17	mA
TEMPERATURE RANGE					
Specification		–25		+85	°C
Operating		–40		+85	°C
Storage		–40		+125	°C
Thermal Resistance, θ_{JA}			100		°C/W

NOTES: (1) Tested without warmup at T_J = 25°C.

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage	±18V
Input Voltage	(V+) +1V to (V–) –1V
Operating Temperature	–40°C to +100°C
Storage Temperature	–40°C to +125°C
Output Short-Circuit to Ground	15s
Junction Temperature	+150°C
Lead Temperature (soldering, 10s)	+300°C

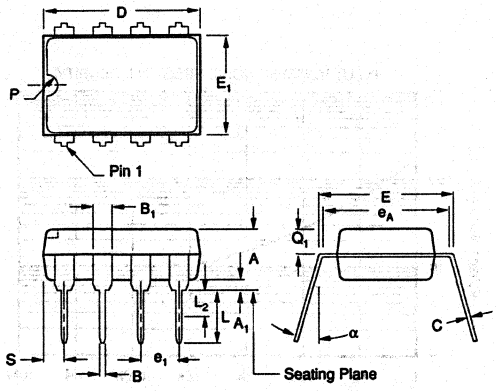
ORDERING INFORMATION

MODEL	PACKAGE	TEMP. RANGE
OPA671AP	8-Pin Plastic DIP	–25°C to +85°C

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

MECHANICAL

P Package — 8-Pin Plastic DIP

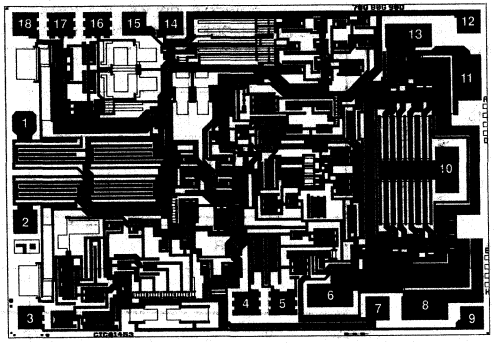


DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.155	.200	3.94	5.08
A1	.020	.050	0.51	1.27
B	.014	.020	0.36	0.51
B1	.045	.065	1.14	1.65
C	.008	.012	0.20	0.30
D (1)	.370	.400	9.40	10.16
E	.300	.325	7.62	8.26
E1	.240	.260	6.10	6.60
e1	.100 BASIC		2.54 BASIC	
eA	.300 BASIC		7.62 BASIC	
L	.125	.150	3.18	3.81

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
L2(2)	0	.030	0.00	0.76
α	0°	15°	0°	15°
P	.015	.050	0.38	1.270
Q1	.040	.075	1.02	1.91
S (1)	.015	.050	0.38	1.27

(1) Not JEDEC Std.
(2) e_1 and e_A apply in zone L_2 when unit installed.
NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

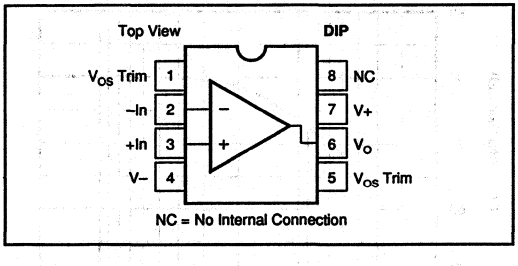
DIE INFORMATION



OPA671 DIE TOPOGRAPHY

PAD	FUNCTION
1	–In
2	+In
3	IQ
4	Comp In
5	Comp Out
6	–Short Circuit Bypass
7	–V
8	–V for O/P Stage
9	Balance 2A
10	Output
11	+V for O/P Stage
12	+V
13	+Short Circuit Bypass
14	Balance 2B
15	Balance 1
16	Slope
17	R_{CM}
18	R9

PIN CONFIGURATIONS



ELECTROSTATIC DISCHARGE SENSITIVITY

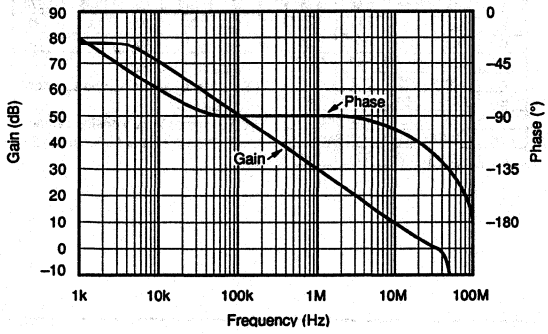
An integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

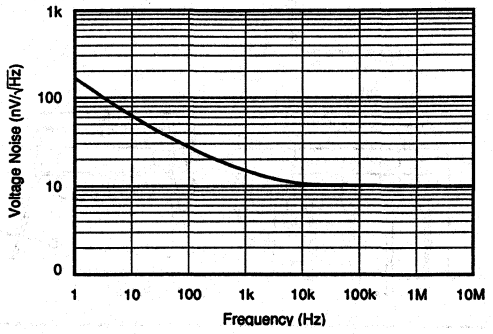
TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_S = ±15V unless otherwise noted.

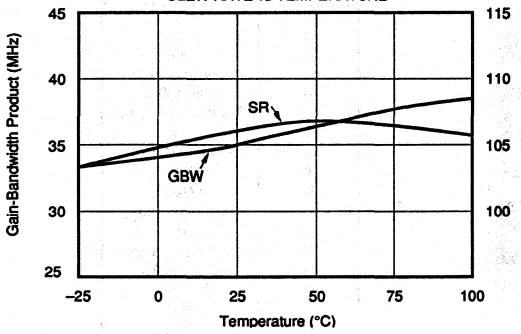
OPEN-LOOP GAIN AND PHASE vs FREQUENCY



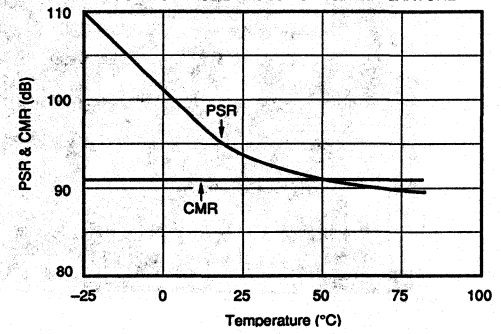
INPUT VOLTAGE NOISE SPECTRAL DENSITY



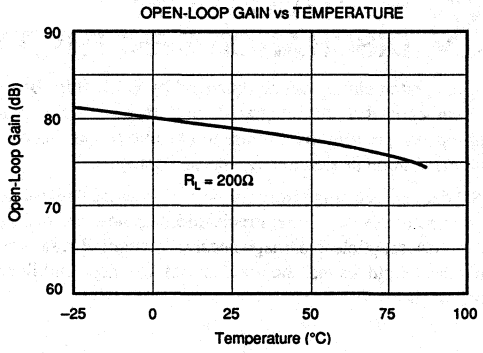
GAIN-BANDWIDTH PRODUCT & SLEW RATE vs TEMPERATURE



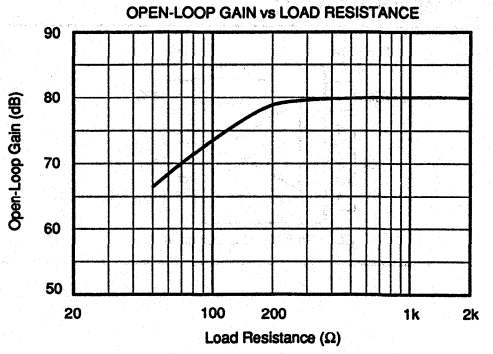
POWER SUPPLY REJECTION & COMMON-MODE REJECTION vs TEMPERATURE



OPEN-LOOP GAIN vs TEMPERATURE



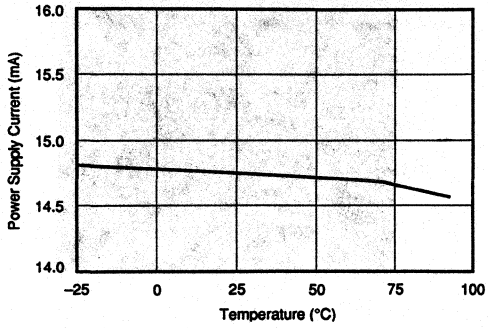
OPEN-LOOP GAIN vs LOAD RESISTANCE



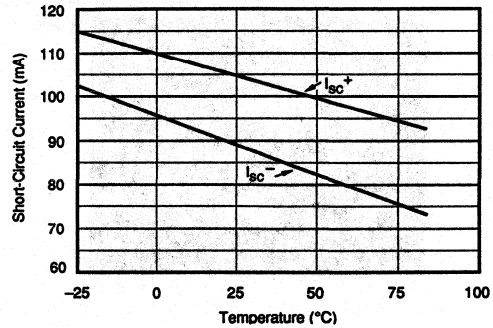
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_S = ±15V unless otherwise noted.

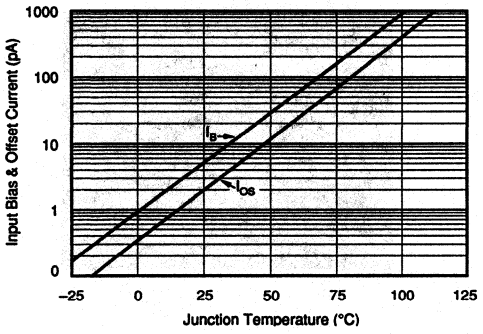
POWER SUPPLY CURRENT vs TEMPERATURE



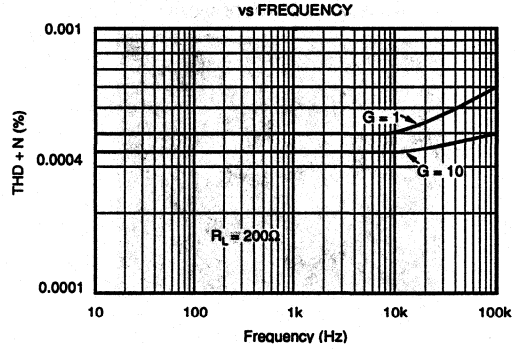
SHORT-CIRCUIT CURRENT vs TEMPERATURE



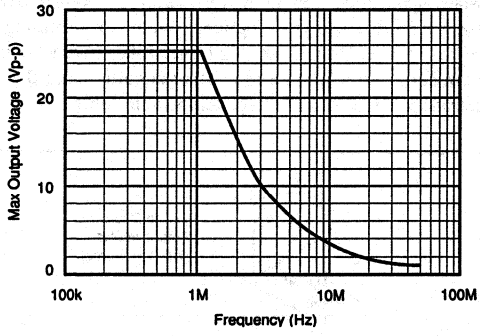
INPUT BIAS CURRENT AND INPUT OFFSET CURRENT vs JUNCTION TEMPERATURE



TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY



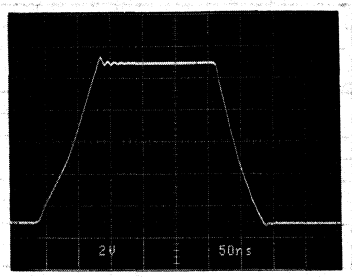
MAX OUTPUT VOLTAGE vs FREQUENCY



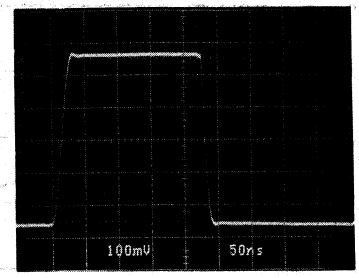
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_S = ±15V unless otherwise noted.

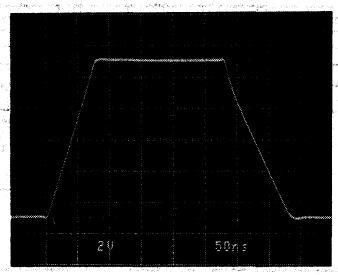
G = +1 LARGE SIGNAL RESPONSE



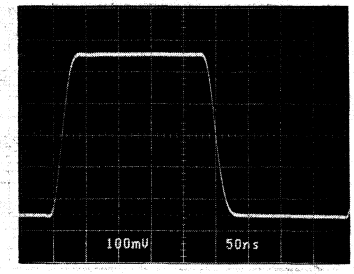
G = +1 SMALL SIGNAL RESPONSE



G = –1 LARGE SIGNAL RESPONSE



G = –1 SMALL SIGNAL RESPONSE



CIRCUIT LAYOUT

With any high-speed, wide-bandwidth circuitry, careful circuit layout will ensure best performance. Make short, direct circuit interconnections and avoid stray wiring capacitance—especially at the inverting input pin. A component-side ground plane will help ensure low ground impedance. Do not place the ground plane under or near the inputs and feedback network.

The power supply connections should be bypassed with good high-frequency capacitors positioned close to the op amp pins. In most cases, a 1µF solid tantalum capacitor for each power supply is adequate. The OPA671 can deliver peak load currents up to 100mA. Even if steady-state load currents are lower, signal transients may demand large current transients from the power supplies. It is the power supply bypass capacitors which must supply these current transients. Larger bypass capacitors such as 4.7µF solid tantalum capacitors may improve dynamic performance in some applications.

OFFSET ADJUSTMENT

Many applications require no external offset voltage adjustment. Figure 1 shows an optional circuit for trimming the offset voltage. Do not use this offset voltage adjustment to correct for offsets produced in other circuitry since this can introduce large offset voltage temperature drift.

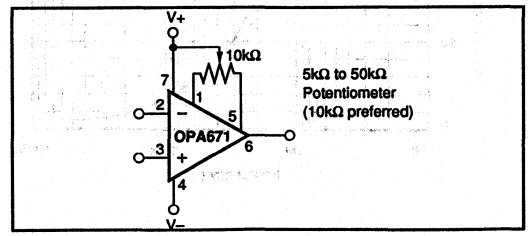


FIGURE 1. Optional Offset Voltage Trim Circuit.

CAPACITIVE LOADS

The OPA671 is internally compensated to be unity-gain stable with minimal capacitive load. The combination of low closed-loop gain and capacitive load will decrease the phase margin and may lead to gain peaking or oscillations. Load capacitance reacts with the op amp's open-loop output resistance to form an additional pole in the feedback loop. With wideband op amps, load capacitance as low as 50pF can introduce enough phase shift to degrade dynamic performance. Figure 2 shows circuits which preserve phase margin with capacitive load. Request Application Bulletin AB-028 for details on various compensation circuits and analysis techniques.

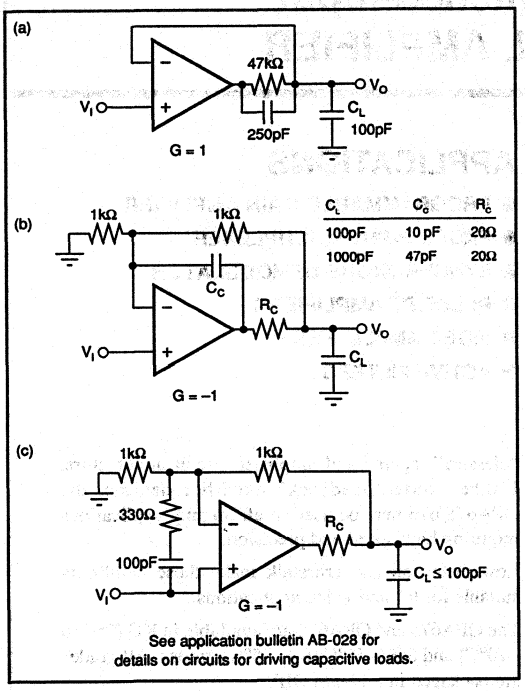


FIGURE 2. Compensation Circuits for Capacitive Loads.

POWER DISSIPATION

High output current can cause large internal power dissipation in the OPA671. Copper leadframe construction improves heat dissipation compared to conventional plastic packages. To achieve best heat dissipation, solder the device directly to the circuit board and use wide circuit board traces close to the device pins. Limit the ambient temperature, load and signal to assure that the maximum junction temperature is not exceeded. The OPA671 may be operated at reduced power supply voltage to minimize power dissipation.

OUTPUT CURRENT LIMIT

Output current is limited by internal circuitry to approximately 90mA at 25°C. The short-circuit limit current decreases with increasing junction temperature as shown in the typical curves. The current limit will protect the device from inadvertent short-circuits to ground. The power dissipation under this condition, however, is quite high so short-circuits should be avoided.

INPUT BIAS CURRENT

The OPA671 is fabricated with Burr-Brown's dielectrically isolated ***Difet*** process, giving it extremely low input bias current. As with other FET-input amplifiers, input bias current approximately doubles with every 10°C increase in junction temperature. Input bias current can be minimized by soldering the device to the circuit board to provided best heat dissipation. Reduced power supply voltage will also minimize input bias current by reducing internal power dissipation.

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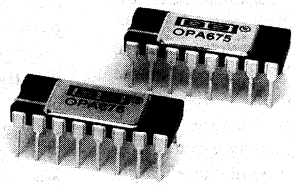


OPA675
OPA676

AVAILABLE IN DIE

Wideband Switched-Input OPERATIONAL AMPLIFIER

FEATURES

- FAST SETTLING: 9ns (1%)
- WIDE BANDWIDTH: 185MHz (A_V = 10)
- LOW OFFSET VOLTAGE: ±250µV
- TWO LOGIC SELECTABLE INPUTS
- FAST INPUT SWITCHING: 8ns (TTL)
- 16-PIN DIP PACKAGE

APPLICATIONS

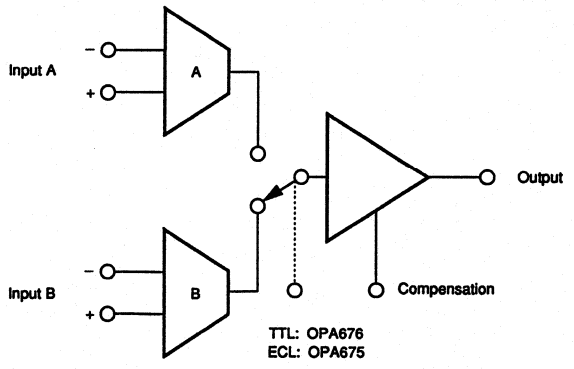
- PROGRAMMABLE-GAIN AMPLIFIER
- FAST 2-INPUT MULTIPLEXER
- SYNCHRONOUS DEMODULATOR
- PULSE/RF AMPLIFIERS
- VIDEO AMPLIFIERS
- ACTIVE FILTERS

DESCRIPTION

The OPA675 and OPA676 are wideband monolithic operational amplifiers with two independent differential inputs. Either input can be selected by an external logic signal. The OPA675 is compatible with ECL logic while the OPA676 is TTL compatible. Both amplifiers are externally compensated and feature very fast input selection speed: ECL = 4ns, TTL = 6ns. This amplifier features fully symmetrical differential inputs due to its "classical" operational amplifier circuit architecture. Unlike "current-feedback" amplifier designs, the OPA675/676 may be used in all op amp applications requiring high speed and precision.

Low distortion and crosstalk make these amplifiers suitable for RF and video applications.

The OPA675 and OPA676 are available in KG (0°C to +70°C) and SG (–55°C to +125°C) grades. All grades are packaged in a 16-pin DIP.



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SPECIFICATIONS

ELECTRICAL

At V_{CC} = ±5VDC, R_L = 150Ω, and T_A = +25°C unless otherwise noted.

PARAMETER	CONDITIONS	OPA675/676JG/SG MIN	OPA675/676JG/SG TYP	OPA675/676JG/SG MAX	OPA675/676KG MIN	OPA675/676KG TYP	OPA675/676KG MAX	UNITS
INPUT NOISE[1]								
Voltage: f_O = 10Hz	R_S = 0Ω		27			*		nV/√Hz
f_O = 100Hz			10			*		nV/√Hz
f_O = 1kHz			3.8			*		nV/√Hz
f_O = 10kHz			2.6			*		nV/√Hz
f_O = 100kHz			2.4			*		nV/√Hz
f_B = 10Hz to 10MHz			7.9			*		µVrms
Current: f_O = 10Hz to 1MHz			2.7			*		pA/√Hz
OFFSET VOLTAGE[1]								
Input Offset Voltage	V_{CM} = 0VDC		±500	±2mV		±250	±1mV	µV
Average Drift	$T_A = T_{MIN}$ to T_{MAX}		±3	±10		±1	±5	µV/°C
Supply Rejection	$\pm V_{CC}$ = 4.5V to 5.5V	65	86		70	*		dB
BIAS CURRENT[1]								
Input Bias Current	V_{CM} = 0VDC		23	35		*	30	µA
OFFSET CURRENT[1]								
Input Offset Current	V_{CM} = 0VDC		0.8	5		*	*	µA
INPUT IMPEDANCE[1]								
Differential			4k||2			*		Ω||pF
Common-Mode			10^6||5			*		Ω||pF
INPUT VOLTAGE RANGE[1]								
Common-Mode Input Range		±1.25	±2.5		*	*		V
Common-Mode Rejection	V_{IN} = ±0.5VDC, V_O = ±1.25V	75	100		85	*		dB
OPEN LOOP GAIN, DC[1]								
Open-Loop Voltage Gain		65	70		*	*		dB
FREQUENCY RESPONSE								
Closed-Loop Bandwidth	Gain = +2V/V		100			*		MHz
	Gain = +5V/V		145			*		MHz
	Gain = +10V/V		185			*		MHz
	Gain = +50V/V		60			*		MHz
Crosstalk	Gain = +10V/V, f = 100kHz		–100			*		dBC[2]
	f = 1MHz		–80			*		dBC
	f = 10MHz		–68			*		dBC
	f = 100MHz		–35			*		dBC
Harmonic Distortion: 10MHz	G = +10V/V, R_L = 50Ω, V_O = 0.5Vp-p							
	Second Harmonic		–61			*		dBC
	Third Harmonic		–73			*		dBC
Full Power Response	V_O = 2.5Vp-p, Gain = +10V/V	25	44		30	*		MHz
Slew Rate	Gain = +10V/V	200	350		240	*		V/µs
Settling Time: 1%			9			*		ns
0.1%	Gain = +10V/V		15			*		ns
0.01%	0.625V Output Step		25			*		ns
INPUT SELECTION[3]								
Transition Time	ECL: OPA675		5			*		ns
50% In to 50% Out	TTL: OPA676		7.5			*		ns
DIGITAL INPUT								
TTL Logic Levels: V_{IL}	Logic "LO"	0		+0.8	*		*	V
V_{IH}	Logic "HI"	+2.0		+5	*		*	V
I_{IL}	Logic "LO", V_{IL} = 0V		–0.05	–0.2		*	*	mA
I_{IH}	Logic "HI", V_{IH} = +2.7V		1	20		*	*	µA
ECL Logic Levels: V_{IL}	Logic "LO"	–1.81		–1.475	*		*	V
V_{IH}	Logic "HI"	–1.15		– 0.88	*		*	V
I_{IL}	Logic "LO", V_{IL} = –1.6V		–50	–100		*	*	µA
I_{IH}	Logic "HI", V_{IH} = –1.0V		–50	–100		*	*	µA
RATED OUTPUT								
Voltage Output	R_L = 150Ω	±2.1	±2.6		*	*		V
	R_L = 50Ω	+1.25	+1.8		*	*		V
		–0.95	–1.1		–1.0	*		V
Current Output			±30			*		mA
Output Resistance	1MHz, Open Loop, C_C = 5pF		5			*		Ω
Load Capacitance Stability	Gain = +2V/V		50			*		pF
Short Circuit Current	Continuous to Gnd		+45			*		mA
			–25			*		mA

* Same specifications as for JG.

SPECIFICATIONS (CONT)

ELECTRICAL

At V_{CC} = ±5VDC, R_L = 150Ω, and T_A = +25°C unless otherwise noted.

PARAMETER	CONDITIONS	OPA675/676JG/SG			OPA675/676KG			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
POWER SUPPLY								
Rated Voltage	$\pm V_{CC}$		5			*		VDC
Derated Performance	$\pm V_{CC}$	4.5		6.5	*		*	VDC
Current, Quiescent	I_O = 0mADC		22	30		*	*	mA
TEMPERATURE RANGE								
Specification	Ambient Temp JG, KG	0		+70	*		*	°C
	SG	−55		+125				°C
Operating:	Ambient Temp JG, KG, SG	−55		+125	*		*	°C
θ_{JA}			125			*		°C/W

* Same specifications as for JG.

ELECTRICAL (FULL TEMPERATURE RANGE SPECIFICATIONS)

At V_{CC} = ±5VDC, R_L = 150Ω, and T_A = T_{MIN} to T_{MAX} unless otherwise noted.

PARAMETER	CONDITIONS	OPA675/676JG/SG			OPA675/676KG			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
TEMPERATURE RANGE								
Specification	Ambient Temp JG, KG	0		+70	*		*	°C
	SG	−55		+125				°C
OFFSET VOLTAGE								
Average Drift	T_A = T_{MIN} to T_{MAX}		±3	±10		±1	±5	µV/°C
Supply Rejection	$\pm V_{CC}$ = 4.5V to 5.5V	60	85		65	*		dB
BIAS CURRENT								
Input Bias Current	V_{CM} = 0VDC		29	50		*	*	µA
OFFSET CURRENT								
Input Offset Current	V_{CM} = 0VDC		0.8	10		*	*	µA
INPUT VOLTAGE RANGE								
Common-Mode Input Range		±2.0	±2.3		*	*		V
Common-Mode Rejection	V_{IN} = ±0.5VDC, V_O = ±1.25V	60	80		65	*		dB
OPEN LOOP GAIN, DC								
Open-Loop Voltage Gain		60	68		63	69		dB
DIGITAL INPUT								
TTL Logic Levels: V_{IL}	Logic "LO"	0		+0.8	*		*	V
V_{IH}	Logic "HI"	+2.0		+5	*		*	V
I_{IL}	Logic "LO", V_{IL} = 0V		−0.08	−0.4		*	*	mA
I_{IH}	Logic "HI", V_{IH} = +2.7V		5	50		*	*	µA
ECL Logic Levels: V_{IL}	Logic "LO"	−1.81		−1.475	*		*	V
V_{IH}	Logic "HI"	−1.15		−0.88	*		*	V
I_{IL}	Logic "LO", V_{IL} = −1.6V		−50			*		µA
I_{IH}	Logic "HI", V_{IH} = −1.0V		−50			*		µA
RATED OUTPUT								
Voltage Output	R_L = 150Ω	±2.0	±2.5		*	*		V
	R_L = 50Ω	+1.25	+1.6		*	*		V
		−0.8	−1.0		−0.9	*		V
POWER SUPPLY								
Current, Quiescent	I_O = 0mADC		25	35		*	*	mA

* Same specifications as for JG.

NOTES: (1) Specifications are for both inputs (A and B). (2) dBC = Level referred to carrier-input signal. (3) Switching time from application of digital logic signal to input signal selection.

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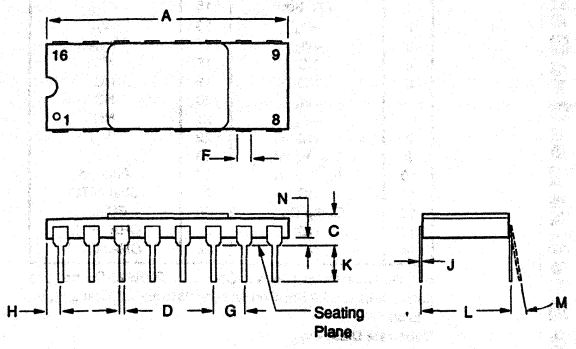
MECHANICAL

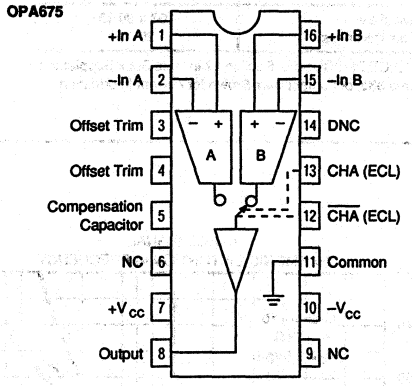
G Package — 16-Pin Hermetic DIP



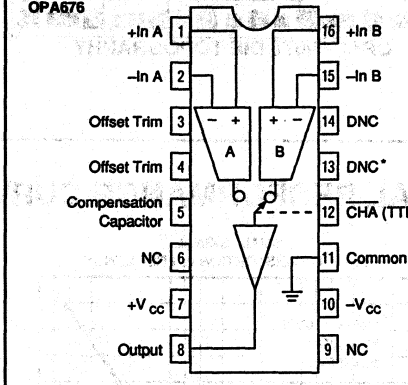
DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.790	.810	20.07	20.57
C	.105	.170	2.67	4.32
D	.015	.021	0.38	0.53
F	.048	.060	1.22	1.52
G	.100 BASIC		2.54 BASIC	
H	.030	.070	0.76	1.78
J	.008	.012	0.20	0.30
K	.120	.240	3.05	6.10
L	.300 BASIC		7.62 BASIC	
M	—	10°	—	10°
N	.025	.060	0.64	1.52

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.

OPA675



OPA676



*Capacitance on this node slows channel select.

PIN ASSIGNMENTS: OPA675

1	+In A	16	+In B
2	–In A	15	–In B
3	Offset Trim	14	DNC
4	Offset Trim	13	CHA (ECL)
5	Compensation Capacitor	12	CHA (ECL)
6	NC	11	Common
7	$+V_{cc}$	10	$-V_{cc}$
8	Output	9	NC

DNC = Do Not Connect NC = No Internal Connection

PIN ASSIGNMENTS: OPA676

1	+In A	16	+In B
2	–In A	15	–In B
3	Offset Trim	14	DNC
4	Offset Trim	13	DNC
5	Compensation Capacitor	12	CHA (TTL)
6	NC	11	Common
7	$+V_{cc}$	10	$-V_{cc}$
8	Output	9	NC

DNC = Do Not Connect NC = No Internal Connection

ABSOLUTE MAXIMUM RATINGS

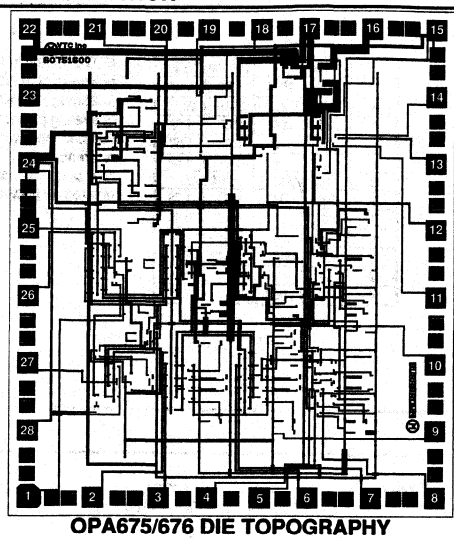
Supply	±7VDC
Differential Input Voltage	Total V_{cc}
Input Voltage Range (Analog and Digital)	$\pm V_{cc}$
Storage Temperature Range	–65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C
Output Short Circuit to Ground (+25°C)	Continuous to ground
Junction Temperature	+175°C

ORDERING INFORMATION

OPA675 ( ) ( )
OPA676 ( ) ( )

Basic Model Number
Performance Grade Code
J, K: 0°C to +70°C
S: –55°C to +125°C
Package Code
G: 16-pin Ceramic DIP

DICE INFORMATION



OPA675/676 DIE TOPOGRAPHY

PAD	FUNCTION	PAD	FUNCTION
1	TTL Set	15	$+V_{CC}$
2	$-In_B$	16	$+V_{CC}$
3	$+In_B$	17	V_{OUT}
4	NC	18	NC
5	NC	19	NC
6	$+In_A$	20	NC
7	$-In_A$	21	NC
8	NC	22	$-V_{CC}$
9	V_{OS} Adjust	23	$-V_{CC}$
10	V_{OS} Adjust	24	Ground
11	NC	25	CHA (TTL)
12	Comp Cap	26	ECL_{OUT}
13	NC	27	CHA (ECL)
14	NC	28	CHA (ECL)

NC: No Connection (Do Not Connect). **OPA675**-Do not use pads 1, 25, 26. **OPA676**-Connect pad 26 to pad 27. Connect pad 1 to pad 28.
Substrate Bias: $-V_{CC}$

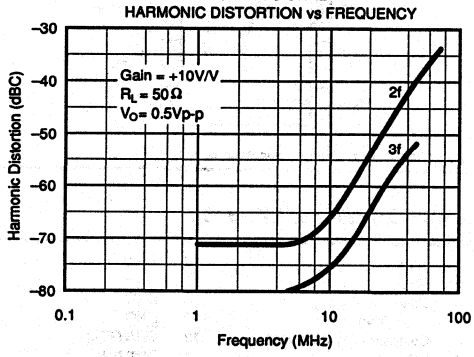
MECHANICAL INFORMATION

	MILS (0.001")
Die Size	103 x 90 ±5
Die Thickness	20 ±3

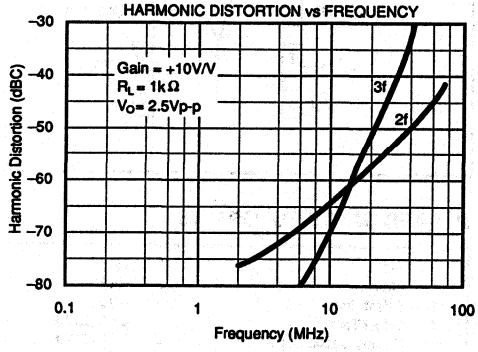
See "DICE PRODUCTS" Section 17 in Data Book Supplement Volume 33c, or contact Burr-Brown for current information.

TYPICAL PERFORMANCE CURVES

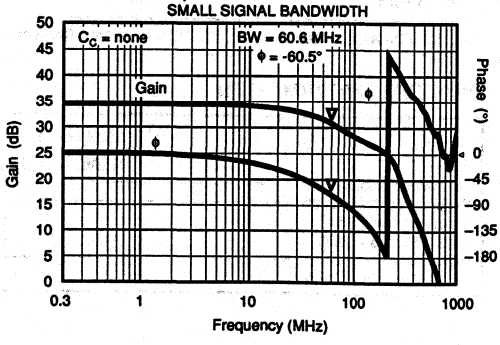
SMALL SIGNAL
HARMONIC DISTORTION vs FREQUENCY



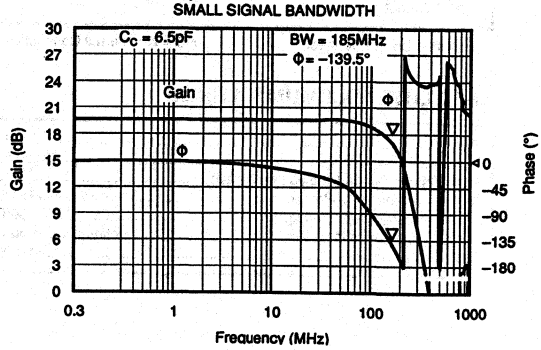
LARGE SIGNAL
HARMONIC DISTORTION vs FREQUENCY



A_V = +50V/V CLOSED-LOOP
SMALL SIGNAL BANDWIDTH

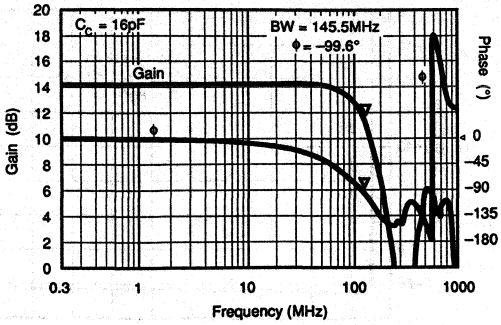


A_V = +10V/V CLOSED-LOOP
SMALL SIGNAL BANDWIDTH

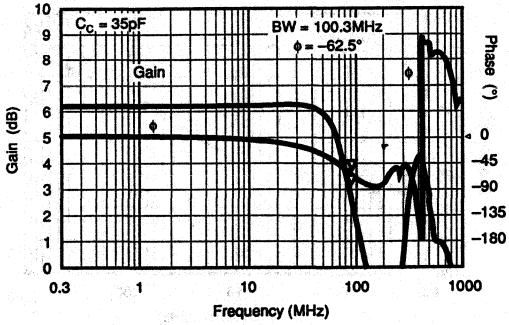


TYPICAL PERFORMANCE CURVES (CONT)

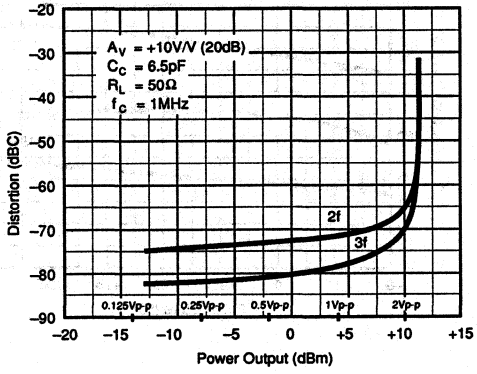
A_V = +5V/V CLOSED-LOOP
SMALL SIGNAL BAND WIDTH



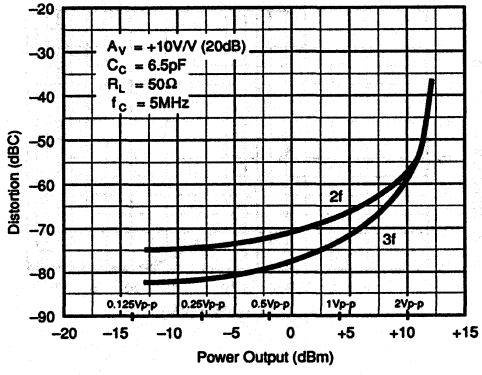
A_V = +2V/V CLOSED-LOOP
SMALL SIGNAL BAND WIDTH



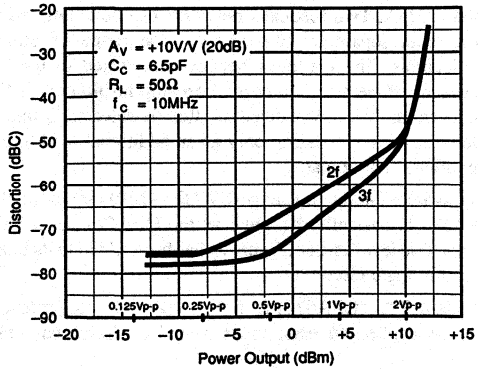
1MHz HARMONIC DISTORTION vs POWER OUTPUT



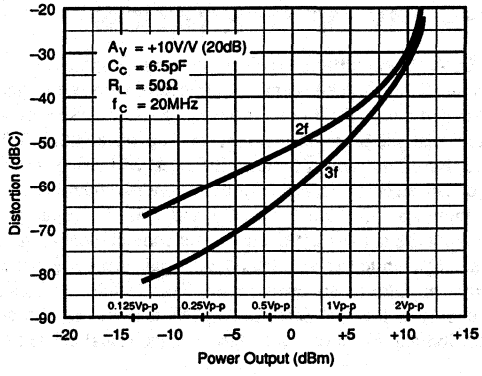
5MHz HARMONIC DISTORTION vs POWER OUTPUT



10MHz HARMONIC DISTORTION vs POWER OUTPUT

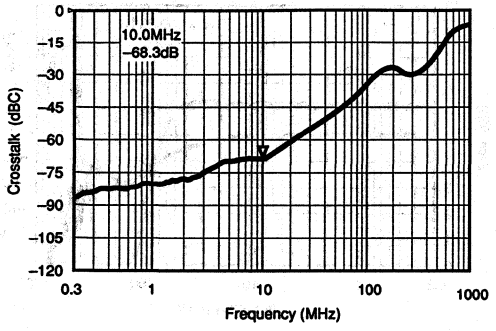


20MHz HARMONIC DISTORTION vs POWER OUTPUT

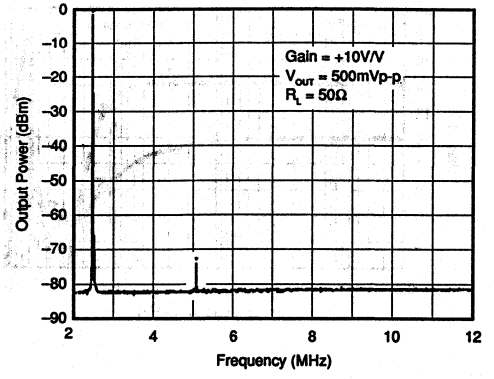


TYPICAL PERFORMANCE CURVES (CONT)

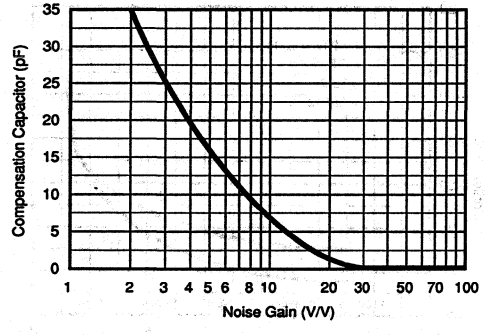
CHANNEL-TO-CHANNEL CROSSTALK vs FREQUENCY



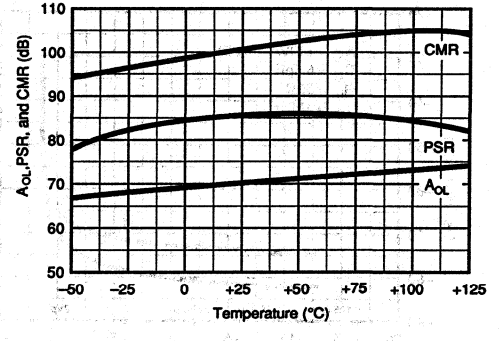
2.5MHz SMALL-SIGNAL HARMONIC DISTORTION SPECTRUM



NOMINAL FREQUENCY COMPENSATION vs NOISE GAIN



OPEN -LOOP GAIN, CMR AND PSR vs TEMPERATURE



THEORY OF OPERATION

An OPA675 simplified circuit is shown in Figure 1. It is a "classical" high-speed op-amp architecture with one important exception — the amplifier has two ECL logic selectable differential input stages. An appropriate differential ECL logic signal on A and $\overline{A}$ (labeled B Select) will turn on either Q5 or Q6, steering operating (tail) current to either differential input pair Q1 and Q2 or Q3 and Q4. The input pair receiving the tail current operates as a conventional op-amp input stage while the de-selected input pair receiving no tail current appears as an open circuit. The de-selected inputs have only a few pF parasitic capacitance and in the off condition exhibit only a very low leakage (bias) current of about 100pA. Two feedback networks can be connected to each input separately allowing a wide range of circuit applications. The feedback network connected to the selected input operates in a normal op amp fashion while the feedback network connected to the de-selected input is totally inactive, appearing only as an additional load to the amplifier's output stage.

The switched-input op amp (SWOP AMP) circuit of the OPA676 is basically the same as the OPA675 but a TTL compatible level shifter (Figure 2) has been added to its input selection logic circuit.

Standard TTL (OPA676) and ECL (OPA675) logic levels may be applied to each input selection circuit but only

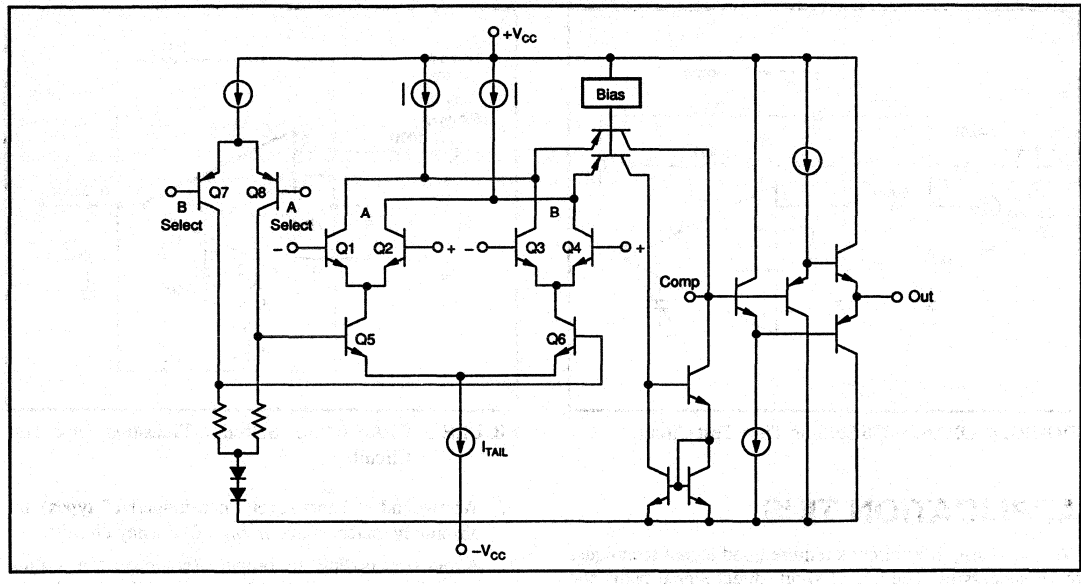


FIGURE 1. OPA675 Simplified Circuit Diagram.

350mV is typically required to switch between inputs. This logic input sensitivity allows simpler high-speed logic driver circuitry and it minimizes digital noise coupling into adjacent wideband analog circuitry and allows single ended ECL inputs to be used with V_{BB} applied to the other input.

The OPA675 and OPA676 are designed to be frequency compensated by a single capacitor connected from pin 5 to ground. Recommended compensation is shown in Typical Performance Curves. A small variable capacitor may be trimmed for best bandwidth, settling time, and gain peaking. This amplifier is designed for optimum performance in gains of 5V/V to 20V/V, but it can also be used over a far wider range of gains with excellent results. Closed-loop gain/phase (Bode) plots are shown in the Typical Performance Curves.

OFFSET TRIM

Input offset voltage is low enough for many video applications. If desired, offset voltage can be trimmed with a 1kΩ potentiometer connected to $+V_{CC}$. Trimming offset voltage in this manner will effect both input A and input B; independent control of input offset will require that trim adjust current be summed into one or both inputs. This technique is shown in a few applications circuits on the pages to follow.

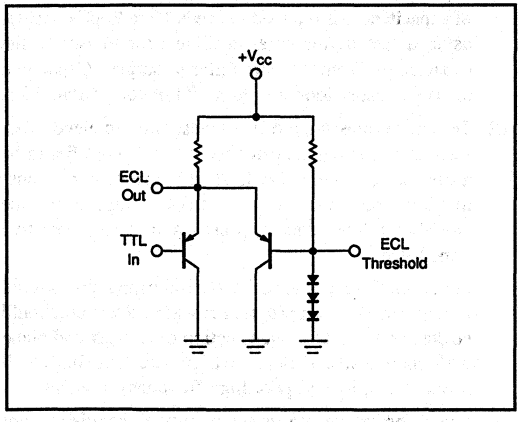


FIGURE 2. Internal OPA676 TTL Logic Level Shifter.

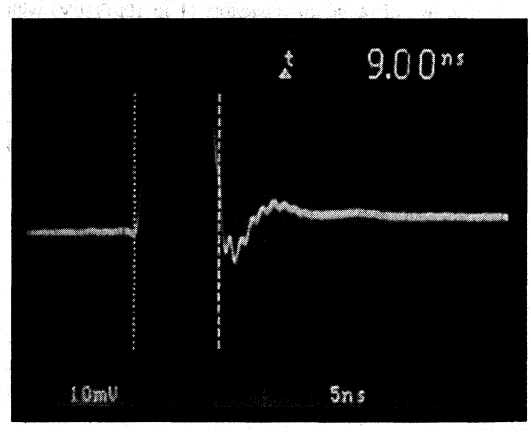


FIGURE 3. 1% Settling Time.

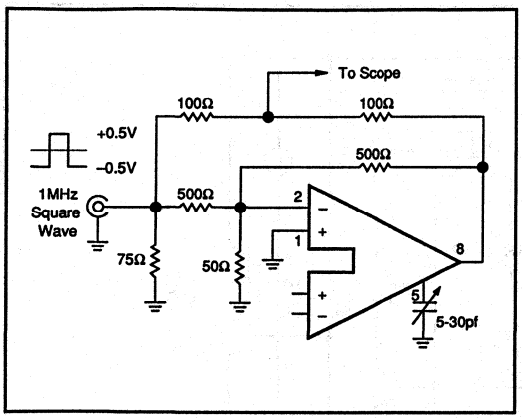


FIGURE 4. OPA675/676 Settling Time Test Circuit.

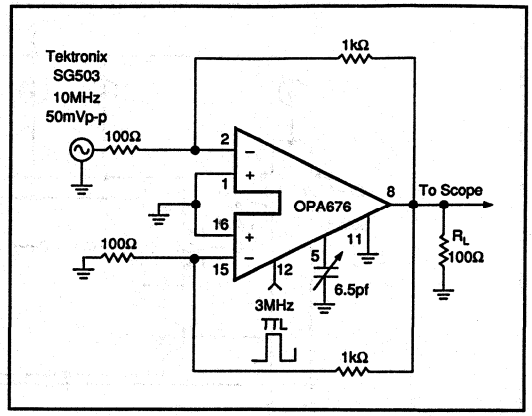


FIGURE 5. OPA676 Input Selection Transition Time Test Circuit.

APPLICATION TIPS

Wideband amplifier circuits require good layout techniques to be successful. The use of short, direct signal paths and heavy (2oz copper recommended) ground planes are absolutely necessary to achieve the performance level inherent in the OPA675/676. Oscillation, ringing, poor bandwith and settling, gain peaking, and instability are typical problems that plague all high-speed amplifiers when they are used in poor layouts. The OPA675 and OPA676 are no different in this respect — any amplifier with a gain bandwith product of a few GHz requires some care be taken in its application.

Points to remember:

1. Use a heavy copper ground plane on the component side of your PC board. This provides a low inductance ground and it also conducts heat from active circuit package pins into ambient air by convection.
2. Bypass power supply pins directly at the active device. The use of tantalum capacitors (1 to 10μF/10V) with very short leads is highly recommended. Supply pins should not be left unbypassed.
3. Signal paths should be short and direct. Feedback resistors, compensation capacitors, termination resistors, etc. should have lead lengths no longer than 1/4 inch (6cm).
4. Surface mount components (chip resistors, capacitors, etc.) have low inductance and are therefore recommended. Parasitic inductance and capacitance should be avoided if best performance is to be achieved.
5. Resistors used in feedback networks should have values of a few hundred ohms for best performance. Shunt capacitance problems limit the acceptable range to about 1kΩ or on the high resistance end and to a value that is within the amplifier's output drive limits on the low end. Metal film and carbon compensation resistors will be satisfactory.
6. Wirewound resistors (even "non-inductive" types) are absolutely unacceptable in high frequency circuits.
7. Avoid overloading the output. Remember that output current must be provided by the amplifier to drive its own feedback network as well as to drive its "load." Lowest distortion is achieved with high impedance loads.
8. PC board traces for signal and power lines should be wide to reduce impedance or inductance.
9. Don't forget that these amplifiers use ±5V supplies. Although they will operate perfectly well with +5V and –5.2V, the use of ±15V supplies will result in destruction.
10. Standard commercial test equipment has not been designed to test devices in the OPA675/676 speed range. Benchtop op amp testers and ATE systems will require a special test head to successfully test these amplifiers.
11. High-speed amplifiers can drive only a limited amount of capacitance. If the load exceeds 10 to 20pF consider using a fast buffer or a small resistor to isolate the capacitance from the amplifier's output. Capacitive loads will cause loop instability if not compensated for.
12. Terminate transmission line loads. Unterminated lines, such as coaxial cable, can appear to the amplifier to be a capacitive or inductive load. By terminating a transmission line with its characteristic impedance, the amplifier's load then appears as a purely resistive impedance.
13. For clean, fast input selection the logic input pins should be terminated with appropriate resistors. Resistors should be connected from input selection pins to ground plane with short leads. Failure to terminate long lines will result in ringing and poor high frequency switching.
14. Plug-in prototype boards and wire-wrap boards will not be satisfactory. A clean layout using RF techniques is required; there is no shortcut.

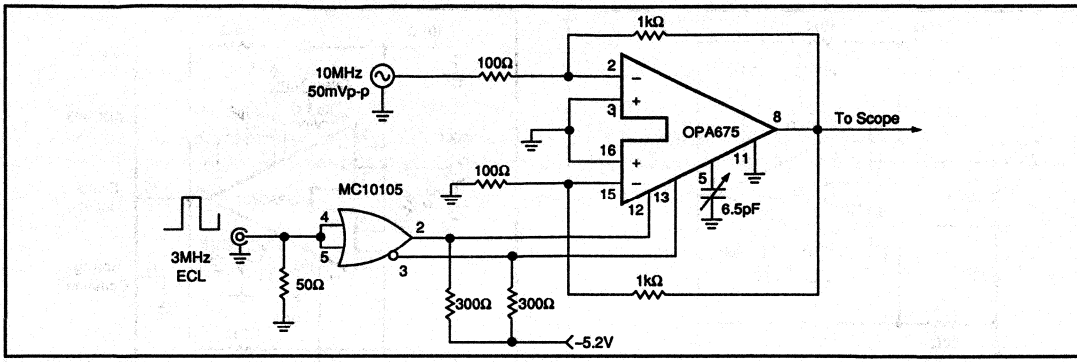


FIGURE 6. OPA675 Input Selection Transition Time Test Circuit.

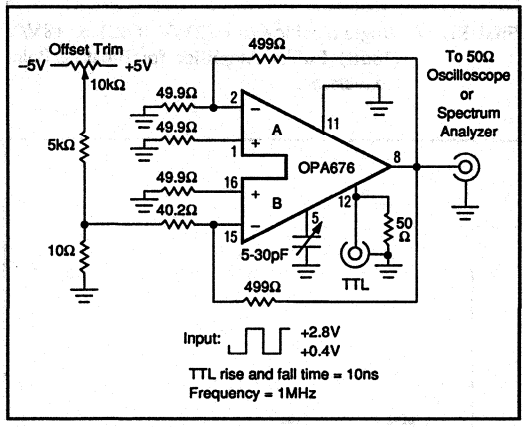


FIGURE 7. OPA676 Carrier Feedthrough and Switching Transient Test Circuit.

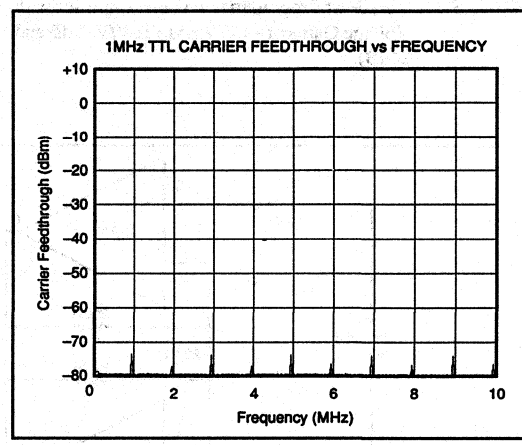


FIGURE 9. Carrier Feedthrough from 1MHz TTL Logic. Offset Trimmed for Maximum Carrier Rejection

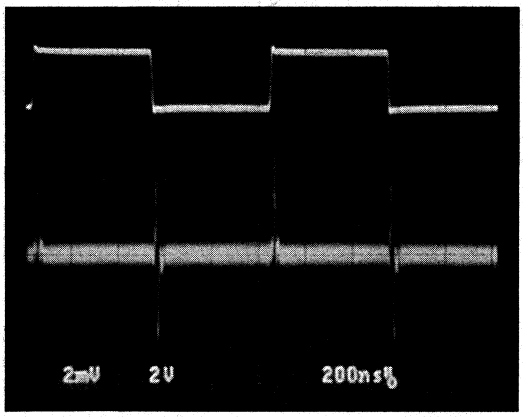


FIGURE 8. OPA676 Switching Transient. Top Trace: TTL Input (2V/cm). Bottom Trace: Amplifier Output (2mV/cm). Input B Offset Voltage has been Trimmed to Match Input A Offset Voltage.

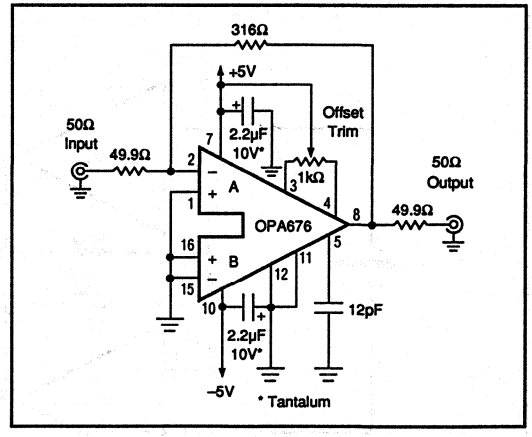


FIGURE 10. OPA676 Used as a Conventional Op Amp: A 10dB Gain Wideband Video Amplifier with 50Ω Input/Output Impedance.

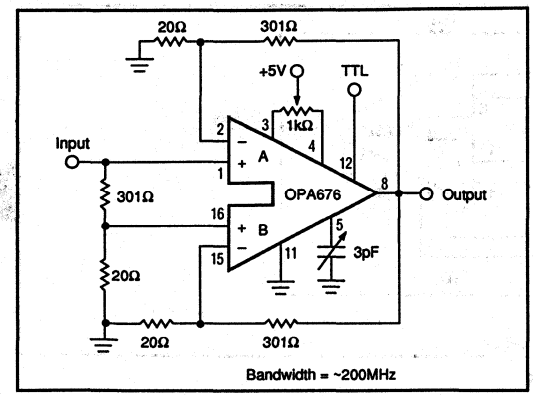


FIGURE 11. Very Fast Programmable Gain Amplifier with Voltage Gains of +1V/V and +16V/V (0dB and 24dB).

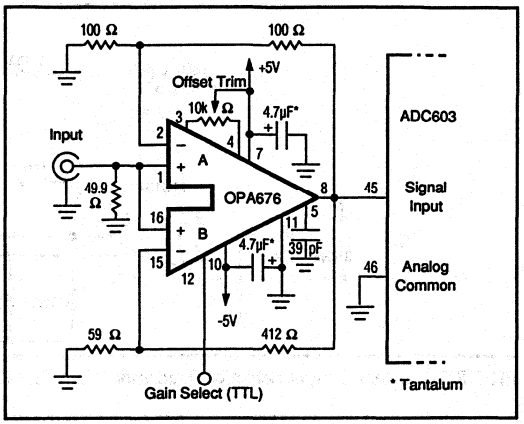


FIGURE 12. Programmable-Gain +2V/V (6dB) or +8V/V (18dB) Buffer Amplifier for Floating-Point Conversion.

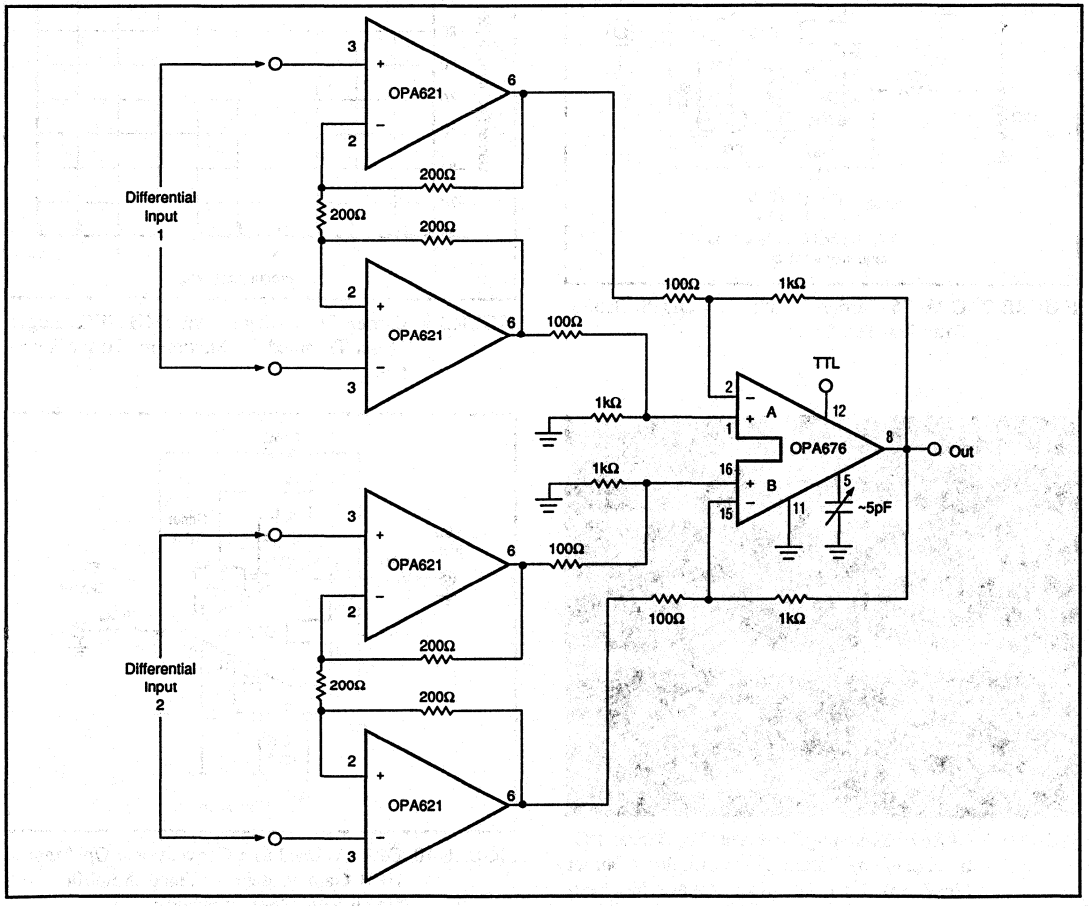


FIGURE 13. High Input Impedance Differential Input Multiplexer with Gain of 30V/V (30dB).

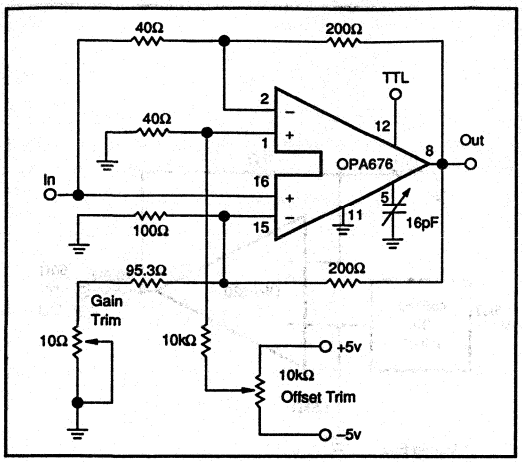


FIGURE 14. Synchronous Modulator/Demodulator with Carrier Balance Trim (Gain = ±5V/V).

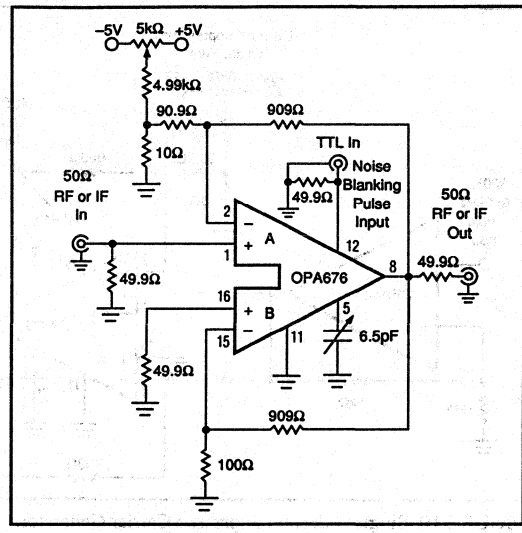


FIGURE 16. Receiver Noise Blanker: A Wideband Gated Video Amplifier.

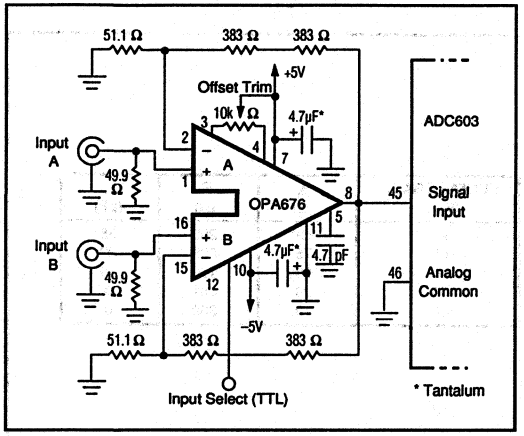


FIGURE 15. Multiplexed Input +16V/V Gain (24dB) Buffer Amplifier.

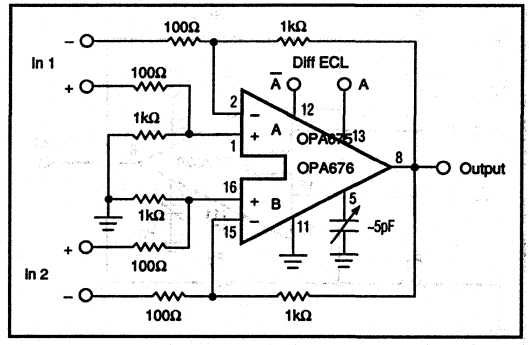
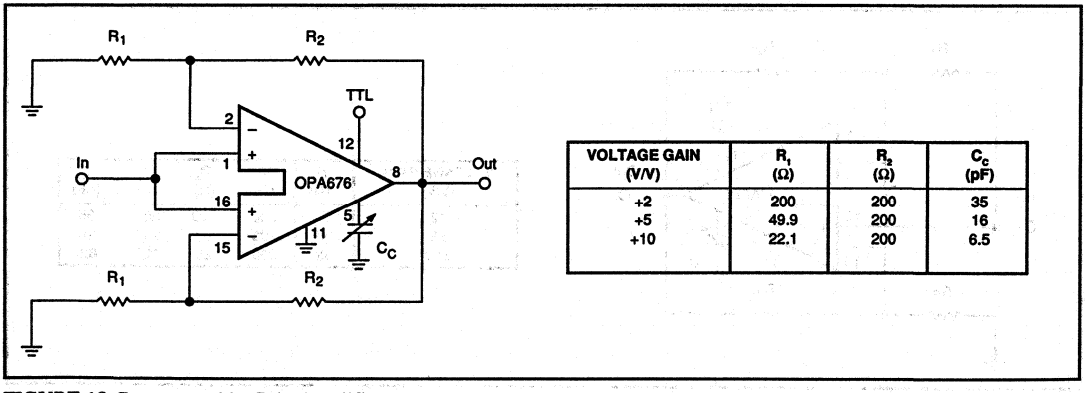


FIGURE 17. Differential Input Multiplexer with Gain of 10V/V (20dB).



VOLTAGE GAIN (V/V)	R_1 (Ω)	R_2 (Ω)	C_C (pF)
+2	200	200	35
+5	49.9	200	16
+10	22.1	200	6.5

FIGURE 18. Programmable-Gain Amplifier.

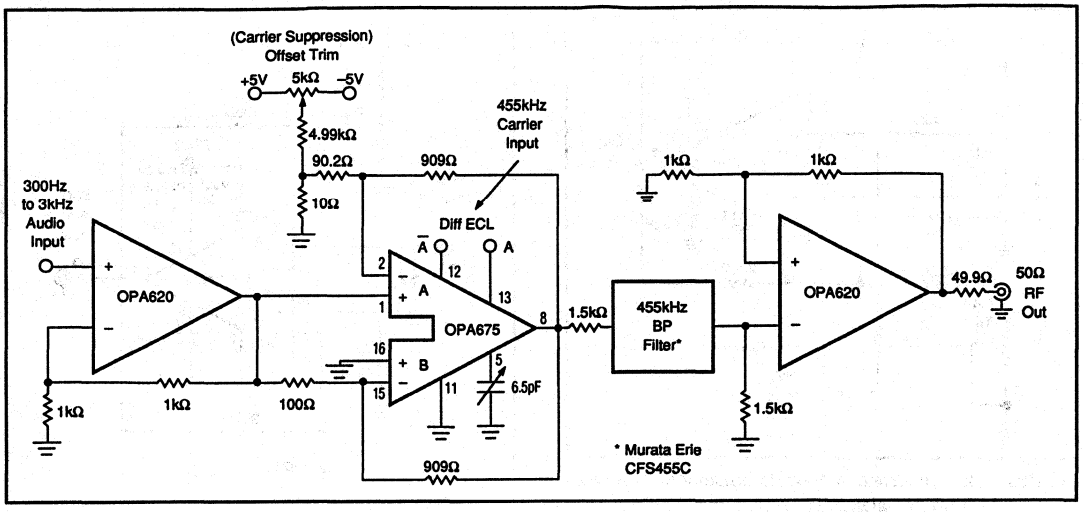
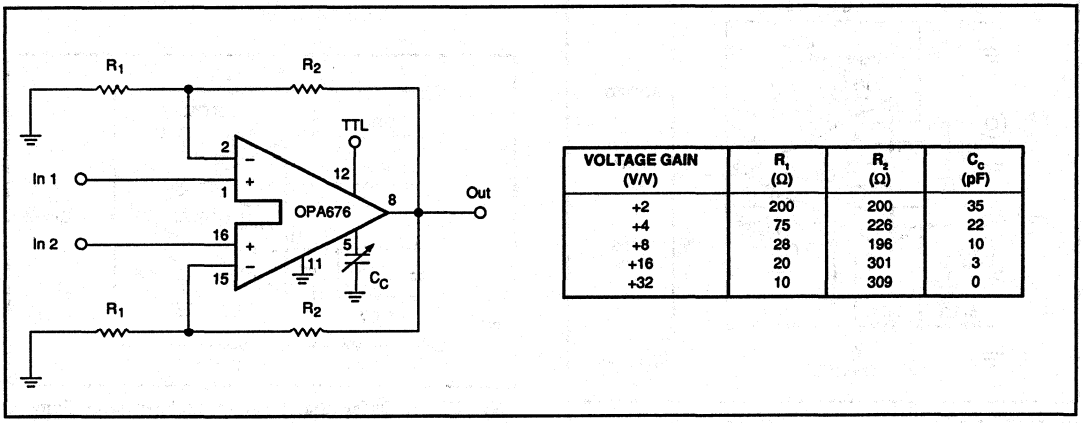
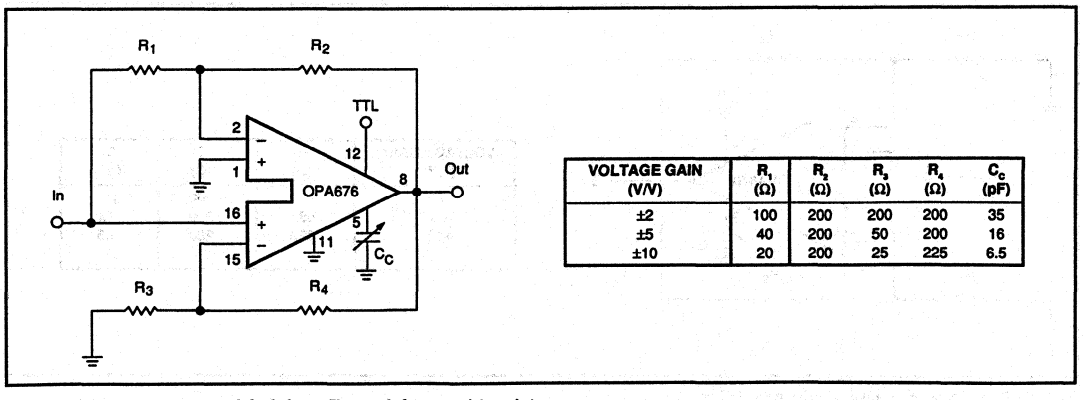


FIGURE 19. Single Sideband Supressed Carrier Generator.



VOLTAGE GAIN (V/V)	R_1 (Ω)	R_2 (Ω)	C_C (pF)
+2	200	200	35
+4	75	226	22
+8	28	196	10
+16	20	301	3
+32	10	309	0

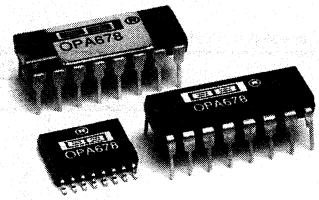
FIGURE 20. Two-Input Multiplexer (with gain).



VOLTAGE GAIN (V/V)	R_1 (Ω)	R_2 (Ω)	R_3 (Ω)	R_4 (Ω)	C_C (pF)
±2	100	200	200	200	35
±5	40	200	50	200	16
±10	20	200	25	225	6.5

FIGURE 21. Synchronous Modulator/Demodulator (with gain).

BURR-BROWN®



OPA678

**ADVANCED INFORMATION
SUBJECT TO CHANGE**

Wideband Switched-Input OPERATIONAL AMPLIFIER

FEATURES

- FAST SETTLING: 9ns (1%)
- WIDE BANDWIDTH: 200MHz
- LOW OFFSET VOLTAGE: ±380µV
- TWO LOGIC SELECTABLE INPUTS
- FAST INPUT SWITCHING: 4ns
- ACCEPTS TTL/ECL SWITCHING SIGNALS
- UNITY GAIN STABLE
- 16-PIN DIP AND SOIC PACKAGES

APPLICATIONS

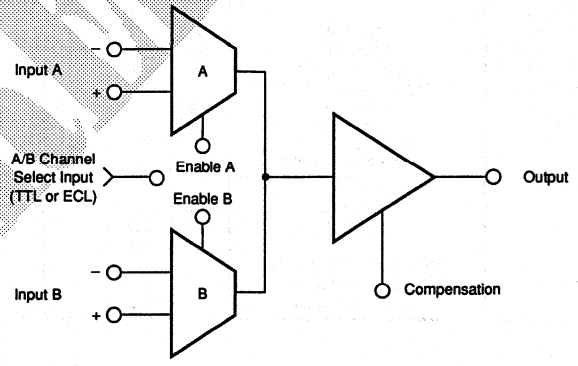
- VIDEO AMPLIFICATION SWITCHING
- FAST 2-INPUT MULTIPLEXER
- PULSE/RF AMPLIFIERS
- PROGRAMMABLE-GAIN AMPLIFIER
- ACTIVE FILTERS
- SYNCHRONOUS DEMODULATOR

DESCRIPTION

The OPA678 is a wideband monolithic operational amplifier with two independent differential inputs. Either input can be selected by an external TTL or ECL logic signal. The amplifier is externally compensated and features a very fast input selection speed, 4ns for either ECL or TTL. This amplifier features fully symmetrical differential inputs due to its "classical" operational amplifier circuit architecture. Unlike "current-feedback" amplifier designs, the OPA678 may be used in all op amp applications requiring high speed and precision.

Low distortion and crosstalk make this amplifier suitable for RF and video applications.

The OPA678 is available in DIP, SOIC, and Sidebraze packages. A military temperature range part is available in the Sidebraze package.



PRELIMINARY

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Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL

At V_{CC} = ±5VDC, R_L = 150Ω, C_{COMP} = 5pF, and T_A = +25°C unless otherwise noted.

PARAMETER	CONDITIONS	OPA678AG/AP/AU MIN	OPA678AG/AP/AU TYP	OPA678AG/AP/AU MAX	OPA678SG MIN	OPA678SG TYP	OPA678SG MAX	UNITS
INPUT NOISE[1]								
Voltage: f_O = 10Hz	R_S = 0Ω		27			*		nV/√Hz
f_O = 100Hz			10			*		nV/√Hz
f_O = 1kHz			3.8			*		nV/√Hz
f_O = 10kHz			2.6			*		nV/√Hz
f_O = 100kHz			2.4			*		nV/√Hz
f_B = 10Hz to 10MHz			7.9			*		µVrms
Current: f_O = 10Hz to 1MHz			2.7			*		pA/√Hz
OFFSET VOLTAGE[1]								
Input Offset Voltage	V_{CM} = 0VDC		±380	±1.5mV		±380	±1mV	µV
Average Drift	$T_A = T_{MIN}$ to T_{MAX}		±3	±10		±3	±5	µV/°C
Supply Rejection	$±V_{CC}$ = 4.5V to 5.5V	65	71		*	*		dB
BIAS CURRENT[1]								
Input Bias Current	V_{CM} = 0VDC		14	50		*	*	µA
OFFSET CURRENT[1]								
Input Offset Current	V_{CM} = 0VDC		0.2	2		*	1.5	µA
INPUT IMPEDANCE[1]								
Differential			25k || 2			*		Ω || pF
Common-Mode			10^6 || 5			*		Ω || pF
INPUT VOLTAGE RANGE[1]								
Common-Mode Input Range		2.0	±2.5		*	*		V
Common-Mode Rejection	V_{IN} = ±0.5VDC, V_O = ±1.25V	75	85		*	*		dB
OPEN LOOP GAIN, DC[1]								
Open-Loop Voltage Gain		50	60		*	*		dB
FREQUENCY RESPONSE								
Closed-Loop Bandwidth	Gain = +1V/V, C_C = 9pF		200			*		MHz
	Gain = +2V/V, C_C = 7pF		100			*		MHz
	Gain = +5V/V, C_C = 0pF		50			*		MHz
	Gain = +10V/V, C_C = 0pF		25			*		MHz
Crosstalk	Gain = +1V/V, f = 100kHz		–100			*		dBC[2]
	f = 1MHz		–80			*		dBC
	f = 10MHz		–68			*		dBC
	f = 100MHz		–35			*		dBC
Harmonic Distortion: 10MHz	G = +1V/V, R_L = 150Ω, V_O = 0.5Vp-p							
	Second Harmonic		–63			*		dBC
	Third Harmonic		–82			*		dBC
Large Signal Response[3]	V_O = 2.5Vp-p, Gain = +1V/V	25	45		*	*		MHz
Slew Rate	Gain = +1V/V	250	350		*	*		V/µs
Settling Time: 1%			9			*		ns
0.1%	Gain = +1V/V		15			*		ns
0.01%	0.625V Output Step		25			*		ns
INPUT SELECTION[4]								
Transition Time	ECL: Operation		4	8		*	9	ns
50% In to 50% Out	TTL: Operation		4	8		*	9	ns
DIGITAL INPUT								
TTL Logic Levels: V_{IL}	Logic "LO"	0		+0.8	*		*	V
V_{IH}	Logic "HI"	+2.0		+5	*		*	V
I_{IL}	Logic "LO", V_{IL} = 0V		–0.05	–0.2		*	*	mA
I_{IH}	Logic "HI", V_{IH} = +2.7V		1	20		*	*	µA
ECL Logic Levels: V_{IL}	Logic "LO"	–1.81		–1.475	*		*	V
V_{IH}	Logic "HI"	–1.15		– 0.88	*		*	V
I_{IL}	Logic "LO", V_{IL} = –1.6V		–50	–100		*		µA
I_{IH}	Logic "HI", V_{IH} = –1.0V		–50	–100		*		µA
RATED OUTPUT								
Voltage Output	R_L = 150Ω	±2.5	±3.75		*	*		V
	R_L = 50Ω	+1.5	+2.0		*	*		V
Current Output			±40			*		mA
Output Resistance	1MHz, Open Loop, C_C = 5pF		5			*		Ω
Load Capacitance Stability, C_C = 10pF	Gain = +1V/V		17			*		pF
Short Circuit Current	Continuous to Gnd		+45			±45		mA

PREVIEW

SPECIFICATIONS (CONT)

ELECTRICAL

At V_{CC} = ±5VDC, R_L = 150Ω, C_{COMP} = 5pF, and T_A = +25°C unless otherwise noted.

PARAMETER	CONDITIONS	OPA678AG/AP/AU MIN	OPA678AG/AP/AU TYP	OPA678AG/AP/AU MAX	OPA678SG MIN	OPA678SG TYP	OPA678SG MAX	UNITS
POWER SUPPLY								
Rated Voltage	±V_{CC}		5			*		VDC
Derated Performance	±V_{CC}	4.5		5.5	*		*	VDC
Current, Quiescent	I_O = 0mADC		26	30		*	*	mA
TEMPERATURE RANGE								
Specification	Ambient Temp AG, AP, AU	–40		+85	*		*	°C
	SG	–55		+125				°C
Operating:	Ambient Temp AP, AU, AG, SG	–55		+125	*		*	°C
θ_{JA}			125			*		°C/W

* Same specifications as for OPA678AG/AP/AU.

ELECTRICAL (FULL TEMPERATURE RANGE SPECIFICATIONS)

At V_{CC} = ±5VDC, R_L = 150Ω, C_{COMP} = 5pF, and T_A = T_{MIN} to T_{MAX} unless otherwise noted.

PARAMETER	CONDITIONS	OPA678AG/AP/AU MIN	OPA678AG/AP/AU TYP	OPA678AG/AP/AU MAX	OPA678SG MIN	OPA678SG TYP	OPA678SG MAX	UNITS
TEMPERATURE RANGE								
Specification	Ambient Temp AG/AP/AU	–40		+85	*		*	°C
	SG				–55		+125	°C
OFFSET VOLTAGE								
Input Offset Voltage	T_A = T_{MIN} to T_{MAX}		600	±1.5mV		*	±2mV	µV
Supply Rejection	±V_{CC} = 4.5V to 5.5V	60	70		**	73		dB
BIAS CURRENT								
Input Bias Current	V_{CM} = 0VDC		15	85		*	*	µA
OFFSET CURRENT								
Input Offset Current	V_{CM} = 0VDC		0.2	5		*	7	µA
INPUT VOLTAGE RANGE								
Common-Mode Input Range		±2.0	±2.5		*	*		V
Common-Mode Rejection	V_{IN} = ±0.5VDC, V_O = ±1.25V	60	80		*	*		dB
OPEN LOOP GAIN, DC								
Open-Loop Voltage Gain		50	60		*	*		dB
DIGITAL INPUT								
TTL Logic Levels: V_{IL}	Logic "LO"	0		+0.8	*		*	V
V_{IH}	Logic "HI"	+2.0		+5	*		*	V
I_{IL}	Logic "LO", V_{IL} = 0V		–0.08	–0.4		*	*	mA
I_{IH}	Logic "HI", V_{IH} = +2.7V		5	50		*	*	µA
ECL Logic Levels: V_{IL}	Logic "LO"	–1.81		–1.475	*		*	V
V_{IH}	Logic "HI"	–1.15		–0.88	*		*	V
I_{IL}	Logic "LO", V_{IL} = –1.6V		–50			*		µA
I_{IH}	Logic "HI", V_{IH} = –1.0V		–50			*		µA
RATED OUTPUT								
Voltage Output	R_L = 150Ω	±2.5	±3.75		*	*		V
	R_L = 50Ω	±1.7	±2.2		±1.5	*		V
POWER SUPPLY								
Current, Quiescent	I_O = 0mADC		25	35		*	*	mA

* Same specifications as for AG/AP/AU.

NOTES: (1) Specifications are for both inputs (A and B). (2) dBC = Level referred to carrier-input signal. (3) Large Signal Response is calculated from the formula $LSBW = \frac{SR}{2\pi V_{PEAK}}$. (4) Switching time from application of digital logic signal to input signal selection.

ABSOLUTE MAXIMUM RATINGS

Supply	±7VDC
Differential Input Voltage	Total V_{CC}
Input Voltage Range (Analog and Digital)	±V_{CC}
Storage Temperature Range	–65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C
Output Short Circuit to Ground (+25°C)	Continuous to ground
Junction Temperature	+175°C

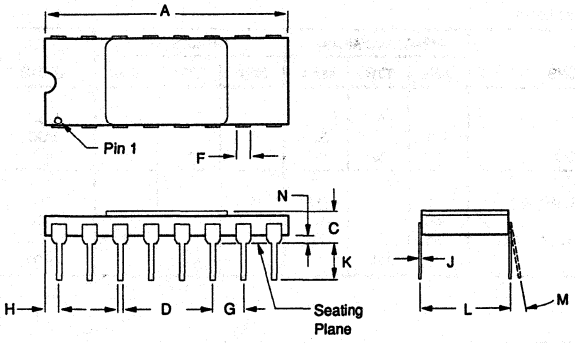
ORDERING INFORMATION

OPA678 ( ) ( )

- Basic Model Number
- Performance Grade Code
  - A: –40°C to +85°C
  - S: –55°C to +125°C
- Package Code
  - G: 16-pin Ceramic DIP
  - P: 16-pin Plastic DIP
  - U: 16-pin SOIC

MECHANICAL

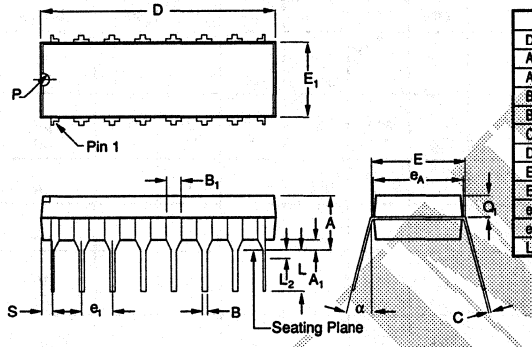
G Package — 16-Pin Hermetic DIP



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.790	.810	20.07	20.57
C	.105	.170	2.67	4.32
D	.015	.021	0.38	0.53
F	.038	.065	0.97	1.65
G	.100 BASIC		2.54 BASIC	
H	.030	.070	0.76	1.78
J	.008	.012	0.20	0.30
K	.125	.200	3.18	5.08
L	.300 BASIC		7.62 BASIC	
M	—	10°	—	10°
N	.025	.060	0.64	1.52

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

P Package — 16-Pin Plastic, Single-Wide DIP



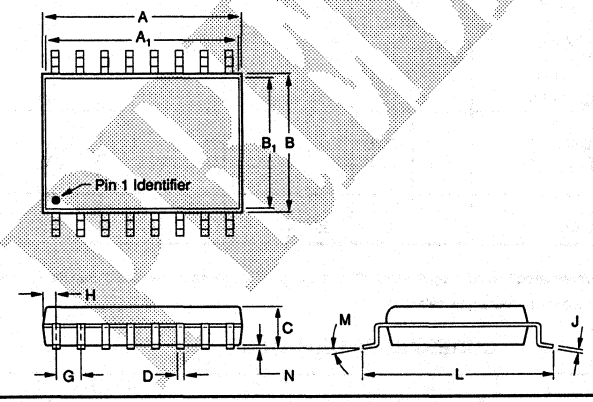
DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.155	.200	3.94	5.08
A1(1)	.015	.050	0.38	1.27
B	.014	.020	0.36	0.51
B1	.035	.065	0.89	1.65
C	.008	.012	0.20	0.30
D	.745	.785	19.00	19.94
E	.300	.325	7.62	8.26
E1	.240	.260	6.10	6.60
e1	.100 BASIC		2.54 BASIC	
eA	.300 BASIC		7.62 BASIC	
L	.125	.150	3.18	3.81

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
L2(4)	.000	.030	0.00	0.76
α	0°	15°	0°	15°
N(2)	16		16	
N1(3)	0		0	
P	.015	.050	0.38	1.27
Q1	.040	.075	1.02	1.91
S	.015	.060	0.38	1.52

(1) Not JEDEC Std.
(2) N = Total number of pins.
(3) N_1 = Total number of missing pins
(4) e_1 and e_A applies in zone L_2 when unit installed.

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

U Package — 16-Pin SOIC



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.400	.416	10.16	10.57
A1	.388	.412	9.86	10.46
B	.286	.302	7.26	7.67
B1	.268	.286	6.81	7.26
C	.093	.109	2.36	2.77
D	.015	.020	0.38	0.51
G	.050 BASIC		1.27 BASIC	
H	.022	.038	0.56	0.97
J	.008	.012	0.20	0.30
L	.391	.421	9.93	10.69
M	5° TYP		5° TYP	
N	.000	.012	0.00	0.30

NOTE: Leads in true position within 0.010" (0.25mm) R at MMC at seating plane.

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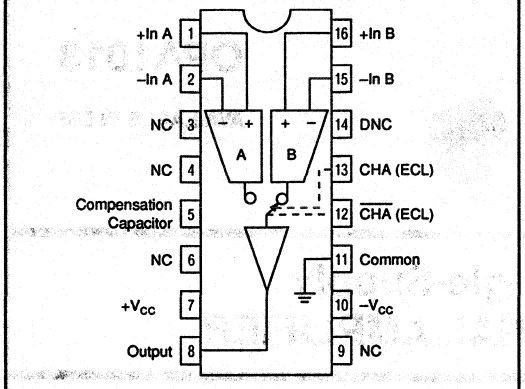
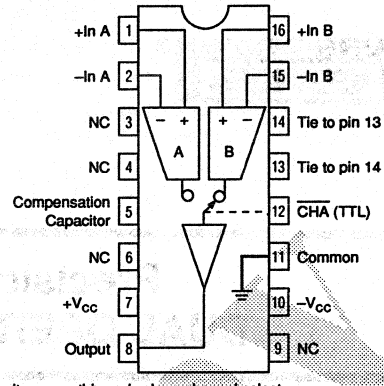
Pin Assignments for ECL Channel Switching



Pin assignments for TTL Channel Switching



*Capacitance on this node slows channel select.

PRELIMINARY

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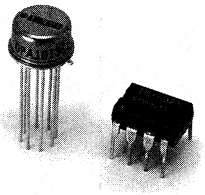


OPA1013

AVAILABLE IN DIE

Precision, Single-Supply DUAL OPERATIONAL AMPLIFIER

FEATURES

- SINGLE POWER SUPPLY OPERATION
- INPUT VOLTAGE RANGE TO GROUND
- OUTPUT SWINGS NEAR GROUND
- LOW QUIESCENT CURRENT: 500μA max
- LOW V_{os}: 150μV max
- LOW DRIFT: 2μV/°C max
- LOW I_{os}: 0.8nA max
- LOW NOISE: 0.55μVp-p, 0.1Hz to 10Hz

APPLICATIONS

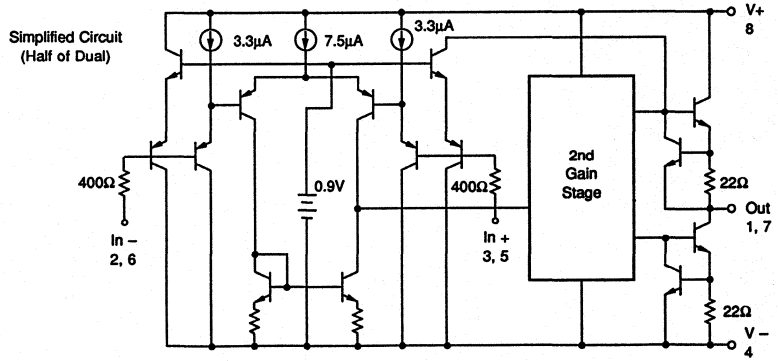
- PRECISION INSTRUMENTATION
- BATTERY-POWERED EQUIPMENT
- BRIDGE AMPLIFIERS
- 4-20mA CURRENT TRANSMITTERS
- VOLTAGE COMPARATOR

DESCRIPTION

The OPA1013 dual operational amplifier provides precision performance in single power supply and low power applications. It is laser trimmed for low offset voltage and drift, greatly reducing the large errors common with LM324-type op amps. Input offset current is also trimmed to reduce errors in high impedance applications.

The OPA1013 is characterized for operation at both +5V (single supply) and ±15V power supplies. When operated from a single supply, the input common-mode range includes ground and the output can swing to within 15mV of ground. Completely independent biasing networks eliminate interaction between the two amplifiers—even when one is used as a comparator.

The OPA1013 is available in 8-pin plastic DIP and metal TO-99 packages, specified for the 0°C to 70°C and –55°C to 125°C temperature ranges.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL

V_S = ±15V, V_{CM} = 0V, T_A = +25°C unless otherwise noted.

PARAMETER	CONDITION	OPA1013AM/AC			OPA1013M/C/DN8			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage			±15	±150		±50	±300	µV
	OPA1013DN8					±200	±800	µV
Time Stability			0.4			0.5		µV/Mo
Input Offset Current			±0.045	±0.8		±0.08	±1.5	nA
Input Bias Current			6	20		7	30	nA
Voltage Noise, BW = 0.1 to 10Hz			0.55			0.55		μV_{p-p}
Noise Density, f = 10Hz			28			28		$nV/\sqrt{Hz}$
f = 1kHz			25			25		$nV/\sqrt{Hz}$
Current Noise Density, f = 10Hz			0.12			0.12		$pA/\sqrt{Hz}$
Input Resistance: Differential		100	400		70	300		MΩ
Input Resistance: Common-Mode			5			4		GΩ
Open-Loop Voltage Gain	V_O = ±10V, R_L = 2kΩ	1.5	3.1		1.2	2.9		V/µV
	V_O = ±10V, R_L = 600Ω	0.8	2.1		0.5	1.9		V/µV
Common-Mode Input Range		+13.5	+13.8		+13.5	+13.8		V
		−15	−15.3		−15	−15.3		V
Common-Mode Rejection	V_{CM} = +13.5 to −15V	100	117		97	114		dB
Power Supply Rejection	V_S = ±2 to ±18V	103	120		100	117		dB
Channel Separation	V_O = ±10V, R_L = 2kΩ	123	140		120	137		dB
Voltage Output	R_L = 2kΩ	±13	±14		±12.5	±14		V
Slew Rate		0.2	0.35		0.2	0.35		V/µs
Quiescent Current (per amplifier)			±0.35	±0.5		±0.35	±0.55	mA

V_S = +5V/0V, V_{CM} = 0V, V_O = +1.4V, T_A = +25°C unless otherwise noted.

PARAMETER	CONDITION	OPA1013AM/AC			OPA1013M/C/DN8			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage			±60	±250		±90	±450	µV
	OPA1013DN8					±250	±950	µV
Input Offset Current			±0.2	±1.3		±0.3	±2.0	nA
Input Bias Current			9	35		10	50	nA
Open-Loop Voltage Gain	V_O = 5mV to 4V		0.1			0.1		V/µV
	R_L = 500Ω							
Common-Mode Input Range		+3.5	+3.8		+3.5	+3.8		V
		0	−0.3		0	−0.3		V
Voltage Output Low	No Load		15	25		15	25	mV
Low	R_L = 600Ω to Ground		5	10		5	10	mV
Low	I_{SINK} = 1mA		200	350		200	350	mV
High	No Load	4	4.4		4	4.4		V
High	R_L = 600Ω to Ground	3.4	4		3.4	4		V
Quiescent Current (per amplifier)			0.31	0.45		0.33	0.5	mA

T_A = −55°C to +125°C, V_S = ±15V, V_{CM} = 0V unless otherwise noted.

PARAMETER	CONDITION	OPA1013AM			OPA1013M			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage			±80	±300		±110	±550	µV
	V_S = +5/0V, V_O = +1.4V							
	T_A = 100°C		±70	±450		±75	±750	µV
	V_{CM} = 0.1V, T_A = 125°C		±100	±450		±150	±750	µV
	V_{CM} = 0V, T_A = 125°C		±200	±900		±300	±1500	µV
Input Offset Voltage Drift			0.4	2.0		0.5	2.5	µV/°C
Input Offset Current			±0.3	±2.5		±0.4	±5.0	nA
	V_S = +5/0V, V_O = +1.4V		±0.6	±6		±0.9	±10	nA
Input Bias Current			7	30		9	45	nA
	V_S = +5/0V, V_O = +1.4V		11	80		15	120	nA
Open-Loop Voltage Gain	V_O = ±10V, R_L = 2kΩ	0.5	2.0		0.25	2.0		V/µV
Common-Mode Rejection	V_{CM} = +13 to −14.9V	97	114		94	113		dB
Power Supply Rejection	V_S = ±2 to ±18V	100	117		97	116		dB
Voltage Output	R_L = 2kΩ	±12	±13.8		±11.5	±13.8		V
V_O Low	V_S = +5/0V, R_L = 600Ω		6	15		6	18	mV
V_O High	V_S = +5/0V, R_L = 600Ω	3.2	3.8		3.1	3.8		V
Quiescent Current (per amplifier)			±0.38	±0.6		±0.38	±0.7	mA
	V_S = +5/0V, V_O = +1.4V		0.34	0.55		0.34	0.65	mA

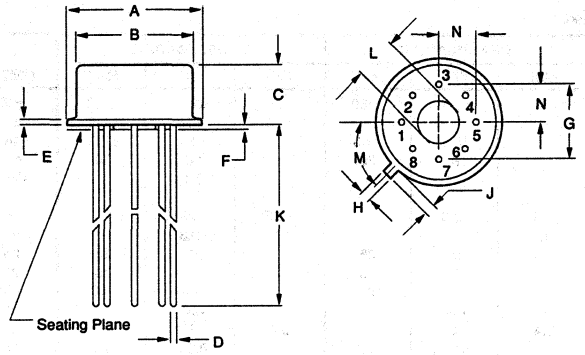
SPECIFICATIONS

T_A = 0°C to +70°C, V_S = ±15V, V_{CM} = 0V unless otherwise noted.

PARAMETER	CONDITION	OPA1013AC MIN	OPA1013AC TYP	OPA1013AC MAX	OPA1013C/DN8 MIN	OPA1013C/DN8 TYP	OPA1013C/DN8 MAX	UNITS
Input Offset Voltage			±55	±240		±80	±400	µV
	OPA1013DN8					±230	±1000	µV
	V_S = +5/0V, V_O = +1.4V		±75	±350		±110	±570	µV
	OPA1013DN8					±280	±1200	µV
Input Offset Voltage Drift			0.3	2		0.4	2.5	µV/°C
	OPA1013DN8					0.7	5	µV/°C
Input Offset Current			±0.2	±1.5		±0.3	±2.8	nA
	V_S = +5/0V, V_O = +1.4V		±0.4	±3.5		±0.5	±6	nA
Input Bias Current			7	25		9	38	nA
	V_S = +5/0V, V_O = +1.4V		10	55		13	90	nA
Open-Loop Voltage Gain	V_O = ±10V, R_L = 2kΩ	1	2.5		0.7	2.2		V/µV
Common-Mode Rejection	V_{CM} = +13 to −15V	98	116		94	113		dB
Power Supply Rejection	V_S = ±2 to ±18V	101	119		97	116		dB
Voltage Output	R_L = 2kΩ	±12.5	±13.9		±12.0	±13.9		V
V_O Low	V_S = +5/0V, R_L = 600Ω		6	13		6	13	mV
V_O High	V_S = +5/0V, R_L = 600Ω	3.3	3.9		3.2	3.9		V
Quiescent Current (per amplifier)			±0.36	±0.55		±0.37	±0.6	mA
	V_S = +5/0V, V_O = +1.4V		0.32	0.50		0.34	0.55	mA

MECHANICAL

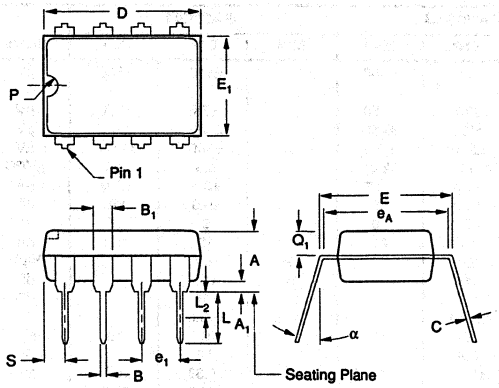
H Package — Metal TO-99



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.335	.370	8.51	9.40
B	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.200 BASIC		5.08 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500	—	12.7	—
L	.110	.160	2.79	4.06
M	45° BASIC		45° BASIC	
N	.095	.105	2.41	2.67

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.

N8 Package — 8-Pin Plastic DIP



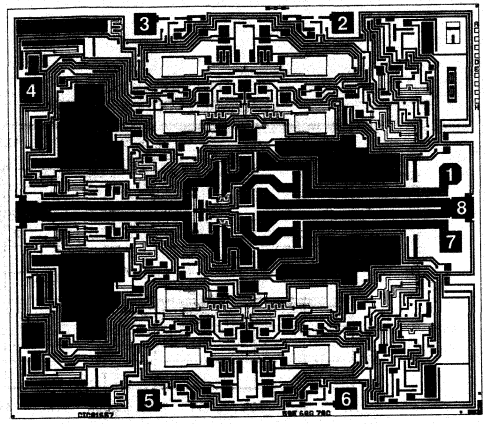
DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.155	.200	3.94	5.08
A1	.020	.050	0.51	1.27
B	.014	.020	0.36	0.51
B1	.045	.065	1.14	1.65
C	.008	.012	0.20	0.30
D (1)	.370	.400	9.40	10.16
E	.300	.325	7.62	8.26
E1	.240	.260	6.10	6.60
e1	.100 BASIC		2.54 BASIC	
eA	.300 BASIC		7.62 BASIC	
L	.125	.150	3.18	3.81

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
L2 (2)	0	.030	0.00	0.76
α	0°	15°	0°	15°
P	.015	.050	0.38	1.270
Q1	.040	.075	1.02	1.91
S (1)	.015	.050	0.38	1.27

(1) Not JEDEC Std.
(2) e1 and e_A applies in zone L_2 when unit installed.

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

DICE INFORMATION



OPA1013 DIE TOPOGRAPHY

PAD	FUNCTION
1	Output A
2	–In A
3	+In A
4	V–
5	+In B
6	–In B
7	Output B
8	V+

Substrate Bias: $-V_S$

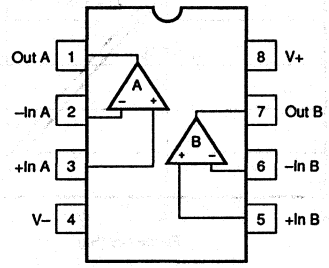
MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	112 x 100 ±5	2.84 x 2.54 ±0.13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.10 x 0.10
Backing	Gold	

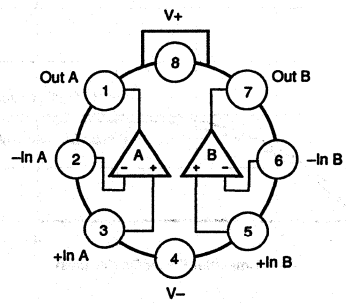
See "DICE PRODUCTS" Section 17 in Data Book Supplement Volume 33c, or contact Burr-Brown for current information.

CONNECTION DIAGRAMS

N8 — Plastic Package — Top View



H — TO-99 Metal — Top View



ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE
OPA1013CN8	Plastic DIP	0°C to +70°C
OPA1013DN8	Plastic DIP	0°C to +70°C
OPA1013ACH	TO-99 Metal	0°C to +70°C
OPA1013CH	TO-99 Metal	0°C to +70°C
OPA1013AMH	TO-99 Metal	–55°C to +125°C
OPA1013MH	TO-99 Metal	–55°C to +125°C

ABSOLUTE MAXIMUM RATINGS

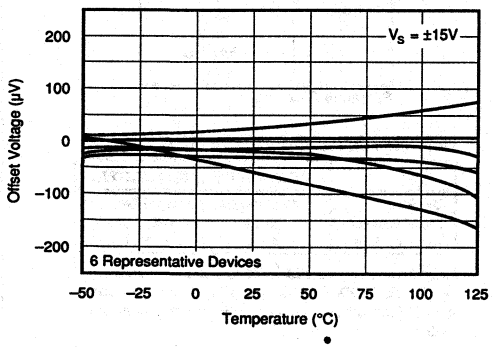
Power Supply Voltage	±22V
Differential Input Voltage	±30V
Input Voltage	V+ to (V–) –5V
Output Short Circuit (T_A = 25°C)	Continuous
Operating Temperature:	
OPA1013AM, OPA1013M	–55 to +125°C
OPA1013AC, OPA1013C, OPA1013D	0 to +70°C
Storage Temperature	–65 to +150°C
Lead Temperature (soldering, 10s)	+300°C

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

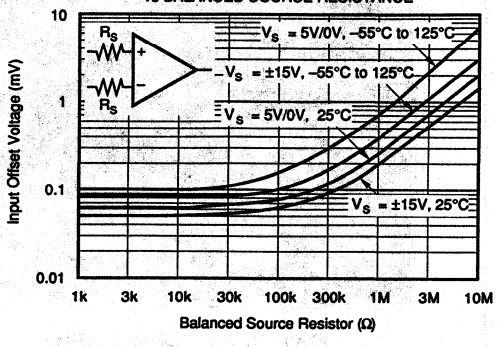
TYPICAL PERFORMANCE CURVES

T_A = +25°C unless otherwise noted.

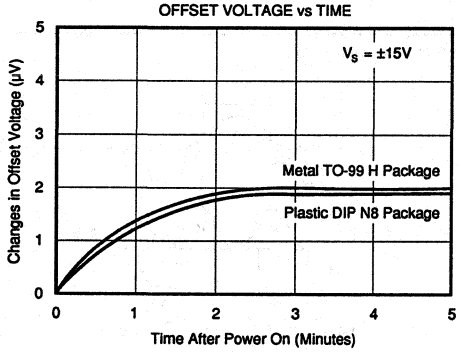
OFFSET VOLTAGE vs TEMPERATURE



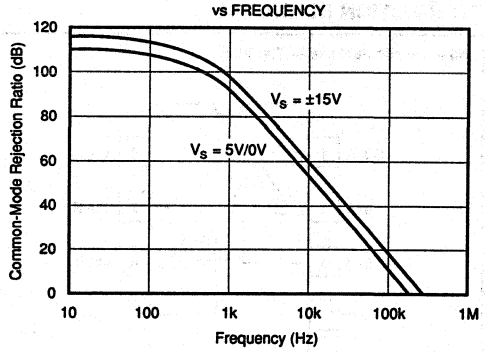
OFFSET VOLTAGE vs BALANCED SOURCE RESISTANCE



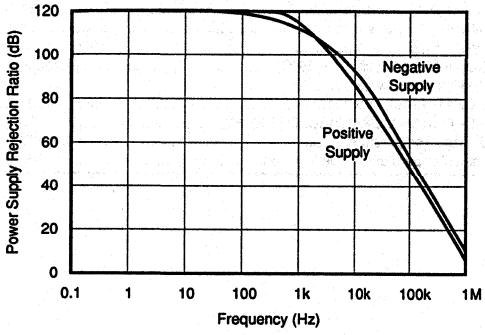
OFFSET VOLTAGE vs TIME



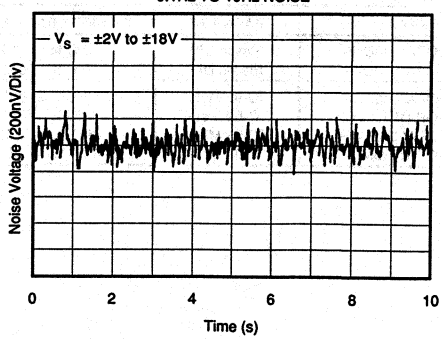
COMMON-MODE REJECTION RATIO vs FREQUENCY



POWER SUPPLY REJECTION RATIO vs FREQUENCY



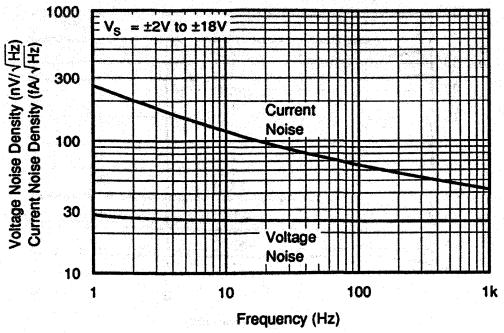
0.1Hz TO 10Hz NOISE



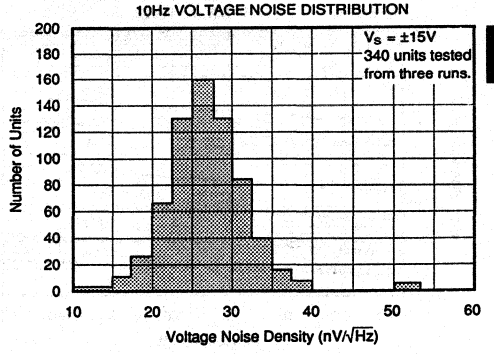
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C unless otherwise noted.

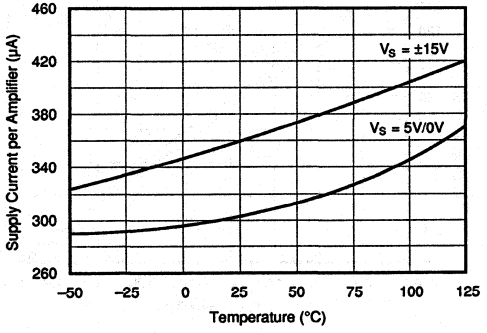
NOISE DENSITY vs FREQUENCY



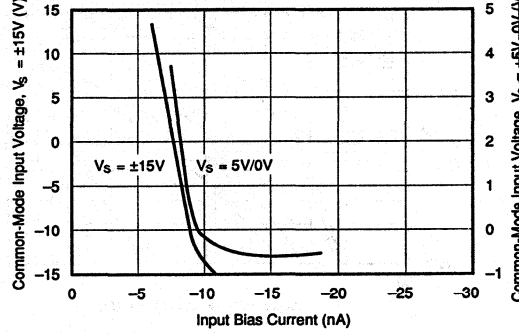
10Hz VOLTAGE NOISE DISTRIBUTION



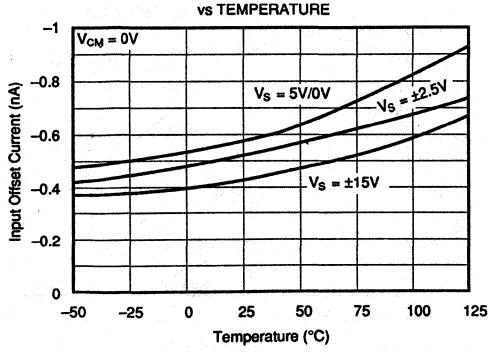
SUPPLY CURRENT vs TEMPERATURE



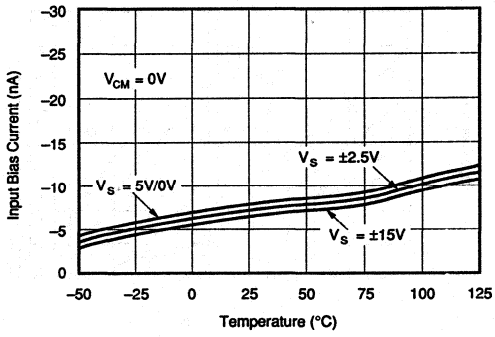
INPUT BIAS CURRENT
vs COMMON-MODE VOLTAGE



INPUT OFFSET CURRENT
vs TEMPERATURE



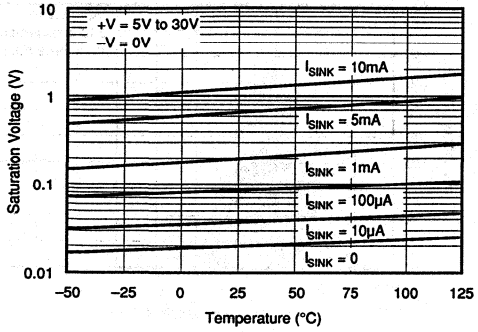
INPUT BIAS CURRENT
vs TEMPERATURE



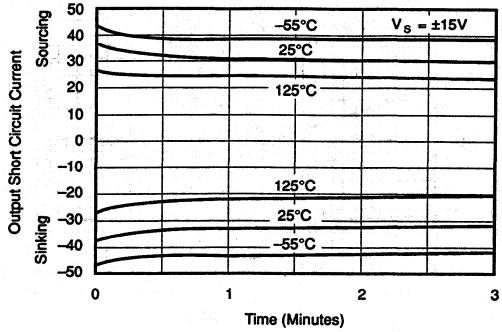
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C unless otherwise noted.

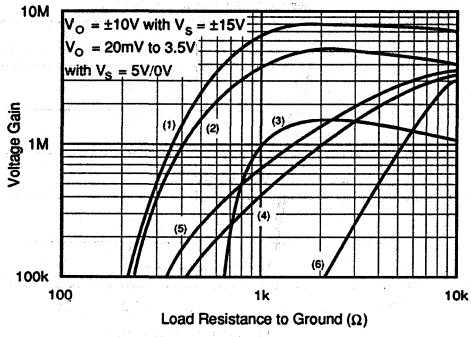
OUTPUT SATURATION AND SINK CURRENT vs TEMPERATURE



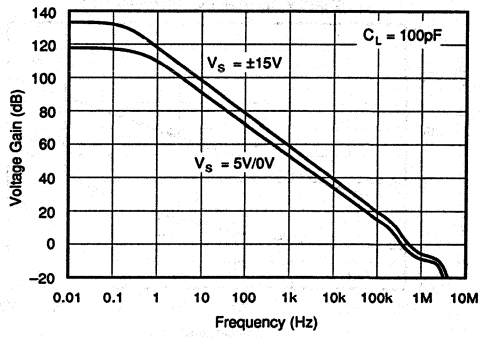
OUTPUT SHORT CIRCUIT CURRENT vs TIME



VOLTAGE GAIN vs LOAD RESISTANCE

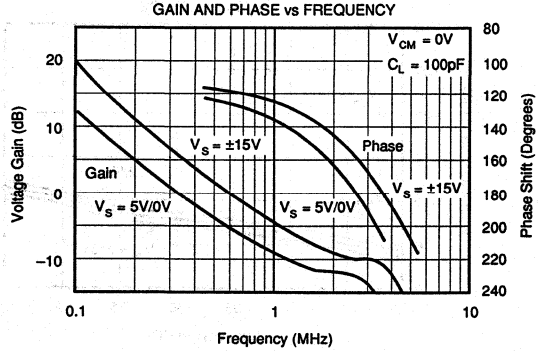


VOLTAGE GAIN vs FREQUENCY

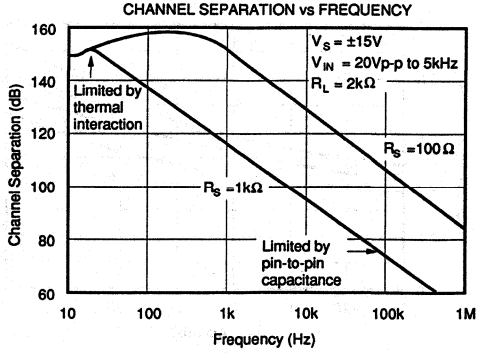


NOTES: (1) T_A = –55°C, V_S = ±15V. (2) T_A = +25°C, V_S = ±15V. (3) T_A = 125°C, V_S = ±15V. (4) T_A = +25°C, V_S = 5V/0V. (5) T_A = –55°C, V_S = 5V/0V. (6) T_A = 125°C, V_S = 5V/0V.

GAIN AND PHASE vs FREQUENCY

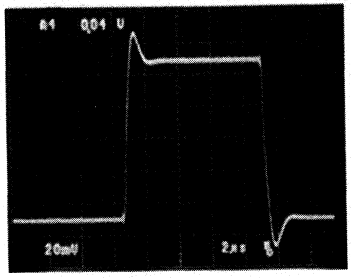


CHANNEL SEPARATION vs FREQUENCY

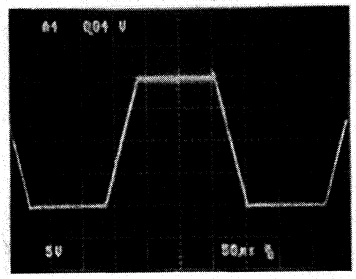


TYPICAL PERFORMANCE CURVES (CONT)

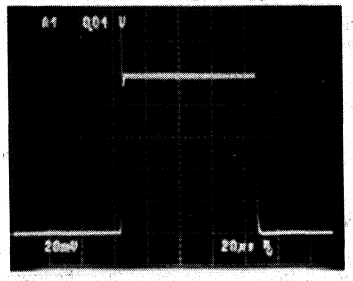
SMALL SIGNAL TRANSIENT RESPONSE
V_S = ±15V, G = +1



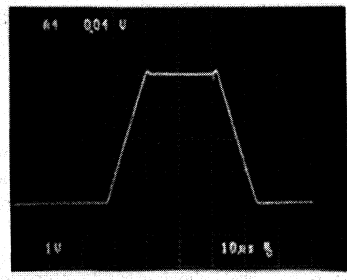
LARGE SIGNAL TRANSIENT RESPONSE
V_S = ±15V, G = +1



SMALL SIGNAL TRANSIENT RESPONSE
V_S = 5V/0V, G = +1, R_L = 600Ω to Ground

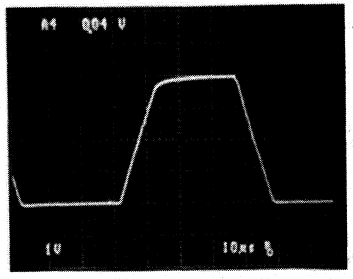


LARGE SIGNAL TRANSIENT RESPONSE
V_S = 5V/0V, G = +1, R_L = 4.7kV to 5V



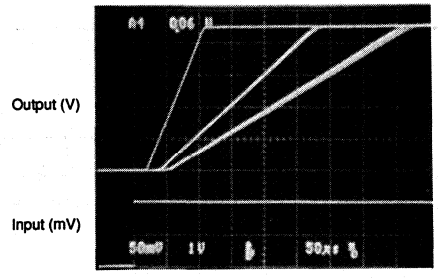
Input = 0V to 4V Pulse

LARGE SIGNAL TRANSIENT RESPONSE
V_S = 5V/0V, G = +1, No Load



Input = 0V to 4V Pulse

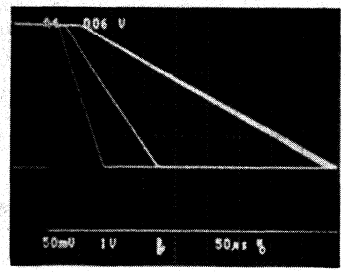
COMPARATOR RISE RESPONSE TIME
10mV, 5mV, 2mV Overdrives



V_S = 5V/0V

TYPICAL PERFORMANCE CURVES (CONT)

COMPARATOR FALL RESPONSE TIME
10mV, 5mV, 2mV Overdrives



V_S = 5V/0V

APPLICATIONS INFORMATION

The OPA1013 is unity-gain stable, making it easy to use and free from oscillations in the widest range of circuitry. Follow good design practice by bypassing the power supplies close to the op amp pins. In most cases 0.1µF ceramic capacitors are adequate.

SINGLE POWER SUPPLY OPERATION

The OPA1013 is specified for operation from a single power supply. This means that linear operation continues with the input terminals at (or even somewhat below) ground potential. When used in a non-inverting amplifier, 0V input must produce 0V output. In practice, the output swing is limited to approximately 15mV above ground with no load. Output swing near ground can be optimized when the output load is connected to ground. If the output must sink current, the ability to swing near ground will be diminished. The output swings to within approximately 200mV of ground when sinking 1mA.

INPUT PROTECTION

The circuitry of the OPA1013 is protected against overload for input voltages ranging from the positive supply voltage to 5V below the negative supply voltage (below ground in single supply operation). No external protection circuitry is required, as it is with other common single-supply op amps.

Furthermore, the OPA1013 is free from phase-reversal problems common with other single-supply op amps. When the inputs are driven below ground (or below the negative power supply), the output polarity remains correct.

COMPARATOR OPERATION

The OPA1013 functions well as a comparator, where high speed is not required. Sometimes, in fact, the low offset and docile characteristics of the OPA1013 may simplify the design of comparator circuitry. The two op amps in the OPA1013 use completely independent bias circuitry to avoid interaction when the inputs are over-driven. Driving one op amp into saturation will not affect the characteristics of the other amplifier. The outputs of the OPA1013 can drive one TTL load. Quiescent current remains stable when the inputs are overdriven.

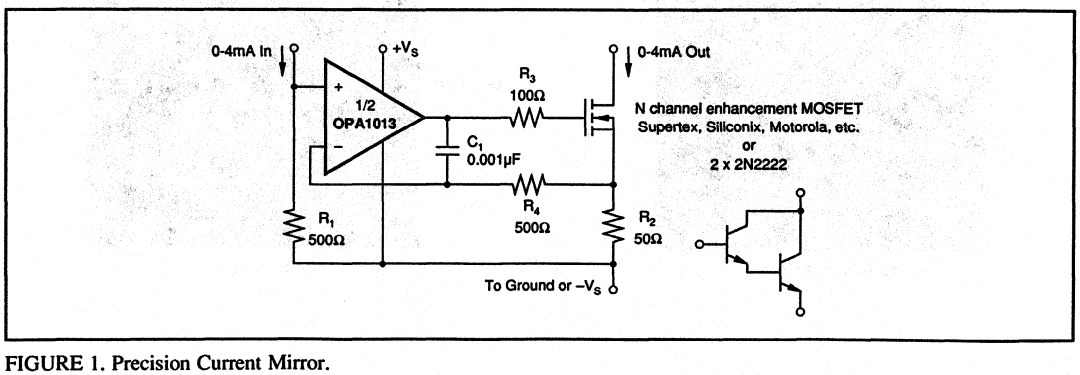


FIGURE 1. Precision Current Mirror.

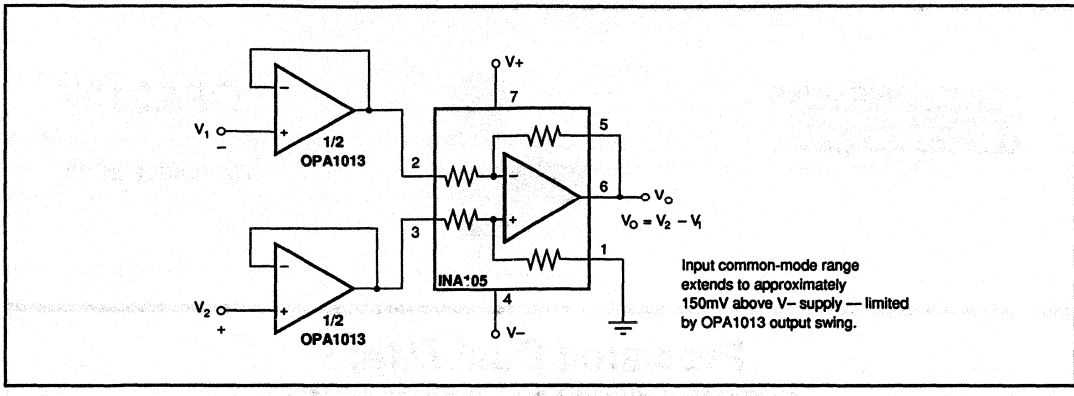


FIGURE 2. Instrumentation Amplifier.

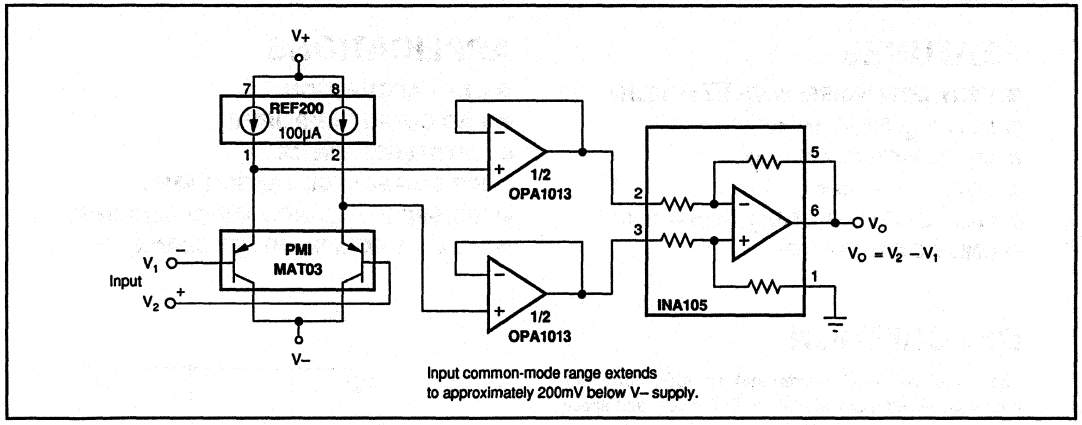


FIGURE 3. Instrumentation Amplifier.

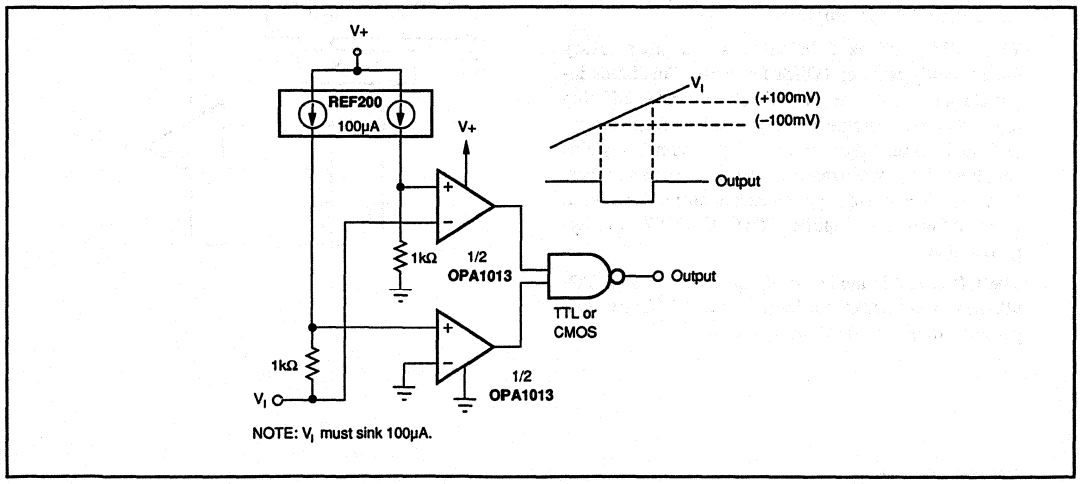
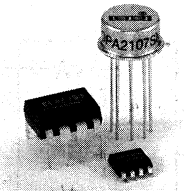


FIGURE 4. Window Comparator.

BURR-BROWN®



OPA2107

AVAILABLE IN DIE

Precision Dual *Difet* ® OPERATIONAL AMPLIFIER

FEATURES

- VERY LOW NOISE: 8nV/√Hz at 10kHz
- LOW V_{OS}: 500µV max
- LOW DRIFT: 5µV/°C max
- LOW I_B: 5pA max
- FAST SETTLING TIME: 2µs to 0.01%
- UNITY-GAIN STABLE

APPLICATIONS

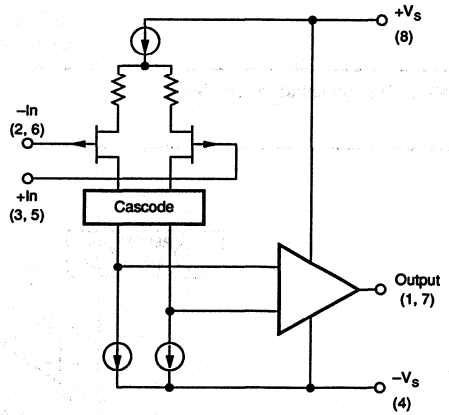
- DATA ACQUISITION
- DAC OUTPUT AMPLIFIER
- OPTOELECTRONICS
- HIGH-IMPEDANCE SENSOR AMPS
- HIGH-PERFORMANCE AUDIO CIRCUITRY
- MEDICAL EQUIPMENT, CT SCANNERS

DESCRIPTION

The OPA2107 dual operational amplifier provides precision ***Difet*** performance with the cost and space savings of a dual op amp. It is useful in a wide range of precision and low-noise analog circuitry and can be used to upgrade the performance of designs currently using BIFET® type amplifiers.

The OPA2107 is fabricated on a proprietary dielectrically isolated (***Difet***) process. This holds input bias currents to very low levels without sacrificing other important parameters, such as input offset voltage, drift and noise. Laser-trimmed input circuitry yields excellent DC performance. Superior dynamic performance is achieved, yet quiescent current is held to under 2.5mA per amplifier. The OPA2107 is unity-gain stable.

The OPA2107 is available in plastic DIP, metal TO-99, and SOIC packages. Industrial and Military temperature range versions are available.



Difet® Burr-Brown Corp.
BIFET® National Semiconductor

International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

PDS-863A

SPECIFICATIONS

T_A = +25°C, V_S = ±15V unless otherwise noted.

PARAMETER	CONDITION	OPA2107AM, SM, AP, AU			OPA2107BM			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
OFFSET VOLTAGE[1]								
Input Offset Voltage	V_{CM} = 0V		100	1mV		50	500	µV
Over Specified Temperature			0.5	2		0.2	1	mV
SM Grade			0.8	2.5				mV
Average Drift Over Specified Temperature			3	10		2	5	µV/°C
Power Supply Rejection	V_S = ±10 to ±18V	80	96		84	100		dB
INPUT BIAS CURRENT[1]								
Input Bias Current	V_{CM} = 0V		4	10		2	5	pA
Over Specified Temperature			0.25	1.5		0.15	1	nA
SM Grade			4	35				nA
Input Offset Current	V_{CM} = 0V		1	8		0.5	3	pA
Over Specified Temperature				1			0.5	nA
SM Grade			1	28				nA
INPUT NOISE								
Voltage: f = 10Hz	R_S = 0		30			•		nV/√Hz
f = 100Hz			12			•		nV/√Hz
f = 1kHz			9			•		nV/√Hz
f = 10kHz			8			•		nV/√Hz
BW = 0.1 to 10Hz			1.2			•		µVp-p
BW = 10 to 10kHz			0.85			•		µVrms
Current: f = 0.1Hz thru 20kHz			1.2			0.9		fA/√Hz
BW = 0.1Hz to 10Hz			23			17		fAp-p
INPUT IMPEDANCE								
Differential			10^{13} || 2			•		Ω || pF
Common-Mode			10^{14} || 4			•		Ω || pF
INPUT VOLTAGE RANGE								
Common-Mode Input Range		±10.5	±11		•	•		V
Over Specified Temperature		±10.2	±10.5		•	•		V
SM Grade		±10	±10.3					V
Common-Mode Rejection	V_{CM} = ±10V	80	94		84	100		dB
OPEN-LOOP GAIN								
Open-Loop Voltage Gain	V_O = ±10V, R_L = 2kΩ	82	96		84	100		dB
Over Specified Temperature		80	94		82	96		dB
SM Grade		80	92					dB
DYNAMIC RESPONSE								
Slew Rate	G = +1	13	18		•	•		V/µs
Settling Time: 0.1%	G = –1, 10V Step		1.5			•		µs
0.01%			2			•		µs
Gain-Bandwidth Product	G = 100		4.5			•		MHz
THD + Noise	G = +1, f = 1kHz		0.001			•		%
Channel Separation	f = 100Hz, R_L = 2kΩ		120			•		dB
POWER SUPPLY								
Specified Operating Voltage			±15			•		V
Operating Voltage Range		±4.5		±18	•		•	V
Current			±4.5	±5		•	•	mA
OUTPUT								
Voltage Output	R_L = 2kΩ	±11	±12		•	•		V
Over Specified Temperature		±10.5	±11.5		•	•		V
SM Grade		±10.2	±11.3					V
Short Circuit Current		±10	±40		•	•		mA
Output Resistance, Open-Loop	1MHz		70			•		Ω
Capacitive Load Stability	G = +1		1000			•		pF
TEMPERATURE RANGE								
Specification								
AP, AU, AM, BM		–25		+85	•		•	°C
SM		–55		+125				°C
Operating								
AP, AU		–25		+85				°C
AM, BM, SM		–55		+125	•		•	°C
Storage								
AP, AU		–40		+125				°C
AM, BM, SM		–65		+150	•		•	°C
Thermal Resistance (θ_{J-A})								
AP			90					°C/W
AU			175					°C/W
AM, BM, SM			200			•		°C/W

* Specifications same as OPA2107AM. NOTE: (1) Specified with devices fully warmed up.

ORDERING INFORMATION

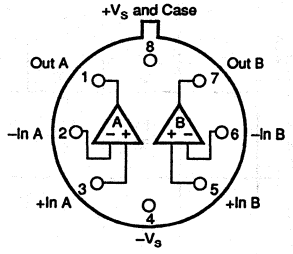
MODELS	PACKAGE	SPECIFICATION TEMPERATURE RANGE
OPA2107AP	Plastic DIP	–25 to +85°C
OPA2107AM	Metal TO-99	–25 to +85°C
OPA2107BM	Metal TO-99	–25 to +85°C
OPA2107SM	Metal TO-99	–55 to +125°C
OPA2107AU	SO-8 SOIC	–25 to +85°C

ABSOLUTE MAXIMUM RATINGS

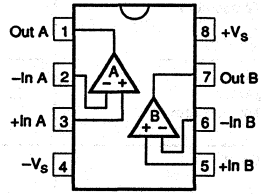
Supply Voltage ..... ±18V
Input Voltage Range ..... $\pm V_S$ ±2V
Differential Input Voltage ..... Total V_S ±4V
Operating Temperature
  M Package ..... –55°C to +125°C
  P and U Packages ..... –25°C to + 85°C
Storage Temperature
  M Package ..... –65°C to +150°C
  P and U Packages ..... –40°C to +125°C
Output Short Circuit to Ground (T_A = +25°C) ..... Continuous
Junction Temperature ..... +175°C
Lead Temperature
  M and P Packages (soldering, 10s) ..... +300°C
  U Package, SOIC (3s) ..... +260°C

PIN CONFIGURATIONS

Top View – M Package

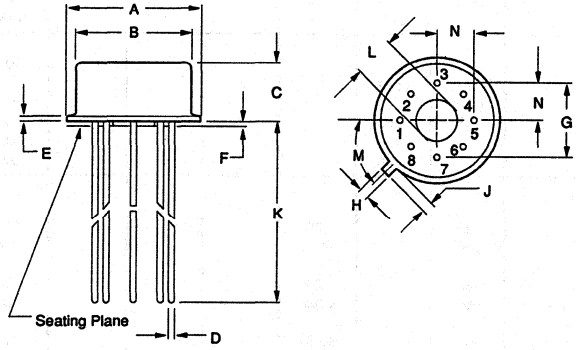


Top View – P & U Packages



MECHANICAL

M Package — Metal TO-99



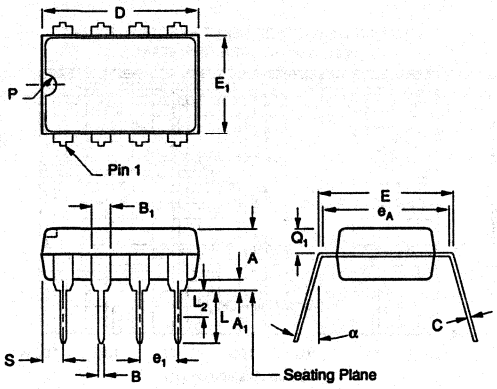
DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.335	.370	8.51	9.40
B	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.200 BASIC		5.08 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500	—	12.7	—
L	.110	.160	2.79	4.06
M	45° BASIC		45° BASIC	
N	.095	.105	2.41	2.67

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

MECHANICAL (CONT)

P Package — 8-Pin Plastic DIP

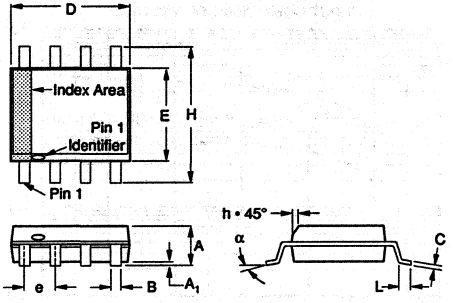


DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.155	.200	3.94	5.08
A_1	.020	.050	0.51	1.27
B	.014	.020	0.36	0.51
B_1	.045	.065	1.14	1.65
C	.008	.012	0.20	0.30
D (1)	.370	.400	9.40	10.16
E	.300	.325	7.62	8.26
E_1	.240	.260	6.10	6.60
e_1	.100 BASIC		2.54 BASIC	
e_A	.300 BASIC		7.62 BASIC	
L	.125	.150	3.18	3.81

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
L_2 (2)	0	.030	0.00	0.76
α	0°	15°	0°	15°
P	.015	.050	0.38	1.270
Q_1	.040	.075	1.02	1.91
S (1)	.015	.050	0.38	1.27

(1) Not JEDEC Std.
(2) e_1 and e_A apply in zone L_2 when unit installed.
NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

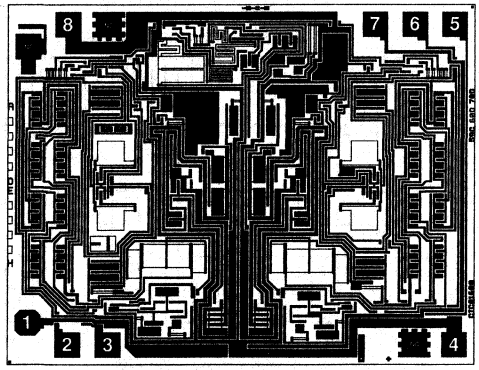
U Package — 8-Pin SO-8 Surface Mount



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.054	.068	1.37	1.73
A_1	.004	.009	0.10	0.23
B	.014	.019	0.36	0.48
C	.008	.0098	0.20	0.25
D	.189	.196	4.80	4.98
E	.150	.157	3.81	3.99
e	.050 BASIC		1.27 BASIC	
H	.229	.244	5.82	6.20
h	.010	.019	0.25	0.48
L	.016	.050	0.41	1.27
N	8		8	
α	0°	8°	0°	8°

NOTES:
1. Dimensioning and tolerancing per ANSI Y14.5M–1982.
2. "D" and "E" are reference datums and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm (.086 in.)
3. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the cross-hatched area.
4. "L" is the length of the terminal for soldering to a substrate.
5. "N" is the number of terminal positions.

DICE INFORMATION



OPA2107 DIE TOPOGRAPHY

PAD	FUNCTION
1	Out A
2	–In A
3	+In A
4	$-V_S$
5	+In B
6	–In B
7	Out B
8	$+V_S$

Substrate Bias: $-V_S$

MECHANICAL INFORMATION

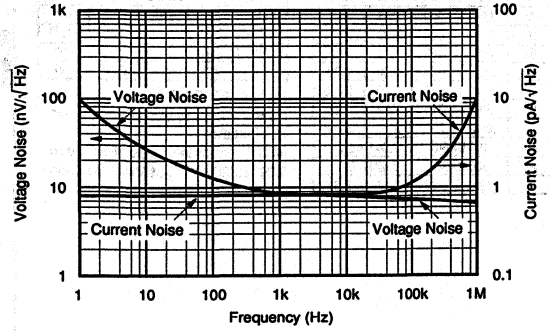
	MILS (0.001")	MILLIMETERS
Die Size	97 x 77 ±3	2.46 x 1.96 ±0.13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.10 x 0.10
Backing	None	

See "DICE PRODUCTS" Section 17 in Data Book Supplement Volume 33c, or contact Burr-Brown for current information.

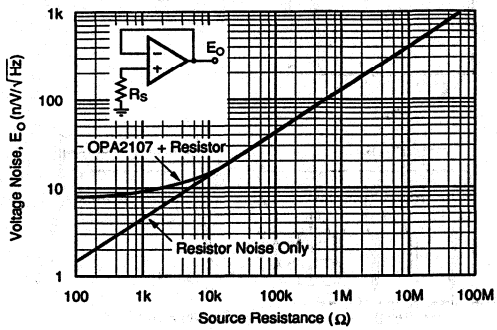
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_S = ±15V unless otherwise noted.

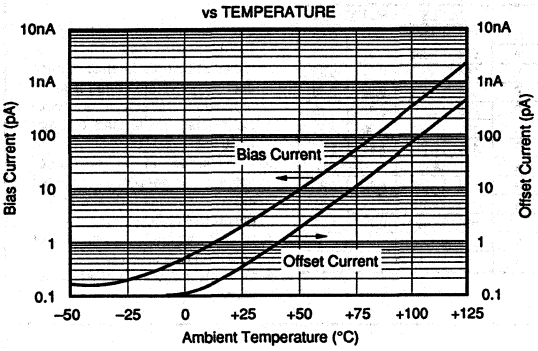
INPUT VOLTAGE AND CURRENT NOISE SPECTRAL DENSITY vs FREQUENCY



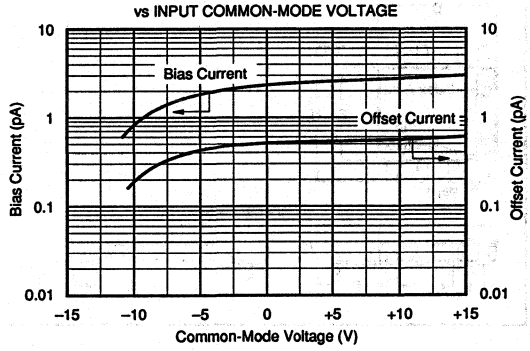
TOTAL INPUT VOLTAGE NOISE SPECTRAL DENSITY at 1kHz vs SOURCE RESISTANCE



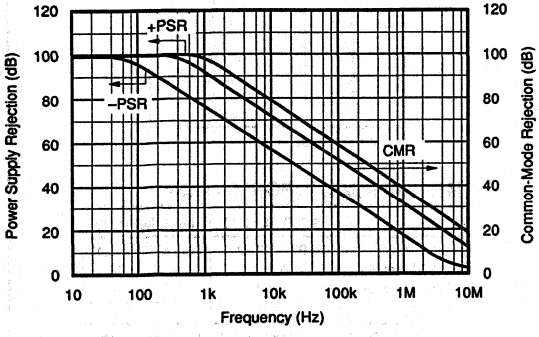
BIAS AND OFFSET CURRENT vs TEMPERATURE



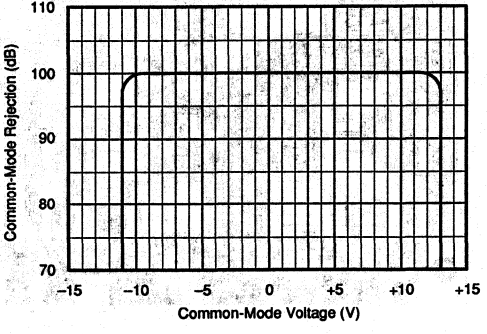
BIAS AND OFFSET CURRENT vs INPUT COMMON-MODE VOLTAGE



POWER SUPPLY AND COMMON-MODE REJECTION vs FREQUENCY



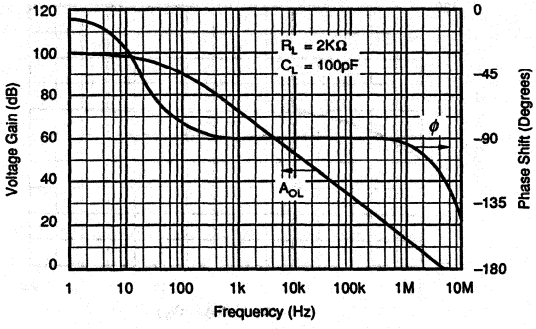
COMMON-MODE REJECTION vs INPUT COMMON-MODE VOLTAGE



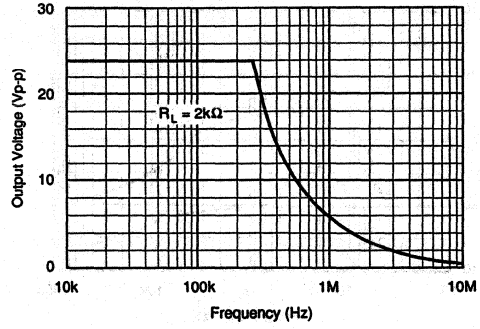
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_S = ±15V unless otherwise noted.

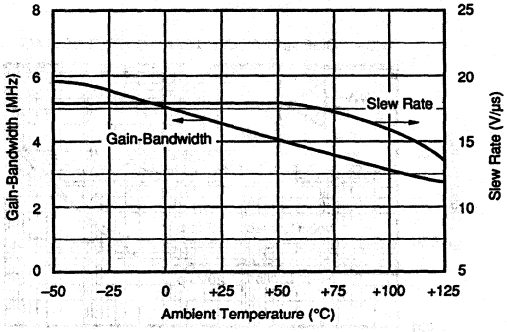
OPEN-LOOP FREQUENCY RESPONSE



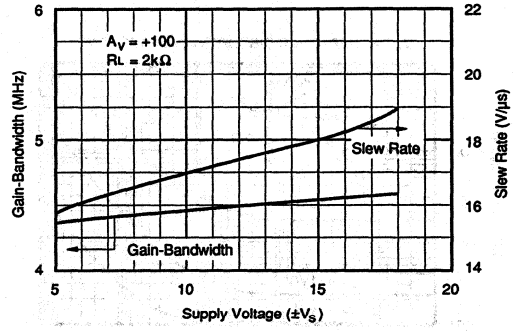
MAXIMUM OUTPUT VOLTAGE SWING vs FREQUENCY



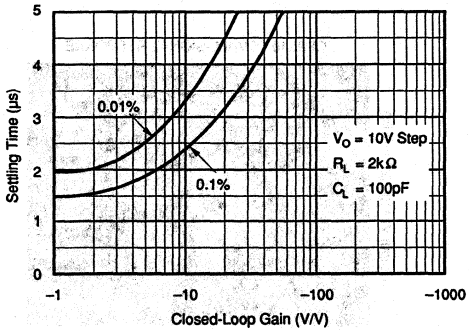
GAIN-BANDWIDTH AND SLEW RATE vs TEMPERATURE



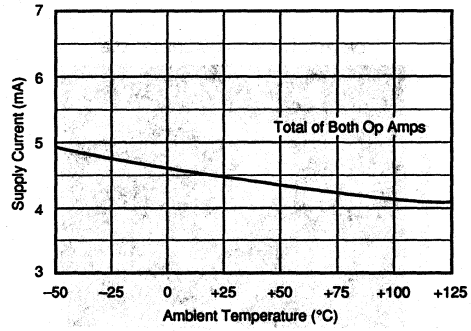
GAIN-BANDWIDTH AND SLEW RATE vs SUPPLY VOLTAGE



SETTLING TIME vs CLOSED-LOOP GAIN



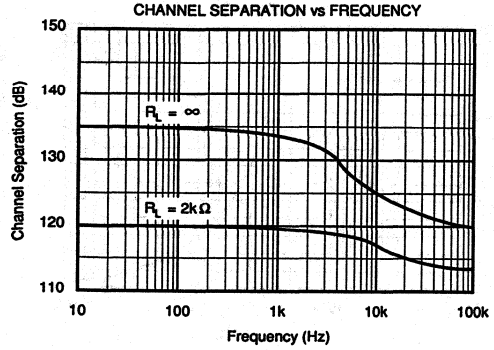
SUPPLY CURRENT vs TEMPERATURE



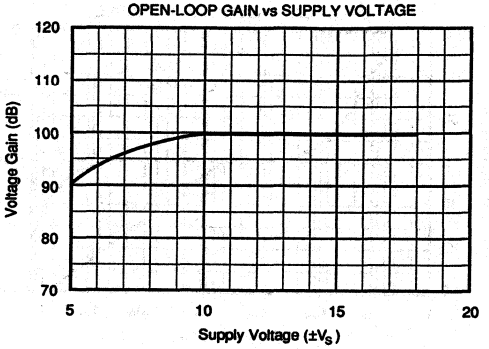
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_S = ±15V unless otherwise noted.

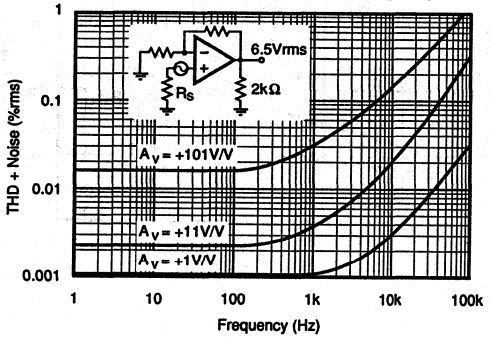
CHANNEL SEPARATION vs FREQUENCY



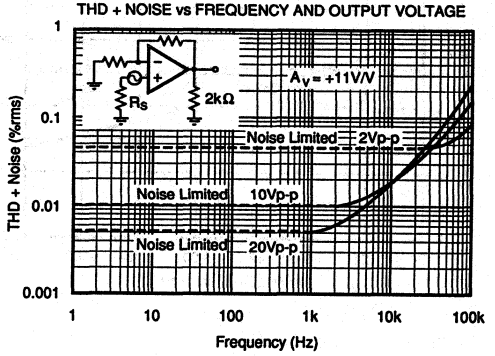
OPEN-LOOP GAIN vs SUPPLY VOLTAGE



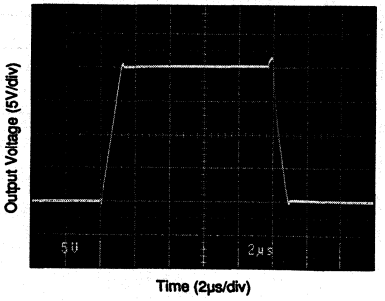
TOTAL HARMONIC DISTORTION vs FREQUENCY



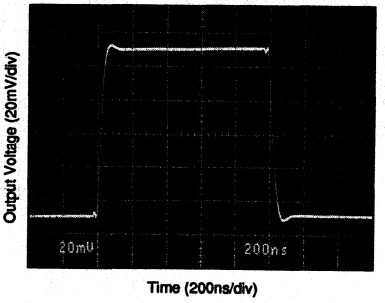
THD + NOISE vs FREQUENCY AND OUTPUT VOLTAGE



OPA2107 LARGE-SIGNAL RESPONSE



OPA2107 SMALL-SIGNAL RESPONSE



APPLICATIONS INFORMATION AND CIRCUITS

The OPA2107 is unity-gain stable and has excellent phase margin. This makes it easy to use in a wide variety of applications.

Power supply connections should be bypassed with capacitors positioned close to the amplifier pins. In most cases, 0.1µF ceramic capacitors are adequate. Applications with larger load currents and fast transient signals may need up to 1µF tantalum bypass capacitors.

INPUT BIAS CURRENT

The OPA2107's ***Difet*** input stages have very low input bias current—an order of magnitude lower than BIFET op amps. Circuit board leakage paths can significantly degrade performance. This is especially evident with the SO-8 surface-mount package where pin-to-pin dimensions are particularly small. Residual soldering flux, dirt, and oils, which conduct leakage current, can be removed by proper cleaning. In most instances a two-step cleaning process is adequate using a clean organic solvent rinse followed by de-ionized water. Each rinse should be followed by a 30-minute bake at 85°C.

A circuit board guard pattern effectively reduces errors due to circuit board leakage (Figure 1). By encircling critical high impedance nodes with a low impedance connection at the same circuit potential, any leakage currents will flow harmlessly to the low impedance node. Guard traces should be placed on all levels of a multiple-layer circuit board.

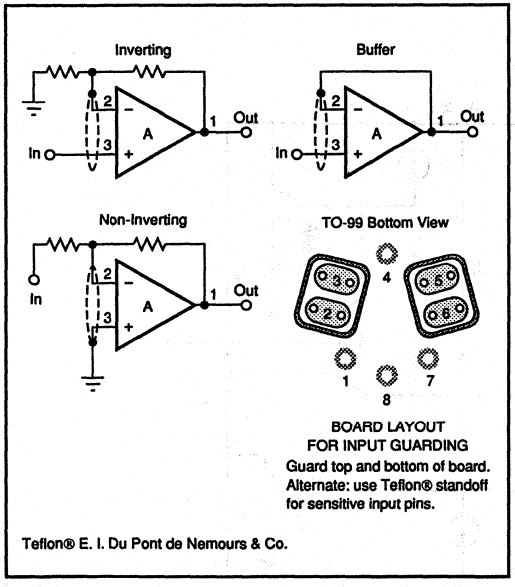


FIGURE 1. Connection of Input Guard.

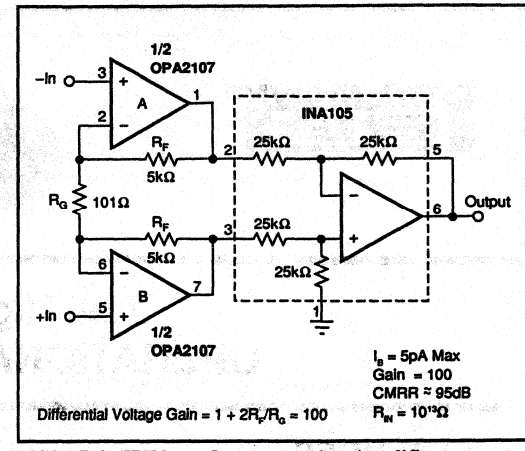


FIGURE 2. FET Input Instrumentation Amplifier.

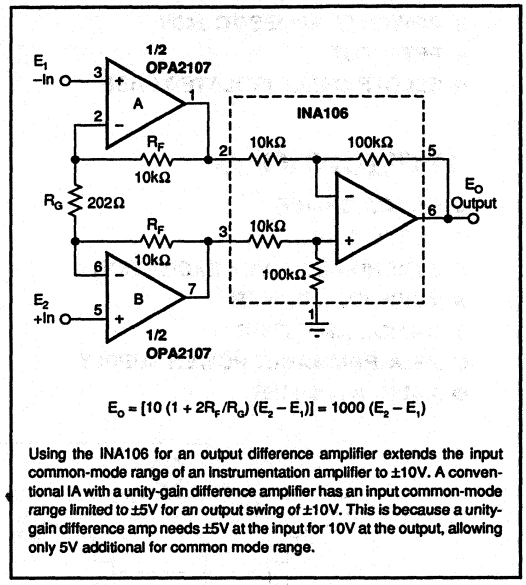


FIGURE 3. Precision Instrumentation Amplifier.

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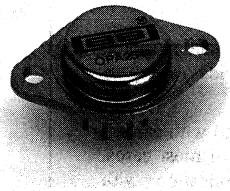


OPA2541

Dual High Power OPERATIONAL AMPLIFIER

FEATURES

- OUTPUT CURRENTS TO 5A
- POWER SUPPLIES TO ±40V
- FET INPUT
- ELECTRICALLY ISOLATED CASE

APPLICATIONS

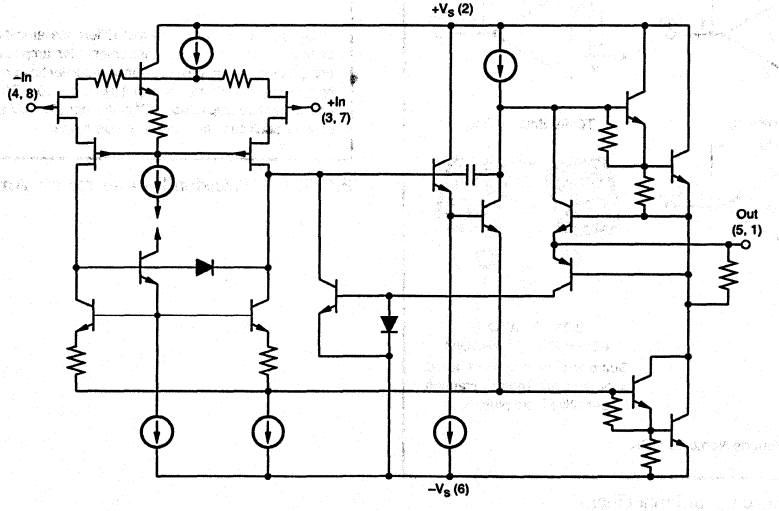
- MOTOR DRIVER
- SERVO AMPLIFIER
- SYNCRO/RESOLVER EXCITATION
- VOICE COIL DRIVER
- BRIDGE AMPLIFIER
- PROGRAMMABLE POWER SUPPLY
- AUDIO AMPLIFIER

DESCRIPTION

The OPA2541 is a dual power operational amplifier capable of operation from power supplies up to ±40V and output currents of 5A continuous. With two monolithic power amplifiers in a single package it provides unequaled functional density.

The industry-standard 8-pin TO-3 package is isolated from all internal circuitry allowing it to be mounted directly to a heat sink without insulators which degrade thermal performance. Internal circuitry limits output current to approximately 6A.

The OPA2541 is available in both industrial and military temperature range versions.



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Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL

At T_C = +25°C and V_S = ±35VDC, unless otherwise noted.

PARAMETER	CONDITIONS	OPA2541AM			OPA2541BM/SM			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
INPUT OFFSET VOLTAGE								
V_{OS}			±2	±10		±0.25	±1	mV
vs Temperature	Specified Temperature Range		±20	±40		±15	±30	µV/°C
vs Supply Voltage	V_S = ±10V to ±V_{MAX}		±2.5	±10		*	*	µV/V
vs Power			±20	±60		*	*	µV/W
INPUT BIAS CURRENT								
I_B			15	50		*	*	pA
	Specified Temperature Range		Note 1			*		
INPUT OFFSET CURRENT								
I_{OS}			±5	±30		*	*	pA
	Specified Temperature Range		Note 1			*		
INPUT CHARACTERISTICS								
Common-Mode Voltage Range	Specified Temperature Range	±($\|V_S\|$ –6)	±($\|V_S\|$ –3)		*	*		V
Common-Mode Rejection	V_{CM} = (±V_S –6V)	95	106		*	*		dB
Input Capacitance			5			*		pF
Input Impedance, DC			1			*		$10^{12}\Omega$
GAIN CHARACTERISTICS								
Open Loop Gain at 10Hz	R_L = 6Ω	90	96		*	*		dB
Gain-Bandwidth Product			1.6			*		MHz
OUTPUT								
Voltage Swing	I_O = 5A	±($\|V_S\|$ –5.5)	±($\|V_S\|$ –4.5)		*	*		V
	I_O = 2A	±($\|V_S\|$ –4.5)	±($\|V_S\|$ –3.6)		*	*		V
	I_O = 0.5A	±($\|V_S\|$ –4)	±($\|V_S\|$ –3.2)		*	*		V
Current, Continuous	+25°C	5	7.0		*	*		A
	+85°C	4	5.0		*			A
	+125°C (SM grade only)				3	3.5		A
AC PERFORMANCE								
Slew Rate		6	8		*	*		V/µs
Power Bandwidth	R_L = 8Ω, V_O = 20Vrms	45	55		*	*		kHz
Settling Time to 0.1%	2V Step		2			*		µs
Capacitive Load	Specified Temperature Range, G = 1			3.3			*	nF
	Specified Temperature Range, G >10			SOA			*	
Phase Margin	Specified Temperature Range, R_L = 8Ω		40			*		Degrees
Channel Separation	1kHz, R_L = 6Ω		80			*		dB
POWER SUPPLY								
Power Supply Voltage, ±V_S	Specified Temperature Range	±10	±30	±35	*	±35	±40	V
Current, Quiescent	Total—Both Amplifiers		40	50		*	*	mA
THERMAL RESISTANCE								
θ_{JC}, (Junction-to-Case)	Both Amplifiers[2], AC Output f > 60Hz		0.8	1.0		*	*	°C/W
θ_{JC}	Both Amplifiers[2], DC Output		0.9	1.2		*	*	°C/W
θ_{JC}	One Amplifier, AC Output f > 60Hz		1.25	1.5		*	*	°C/W
θ_{JC}	One Amplifier, DC Output		1.4	1.9		*	*	°C/W
θ_{JA}, (Junction-to-Ambient)	No Heat Sink		30			*		°C/W
TEMPERATURE RANGE								
Case	AM, BM	–25		+85	*		*	°C
	SM				–55		+125	°C

*Specification same as OPA2541AM.

NOTES: (1) Input bias and offset current approximately doubles for every 10°C increase in temperature. (2) Assumes equal dissipation in both amplifiers.

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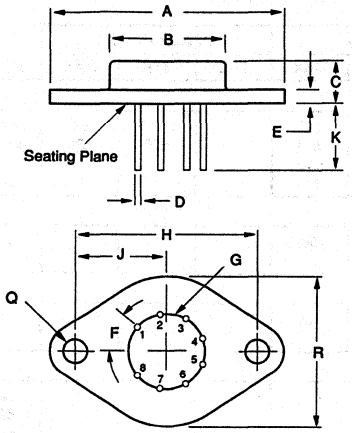
MECHANICAL

M Package — 8-Pin Metal TO-3



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.510	1.550	38.35	39.37
B	.745	.770	18.92	19.56
C	.260	.300	6.60	7.62
D	.038	.042	0.97	1.07
E	.080	.105	2.03	2.67
F	40° BASIC		40° BASIC	
G	.500 BASIC		12.70 BASIC	
H	1.182	1.192	30.02	30.28
J	.591	.596	15.01	15.14
K	.400	.500	10.16	12.70
Q	.151	.161	3.84	4.09
R	.980	1.020	24.89	25.91

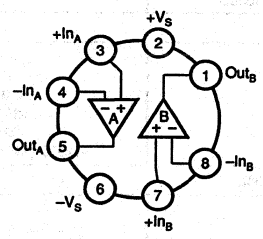
NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, $+V_S$ to $-V_S$ 80V
Output Current ..... see SOA
Power Dissipation, Internal(1) 125W
Input Voltage: Differential ..... $\pm V_S$
Common-mode ..... $\pm V_S$
Temperature: Pin Solder, 10s ..... +300°C
Junction(1) ..... +150°C
Temperature Range:
Storage ..... –65°C to +150°C
Operating (Case) ..... –55°C to +125°C

NOTE: (1) Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF.

CONNECTION DIAGRAM



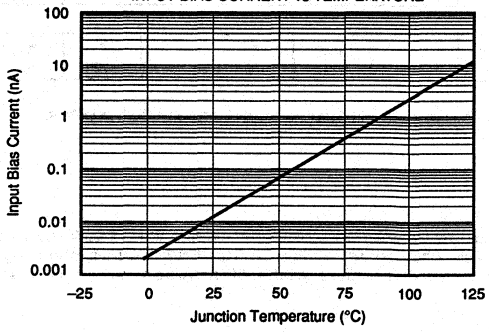
ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE
OPA2541AM	TO-3	–25°C to +85°C
OPA2541BM	TO-3	–25°C to +85°C
OPA2541SM	TO-3	–55°C to +125°C

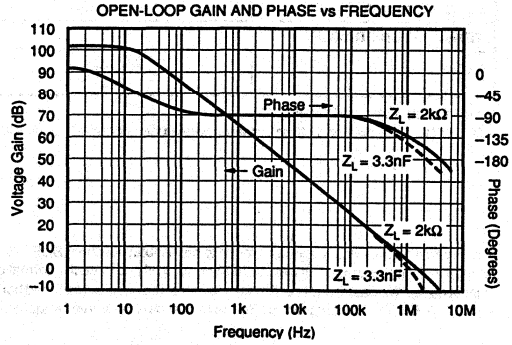
TYPICAL PERFORMANCE CURVES

T_A = +25°C and V_S = ±35VDC, unless otherwise noted.

INPUT BIAS CURRENT vs TEMPERATURE



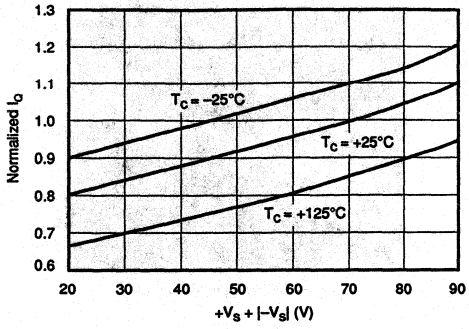
OPEN-LOOP GAIN AND PHASE vs FREQUENCY



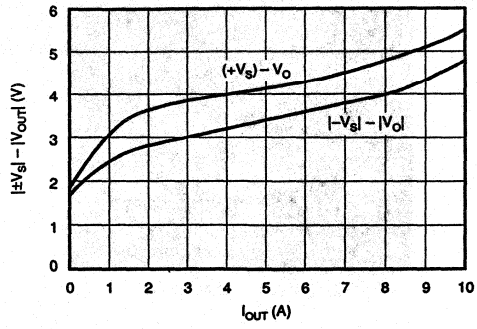
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C and V_S = ±35VDC, unless otherwise noted.

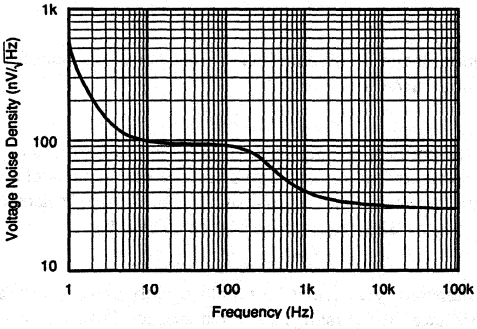
NORMALIZED QUIESCENT CURRENT vs TOTAL POWER SUPPLY VOLTAGE



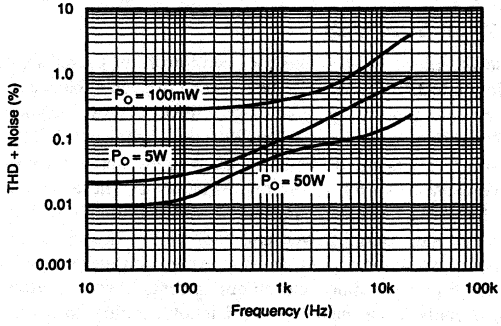
OUTPUT VOLTAGE SWING vs OUTPUT CURRENT



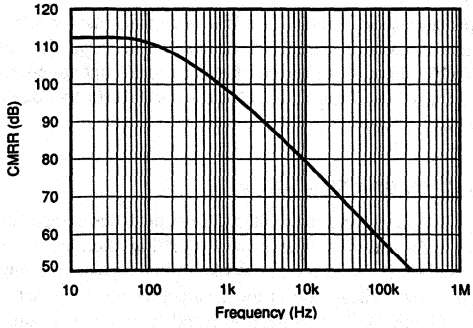
VOLTAGE NOISE DENSITY vs FREQUENCY



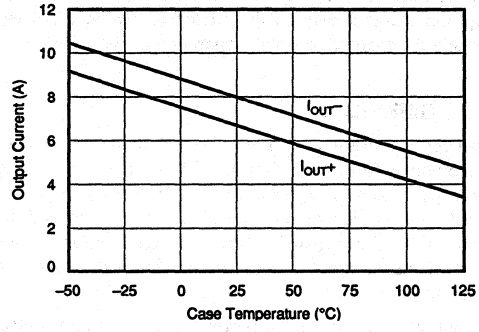
TOTAL HARMONIC DISTORTION vs FREQUENCY



COMMON-MODE REJECTION vs FREQUENCY



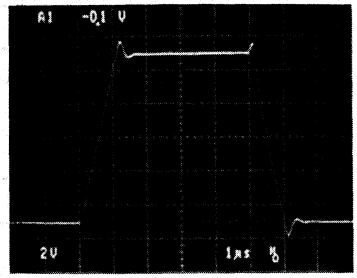
OUTPUT CURRENT vs TEMPERATURE



TYPICAL PERFORMANCE CURVES (CONT)

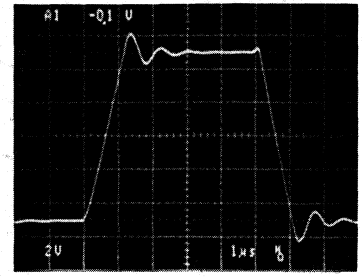
T_A = +25°C and V_S = ±35VDC, unless otherwise noted.

DYNAMIC RESPONSE



Z_{LOAD} = ∞, V_S = ±35V, A_V = +1

DYNAMIC RESPONSE



Z_{LOAD} = 4700pF, V_S = ±35V, A_V = +1

INSTALLATION INSTRUCTIONS

POWER SUPPLIES

The OPA2541 is specified for operation from power supplies up to ±40V. It can also be operated from an unbalanced or a single power supply so long as the total power supply voltage does not exceed 80V (70V for "AM" grade). The power supplies should be bypassed with low series impedance capacitors such as ceramic or tantalum. These should be located as near as practical to the amplifier's power supply pins. Good power amplifier circuit layout is, in general, like good high-frequency layout. Consider the path of large power supply and output currents. Avoid routing these connections near low-level input circuitry to avoid waveform distortion and instability.

Signal dependent load current can modulate the power supply voltage with inadequate power supply bypassing. This can affect both amplifiers' outputs. Since the second amplifier's signal may not be related to the first, this will degrade the inherent channel separation of the OPA2541.

HEAT SINKING

Most applications will require a heat sink to prevent junction temperatures from exceeding the 150°C maximum rating. The type of heat sink required will depend on the output signals, power dissipation of each amplifier, and ambient temperature. The thermal resistance from junction-to-case, θ_{JC}, depends on how the power dissipation is distributed on the amplifier die.

DC output concentrates the power dissipation in one output transistor. AC output distributes the power dissipation equally between the two output transistors and therefore has lower thermal resistance. Similarly, the power dissipation may be all in one amplifier (worst case) or equally distributed between the two amplifiers (best case). Thermal resistances are provided for each of these possibilities. The case-to-junction temperature rise is the product of the power dissipation (total of both amplifiers) times the appropriate thermal resistance—

$$\Delta T_{JC} = (P_D \text{ total})\ (\theta_{JC}).$$

Sufficient heat sinking must be provided to keep the case temperature within safe limits for the maximum ambient temperature and power dissipation. The thermal resistance of the heat sink required may be calculated by:

$$\theta_{HS} = (150°C - \Delta T_{JC} - T_A)/P_D.$$

Commercially available heat sinks usually specify thermal resistance. These ratings are often suspect, however, since they depend greatly on the mounting environment and air flow conditions. Actual thermal performance should be verified by measurement of case temperature under the required load and environmental conditions.

No insulating hardware is required when using the OPA2541. Since mica and other similar insulators typically add 0.7°C/W thermal resistance, this is a significant advantage. See Burr-Brown Application Note AN-83 for further details on heat sinking.

SAFE OPERATING AREA

The Safe Operating Area (SOA) curve provides comprehensive information on the power handling abilities of the OPA2541. It shows the allowable output current as a function of the voltage across the conducting output transistor (see Figure 1). This voltage is equal to the power supply voltage minus the output voltage. For example, as the amplifier output swings near the positive power supply voltage, the voltage across the output transistor decreases and the device can safely provide large output currents demanded by the load.

The internal current limit will not provide short-circuit protection in most applications. When the amplifier output is shorted to ground, the full power supply voltage is impressed across the conducting output transistor. For instance, with V_S = ±35V, a short circuit to ground would impress 35V across the conducting power transistor. The maximum safe output current at this voltage is 1.8A, so the internal current limit would not protect the amplifier. The unit-to-unit variation and temperature dependence of the internal current limit suggest that it be used to handle abnormal conditions and not activated in commonly encountered circuit operation.

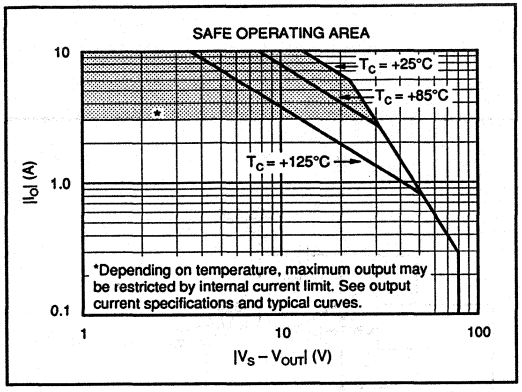


FIGURE 1. Safe Operating Area.

Reactive, or EMF generating loads such as DC motors can present demanding SOA requirements. With a purely reactive load, output voltage current occurs when the output voltage is zero and the voltage across the conducting transistor is equal to the full power supply voltage. See Burr-Brown Application Note AN-123 for further information on evaluating SOA.

Applications with inductive or EMF-generating loads which can produce "kick back" voltage surges to the amplifiers should include clamp diodes from the output terminals to the power supplies. These diodes should be chosen to limit the peak amplifier output voltage surges to less than 2V beyond the power supply rail voltage. Common 1A rated rectifier diodes will suffice in most applications.

APPLICATIONS CIRCUITS

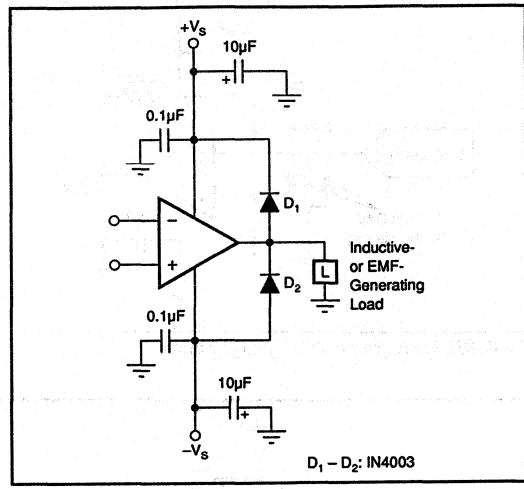


FIGURE 2. Clamping Output for EMF-Generating Loads.

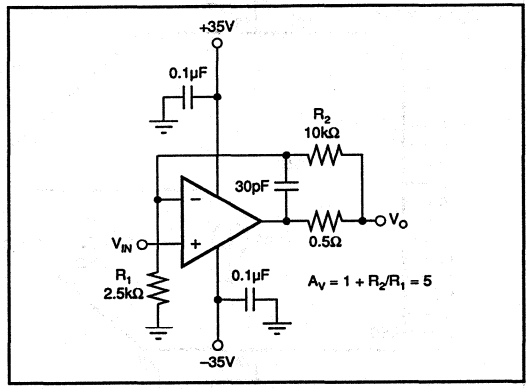


FIGURE 3. Isolating Capacitive Loads.

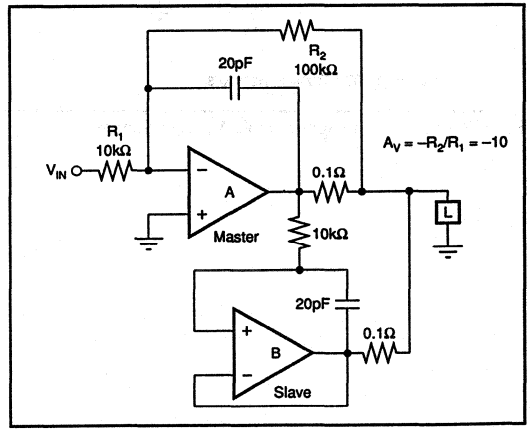


FIGURE 4. Paralleled Operation, Extended SOA.

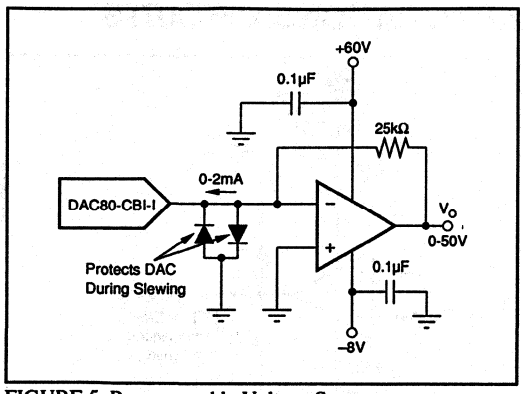


FIGURE 5. Programmable Voltage Source.

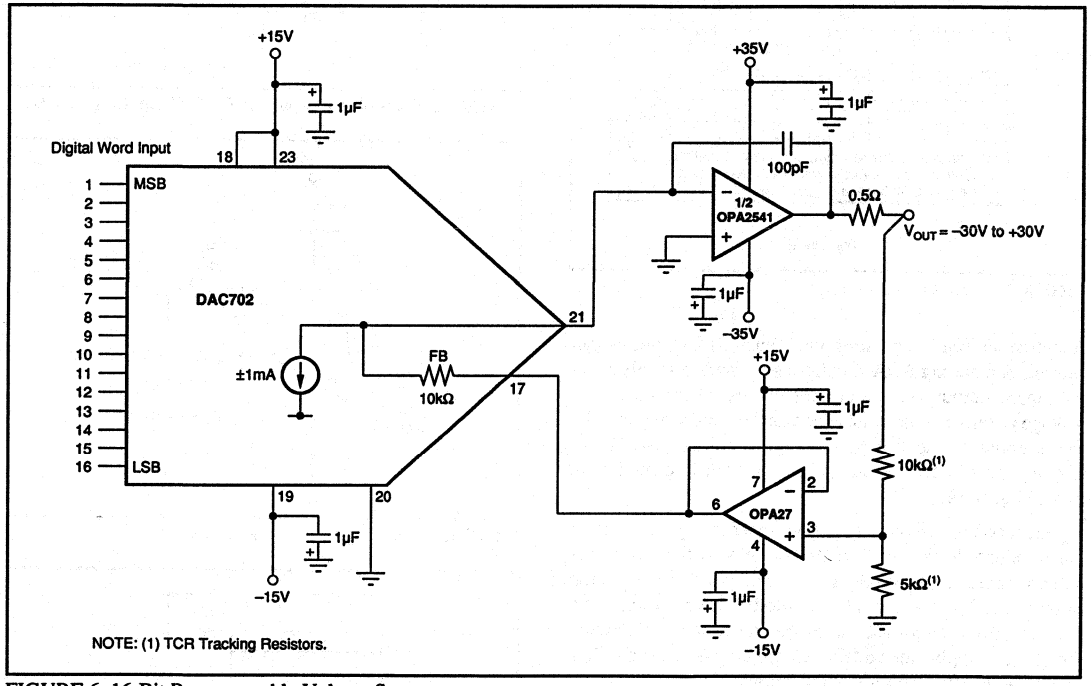


FIGURE 6. 16-Bit Programmable Voltage Source.

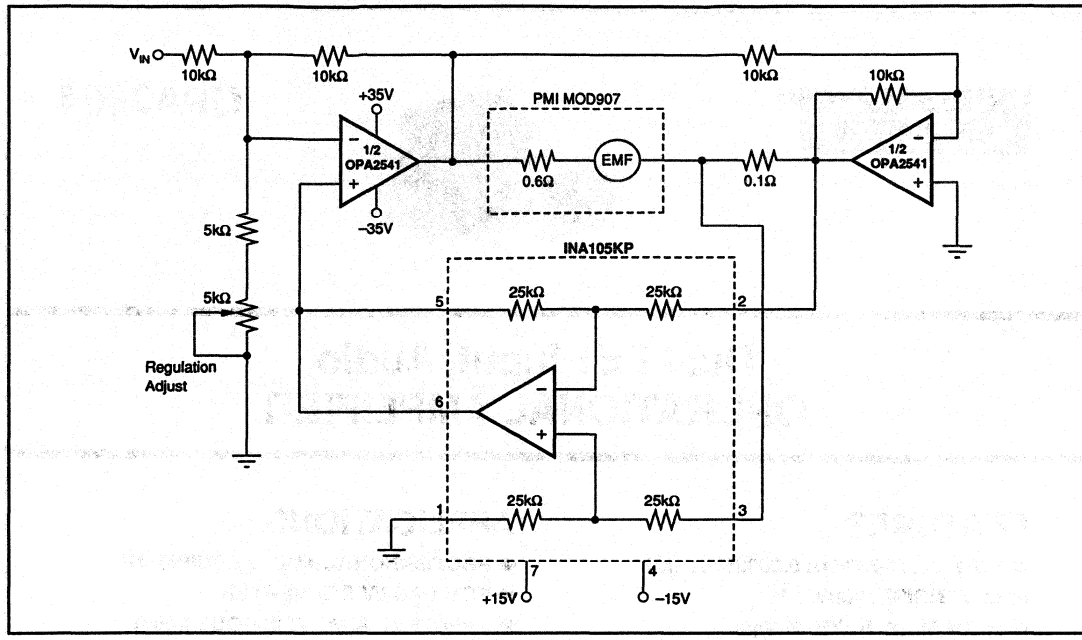


FIGURE 7. Bridge Amplifier Motor-Speed Controller.

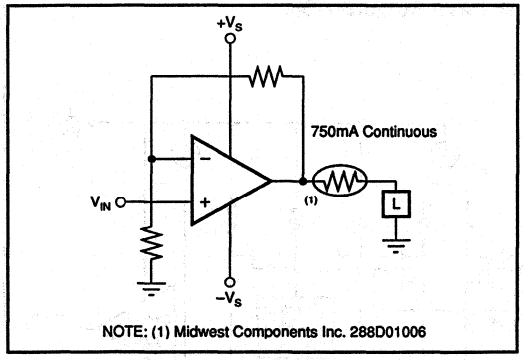


FIGURE 8. Limiting Output Current.

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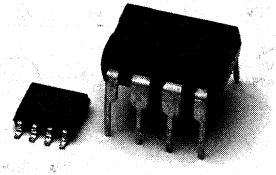


OPA2604

Dual FET-Input, Audio OPERATIONAL AMPLIFIER

FEATURES

- LOW DISTORTION: 0.0003% at 1kHz
- LOW NOISE: 10nV/√Hz
- HIGH SLEW RATE: 25V/µs
- WIDE GAIN-BANDWIDTH: 20MHz
- UNITY-GAIN STABLE
- WIDE SUPPLY RANGE: V_S = ±4.5 to ±24V
- DRIVES 600Ω LOADS

APPLICATIONS

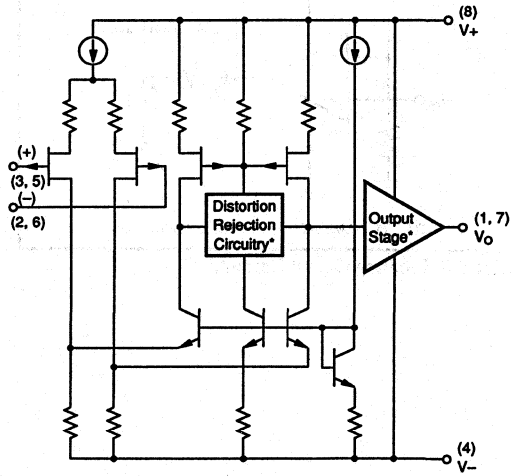
- PROFESSIONAL AUDIO EQUIPMENT
- PCM DAC I/V CONVERTER
- SPECTRAL ANALYSIS EQUIPMENT
- ACTIVE FILTERS
- TRANSDUCER AMPLIFIER
- DATA ACQUISITION

DESCRIPTION

The OPA2604 is a dual, FET-input operational amplifier designed for enhanced AC performance. Very low distortion, low noise and wide bandwidth provide superior performance in high quality audio and other applications requiring excellent dynamic performance.

New circuit techniques and special laser trimming of dynamic circuit performance yield very low harmonic distortion. The result is an op amp with exceptional sound quality. The low-noise FET input of the OPA2604 provides wide dynamic range, even with high source impedance. Offset voltage is laser-trimmed to minimize the need for interstage coupling capacitors.

The OPA2604 is available in 8-pin plastic mini-DIP and SO-8 surface-mount packages, specified for the –25°C to +85°C temperature range.



* Patents Granted:
#5053718, 5019789

International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

PDS-1069A

SPECIFICATIONS

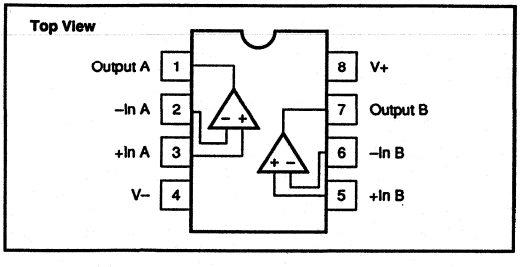
ELECTRICAL

T_A = +25°C, V_S = ±15V unless otherwise noted.

PARAMETER	CONDITION	OPA2604AP, AU MIN	TYP	MAX	UNITS
OFFSET VOLTAGE					
Input Offset Voltage			±0.1	±3	mV
Average Drift			±8		µV/°C
Power Supply Rejection	V_S = ±5 to ±24V	80	100		dB
INPUT BIAS CURRENT(1)					
Input Bias Current	V_{CM} = 0V		100		pA
Input Offset Current	V_{CM} = 0V		±4		pA
NOISE					
Input Voltage Noise					
Noise Density: f = 10Hz			25		nV/√Hz
f = 100Hz			15		nV/√Hz
f = 1kHz			11		nV/√Hz
f = 10kHz			10		nV/√Hz
Voltage Noise, BW = 20Hz to 20kHz			1.5		µVp-p
Input Bias Current Noise					
Current Noise Density, f = 0.1Hz to 20kHz			6		fA/√Hz
INPUT VOLTAGE RANGE					
Common-Mode Input Range		±12	±13		V
Common-Mode Rejection	V_{CM} = ±12V	80	100		dB
INPUT IMPEDANCE					
Differential			10^{12} || 8		Ω || pF
Common-Mode			10^{12} || 10		Ω || pF
OPEN-LOOP GAIN					
Open-loop Voltage Gain	V_O = ±10V, R_L = 1kΩ	80	100		dB
FREQUENCY RESPONSE					
Gain-Bandwidth Product	G = 100		20		MHz
Slew Rate	20Vp-p, R_L = 1kΩ	15	25		V/µs
Settling Time: 0.01%	G = –1, 10V Step		1.5		µs
0.1%			1		µs
Total Harmonic Distortion + Noise (THD + N)	G = 1, f = 1kHz		0.0003		%
	V_O = 3.5Vrms, R_L = 1kΩ				
Channel Separation	f = 1kHz, R_L = 1kΩ		142		dB
OUTPUT					
Voltage Output	R_L = 600Ω	±11	±12		V
Current Output	V_O = ±12V		±35		mA
Short Circuit Current			±40		mA
Output Resistance, Open-Loop			25		Ω
POWER SUPPLY					
Specified Operating Voltage			±15		V
Operating Voltage Range		±4.5		±24	V
Current, Total Both Amplifiers			±10.5	±12	mA
TEMPERATURE RANGE					
Specification		–25		+85	°C
Storage		–40		+125	°C
Thermal Resistance(2), θ_{JA}			90		°C/W

NOTES: (1) Typical performance, measured fully warmed-up. (2) Soldered to circuit board—see text.

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

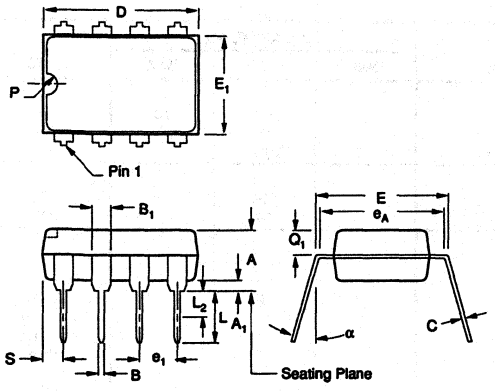
Power Supply Voltage	±25V
Input Voltage	(V–)–1V to (V+)+1V
Output Short Circuit to Ground	Continuous
Operating Temperature	–40°C to +100°C
Storage Temperature	–40°C to +125°C
Junction Temperature	+150°C
Lead Temperature (soldering, 10s) AP	+300°C
Lead Temperature (soldering, 3s) AU	+260°C

ORDERING INFORMATION

MODEL	PACKAGE	TEMP. RANGE
OPA2604AP	8-Pin Plastic DIP	–25°C to +85°C
OPA2604AU	SO-8 Surface-Mount	–25°C to +85°C

MECHANICAL

P Package — 8-Pin Plastic DIP

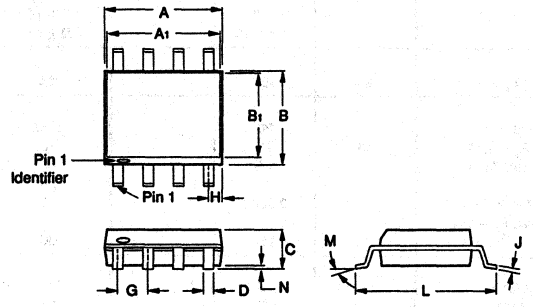


DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.155	.200	3.94	5.08
A1	.020	.050	0.51	1.27
B	.014	.020	0.36	0.51
B1	.045	.065	1.14	1.65
C	.008	.012	0.20	0.30
D (1)	.370	.400	9.40	10.16
E	.300	.325	7.62	8.26
E1	.240	.260	6.10	6.60
e1	.100 BASIC		2.54 BASIC	
eA	.300 BASIC		7.62 BASIC	
L	.125	.150	3.18	3.81

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
L2 (2)	0	.030	0.00	0.76
α	0°	15°	0°	15°
P	.015	.050	0.38	1.270
Q1	.040	.075	1.02	1.91
S (1)	.015	.050	0.38	1.27

(1) Not JEDEC Std.
(2) e1 and e_A apply in zone L_2 when unit installed.
NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

U Package — 8-Pin SO-8 Surface Mount



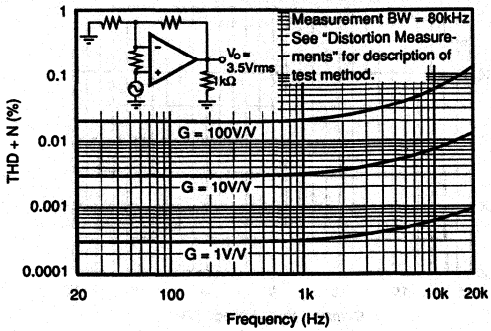
DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.185	.201	4.70	5.11
A1	.178	.201	4.52	5.11
B	.146	.162	3.71	4.11
B1	.130	.149	3.30	3.78
C	.054	.071	1.37	1.80
D	.015	.019	0.38	0.48
G	.050 BASIC		1.27 BASIC	
H	.018	.026	0.46	0.66
J	.008	.012	0.20	0.30
L	.220	.252	5.59	6.40
M	0°	10°	0°	10°
N	.000	.012	0.00	0.30

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

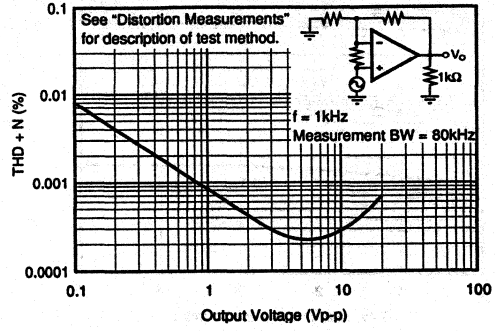
TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_S = ±15V unless otherwise noted.

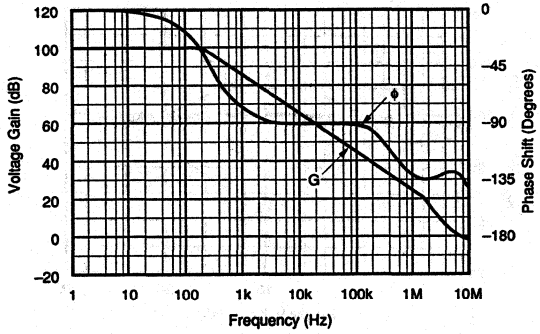
TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY



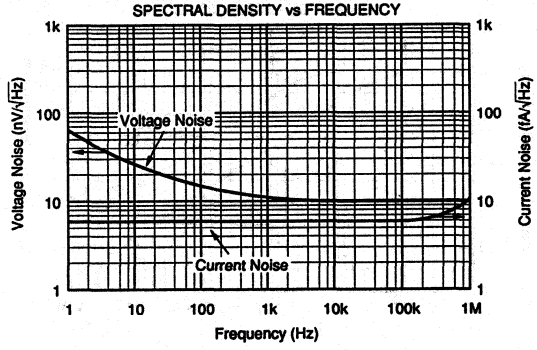
TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT VOLTAGE



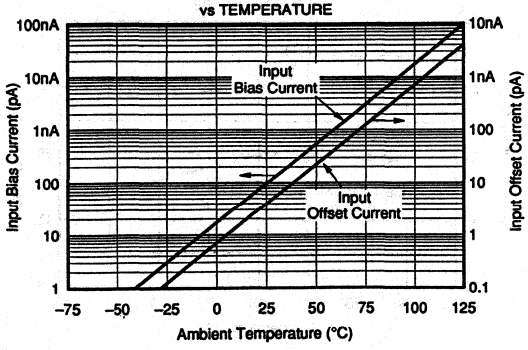
OPEN-LOOP GAIN/PHASE vs FREQUENCY



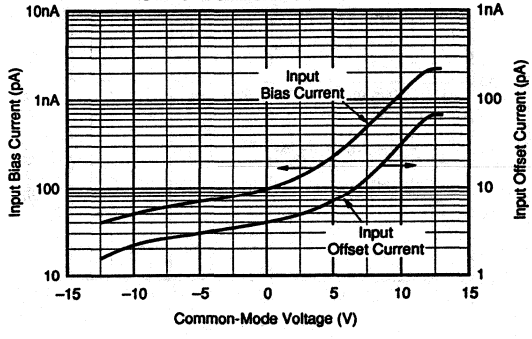
INPUT VOLTAGE AND CURRENT NOISE SPECTRAL DENSITY vs FREQUENCY



INPUT BIAS AND INPUT OFFSET CURRENT vs TEMPERATURE



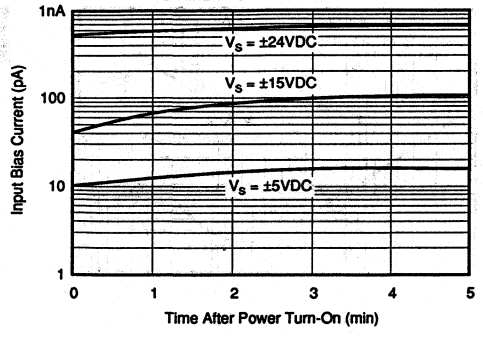
INPUT BIAS AND INPUT OFFSET CURRENT vs INPUT COMMON-MODE VOLTAGE



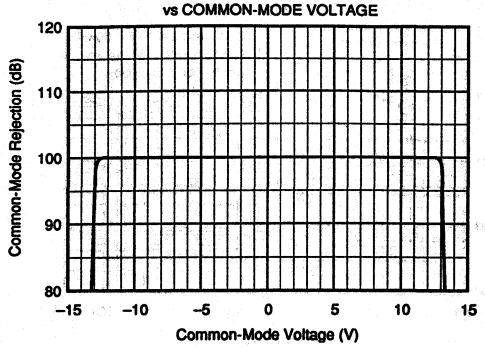
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_S = ±15V unless otherwise noted.

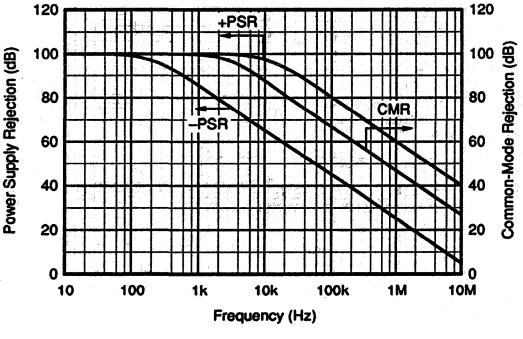
INPUT BIAS CURRENT vs TIME FROM POWER TURN-ON



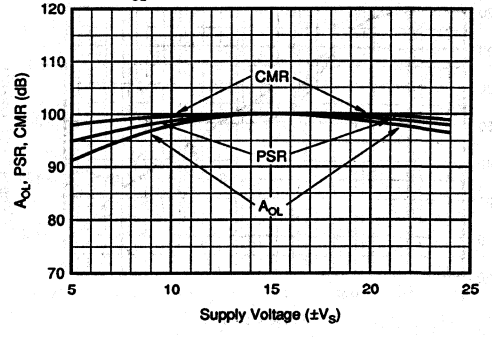
COMMON-MODE REJECTION vs COMMON-MODE VOLTAGE



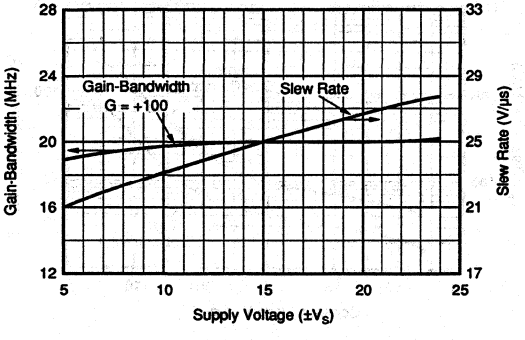
POWER SUPPLY AND COMMON-MODE REJECTION vs FREQUENCY



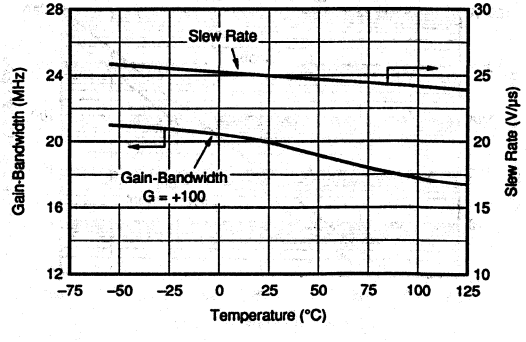
A_{OL}, PSR, AND CMR vs SUPPLY VOLTAGE



GAIN-BANDWIDTH AND SLEW RATE vs SUPPLY VOLTAGE



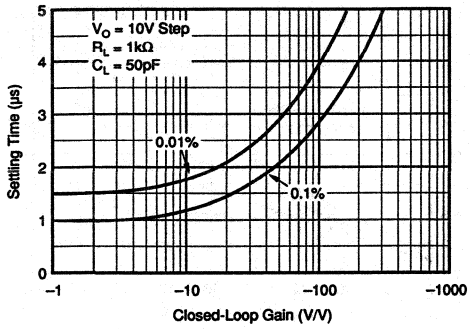
GAIN-BANDWIDTH AND SLEW RATE vs TEMPERATURE



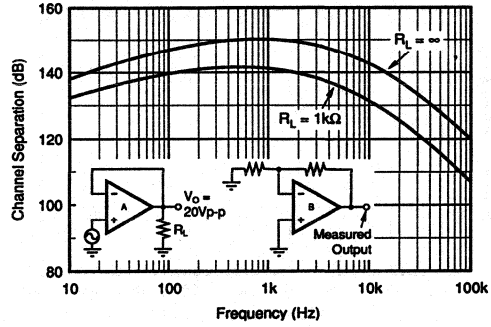
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_S = ±15V unless otherwise noted.

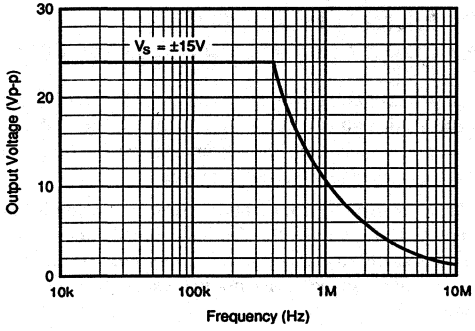
SETTLING TIME vs CLOSED-LOOP GAIN



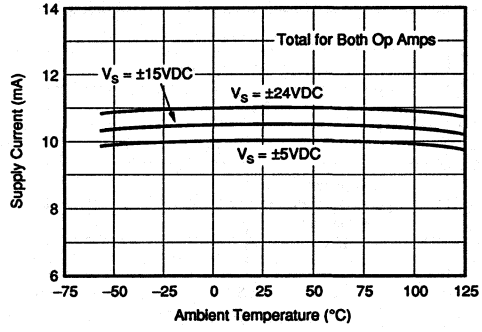
CHANNEL SEPARATION vs FREQUENCY



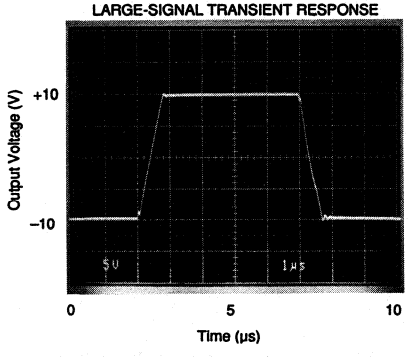
MAXIMUM OUTPUT VOLTAGE SWING vs FREQUENCY



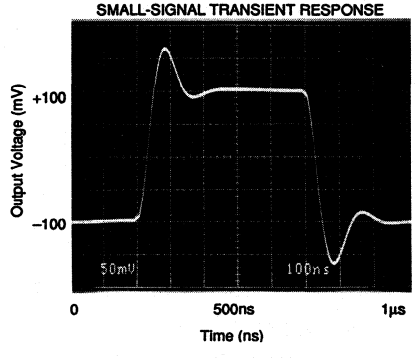
SUPPLY CURRENT vs TEMPERATURE



LARGE-SIGNAL TRANSIENT RESPONSE



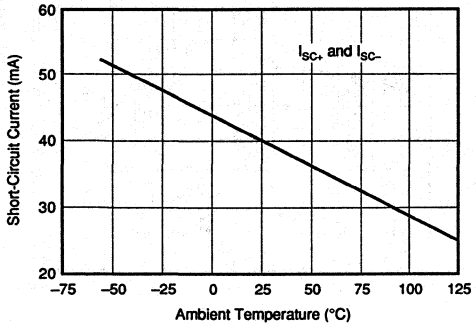
SMALL-SIGNAL TRANSIENT RESPONSE



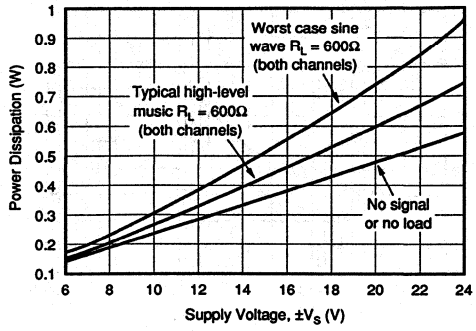
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_S = ±15V unless otherwise noted.

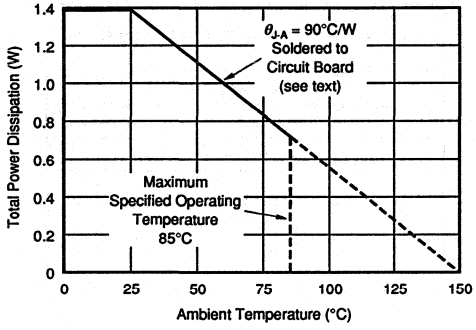
SHORT-CIRCUIT CURRENT vs TEMPERATURE



POWER DISSIPATION vs SUPPLY VOLTAGE



MAXIMUM POWER DISSIPATION vs TEMPERATURE



ELECTROSTATIC DISCHARGE SENSITIVITY

Any integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

APPLICATIONS INFORMATION

The OPA2604 is unity-gain stable, making it easy to use in a wide range of circuitry. Applications with noisy or high impedance power supply lines may require decoupling capacitors close to the device pins. In most cases 0.1µF ceramic capacitors are adequate.

DISTORTION MEASUREMENTS

The distortion produced by the OPA2604 is below the measurement limit of virtually all commercially available equipment. A special test circuit, however, can be used to extend the measurement capabilities.

Op amp distortion can be considered an internal error source which can be referred to the input. Figure 1 shows a circuit which causes the op amp distortion to be 101 times greater than normally produced by the op amp. The addition of R_3 to the otherwise standard non-inverting amplifier configuration alters the feedback factor or noise gain of the circuit. The closed-loop gain is unchanged, but the feedback available for error correction is reduced by a factor of 101. This extends the measurement limit, including the effects of the signal-source purity, by a factor of 101. Note that the input signal and load applied to the op amp are the same as with conventional feedback without R_3.

Validity of this technique can be verified by duplicating measurements at high gain and/or high frequency where the distortion is within the measurement capability of the test equipment. Measurements for this data sheet were made with the Audio Precision, System One which greatly simplifies such repetitive measurements. The measurement technique can, however, be performed with manual distortion measurement instruments.

CAPACITIVE LOADS

The dynamic characteristics of the OPA2604 have been optimized for commonly encountered gains, loads and operating conditions. The combination of low closed-loop gain and capacitive load will decrease the phase margin and may lead to gain peaking or oscillations. Load capacitance reacts with the op amp's open-loop output resistance to form an additional pole in the feedback loop. Figure 2 shows various circuits which preserve phase margin with capacitive load. Request Application Bulletin AB-028 for details of analysis techniques and applications circuits.

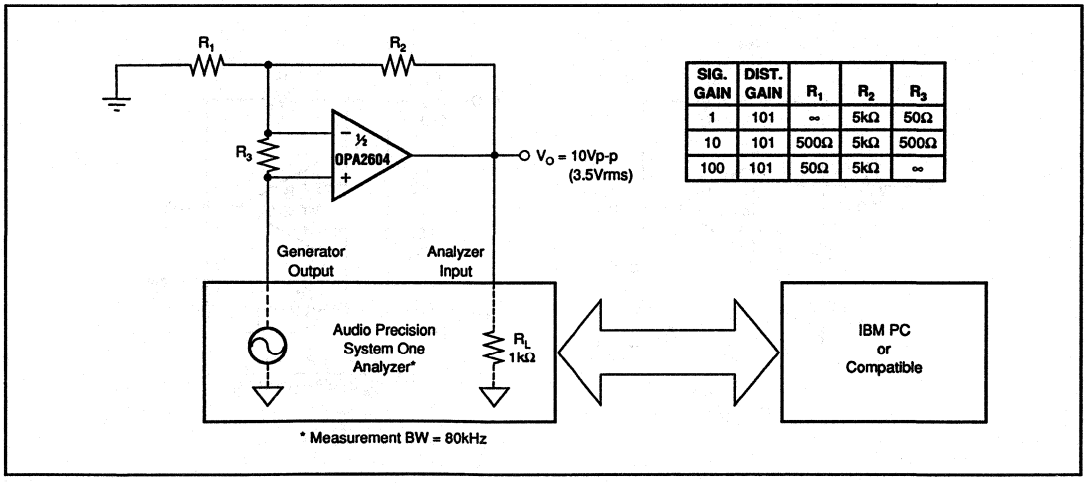
For the unity-gain buffer, Figure 2a, stability is preserved by adding a phase-lead network, R_C and C_C. Voltage drop across R_C will reduce output voltage swing with heavy loads. An alternate circuit, Figure 2b, does not limit the output with low load impedance. It provides a small amount of positive feedback to reduce the net feedback factor. Input impedance of this circuit falls at high frequency as op amp gain rolloff reduces the bootstrap action on the compensation network.

Figures 2c and 2d show compensation techniques for noninverting amplifiers. Like the follower circuits, the circuit in Figure 2d eliminates voltage drop due to load current, but at the penalty of somewhat reduced input impedance at high frequency.

Figures 2e and 2f show input lead compensation networks for inverting and difference amplifier configurations.

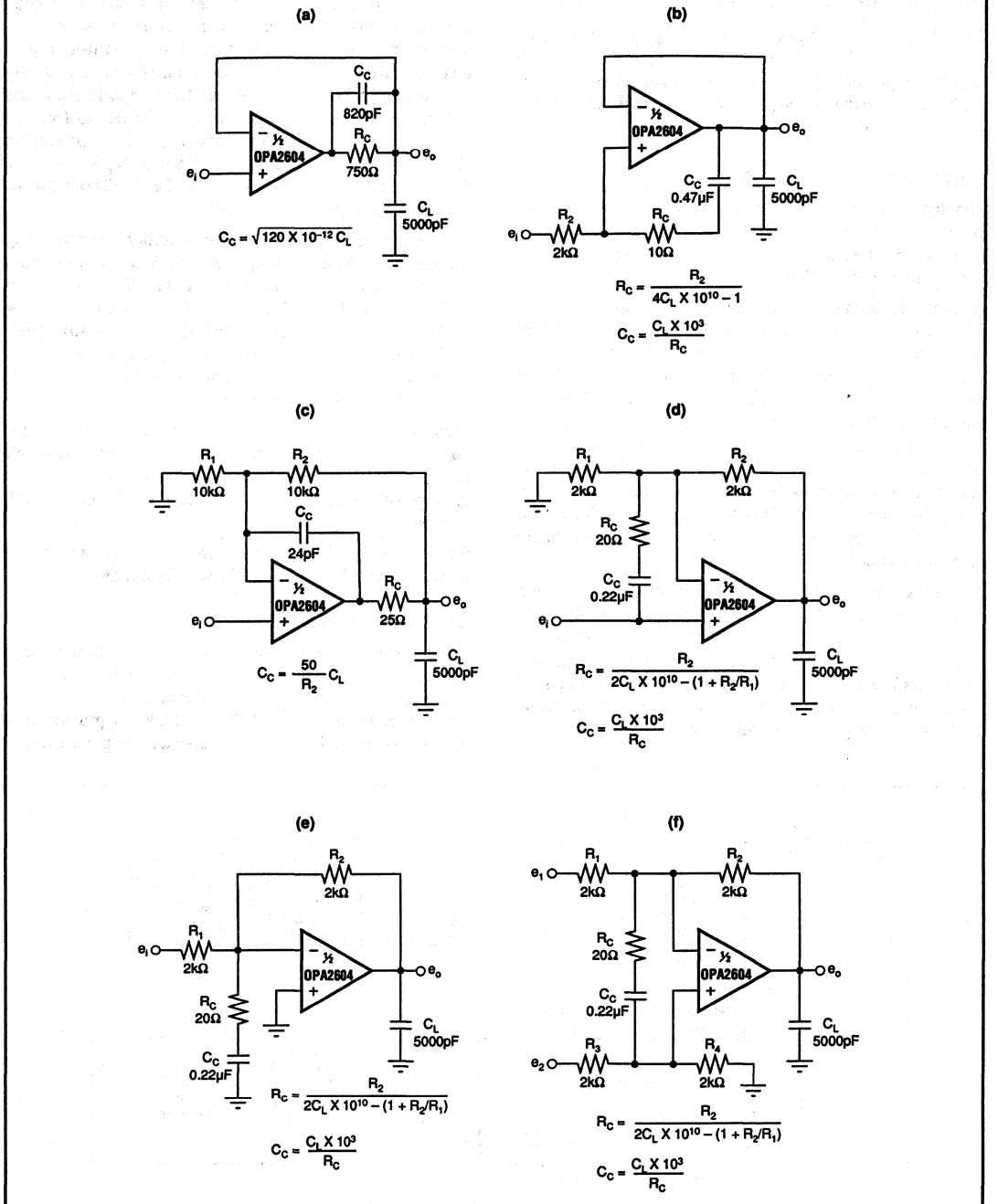
NOISE PERFORMANCE

Op amp noise is described by two parameters—noise voltage and noise current. The voltage noise determines the noise performance with low source impedance. Low noise bipolar-input op amps such as the OPA27 and OPA37 provide very low voltage noise. But if source impedance is greater than a



SIG. GAIN	DIST. GAIN	R_1	R_2	R_3
1	101	∞	5kΩ	50Ω
10	101	500Ω	5kΩ	500Ω
100	101	50Ω	5kΩ	∞

FIGURE 1. Distortion Test Circuit.



NOTE: Design equations and component values are approximate. User adjustment is required for optimum performance.

FIGURE 2. Driving Large Capacitive Loads.

few thousand ohms, the current noise of bipolar-input op amps react with the source impedance and will dominate. At a few thousand ohms source impedance and above, the OPA2604 will generally provide lower noise.

POWER DISSIPATION

The OPA2604 is capable of driving 600Ω loads with power supply voltages up to ±24V. Internal power dissipation is increased when operating at high power supply voltage. The typical performance curve, Power Dissipation vs Power Supply Voltage, shows quiescent dissipation (no signal or no load) as well as dissipation with a worst case continuous sine wave. Continuous high-level music signals typically produce dissipation significantly less than worst case sine waves.

Copper leadframe construction used in the OPA2604 improves heat dissipation compared to conventional plastic packages. To achieve best heat dissipation, solder the device directly to the circuit board and use wide circuit board traces.

OUTPUT CURRENT LIMIT

Output current is limited by internal circuitry to approximately ±40mA at 25°C. The limit current decreases with increasing temperature as shown in the typical curves.

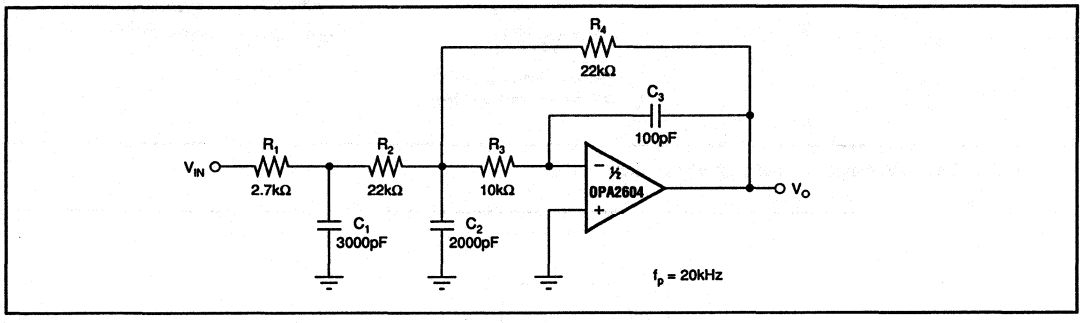


FIGURE 3. Three-Pole Low-Pass Filter.

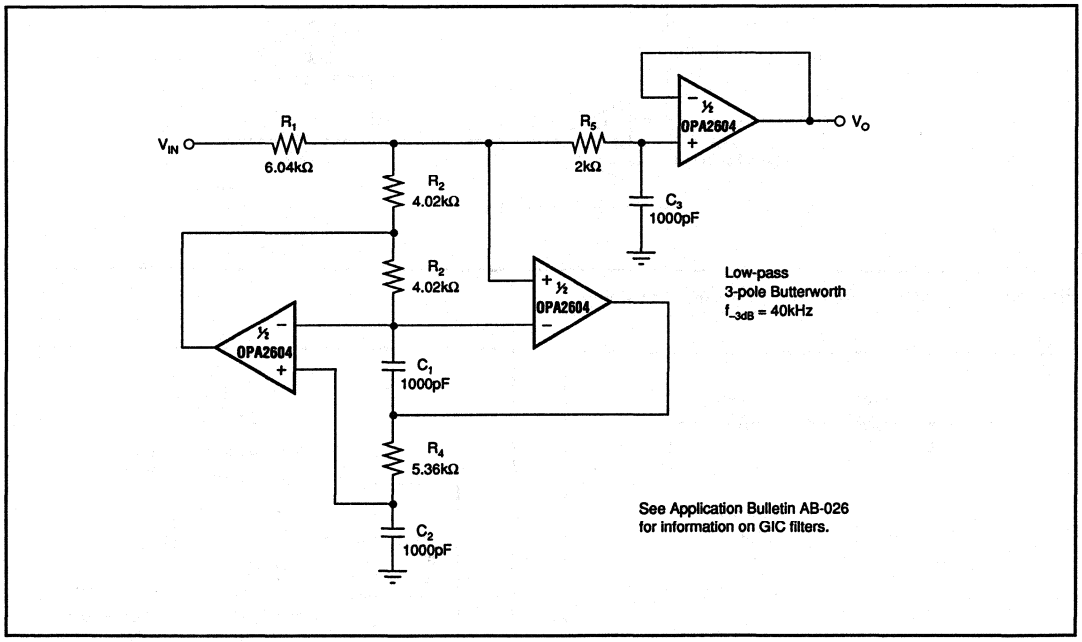


FIGURE 4. Three-Pole Generalized Immittance Converter (GIC) Low-Pass Filter.

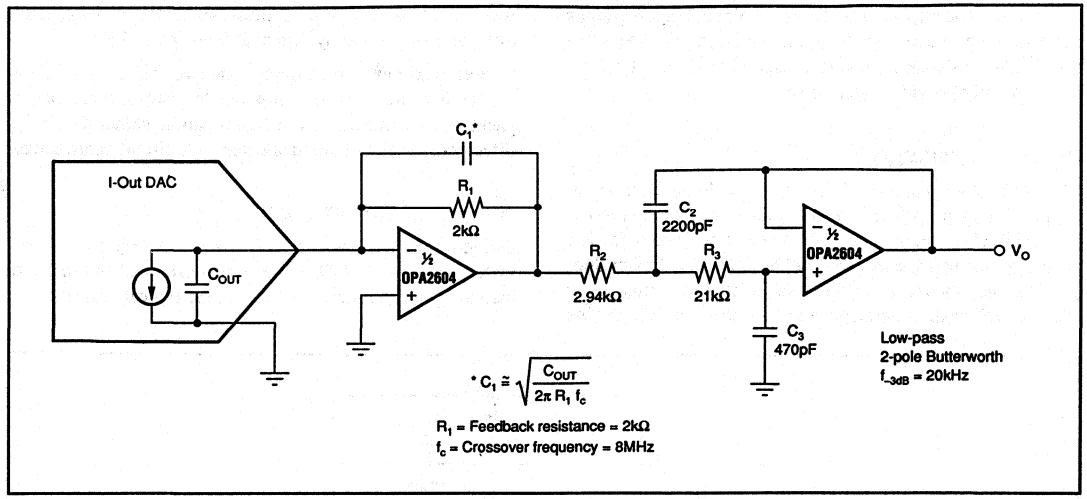


FIGURE 5. DAC I/V Amplifier and Low-Pass Filter.

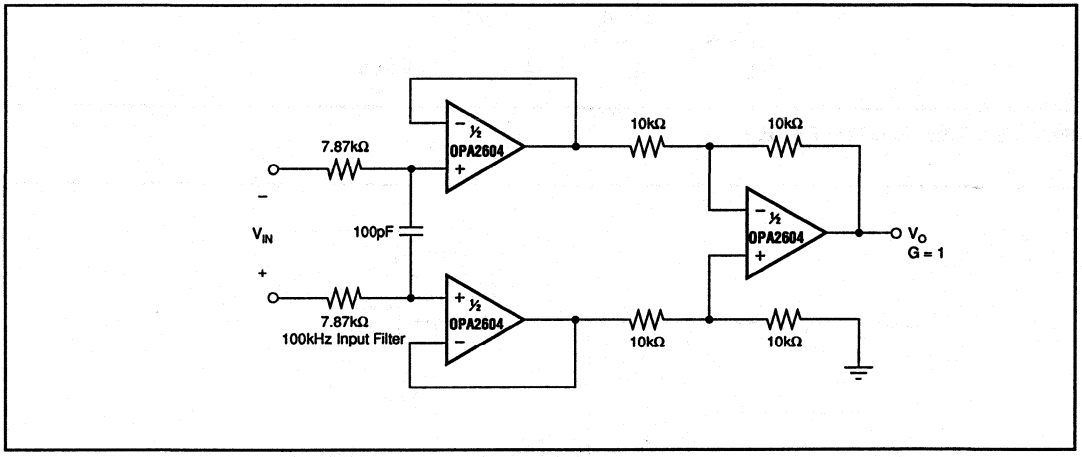


FIGURE 6. Differential Amplifier with Low-Pass Filter.

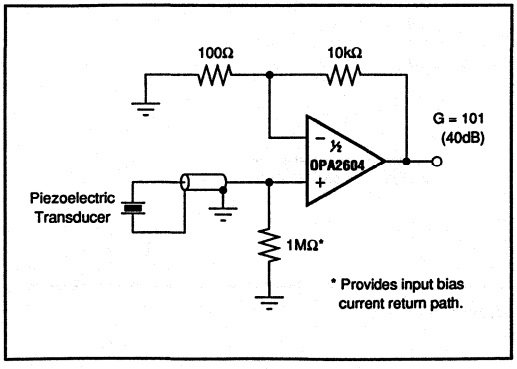


FIGURE 7. High Impedance Amplifier.

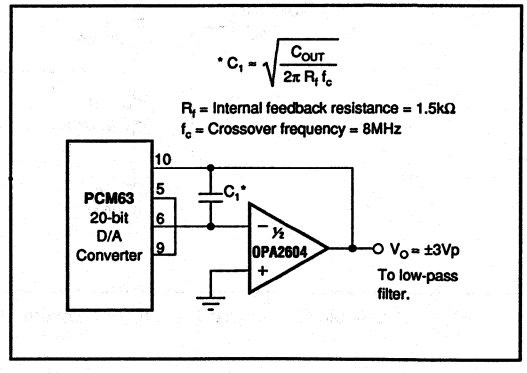


FIGURE 8. Digital Audio DAC I-V Amplifier.

SOUND QUALITY

The following discussion is provided, recognizing that not all measured performance behavior explains or correlates with listening tests by audio experts. The design of the OPA2604 included consideration of both objective performance measurements, as well as an awareness of widely held theory on the success and failure of previous op amp designs.

SOUND QUALITY

The sound quality of an op amp is often the crucial selection criteria—even when a data sheet claims exceptional distortion performance. By its nature, sound quality is subjective. Furthermore, results of listening tests can vary depending on application and circuit configuration. Even experienced listeners in controlled tests often reach different conclusions.

Many audio experts believe that the sound quality of a high performance FET op amp is superior to that of bipolar op amps. A possible reason for this is that bipolar designs generate greater odd-order harmonics than FETs. To the human ear, odd-order harmonics have long been identified as sounding more unpleasant than even-order harmonics. FETs, like vacuum tubes, have a square-law I-V transfer function which is more linear than the exponential transfer function of a bipolar transistor. As a direct result of this square-law characteristic, FETs produce predominantly even-order harmonics. Figure 9 shows the transfer function of a bipolar transistor and FET. Fourier transformation of both transfer functions reveals the lower odd-order harmonics of the FET amplifier stage.

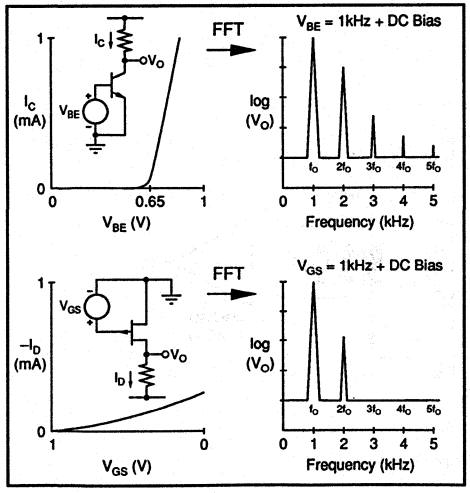
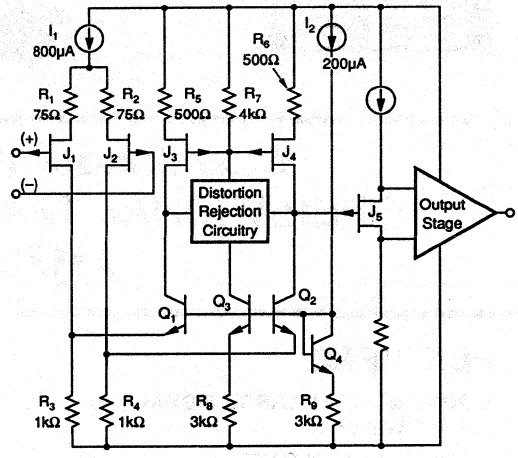


FIGURE 9. I-V and Spectral Response of NPN and JFET.



THE OPA2604 DESIGN

The OPA2604 uses FETs throughout the signal path, including the input stage, input-stage load, and the important phase-splitting section of the output stage. Bipolar transistors are used where their attributes, such as current capability are important and where their transfer characteristics have minimal impact.

The topology consists of a single folded-cascode gain stage followed by a unity-gain output stage. Differential input transistors J_1 and J_2 are special large-geometry, P-channel JFETs. Input stage current is a relatively high 800µA, providing high transconductance and reducing voltage noise. Laser trimming of stage currents and careful attention to symmetry yields a nearly symmetrical slew rate of ±25V/µs.

The JFET input stage holds input bias current to approximately 100pA, or roughly 3000 times lower than common bipolar-input audio op amps. This dramatically reduces noise with high-impedance circuitry.

The drains of J_1 and J_2 are cascoded by Q_1 and Q_2, driving the input stage loads, FETs J_3 and J_4. Distortion reduction circuitry (patent pending) linearizes the open-loop response and increases voltage gain. The 20MHz bandwidth of the OPA2604 further reduces distortion through the user-connected feedback loop.

The output stage consists of a JFET phase-splitter loaded into high speed all-NPN output drivers. Output transistors are biased by a special circuit to prevent cutoff, even with full output swing into 600Ω loads.

The two channels of the OPA2604 are completely independent, including all bias circuitry. This eliminates any possibility of crosstalk through shared circuits—even when one channel is overdriven.

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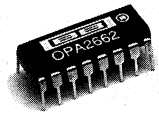


OPA2662

ADVANCE INFORMATION
SUBJECT TO CHANGE

Wide Bandwidth, Dual, Power OPERATIONAL TRANSCONDUCTANCE AMPLIFIER

FEATURES

- 200MHz SMALL/LARGE SIGNAL BANDWIDTH
- 2000V/µs SLEW RATE
- VOLTAGE-CONTROLLED CURRENT SOURCE
- HIGH OUTPUT CURRENT: ±75mA
- LOW DIFFERENTIAL GAIN/PHASE ERROR

APPLICATIONS

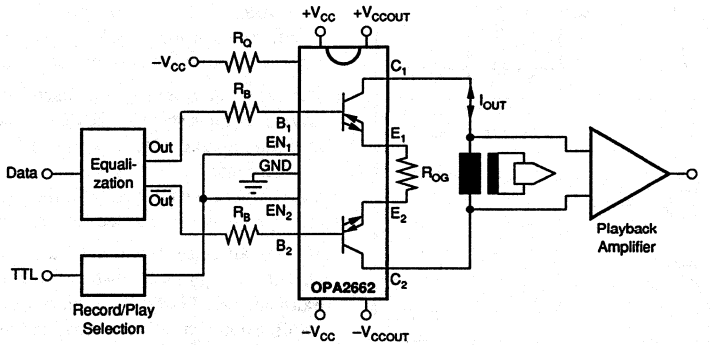
- VIDEO EQUIPMENT (HDTV)
- FIBER OPTIC SYSTEMS
- DRIVER DEVICE FOR VIDEO TAPE HEADS, LEDs, AND LASER DIODES
- VIDEO BUFFER OR LINE DRIVER
- SAW FILTER (DIFFERENTIAL)

DESCRIPTION

The OPA2662 is a versatile driver device for ultra-wide bandwidth systems, including high-resolution video, RF and IF circuitry, and communications and test equipment. The OPA2662 includes two power voltage-controlled current sources in a 16-pin DIP or SO package and is specified for the industrial temperature range (–40°C to +85°C).

The current sources can be viewed as "ideal transistors" which are, however, self-biased and bipolar.

The output current is zero for zero differential input voltage. The OTAs provide a 200MHz large-signal bandwidth and a 2000V/µs slew rate, and each collector output stage can deliver ±75mA output current. The quiescent current of both OTAs can be adjusted with an external resistor, and each OTA can be switched on or off within some ns by logic TTL level signal.



Analog/Digital Video Tape Record Amplifier

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Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

PDS-1129

SPECIFICATIONS

ELECTRICAL

Typical at I_O = 30mA, V_S = ±5VDC, T_A = +25°C unless otherwise specified. EN = Logic "HI", R_E = 100Ω, R_C = 33Ω.

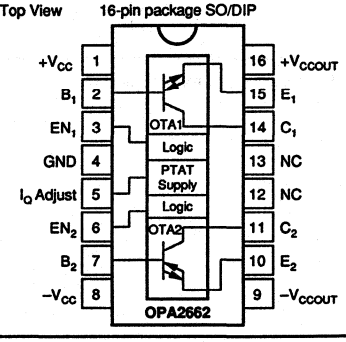
PARAMETER	CONDITIONS	OPA2662 MIN	OPA2662 TYP	OPA2662 MAX	UNITS
OTA TRANSCONDUCTANCE					
Transconductance	V_C = 0V	150	300		mA/V
OTA INPUT OFFSET VOLTAGE					
Initial			+7		mV
vs Temperature			50		µV/°C
vs Supply (tracking)	V_S = ±4.5V to ±5.5V				dB
vs Supply (non-tracking)	V+ = 4.5V to 5.5V				dB
vs Supply (non-tracking)	V– = –4.5V to –5.5V				dB
OTA B-INPUT BIAS CURRENT					
Initial			1.5		µA
vs Temperature					nA/°C
vs Supply (tracking)	V_S = ±4.5V to ±5.5V			±750	nA/V
vs Supply (non-tracking)	V+ = 4.5V to 5.5V			±1500	nA/V
vs Supply (non-tracking)	V– = –4.5V to –5.5V			±500	nA/V
OTA OUTPUT BIAS CURRENT					
Output Bias Current	V_C = 0V		500		µA
vs Temperature					nA/°C
vs Supply (tracking)	V_S = ±4.5V to ±5.5V			±25	µA/V
vs Supply (non-tracking)	V+ = 4.5V to 5.5V			±25	µA/V
vs Supply (non-tracking)	V– = –4.5V to –5.5V			±25	µA/V
OTA OUTPUT					
Output Current		±70	±75		mA
Output Voltage Compliance	I_C = ±1mA	±4.0			V
Output Impedance			3.7 || 20		kΩ || pF
OTA INPUT IMPEDANCE					
Input Impedance			2 || 1.0		MΩ || pF
OTA INPUT NOISE					
Voltage Noise Density, f = 100kHz			5		nV/√Hz
OTA DYNAMIC RESPONSE					
Small Signal Bandwidth	V_O = ±100mV		200		MHz
Full Power Bandwidth	R_L = 33Ω, V_O = ±2V		200		MHz
Differential Gain Error	3.58MHz, at 0.7V		0.1		%
Differential Phase Error	3.58MHz, at 0.7V		0.05		Degrees
Harmonic Distortion, 2nd Harmonic	f = 10MHz, V_O = 0.5Vp-p		–68		dBc
Slew Rate	5V Step		2000		V/µs
Settling Time 0.1%	2V Step				ns
Rise Time (10% to 90%)	V_O = 100mVp-p				ns
	5V Step		2.2		ns
Group Delay Time			600		ps
POWER SUPPLY					
Voltage, Rated			±5		V
Derated Performance		±4.5		±5.5	V
Quiescent Current (Programmable, Useful Range)			4–32		mA

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage	±6V
Input Voltage	±V_{CC} ±0.7V
Operating Temperature	–40°C to +85°C
Storage Temperature	–40°C to +125°C
Junction Temperature	+159°C
Lead Temperature (soldering, 10s)	+300°C

PIN CONFIGURATION

Top View 16-pin package SO/DIP



APPLICATIONS INFORMATION

The OPA2662 is a versatile driver device designed for wide-bandwidth systems, including high-performance video recorders and equipment and light transmission systems. The OPA2662 includes two integrated voltage-controlled current sources in a 16-pin DIP or SO package.

The voltage-controlled current sources, or Operational Transconductance Amplifiers (OTA), can be viewed as "ideal transistors."

Like a transistor, they have three terminals—a high-impedance input (base), low-impedance input/output (emitter), and current output (collector). The OTAs, however, are self-biased and bipolar. The output current is zero for zero differential input voltage. AC inputs centered at about zero produce an output current which is bipolar and centered at about zero. The transconductance of both OTAs can be adjusted with an external resistor, allowing bandwidth, quiescent current, and gain tradeoffs to be optimized.

The OTA provides a 200MHz large-signal bandwidth and a 2000V/µs slew rate. Each output stage can deliver ±75mA output current.

When the two collectors of the OPA2662 are combined parallel to each other, the capability to deliver output current is doubled, which enables it to drive medium-power laser diodes. When the collector is combined with the emitter terminal, the OPA2662s can be interconnected as voltage buffers, two channel output multiplexers or line drivers. The high output current capability allows the OPA2662 to drive 50Ω and 75Ω lines with ±3V output swing, making it ideal for RF, IF, and video applications.

Used as basic building blocks, the OTAs can simplify the design of complex signal processing stages in video systems, communications, high-speed light measurement equipment, and high-speed data acquisition circuitry.

The OPA2662 is specified for the industrial temperature range (–40°C to +85°C).

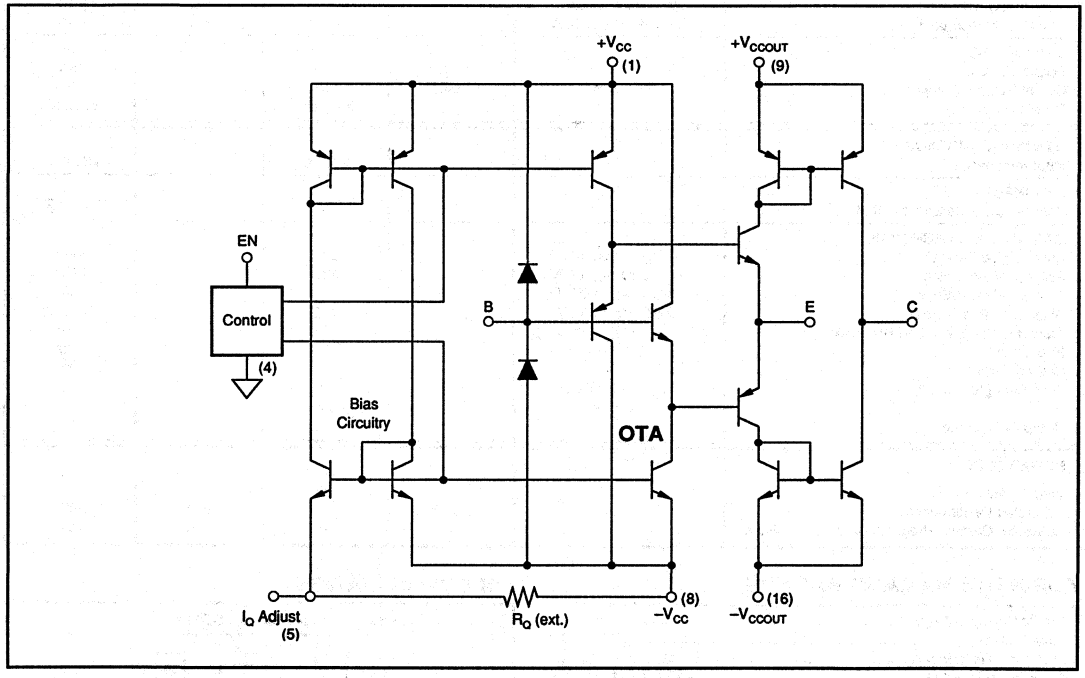
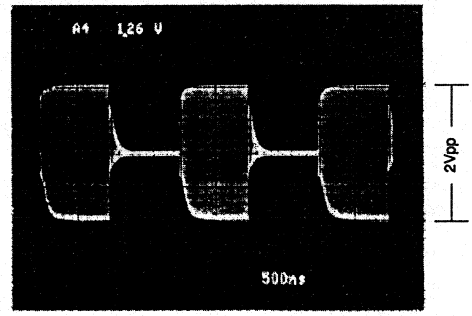


FIGURE 1. Simplified Circuit Diagram.

TTL Logic Levels V_{IL} (logic "LO") = 0 → 0.8V
V_{IH} (logic "HI") = 2.0 → 5V
I_{IL} (logic "LO", V_{IL} = 0V) = typ
I_{IH} (logic "HI", V_{IH} = 2.7V) = TBD typ
OTA Quiescent Current (V_{IL} 0 → 0.8V) = µA
OTA Output Impedance (V_{IL} 0 → 0.8V) = MΩ



OPA2662
Selection Time < 100ns
OFF to ON
ON to OFF
V_{OUT} 10% to 90%

FIGURE 2. Digital EN Input.

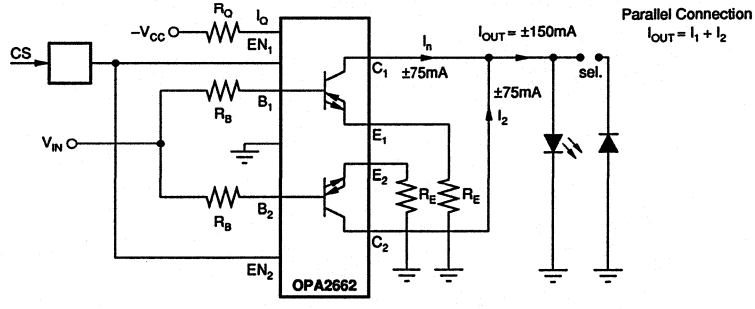


FIGURE 3. Analog/Digital LED and Laser Diode Driver for Fiber Optic Transmission Systems, Measurement Equipment.

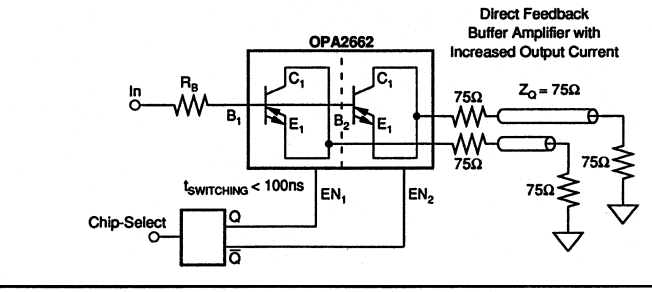


FIGURE 4. Two Channel Output Driver.

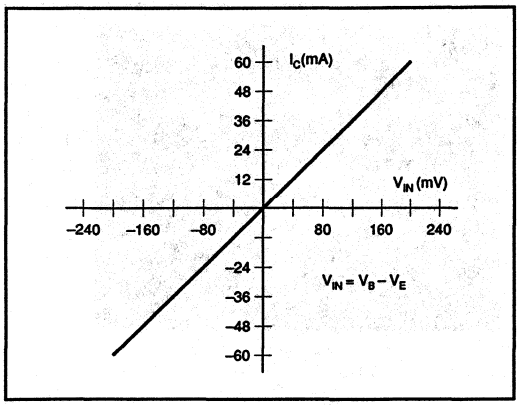


FIGURE 5. OTA Transfer Characteristic.

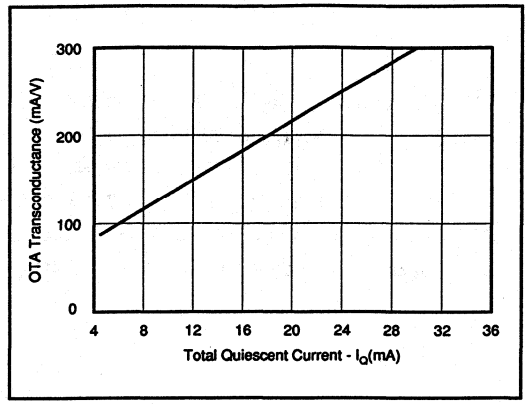


FIGURE 6. OTA Transconductance vs Total Quiescent Current.

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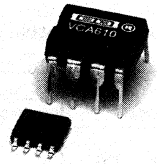


VCA610

**ADVANCED INFORMATION
SUBJECT TO CHANGE**

WIDEBAND VOLTAGE CONTROLLED AMPLIFIER

FEATURES

- WIDE GAIN CONTROL RANGE: 80dB
- SMALL PACKAGE: 8-pin SOIC or DIP
- WIDE BANDWIDTH: 35MHz
- LOW NOISE FIGURE: 3.5dB
- FAST OVERLOAD RECOVERY: 50ns
- FAST GAIN SLEW RATE: 80dB/µs
- LOW DISTORTION: –70dBc IMD

APPLICATIONS

- ULTRASOUND
- VIDEO AGC AMPLIFIERS
- ANALYTICAL INSTRUMENTATION
- SONAR
- ACTIVE FILTERS
- HIGH SPEED SIGNAL PROCESSING

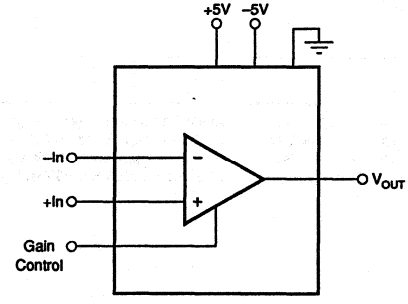
DESCRIPTION

The VCA610 is a stable, wideband, voltage controlled gain amplifier. It provides linear-dB gain control with op amp style, high impedance inputs. It is designed to be used as a flexible gain control element in a variety of electronic systems.

The VCA610 has a gain control range of 80dB (–40dB to +40dB) providing both gain and attenuation for maximum flexibility in a small 8-pin SOIC or plastic dual in line package. The broad attenuation range can be used for gradual or controlled channel turn-on and turn-off for applications in which abrupt gain changes can create artifacts or other errors. Group delay variation from unit to unit is less than ±2ns across a bandwidth of 1 to 15MHz.

The VCA610 has a noise figure of 3.5dB (with an R_S of 200Ω) including the effects of both current and voltage noise, 2.3pA/$\sqrt{Hz}$ and 2.2nV/$\sqrt{Hz}$ respectively. Instantaneous output dynamic range is 75dB for gains of 0dB to +40dB with 1MHz noise bandwidth. The output is capable of driving 50Ω. The high speed, 80dB/µs, gain control signal is an easy to generate unipolar voltage that varies the gain linearly in dB/V.

The VCA610 is designed with a very fast overload recovery time of only 50ns. This allows a large signal transient to overload the output at high gain, without obscuring low-level signals following closely behind. Distortion is also optimized, particularly for low-level signals. Intermodulation distortion is a very low –70dBc for low-level signals. The excellent overload recovery time and distortion specifications optimize this device for low-level doppler measurements.



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Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL

Specifications may change in any manner without notice. All specifications over 1 to 15MHz passband, at +25°C, R_L = 500Ω, R_S = 0Ω, and V_S = ±5VDC unless otherwise noted.

PARAMETER	CONDITIONS	VCA610AP/AU MIN	VCA610AP/AU TYP	VCA610AP/AU MAX	UNITS
INPUT NOISE					
Noise Figure	G = +40dB, R_S = 200Ω		3.5		dB
Input Voltage Noise	G = +40dB, R_S = 0Ω		2.2		nV/√Hz
Input Current Noise	G = –40dB to +40dB		2.3		pA/√Hz
INPUT					
Input Impedance	Common-mode		1 || 1		MΩ || pF
Bias Current			12		µA
Maximum Signal Level		2.0			Vp-p
GAIN					
Range		–40		+40	dB
Accuracy, (1)			±1.0		dB
Variation, part to part, (2)				±1.0	dB
GAIN CONTROL					
Control Law	Full Range		Logarithmic		
Scaling			40		dB/V
Control Voltage (V_C)		0		–2	V
Slew Rate			80		dB/µs
Feedthrough	Output Referred		–40		dB
Impedance			1 || 1		MΩ || pF
FREQUENCY RESPONSE					
Bandwidth, Small-Signal	–3dB	35			MHz
Bandwidth, Large-Signal	V_O = 1Vp-p	25			MHz
Group Delay Variation	Δ Gain = 20dB			±2.0	ns
Output Slew Rate	V_O = 2Vp-p		100		V/µs
Settling Time	V_{IN} = 10mVp-p, (3)		50		ns
Overload Recovery	(7)		50		ns
Two-tone Intermodulation Distortion	Small-Signal, (5)		–70		dBc
Two-tone IMD Intercept	(5)		25		dBm
OUTPUT					
Maximum Output			2.5		Vp-p
1dB Compression Point		2.0			Vp-p
Output Voltage Limit			Symmetrical to Ground (±10%)		
Short-Circuit Current	Continuous to Common	±50			mA
Instantaneous Dynamic Range (IDR)					
Gain = 0dB to +40dB	(4), V_O = 1Vrms		75		dB
Gain = –20dB	(4), V_O = 106mVrms		70		dB
Gain = –40dB	(4), V_O = 10.6mVrms		55		dB
POWER SUPPLY					
Specification	±5VDC Recommended	±4.5		±5.5	VDC
Operation		±4		±6	VDC
PSRR	Output Referred	–40			dB
Quiescent Current	G = +40dB		24		mA
TEMPERATURE					
Operation		–25		+85	°C
θ_{JA}					
AP			90		°C/W
AU			100		°C/W
MECHANICAL					
Package			Plastic, DIP/SOIC		

NOTES: (1) Accuracy is deviation from Control Law over entire gain range. (2) Variation is gain variation from part to part over entire gain range; Gain is tested at gains of –40dB, –20dB, 0dB, +20dB and +40dB. (3) Settling to ±0.1% of Full Scale with maximum gain step. (4) With R_S = 0Ω, and noise bandwidth of 1MHz. IDR = 20 log (V_O/(e_{ORMS} x √BW)); where V_O is rms output voltage, e_{ORMS} is output noise spectral density, and BW is noise bandwidth. (5) V_{IN} = 7mVp-p, V_{OUT} = 700mVp-p (250mVrms); Output Power = –10dBm/tone, equal amplitude tones of 5MHz ±500Hz, G = +40dB. (6) At +40dB gain and 8dB/µs slew rate. (7) Gain = +40dB; Input step of 2V to 2mV.

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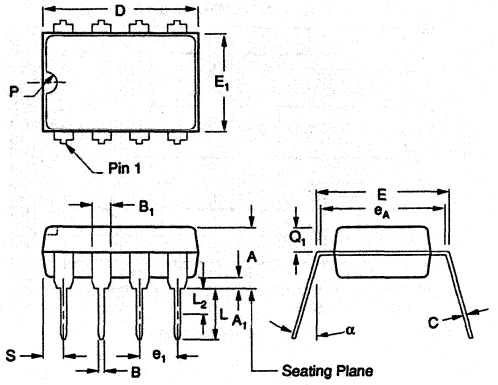
MECHANICALS

P Package — 8-Pin Plastic DIP

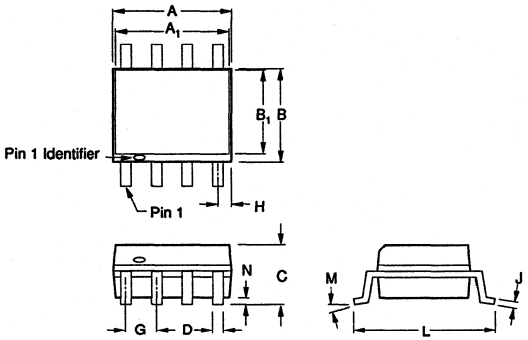


DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.155	.200	3.94	5.08
A_1	.020	.050	0.51	1.27
B	.014	.020	0.36	0.51
B_1	.045	.065	1.14	1.65
C	.008	.012	0.20	0.30
D (1)	.370	.400	9.40	10.16
E	.300	.325	7.62	8.26
E_1	.240	.260	6.10	6.60
e_1	.100 BASIC		2.54 BASIC	
e_A	.300 BASIC		7.62 BASIC	
L	.125	.150	3.18	3.81

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
L_2 (2)	0	.030	0.00	0.76
α	0°	15°	0°	15°
P	.015	.050	0.38	1.270
Q_1	.040	.075	1.02	1.91
S (1)	.015	.050	0.38	1.27

(1) Not JEDEC Std.
(2) e_1 and e_A applies in zone L_2 when unit installed.
NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

U Package — 8-Pin SOIC

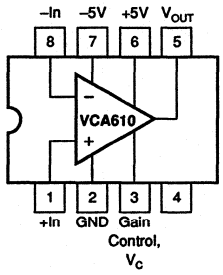


DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.185	.201	4.70	5.11
A_1	.178	.201	4.52	5.11
B	.146	.162	3.71	4.11
B_1	.130	.149	3.30	3.78
C	.054	.145	1.37	3.69
D	.015	.019	0.38	0.48
G	.050 BASIC		1.27 BASIC	
H	.018	.026	0.46	0.66
J	.008	.012	0.20	0.30
L	.220	.252	5.59	6.40
M	0°	10°	0°	10°
N	.000	.012	0.00	0.30

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

PIN CONFIGURATION

Top View

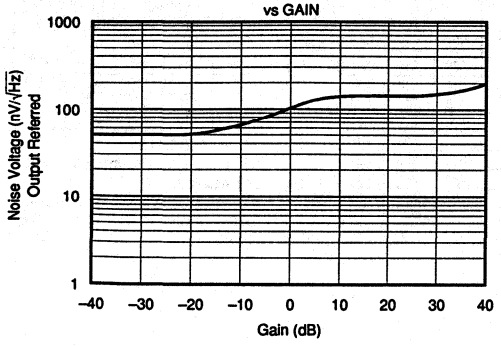


The use of the inverting input (–In, pin 8) is recommended. If not used, the noninverting input (+In, pin 1) should be grounded as close to package as possible for minimum noise pickup.

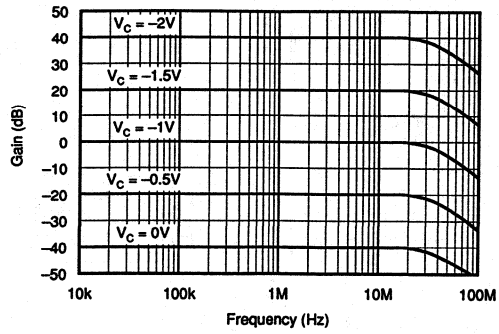
The VCA610 is available in 8-pin plastic DIP and SOIC packages.

TYPICAL PERFORMANCE CURVES

TYPICAL OUTPUT NOISE VOLTAGE vs GAIN



GAIN vs SMALL SIGNAL BANDWIDTH



3 Instrumentation Amplifiers

Instrumentation amplifiers are generally used in applications where extracting and accurately amplifying low level differential signals riding on high common-mode voltages (±10V) is very important. Such applications require high input impedance, high CMRR, low input noise, and excellent DC level stability (low offset voltage drift).

Instrumentation amplifiers are used as transducer amplifiers for various types of transducers such as strain gauge bridges, load cells, thermistor networks, thermocouples, current shunts, biological probes, weather gauges, and so forth. Other applications include recorder preamplifiers, multiplexer buffers, servo error amplifiers, current sensors, signal conditioners in process control and data acquisition systems, and in general measurements of small differential signals riding on common-mode voltages.

The small size, low cost, and high performance of these amplifiers offer an attractive approach for data acquisition applications: assigning a fixed-gain amplifier to each transducer and locating the amplifier physically near the transducer. This approach largely eliminates common-mode noise pickup problems since a high level signal (rather than a low level transducer signal) is then transmitted to the data gathering station. The result is a higher signal/noise ratio at the output.

The following Selection Guides show parameters for the high grade. Models shown in **boldface** are products included in this supplement.

INSTRUMENTATION AMPLIFIERS

Description	Model	Gain Range	Gain Accuracy, G=100 25°C, max(%)	Gain Drift, G=100 (ppm/°C)	Non-Linearity G=100 max(%)	Input Parameters CMR[6] min(dB)	Input Parameters Offset Voltage vs Temp max(µV/°C)	Dynamic Response, G=100 –3dB BW (kHz)	Temp Range[1]	Pkg	Page No.
	INA114	**1-10,000[2]**	**0.5**	**50**	**±0.002**	**96**	**±(50+100/G)**	**10**	**Ind**	**DIP, SOIC**	**S-3.48**
	INA131	**100**	**0.2**	**10**	**±0.002**	**110**	**±50**	**50**	**Ind**	**DIP. SOIC**	**S-3.75**
Very High Accuracy	**INA120**	**1, 10, 100, 1000**	**0.5**	**30**	**±0.01**	**96**	**±(0.25±10/G)**	**20**	**Ind**	**DIP**	**S-3.65**
	INA104	1-1000[2]	0.15	22[3]	±0.003	96	±(0.25±10/G)	25	Ind	DIP	3-34
	INA101	1-1000[2]	0.03	22[3]	±0.003	96	±(0.25±10/G)	25	Ind, Mil	DIP	3-11
										TO-100,	3-11
		1-1000[2]	0.3	22[3]	±0.007	90	±(2±20/G) typ	25	Com	DIP	3-11
										SOIC	3-11
Low Quiescent Power	**INA102[8]**	**1,10,100, 1000**	**0.15**	**15**	**±0.02**	**90**	**±(2±5/G)**	**3**	**Ind**	**DIP**	**S-3.4**
		1,10,100, 1000	**0.4**	**20**	**±0.05**	**80**	**±(5±10/G)**	**3**	**Com, Ind**	**DIP**	**S-3.4**
										SOIC	**S-3.4**
Low Noise, Low Distortion	**INA103**	**1-1000[2]**	**0.1**	**25**	**±0.004**	**100**	**±(0.5+10/G) typ**	**800**	**Ind**	**DIP**	**S-3.17**
		1-1000[2]	**0.25**	**25**	**±0.010**	**90**	**±(0.5+20/G) typ**	**800**	**Com**	**DIP**	**S-3.17**
Fast Settling FET Input	INA110[8]	1,10,100, 200,500	0.1	20	±0.01	96	±(2±50/G)	470	Ind	DIP,	3-65
		1,10,100, 200, 500	0.2	6 typ	±0.02	87	±(2±20/G) typ	470	Com	DIP,	3-65
										SOIC	3-65
	INA111	**1-10,000[2]**	**0.3**	**50**	**±0.01**	**96**	**±(500+3000/G)**	**470**	**Ind**	**DIP, SOIC**	**S-3.46**

(Continued on next page)

INSTRUMENTATION AMPLIFIERS (Continued)

Description	Model	Gain Range	Gain Accuracy, G=100 25°C, max(%)	Gain Drift, G=100 (ppm/°C)	Non-Linearity G=100 max(%)	Input Parameters CMR[6] min(dB)	Input Parameters Offset Voltage vs Temp max(µV/°C)	Dynamic Response, G=100 –3dB BW (kHz)	Temp Range[1]	Pkg	Page No.
Buffer,	3627	1V/V,fixed	0.01[3]	5	±0.001[3]	100	20	800[3]	Ind	TO-99	3-158
Unity-Gain	**INA105[8]**	**1V/V,fixed**	**0.01[3]**	**5**	**±0.001[3]**	**86[5]**	**10**	**1000[3]**	**Ind**	**TO-99**	**S-3.32**
Difference		1V/V,fixed	0.025[3]	5	±0.001[3]	72[5]	5 typ	1000[3]	Com	DIP,	S-3.32
Amp										SOIC	S-3.32
Gain of 10	INA106	10V/V,fixed	0.01[4]	10	±0.001[4]	100[5]	2	500[4]	Ind	TO-99	3-57
Difference		10V/V,fixed	0.025[4]	4 typ	±0.001[4]	86[5]	0.2 typ	500[4]	Com	DIP	3-57
High Com.	**INA117**	**1V/V,fixed**	**0.02[3]**	**10[3]**	**±0.001[3]**	**86[5]**	**20**	**200[3]**	**Ind**	**TO-99**	**S-3-50**
Mode Volt.		**1V/V,fixed**	**0.05[3]**	**10[3]**	**±0.001[3]**	**74[5]**	**40**	**200[3]**	**Com**	**DIP**	**S-3-50**
Difference (200VDC CMV)											
4-20mA Loop	**RCV420**	**0.3125V/mA**	**0.05**	**25**	**±0.002**	**86**	**25[7]**	**150**	**Ind**	**DIP**	**S-3-88**
Receiver		**0.3125V/mA**	**0.1**	**50**	**±0.002**	**72**	**50[7]**	**150**	**Com**	**DIP**	**S-3-88**

NOTES: (1) Com = 0°C to +70°C, Ind = –25°C to +85°C, Mil = –55°C to +125°C. (2) Set with external resistor. (3) Unity-gain. (4) Gain = 10. (5) No source imbalance. (6) DC to 60Hz, Gain = 10, 1kΩ unbalanced. (7) RTO. (8) BS 9000 Screening is available.

PROGRAMMABLE GAIN AMPLIFIERS

Description	Model	Gain Range	Gain Accuracy, G=100 25°C, max(%)	Gain Drift, G=100 (ppm/°C)	Non-Linearity G=100 max(%)	Input Parameters CMR[6] min (dB)	Input Parameters Offset Voltage vs Temp max (µV/°C)	Dynamic Response, G=100 ±3dB BW (kHz)	Temp Range[1]	Pkg	Page No.
Noninverting	PGA100	Gain set	0.02	10	±0.005	NA	6 typ	5MHz	Ind	DIP	3-85
Input		word 1, 2, 4, 8...128									
	PGA102	Gain set	0.01	20	±0.01		3,G=100	250	Ind	DIP	3-93
		with 2-bit 100	0.02	50	±0.01		3,G=100	250	Com	DIP	3-93
Instr.	PGA200	Gain set	0.02	10	±0.003	96	0.4,G=100	30	Ind	DIP	3-103
Amplifier		word 1, 10,									
Input		100, 1000									
Fast	**PGA202**	**Gain set**	**0.15**	**5**	**±0.012**	**86**	**±(3+25/G)**	**1000**	**Ind, Com**	**DIP**	**S-3.77**
Settling		**word 1, 10,**									
2µs to 0.01%		**100, 1000**									
Differential	**PGA203**	**Gain set**	**0.15**	**5**	**±0.012**	**86**	**±(3+25/G)**	**1000**	**Ind, Com**	**DIP**	**S-3.77**
		word 1, 2, 4, 8									
Differential	3606	Gain set	0.02	10	±0.004	90,G=1	±(1+20/G)	40	Ind	DIP	3-150
		word 1, 2, 4, 8...1024									

NOTES: (1) Com = 0°C to +70°C, Ind = –25°C to +85°C. (2) Set with external resistor. (3) Unity-gain. (4) Gain = 10 (5) No source imbalance. (6) DC to 60Hz, Gain = 10, 1kΩ unbalanced.

PRECISION CURRENT TRANSMITTERS

Description	Model	Span: Untrimmed Error, max (%)	Span: Non-linearity, max (%)	Span: Temp Drift[1] (ppm/°C)	Input Parameters: Offset Voltage: Offset Voltage max	Input Parameters: Offset Voltage: vs Temp max (µV/°C)	Input Parameters: CMR, DC, min (dB)	Output Parameters: Current Range (mA)	Output Parameters: Offset Current Error, max (µA)	Output Parameters: FS Output Current Error, max (µA)	Temp Range[2]	Pkg	Page No.
Two-Wire	XTR101	5	0.01	±100	±30µV	±0.75	90	4-20	±6	±30	Ind	DIP SOIC	S-3.100 S-3.100
Two-Wire RTD Linearity Compensation	XTR103	1[5]	0.01	±50	±2500	±2.5	86	4-20	±25	50	Ind[3]	DIP SOIC	S-3.116 S-3.116
Two-Wire Bridge Linearity Compensation	XTR104	1[5]	0.01	±50	±2500	±2.5	86	4-20	±25	±50	Ind[3]	DIP SOIC	S-3.119 S-3.119
Three-Wire and Current Source	XTR110	0.2 0.6	0.005 0.025	30 50	— —	— —	— —	4-20, 0-20, 5-25[4]	±16 ±64	±32 ±96	Ind Com	DIP DIP SOIC	3-139 3-139 3-139

NOTES: (1) With zero TC span resistor. (2) Com = 0°C to +70°C, Ind = –25°C to +85°C. (3) –40°C to +85°C. (4) Many more ranges with appropriate circuit. (5) Adjust error, including correction of sensor nonlinearity.

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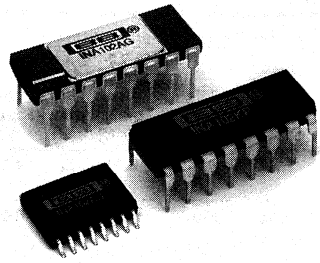


INA102

AVAILABLE IN DIE

Low Power INSTRUMENTATION AMPLIFIER

FEATURES

- LOW QUIESCENT CURRENT: 750μA max
- INTERNAL GAINS: 1, 10, 100, 1000
- LOW GAIN DRIFT: 5ppm/°C max
- HIGH CMR: 90dB min
- LOW OFFSET VOLTAGE DRIFT: 2μV/°C max
- LOW OFFSET VOLTAGE: 100μV max
- LOW NONLINEARITY: 0.01% max
- HIGH INPUT IMPEDANCE: $10^{10}\Omega$

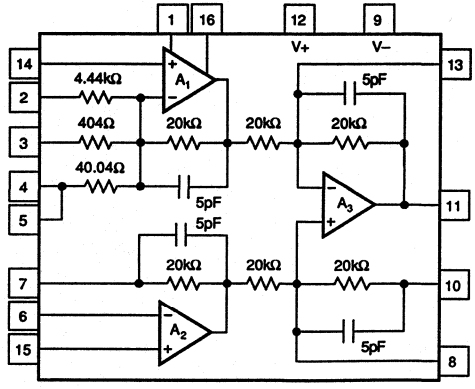
APPLICATIONS

- AMPLIFICATION OF SIGNALS FROM SOURCES SUCH AS:
  Strain Gages (Weigh Scale Applications)
  Thermocouples
  Bridge Transducers
- REMOTE TRANSDUCER AMPLIFIER
- LOW-LEVEL SIGNAL AMPLIFIER
- MEDICAL INSTRUMENTATION
- MULTICHANNEL SYSTEMS
- BATTERY POWERED EQUIPMENT

DESCRIPTION

The INA102 is a high-accuracy monolithic instrumentation amplifier designed for signal conditioning applications where low quiescent power is desired. On-chip thin-film resistors provide excellent temperature and stability performance. State-of-the-art laser-trimming technology insures high gain accuracy and common-mode rejection while avoiding expensive external components. These features make the INA102 ideally suited for battery-powered and high-volume applications.

The INA102 is also convenient to use. A gain of 1, 10, 100, or 1000 may be selected by simply strapping the appropriate pins together. A gain drift of 5ppm/°C in low gains can then be achieved without external adjustment. When higher-than-specified CMR is required, CMR can be trimmed using the pins provided. In addition, balanced filtering can be accomplished in the output stage.



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Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL

At T_A = +25°C with ±15VDC power supply and in circuit of Figure 2 unless otherwise noted.

PARAMETER	CONDITIONS	INA102AG MIN	INA102AG TYP	INA102AG MAX	INA102CG MIN	INA102CG TYP	INA102CG MAX	INA102KP/INA102AU MIN	INA102KP/INA102AU TYP	INA102KP/INA102AU MAX	UNITS
GAIN											
Range of Gain		1		1000	•		•	•		•	V/V
Gain Equation, External, ±20%			G = 1 + (40k/R_G)[1]			•			•		V/V
Error, DC: G = 1	T_A = +25°C			0.1			0.05			0.15	%
G = 10	T_A = +25°C			0.1			0.05			0.35	%
G = 100	T_A = +25°C			0.25			0.15			0.4	%
G = 1000	T_A = +25°C			0.75			0.5			0.9	%
G = 1	$T_A = T_{MIN}$ to T_{MAX}			0.16			0.08			0.21	%
G = 10	$T_A = T_{MIN}$ to T_{MAX}			0.19			0.11			0.44	%
G = 100	$T_A = T_{MIN}$ to T_{MAX}			0.37			0.21			0.52	%
G = 1000	$T_A = T_{MIN}$ to T_{MAX}			0.93			0.62			1.08	%
Gain Temp. Coefficient											
G = 1				10			5			•	ppm/°C
G = 10				15			10			•	ppm/°C
G = 100				20			15			•	ppm/°C
G = 1000				30			20			•	ppm/°C
Nonlinearity, DC											
G = 1	T_A = +25°C			0.03			0.01			•	% of FS
G = 10	T_A = +25°C			0.03			0.01			•	% of FS
G = 100	T_A = +25°C			0.05			0.02			•	% of FS
G = 1000	T_A = +25°C			0.1			0.05			•	% of FS
G = 1	$T_A = T_{MIN}$ to T_{MAX}			0.045			0.015			•	% of FS
G = 10	$T_A = T_{MIN}$ to T_{MAX}			0.045			0.015			•	% of FS
G = 100	$T_A = T_{MIN}$ to T_{MAX}			0.075			0.03			•	% of FS
G = 1000	$T_A = T_{MIN}$ to T_{MAX}			0.15			0.1			•	% of FS
RATED OUTPUT											
Voltage	R_L = 10kΩ	±(|V_{CC}| – 2.5)			•			•			V
Current		±1			•			•			mA
Short-Circuit Current[2]			2			•			•		mA
Output Impedance, G = 1000			0.1			•			•		Ω
INPUT											
OFFSET VOLTAGE											
Initial Offset[3]	T_A = +25°C		±300	±300/G		±100	±200/G			•	µV
INA102AU										±500	±300/G µV
vs Temperature			±5	±10/G		±2	±5/G			•	µV/°C
vs Supply			±40	±50/G		±10	±20/G			•	µV/V
vs Time			±(20 + 30/G)			•			•		µV/mo
BIAS CURRENT											
Initial Bias Current											
(Each Input)	$T_A = T_{MIN}$ to T_{MAX}		25	50		6	30		•	•	nA
vs Temperature			±0.1			•			•		nA/°C
vs Supply			±0.1			•			•		nA/V
Initial Offset Current	$T_A = T_{MIN}$ to T_{MAX}		±2.5	±15		±2.5	±10		•	•	nA
vs Temperature			±0.1			•			•		nA/°C
IMPEDANCE											
Differential			10^{10} || 2			•			•		Ω || pF
Common-Mode			10^{10} || 2			•			•		Ω || pF
VOLTAGE RANGE											
Range, Linear Response	$T_A = T_{MIN}$ to T_{MAX}	±(|V_{CC}| – 4.5)			•			•			V
CMR With 1kΩ Source Imbalance											
G = 1	DC to 60Hz	80	94		90	•		75	•		dB
G = 10	DC to 60Hz	80	100		90	•		•	•		dB
G = 10 to 1000	DC to 60Hz	80	100		90	•		•	•		dB
NOISE											
Input Voltage Noise											
f_B = 0.01Hz to 10Hz			1			•			•		µVp-p
Density, G = 1000: f_O = 10Hz			30			•			•		nV/√Hz
f_O = 100Hz			25			•			•		nV/√Hz
f_O = 1kHz			25			•			•		nV/√Hz
Input Current Noise											
f_B = 0.01Hz to 10Hz			25			•			•		pAp-p
Density: f_O = 10Hz			0.3			•			•		pA/√Hz
f_O = 100Hz			0.2			•			•		pA/√Hz
f_O = 1kHz			0.15			•			•		pA/√Hz

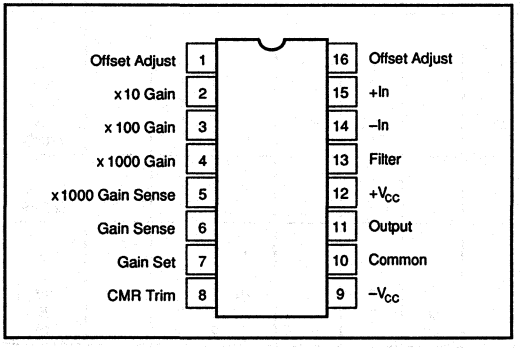
ELECTRICAL (CONT)

PARAMETER	CONDITIONS	INA102AG MIN	INA102AG TYP	INA102AG MAX	INA102CG MIN	INA102CG TYP	INA102CG MAX	INA102KP/INA102AU MIN	INA102KP/INA102AU TYP	INA102KP/INA102AU MAX	UNITS
DYNAMIC RESPONSE											
Small Signal ±3dB Flatness	V_{OUT} = 0.1Vrms										
G = 1			300			•			•		kHz
G = 10			30			•			•		kHz
G = 100			3			•			•		kHz
G = 1000			0.3			•			•		kHz
Small Signal, ±1% Flatness	V_{OUT} = 0.1Vrms										
G = 1			30			•			•		kHz
G = 10			3			•			•		kHz
G = 100			0.3			•			•		kHz
G = 1000			0.03			•			•		kHz
Full Power, G = 1 to 100	V_{OUT} = 10V, R_L = 10kΩ	1.7	2.5		•	•		•	•		kHz
Slew Rate, G = 1 to 100	V_{OUT} = 10V, R_L = 10kΩ	0.1	0.15		•	•		•	•		V/µs
Settling Time	R_L = 10kΩ, C_L = 100pF										
0.1%: G = 1	10V Step		50			•			•		µs
G = 100			360			•			•		µs
G = 1000			3300			•			•		µs
0.01%: G = 1	10V Step		60			•			•		µs
G = 100			500			•			•		µs
G = 1000			4500			•			•		µs
POWER SUPPLY											
Rated Voltage			±15			•			•		V
Voltage Range		±3.5		±18	•		•	•		•	V
Quiescent Current	V_O = 0V, $T_A = T_{MIN}$ to T_{MAX}		±500	±750		•	•		•	•	µA
TEMPERATURE RANGE											
Specification		–25		+85	•		•	0		+70	°C
INA102AU								**–25**		**+85**	°C
Operation	R_L > 50kΩ[2]	–25		+85	•		•	–25		+85	°C
Storage		–65		+150	•		•	–55		+125	°C

*Specification same as for INA102AG.

NOTES: (1) The internal gain set resistors have an absolute tolerance of ±20%; however, their tracking is 50ppm/°C. R_G will add to the gain error if gains other than 1, 10, 100 or 1000 are set externally. (2) At high temperature, output drive current is limited. An external buffer can be used if required. (3) Adjustable to zero.

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Supply ..... ±18V
Input Voltage Range ..... $\pm V_{CC}$
Operating Temperature Range ..... –25°C to +85°C
Storage Temperature Range: Ceramic ..... –65°C to +150°C
Plastic, SOIC ..... –55°C to +125°C
Lead Temperature (soldering, 10s) ..... +300°C
Output Short-Circuit Duration ..... Continuous to Ground

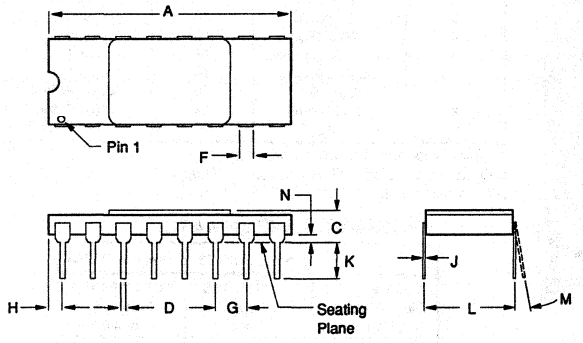
The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE
INA102AG	Ceramic DIP	–25°C to +85°C
INA102CG	Ceramic DIP	–25°C to +85°C
INA102KP	Plastic DIP	0°C to +70°C
INA102AU	Plastic SOIC	–25°C to +85°C

MECHANICAL

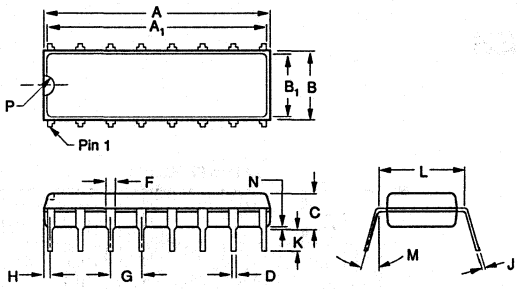
G Package — 16-Pin Ceramic DIP



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.790	.810	20.07	20.57
C	.105	.170	2.67	4.32
D	.015	.021	0.38	0.53
F	.048	.060	1.22	1.52
G	.100 BASIC		2.54 BASIC	
H	.030	.070	0.76	1.78
J	.008	.012	0.20	0.30
K	.120	.240	3.05	6.10
L	.300 BASIC		7.62 BASIC	
M	—	10°	—	10°
N	.025	.060	0.64	1.52

NOTE: Leads in true position within 0.010" (0.25mm) R at MMC at seating plane.

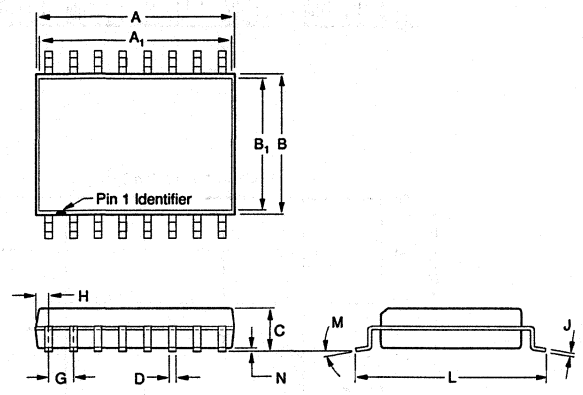
P Package — 16-Pin Plastic DIP



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.740	.800	18.80	20.32
A1	.725	.785	18.42	19.94
B	.230	.290	5.85	7.38
B1	.200	.250	5.09	6.36
C	.120	.200	3.05	5.09
D	.015	.023	0.38	0.59
F	.030	.070	0.76	1.78
G	.100 BASIC		2.54 BASIC	
H	0.20	.050	0.51	1.27
J	.008	.015	0.20	0.38
K	.070	.150	1.78	3.82
L	.300 BASIC		7.63 BASIC	
M	0°	15°	0°	15°
N	.010	.030	0.25	0.76
P	.025	.050	0.64	1.27

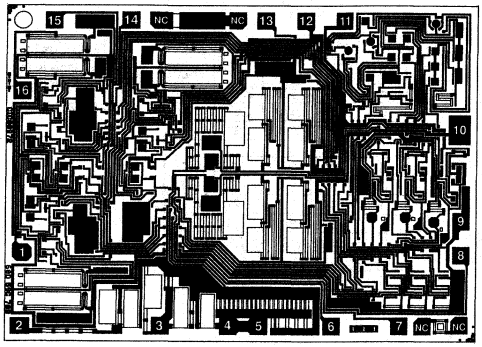
NOTE: Leads in true position within 0.010" (0.25mm) R at MMC at seating plane.

U Package — 16-Pin SOIC



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.400	.416	10.16	10.57
A1	.388	.412	9.86	10.46
B	.286	.302	7.26	7.67
B1	.268	.286	6.81	7.26
C	.093	.109	2.36	2.77
D	.015	.020	0.38	0.51
G	.0.50 BASIC		1.27 BASIC	
H	.022	.038	0.56	0.97
J	.008	.012	0.20	0.30
L	.391	.421	9.93	10.69
M	5° TYP		5° TYP	
N	.000	.012	0.00	0.30

NOTE: Leads in true position within 0.010" (0.25mm) R at MMC at seating plane.



INA102 DIE TOPOGRAPHY

PAD	FUNCTION	PAD	FUNCTION
1	Offset Adjust	10*	Common
2	X10 Gain	11	Output
3	X100 Gain	12	$+V_{CC}$
4	X1000 Gain	13	Filter
5	X1000 Gain Sense	14	–In
6	Gain Sense	15	+In
7	Gain Set	16	Offset Adjust
8	CMR Trim	17	(A_1 Output)
9	$-V_{CC}$	18	(A_2 Output)

* Glass covers upper one-third of this pad.
Substrate Bias: Electrically connected to –V supply.
NC: No Connection.

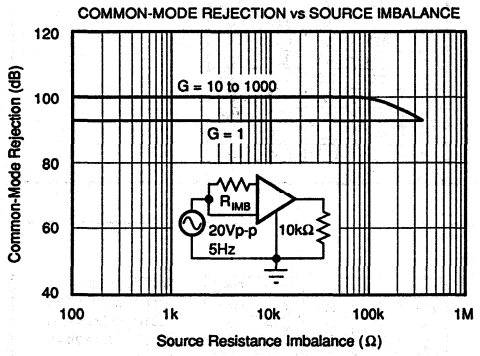
MECHANICAL INFORMATION

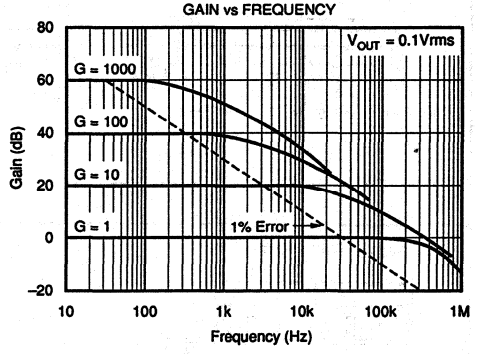
	MILS (0.001")	MILLIMETERS
Die Size	142 x 104 ±5	3.61 x 2.64 ±0.13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.10 x 0.10
Backing	Gold	

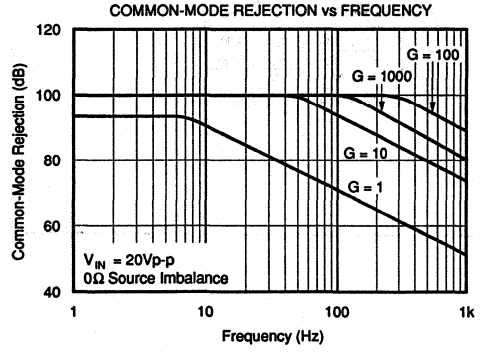
See "DICE PRODUCTS" Section 17 in Data Book Supplement Volume 33c, or contact Burr-Brown for current information.

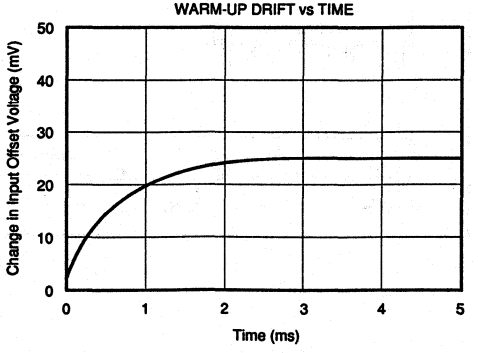
TYPICAL PERFORMANCE CURVES

At +25°C and in circuit of Figure 2 unless otherwise noted.



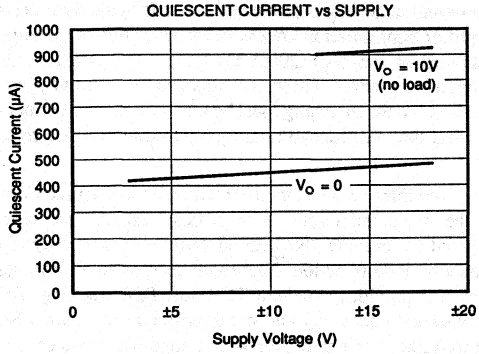


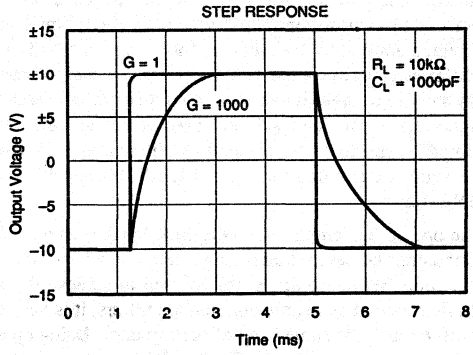


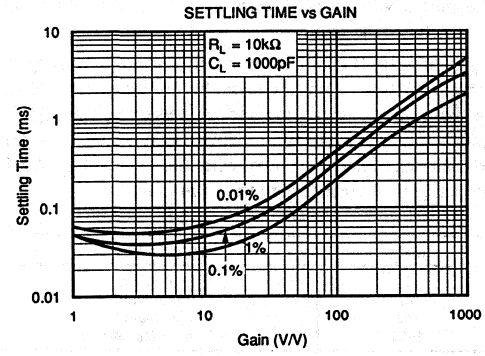


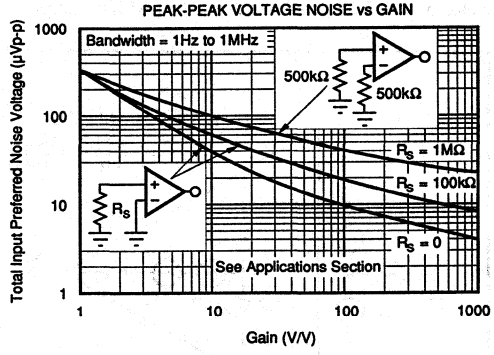
TYPICAL PERFORMANCE CURVES (CONT)

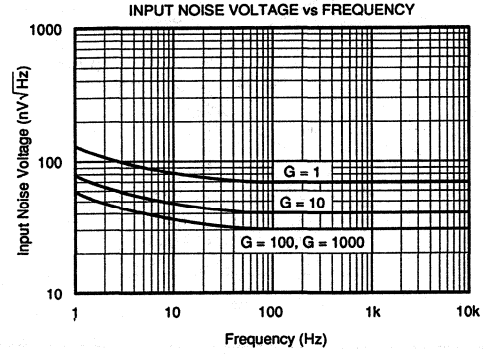
At +25°C and in circuit of Figure 2 unless otherwise noted.

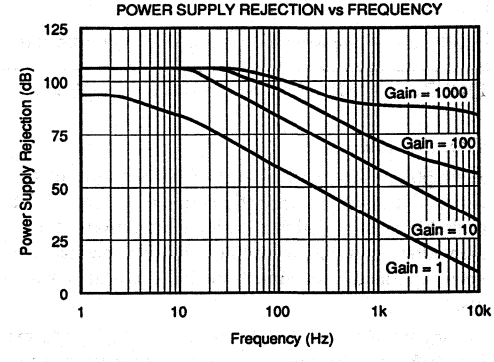












DISCUSSION OF PERFORMANCE

INSTRUMENTATION AMPLIFIERS

Instrumentation amplifiers are differential-input closed-loop gain blocks whose committed circuit accurately amplifies the voltage applied to their inputs. They respond mainly to the difference between the two input signals and exhibit extremely high input impedance, both differentially and common-mode. The feedback networks of this instrumentation amplifier are included on the monolithic chip. No external resistors are required for gains of 1, 10, 100, and 1000 in the INA102.

An operational amplifier, on the other hand, is an open-loop, uncommitted device that requires external networks to close the loop. While op amps can be used to achieve the same basic function as instrumentation amplifiers, it is very difficult to reach the same level of performance. Using op amps often leads to design tradeoffs when it is necessary to amplify low-level signals in the presence of common-mode voltages while maintaining high-input impedances. Figure 1 shows a simplified model of an instrumentation amplifier that eliminates most of the problems associated with op amps.

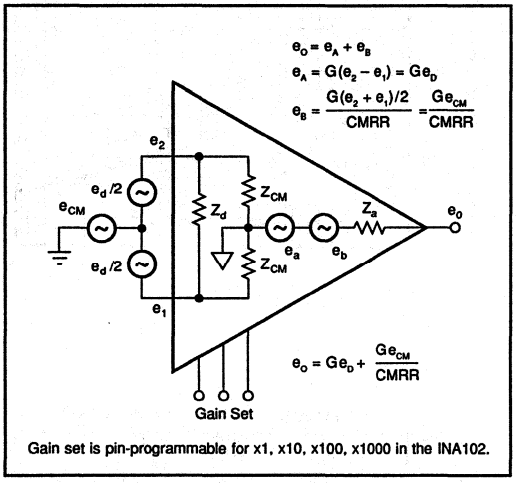


FIGURE 1. Model of an Instrumentation Amplifier.

THE INA102

A simplified schematic of the INA102 is shown on the first page. A three-amplifier configuration is used to provide the desirable characteristics of a premium performance instrumentation amplifier. In addition, INA102 has features not normally found in integrated circuit instrumentation amplifiers.

The input buffers (A_1 and A_2) incorporate high performance, low-drift amplifier circuitry. The amplifiers are connected in the noninverting configuration to provide the high input impedance ($10^{10}\Omega$) desirable in instrumentation amplifier applications. The offset voltage, and offset voltage versus temperature, are low due to the monolithic design, and improved even further by state-of-the-art laser-trimming techniques.

The output stage (A_3) is connected in a unity-gain differential amplifier configuration. A critical part of this stage is the matching of the four 20kΩ resistors which provide the difference function. These resistors must be initially well matched and the matching must be maintained over temperature and time in order to retain good common-mode rejection.

All of the internal resistors are made of thin-film nichrome on the integrated circuit. The critical resistors are laser-trimmed to provide the desired high gain accuracy and common-mode rejection. Nichrome ensures long-term stability and provides excellent TCR and TCR tracking. This provides gain accuracy and common-mode rejection when the INA102 is operated over wide temperature ranges.

USING THE INA102

Figure 2 shows the simplest configuration of the INA102. The output voltage is a function of the differential input voltage times the gain.

A gain of 1, 10, 100, or 1000 is selected by programming pins 2 through 7 (see Table I). Notice that for the gain of 1000, a special gain sense is provided to preserve accuracy. Although this is not always required, gain errors caused by external resistance in series with the low value 40.04Ω internal gain set resistor are thus eliminated.

GAIN	CONNECT PINS
1	6 to 7
10	2 to 6 and 7
100	3 to 6 and 7
1000	4 to 7 and separately 5 to 6

TABLE I. Pin-Programmable Gain Connections.

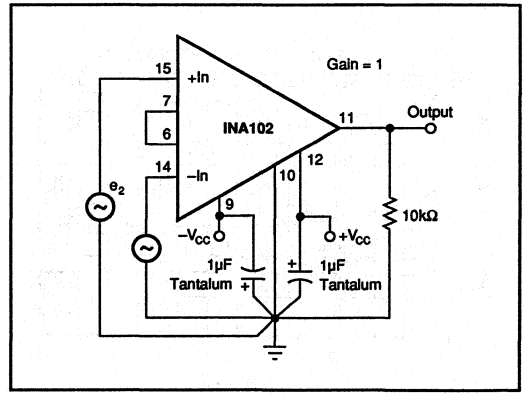


FIGURE 2. Basic Circuit Connection for the INA102.

Other gains between 1 and 10, 10 and 100, and 100 and 1000 can also be obtained by connecting an external resistor between pin 6 and either pin 2, 3, or 4, respectively (see Figure 6 for application).

$G = 1 + (40/R_G)$ where R_G is the total resistance between the two inverting inputs of the input op amps. At high gains, where the value of R_G becomes small, additional resistance (i.e., relays or sockets) in the R_G circuit will contribute to a gain error. Care should be taken to minimize this effect.

OPTIONAL OFFSET ADJUSTMENT PROCEDURE

It is sometimes desirable to null the input and/or output offset to achieve higher accuracy. The quality of the potentiometer will affect the results; therefore, choose one with good temperature and mechanical-resistance stability.

The optional offset null capabilities are shown in Figure 3. R_4 adjustment affects only the input stage component of the offset voltage. Note that the null condition will be disturbed when the gain is changed. Also, the input drift will be affected by approximately 0.31µV/°C per 100µV of input offset voltage that is trimmed. Therefore, care should be taken when considering use of the control for removal of other sources of offset. Output offset correction can be accomplished with A_1, R_1, R_2, and R_3, by applying a voltage to Common (pin 10) through a buffer amplifier. This buffer limits the resistance in series with pin 10 to minimize CMR error. Resistance above 0.1Ω will cause the common-mode rejection to fall below 100dB. Be certain to keep this resistance low.

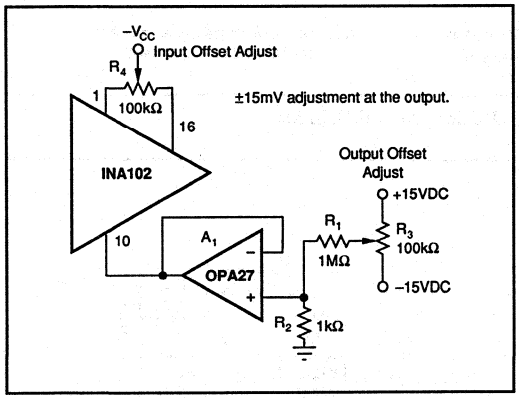


FIGURE 3. Optional Offset Nulling.

It is important to not exceed the input amplifiers' dynamic range. The amplified differential input signal and its associated common-mode voltage should not cause the output of A_1 or A_2 to exceed approximately ±12V with ±15V supplies, or nonlinear operation will result. To protect against moisture, especially in high gain, sealing compound may be used. Current injected into the offset pins should be minimized.

OPTIONAL FILTERING

The INA102 has provisions for accomplishing filtering with one external capacitor between pins 11 and 13. This single-pole filter can be used to reduce noise outside the signal bandwidth, but with some degradation to AC CMR.

When it is important to preserve CMR versus frequency (especially at 60Hz), two capacitors should be used. The additional capacitor is connected between pins 8 and 10. This will maintain a balance of impedances in the output stage. Either of these capacitors could also be trimmed slightly, to maximize CMR, if desired. Note that their ratio tracking will affect CMR over temperature.

OPTIONAL COMMON-MODE REJECTION TRIM

The INA102 is laser-adjusted during manufacturing to assure high CMR. However, if desired, a small resistance can be added in series with pin 10 to trim the CMR to an improved level. Depending upon the nature of the internal imbalances, either positive or negative resistance value could be required. The circuit shown in Figure 4 acts as a bipolar potentiometer and allows easy adjustment of CMR.

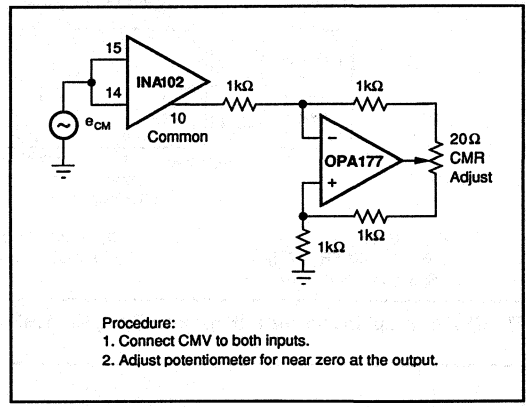


FIGURE 4. Optional Circuit for Externally Trimming CMR.

TYPICAL APPLICATIONS

Many applications of instrumentation amplifiers involve the amplification of low-level differential signals from bridges and transducers such as strain gages, thermocouples, and RTDs. Some of the important parameters include common-mode rejection (differential cancellation of common-mode offset and noise, see Figure 1), input impedance, offset voltage and drift, gain accuracy, linearity, and noise. The INA102 accomplishes all of these with high precision at surprisingly low quiescent current. However, in higher gains (>100), the bias current can cause a large offset error at the output. This can saturate the output unless the source impedance is separated, e.g., two 500kΩ paths instead of one 1MΩ unbalanced input. Figures 5 through 16 show some typical applications circuits.

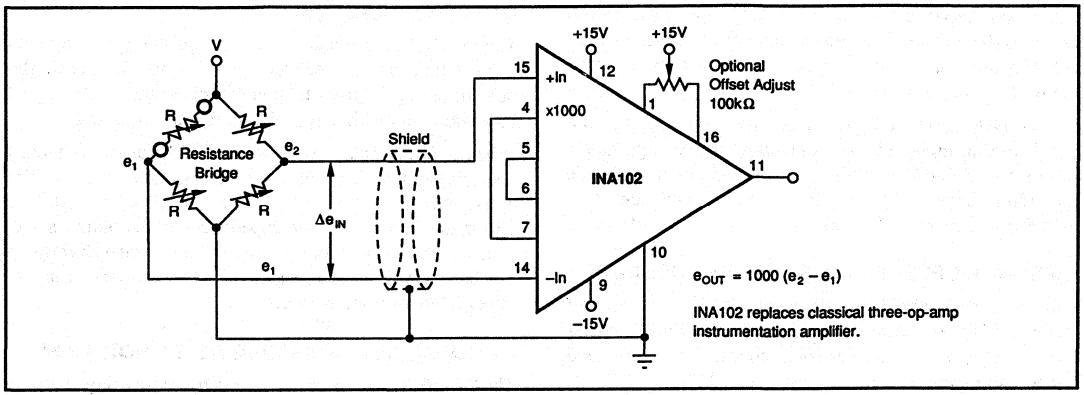


FIGURE 5. Amplification of a Differential Voltage from a Resistance Bridge.

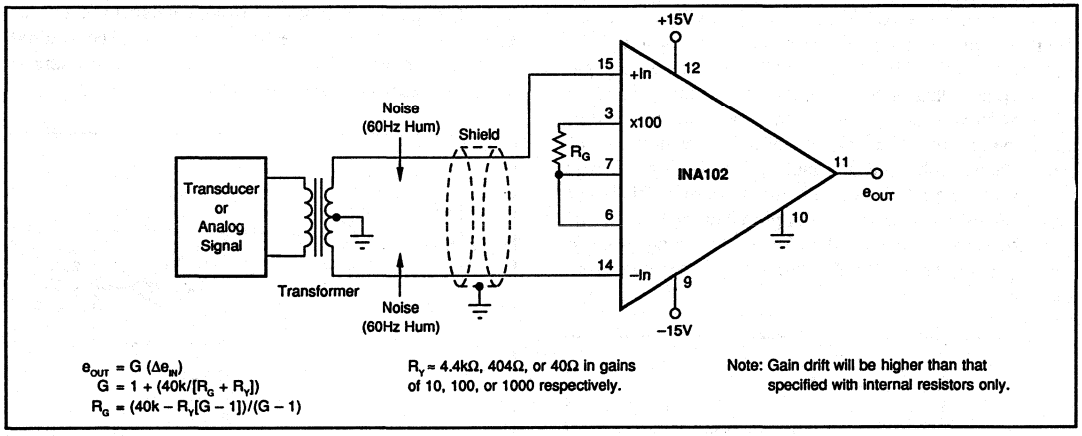


FIGURE 6. Amplification of a Transformer-Coupled Analog Signal Using External Gain Set.

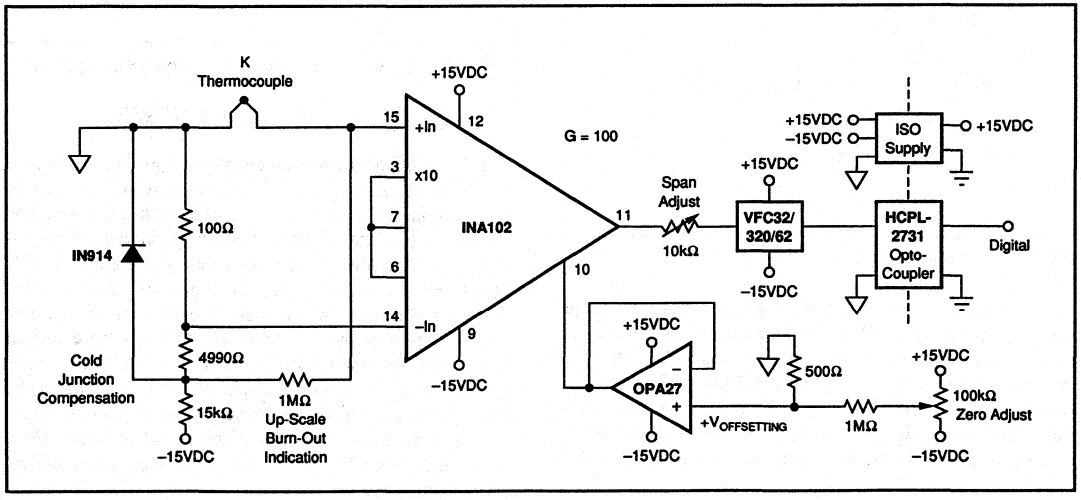


FIGURE 7. Isolated Thermocouple Amplifier with Cold Junction Compensation.

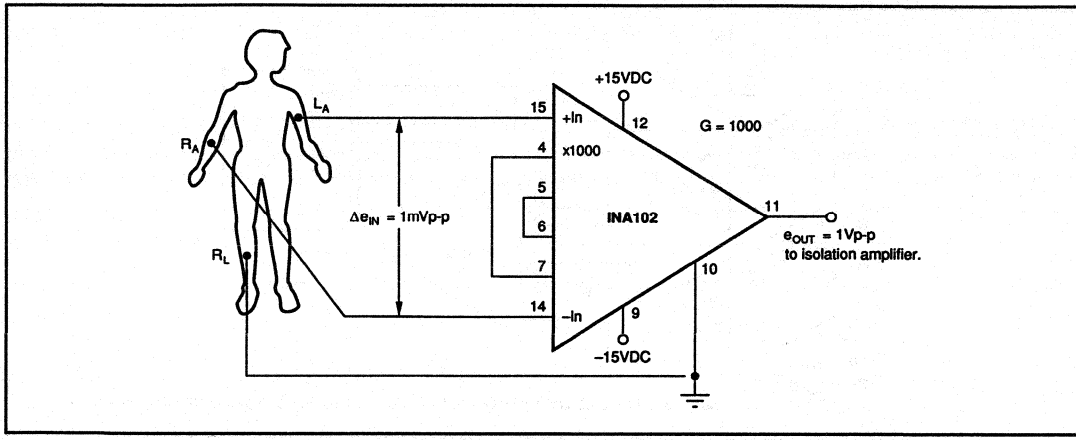


FIGURE 8. ECG Amplifier or Recorder Preamp for Biological Signals.

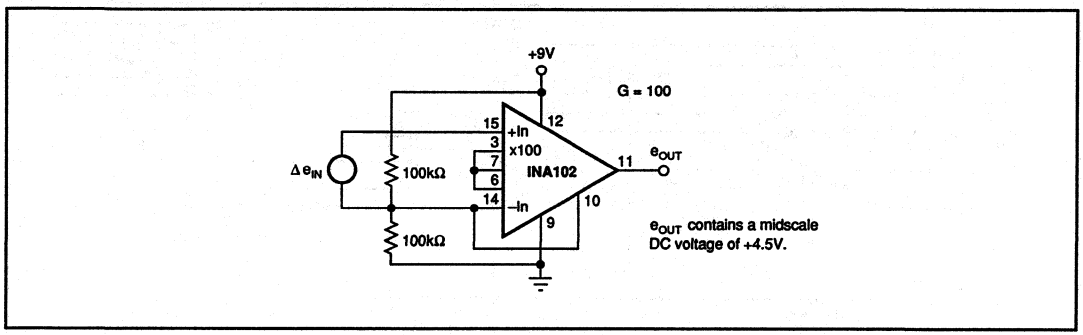


FIGURE 9. Single Supply Low Power Instrumentation Amplifier.

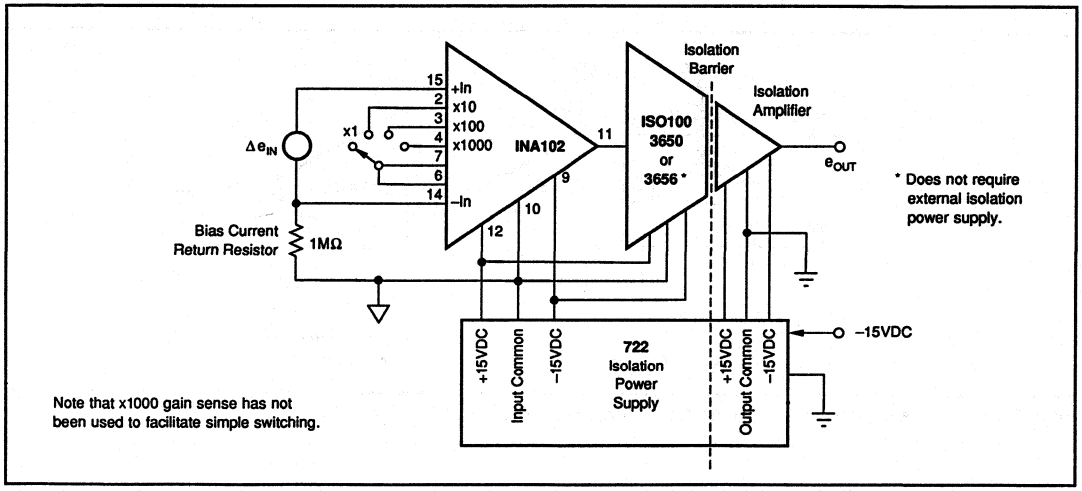


FIGURE 10. Precision Isolated Instrumentation Amplifier.

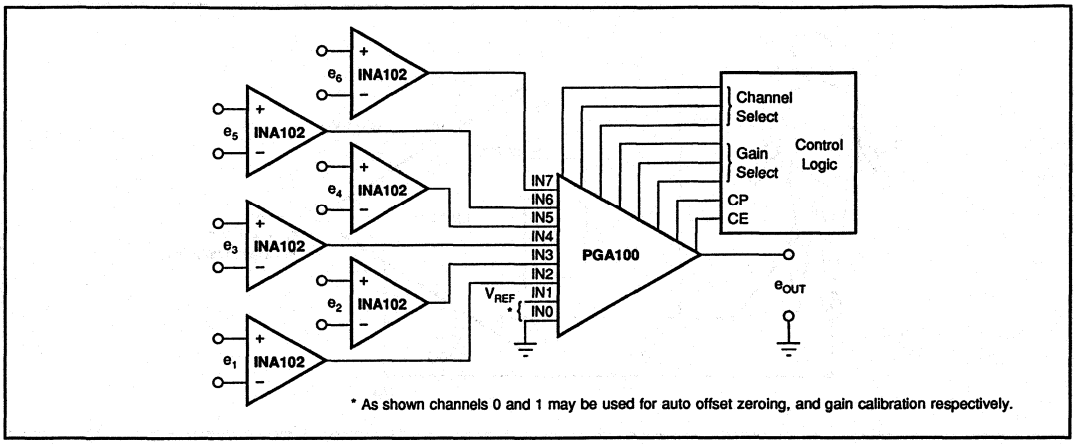


FIGURE 11. Multiple Channel Precision Instrumentation Amplifier with Programmable Gain.

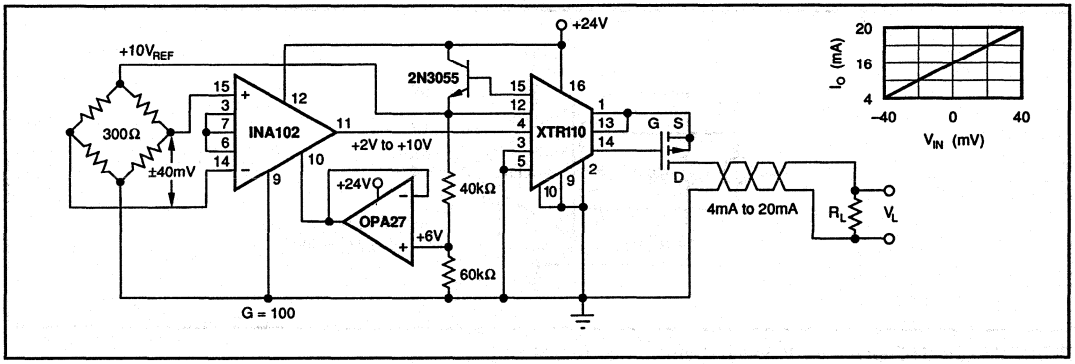


FIGURE 12. 4mA to 20mA Bridge Transmitter Using Single Supply Instrumentation Amplifier.

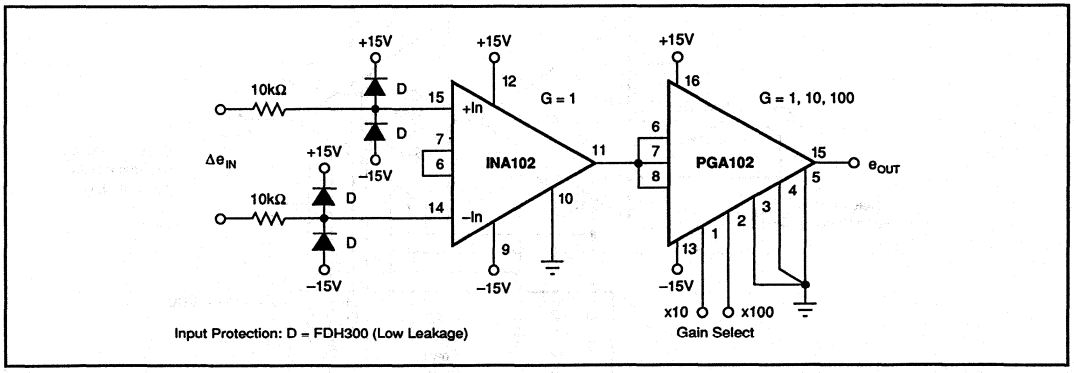


FIGURE 13. Programmable-Gain Instrumentation Amplifier Using the INA102 and PGA102.

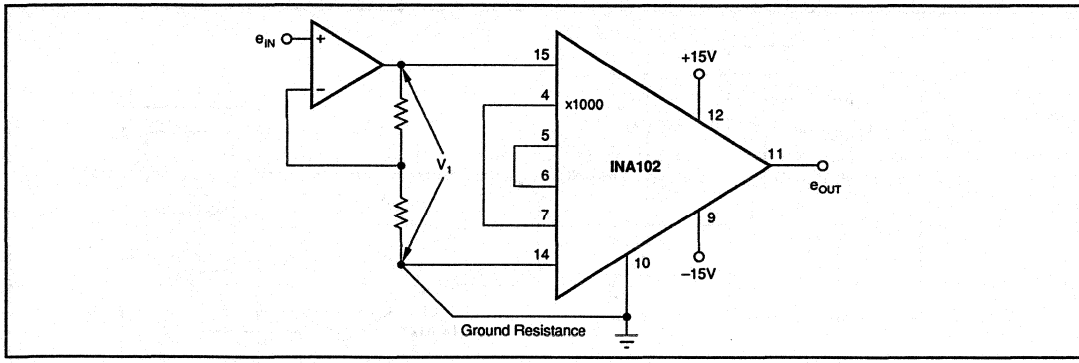


FIGURE 14. Ground Resistance Loop Eliminator (INA102 senses and amplifies V_1 accurately).

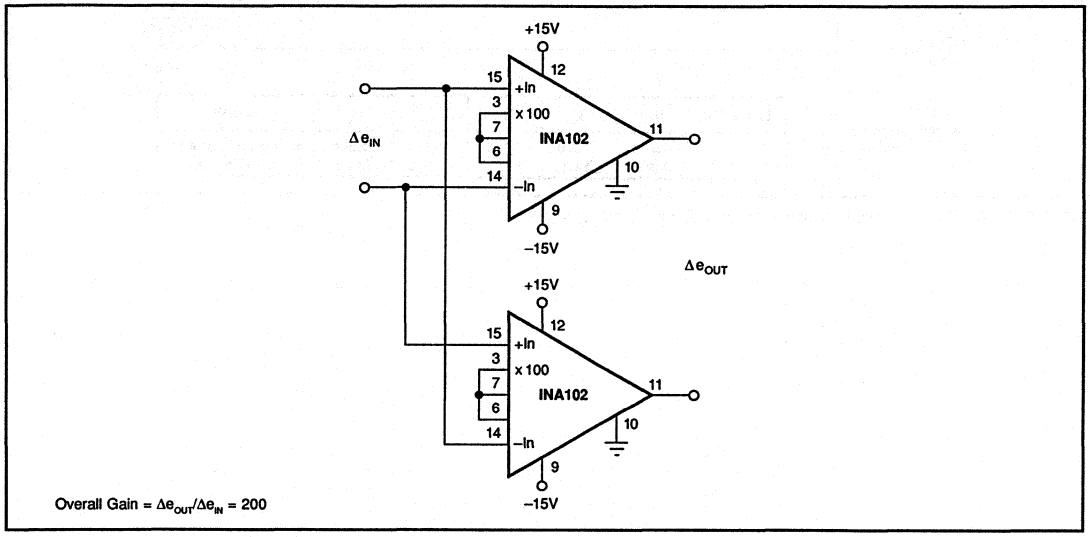
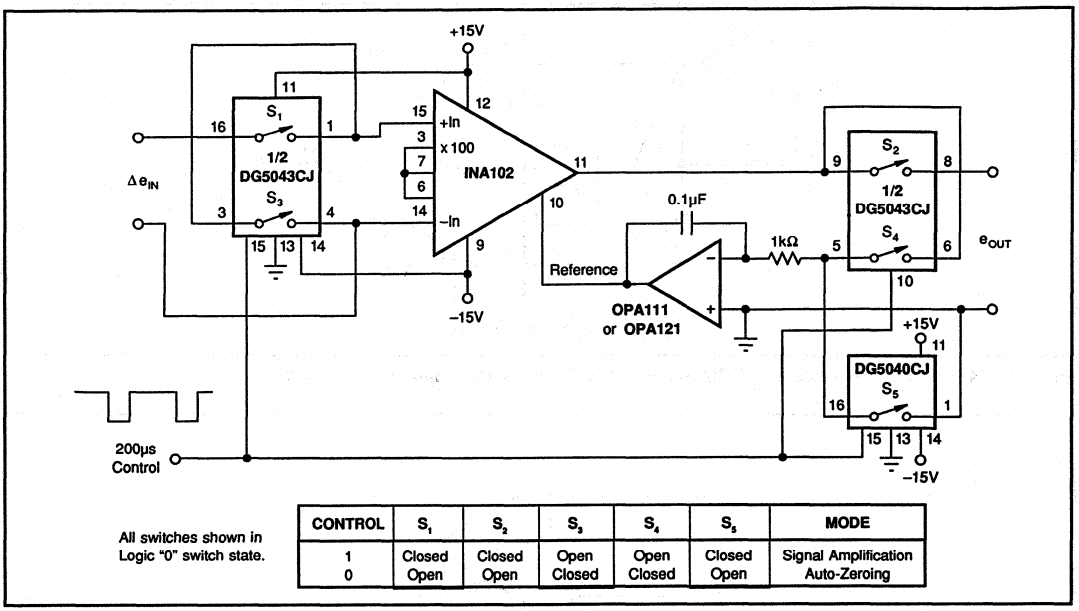


FIGURE 15. Differential Input/Differential Output Amplifier (twice the gain of one INA).

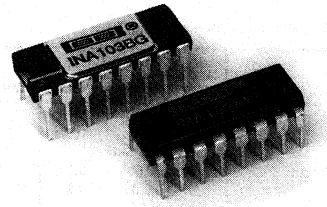


All switches shown in Logic "0" switch state.

CONTROL	S_1	S_2	S_3	S_4	S_5	MODE
1	Closed	Closed	Open	Open	Closed	Signal Amplification
0	Open	Open	Closed	Closed	Open	Auto-Zeroing

FIGURE 16. Auto-Zeroing Instrumentation Amplifier Circuit.

BURR-BROWN®



INA103

AVAILABLE IN DIE

Low Noise, Low Distortion INSTRUMENTATION AMPLIFIER

FEATURES

- LOW NOISE : 1nV/√Hz
- LOW THD : <0.002% typ 20Hz-20kHz, G = 1 to 100
- HIGH GBW: 100MHz at G = 1000
- WIDE SUPPLY RANGE: ±9V to ±25V
- HIGH CMRR: >110dB
- BUILT-IN GAIN SETTING RESISTORS: G = 1, 100
- UPGRADES AD625

APPLICATIONS

- HIGH QUALITY MICROPHONE PREAMPS (REPLACES TRANSFORMERS)
- MOVING-COIL PREAMPLIFIERS
- DIFFERENTIAL RECEIVERS
- AMPLIFICATION OF SIGNALS FROM SOURCES SUCH AS:
  Strain Gages (Weigh Scale Applications)
  Thermocouples
  Bridge Transducers

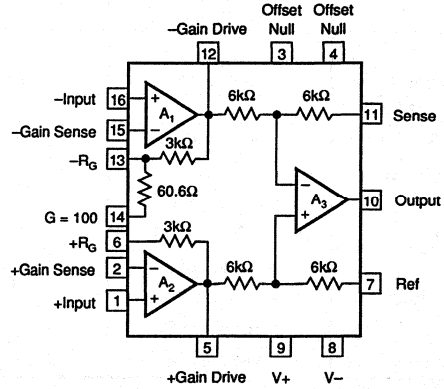
DESCRIPTION

The INA103 is an extremely low noise, low distortion monolithic instrumentation amplifier which is especially suitable for amplification of low level signals in audio systems. Input circuitry provides near-theoretical limit noise performance for 200Ω source impedances. A unique distortion-cancellation network in the input stage reduces THD to extremely low levels.

The INA103 is equally well-suited to preamplification and signal conditioning applications where low noise is required. In many cases, transformer coupling can be replaced by the INA103 to reduce cost and improve performance in signal conditioning systems.

The wide supply range (±9V to ±25V) of the INA103 increases its versatility. A copper lead frame in the plastic DIP package assures excellent thermal performance.

The INA103 pin configuration is compatible with the AD625. In many applications, the INA103 can replace the AD625 for improved performance. The INA103 is available in 16-pin DIP packages specified for the commercial (plastic DIP) and industrial (ceramic DIP) temperature ranges.



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Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL

All specifications at T_A = +25°C, V_S = ±15V and R_L = 2kΩ, unless otherwise noted.

PARAMETER	CONDITIONS	INA103AG			INA103BG			INA103KP			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
GAIN											
Range of Gain		1		1000	*		*	*		*	V/V
Gain Equation [1]			G = 1 + 6kΩ/R_G			*			*		V/V
Gain Error, DC G = 1	±10V Output		0.005	0.05		0.003	0.01		*	*	%
G = 100			0.05	0.25		0.04	0.1		0.07	*	%
Equation			0.5			0.1			*		%
Gain Temp. Co. G = 1	±10V Output		10			*			*		ppm/°C
G = 100			25			*			*		ppm/°C
Equation			25			*			*		ppm/°C
Nonlinearity, DC G = 1	±10V Output		0.0003	0.01		0.0002	0.002		*	*	% of FS[2]
G = 100			0.0006	0.01		0.0006	0.004		*	*	% of FS
OUTPUT											
Voltage, R_L = 600Ω	T_A = T_{MIN} to T_{MAX}	±11.5	±12		*	*		*	*		V
R_L = 600Ω	V_S = ±25, T_A = 25°C	±20	±21		*	*		*	*		V
Current	T_A = T_{MIN} to T_{MAX}	±40			*			*			mA
Short Circuit Current			±70			*			*		mA
Capacitive Load Stability			10			*			*		nF
INPUT											
OFFSET VOLTAGE											
Initial Offset RTI [3]			(20 + 700/G)	(100 + 5000/G)		(20 + 320/G)	(50 + 2000/G)		(30 + 1200/G)	*	µV
vs Temp G = 1 to 1000	T_A = T_{MIN} to T_{MAX}		1 + 20/G			0.75 + 10/G			1 + 20/G		µV/°C
G = 1000	T_A = T_{MIN} to T_{MAX}		1	2		0.75	1.25		*		µV/°C
vs Supply	±9V to ±25V		0.2 + 8/G	4 + 60/G		*	2 + 30/G		*	*	µV/V
BIAS CURRENT											
Initial Bias Current			2.5	12		*	8		*	*	µA
vs Temp	T_A = T_{MIN} to T_{MAX}		15			*	40 [4]		*		nA/°C
Initial Offset Current			0.04	1		0.03	0.5		*	*	µA
vs Temp	T_A = T_{MIN} to T_{MAX}		0.5			*	2.5 [4]		*		nA/°C
IMPEDANCE											
Differential Mode			60 || 2			*			*		MΩ || pF
Common-Mode			60 || 5			*			*		MΩ || pF
VOLTAGE RANGE											
Range, Linear Response	Common Mode [5]	±11	±12		*	*		*	*		V
CMR											
G = 1	DC to 60Hz	72	86		80	91		*	*		dB
G = 100	DC to 60Hz	100	125		110	129		*	*		dB
NOISE											
INPUT											
Voltage [6]	R_S = 0Ω										
	10Hz		2			*			*		nV/√Hz
	100Hz		1.2			*			*		nV/√Hz
	1kHz		1			*	1.4 [4]		*		nV/√Hz
Current	1kHz		2			*			*		pA/√Hz
OUTPUT											
Voltage	1kHz		65			*			*		nV/√Hz
A Weighted, 20Hz-20kHz	20Hz-20kHz		–100			*			*		dBu
DYNAMIC RESPONSE											
–3dB Bandwidth: G = 1	Small Signal		6			*			*		MHz
G = 100	Small Signal		800			*			*		kHz
Full Power Bandwidth	G = 1										
	V_{OUT} = ±10V, R_L = 600Ω		240			*			*		kHz
Slew Rate	G = 1 to 500		15			*			*		V/µs
THD + Noise	G = 100, f = 1kHz		0.0009			*			*		%
Settling Time 0.1%											
G = 1	V_O = 20V Step		1.7			*			*		µs
G = 100			1.5			*			*		µs
Settling Time 0.01%											
G = 1	V_O = 20V Step		2			*			*		µs
G = 100			3.5			*			*		µs
Overload Recovery [7]	50% Overdrive		1			*			*		µs

*Same specification as INA103AG.

NOTES: (1) Gains other than 1 and 100 can be set by adding an external resistor, R_G between pins 2 and 15. Gain accuracy is a function of R_G. (2) FS = Full Scale. (3) Adjustable to zero. (4) Guaranteed but not tested. (5) V_O = 0V, see Typical Curves for V_{CM} vs V_O. (6) $V_{NOISE\ RTI} = \sqrt{V^2_{N\ INPUT} + (V_{N\ OUTPUT}/Gain)^2 + 4KTR_G}$. See Typical Curves. (7) Time required for output to return from saturation to linear operation following the removal of an input overdrive voltage.

SPECIFICATIONS (CONT)

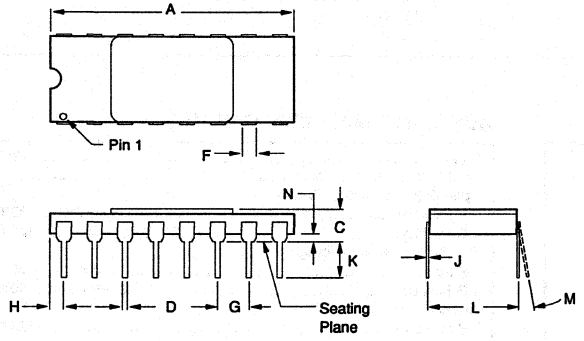
ELECTRICAL

All specifications at T_A = +25°C, V_S = ±15V and R_L = 2kΩ, unless otherwise noted.

PARAMETER	CONDITIONS	INA103AG			INA103BG			INA103KP			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
POWER SUPPLY											
Rated Voltage			±15			•			•		V
Voltage Range		±9		±25	•		•	•		•	V
Quiescent Current			9	12.5		•	•		•	•	mA
TEMPERATURE RANGE											
Specification		–25		+85	•		•	0		+70	°C
Operation		–55		+125	•		•	–40		+85	°C
Storage		–65		+150	•		•	–40		+100	°C
Thermal Resistance, θ_{JA}			100			•			•		°C/W

MECHANICAL

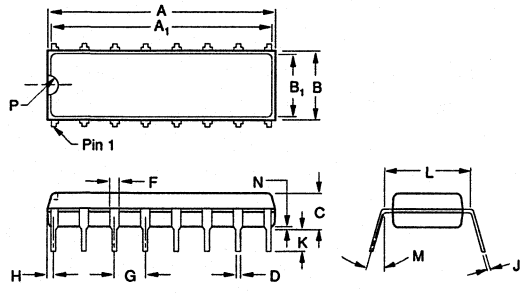
G Package — 16-Pin Hermetic DIP



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.790	.810	20.07	20.57
C	.105	.170	2.67	4.32
D	.015	.021	0.38	0.53
F	.048	.060	1.22	1.52
G	.100 BASIC		2.54 BASIC	
H	.030	.070	0.76	1.78
J	.008	.012	0.20	0.30
K	.120	.240	3.05	6.10
L	.300 BASIC		7.62 BASIC	
M	—	10°	—	10°
N	.025	.060	0.64	1.52

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

P Package — 16-Pin Plastic DIP



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.740	.800	18.80	20.32
A1	.725	.785	18.42	19.94
B	.230	.290	5.85	7.38
B1	.200	.250	5.09	6.36
C	.120	.200	3.05	5.09
D	.015	.023	0.38	0.59
F	.030	.070	0.76	1.78
G	.100 BASIC		2.54 BASIC	
H	0.20	.050	0.51	1.27
J	.008	.015	0.20	0.38
K	.070	.150	1.78	3.82
L	.300 BASIC		7.63 BASIC	
M	0°	15°	0°	15°
N	.010	.030	0.25	0.76
P	.025	.050	0.64	1.27

NOTE: Leads in true position within 0.010" (0.25mm) R at MMC at seating plane.

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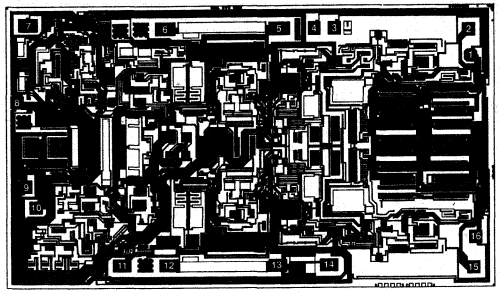
DICE INFORMATION



INA103 DIE TOPOGRAPHY

PAD	FUNCTION	PAD	FUNCTION
1	+Input	9	V+
2	+Gain Sense	10	Output
3	+Offset Null	11	Sense
4	–Offset Null	12	–Gain Drive
5	+Gain Drive	13	$-R_G$
6	$+R_G$	14	G = 100
7	Ref	15	– Gain Sense
8	V–	16	–Input

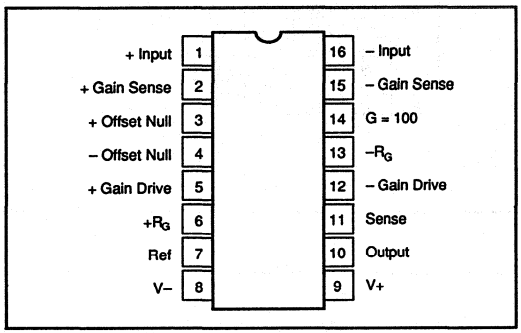
Substrate Bias: Electrically connected to V– supply.

MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	194 x 115 ±5	4.93 x 2.92 ±0.13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.1 x 0.1
Backing: Chrominum-Silver		

See "DICE PRODUCTS" Section 17 in Data Book Supplement Volume 33c, or contact Burr-Brown for current information.

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

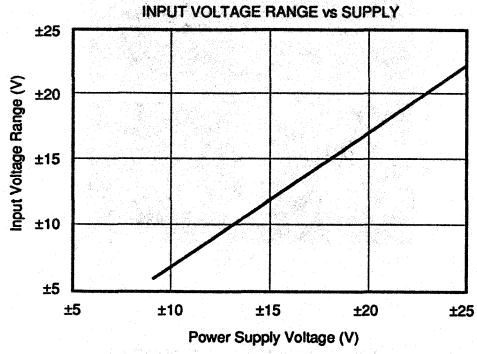
Supply ..... ±25V
Input Voltage Range, Continuous ..... $\pm V_s$
Operating Temperature Range:
P Package ..... –40°C to +85°C
G Package ..... –55°C to +125°C
Storage Temperature Range:
P Package ..... –40°C to +100°C
G Package ..... –65°C to +150°C
Junction Temperature:
P Package ..... +125°C
G Package ..... +150°C
Lead Temperature (soldering, 10s) ..... +300°C
Output Short Circuit to Common ..... Continuous

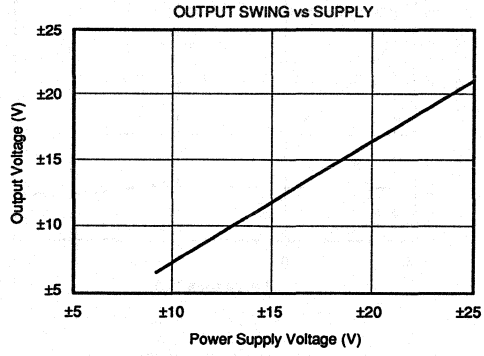
ORDERING INFORMATION

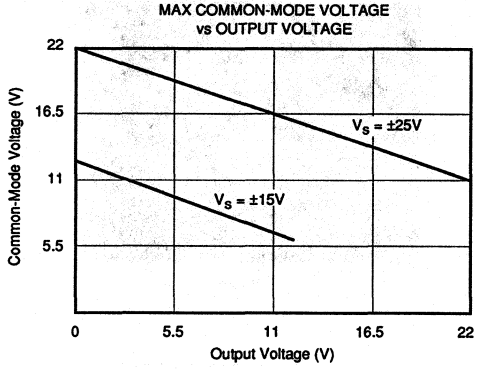
MODEL	PACKAGE	TEMP RANGE
INA103AG	Ceramic DIP	–25°C to +85°C
INA103BG	Ceramic DIP	–25°C to +85°C
INA103KP	Plastic DIP	0°C to +70°C

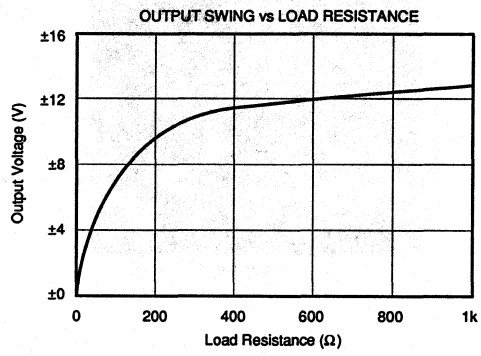
TYPICAL PERFORMANCE CURVES

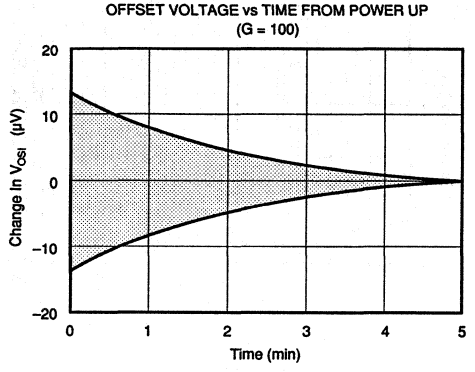
At T_A = +25°C, V_S = ±15V unless otherwise noted.

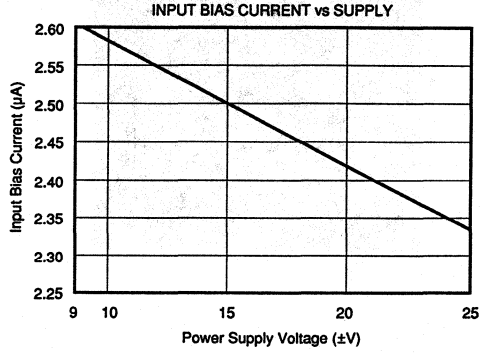








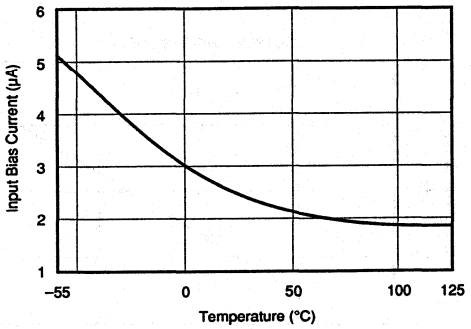




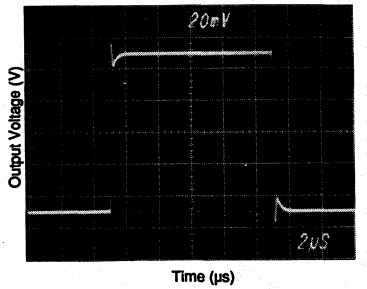
TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C, V_S = ±15V unless otherwise noted.

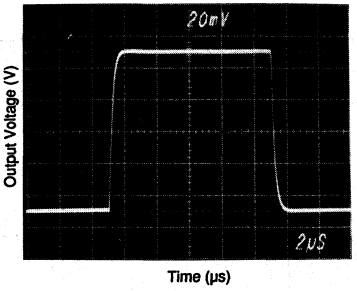
INPUT BIAS CURRENT vs TEMPERATURE



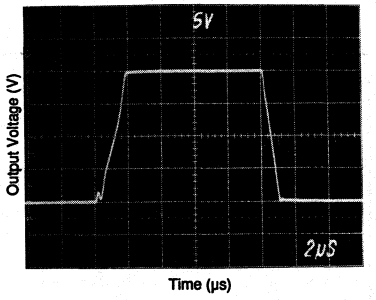
SMALL SIGNAL TRANSIENT RESPONSE
(G = 1)



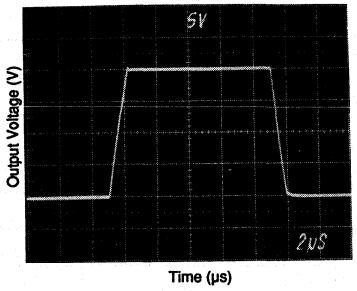
SMALL SIGNAL TRANSIENT RESPONSE
(G = 100)



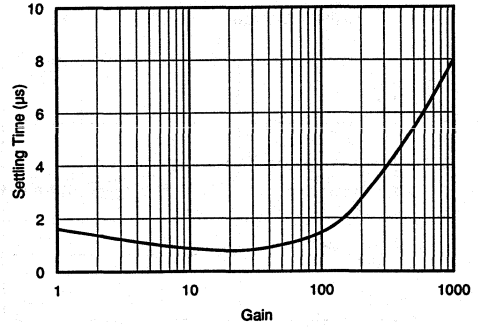
LARGE SIGNAL TRANSIENT RESPONSE
(G = 1)



LARGE SIGNAL TRANSIENT RESPONSE
(G = 100)



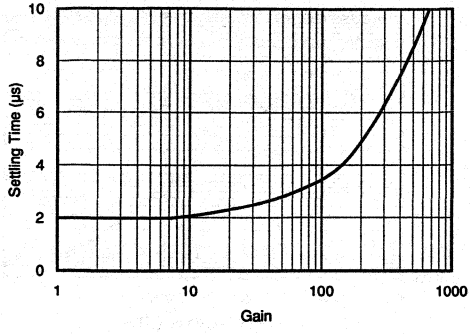
SETTLING TIME vs GAIN
(0.1%, 20V STEP)



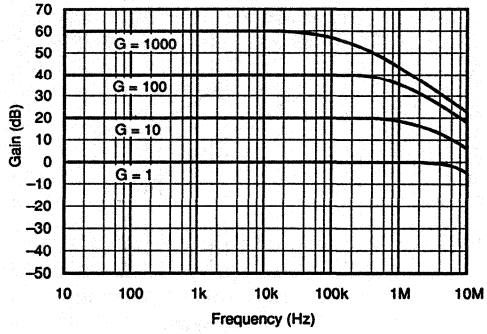
TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C, V_S = ±15V unless otherwise noted.

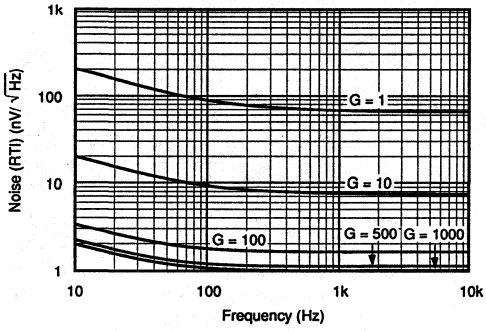
SETTLING TIME vs GAIN
(0.01%, 20V STEP)



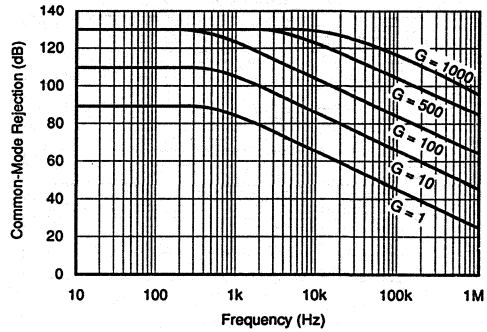
SMALL-SIGNAL FREQUENCY RESPONSE



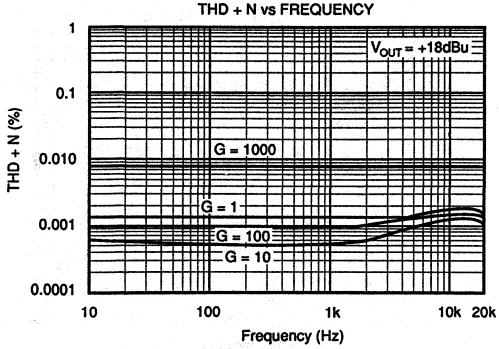
NOISE (RTI) vs FREQUENCY



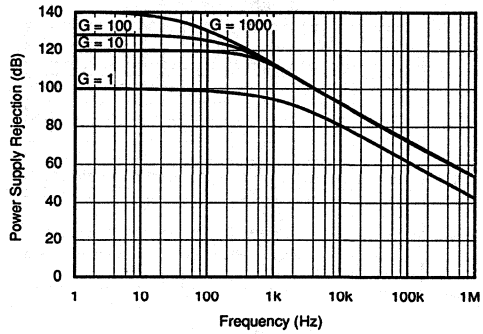
CMR vs FREQUENCY



THD + N vs FREQUENCY



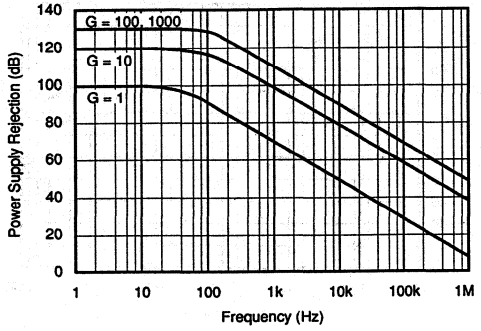
V+ POWER SUPPLY REJECTION
vs FREQUENCY



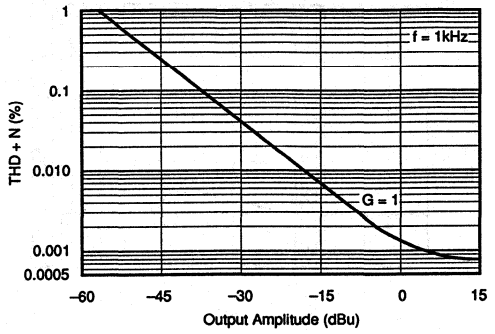
TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C, V_S = ±15V unless otherwise noted.

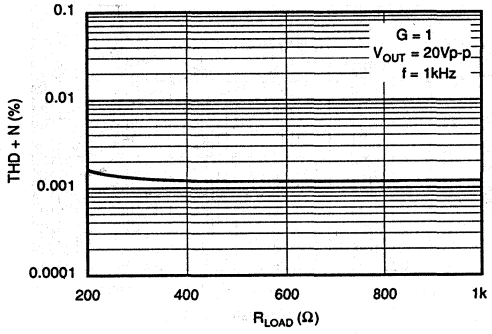
V– POWER SUPPLY REJECTION vs FREQUENCY



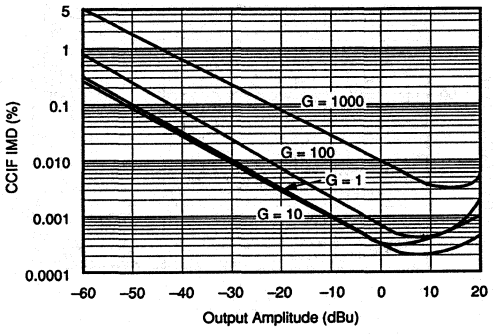
THD + N vs LEVEL



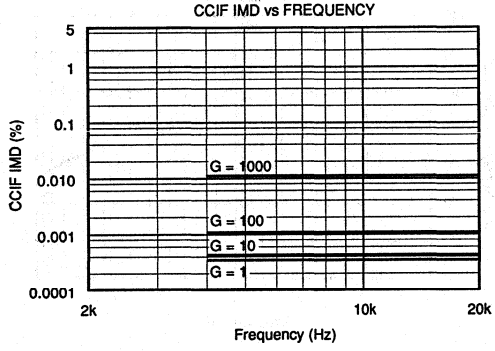
THD + N vs LOAD



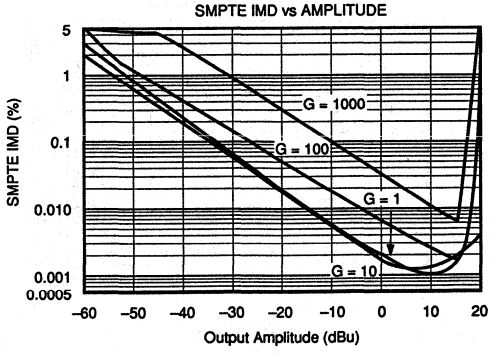
CCIF IMD vs AMPLITUDE



CCIF IMD vs FREQUENCY

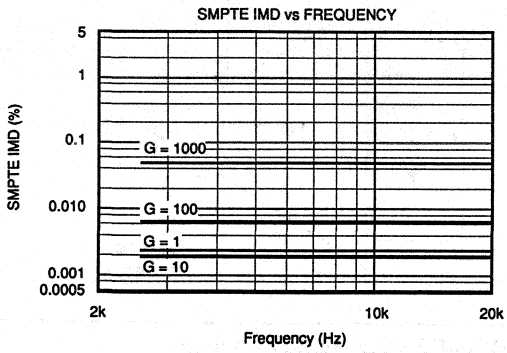


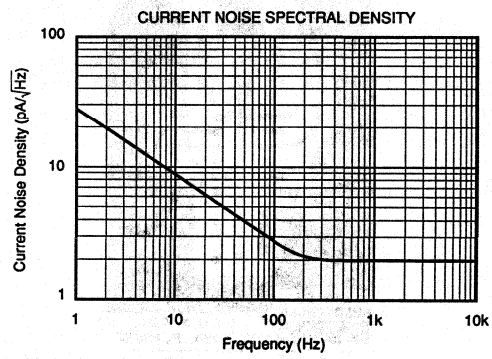
SMPTE IMD vs AMPLITUDE



TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C, V_S = ±15V unless otherwise noted.





DISCUSSION OF PERFORMANCE

A simplified diagram of the INA103 is shown on the first page. The design uses a current feedback architecture which can be thought of as a classical three-op-amp instrumentation amplifier. The input stage (A_1 and A_2) incorporates wide-bandwidth, low noise, low drift amplifier circuitry. The unity-gain difference amp removes the common-mode signal from this input stage output signal, giving a single-ended output referred to the potential at the reference pin.

The Gain vs Frequency performance (shown in the Typical Performance Curves) illustrates the advantage of the circuit topology used in the INA103: bandwidth remains nearly constant over gain ranges from 1 to 100. This yields a gain-bandwidth product (GBW) of >100MHz at G = 1000. Gain-related errors are greatly reduced due to this high GBW. A distortion cancellation input stage and improved output stage reduce THD + N to less than 0.002% from 20Hz to 20kHz. The output can drive 200Ω loads with no crossover distortion (at 1kHz).

These performance advantages make the INA103 ideal for instrumentation amplifier applications which require low noise, excellent dynamic and spectral response, and wide bandwidth.

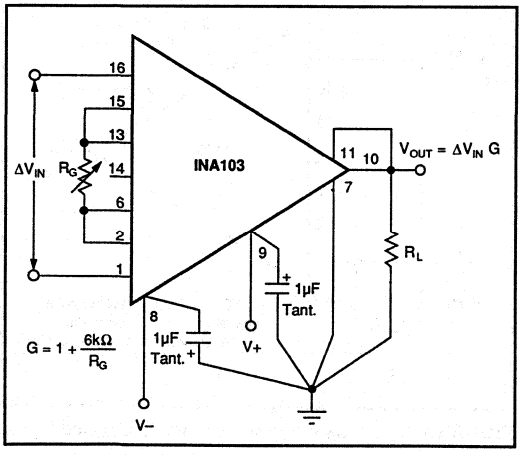


FIGURE 1. Basic Circuit Configuration.

BASIC POWER SUPPLY AND SIGNAL CONNECTIONS

Figure 1 shows the proper connections for power supply and signal. Supplies should be decoupled with 1µF tantalum capacitors as close to the amplifier as possible. To avoid gain and CMR errors introduced by the external circuit, connect grounds as indicated, being sure to minimize ground resistance. Resistance in series with the reference (pin 7) or the sense (pin 11) will degrade CMR. Also, to maintain stability, avoid capacitance from the output to the gain set, offset adjust, and input pins. A suggested PC board layout is shown in Figure 2.

OFFSET ADJUSTMENT

As with all instrumentation amplifiers, voltage offsets occur in both the input and output stages of the INA103. Input-referred voltage offsets are multiplied by the overall gain of the IA. Output-referred offsets are multiplied by the gain of the output stage (usually gain = 1). Input and output voltage offsets are actively laser-trimmed to near zero at the factory. Applications which require user voltage offset adjustment can employ one of the methods discussed below.

Output voltage offset can be adjusted using the null pins on the INA103, as shown in Figure 3. Although the null pins primarily adjust the output offset, they also have a small

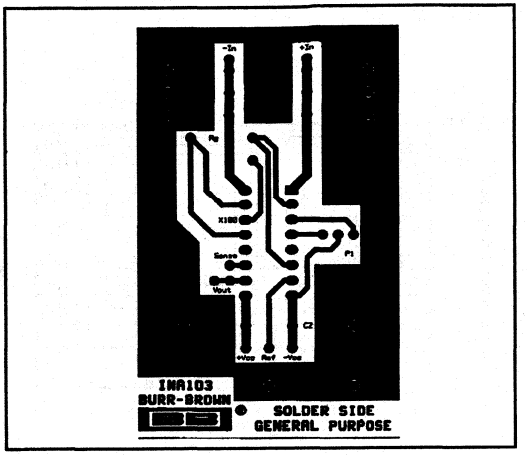


FIGURE 2. Suggested PC Board Layout for INA103. (Not Available from Burr-Brown).

effect on the input offset. For 1mV of output offset change, the input offset will change approximately 1µV. Also, offset adjustment using the null pins will change the offset voltage drift of the INA103. For 1mV of offset change, the output offset drift changes by 3µV/°C. The change in input offset drift is negligible.

For output voltage offset adjustment with no effect on voltage offset drift or input voltage offset, use the circuit shown in Figure 4.

The INA103 has no trim pins for input offset adjustment. However, in AC coupled applications, input offset adjustment can be accomplished using the circuit shown in Figure 5.

The circuit shown in Figure 6 will provide automatic DC restoration for the Figure 5 circuit. The low frequency roll-off of this circuit is a function of the IA gain.

$$f_{-3dB} = \text{gain}/(12 \bullet \pi \bullet R \bullet C).$$

The circuit shown in Figure 7 can also be used for V_{OS} adjustment in floating source applications as long as the source impedance is greater than 10Ω. If the source impedance is less than 10Ω, the offset range may not be adequate to trim out the maximum input-referred V_{OS} of the INA103.

GAIN SELECTION

Gain selection is accomplished by strapping together the appropriate pins on the INA103. Table I shows possible gains from the internal resistors. To use the internal feedback resistors, connect pin 13 to pin 15, and pin 2 to pin 6. Keep the connections as short as possible to maintain accuracy.

GAIN	CONNECT PIN 14 TO	GAIN ACCURACY (%)
1	None	0.01
100	Pin 2	0.1

TABLE I. Internal Gain Connections.

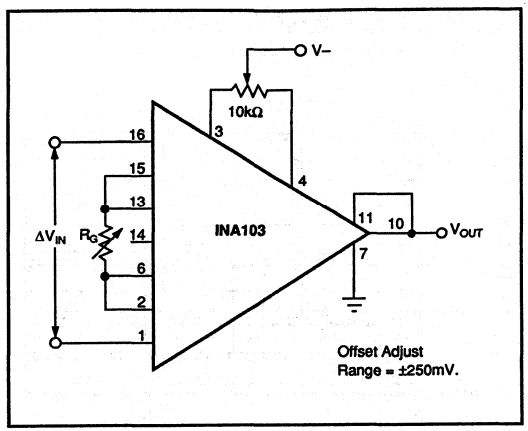


FIGURE 3. Offset Adjustment Circuit.

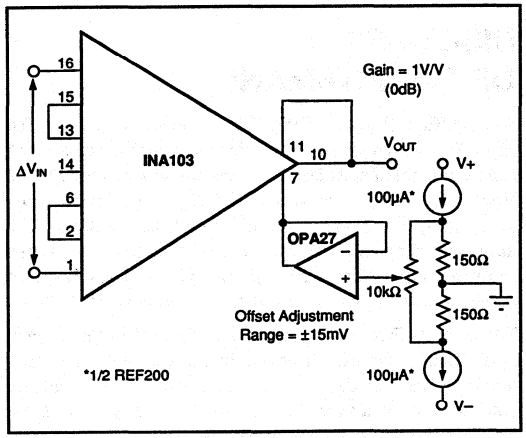


FIGURE 4. Output Offsetting.

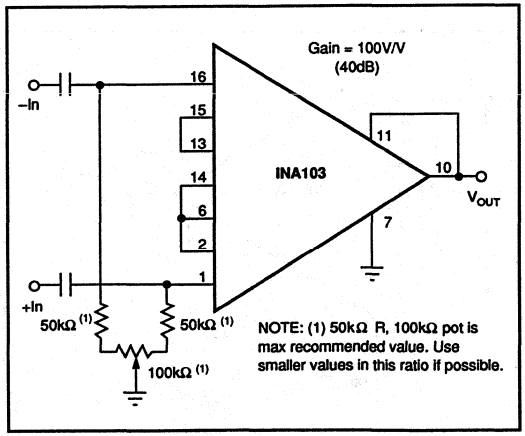


FIGURE 5. Input Offset Adjustment for AC-Coupled Inputs.

Gains other than 1 and 100 can be set by adding an external resistor, R_G, as shown in Figure 8. Gain accuracy is a function of resistor matching. For internal gains, accuracy is as shown in Table I. For external R_G, accuracy is a function of the external resistor accuracy, internal feedback resistor accuracy (typically 0.1%) and interconnection resistance (typically 0.1Ω). The equation for choosing R_G is shown below:

$$R_G = \frac{6k\Omega}{G-1}$$

where G is the gain value in V/V.

COMMON-MODE INPUT RANGE

For low distortion, the differential input signal and its common-mode voltage must not cause the input amplifiers' outputs to exceed their linear output range (See Max Common-Mode Voltage vs Output Voltage curve). This can be avoided by reducing the input stage gain and increasing the output stage gain as shown in Figure 9. This is also useful for increasing total gain.

Unlike some instrumentation amplifiers, the INA103 will limit cleanly under overload conditions. See Figure 10.

OPTIONAL COMMON-MODE REJECTION TRIM

The INA103 is laser-adjusted during manufacturing to assure high CMR. However, if desired, the circuit shown in Figure 11 may be used to trim the CMR. Note that an approximate +0.2% gain error is induced.

OUTPUT SENSE

An output-sense terminal allows greater accuracy in connecting the load. By attaching this feedback point at the load, IR drops due to load currents are eliminated since they are inside the feedback loop. Proper connection is shown in Figure 1. When more output current is needed, a power booster can be placed within the feedback loop as shown in Figure 12. Buffer errors are reduced by the loop gain of the output amplifier.

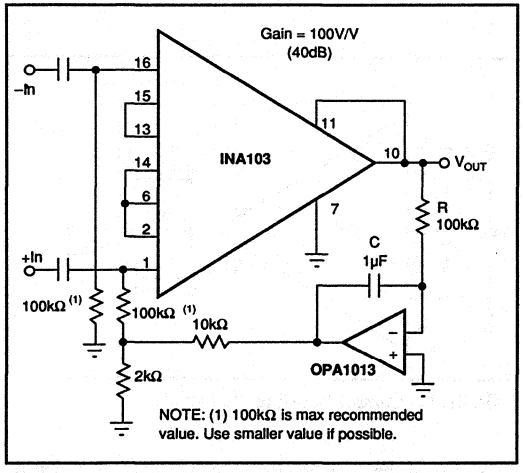


FIGURE 6. Automatic DC Restoration.

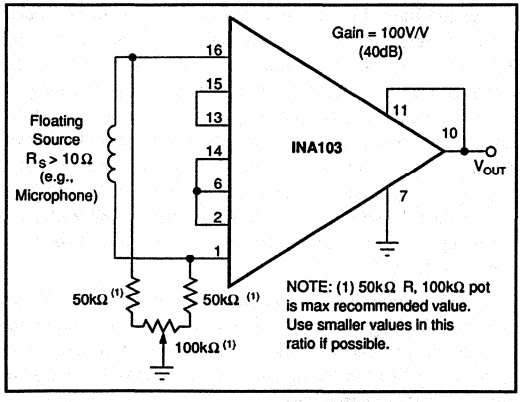
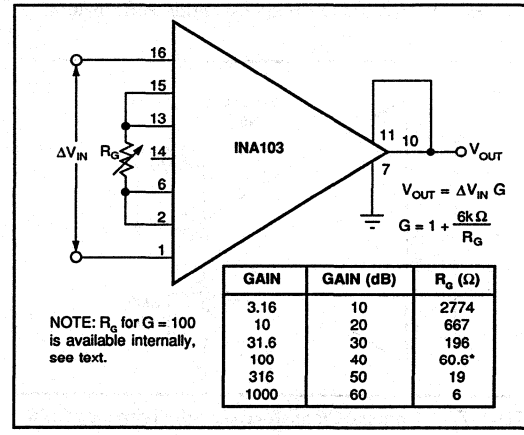
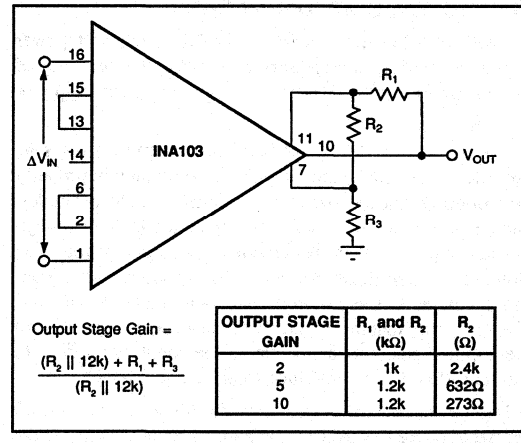


FIGURE 7. Input Offset Adjustment for Floating Source.



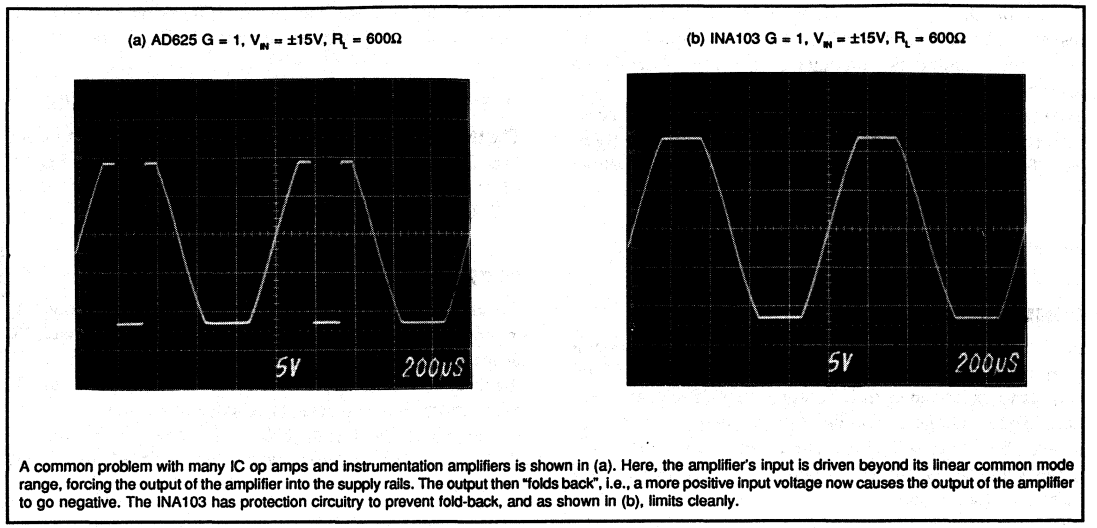
GAIN	GAIN (dB)	R_G (Ω)
3.16	10	2774
10	20	667
31.6	30	196
100	40	60.6*
316	50	19
1000	60	6

FIGURE 8. Gain Setting Using External Resistor.



OUTPUT STAGE GAIN	R_1 and R_2 (kΩ)	R_2 (Ω)
2	1k	2.4k
5	1.2k	632Ω
10	1.2k	273Ω

FIGURE 9. Gain Adjustment of Output Stage.



A common problem with many IC op amps and instrumentation amplifiers is shown in (a). Here, the amplifier's input is driven beyond its linear common mode range, forcing the output of the amplifier into the supply rails. The output then "folds back", i.e., a more positive input voltage now causes the output of the amplifier to go negative. The INA103 has protection circuitry to prevent fold-back, and as shown in (b), limits cleanly.

FIGURE 10. INA103 Overload Condition Performance.

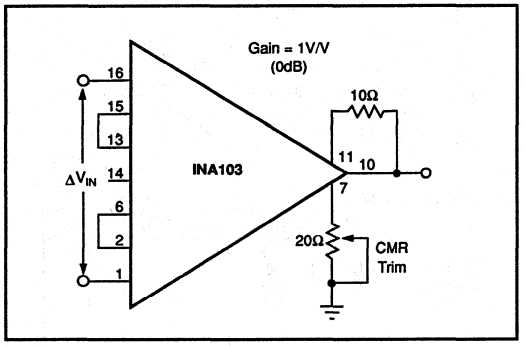


FIGURE 11. Optional Circuit for Externally Trimming CMR.

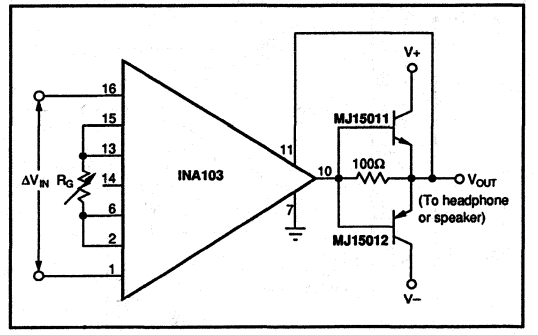


FIGURE 12. Current Boosting the Output.

INPUT IMPEDANCE AND PROTECTION CONSIDERATIONS

As with any low noise circuit, careful layout and power supply bypassing is necessary to prevent the coupling of noise sources into the INA103 through the power supply or from EMI radiation.

A return path for the input bias currents must always be provided. A resistor from the input to common will properly bias floating sources such as transformers, thermocouples, and AC-coupled inputs. This resistor should be high enough in value to prevent loading the source. The input bias currents flowing through these resistors will introduce a common-mode voltage to the amplifier, and caution should be exercised to assure that this common-mode voltage, in addition to the input signal, does not cause the input amplifiers to saturate. (See Common-Mode Input Range, above).

It is often necessary to decouple the input of the INA103 from the source (for example, in audio mixing systems where the INA103 may be placed on a buss). In this case, series resistors may be used to decouple the input. The source impedance presented to the INA103 should be as low as possible, to minimize DC errors and noise which may result due to the input bias current of the INA103. In addition, resistor values should be chosen to limit the input current to the INA103 to 10mA. While it is unlikely such currents would result from a signal input, should one power supply rail be lost due to a power supply failure or other system fault, it is possible for large currents to flow from the other power supply to ground through the input stage. Setting $R_{DECOUPLE} \geq 250\Omega$ should be adequate to provide this protection. Figure 13 shows a circuit with a decoupled and protected input. A graph is included to assist in choosing the best resistor values.

Inductive source impedances may cause the INA103 to oscillate. Placing a 470pF capacitor from each input to ground will prevent oscillation in such rare instances. Typical audio applications using twisted pair or coax generally do not require these capacitors.

APPLICATIONS

Many applications of instrumentation amplifiers involve the amplification of low-level differential signals from bridges and transducers such as strain gages, thermocouples, and RTDs. Some of the important parameters include common-mode rejection (differential cancellation of common-mode offset and noise), input impedance, offset voltage and drift, gain accuracy, linearity and noise. The INA103 accomplishes all of these with high precision.

In addition, the INA103 has been designed to provide extremely low noise and distortion for dynamic applications such as microphone preamplifiers in professional-quality mixing consoles.

Although the INA103 contains internal 3kΩ feedback resistors to set input stage gain, external feedback resistors can be used, as shown in Figure 14. For gains other than 1 or 100, it is possible to improve gain accuracy and gain temperature coefficient by using matched external feedback and gain set resistors (the internal feedback resistors can have 50ppm/°C TCR). Other amplifiers, such as the AD625, have no internal feedback resistors. When using the INA103 to replace the AD625 in existing circuits, the external feedback resistors present in the existing circuit may be used (see Figure 14), or the circuit may be modified to take advantage of the INA103's internal resistors.

The INA103 input amplifiers are current feedback type. The value of the feedback resistors affects the dynamic performance and stability. Feedback resistors less than 2.5kΩ may result in instability. Feedback resistors larger than 3kΩ will result in reduced gain bandwidth and increased noise. For example, feedback resistors of 20kΩ will increase the gain-of-1000 input referred-noise of the INA103 from 1nV/√Hz to 1.5nV/√Hz.

Figure 15 is one way to make a microphone preamplifier with the INA103. This circuit is designed to allow the microphone to be phantom powered, and also allows for a 20dB pad on the input. The DC restoration circuit using the OPA627 has a low frequency cutoff of 1.59Hz, and automatically removes DC offsets from the amplified output signal.

Figures 16 through 19 show other applications circuits.

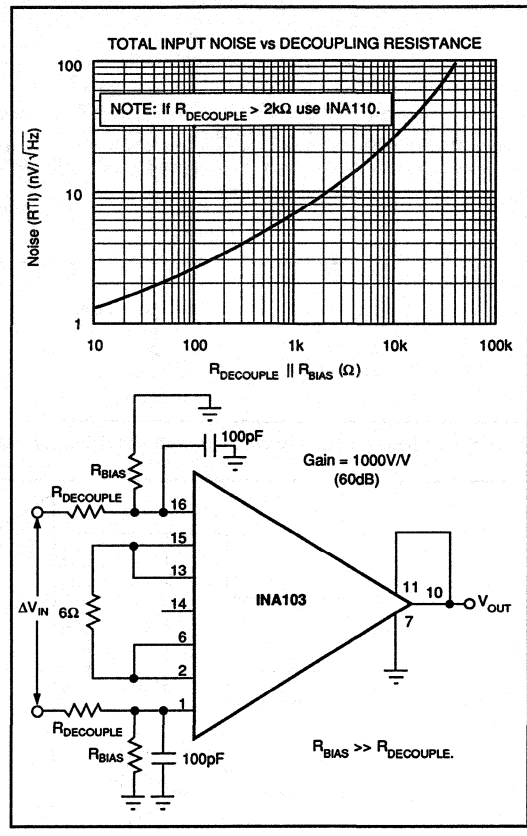


FIGURE 13. Input Decoupling and Protection.

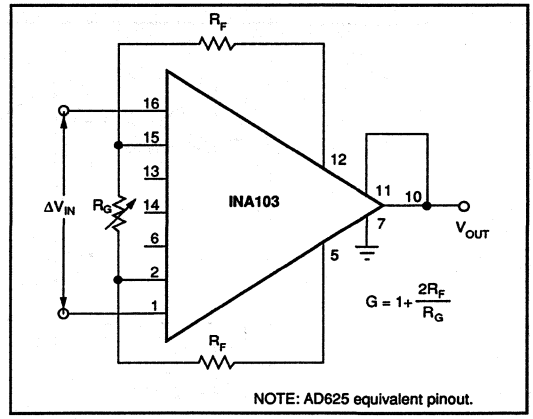


FIGURE 14. Use of External Resistors for Gain Set.

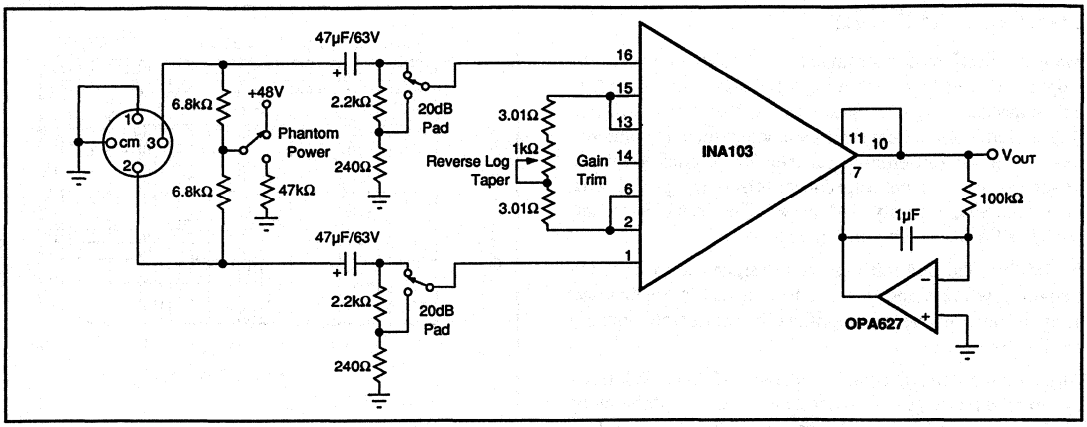


FIGURE 15.Microphone Preamplifier with Provision for Phantom Power Microphones.

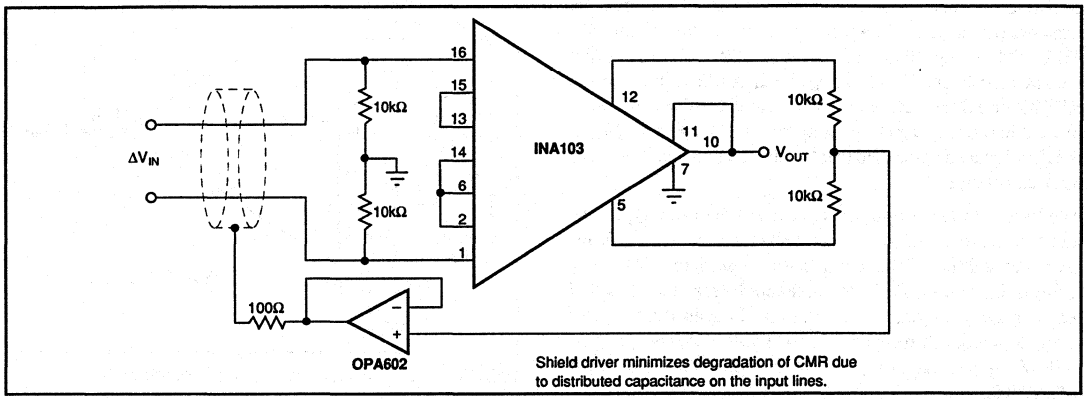


FIGURE 16. Instrumentation Amplifier with Shield Driver.

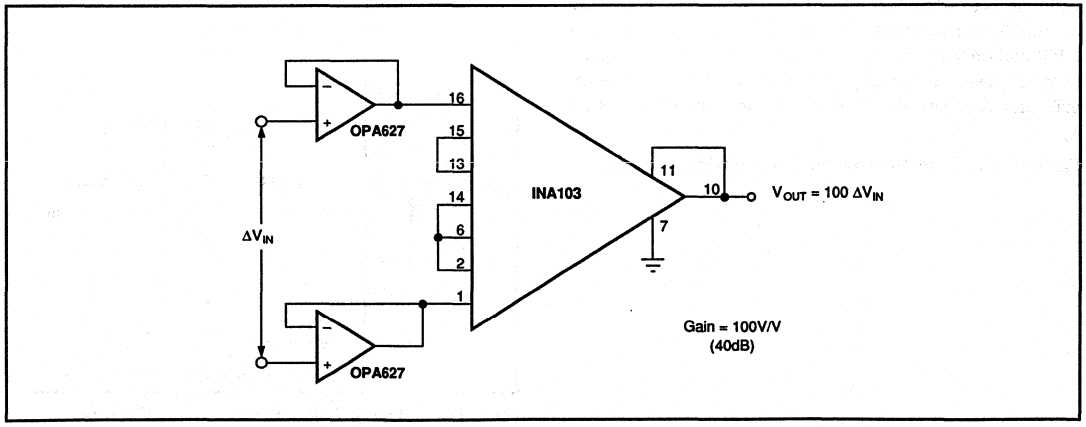


FIGURE 17. Gain-of-100 INA103 with FET Buffers.

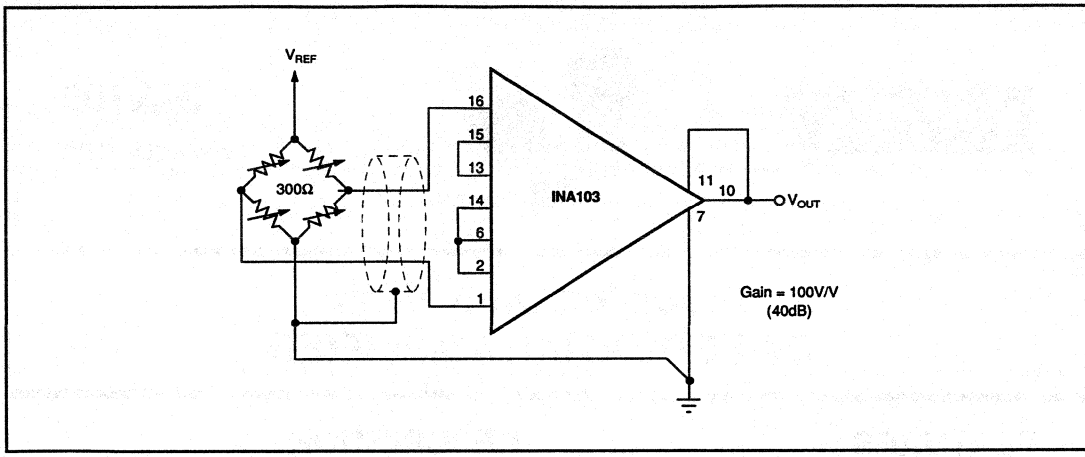


FIGURE 18. Bridge Amplifier.

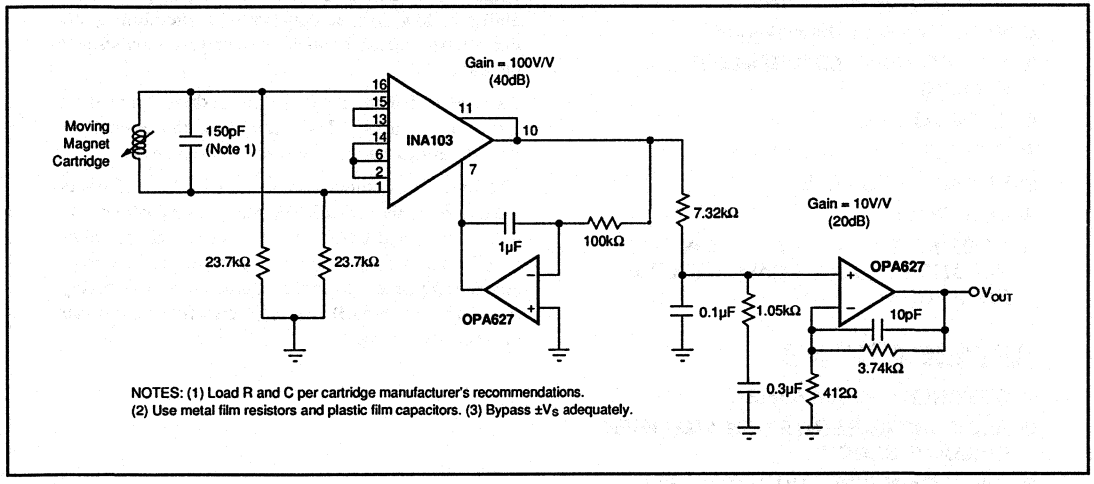


FIGURE 19. RIAA Phono Preamplifier.

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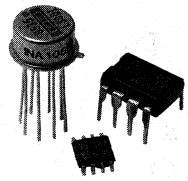


INA105

AVAILABLE IN DIE

Precision Unity Gain DIFFERENTIAL AMPLIFIER

FEATURES

- CMR 86dB min OVER TEMPERATURE
- GAIN ERROR 0.01% max
- NONLINEARITY 0.001% max
- NO EXTERNAL ADJUSTMENTS REQUIRED
- EASY TO USE
- COMPLETE SOLUTION
- HIGHLY VERSATILE
- LOW COST
- TO-99 HERMETIC METAL, LOW COST PLASTIC DIP, AND SMALL OUTLINE PACKAGES

APPLICATIONS

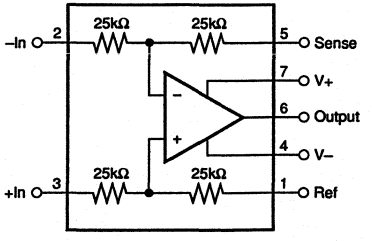
- DIFFERENTIAL AMPLIFIER
- BASIC INSTRUMENTATION AMPLIFIER BUILDING BLOCK
- UNITY-GAIN INVERTING AMPLIFIER
- GAIN-OF-1/2 AMPLIFIER
- NONINVERTING GAIN-OF-2 AMPLIFIER
- AVERAGE VALUE AMPLIFIER
- ABSOLUTE VALUE AMPLIFIER
- SUMMING AMPLIFIER
- SYNCHRONOUS DEMODULATOR
- CURRENT RECEIVER WITH COMPLIANCE TO RAILS
- 4mA TO 20mA TRANSMITTER
- VOLTAGE-CONTROLLED CURRENT SOURCE
- ALL-PASS FILTERS

DESCRIPTION

The INA105 is a precision unity-gain differential amplifier. As a monolithic circuit, it offers high reliability at low cost. It consists of a premium grade operational amplifier and an on-chip precision resistor network.

As a special feature, the INA105 can drive 20mA from the positive supply. This simplifies construction of 4mA to 20mA current sources and transmitters.

The INA105 is completely self-contained and offers the user a highly versatile function. No adjustments to gain, offset, and CMR are necessary. This provides three important advantages: (1) lower initial design engineering time, (2) lower manufacturing assembly time and cost, and (3) easy cost-effective field repair of a precision circuit.



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Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

PDS-617D

SPECIFICATIONS

ELECTRICAL

At +25°C, V_{CC} = ±15V unless otherwise noted.

PARAMETER	CONDITIONS	INA105AM MIN	INA105AM TYP	INA105AM MAX	INA105BM MIN	INA105BM TYP	INA105BM MAX	INA105KP/KU MIN	INA105KP/KU TYP	INA105KP/KU MAX	UNITS
GAIN											
Initial[1]			1			*			*		V/V
Error			0.005	0.01		*	*		0.01	0.025	%
vs Temperature			1	5		*	*		*		ppm/°C
Nonlinearity[2]			0.0002	0.001		*	*		*	*	%
OUTPUT											
Rated Voltage	I_O = +20mA, –5mA	10	12		*	*		*	*		V
Rated Current	V_O = 10V	+20, –5			*			*			mA
Impedance			0.01			*			*		Ω
Current Limit	To Common		+40/–10			*			*		mA
Capacitive Load	Stable Operation		1000			*			*		pF
INPUT											
Impedance[3]	Differential		50			*			*		kΩ
	Common-mode		50			*			*		kΩ
Voltage Range[4]	Differential	±10			*			*			V
	Common-mode	±20			*			*			V
Common-mode Rejection[5]	$T_A = T_{MIN}$ to T_{MAX}	80	90		86	100		72	*		dB
OFFSET VOLTAGE	RTO[6][7]										
Initial			50	250		*	*		*	500	µV
vs Temperature			5	20		5	10		*		µV/°C
vs Supply	$\pm V_S$ = 6V to 18V		1	25		*	15		*	*	µV/V
vs Time			20			*			*		µV/mo
OUTPUT NOISE VOLTAGE	RTO[6][8]										
f_B = 0.01Hz to 10Hz			2.4			*			*		µVp-p
f_O = 10kHz			60			*			*		nV/√Hz
DYNAMIC RESPONSE											
Small Signal	–3dB		1			*			*		MHz
Full Power BW	V_O = 20Vp-p	30	50		*	*		*	*		kHz
Slew Rate		2	3		*	*		*	*		V/µs
Settling Time: 0.1%	V_O = 10V Step		4			*			*		µs
0.01%	V_O = 10V Step		5			*			*		µs
0.01%	V_{CM} = 10V Step, V_{DIFF} = 0V		1.5			*			*		µs
POWER SUPPLY											
Rated			±15			*			*		V
Voltage Range	Derated Performance	±5		±18	*		*	*		*	V
Quiescent Current	V_O = 0V		±1.5	±2		*	*		*	*	mA
TEMPERATURE RANGE											
Specification		–25		+85	*		*	0		+70	°C
Operation		–55		+125	*		*	–25		+85	°C
Storage		–65		+150	*		*	–40		+85	°C

* Specification same as for INA105AM.

NOTES: (1) Connected as difference amplifier (see Figure 4). (2) Nonlinearity is the maximum peak deviation from the best-fit straight line as a percent of full-scale peak-to-peak output. (3) 25kΩ resistors are ratio matched but have ±20% absolute value. (4) Maximum input voltage without protection is 10V more than either ±15V supply (±25V). Limit I_{IN} to 1mA. (5) With zero source impedance (see "Maintaining CMR" section). (6) Referred to output in unity-gain difference configuration. Note that this circuit has a gain of 2 for the operational amplifier's offset voltage and noise voltage. (7) Includes effects of amplifier's input bias and offset currents. (8) Includes effects of amplifier's input current noise and thermal noise contribution of resistor network.

ABSOLUTE MAXIMUM RATINGS

Supply	±18V
Input Voltage Range	$\pm V_S$
Operating Temperature Range: M	–55°C to +125°C
P, U	–40°C to +85°C
Storage Temperature Range	–65°C to +150°C
Lead Temperature (soldering, 10s) M, P	+300°C
Wave Soldering (3s, max) U	+260°C
Output Short Circuit to Common	Continuous

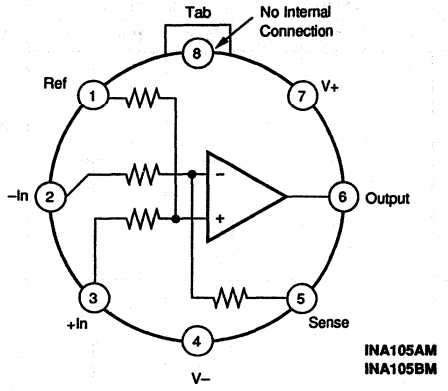
ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE
INA105AM	TO-99 Metal	–25°C to +85°C
INA105BM	TO-99 Metal	–25°C to +85°C
INA105KP	8-pin Plastic DIP	0°C to +70°C
INA105KU	8-pin SOIC	0°C to +70°C

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

PIN DESIGNATIONS

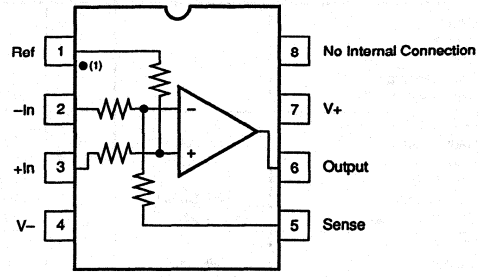
TOP VIEW
TO-99



INA105AM
INA105BM

Case internally connected to V–. Make no connection.

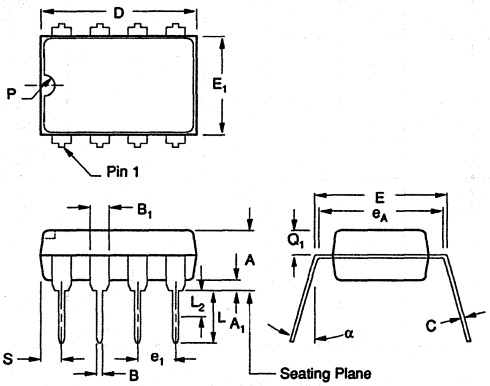
TOP VIEW
PLASTIC DIP AND SMALL OUTLINE
INA105



NOTE: (1) Performance grade identifier box for small outline surface mount. Blank indicates K grade. Part is marked INA105U.

MECHANICALS

P Package — 8-Pin Plastic DIP

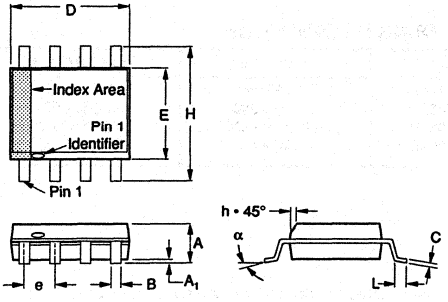


DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.155	.200	3.94	5.08
A1	.020	.050	0.51	1.27
B	.014	.020	0.36	0.51
B1	.045	.065	1.14	1.65
C	.008	.012	0.20	0.30
D (1)	.370	.400	9.40	10.16
E	.300	.325	7.62	8.26
E1	.240	.260	6.10	6.60
e1	.100 BASIC		2.54 BASIC	
eA	.300 BASIC		7.62 BASIC	
L	.125	.150	3.18	3.81

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
L2(2)	0	.030	0.00	0.76
α	0°	15°	0°	15°
P	.015	.050	0.38	1.270
Q1	.040	.075	1.02	1.91
S (1)	.015	.050	0.38	1.27

(1) Not JEDEC Std.
(2) e_1 and e_A apply in zone L_2 when unit installed.
NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

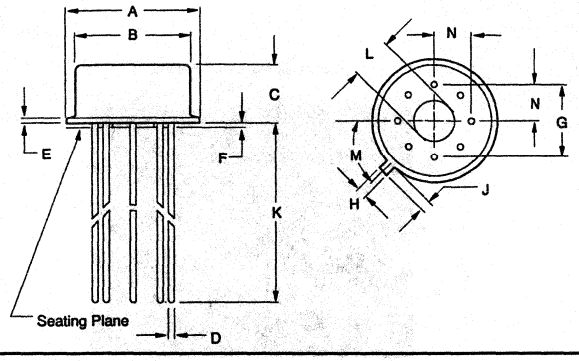
U Package — 8-Pin SO-8 Surface Mount



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.054	.068	1.37	1.73
A1	.004	.009	0.10	0.23
B	.014	.019	0.36	0.48
C	.008	.0098	0.20	0.25
D	.189	.196	4.80	4.98
E	.150	.157	3.81	3.99
e	.050 BASIC		1.27 BASIC	
H	.229	.244	5.82	6.20
h	.010	.019	0.25	0.48
L	.016	.050	0.41	1.27
N	8		8	
α	0°	8°	0°	8°

NOTES:
1. Dimensioning and tolerancing per ANSI Y14.5M–1982.
2. "D" and "E" are reference datums and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm (.086 in.)
3. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the cross-hatched area.
4. "L" is the length of the terminal for soldering to a substrate.
5. "N" is the number of terminal positions.

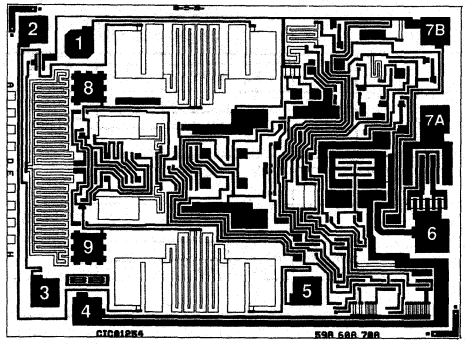
M Package — Metal TO-99



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.335	.370	8.51	9.40
B	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.200 BASIC		5.08 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500	—	12.7	—
L	.110	.160	2.79	4.06
M	45° BASIC		45° BASIC	
N	.095	.105	2.41	2.67

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Tab is pin 8.

DICE INFORMATION



INA105 DIE TOPOGRAPHY

PAD	FUNCTION
1	Reference
2	–In
3	+In
4	V–
5	Sense
6	Output
7A	V+ (Connect Both)
7B	V+ (Connect Both)
8	(Op Amp +In)
9	(Op Amp –In)

Substrate Bias: Electrically connected to V– supply.

MECHANICAL INFORMATION

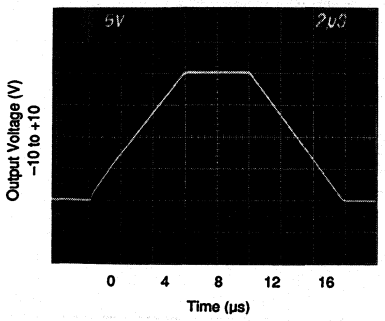
	MILS (0.001")	MILLIMETERS
Die Size	83 x 63 ±5	2.11 x 1.60 ±0.13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.10 x 0.10
Backing: Gold		

See "DICE PRODUCTS" Section 17 in Data Book Supplement Volume 33c, or contact Burr-Brown for current information.

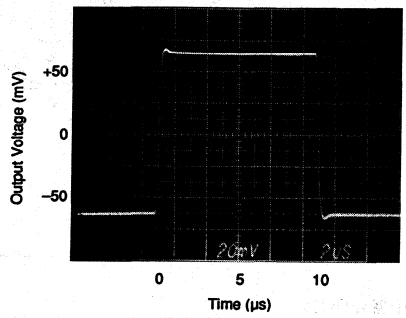
TYPICAL PERFORMANCE CURVES

T_A = 25°C, V_S = ±15V unless otherwise noted.

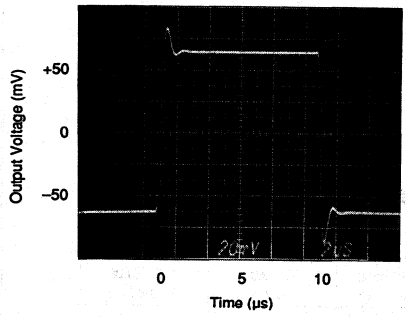
STEP RESPONSE



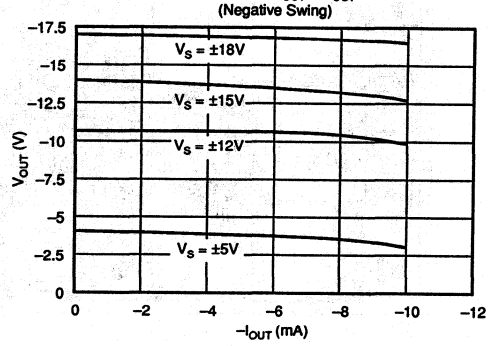
SMALL SIGNAL RESPONSE
(No Load)



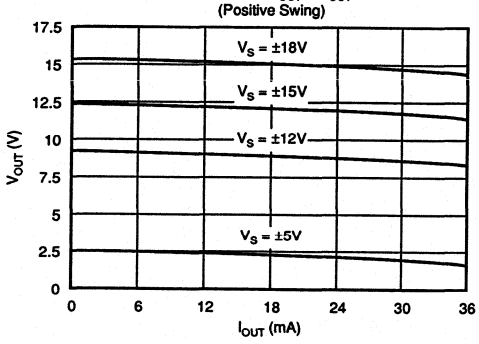
SMALL SIGNAL RESPONSE
(R_{LOAD} = ∞Ω, C_{LOAD} = 1000pF)



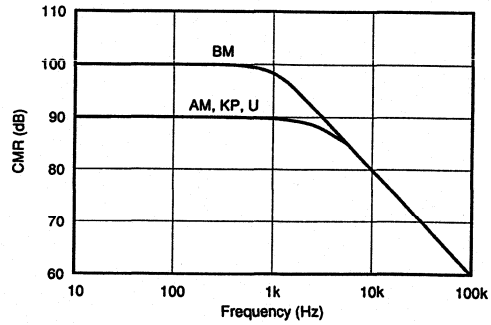
MAXIMUM V_{OUT} vs I_{OUT}
(Negative Swing)



MAXIMUM V_{OUT} vs I_{OUT}
(Positive Swing)

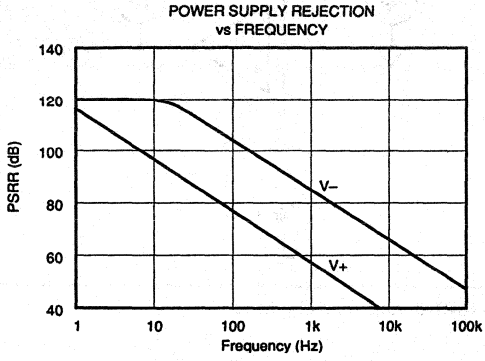


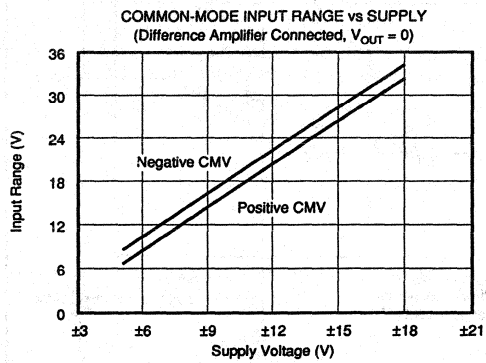
CMR vs FREQUENCY



TYPICAL PERFORMANCE CURVES (CONT)

T_A = 25°C, V_S = ±15V unless otherwise noted.





DISCUSSION OF PERFORMANCE

The INA105 is the new solution to a widely occuring problem—how to realize a very accurate unity-gain differential amplifier at low cost. Burr-Brown's solution is a reliable monolithic circuit including both operational amplifier and thin-film resistors on the chip. State-of-the-art laser-trimming techniques assure total error of less than ±0.015% (gain error, nonlinearity, offsets, and common-mode rejection).

The performance of the unity-gain differential amplifier circuit can mistakenly be taken for granted. The necessary resistor accuracy is difficult to achieve, especially over temperature. Two classical techniques employed for obtaining the necessary accuracy are either manual trimming or the use of available packaged matched and tracking resistor networks. Both are expensive compared to the cost of the complete INA105.

The INA105 provides the total solution. By using a computer-controlled laser-trimming procedure, both accuracy and low cost are guaranteed. This makes external adjustment of gain, CMR, and offset voltage unnecessary. The user can be assured of excellent accuracy over temperature due to the properties inherent in Burr-Brown's thin-film resistors.

Other advantages are also apparent. Design, purchasing, and inventory costs are reduced. Labor time in adjusting independent resistors is eliminated both during manufacturing and field repair. Best of all, expensive potentiometers are not required. This further enhances circuit reliability.

BASIC POWER SUPPLY AND SIGNAL CONNECTIONS

Figure 1 shows the proper connections for power supply and signal. Supplies should be decoupled with 1µF tantalum capacitors as close to the amplifier as possible. To avoid gain and CMR errors introduced by the external circuit, connect grounds as indicated, being sure to minimize ground resistance.

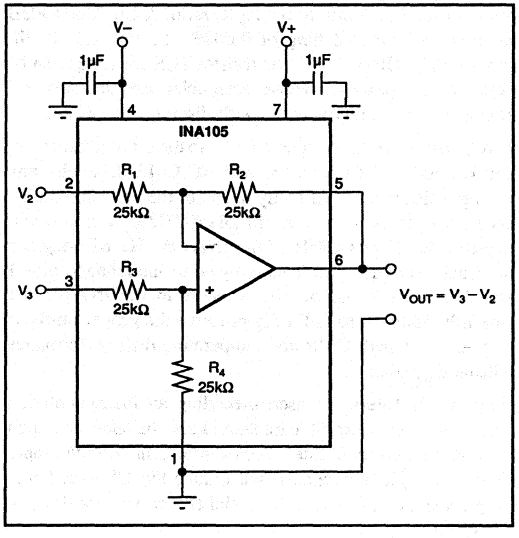


FIGURE 1. Basic Power Supply and Signal Connections.

OFFSET ADJUSTMENT

Figure 2 shows the offset adjustment circuit for the INA105. This circuit will allow ±300µV of adjustment and will not affect the gain accuracy or CMR.

MAINTAINING COMMON-MODE REJECTION

Two factors are important in maintaining high CMR: (1) resistor matching and tracking (the internal INA105 circuitry does this for the user) and (2) source impedance including its imbalance.

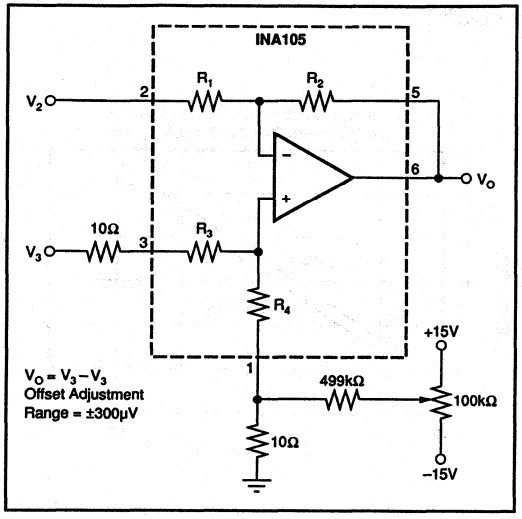


FIGURE 2. Offset Adjustment.

Referring to Figure 1, the CMR depends upon the match of the internal R_4/R_3 ratio to the R_1/R_2 ratio. A CMR of 100dB requires resistor matching of 0.002%. To maintain 86dB, minimum CMR to +85°C, the resistor TCR tracking must be better than 2ppm/°C. These accuracies are difficult and expensive to reliably achieve with discrete components.

Any source impedance adds directly to the input resistors, R_1 and R_3, and will degrade DC and AC CMR. Likewise any wiring resistance adds directly to any of the precision difference resistors. A resistance of 0.5Ω (0.002% of 25kΩ) will degrade the 100dB CMR of the INA105; 5Ω will degrade the CMR to 80dB. Don't be tempted to interchange pins 1 and 3 or pins 2 and 5. The resistors in the INA105 are carefully matched to faithfully preserve the proper ratios. If they are switched, CMR and temperature drift performance will be degraded.

When input filters are used preceding an instrumentation amplifier (see Figure 5), care should also be taken to match RCs on the two input lines. For example, mismatched input filters for high frequencies will reduce the CMR at lower frequencies, e.g, 60Hz. Differential filters will not degrade AC CMR.

RESISTOR NOISE IN THE INA105

Figure 3 shows the model for calculating resistor noise in the INA105. Resistors have Johnson noise resulting from thermal agitation. The expression for this noise is:

$$V_{RMS} = \sqrt{4KTRB}$$

Where: K = Boltzman's constant (J/°K)
T = Absolute temperature (°K)
R = Resistance (Ω)
B = Bandwidth (Hz)

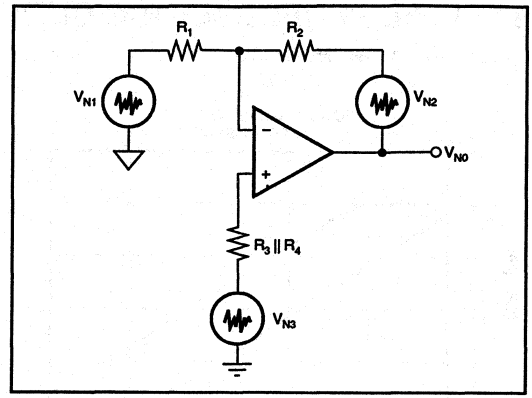


FIGURE 3. Resistor Noise Model.

At room temperature, this noise becomes:

$$V_N = 1.3^{-10}\sqrt{R} \qquad (V/\sqrt{Hz})$$

The three noise sources in Figure 2 are:

$$V_{N1} = 1.3^{-10}(R_2/R_1)\sqrt{R_1}$$

$$V_{N2} = 1.3^{-10}\sqrt{R_2}$$

$$V_{N3} = 1.3^{-10}(1 + R_2/R_1)\sqrt{R_3 \| R_4}$$

The output noise (given $R_1 = R_2 = R_3 = R_4 = 25k\Omega$) is:

$$V_{NO} = 2.6^{-10}\sqrt{R}$$

$$\boxed{V_{NO} = 41nV_{RMS}/\sqrt{Hz}}$$

For example,

V_{NO} within a

100Hz BW = $410nV_{RMS}$
= 2460nVp-p with a crest factor of 6 (statistically includes 99.7% of all noise peak occurrences)

This is the noise due to the resistors alone. It is included in the noise specification of the INA105.

APPLICATIONS CIRCUITS

The INA105 is ideally suited for a wide range of circuit functions. Figures 4 through 29 show many applications circuits ranging from difference amplifiers and single-ended gain blocks to average and absolute value amplifiers. It is ideal as a current-loop receiver. Also, since the positive output current drive has been extended, it serves uniquely as a current transmitter for ranges such as 4mA to 20mA. When using these applications recall that the internal 25kΩ resistors are ratio-matched but ±20% absolute.

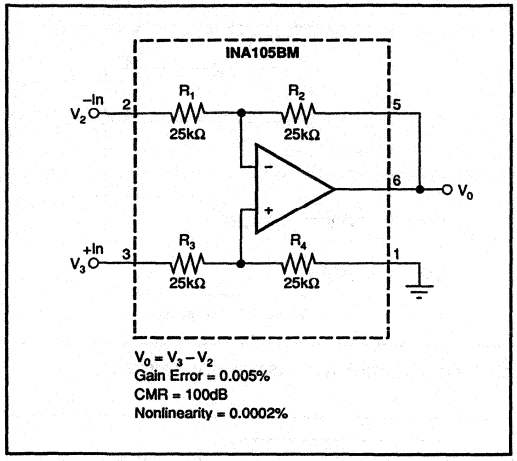
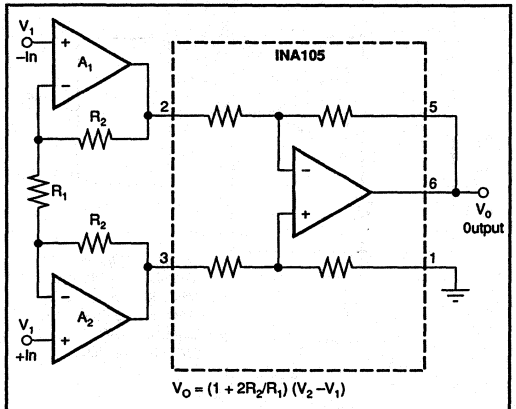


FIGURE 4. Precision Difference Amplifier.



For low source impedance applications, an input stage using OPA27 op amps will give the best low noise, offset, and temperature drift performance. At source impedances above about 10kΩ, the bias current noise of the OPA27 reacting with the input impedance begins to dominate the noise performance. For these applications, using the OPA111 or Dual OPA2111 FET input op amp will provide lower noise performance. For lower cost use the OPA121 plastic. To construct an electrometer use the OPA128.

A_1, A_2	R_1 (Ω)	R_2 (Ω)	GAIN (V/V)	CMRR (dB)	MAX I_B	NOISE AT 1kHz (nV/√HZ)
OPA27A	50.5	2.5k	100	128	40nA	4
OPA111B	202	10k	100	110	1pA	10
OPA128LM	202	10k	100	118	75fA	38

FIGURE 5. Precision Instrumentation Amplifier.

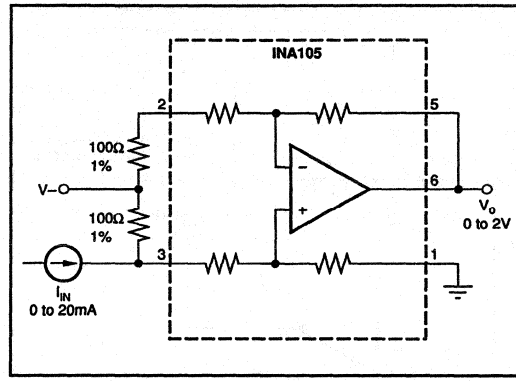


FIGURE 6. Current Receiver with Compliance to Rails.

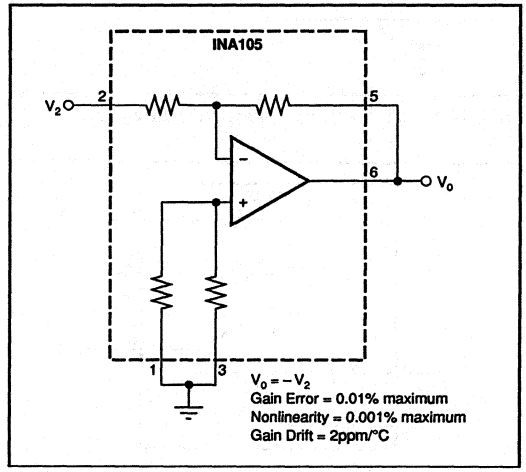


FIGURE 7. Precision Unity-Gain Inverting Amplifier.

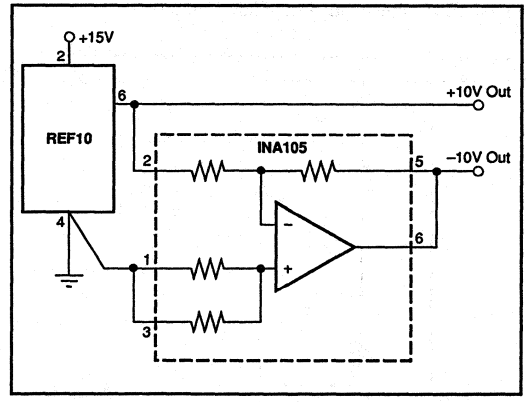


FIGURE 8. ±10V Precision Voltage Reference.

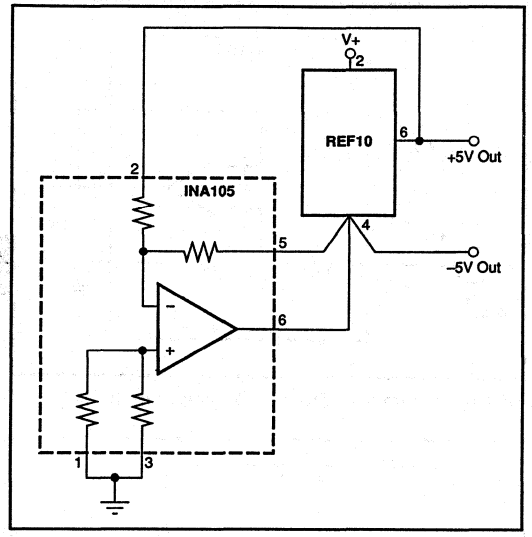


FIGURE 9. ±5V Precision Voltage Reference.

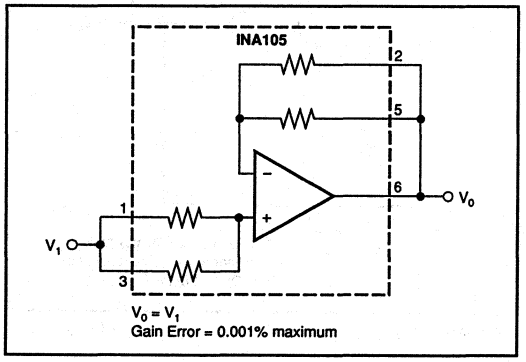


FIGURE 10. Precision Unity-Gain Buffer.

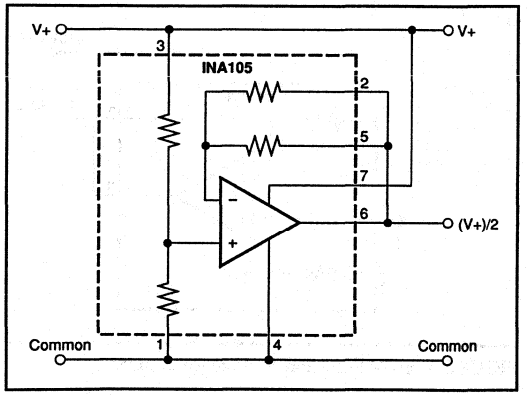


FIGURE 11. Pseudoground Generator.

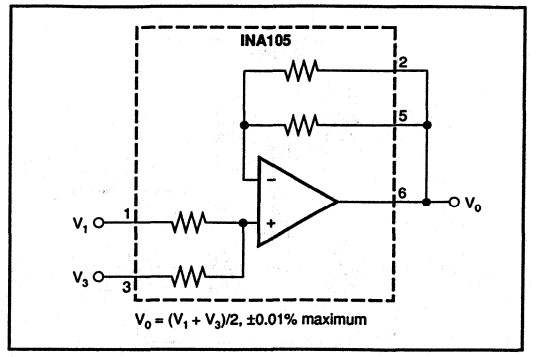


FIGURE 12. Precision Average Value Amplifier.

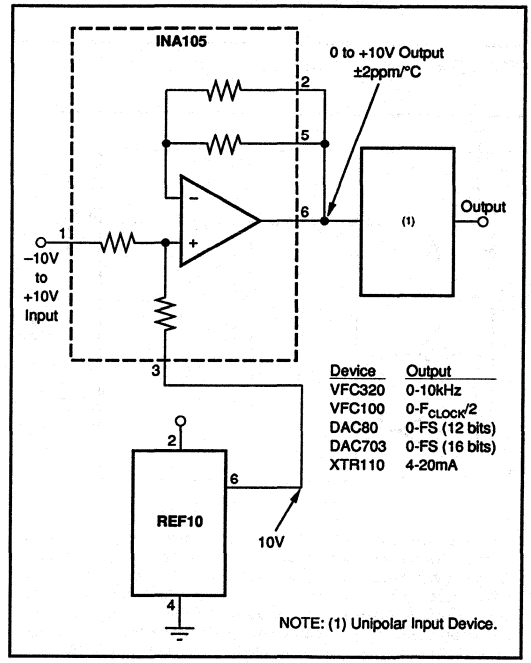


FIGURE 13. Precision Bipolar Offsetting.

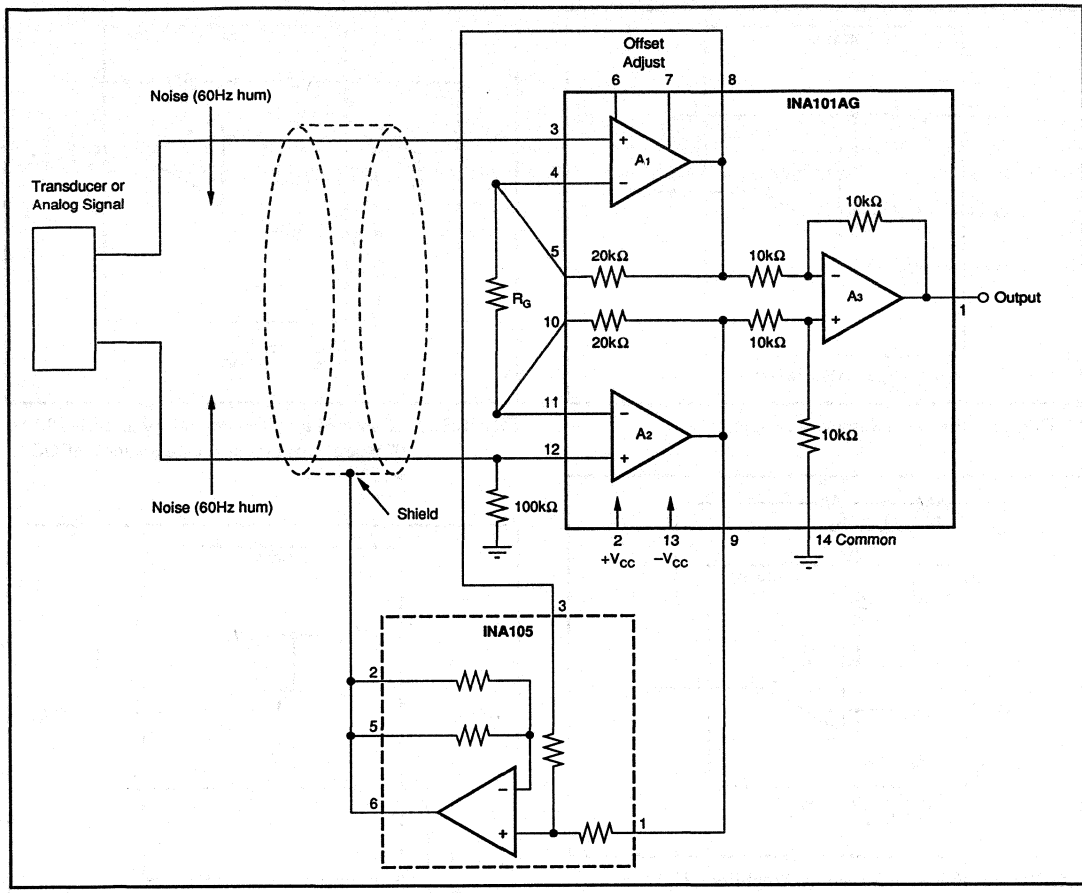


FIGURE 14. Instrumentation Amplifier Guard Drive Generator.

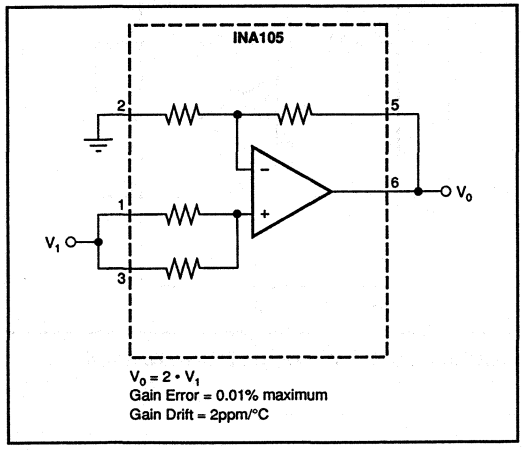


FIGURE 15. Precision (G = 2) Amplifier.

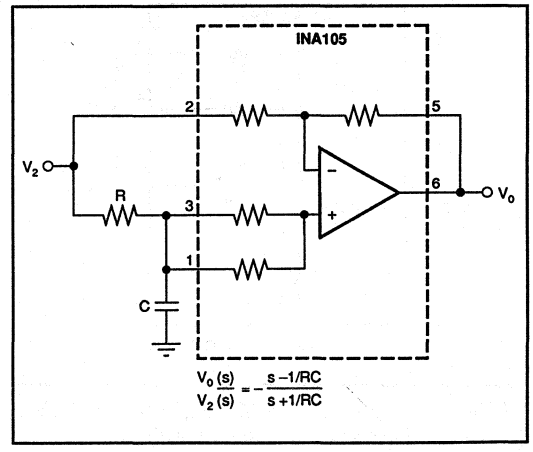


FIGURE 16. All-Pass Filter (provides unity gain and 0° to 180° phase shift output for frequencies of DC to ∞Hz).

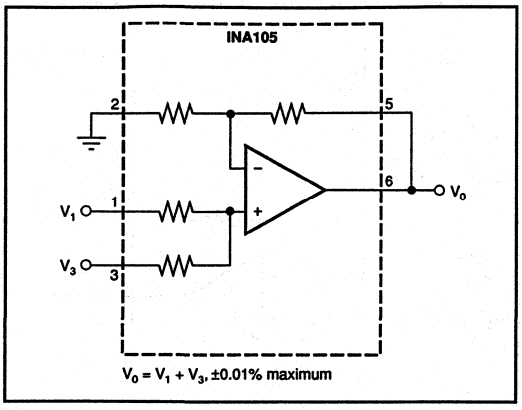


FIGURE 17. Precision Summing Amplifier.

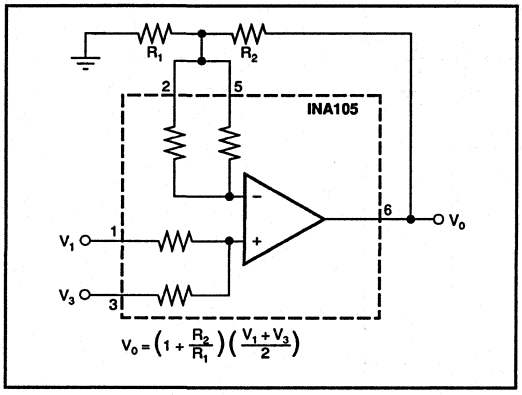


FIGURE 18. Precision Summing Amplifier with Gain.

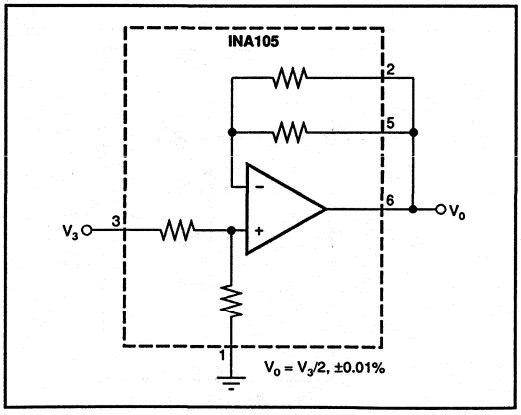


FIGURE 19. Precision (Gain = 1/2) Amplifier. Allows ±20V input with ±15V power supplies.

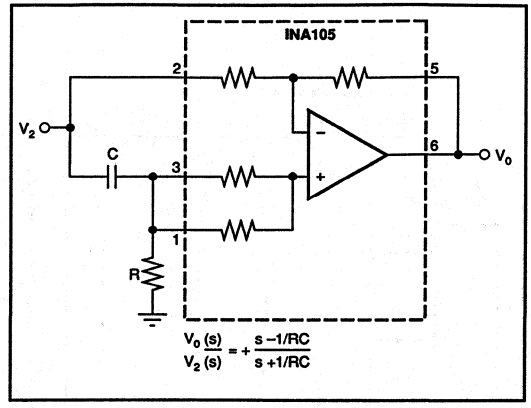


FIGURE 20. All-Pass Filter (provides unity gain and –180° to 0° phase shift output for frequencies of DC to ∞Hz).

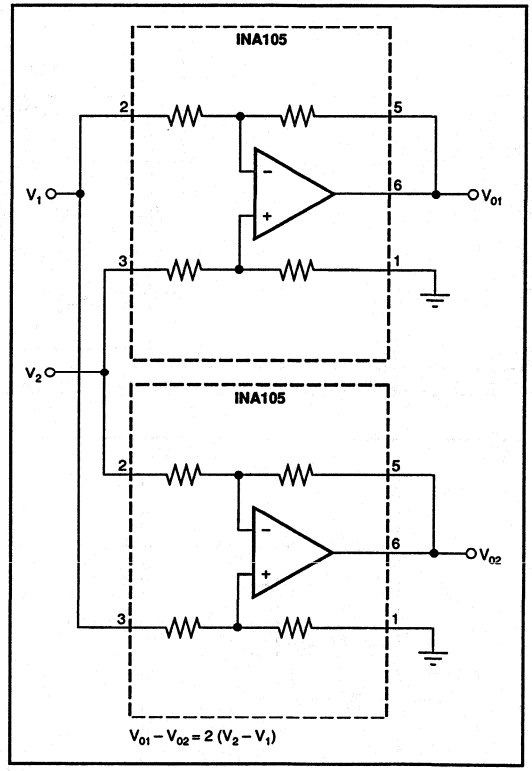


FIGURE 21. Differential Output Difference Amplifier.

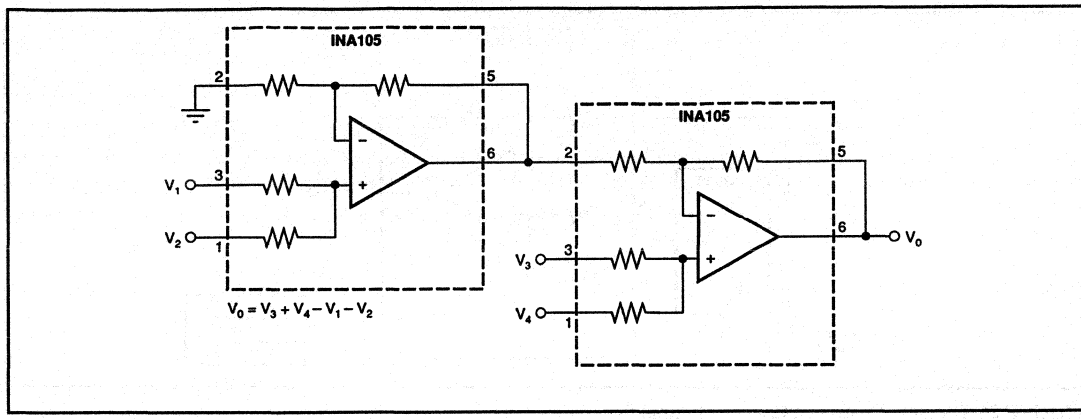


FIGURE 22. Precision Summing Instrumentation Amplifier.

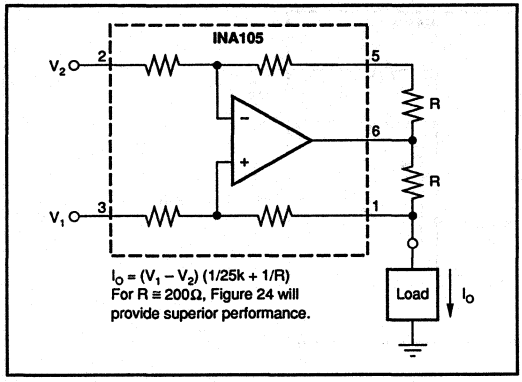


FIGURE 23. Precision Voltage-to-Current Converter with Differential Inputs.

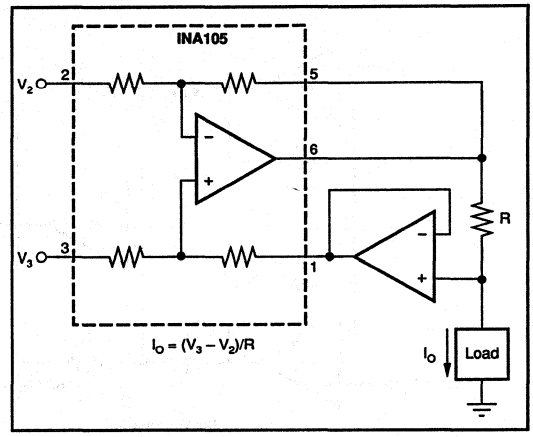


FIGURE 24. Differential Input Voltage-to-Current Converter for Low I_{OUT}.

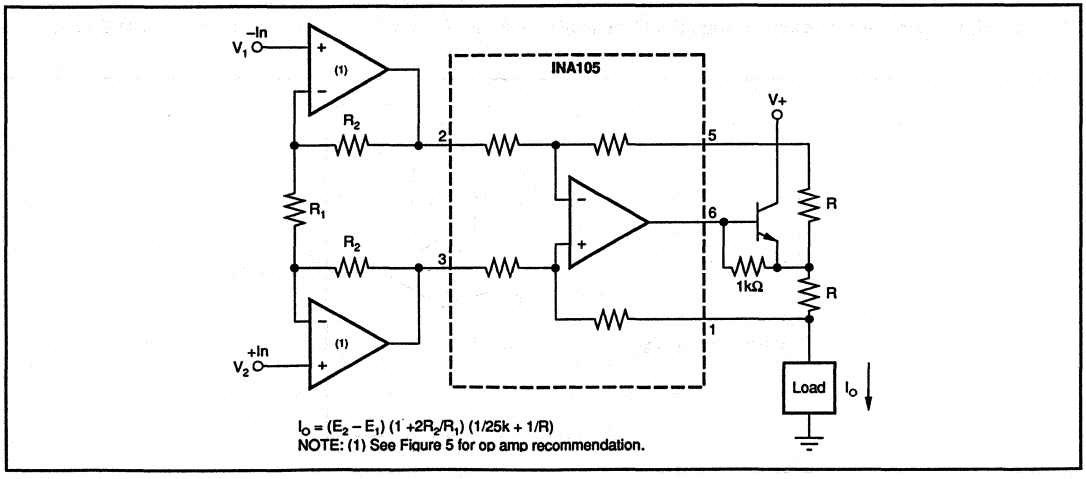


FIGURE 25. Precision Voltage-Controlled Current Source with Buffered Differential Inputs and Gain.

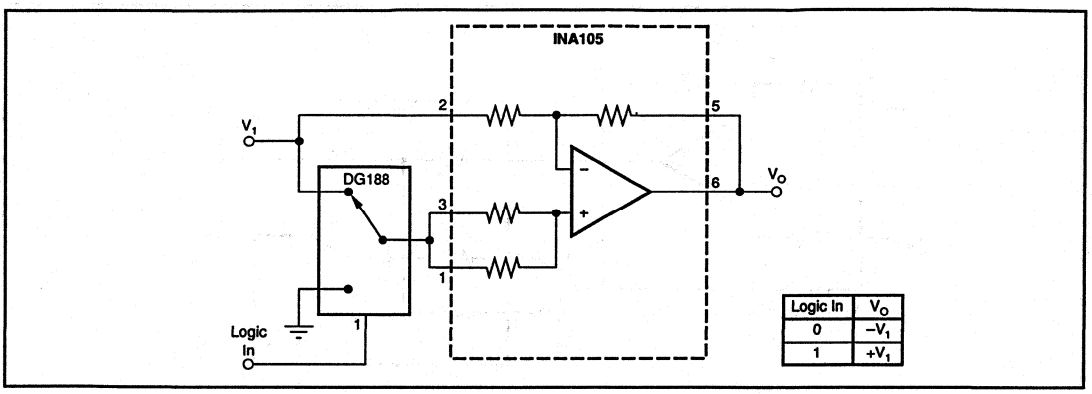


FIGURE 26. Digitally Controlled Gain of ±1 Amplifier.

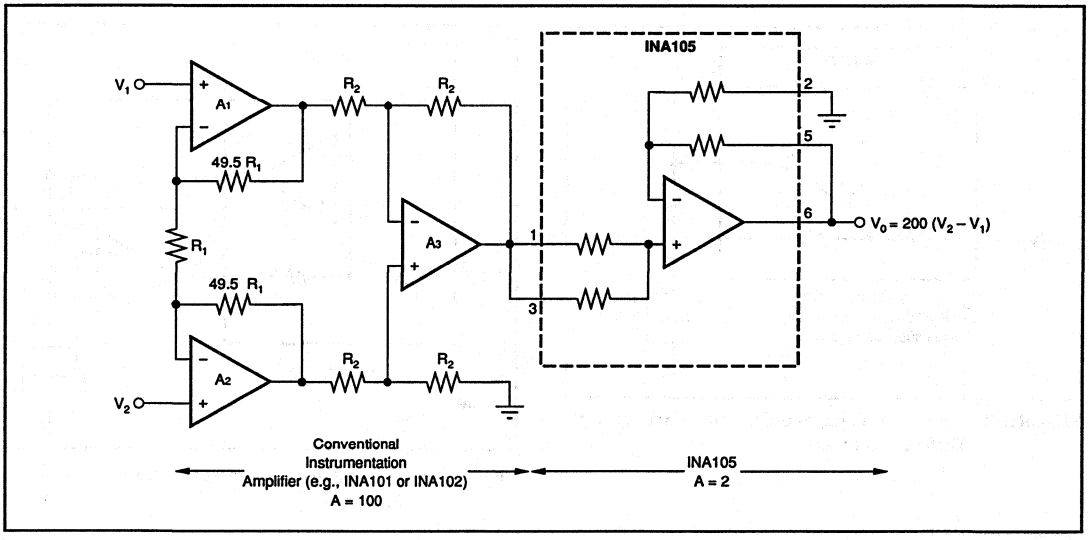


FIGURE 27. Boosting Instrumentation Amplifier Common-Mode Range From ±5 to ±7.5V with 10V Full-Scale Output.

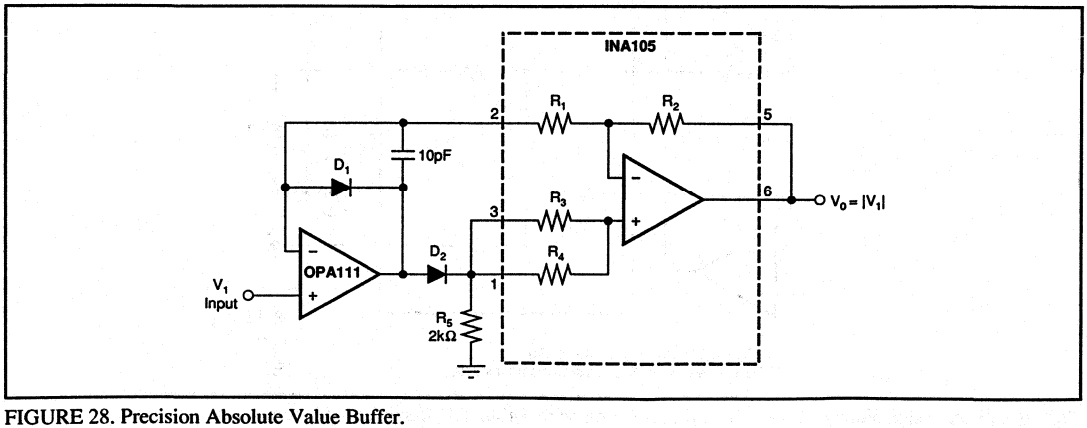


FIGURE 28. Precision Absolute Value Buffer.

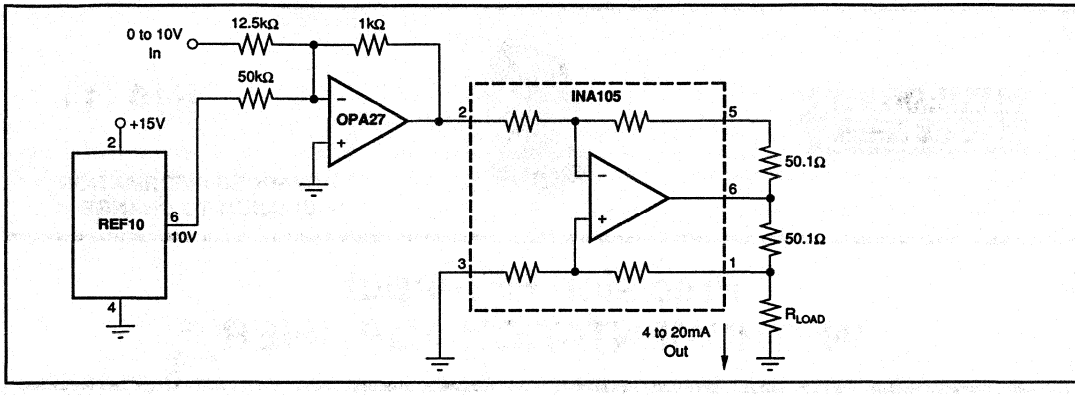


FIGURE 29. Precision 4-20mA Current Transmitter.

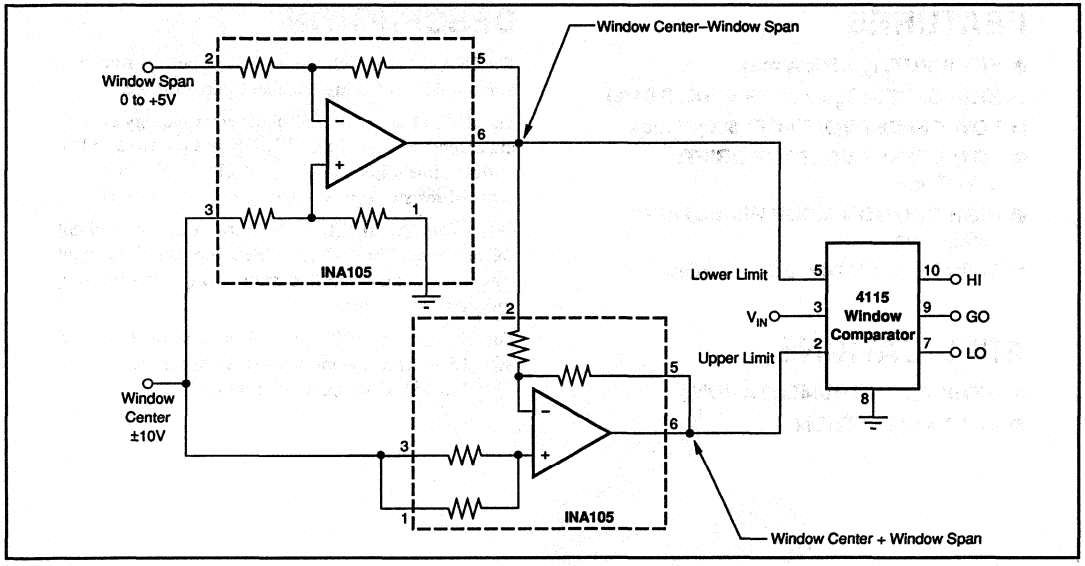


FIGURE 30. Window Comparator with Window Span and Window Center Inputs.

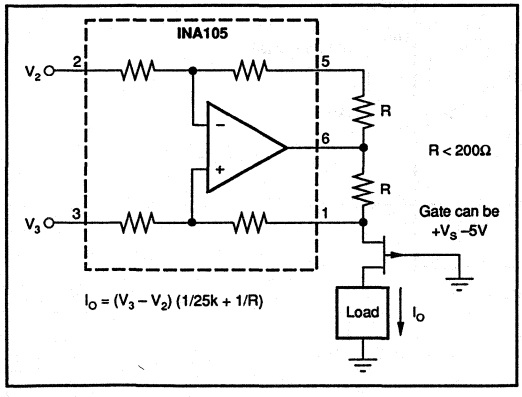


FIGURE 31. Isolating Current Source.

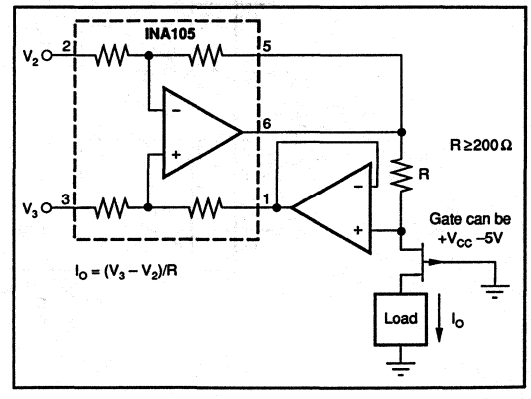


FIGURE 32. Isolating Current Source with Buffering Amplifier for Greater Accuracy.

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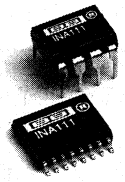


INA111

ADVANCED INFORMATION
SUBJECT TO CHANGE

Precision FET-Input INSTRUMENTATION AMPLIFIER

FEATURES

- **FET INPUT: I_B = 50pA max**
- **HIGH SPEED: T_S = 4µs (G = 100, 0.01%)**
- **LOW OFFSET VOLTAGE: 500µV max**
- **LOW OFFSET VOLTAGE DRIFT: 5µV/°C max**
- **HIGH COMMON-MODE REJECTION: 106dB min**
- **8-PIN PLASTIC DIP, SOL-16 SOIC**

APPLICATIONS

- **MEDICAL INSTRUMENTATION**
- **DATA ACQUISITION**

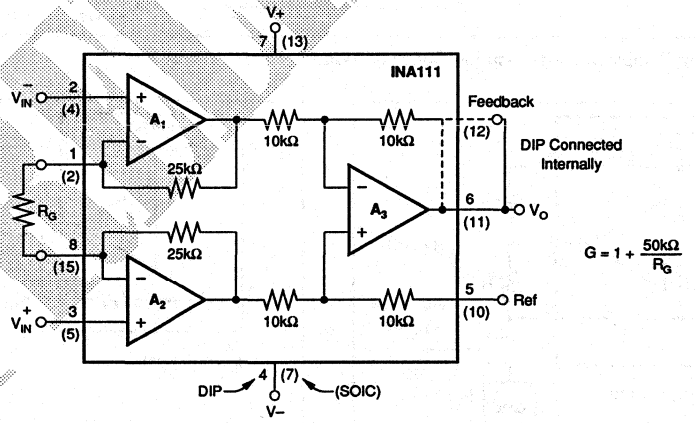
DESCRIPTION

The INA111 is a high speed, FET-input instrumentation amplifier offering excellent performance.

The INA111 uses a current-feedback topology providing extended bandwidth (2.5MHz at G = 10) and fast settling time (4µs to 0.01% at G = 100). A single external resistor sets any gain from 1 to over 1000.

Offset voltage and drift are laser trimmed for excellent DC accuracy. The INA111's FET inputs reduce input bias current to under 50pA, simplifying input filtering and limiting circuitry.

The INA111 is available in 8-pin plastic DIP, and SOL-16 surface-mount packages, specified for the –40°C to +85°C temperature range.



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PDS-1143

PRELIMINARY

SPECIFICATIONS

ELECTRICAL

T_A = +25°C, V_S = ±15V, R_L = 2kΩ, unless otherwise noted.

PARAMETER	CONDITIONS	INA111BP MIN	INA111BP TYP	INA111BP MAX	INA111AP/AU MIN	INA111AP/AU TYP	INA111AP/AU MAX	UNITS
INPUT								
Offset Voltage, RTI								
Initial	T_A = +25°C		±50 + 600/G	±500 + 3000/G		±200 + 20000/G	±1000 + 5000/G	µV
vs Temperature	T_A = T_{MIN} to T_{MAX}		±2 + 10/G	±5 + 50/G		±2 + 20/G	±5 + 100/G	µV/°C
vs Power Supply	V_S = ±6V to ±18V		3 +10/G	30 + 300/G		4 + 60/G	30 + 300/G	µV/V
Impedance, Differential			10^{12} || 6			*		Ω || pF
Common-Mode			10^{12} || 1			*		Ω || pF
Input Common-Mode Range	V_{DIFF} = 0V	±10	±12		*	*		V
Common-Mode Rejection	V_{CM} = ±10V, ΔR_S = 1kΩ							
	G = 1	80	90		70	90		dB
	G = 10	96	104		86	104		dB
	G = 100	106	115		100	110		dB
	G = 1000	106	120		100	110		dB
BIAS CURRENT			±20	±50		*	±100	pA
OFFSET CURRENT			±10	±25		*	±50	pA
NOISE VOLTAGE, RTI	G = 1000, R_S = 0Ω							
f = 100Hz			18			*		nV/√Hz
f = 1kHz			12			*		nV/√Hz
f = 10kHz			10			*		nV/√Hz
f_B = 0.1Hz to 10Hz			1			*		µVp-p
Noise Current								
f = 10kHz			1.8			*		fA/√Hz
GAIN								
Gain Equation			1 + (50kΩ/R_G)			*		V/V
Range of Gain		1		10000	*		*	V/V
Gain Error	G = 1		±0.01	±0.02		*	0.05	%
	G = 10		±0.1	±0.25		*	±0.5	%
	G = 100		±0.15	±0.3		*	±0.7	%
	G = 1000		±0.25	±0.5		*	±1	%
Gain vs Temperature	G = 1		±5	±10		*	±20	ppm/°C
50kΩ Resistance[1]			±25	±50	±25	±100		ppm/°C
Nonlinearity	G = 1		±0.0005	±0.005		*	±0.01	% of FSR
	G = 10		±0.001	±0.005		*	±0.01	% of FSR
	G = 100		±0.001	±0.01		*	±0.02	% of FSR
	G = 1000		±0.005	±0.02		*	±0.04	% of FSR
OUTPUT								
Voltage	I_O = 5mA, T_{MIN} to T_{MAX}	±10	±12.7	*	*			V
Load Capacitance Stability			5000			*		pF
Short Circuit Current			±25			*		mA
FREQUENCY RESPONSE								
Bandwidth, –3dB	G = 1		2.5			*		MHz
	G = 10		2.5			*		MHz
	G = 100		470			*		kHz
	G = 1000		50			*		kHz
Slew Rate	V_O = ±10V, G = 1 to 100		17			*		V/µs
Settling Time, 0.01%	G = 1		5			*		µs
	G = 10		3			*		µs
	G = 100		4			*		µs
	G = 1000		30			*		µs
Overload Recovery	50% Overdrive		1			*		µs
POWER SUPPLY								
Voltage Range		±6	±15	±18	*	*	*	V
Current	V_{IN} = 0V		±3	±4		*	*	mA
TEMPERATURE RANGE								
Specification		–40		85	*		*	°C
Operating	Plastic P, U	–40		125	*		*	°C
θ_{JA}	Plastic P, U		100			*		°C/W

* Specification same as INA111BP.

NOTE: (1) Temperature coefficient of the "50kΩ" term in the gain equation.

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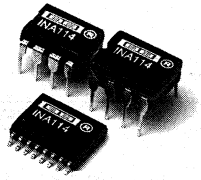


INA114

**ADVANCED INFORMATION
SUBJECT TO CHANGE**

Precision INSTRUMENTATION AMPLIFIER

FEATURES

- LOW OFFSET VOLTAGE: 50µV max
- LOW OFFSET VOLTAGE DRIFT: 0.25µV/°C max
- LOW INPUT BIAS CURRENT: 2nA max
- HIGH COMMON-MODE REJECTION: 115dB min
- INPUT OVERVOLTAGE PROTECTION: ±40V
- LOW QUIESCENT CURRENT: 3mA max
- 8-PIN PLASTIC AND CERAMIC DIP, SOL-16

APPLICATIONS

- BRIDGE AMPLIFIER
- THERMOCOUPLE AMPLIFIER
- RTD SENSOR AMPLIFIER
- MEDICAL INSTRUMENTATION
- DATA ACQUISITION SYSTEM

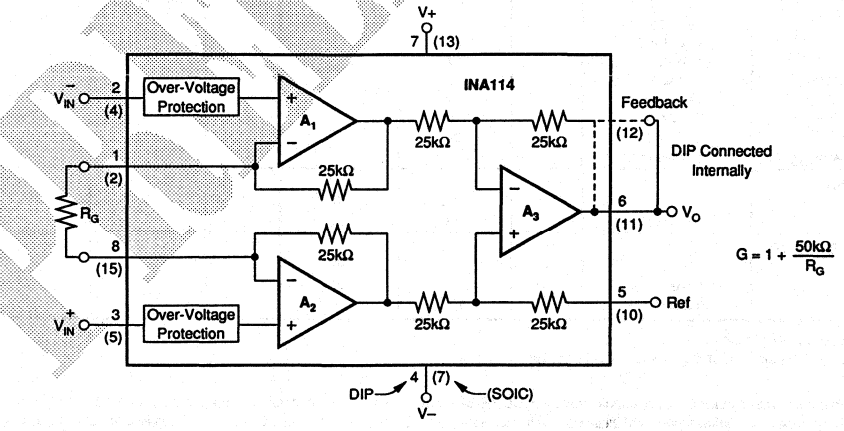
DESCRIPTION

The INA114 is a low cost, general purpose instrumentation amplifier offering excellent accuracy. Its versatile 3-op amp design and small size make it ideal for a wide range of applications.

A single external resistor sets any gain from 1 to 10,000. Internal input protection can withstand up to ±40V without damage.

The INA114 is laser trimmed for very low offset voltage (50µV), drift (0.25µV/°C) and high common-mode rejection (115dB at G = 1000). It operates with power supplies as low as ±2.25V, allowing use in battery operated and single 5V supply systems. Quiescent current is 3mA maximum.

The INA114 is available in 8-pin plastic or ceramic DIPs, and SOL-16 surface-mount packages, specified for the –40°C to +85°C temperature range.



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PDS-1142

SPECIFICATIONS

ELECTRICAL

At T_A = +25°C, V_S = ±15V, R_L = 2kΩ unless otherwise noted.

PARAMETER	CONDITIONS	INA114BP/BG MIN	INA114BP/BG TYP	INA114BP/BG MAX	INA114AP/AG/AU MIN	INA114AP/AG/AU TYP	INA114AP/AG/AU MAX	UNITS
INPUT								
Offset Voltage, RTI								
Initial	T_A = +25°C		±10 + 30/G	±50 + 100/G		±25 + 30/G	±125 + 500/G	µV
vs Temperature	T_A = T_{MIN} to T_{MAX}		±0.1 + 5/G	±0.25 + 10/G		±0.25 + 5/G	±1 + 100/G	µV/°C
Long-Term Stability			±1 + 20/G			*		µV/mo
vs Power Supply	V_S = ±2.25V to ±18V		1 + 10/G	3 + 10/G		*	*	µV/V
Impedance, Differential			10^9 || 3			*		Ω || pF
Common-Mode			10^{10} || 3			*		Ω || pF
Input Common-Mode Range		±11	±13.5		*	*		V
Safe Input Voltage			±40			*		V
Common-Mode Rejection	V_{CM} = ±10V, ΔR_S = 1kΩ							
	G = 1	80	92		*	90		dB
	G = 10	96	106		90	106		dB
	G = 100	110	115		106	110		dB
	G = 1000	115	120		106	110		dB
BIAS CURRENT			±0.3	±2		*	±5	nA
vs Temperature			±15			*		pA/°C
OFFSET CURRENT			±0.5	±2		*	±5	nA
vs Temperature			±15			*		pA/°C
NOISE VOLTAGE, RTI	G = 1000, R_S = 0Ω							
f = 10Hz			18			*		nV/√Hz
f = 100Hz			15			*		nV/√Hz
f = 1kHz			12			*		nV/√Hz
f = 10kHz			10			*		nV/√Hz
f_B = 0.1Hz to 10Hz			0.7			*		µVp-p
Noise Current								
f=10Hz			1			*		pA/√Hz
f=1kHz			0.5			*		pA/√Hz
f_B = 0.1Hz to 100Hz			40			*		pAp-p
GAIN								
Gain Equation			1 + (50kΩ/R_G)			*		V/V
Range of Gain		1		10000	*		*	V/V
Gain Error	G = 1		±0.01	±0.05		*	*	%
	G = 10		±0.25	±0.4		*	±0.5	%
	G = 100		±0.35	±0.5		*	±0.7	%
	G = 1000		±1.25	±1.75		*	±2	%
Gain vs Temperature	G = 1		±5	±10		*	±20	ppm/°C
50kΩ Resistance[1]			±25	±100		*	*	ppm/°C
Nonlinearity	G = 1		±0.0005	±0.001		*	±0.002	% of FSR
	G = 10		±0.001	±0.002		*	±0.004	% of FSR
	G = 100		±0.001	±0.002		*	±0.004	% of FSR
	G = 1000		±0.005	±0.01		*	±0.02	% of FSR
OUTPUT								
Voltage	I_O = 5mA, T_{MIN} to T_{MAX}	±13.5	±13.7	*	*			V
	V_S = ±11.4V, R_L = 2kΩ	±10			*			V
	V_S = ±2.25V, R_L = 2kΩ	±1			*			V
Load Capacitance Stability			1000			*		pF
Short Circuit Current			+20/–12			*		mA
FREQUENCY RESPONSE								
Bandwidth, –3dB	G = 1		1			*		MHz
	G = 10		100			*		kHz
	G = 100		10			*		kHz
	G = 1000		1			*		kHz
Slew Rate	V_O = ±10V, G = 10 to 200	0.3	0.5		*	*		V/µs
Settling Time, 0.01%	G = 1		22			*		µs
	G = 10		25			*		µs
	G = 100		145			*		µs
	G = 1000		1500			*		µs
Overload Recovery	50% Overdrive		20			*		µs
POWER SUPPLY								
Voltage Range		±2.25	±15	±18	*	*	*	V
Current	V_{IN} = 0V		±2.2	±3		*	*	mA
TEMPERATURE RANGE								
Specification		–40		85	*		*	°C
Operating	Plastic P, U	–40		125	*		*	°C
	Ceramic G	–55		125	*		*	°C
θ_{JA}	Plastic P, U		80			*		°C/W
	Ceramic, G		90		*			°C/W

* Specification same as INA114BG.

NOTE: (1) Temperature coefficient of the "50kΩ" term in the gain equation.

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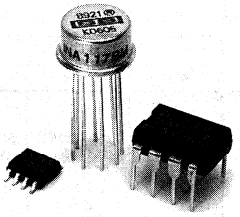


INA117

AVAILABLE IN DIE

High Common-Mode Voltage DIFFERENCE AMPLIFIER

FEATURES

- **COMMON-MODE INPUT RANGE: ±200V (V_S = ±15V)**
- **PROTECTED INPUTS: ±500V Common-Mode ±500V Differential**
- **UNITY GAIN: 0.02% Gain Error max**
- **NONLINEARITY: 0.001% max**
- **CMRR: 86dB min**

APPLICATIONS

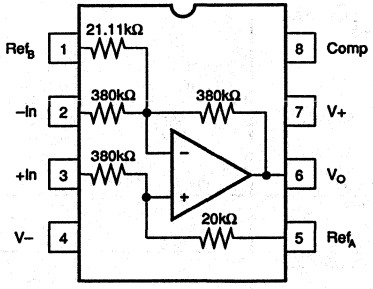
- **CURRENT MONITOR**
- **BATTERY CELL-VOLTAGE MONITOR**
- **GROUND BREAKER**
- **INPUT PROTECTION**
- **SIGNAL ACQUISITION IN NOISY ENVIRONMENTS**
- **FACTORY AUTOMATION**

DESCRIPTION

The INA117 is a precision unity-gain difference amplifier with very high common-mode input voltage range. It is a single monolithic IC consisting of a precision op amp and integrated thin-film resistor network. It can accurately measure small differential voltages in the presence of common-mode signals up to ±200V. The INA117 inputs are protected from momentary common-mode or differential overloads up to ±500V.

In many applications, where galvanic isolation is not essential, the INA117 can replace isolation amplifiers. This can eliminate costly isolated input-side power supplies and their associated ripple, noise and quiescent current. The INA117's 0.001% nonlinearity and 200kHz bandwidth are superior to those of conventional isolation amplifiers.

The INA117 is available in 8-pin plastic mini-DIP and SO-8 surface-mount packages, specified for the 0°C to +70°C temperature range. The metal TO-99 models are available specified for the –25°C to +85°C and –55°C to +125°C temperature range.



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PDS-748E

SPECIFICATIONS

ELECTRICAL

At T_A = +25°C, V_S = ±15V unless otherwise noted.

PARAMETER	CONDITIONS	INA117AM, SM			INA117BM			INA117P, KU			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
GAIN											
Initial [1]			1			•			•		V/V
Error			0.01	0.05		•	0.02		•	•	%
vs Temperature			2	10			•		•		ppm/°C
Nonlinearity [2]			0.0002	0.001		•	•		•	•	%
OUTPUT											
Rated Voltage	I_O = +20mA, –5mA	10	12		•	•		•	•		V
Rated Current	V_O = 10V	+20, –5			•			•			mA
Impedance			0.01			•			•		Ω
Current Limit	To Common		+49, –13			•			•		mA
Capacitive Load	Stable Operation		1000			•			•		pF
INPUT											
Impedance	Differential		800			•			•		kΩ
	Common-Mode		400			•			•		kΩ
Voltage Range	Differential	±10				•			•		V
	Common-Mode, Continuous	±200			•			•			V
Common-Mode Rejection [3]											
DC		70	80		86	94		•	•		dB
AC, 60Hz	V_{CM} = 400Vp-p	66	80		66	94		•	•		dB
vs Temperature, DC	$T_A = T_{MIN}$ to T_{MAX}										
AM, BM, P, KU		66	75		80	90			•		dB
SM		60	75								dB
OFFSET VOLTAGE	RTO [4]										
Initial			120	1000		•	1000		•	•	µV
KU Grade (SO-8 Package)									600	2000	µV
vs Temperature	$T_A = T_{MIN}$ to T_{MAX}		8.5	40		•	20		•		µV/°C
vs Supply	V_S = ±5V to ±18V	74	90		80	•		•	•		dB
vs Time			200			•			•		µV/mo
OUTPUT NOISE VOLTAGE	RTO [5]										
f_B = 0.01Hz to 10Hz			25			•			•		µVp-p
f_B = 10kHz			550			•			•		nV/√Hz
DYNAMIC RESPONSE											
Gain Bandwidth, –3dB			200			•			•		kHz
Full Power Bandwidth	V_O = 20Vp-p	30			•			•			kHz
Slew Rate		2	2.6		•	•		•	•		V/µs
Settling Time: 0.1%	V_O = 10V Step		6.5			•			•		µs
0.01%	V_O = 10V Step		10			•			•		µs
0.01%	V_{CM} = 10V Step, V_{DIFF} = 0V		4.5			•			•		µs
POWER SUPPLY											
Rated			±15			•			•		V
Voltage Range	Derated Performance	±5		±18	•		•	•		•	V
Quiescent Current	V_O = 0V		1.5	2		•	•		•	•	mA
TEMPERATURE RANGE											
Specification: AM, BM, P, KU		–25		+85	•		•	0		+70	°C
SM		–55		+125							°C
Operation		–55		+125	•		•	–25		+85	°C
Storage		–65		+150	•		•	–40		+85	°C

*Specification same as for INA117AM.

NOTES: (1) Connected as difference amplifier (see Figure 1). (2) Nonlinearity is the maximum peak deviation from the best-fit straight line as a percent of full-scale peak-to-peak output. (3) With zero source impedance (see discussion of common-mode rejection in Application Information section). (4) Includes effects of amplifier's input bias and offset currents. (5) Includes effects of amplifier's input current noise and thermal noise contribution of resistor network.

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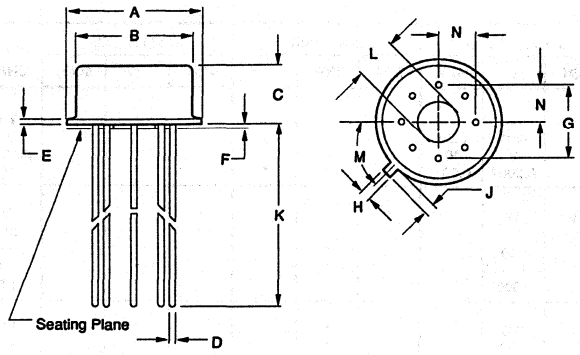
MECHANICAL

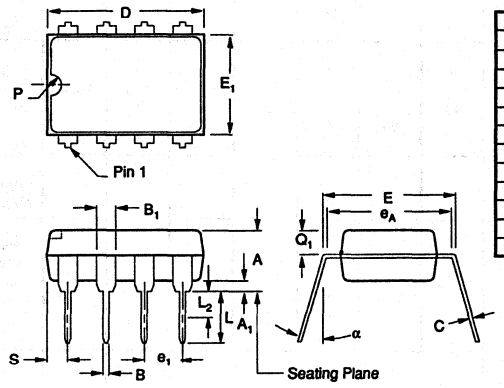
M Package — Metal TO-99



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.335	.370	8.51	9.40
B	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.200 BASIC		5.08 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500	—	12.7	—
L	.110	.160	2.79	4.06
M	45° BASIC		45° BASIC	
N	.095	.105	2.41	2.67

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Tab is pin 8.

P Package — 8-Pin Plastic DIP

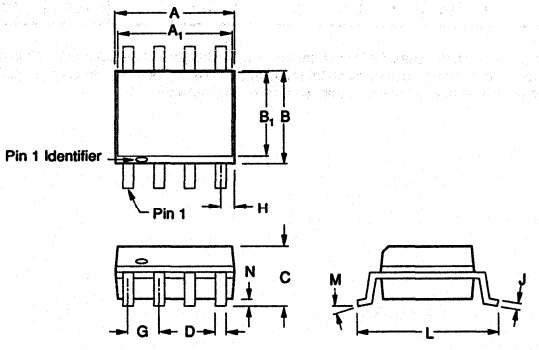


DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.155	.200	3.94	5.08
A_1	.020	.050	0.51	1.27
B	.014	.020	0.36	0.51
B_1	.045	.065	1.14	1.65
C	.008	.012	0.20	0.30
D (1)	.370	.400	9.40	10.16
E	.300	.325	7.62	8.26
E_1	.240	.260	6.10	6.60
e_1	.100 BASIC		2.54 BASIC	
e_A	.300 BASIC		7.62 BASIC	
L	.125	.150	3.18	3.81

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
L_2 (2)	0	.030	0.00	0.76
α	0°	15°	0°	15°
P	.015	.050	0.38	1.270
Q_1	.040	.075	1.02	1.91
S (1)	.015	.050	0.38	1.27

(1) Not JEDEC Std.
(2) e_1 and e_A applies in zone L_2 when unit installed.
NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

U Package — 8-Pin SOIC



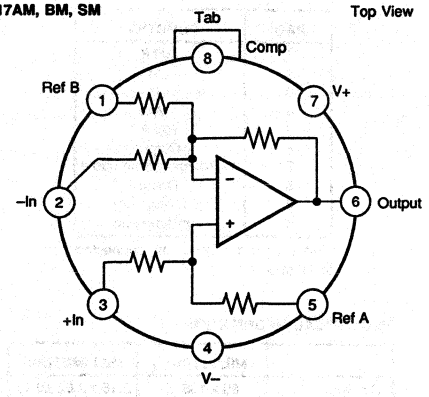
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.185	.201	4.70	5.11
A_1	.178	.201	4.52	5.11
B	.146	.162	3.71	4.11
B_1	.130	.149	3.30	3.78
C	.054	.145	1.37	3.69
D	.015	.019	0.38	0.48
G	.050 BASIC		1.27 BASIC	
H	.018	.026	0.46	0.66
J	.008	.012	0.20	0.30
L	.220	.252	5.59	6.40
M	0°	10°	0°	10°
N	.000	.012	0.00	0.30

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

PIN CONFIGURATION

Metal TO-99
INA117AM, BM, SM

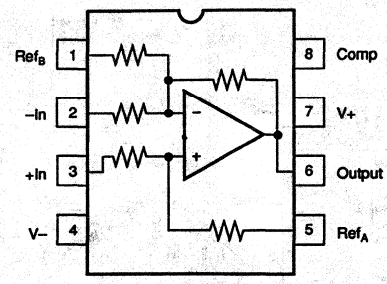
Top View



Case internally connected to V–. Make no connection.

Plastic DIP and SOIC
INA117P, KU

Top View



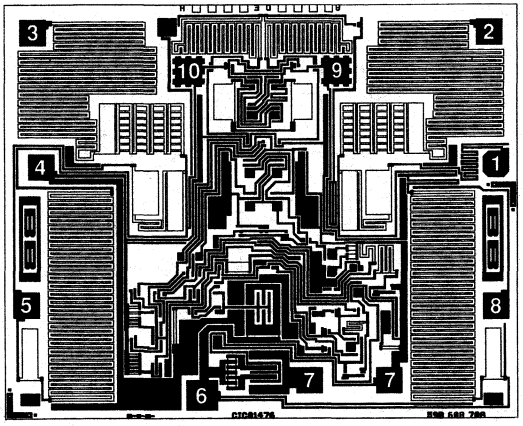
ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±22V
Input Voltage Range, Continuous	±200V
Common-Mode and Differential, 10s	±500V
Operating Temperature	
M Metal TO-99	–55 to +125°C
P Plastic DIP and U SO-8	–40 to +85°C
Storage Temperature	
M Package	–65 to +150°C
P Plastic DIP and U SO-8	–40 to +85°C
Lead Temperature (soldering, 10s)	+300°C
Output Short Circuit to Common	Continuous

ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE
INA117P	Plastic DIP	0°C to +70°C
INA117KU	SO-8 Surface-Mount	0°C to +70°C
INA117AM	TO-99 Metal	–25°C to +85°C
INA117BM	TO-99 Metal	–25°C to +85°C
INA117SM	TO-99 Metal	–55°C to +125°C

DICE INFORMATION



INA117 DIE TOPOGRAPHY

PAD	FUNCTION
1	Ref B
2	–In
3	+In
4	V–
5	Ref A
6	Output
7	V+ (connect both pads)
8	Comp
9	(Op Amp –In)
10	(Op Amp +In)

Substrate Bias: Electrically connected to –V supply.

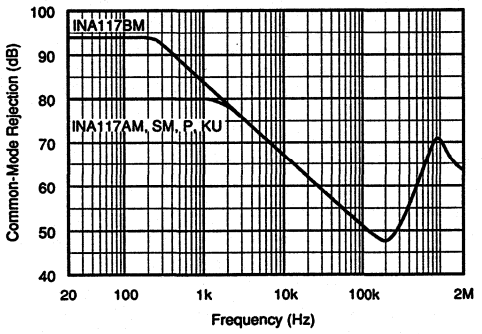
MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	85 x 103 ±5	2.16 x 2.62 ±0.13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.01 x 0.01
Backing	Gold	

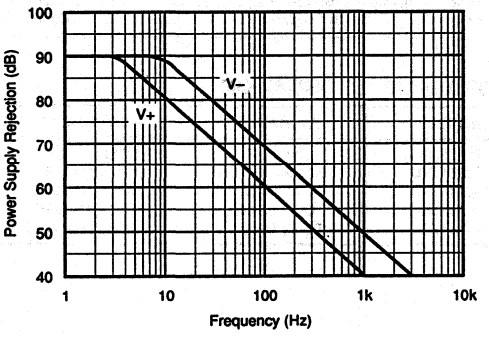
TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_S = ±15V, unless otherwise noted.

COMMON-MODE REJECTION vs FREQUENCY



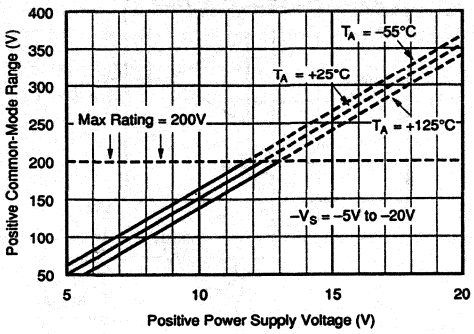
POWER SUPPLY REJECTION vs FREQUENCY



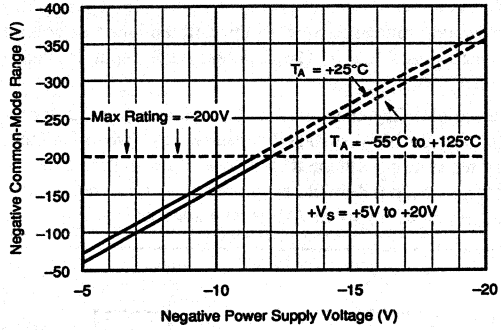
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_S = ±15V unless otherwise noted.

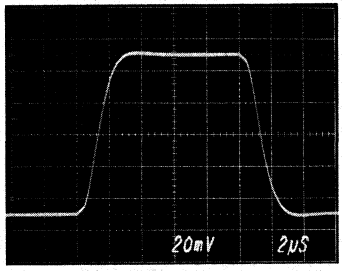
POSITIVE COMMON-MODE VOLTAGE RANGE vs POSITIVE POWER SUPPLY VOLTAGE



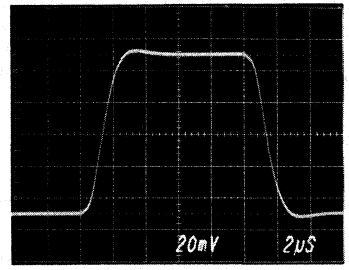
NEGATIVE COMMON-MODE VOLTAGE RANGE vs NEGATIVE POWER SUPPLY VOLTAGE



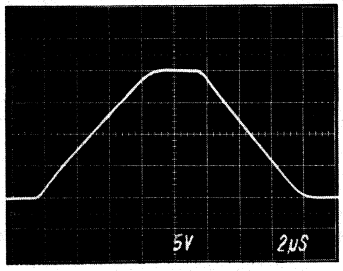
SMALL SIGNAL STEP RESPONSE
C_L = 0



SMALL SIGNAL STEP RESPONSE
C_L = 1000pF



LARGE SIGNAL STEP RESPONSE



APPLICATION INFORMATION

Figure 1 shows the basic connections required for operation.

Applications with noisy or high impedance power supply lines may require decoupling capacitors close to the device pins.

The output voltage is equal to the differential input voltage between pins 2 and 3. The common mode input voltage is rejected.

Internal circuitry connected to the compensation pin 8 cancels the parasitic distributed capacitance between the feedback resistor, R_2, and the IC substrate. For specified dynamic performance, pin 8 should be grounded or connected through a 0.1µF capacitor to an AC ground such as V+.

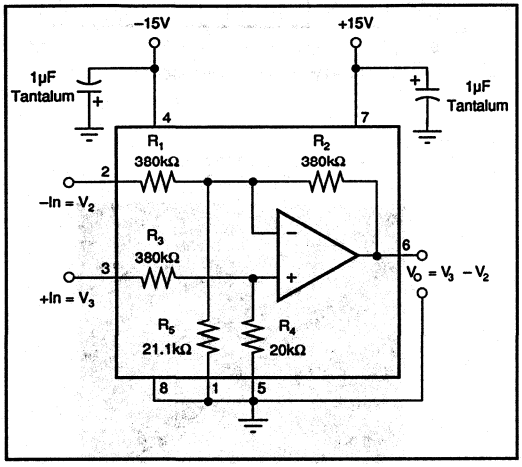


FIGURE 1. Basic Power and Signal Connections.

COMMON-MODE REJECTION

Common-mode rejection (CMR) of the INA117 is dependent on the input resistor network, which is laser-trimmed for accurate ratio matching. To maintain high CMR, it is important to have low source impedances driving the two inputs. A 75Ω resistance in series with pin 2 or 3 will decrease CMR from 86dB to 72dB.

Resistance in series with the reference pins will also degrade CMR. A 4Ω resistance in series with pin 1 or 5 will decrease CMRR from 86dB to 72dB.

Most applications do not require trimming. Figures 2 and 3 show optional circuits that may be used for trimming offset voltage and common-mode rejection.

TRANSFER FUNCTION

Most applications use the INA117 as a simple unity-gain difference amplifier. The transfer function is:

$$V_O = V_3 - V_2$$

V_3 and V_2 are the voltages at pins 3 and 2.

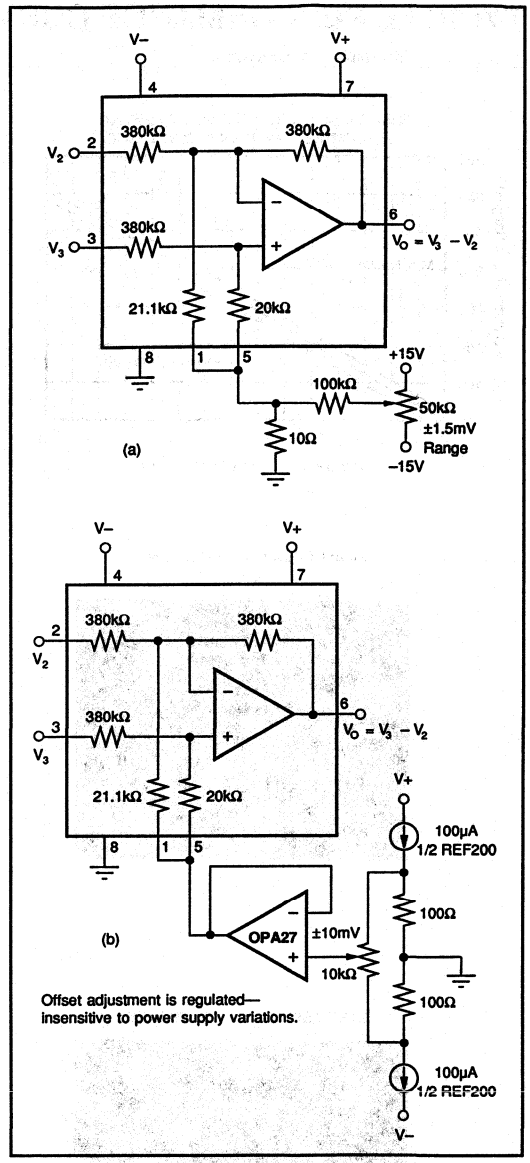


FIGURE 2. Offset Voltage Trim Circuits.

Some applications, however, apply voltages to the reference terminals (pins 1 and 5). A more complete transfer function is:

$$V_O = V_3 - V_2 + 19 \cdot V_5 - 18 \cdot V_1$$

V_5 and V_1 are the voltages at pins 5 and 1.

MEASURING CURRENT

The INA117 can be used to measure a current by sensing the voltage drop across a series resistor, R_S. Figure 4 shows the INA117 used to measure the supply currents of a device under test. The circuit in Figure 5 measures the output current of a power supply. If the power supply has a sense connection, it can be connected to the output side of R_S to eliminate the voltage-drop error. Another common application is current-to-voltage conversion as shown in Figure 6.

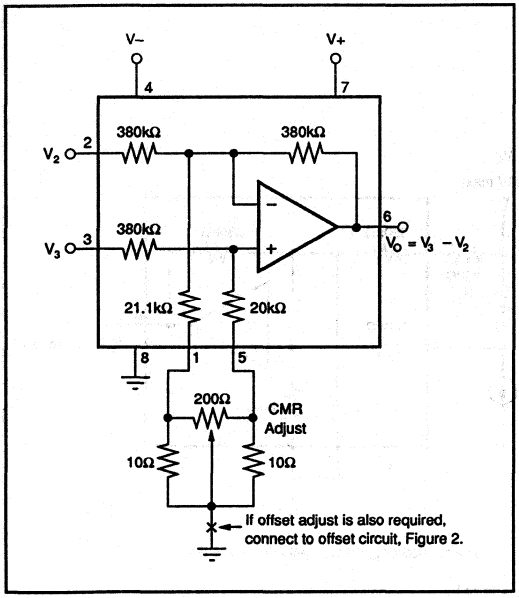


FIGURE 3. CMR Trim Circuit.

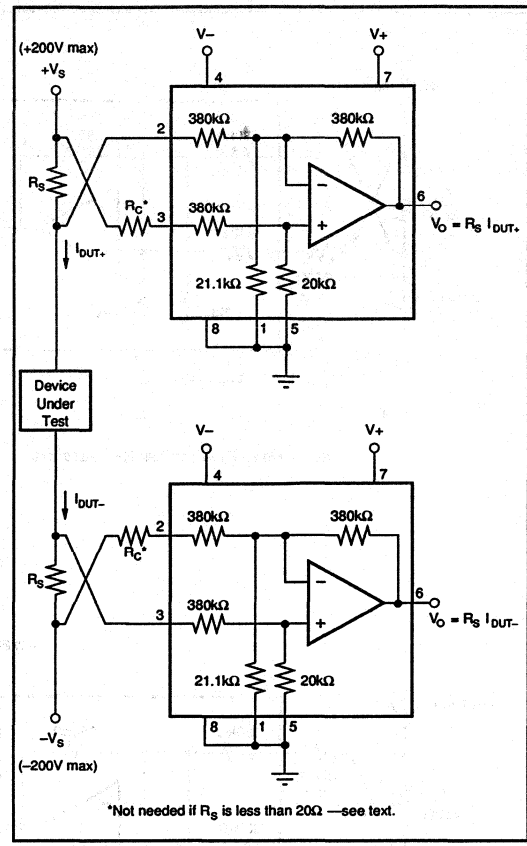


FIGURE 4. Measuring Supply Currents of Device Under Test.

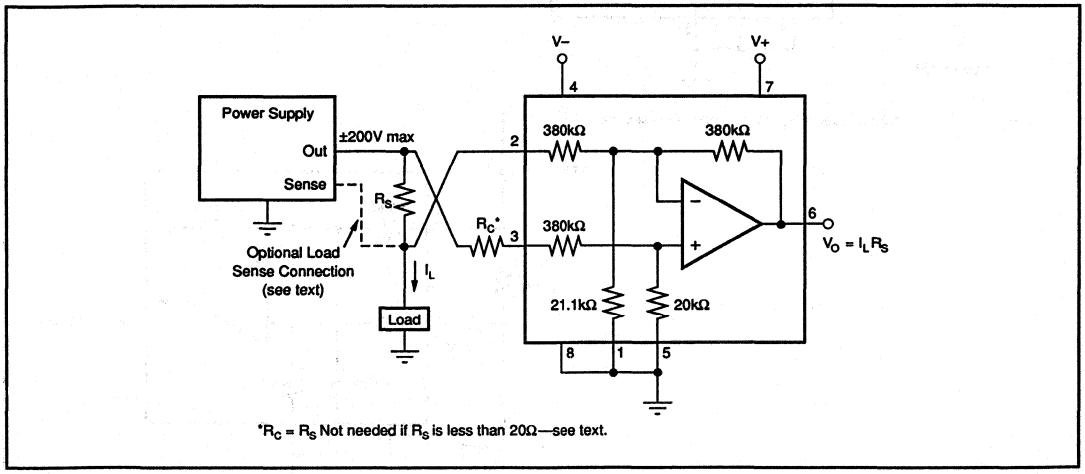


FIGURE 5. Measuring Power Supply Output Current.

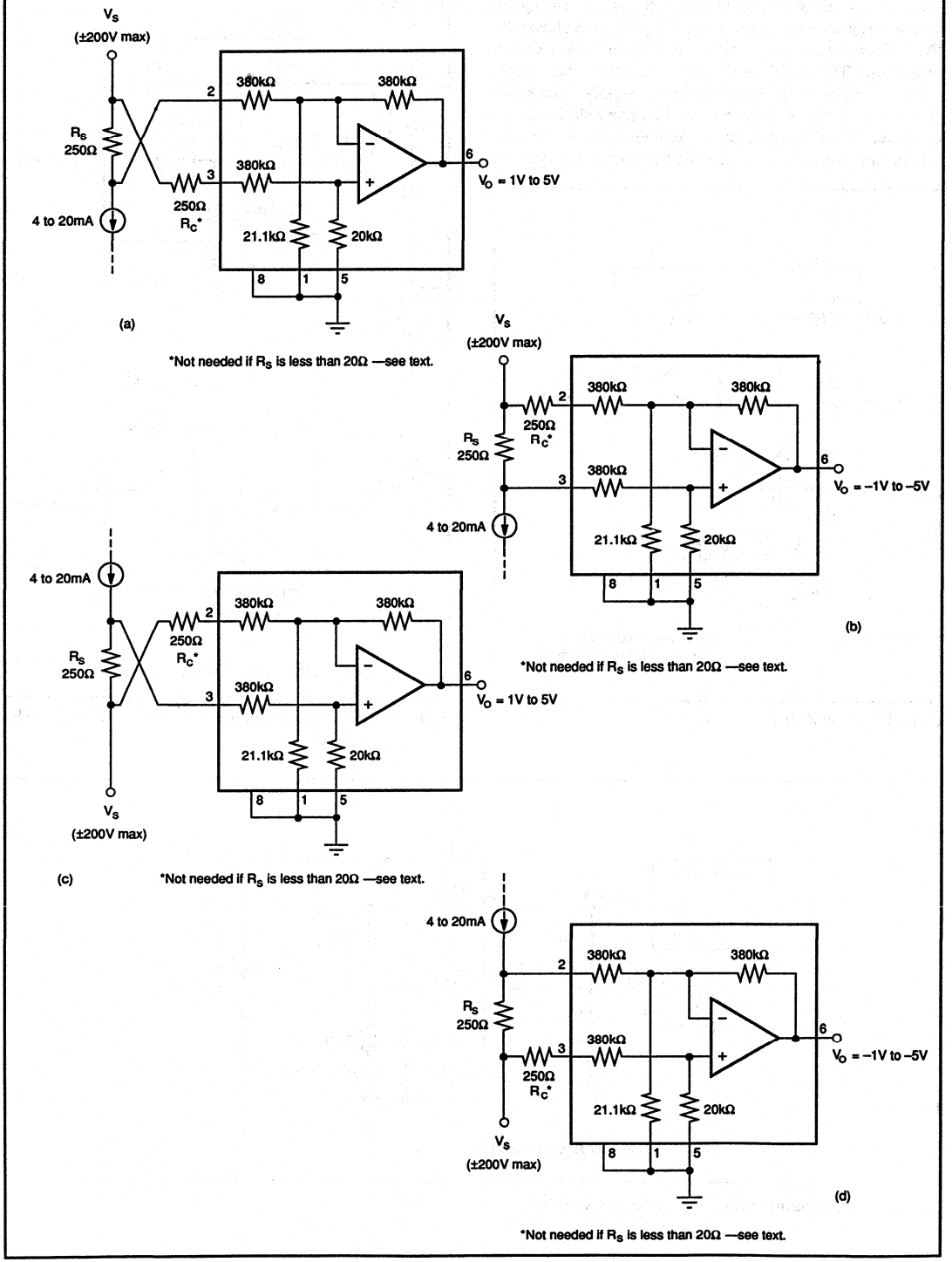


FIGURE 6. Current to Voltage Converter.

In all cases, the sense resistor imbalances the input resistor matching of the INA117, degrading its CMR. Also, the input impedance of the INA117 loads R_S, causing gain error in the voltage-to-current conversion. Both of these errors can be easily corrected.

The CMR error can be corrected with the addition of a compensation resistor, R_C, equal in value to R_S as shown in Figures 4, 5, and 6. If R_S is less than 20Ω, the degradation in CMR is negligible and R_C can be omitted. If R_S is larger than approximately 2kΩ, trimming R_C may be required to achieve greater than 86dB CMR. This is because the actual INA117 input impedances have 1% typical mismatch.

If R_S is more than approximately 100Ω, the gain error will be greater than the 0.02% specification of the INA117. This gain error can be corrected by slightly increasing the value of R_S. The corrected value, R_S', can be calculated by—

$$R_S' = \frac{R_S \cdot 380k\Omega}{380k\Omega - R_S}$$

Example: For a 1V/mA transfer function, the nominal, uncorrected value for R_S would be 1kΩ. A slightly larger value, $R_S' = 1002.6\Omega$, compensates for the gain error due to loading.

The 380kΩ term in the equation for R_S' has a tolerance of ±25%, so sense resistors above approximately 400Ω may require trimming to achieve gain accuracy better than 0.02%.

Of course, if a buffer amplifier is added as shown in Figure 7, both inputs see a low source impedance, and the sense resistor is not loaded. As a result, there is no gain error or CMR degradation. The buffer amplifier can operate as a unity gain buffer or as an amplifier with noninverting gain. Gain added ahead of the INA117 improves both CMR and signal-to-noise. Added gain also allows a lower voltage drop across the sense resistor. The OPA1013 is a good choice for the buffer amplifier since both its input and output can swing close to its negative power supply.

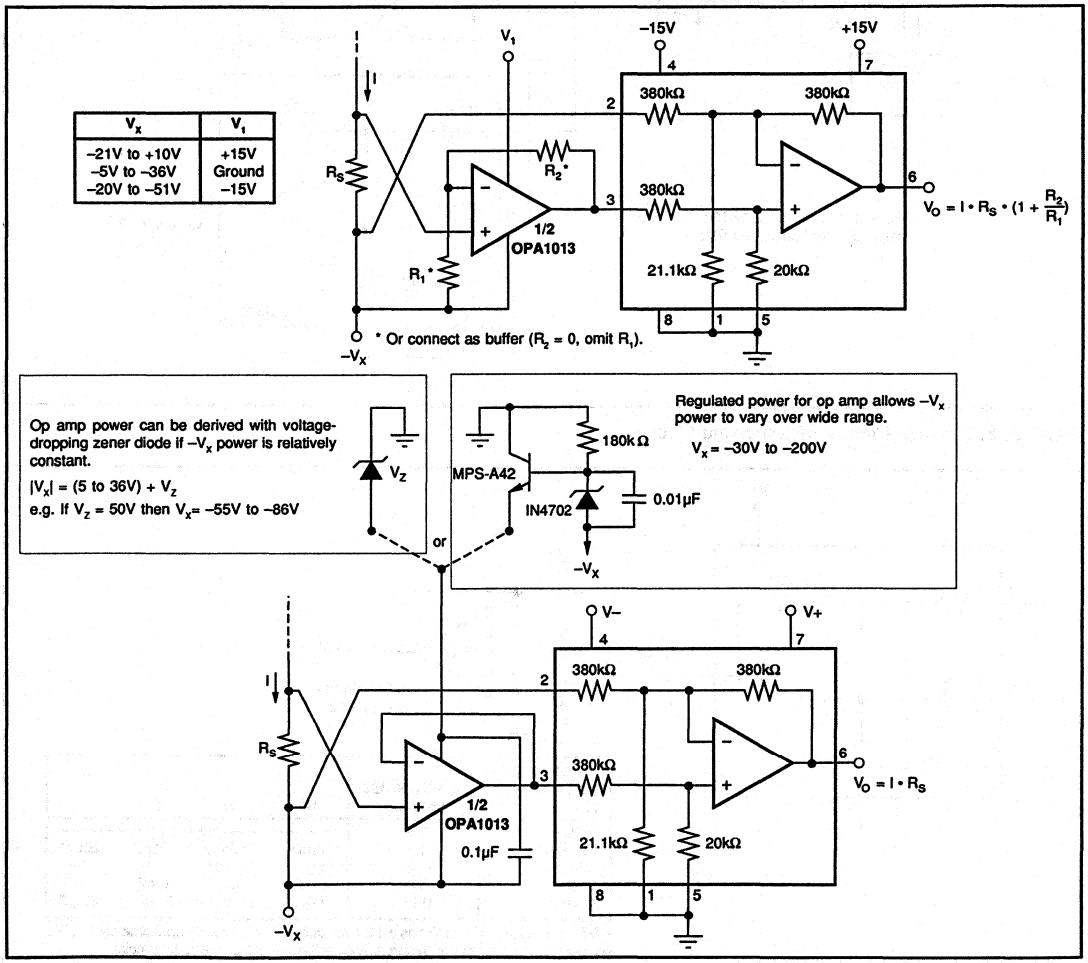


FIGURE 7. Current Sensing with Input Buffer.

Figure 8 shows very high input impedance buffer used to measure low leakage currents. Here, the buffer op amp is powered with an isolated, split-voltage power supply. Using an isolated power supply allows full ±200V common-mode input range.

NOISE PERFORMANCE

The noise performance of the INA117 is dominated by the internal resistor network. The thermal or Johnson noise of these resistors produces approximately 550nV/$\sqrt{Hz}$ noise. The internal op amp contributes virtually no excess noise at frequencies above 100Hz.

Many applications may be satisfied with less than the full 200kHz bandwidth of the INA117. In these cases, the noise can be reduced with a low-pass filter on the output. The two-pole filter shown in Figure 9 limits bandwidth to 1kHz and reduces noise by more than 15:1. Since the INA117 has a 1/f noise corner frequency of approximately 100Hz, a cutoff frequency below 100Hz will not further reduce noise.

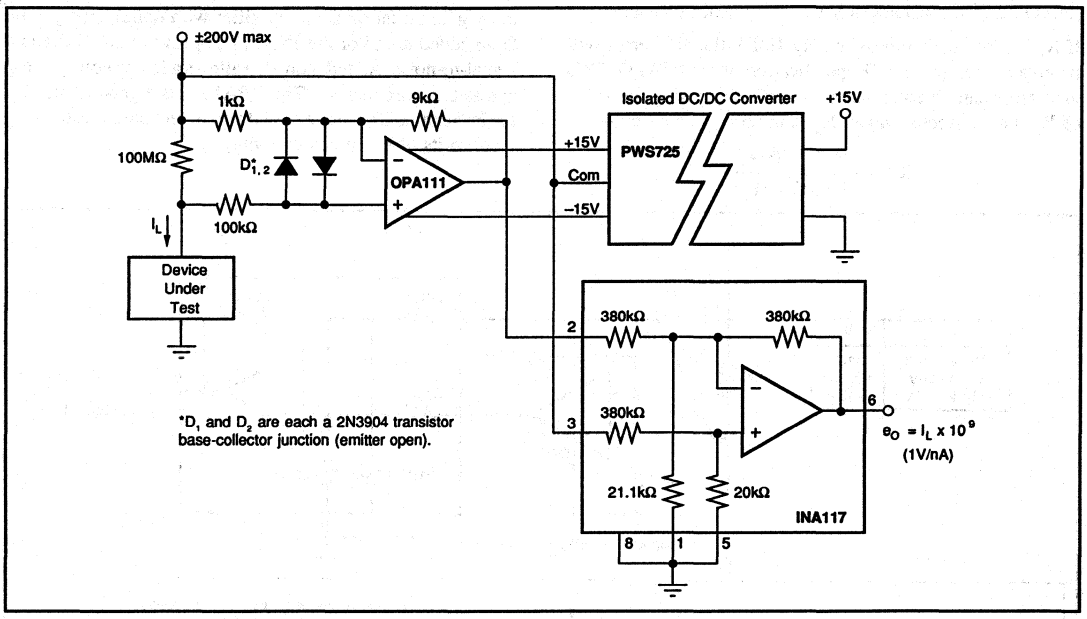
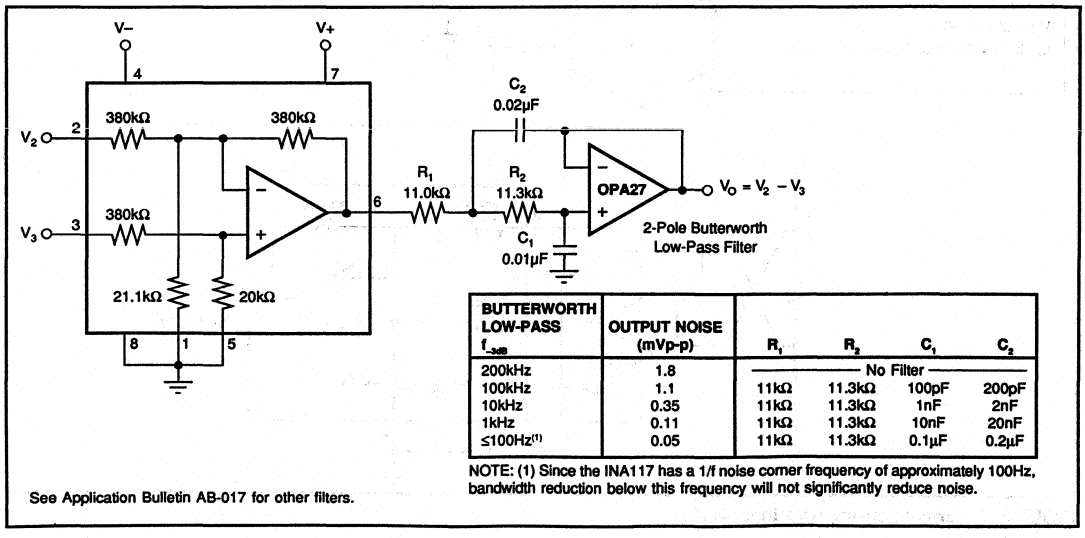


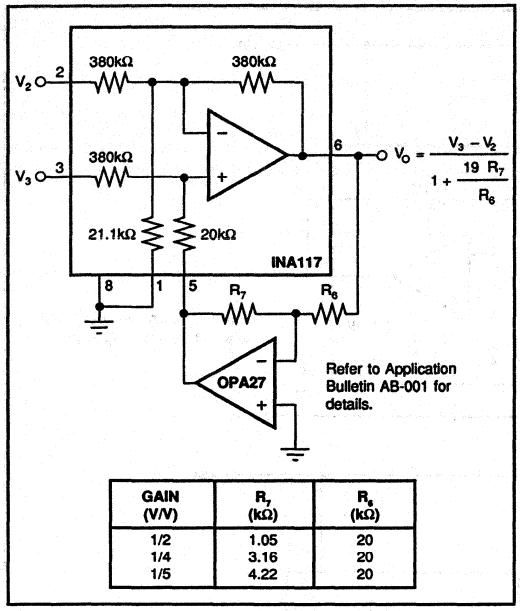
FIGURE 8. Leakage Current Measurement Circuit.



BUTTERWORTH LOW-PASS f_{-3dB}	OUTPUT NOISE (mVp-p)	R_1	R_2	C_1	C_2
200kHz	1.8	No Filter			
100kHz	1.1	11kΩ	11.3kΩ	100pF	200pF
10kHz	0.35	11kΩ	11.3kΩ	1nF	2nF
1kHz	0.11	11kΩ	11.3kΩ	10nF	20nF
≤100Hz(1)	0.05	11kΩ	11.3kΩ	0.1µF	0.2µF

NOTE: (1) Since the INA117 has a 1/f noise corner frequency of approximately 100Hz, bandwidth reduction below this frequency will not significantly reduce noise.

FIGURE 9. Output Filter for Noise Reduction.



GAIN (V/V)	R_7 (kΩ)	R_6 (kΩ)
1/2	1.05	20
1/4	3.16	20
1/5	4.22	20

FIGURE 10. Reducing Differential Gain.

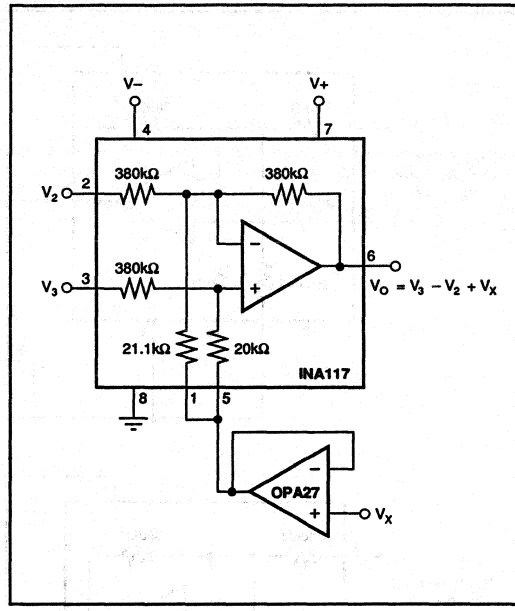


FIGURE 11. Summing V_X in Output.

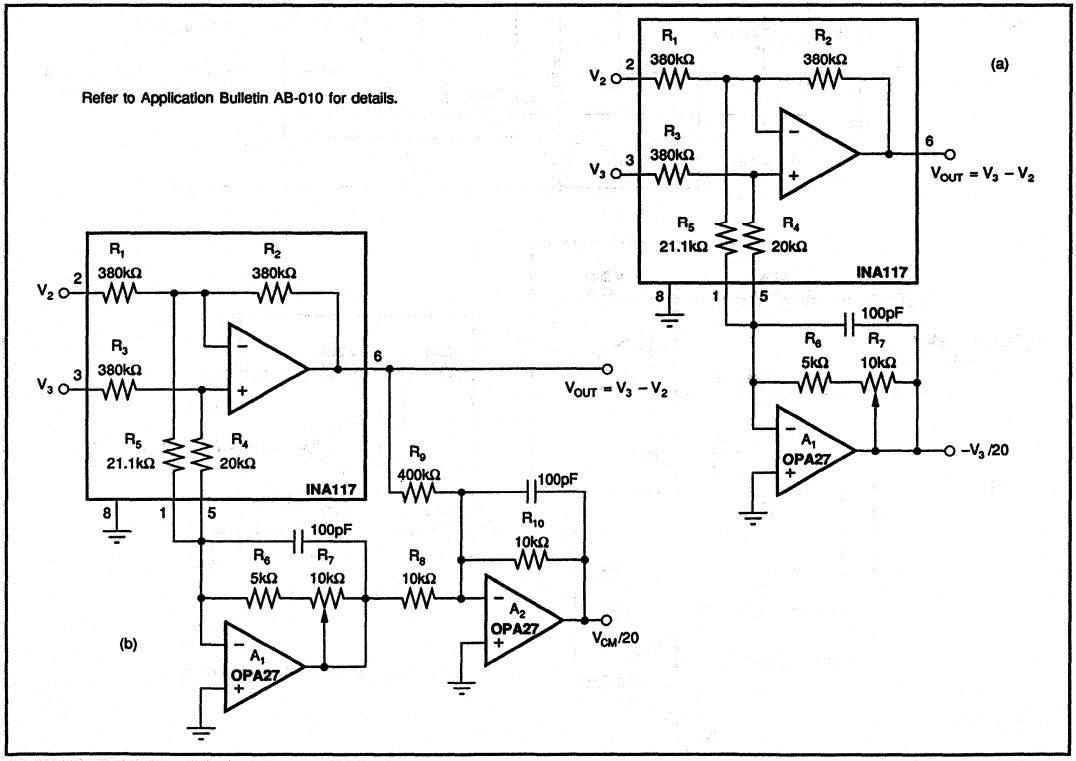


FIGURE 12. Common-Mode Voltage Monitoring.

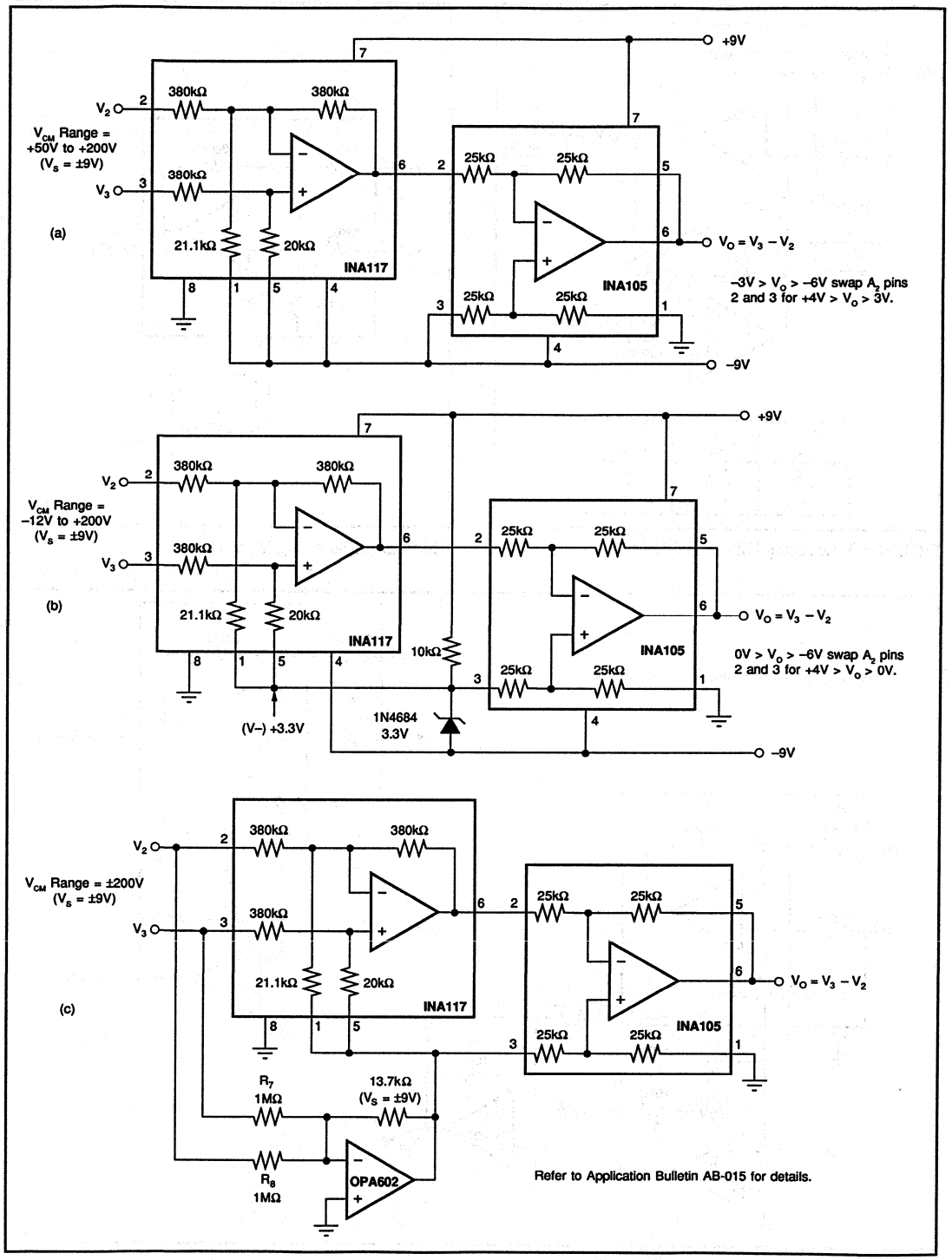


FIGURE 13. Offsetting or Boosting Common-Mode Voltage Range for Reduced Power Supply Voltage Operation.

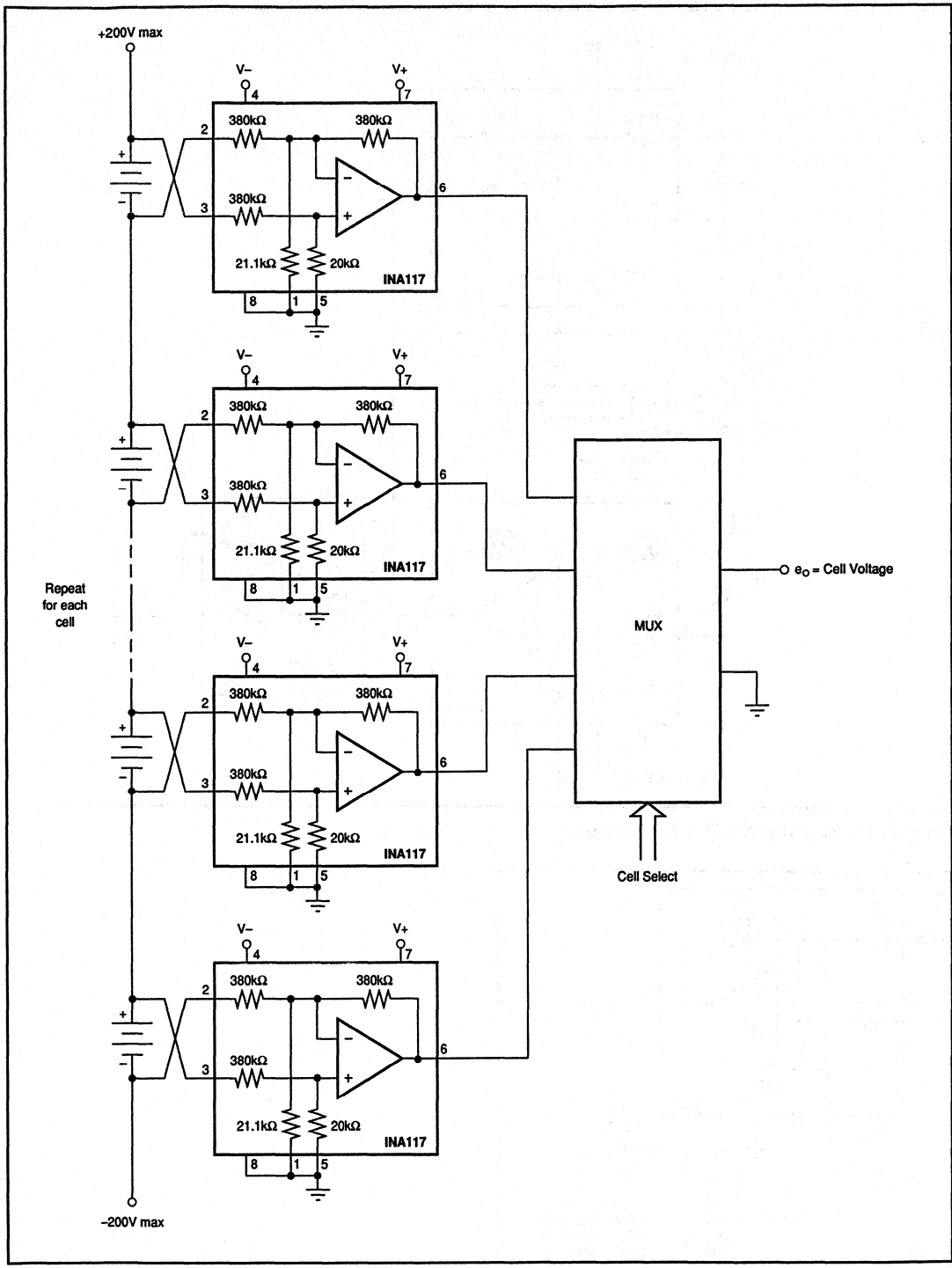


FIGURE 14. Battery Cell Voltage Monitor.

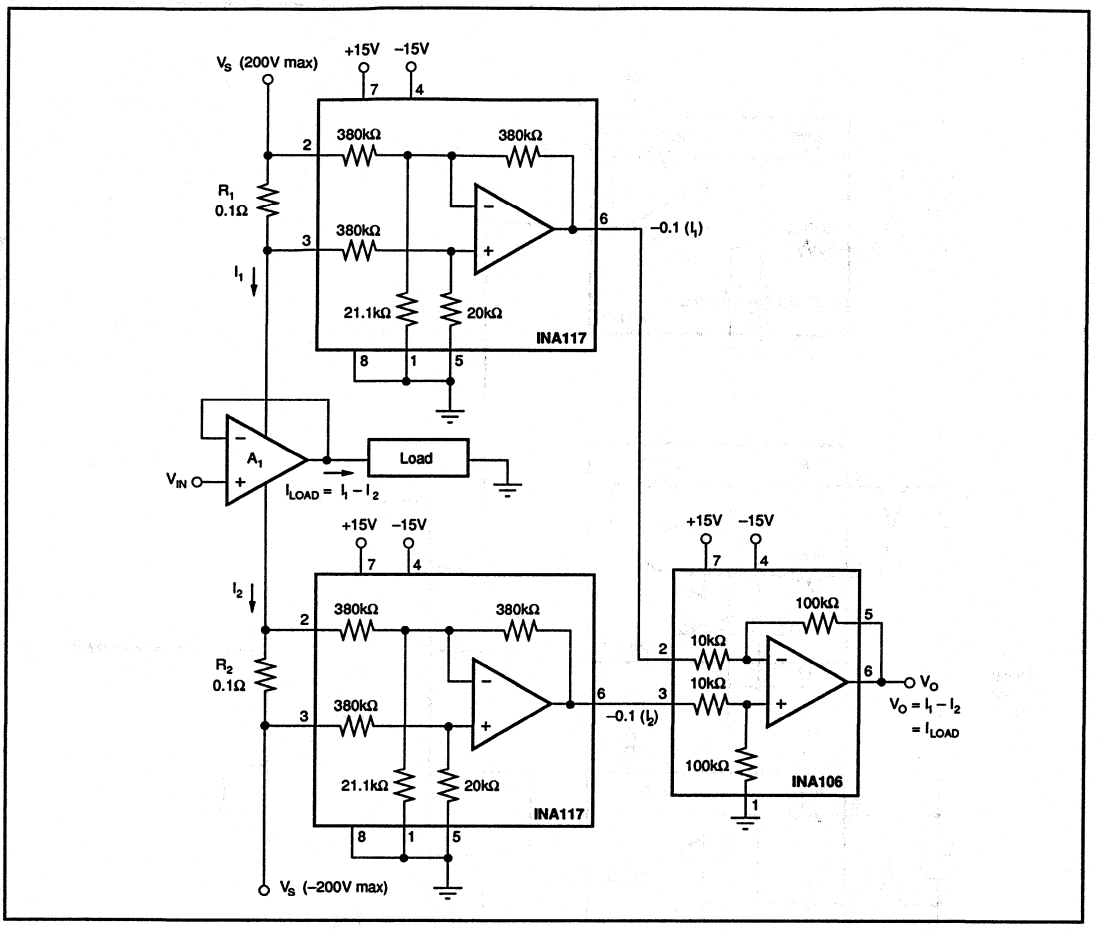


FIGURE 15. Measuring Amplifier Load Current.

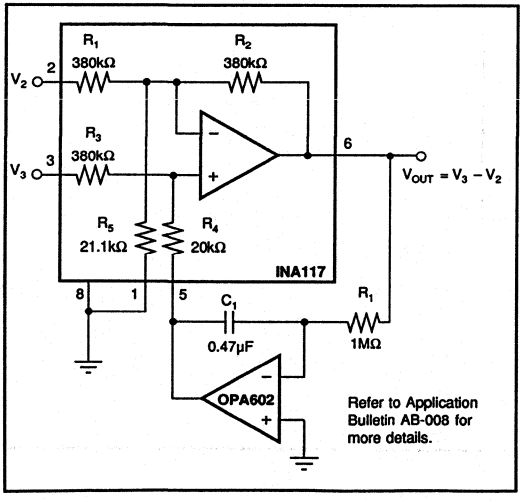
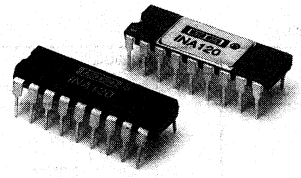


FIGURE 16. AC-Coupled INA117.

BURR-BROWN®



INA120

Precision INSTRUMENTATION AMPLIFIER

FEATURES

- LOW OFFSET VOLTAGE: 25µV max
- LOW OFFSET VOLTAGE DRIFT: 0.25µV/°C max
- PIN-STRAPPED GAINS: 1, 10, 100, 1000
- LOW GAIN DRIFT: 30ppm/°C max at G = 100
- HIGH COMMON-MODE REJECTION: 106dB at 60Hz, G = 100

APPLICATIONS

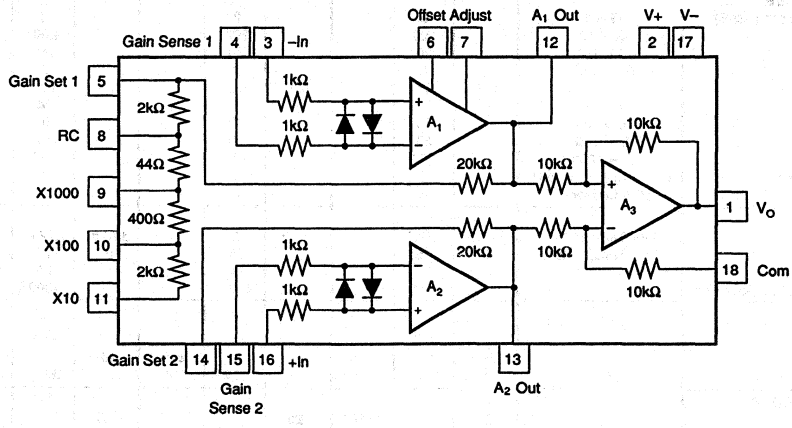
- BRIDGE AMPLIFIER
- THERMOCOUPLE AMPLIFIER
- RTD SENSOR AMPLIFIER
- MEDICAL INSTRUMENTATION
- DATA ACQUISITION SYSTEM
- SWITCHED-GAIN AMPLIFIER

DESCRIPTION

The INA120 is a precision instrumentation amplifier ideal for accurate signal acquisition. It combines precision, protected-input operational amplifiers, laser-trimmed gain-setting resistors, and a high common-mode rejection difference amplifier on a single chip.

Simple pin-strapped connections set precise gains of 1, 10, 100 or 1000. External resistors can be used to set any gain from one to 5000. Gains can be digitally selected with an external multiplexer. Gain-sense connections on the INA120 maintain accuracy when using multiplexer or gain-switching circuitry. Low power dissipation and careful on-chip thermal management reduce warm-up drift and assure excellent long-term stability.

The INA120 is available in both plastic and ceramic 18-pin DIP packages, specified for the industrial temperature range.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

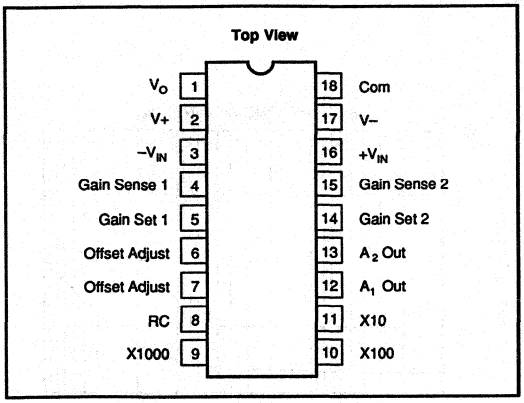
ELECTRICAL

At T_A = +25°C and V_S = ±15V unless otherwise specified.

PARAMETER	CONDITIONS	INA120CG			INA120BG/BP			INA120AP			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
GAIN											
Range of Gain		1		1000	1		1000	1		1000	V/V
Gain Equation			$1 + (2R_F/R_G)$			$1 + (2R_F/R_G)$			$1 + (2R_F/R_G)$		V/V
Gain Error	G = 1		0.01	0.05		0.01	0.05		0.02	0.1	%
	G = 10		0.05	0.1		0.05	0.2		0.1	0.2	%
	G = 100		0.1	0.2		0.1	0.3		0.2	0.5	%
	G = 1000		0.3	0.5		0.3	1		0.5	1	%
Gain Temp Coefficient	G = 1		4	10		4	20		6	20	ppm/°C
	G = 10		4	10		4	20		8	40	ppm/°C
	G = 100		6	30		6	40		10	60	ppm/°C
	G = 1000		22	50		22	50		40	100	ppm/°C
Nonlinearity	G = 1		0.001	0.005		0.001	0.01		0.001	0.01	% of FS
	G = 10		0.002	0.005		0.002	0.01		0.002	0.01	% of FS
	G = 100		0.004	0.01		0.004	0.02		0.004	0.02	% of FS
	G = 1000		0.008	0.05		0.008	0.1		0.008	0.1	% of FS
OFFSET VOLTAGE											
Initial Offset			(10+ 300/G)	(25+ 600/G)		(50+ 300/G)	(100+ 1000/G)		(50+ 600/G)	(200+ 2000/G)	µV
vs Temperature			(.25 + 10/G)			(1 + 20/G)			(2 + 20/G)		µV/°C
vs Power Supply	V_S = ±6V to ±18V		(1 + 20/G)	(10 + 150/G)		(1 + 20/G)	(20 + 250/G)		(1 + 20/G)	(40 + 300/G)	µV/V
INPUT BIAS CURRENT											
Initial Bias Current			±7	±20		±7	±20		±20	±50	nA
vs Temperature			±0.2			±0.2			±0.2		nA/°C
Initial Offset Current			±5	±10		±5	±20		±10	±50	nA
vs Temperature			±0.2			±0.2			±0.2		nA/°C
Impedance: Differential			10^{10} || 3			10^{10} || 3			10^{10} || 3		Ω || pF
Common-Mode			10^{10} || 3			10^{10} || 3			10^{10} || 3		Ω || pF
INPUT VOLTAGE RANGE											
Range, Linear Response		±10	±12.5		±10	±12.5		±10	±12.5		V
CMRR (DC, 1kΩ Source Imbalance)	G = 1	80	90		74	90		70	85		dB
	G = 10	96	106		90	106		86	95		dB
	G = 100	106	110		106	110		100	105		dB
	G = 1000	106	110		106	110		100	105		dB
NOISE											
Input Voltage Noise											
f_B = 0.1Hz to 10Hz	G = 1000		0.7			0.7			0.7		µV p-p
Density; f = 10Hz	G = 1000		14			14			14		nV/√Hz
f = 100Hz			11			11			11		nV/√Hz
f = 1000Hz			10			10			10		nV/√Hz
Input Current Noise											
f_B = 0.1Hz to 10Hz			50			50			50		pAp-p
Density; f = 10Hz			1.8			1.8			1.8		pA/√Hz
f = 1kHz			0.4			0.4			0.4		pA/√Hz
Output Voltage Noise											
f_B = 0.1Hz to 10Hz			8			8			8		µVp-p
DYNAMIC RESPONSE											
Small Signal Bandwidth (–3dB)	G = 1		2			2			2		MHz
	G = 10		200			200			200		kHz
	G = 100		20			20			20		kHz
	G = 1000		2			2			2		kHz
Slew Rate		0.4	0.6		0.4	0.6		0.4	0.6		V/µs
Settling Time to 0.01%	G = 1		24			24			24		µs
	G = 10		30			30			30		µs
	G = 100		50			50			50		µs
	G = 1000		200			200			200		µs
Full Power Bandwidth, G < 200	V_O = ±10V, R_L = 2kΩ		9			9			9		kHz
Overload Recovery	50% Overdrive		2			2			2		µs
OUTPUT											
Voltage, R_L = 2kΩ	Over Temperature	±10.5	±12.8		±10.5	±12.8		±10.5	±12.8		V
Current	Over Temperature	5	15		5	15		5	15		mA
Short-Circuit Current			24			24			24		mA
Capacitive Load, Stable Operation			4000			4000			4000		pF
POWER SUPPLY											
Rated Voltage			±15			±15			±15		V
Voltage Range		±6		±18	±6		±18	±6		±18	V
Supply Current	V_O = 0V		±2.7	±4		±2.7	±4		±2.7	±4	mA
TEMPERATURE RANGE											
Specification		–25		+85	–25		+85	–25		+85	°C
Operation BP,AP					–40		+85	–40		+85	°C
Operation CG,BG		–55		+125	–55		+125				°C
Storage		–65		+150	–65		+150	–65		+150	°C

See Absolute Maximum Table.

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18V
Input Voltage Range	(V+) +2 to (V–) –2V
Differential Input Voltage	Total V_S +4V
Operating Temperature	
Ceramic G Package	–65°C to +150°C
Plastic P Package	–40°C to +125°C
Storage Temperature	
Ceramic G Package	–65°C to +150°C
Plastic P Package	–40°C to +125°C
Junction Temperature	
Ceramic G Package	+175°C
Plastic P Package	+125°C
Lead Temperature (soldering, 10s)	+300°C

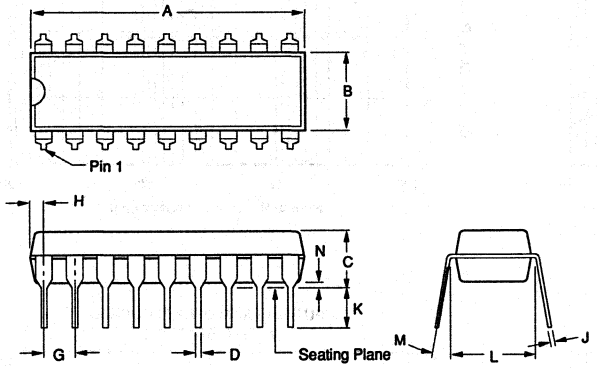
The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE
INA120AP	Plastic DIP	–25°C to +85°C
INA120BP	Plastic DIP	–25°C to +85°C
INA120BG	Ceramic DIP	–25°C to +85°C
INA120CG	Ceramic DIP	–25°C to +85°C

MECHANICAL

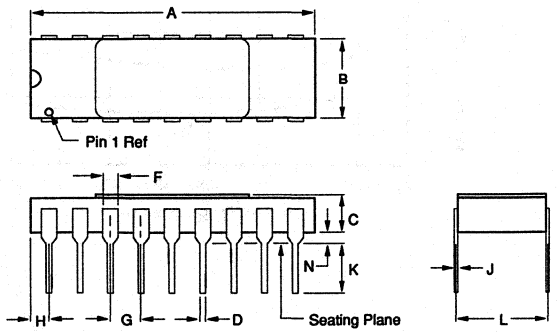
P Package — 18-Pin Plastic DIP



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	.840	.940	21.34	23.88
B	.240	.280	6.10	7.11
C	—	.210	—	5.33
D	.014	.022	0.36	0.59
G	.100 BASIC		2.54 BASIC	
H	.040	.060	1.02	1.52
J	.008	.015	0.20	0.38
K	.115	.150	2.92	3.81
L	.280	.300	7.11	7.62
M	0°	10°	0°	10°
N	.000	.012	0.00	0.30

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

G Package — 18-Pin Ceramic DIP



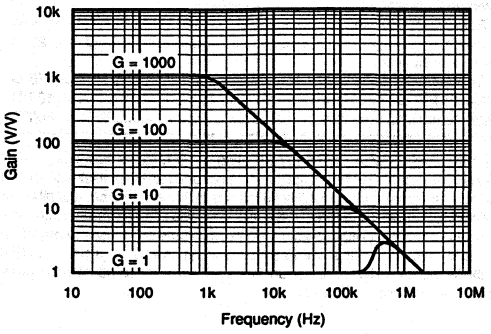
	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	—	.960	—	24.38
B	.220	.310	5.59	7.87
C	—	.200	—	5.08
D	.014	.023	.36	.58
F	.030	.070	.76	1.78
G	.100 BASIC		2.54 BASIC	
H	—	.098	—	2.49
J	.008	.015	.20	.38
K	.125	.200	3.18	5.08
L	.290	.320	7.37	8.13
N	.015	.060	.38	1.52

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

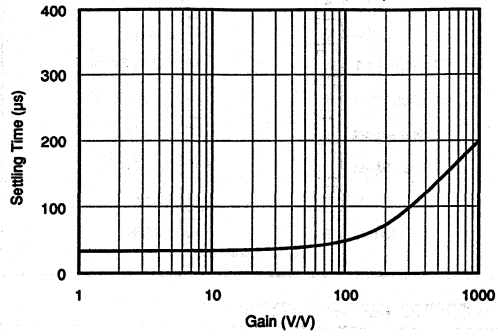
TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_S = ±15V unless otherwise noted.

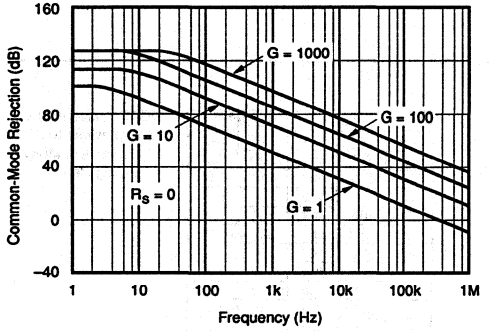
GAIN vs FREQUENCY



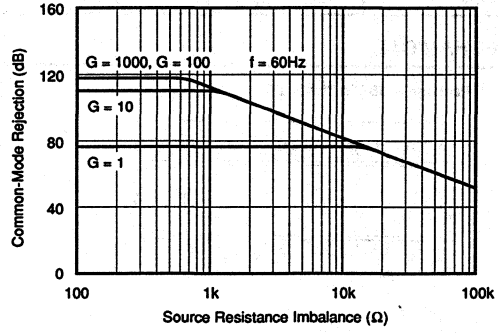
SETTLING TIME vs GAIN (0.1%)



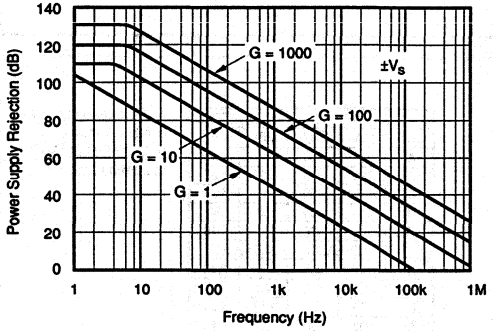
COMMON-MODE REJECTION vs FREQUENCY



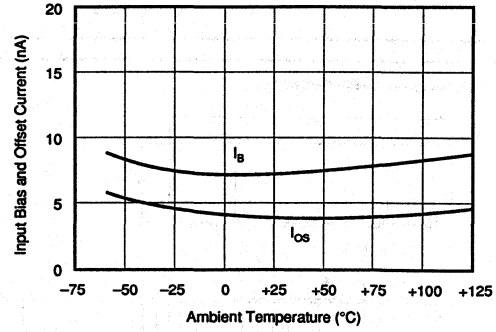
COMMON-MODE REJECTION vs SOURCE RESISTANCE IMBALANCE



POWER SUPPLY REJECTION vs FREQUENCY



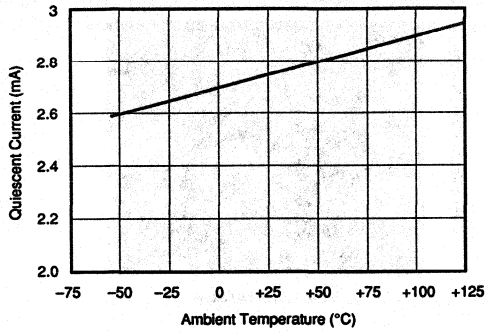
INPUT BIAS AND OFFSET CURRENT vs TEMPERATURE



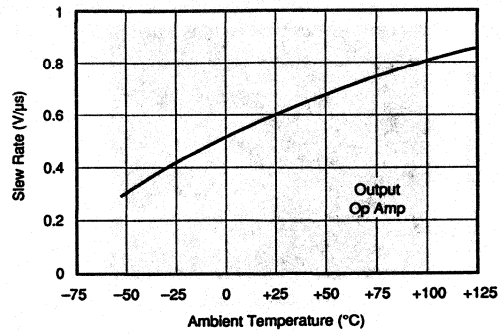
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_S = ±15V unless otherwise noted.

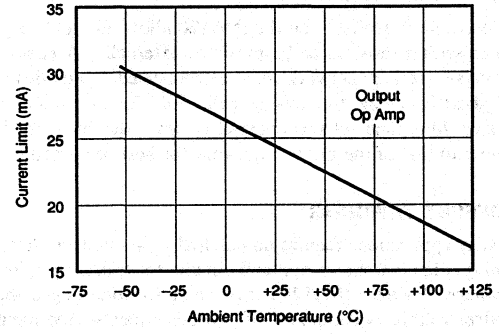
QUIESCENT CURRENT vs TEMPERATURE



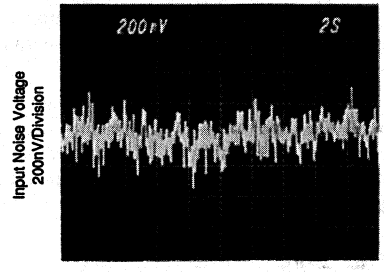
SLEW RATE vs TEMPERATURE



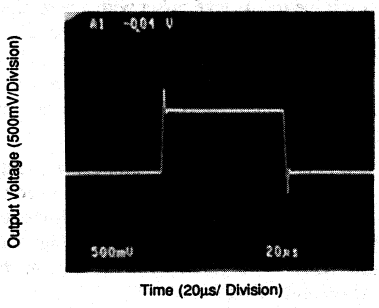
CURRENT LIMIT vs TEMPERATURE



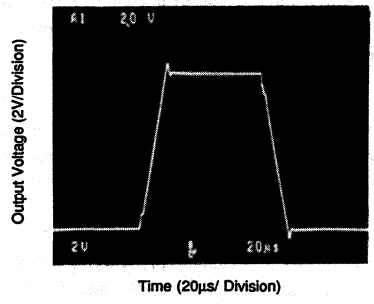
INPUT-REFERRED NOISE
G = 1000



SMALL-SIGNAL TRANSIENT RESPONSE
G = 1



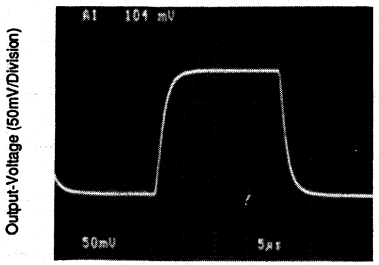
LARGE-SIGNAL TRANSIENT
RESPONSE G = 1



TYPICAL PERFORMANCE CURVES (CONT)

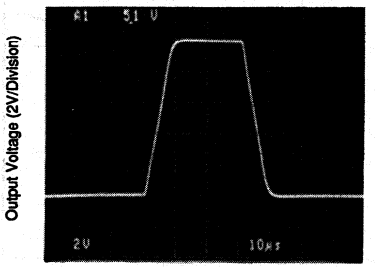
T_A = +25°C, V_S = ±15V unless otherwise noted.

SMALL-SIGNAL TRANSIENT RESPONSE
G = 100



Time (5µs/ Division)

LARGE-SIGNAL TRANSIENT
RESPONSE G = 100



Time (10µs/ Division)

APPLICATION INFORMATION

Figure 1 shows the basic connections required for operation of the INA120. Applications with noisy or high impedance power supply lines may require decoupling capacitors close to the device pins as shown. The differential input voltage is applied to pins 16 and 3.

The output is referred to the output common reference terminal, pin 18. This terminal must have a low-impedance connection to ground. A resistance of 1Ω or greater in series with the common terminal could degrade common-mode rejection beyond the specified value.

SETTING THE GAIN

Gains of 1, 10, 100 or 1000 can be configured by interconnecting the gain-set pins as shown in the table of Figure 1. These pin-strapped gains provide best gain accuracy and drift because they are determined by the ratios of accurately trimmed and matched on-chip resistors.

Digital gain control can be achieved using an analog multiplexer as shown in Figure 2. Since the switches are in series with the high impedance gain-sense connections, pins 4 and 15, their series resistance does not significantly affect gain error or drift. Gain error at G = 1 is slightly higher than with direct pin connections shown in Figure 1. The gain is selected with a two-bit address, A_0 and A_1. The Multiplexer Enable control is directly connected to V+ since a logic "low" on this line would cause the input amplifiers to run open-loop.

Other gains may be set by connecting an external resistor, R_G, as shown in Figure 3a. Gain accuracy using an external gain-setting resistor is a function of R_G and the internal 20kΩ resistors. The internal resistors are typically within ±0.2% of nominal value and their drift under ±80ppm/°C. Inaccuracy and drift of R_G will contribute additional gain error and drift.

Figure 3b shows an external gain-setting resistor connected in parallel with internal resistors. By forming a portion of the effective R_G with internal resistors, gain accuracy and drift can be somewhat improved.

Connections available on the INA120 allow all input stage gain-setting resistors to be provided externally. A custom precision resistor network could be connected to provide the highest accuracy and lowest gain drift for non-standard gains. Impedance of this external network should be made close to that of the internal network for best performance.

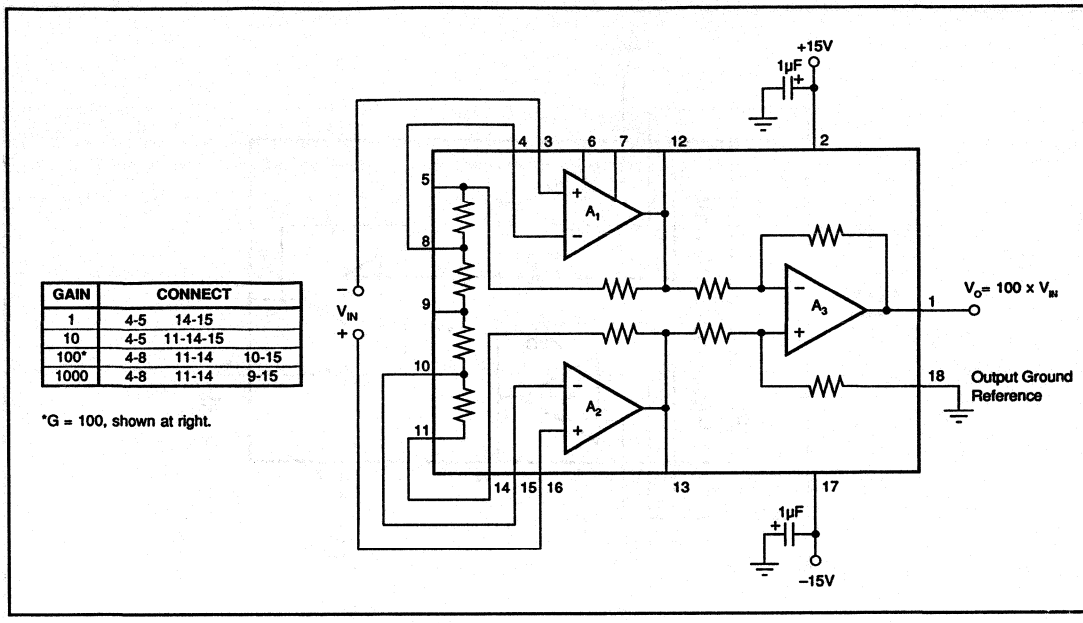
OFFSET TRIMMING

Many applications require no external offset voltage trimming. Figure 4 shows optional circuits for trimming offset voltage. Since the INA120 has two amplification stages, the offset voltage is comprised of two components—the input stage offset and output stage offset.

The input stage offset is equal to the combined offset of op amps A_1 and A_2. This input stage offset dominates at high gain. When used in gains of 100 to 1000, it is often sufficient to adjust the input stage offset with a potentiometer connected to pins 6 and 7 as shown. Connect both inputs to ground and adjust for 0V at the output, pin 1. Do not use pins 6 and 7 to trim offset voltage at G = 1 or to correct for offset in devices following the INA120 since this can cause excessive offset voltage drift.

At G = 1, offset is dominated by the output stage. Output stage offset can be trimmed by applying a correction voltage at the output reference terminal, pin 18. Low impedance must be maintained at this node to preserve the high CMR of the INA120. This is achieved by buffering the trim voltage with an op amp as shown.

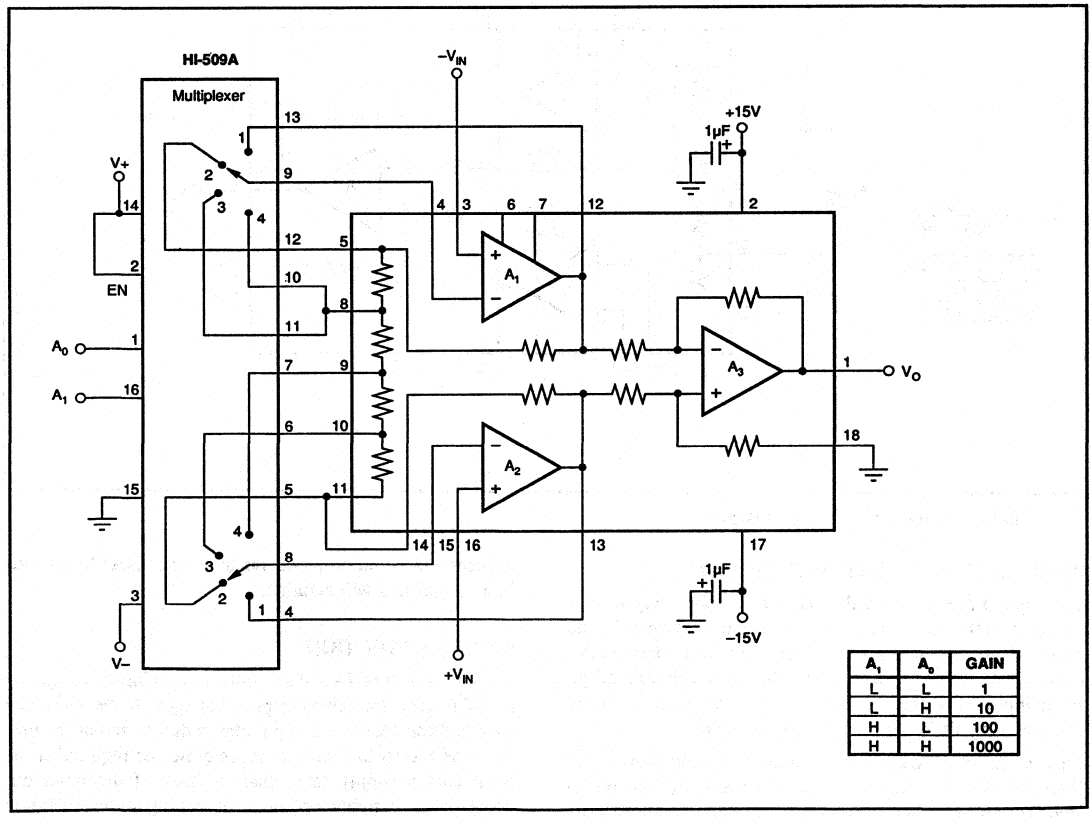
At intermediate gains it may be necessary to provide both input stage and output stage offset adjustments. Again, ground both inputs. Connect a jumper between pins 9 and 11 (temporarily connects the INA120 in high gain) and adjust R_1 for 0V at the output, pin 1. Then disconnect the jumper and adjust the output offset control for 0V output.



GAIN	CONNECT		
1	4-5	14-15	
10	4-5	11-14-15	
100*	4-8	11-14	10-15
1000	4-8	11-14	9-15

*G = 100, shown at right.

FIGURE 1. Basic Connection.



A1	A0	GAIN
L	L	1
L	H	10
H	L	100
H	H	1000

FIGURE 2. Digital Gain Control.

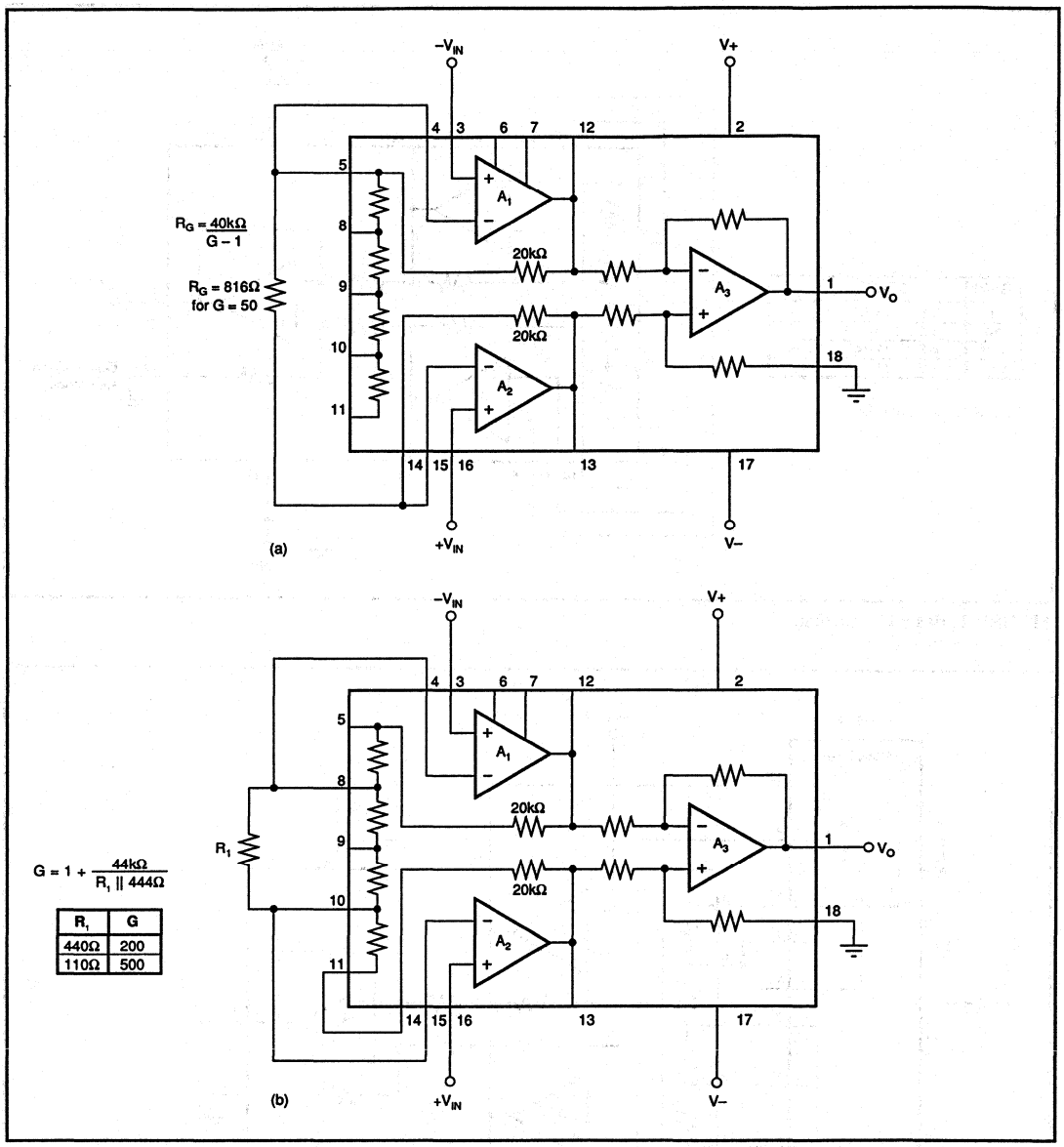


FIGURE 3. External Gain-Setting Resistors.

INPUT BIAS CURRENT RETURN PATH

The input impedance of the INA120 is extremely high—approximately $10^{10}\Omega$. This does not mean, however, that no current flows in the input terminals. The input bias current of the INA120 is typically ±10nA (it can be either polarity). High input impedance means that this input bias current changes very little with varying input voltage.

Input circuitry must provide a path for this input bias current if the INA120 is to function. Figure 5 shows various provisions for an input bias current path. Without an appropriate current path, the inputs will float to a potential which exceeds the common-mode range of the INA120 and the input amplifiers will saturate.

INPUT PROTECTION

The inputs of the INA120 are protected for input voltages up to 2V beyond the power supply voltages. If the input can exceed these conditions, input clamp diodes should be provided as shown in Figure 6. R_s may not be required if the input cannot supply more than 100mA. If the input can supply larger currents, choose R_s according to the maximum source voltage, limiting current to under 100mA.

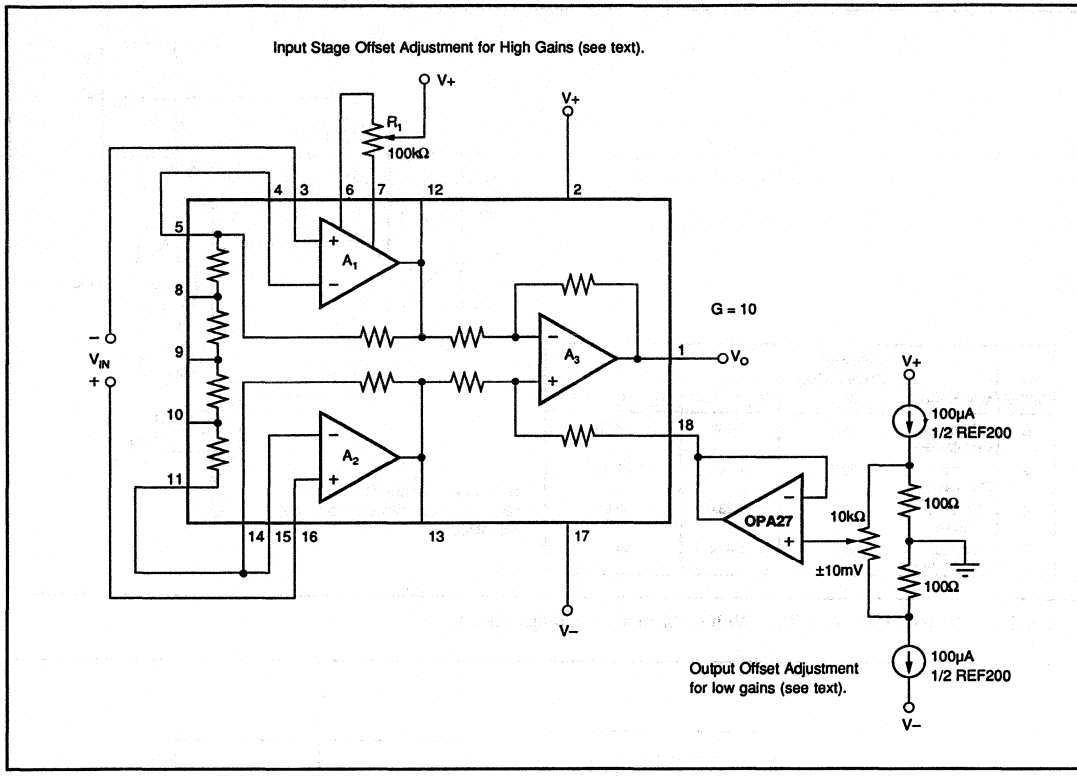


FIGURE 4. Offset Adjustment Circuits.

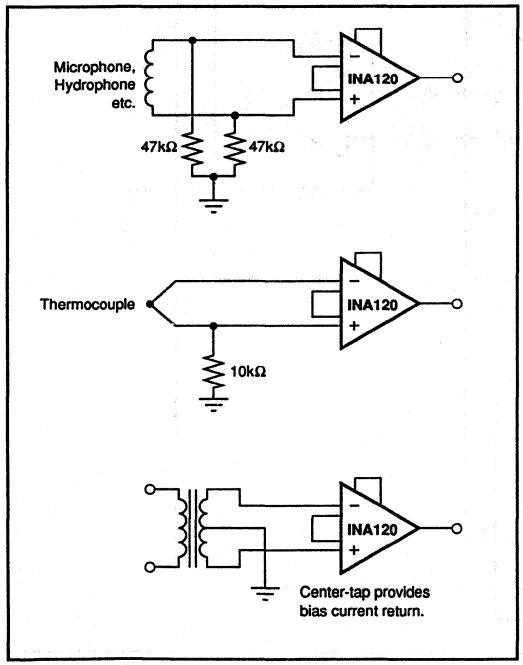


FIGURE 5. Providing an Input Bias Current Path.

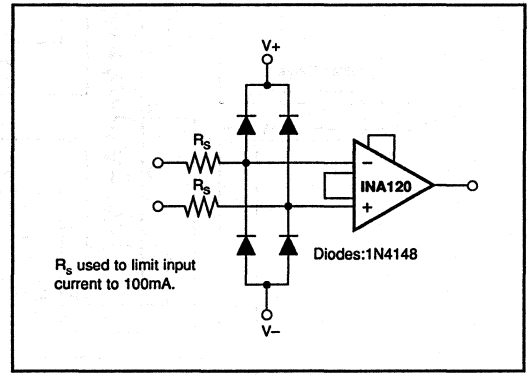
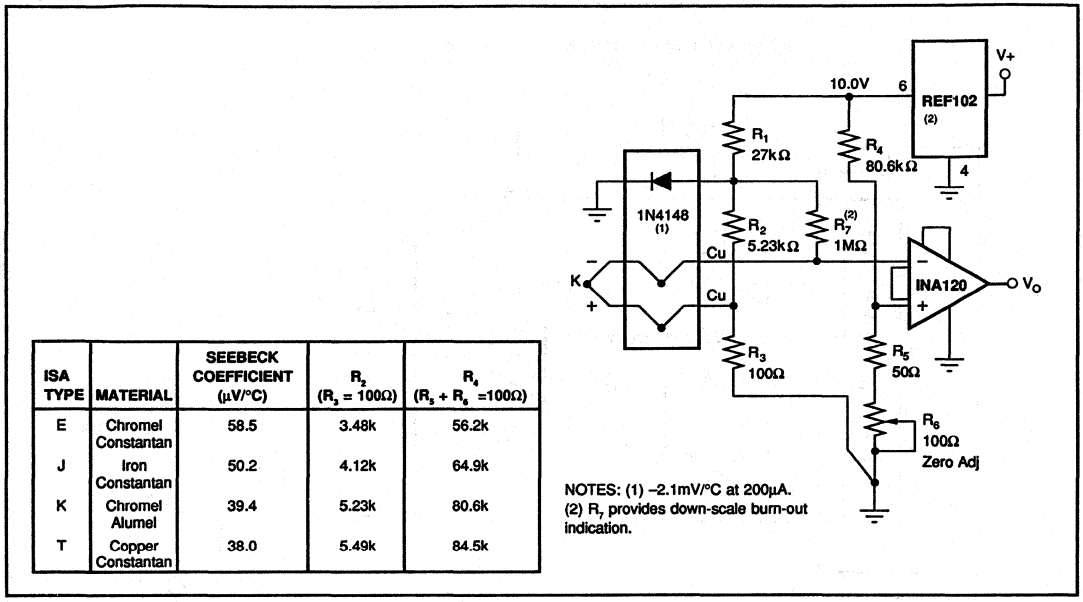


FIGURE 6. Input Protection Circuit.



ISA TYPE	MATERIAL	SEEBECK COEFFICIENT (µV/°C)	R_2 (R_2 = 100Ω)	R_4 ($R_5 + R_6$ =100Ω)
E	Chromel Constantan	58.5	3.48k	56.2k
J	Iron Constantan	50.2	4.12k	64.9k
K	Chromel Alumel	39.4	5.23k	80.6k
T	Copper Constantan	38.0	5.49k	84.5k

FIGURE 7. Thermocouple Amplifier With Cold Junction Compensation.

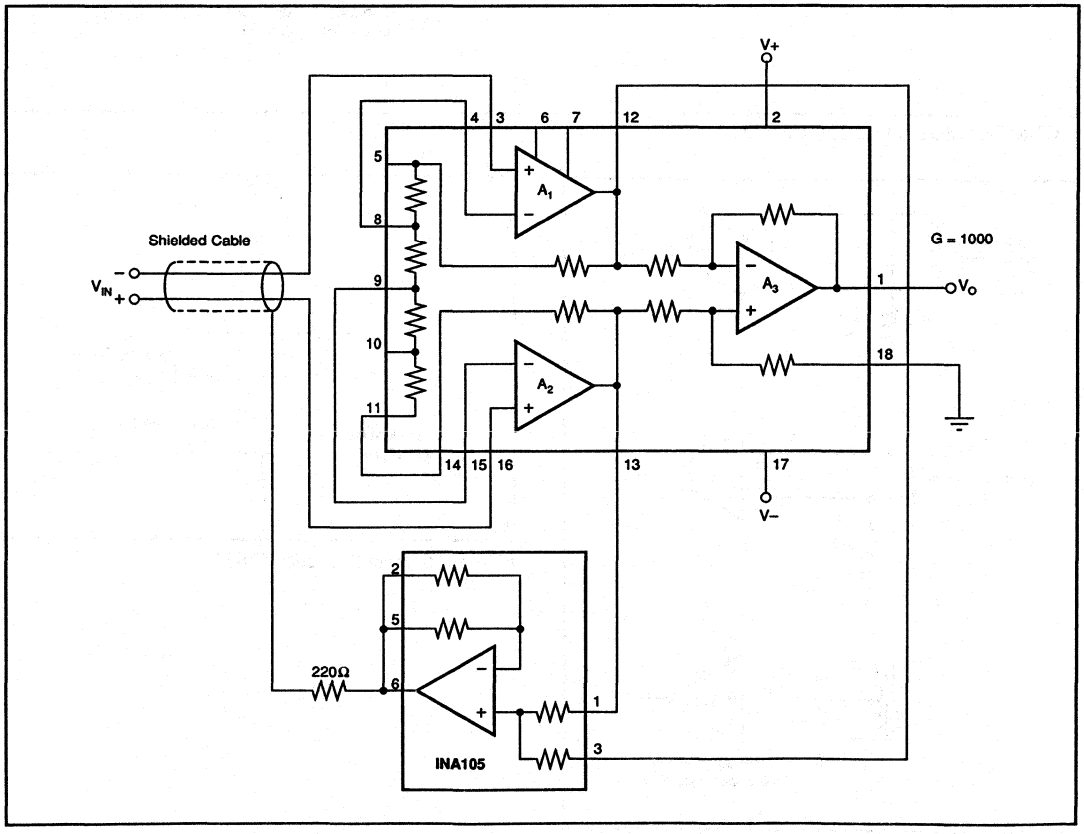


FIGURE 8. Guard Drive Circuit.

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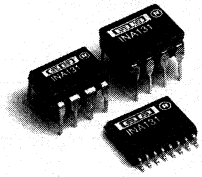


INA131

**ADVANCED INFORMATION
SUBJECT TO CHANGE**

Precision G = 100 INSTRUMENTATION AMPLIFIER

FEATURES

- LOW OFFSET VOLTAGE: 50µV max
- LOW OFFSET VOLTAGE DRIFT: 0.35µV/°C max
- LOW INPUT BIAS CURRENT: 2nA max
- HIGH COMMON-MODE REJECTION: 110dB at 60Hz
- INPUT OVERVOLTAGE PROTECTION: ±40V
- 8-PIN PLASTIC AND CERAMIC DIP, SOL-16 SOIC

APPLICATIONS

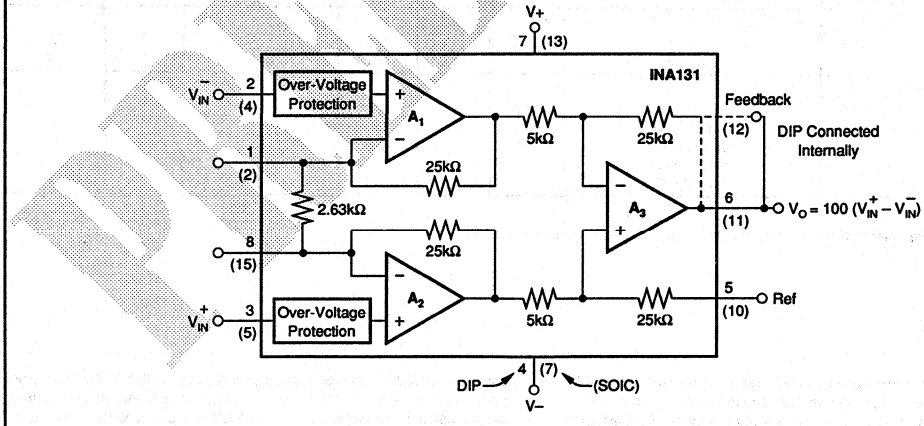
- BRIDGE AMPLIFIER
- THERMOCOUPLE AMPLIFIER
- RTD SENSOR AMPLIFIER
- MEDICAL INSTRUMENTATION
- DATA ACQUISITION SYSTEM

DESCRIPTION

The INA131 is a low cost, general purpose G = 100 instrumentation amplifier offering excellent accuracy. Its 3-op amp design and small size make it ideal for a wide range of applications.

On-chip laser trimmed resistors accurately set a fixed gain of 100. The INA131 is laser trimmed to achieve very low offset voltage (50µV), drift (0.35µV/°C) and high CMR (110dB). Internal input protection can withstand up to ±40V inputs without damage.

The INA131 is available in 8-pin plastic and ceramic DIPs and SOL-16 surface-mount packages. They are specified over the –40°C to +85°C temperature range.



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SPECIFICATIONS

ELECTRICAL

T_A = +25°C, V_S = ±15V, R_L = 2kΩ, unless otherwise noted.

PARAMETER	CONDITIONS	INA131BP/BG MIN	INA131BP/BG TYP	INA131BP/BG MAX	INA131AP/AG/AU MIN	INA131AP/AG/AU TYP	INA131AP/AG/AU MAX	UNITS
INPUT								
Offset Voltage, RTI								
Initial	T_A = +25°C		±10	±50		±25	±125	µV
vs Temperature	T_A = T_{MIN} to T_{MAX}		±0.1	±0.35		±0.25	±2	µV/°C
Long-Term Stability			±1			*		µV/mo
vs Power Supply	V_S = ±2.25V to ±18V		1	3		*	*	µV/V
Impedance, Differential			10^9 || 3			*		Ω || pF
Common-Mode			10^{10} || 3			*		Ω || pF
Input Common-Mode Range		±11	±13.5		*	*		V
Safe Input Voltage			±40			*		V
Common-Mode Rejection	V_{CM} = ±10V, ΔR_S = 1kΩ	110	115		106	110		dB
BIAS CURRENT			±0.3	±2		*	±5	nA
vs Temperature			±15			*		pA/°C
OFFSET CURRENT			±0.5	±2		*	±5	nA
vs Temperature			±15			*		pA/°C
NOISE VOLTAGE, RTI	R_S = 0Ω							
f = 10Hz			18			*		nV/√Hz
f = 100Hz			15			*		nV/√Hz
f = 1kHz			12			*		nV/√Hz
f = 10kHz			10			*		nV/√Hz
f_B = 0.1Hz to 10Hz			0.7			*		µVp-p
Noise Current								
f = 10Hz			1			*		pA/√Hz
f= 1kHz			0.5			*		pA/√Hz
f_B = 0.1Hz to 100Hz			40			*		pAp-p
GAIN								
Gain Error			±0.1	±0.2		*	±0.5	%
Resistor Value[1]			±10	±30		*	*	%
Gain vs Temperature			±5	±10		*	±20	ppm/°C
Nonlinearity			±0.001	±0.002		*	±0.004	% of FSR
OUTPUT								
Voltage	I_O = 5mA, T_{MIN} to T_{MAX}	±13.5	±13.7	*	*			V
	V_S = ±11.4V, R_L = 2kΩ	±10			*			V
	V_S = ±2.25V, R_L = 2kΩ	±1			*			V
Load Capacitance Stability			1000			*		pF
Short Circuit Current			+20/–12			*		mA
FREQUENCY RESPONSE								
Bandwidth, –3dB			50			*		kHz
Slew Rate	V_O = ±10V	0.3	0.5		*	*		V/µs
Settling Time, 0.1%			50			*		µs
0.01%			60			*		µs
Overload Recovery	50% Overdrive		20			*		µs
POWER SUPPLY								
Voltage Range		±2.25	±15	±18	*	*	*	V
Current	V_{IN} = 0V		±2.2	±3		*	*	mA
TEMPERATURE RANGE								
Specification		–40		85	*		*	°C
Operating	Plastic P, U	–40		125	*		*	°C
	Ceramic, G	–55		125	*		*	°C
θ_{JA}	Plastic, P, U		80			*		°C/W
	Ceramic, G		90			*		°C/W

* Specification same as INA131BG.

NOTE: (1) Absolute value of internal gain-setting resistors. (Gain depends on resistor ratios.)

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

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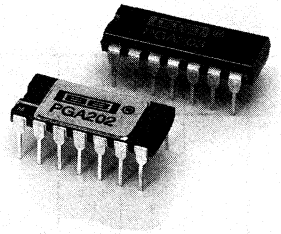


PGA202/203

Digitally Controlled Programmable-Gain INSTRUMENTATION AMPLIFIER

FEATURES

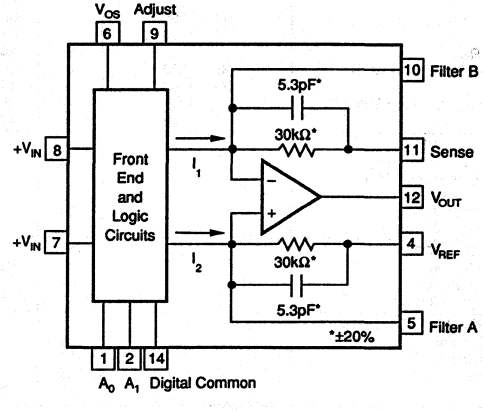
- DIGITALLY PROGRAMMABLE GAINS:
  DECADE MODEL—PGA202
  GAINS OF 1, 10, 100, 1000
  BINARY MODEL—PGA203
  GAINS OF 1, 2, 4, 8
- LOW BIAS CURRENT: 50pA max
- FAST SETTLING: 2µs to 0.01%
- LOW NON-LINEARITY: 0.012% max
- HIGH CMRR: 80dB min
- NEW TRANSCONDUCTANCE CIRCUITRY
- LOW COST

APPLICATIONS

- DATA ACQUISITION SYSTEMS
- AUTO-RANGING CIRCUITS
- DYNAMIC RANGE EXPANSION
- REMOTE INSTRUMENTATION
- TEST EQUIPMENT

DESCRIPTION

The PGA202 is a monolithic instrumentation amplifier with digitally controlled gains of 1, 10, 100 and 1000. The PGA203 provides gains of 1, 2, 4, and 8. Both have TTL or CMOS-compatible inputs for easy microprocessor interface. Both have FET inputs and a new transconductance circuitry that keeps the bandwidth nearly constant with gain. Gain and offsets are laser trimmed to allow use without any external components. Both amplifiers are available in ceramic or plastic packages. The ceramic package is specified over the full industrial temperature range while the plastic package covers the commercial range.



Covered by U.S. PATENT #4,883,422

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SPECIFICATIONS

ELECTRICAL

At +25°C, V_{CC} = ±15V unless otherwise noted.

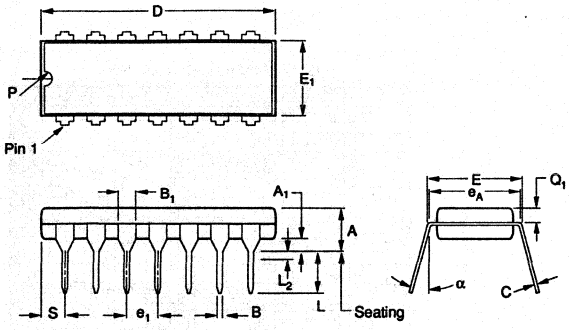
PARAMETER	CONDITION	PGA202/203AG[1] MIN	PGA202/203AG[1] TYP	PGA202/203AG[1] MAX	PGA202/203BG[1] MIN	PGA202/203BG[1] TYP	PGA202/203BG[1] MAX	PGA202/203KP[1] MIN	PGA202/203KP[1] TYP	PGA202/203KP[1] MAX	UNITS
GAIN											
Error[2]	G < 1000		0.05	0.25		*	0.15		*	*	%
	G = 1000		0.1	1		0.08	0.5		*	*	%
Nonlinearity	G < 1000		0.002	0.015		*	0.012		*	*	%
	G = 1000		0.02	0.06		*	0.04		*	*	%
Gain vs Temperature	G < 100		3	12		*	8		*		ppm/°C
	G = 100		40	120		*	60		*		ppm/°C
	G = 1000		100	300		*	150		*		ppm/°C
RATED OUTPUT											
Voltage	$\|I_{OUT}\| \leq$ 5mA	±10	±12		*	*		*	*		V
Over Specified Temperature	See Typical Perf. Curve		±9			*			±10		V
Current	$\|V_{OUT}\| \leq$ 10V	±5	±10		*	*		*	*		mA
Impedance			0.5			*			*		Ω
ANALOG INPUTS											
Common-Mode Range		±10	±13		*	*		*	*		V
Abolute Max Voltage[3]	No Damage			±V_{CC}			*			*	V
Impedance, Differential			10 || 3			*			*		GΩ || pF
Common-Mode			10 || 1			*			*		GΩ || pF
OFFSET VOLTAGE (RTI)											
Initial Offset at 25°C[4]			±(0.5 + 5/G)	±(2 + 24/G)		*	±(1 + 12/G)		*	*	mV
vs Temperature			±(3 + 50/G)	±(12 + 240/G)		*	±(6 + 120/G)		*		µV/°C
Offset vs Time			50			*			*		µV/Month
Offset vs Supply	10 ≤ V_{CC} ≤ 15		10 + 250/G	100 + 900/G		*	50 + 450/G		*	*	µV/V
INPUT BIAS CURRENT											
Initial Bias Current: at 25°C			10	50		*	*		*	*	pA
at 85°C			640	3200		*	*		*	*	pA
Initial Offset Current: at 25°C			5	25		*	*		*	*	pA
at 85°C			320	1600		*	*		*	*	pA
COMMON MODE REJECTION RATIO											
	G = 1	80	100		*	*		*	*		dB
	G = 10	86	110		*	*		*	*		dB
	G = 100	92	120		*	*		*	*		dB
	G = 1000	94	120		*	*		*	*		dB
INPUT NOISE											
Noise Voltage 0.1 to 10Hz			1.7			*			*		µVp-p
Noise Density at 10kHz[5]			12			*			*		nV/√Hz
OUTPUT NOISE											
Noise Voltage 0.1 to 10Hz			32			*			*		µVp-p
Density at 1kHz[5]			400			*			*		nV/√Hz
DYNAMIC RESPONSE											
Frequency Response	G < 1000		1000			*			*		kHz
	G = 1000		250			*			*		kHz
Full Power Bandwidth	G < 1000		400			*			*		kHz
	G = 1000		100			*			*		kHz
Slew Rate		10	20		15	*		*	*		V/µs
Settling Time (0.01%)[7]	G < 1000		2			*			*		µs
	G = 1000		10			*			*		µs
Overload Recovery Time[7]	G < 1000		5			*			*		µs
	G = 1000		10			*			*		µs
DIGITAL INPUTS											
Digital Common Range		-V_{CC}		V_{CC} – 8	*		*	*		*	V
Input Low Threshold[6]				0.8			*			*	V
Input Low Current				10			*			*	µA
Input High Voltage		2.4			*			*			V
Input High Current				10			*			*	µA
POWER SUPPLY											
Rated Voltage			±15			*			*		V
Voltage Range		±6		±18	*		*	*		*	V
Quiescent Current			6.5			*			*		mA
TEMPERATURE RANGE											
Specification		–25		85	*		*	0		70	°C
Operating		–55		125	*		*	–25		85	°C
Storage		–65		150	*		*	–40		100	°C
θ_{JA}			100			*			*		°C/W

* Same as the PGA202/203AG

NOTES: (1) All specifications apply to both the PGA202 and the PGA203. Values given for a gain of 10 are the same for a gain of 8 and other values may be interpolated. (2) Measured with a 10k load. (3) The analog inputs are internally diode clamped. (4) Adjustable to zero. (5) $V_{NOISE\ (RTI)} = \sqrt{(V_{N\ INPUT})^2 + (V_{N\ OUTPUT}/Gain)^2}$. (6) Threshold voltages are referenced to Digital Common. (7) From input change or gain change.

MECHANICAL

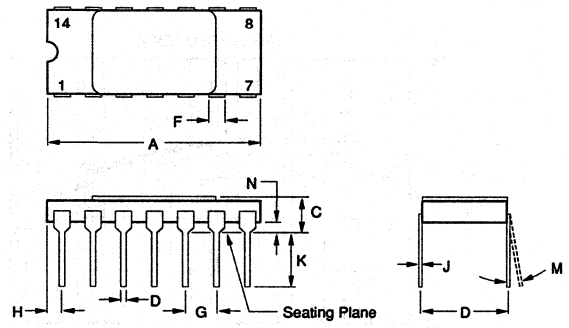
G Package — 14-Pin Plastic Package



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.120	.160	3.048	4.064
A_1	.015	.065	.381	1.651
B	.014	.020	.355	.508
B_1	.050	.065	1.270	1.651
C	.008	.012	.203	.304
D	.745	.770	18.923	19.558
E	.300	.325	7.620	8.255
E_1	.240	.260	6.096	6.604
e_1	.100 BASIC		2.540 BASIC	
e_A	.300 BASIC		7.620 BASIC	
L	.125	.150	3.175	3.810
L_2(1)	0	.030	0	.762
α	0°	15°	0°	15
P	—	.050	—	1.270
Q_1	.050	.085	1.270	2.159
S(2)	.065	.090	1.651	2.286

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.
(1) e_1 and e_A apply in zone L_2 when unit is installed.
(2) Not per JEDEC.

G Package — 14-Pin Hermetic DIP



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.670	.710	17.02	18.03
C	.065	.170	1.65	4.32
D	.015	.021	0.38	0.53
F	.045	.060	1.14	1.52
G	.100 BASIC		2.54 BASIC	
H	.025	.070	0.64	1.78
J	.008	.012	0.20	0.30
K	.120	.240	3.05	6.10
L	.300 BASIC		7.62 BASIC	
M	—	10°	—	10°
N	.009	.060	0.23	1.52

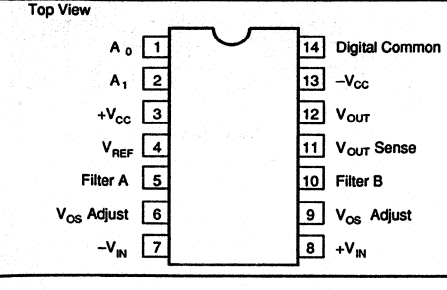
NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.

ORDERING INFORMATION

MODEL	GAINS	PACKAGE	TEMPERATURE RANGE	OFFSET VOLTAGE MAX (mV)
PGA202KP	1, 10, 100, 1000	Plastic DIP	0°C to +70°C	±(2 + 24/G)
PGA202AG	1, 10, 100, 1000	Ceramic DIP	–25°C to +85°C	±(2 + 24/G)
PGA202BG	1, 10, 100, 1000	Ceramic DIP	–25°C to +85°C	±(1 + 12/G)
PGA203KP	1, 2, 4, 8	Plastic DIP	0°C to +70°C	±(2 + 24/G)
PGA203AG	1, 2, 4, 8	Ceramic DIP	–25°C to +85°C	±(2 + 24/G)
PGA203BG	1, 2, 4, 8	Ceramic DIP	–25°C to +85°C	±(1 + 12/G)

PIN CONFIGURATION

Top View



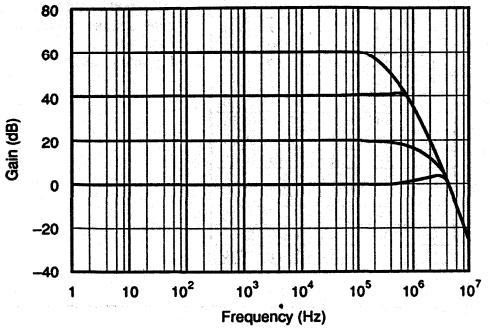
ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18V
Internal Power Dissipation	750mW
Analog and Digital Inputs	±(V_{CC} + 0.5V)
Operating Temperature Range:	
G Package	–55°C to +125°C
P Package	–40°C to +100°C
Lead Temperature (soldering, 10s)	300°C
Output Short Circuit Duration	Continuous
Junction Temperature	175°C

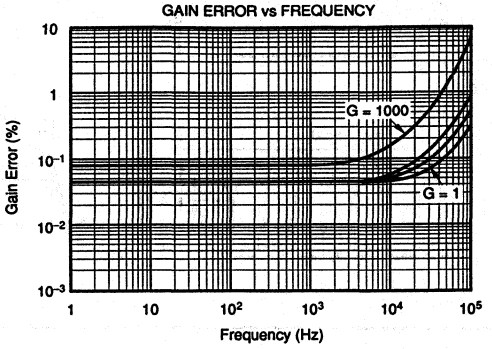
TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_S = ±15V unless otherwise noted.

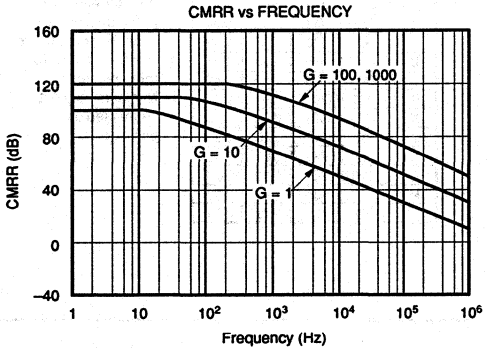
GAIN vs FREQUENCY



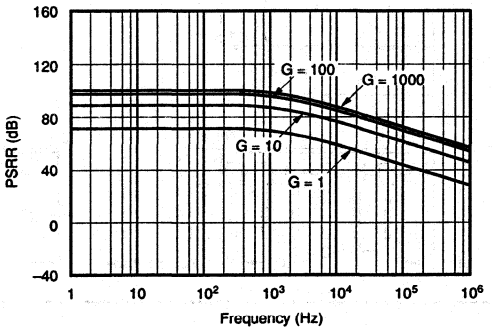
GAIN ERROR vs FREQUENCY



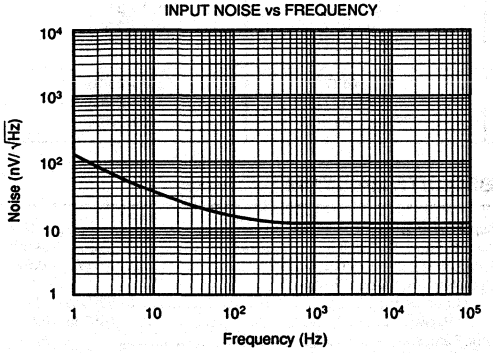
CMRR vs FREQUENCY



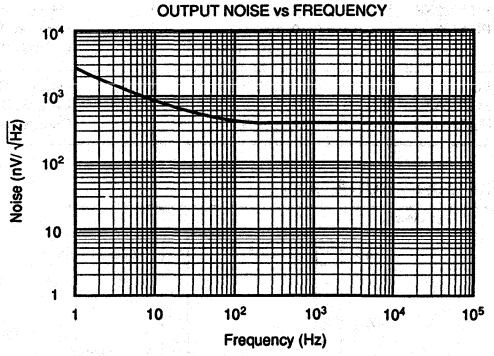
PSRR vs FREQUENCY



INPUT NOISE vs FREQUENCY



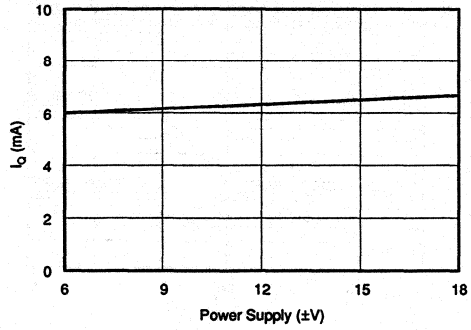
OUTPUT NOISE vs FREQUENCY



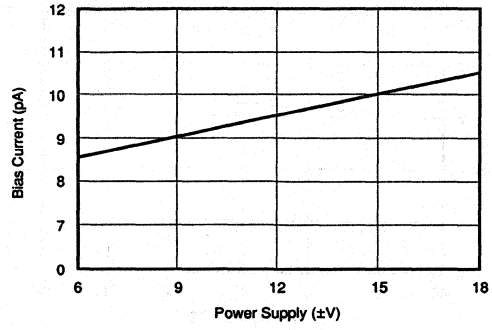
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_S = ±15V unless otherwise noted.

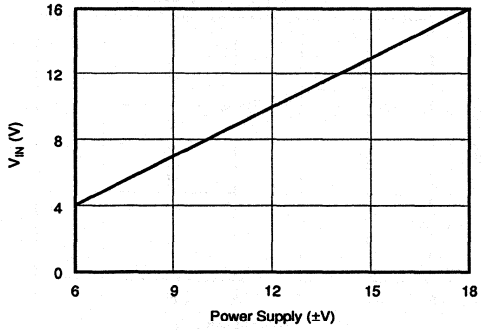
QUIESCENT CURRENT vs POWER SUPPLY



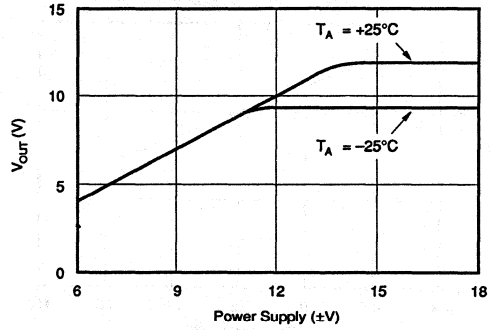
BIAS CURRENT vs POWER SUPPLY



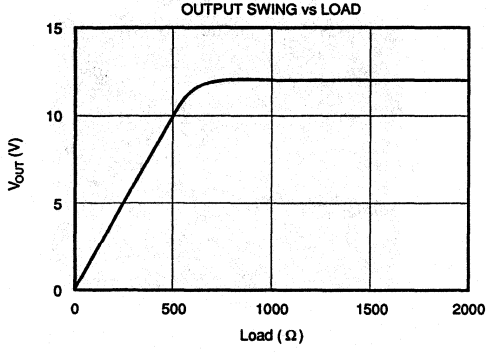
INPUT RANGE vs POWER SUPPLY



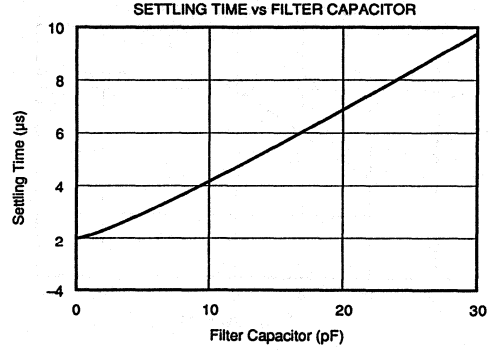
OUTPUT SWING vs POWER SUPPLY



OUTPUT SWING vs LOAD



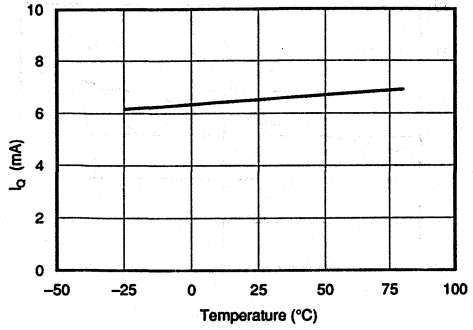
SETTLING TIME vs FILTER CAPACITOR



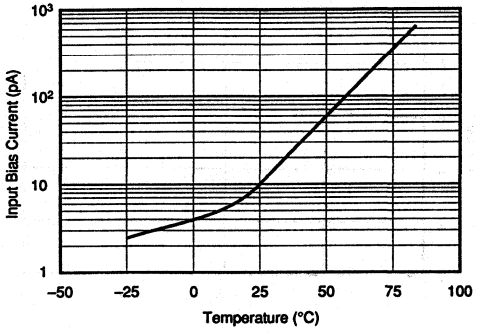
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_S = ±15V unless otherwise noted.

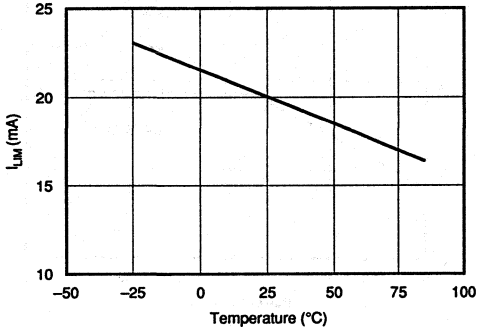
QUIESCENT CURRENT vs TEMPERATURE



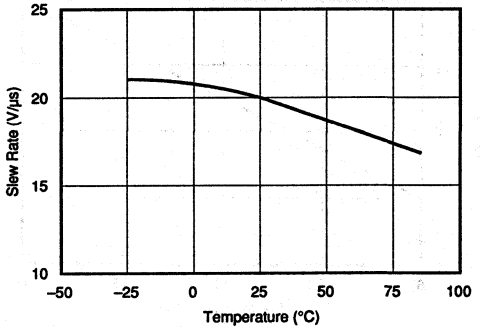
INPUT BIAS CURRENT vs TEMPERATURE



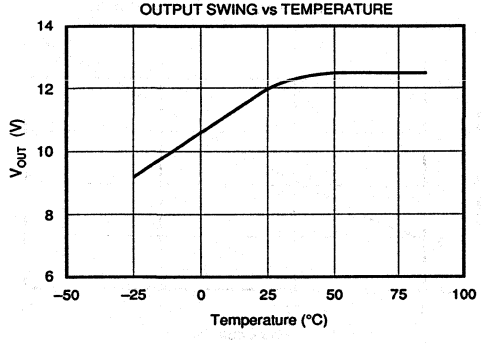
CURRENT LIMIT vs TEMPERATURE



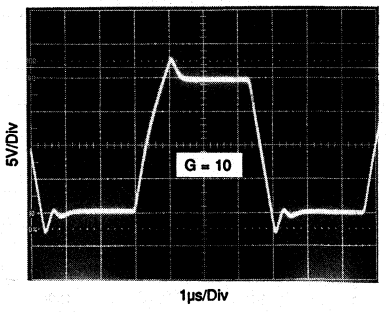
SLEW RATE vs TEMPERATURE



OUTPUT SWING vs TEMPERATURE



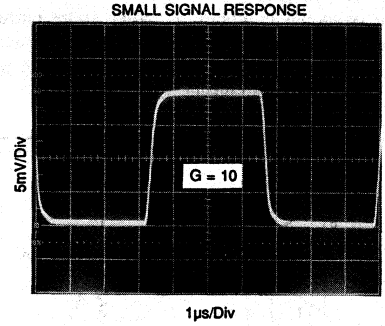
LARGE SIGNAL RESPONSE



TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_{CC} = ±15V unless otherwise noted.

SMALL SIGNAL RESPONSE



DISCUSSION OF PERFORMANCE

A simplified diagram of the PGA202/203 is shown on the first page. The design consists of a digitally controlled, differential transconductance front end stage using precision FET buffers and the classical transimpedance output stage. Gain switching is accomplished with a novel current steering technique that allows for fast settling when changing gains. The result is a high performance, programmable instrumentation amplifier with excellent speed and gain accuracy.

The input stage uses a new circuit topology that includes FET buffers to give extremely low input bias currents. The differential input voltage is converted into a differential output current with the transconductance gain selected by steering the input stage bias current between four identical input stages differing only in the value of the gain setting resistor. Each input stage is individually laser-trimmed for input offset, offset drift and gain.

The output stage is a differential transimpedance amplifier. Unlike the classical difference amplifier output stage, the common mode rejection is not limited by the resistor matching. However, the output resistors are laser-trimmed to help minimize the output offset and drift.

BASIC CONNECTIONS

Figure 1 shows the proper connections for power supply and signal. The power supplies should be decoupled with 1µF tantalum capacitors placed as close to the amplifier as possible for maximum performance. To avoid gain and CMR errors introduced by the external components, you should connect the grounds as indicated. Any resistance in the sense line (pin 11) or the V_{REF} line (pin 4) will lead to a gain error, so these lines should be kept as short as possible. Also to maintain stability, avoid capacitance from the output to the input or the offset adjust pins.

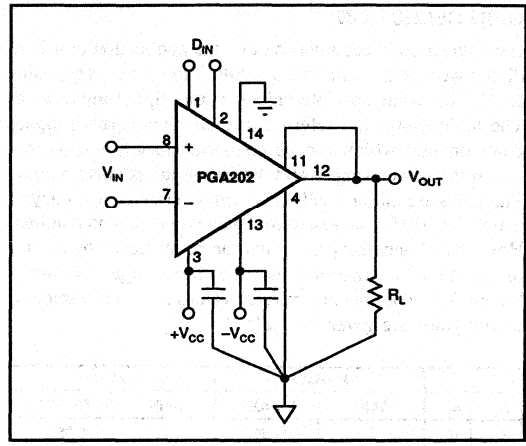


FIGURE 1. Basic Circuit Connections.

OFFSET ADJUSTMENT

Figure 2 shows the offset adjustment circuits for the PGA202/203. The input offset and the output offset are both separately adjustable. Notice that because the PGA202/203 change between four different input stages to change gain, the input offset voltage will change slightly with gain. For systems using computer autozeroing techniques, neither offset nor drift is a major concern, but it should be noted that since the input offset does change with gain, these systems should perform an autozero cycle after each gain change for optimum performance.

In the output offset adjustment circuit, the choice of the buffering op amp is very important. The op amp needs to have low output impedance and a wide bandwidth to maintain full accuracy over the entire frequency range of the PGA202/203. For these reasons we recommend the OPA602 as an excellent choice for this application.

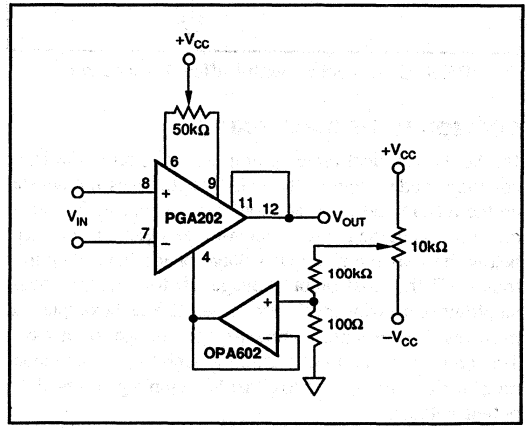


FIGURE 2. Offset Adjustment Circuits.

GAIN SELECTION

Gain selection is accomplished by the application of a 2-bit digital word to the gain select inputs. Table I shows the gains for the different possible values of the digital input word. The logic inputs are referred to their own separate digital common pin, which can be connected to any voltage between the minus supply and 8V below the positive supply. The gains are all internally trimmed to an initial accuracy of better than 0.1%, so no external gain adjustment is required. However, if necessary the gains can be increased by the use of an external attenuator around the output stage as shown in Figure 3. Recommended resistor values for certain selected output gains are given in Table II.

		PGA202		PGA203	
A_1	A_0	GAIN	ERROR	GAIN	ERROR
0	0	1	0.05%	1	0.05%
0	1	10	0.05%	2	0.05%
1	0	100	0.05%	4	0.05%
1	1	1000	0.10%	8	0.05%

TABLE I. Software Gain Selection.

OUTPUT GAIN	R_1	R_2
2	5kΩ	5kΩ
5	2kΩ	8kΩ
10	1kΩ	9kΩ

TABLE II. Output Stage Gain Control.

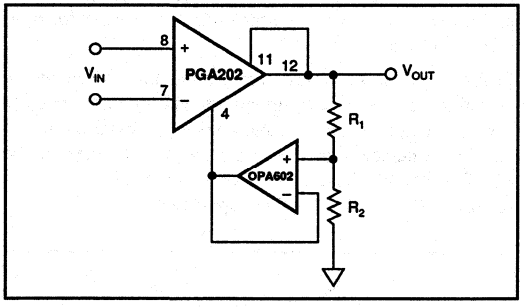


FIGURE 3. Gain Increase with Buffered Attenuator.

COMMON-MODE INPUT RANGE

Unlike the classical three op amp type of circuit, the input common-mode range of the PGA202/203 does not depend on the differential input and the gain. In the standard three op amp circuit, the input common-mode signal must be kept below the maximum output voltage of the input amplifier minus 1/2 the final output voltage. If, for example, these amplifiers can swing ±12V, then to get 12V at the output you must restrict the input common-mode voltage to only 6V. The circuitry of the PGA202/203 is such that the common-mode input range applies to either input pin regardless of the output voltage.

OUTPUT SENSE

An output sense has been provided to allow greater accuracy in connecting the load. By attaching this feedback point to the load at the load site, IR drops due to the load currents are eliminated since they are inside the feedback loop. Proper connection is shown in Figure 1. When more current is required, a power booster can be placed in the feedback loop as shown in Figure 4. Buffer errors are minimized by the loop gain of the output amplifier.

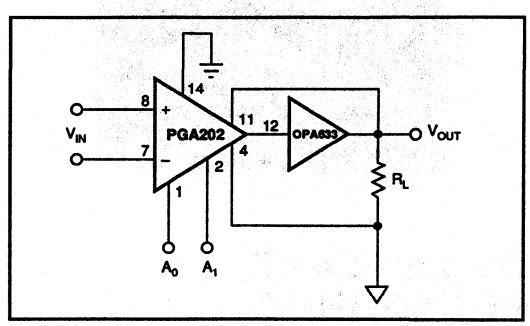


FIGURE 4. Current Boosting the Output.

OUTPUT FILTERING

The summing nodes of the output amplifier have also been made available to allow for output filtering. By placing matched capacitors in parallel with the existing internal capacitors as shown in Figure 5, you can lower the frequency response of the output amplifier. This will reduce the noise of the amplifier, at the cost of a slower response. The nominal frequency responses for some selected values of capacitor are shown in Table III.

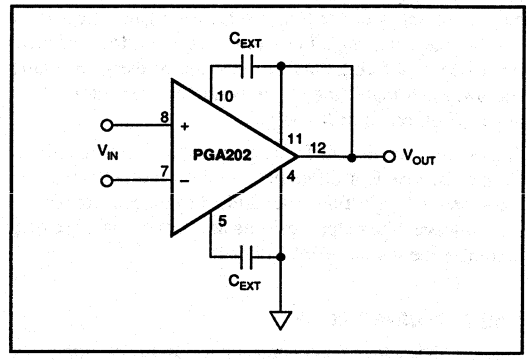


FIGURE 5. Output Filtering.

CUTOFF FREQUENCY	C_1 AND C_2
1MHz	None
100kHz	47pF
10kHz	525pF

TABLE III. Output Frequency vs Filter Capacitors.

INPUT CHARACTERISTICS

Because the PGA202/203 have FET inputs, the bias currents drawn through input source resistors have a negligible effect on DC accuracy. The picoamp currents produce no more than microvolts through megohm sources. The inputs are also internally diode clamped to the supplies. Thus, input filtering and input series protection are easily achievable.

A return path for the input bias currents must always be provided to prevent the charging of any stray capacitance. Otherwise the amplifier could wander and saturate. A 1MΩ to 10MΩ resistor from the input to common will return floating sources such as thermocouples and AC-coupled inputs (see Applications Section, Figures 8 and 9.)

DYNAMIC PERFORMANCE

The PGA202 and the PGA203 are fast-settling FET input programmable gain instrumentation amplifiers. Careful attention to minimize stray capacitance is necessary to achieve specified performance. High source resistance will interact with the input capacitance to reduce speed and overall bandwidth. Also, to maintain stability, avoid capacitance from the output to the input or the offset adjust pins.

Applications with balanced source impedance will provide the best performance. In some applications, mismatched source impedances may be required. If the impedance in the negative input exceeds that in the positive input, stray capacitance from the output will create a net negative feedback and improve the stability of the circuit. If, however, the impedance in the positive input is greater, then the feedback due to stray capacitance will be positive and instability may result. The degree of positive feedback will, of course, depend on the source impedance imbalance as well as the board layout and the operating gain. The addition of a small bypass capacitor of about 5 to 50pF directly across the input terminals of the PGIA will generally eliminate any instability arising from these stray capacitances. CMR errors due to the source imbalance will also be reduced by the addition of this capacitor.

The PGA202 and the PGA203 are designed for fast settling in response to changes in either the input voltage or the gain. The bandwidth and the settling times are mostly determined by the output stage and are therefore independent of gain, except at the highest gain of the PGA202 where other factors in the input stage begin to dominate.

APPLICATIONS

In addition to general purpose applications, the PGA202/203 are designed to handle two important and demanding classes of applications: inputs with high source impedances, and rapid scanning data acquisition systems requiring fast settling time. Because the user has access to output sense and output common pins, current sources can also be constructed with a minimum of external components. Some basic application circuits are shown in Figures 6 through 14.

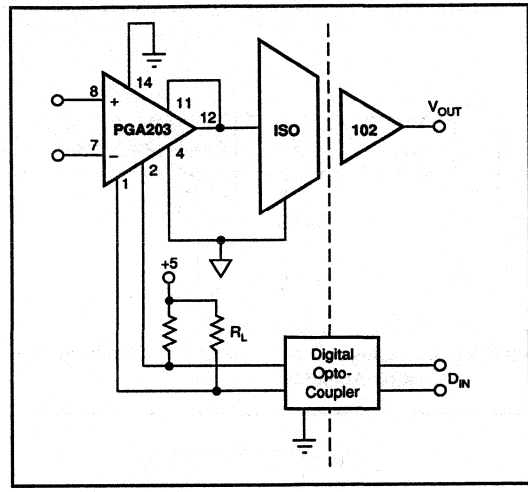


FIGURE 6. Isolated Programmable Gain Instrumentation Amplifier.

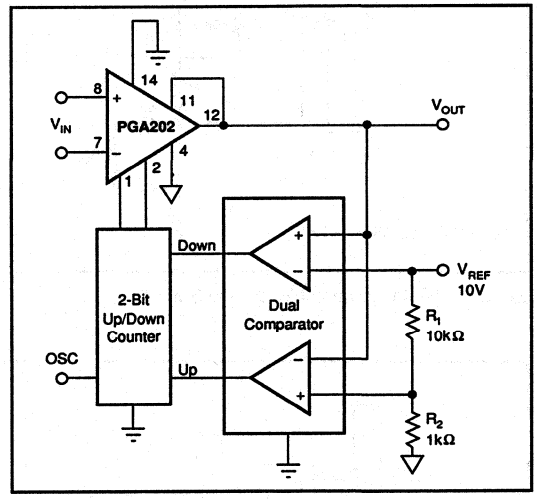


FIGURE 7. Auto Gain Ranging.

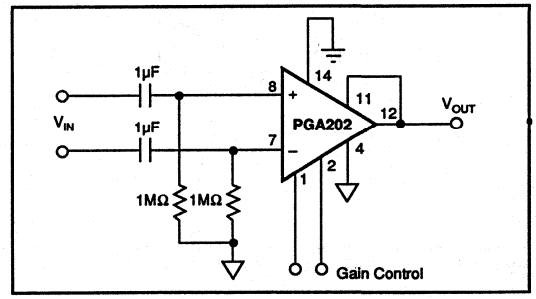


FIGURE 8. AC-Coupled Differential Amplifier for Frequencies above 0.16Hz.

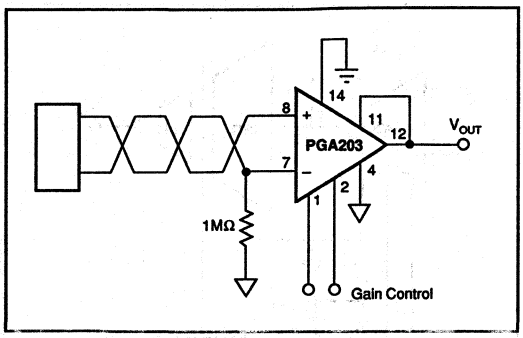


FIGURE 9. Floating Source Programmable Gain Instrumentation Amplifier.

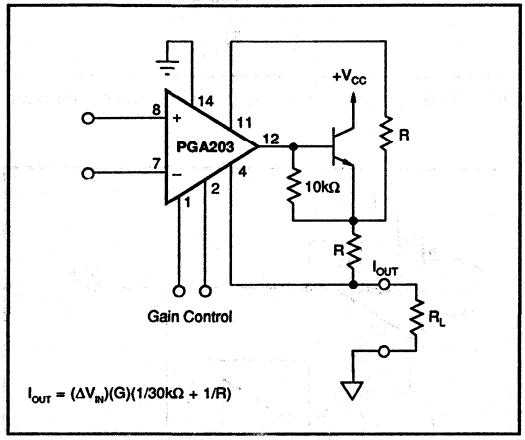


FIGURE 10. Programmable Current Source.

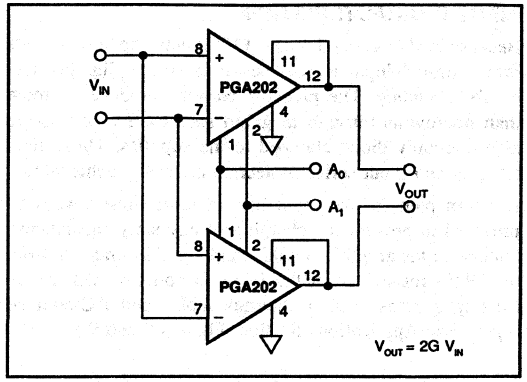


FIGURE 11. Programable Differential In/Differential Out Amplifier.

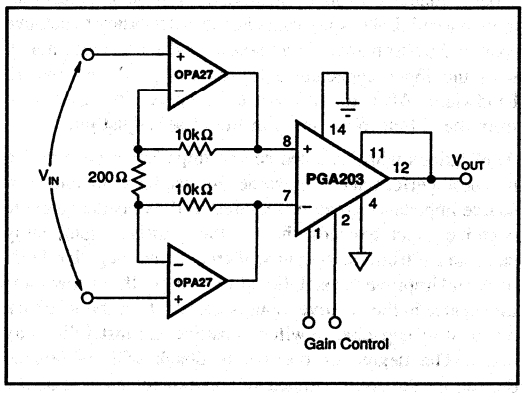
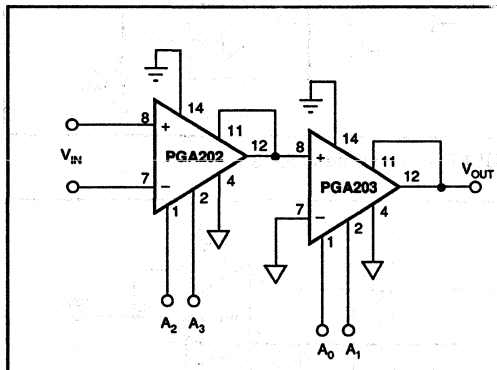


FIGURE 12. Low Noise Differential Amplifier with Gains of 100, 200, 400, 800.



A_3	A_2	A_1	A_0	GAIN
0	0	0	0	1
0	0	0	1	2
0	0	1	0	4
0	0	1	1	8
0	1	0	0	10
0	1	0	1	20
0	1	1	0	40
0	1	1	1	80
1	0	0	0	100
1	0	0	1	200
1	0	1	0	400
1	0	1	1	800
1	1	0	0	1000
1	1	0	1	2000
1	1	1	0	4000
1	1	1	1	8000

FIGURE 13. Cascaded Amplifiers.

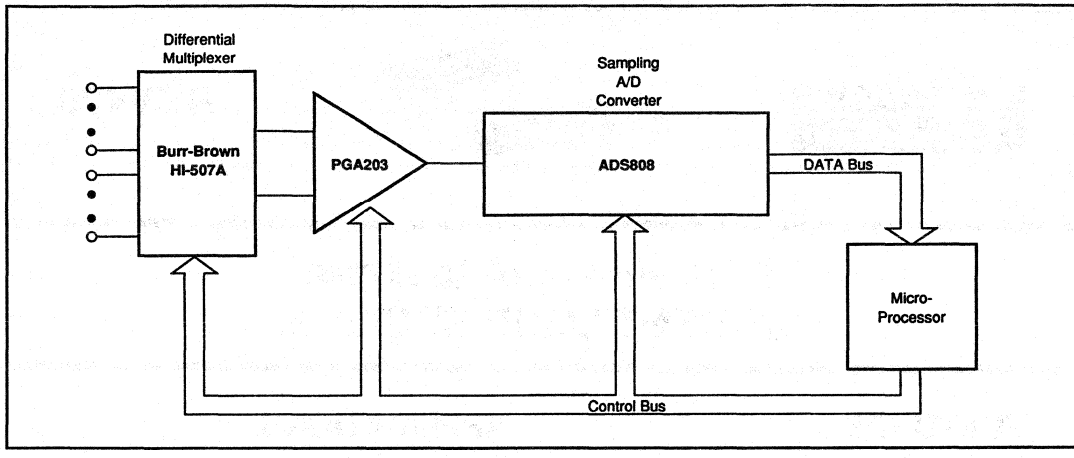


FIGURE 14. 8-Channel Differential Data Acquisition System.

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

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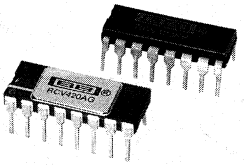


RCV420

Precision 4mA to 20mA CURRENT LOOP RECEIVER

FEATURES

- COMPLETE 4-20mA TO 0-5V CONVERSION
- INTERNAL SENSE RESISTORS
- PRECISION 10V REFERENCE
- BUILT-IN LEVEL-SHIFTING
- ±40V COMMON-MODE INPUT RANGE
- 0.1% OVERALL CONVERSION ACCURACY
- HIGH NOISE IMMUNITY: 86dB CMR

APPLICATIONS

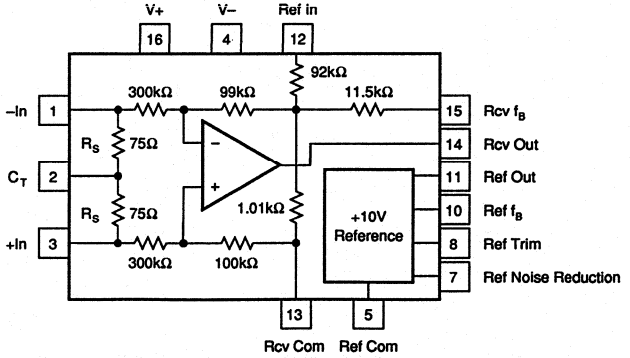
- PROCESS CONTROL
- INDUSTRIAL CONTROL
- FACTORY AUTOMATION
- DATA ACQUISITION
- SCADA
- RTUs
- ESD
- MACHINE MONITORING

DESCRIPTION

The RCV420 is a precision current-loop receiver designed to convert a 4–20mA input signal into a 0–5V output signal. As a monolithic circuit, it offers high reliability at low cost. The circuit consists of a premium grade operational amplifier, an on-chip precision resistor network, and a precision 10V reference. The RCV420 features 0.1% overall conversion accuracy, 86dB CMR, and ±40V common-mode input range.

The circuit introduces only a 1.5V drop at full scale, which is useful in loops containing extra instrument burdens or in intrinsically safe applications where transmitter compliance voltage is at a premium. The 10V reference provides a precise 10V output with a typical drift of 5ppm/°C.

The RCV420 is completely self-contained and offers a highly versatile function. No adjustments are needed for gain, offset, or CMR. This provides three important advantages over discrete, board-level designs: 1) lower initial design cost, 2) lower manufacturing cost, and 3) easy, cost-effective field repair of a precision circuit.



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Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 741-4395 • Immediate Product Info: (800) 548-6132

PDS-837C

SPECIFICATIONS

ELECTRICAL

T = +25°C and V_S = ±15V unless otherwise noted.

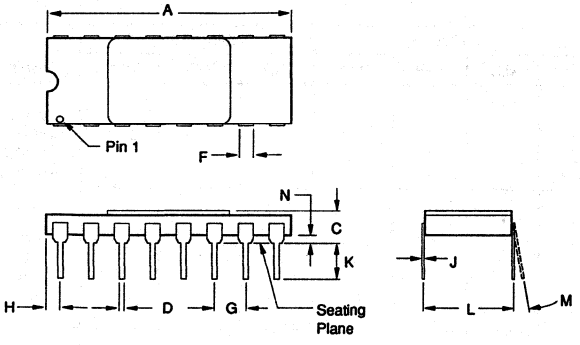
CHARACTERISTICS	RCV420AG			RCV420BG			RCV420KP			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
GAIN										
Initial		0.3125			•			•		V/mA
Error		0.025	0.1		•	0.05		0.05	0.15	% of span
vs Temp		15	50		•	25		•		ppm/°C
Nonlinearity[1]		0.0002	0.002		•	•		•	•	% of span
OUTPUT										
Rated Voltage (I_O = +10mA, –5mA)	10	12		•	•		•	•		V
Rated Current (E_O = 10V)	+10, –5			•			•			mA
Impedance (Differential)		0.01			•			•		Ω
Current Limit (To Common)		+49, –13			•			•		mA
Capacitive Load (Stable Operation)		1000			•			•		pF
INPUT										
Sense Resistance	74.25	75	75.75	•	•	•	•	•	•	Ω
Input Impedance (Common Mode)		200			•			•		kΩ
Common Mode Voltage			±40			•			•	V
CMR[2]	72	80		86	94		70	•		dB
vs Temp (DC) (T_A = T_{MIN} to T_{MAX})	66	76		80	90			•		dB
AC 60Hz		80			94			•		dB
OFFSET VOLTAGE (RTO) [3]										
Initial			1			•			•	mV
vs Temp		10	50		•	25		•		µV/°C
vs Supply (±11.4V to ±18V)	74	90		80	•		•	•		dB
vs Time		200			•			•		µV/mo
ZERO ERROR[4]										
Initial		0.01	0.05		•	0.025		0.025	0.075	% of span
vs Temp		10	50		•	25		•		ppm of span/°C
OUTPUT NOISE VOLTAGE										
f_B = 0.1Hz to 10Hz		50			•			•		µVp-p
f_O = 10kHz		800			•			•		nV/√Hz
DYNAMIC RESPONSE										
Gain Bandwidth		150			•			•		kHz
Full Power Bandwidth		30			•			•		kHz
Slew Rate		1.5			•			•		V/µs
Settling Time (0.01%)		10			•			•		µs
VOLTAGE REFERENCE										
Initial	9.995		10.005	•		•	9.99		10.01	V
Trim Range[5]		±4			•			•		%
vs Temp[6]		5	20		•	•		•		ppm/°C
vs Supply (±11.4V to ±18V)		0.0002			•			•		%/V
vs Output Current (I_O = 0 to +10mA)		0.0002			•			•		%/mA
vs Time		15			•			•		ppm/kHr
Noise (0.1Hz to 10Hz)		5			•			•		µVp-p
Output Current	+10, –2			•			•			mA
POWER SUPPLY										
Rated		±15			•			•		V
Voltage Range[7]	–5, +11.4		±18	•		•	•		•	V
Quiescent Current (V_O = 0V)		3	4		•	•		•	•	mA
TEMPERATURE RANGE										
Specification	–25		+85	•		•	0		+70	°C
Operation	–55		+125	•		•	–25		+85	°C
Storage	–65		+150	•		•	–40		+85	°C

*Specification same as RCV420AG.

NOTES: (1) Nonlinearity is the max peak deviation from best fit straight line. (2) With 0 source impedance on Rcv Com pin. (3) Referred to output with all inputs grounded including Ref In. (4) With 4mA input signal and Voltage Reference connected (includes V_{OS}, Gain Error, and Voltage Reference Errors). (5) External trim slightly affects drift. (6) The "box method" is used to specify output voltage drift vs temperature. (7) I_O Ref = 5mA, I_O Rcv = 2mA.

MECHANICAL

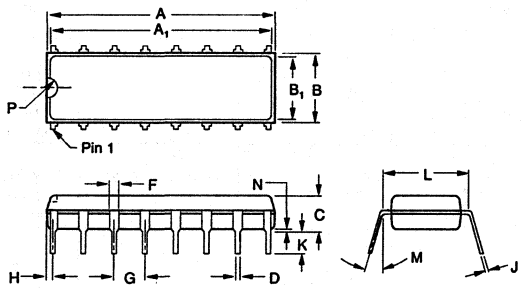
G Package — 16-Pin Hermetic DIP



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.790	.810	20.07	20.57
C	.105	.170	2.67	4.32
D	.015	.021	0.38	0.53
F	.048	.060	1.22	1.52
G	.100 BASIC		2.54 BASIC	
H	.030	.070	0.76	1.78
J	.008	.012	0.20	0.30
K	.120	.240	3.05	6.10
L	.300 BASIC		7.62 BASIC	
M	—	10°	—	10°
N	.025	.060	0.64	1.52

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.

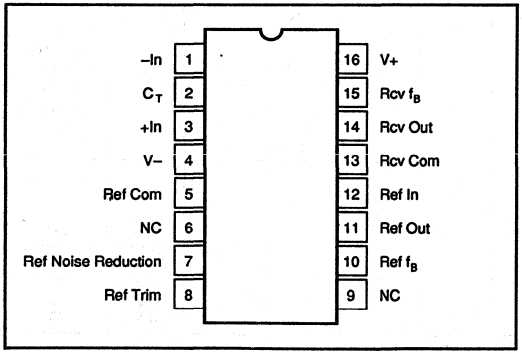
P Package — 16-Pin Plastic DIP



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.740	.800	18.80	20.32
A_1	.725	.785	18.42	19.94
B	.230	.290	5.85	7.38
B_1	.200	.250	5.09	6.36
C	.120	.200	3.05	5.09
D	.015	.023	0.38	0.59
F	.030	.070	0.76	1.78
G	.100 BASIC		2.54 BASIC	
H	0.20	.050	0.51	1.27
J	.008	.015	0.20	0.38
K	.070	.150	1.78	3.82
L	.300 BASIC		7.63 BASIC	
M	0°	15°	0°	15°
N	.010	.030	0.25	0.76
P	.025	.050	0.64	1.27

NOTE: Leads in true position within 0.010" (0.25mm) R at MMC at seating plane.

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Supply	±22V
Input Current, Continuous	40mA
Input Current Momentary, 0.1s	250mA, 1% Duty Cycle
Common Mode Input Voltage, Continuous	±40V
Lead Temperature (soldering, 10s)	+300°C
Output Short Circuit to Common (Rcv and Ref)	Continuous

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

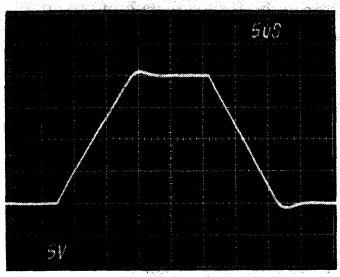
ORDERING INFORMATION

MODEL	PERFORMANCE GRADE	PACKAGE
RCV420AG	–25°C to +85°C	16-Pin Hermetic DIP
RCV420BG	–25°C to +85°C	16-Pin Hermetic DIP
RCV420KP	0°C to +70°C	16-Pin Plastic DIP

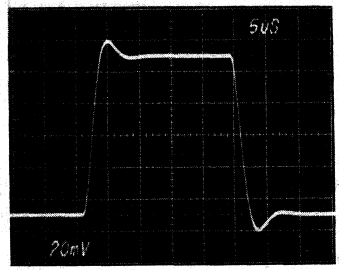
TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_S = ±15V unless otherwise noted.

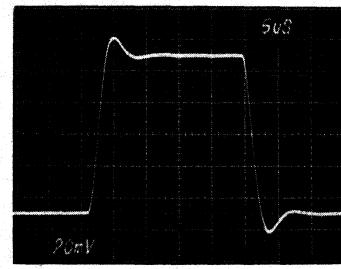
STEP RESPONSE
NO LOAD



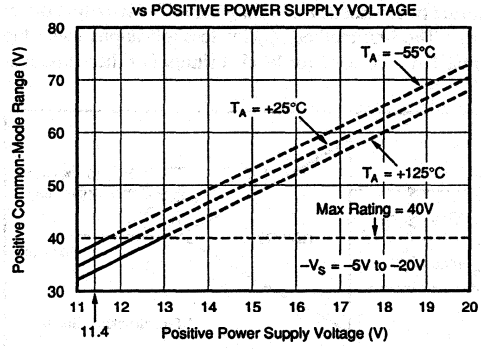
SMALL SIGNAL RESPONSE
NO LOAD



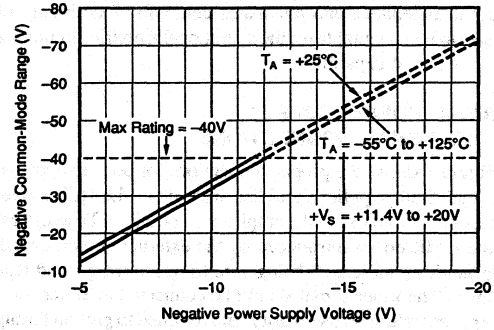
SMALL SIGNAL RESPONSE
R_L = ∞, C_L = 1000pF



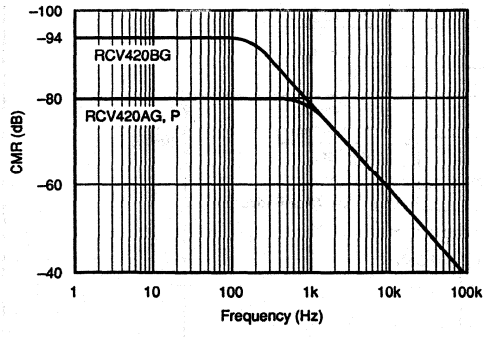
POSITIVE COMMON-MODE VOLTAGE RANGE
vs POSITIVE POWER SUPPLY VOLTAGE



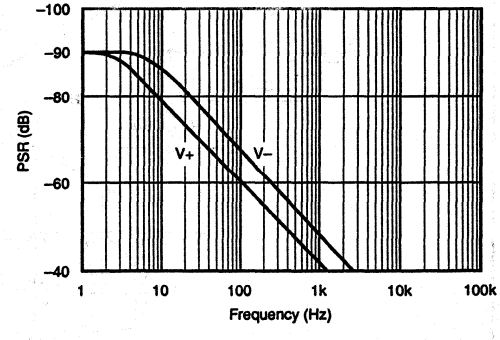
NEGATIVE COMMON-MODE VOLTAGE RANGE
vs NEGATIVE POWER SUPPLY VOLTAGE



COMMON-MODE REJECTION
vs FREQUENCY



POWER-SUPPLY REJECTION
vs FREQUENCY



THEORY OF OPERATION

Refer to the figure on the first page. For 0–5V output with 4–20mA input, the required transimpedance of the circuit is:

$$V_{OUT}/I_{IN} = 5V/16mA = 0.3125V/mA.$$

To achieve the desired output levels, 0V for 4mA and 5V for 20mA, the output of the amplifier must be offset by an amount:

$$V_{OS} = -(4mA)(0.3125V/mA) = -1.25V.$$

The input current signal is connected to either +In or –In, depending on the polarity of the signal, and returned to ground through the center tap, C_T. The balanced input—two matched 75Ω sense resistors, R_S—provides maximum rejection of common-mode voltage signals on C_T and true differential current-to-voltage conversion. The sense resistors convert the input current signal into a proportional voltage, which is amplified by the differential amplifier. The voltage gain of the amplifier is:

$$A_D = 5V/(16mA)(75\Omega) = 4.1667V/V.$$

The tee network in the feedback path of the amplifier provides a summing junction used to generate the required –1.25V offset voltage. The input resistor network provides high-input impedance and attenuates common-mode input voltages to levels suitable for the operational amplifier's common-mode signal capabilities.

BASIC POWER SUPPLY AND SIGNAL CONNECTIONS

Figure 1 shows the proper connections for power supply and signal. Both supplies should be decoupled with 1µF tantalum capacitors as close to the amplifier as possible. To avoid gain and CMR errors introduced by the external circuit, connect grounds as indicated, being sure to minimize ground resistance. The input signal should be connected to either +In or –In, depending on its polarity, and returned to ground through the center tap, C_T. The output of the voltage reference, Ref Out, should be connected to Ref In for the necessary level shifting. If the Ref In pin is not used for level shifting, then it must be grounded to maintain high CMR.

GAIN AND OFFSET ADJUSTMENT

Figure 2 shows the circuit for adjusting the RCV420 gain. Increasing the gain of the RCV420 is accomplished by inserting a small resistor in the feedback path of the amplifier. Increasing the gain using this technique results in CMR degradation, and therefore, gain adjustments should be kept as small as possible. For example, a 1% increase in gain is typically realized with a 125Ω resistor, which degrades CMR by about 6dB.

A decrease in gain can be achieved by placing matched resistors in parallel with the sense resistors, also shown in Figure 2. The adjusted gain is given by the following expression

$$V_{OUT}/I_{IN} = 0.3125 \times R_X/(R_X + R_S).$$

A 1% decrease in gain can be achieved with a 7.5kΩ resistor. It is important to match the parallel resistance on each sense resistor to maintain high CMR. The TCR mismatch between the two external resistors will effect gain error drift and CMR drift.

There are two methods for nulling the RCV420 output offset voltage. The first method applies to applications using the internal 10V reference for level shifting. For these applica-

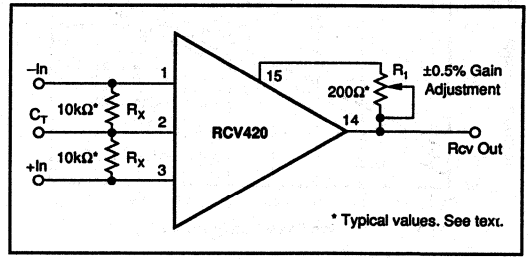


FIGURE 2. Optional Gain Adjustment.

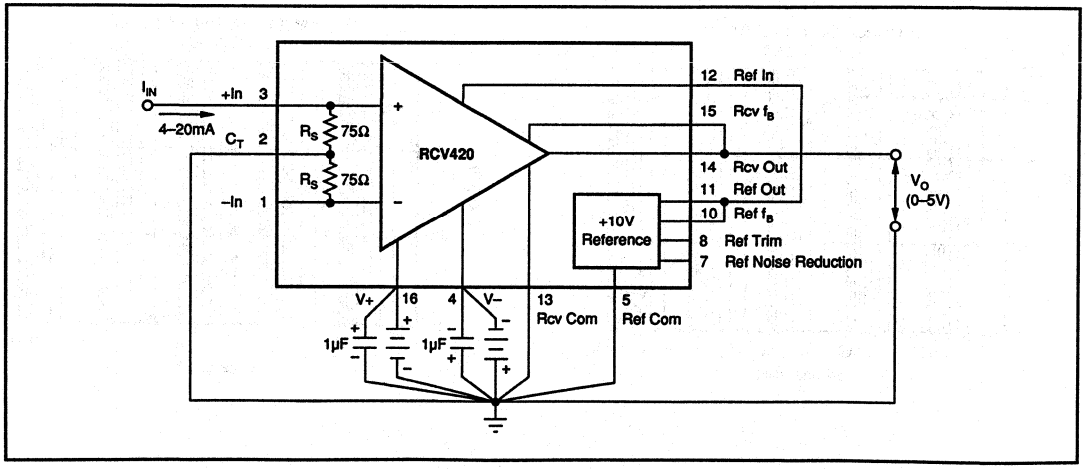


FIGURE 1. Basic Power Supply and Signal Connections.

tions, the voltage reference output trim procedure can be used to null offset errors at the output of the RCV420. The voltage reference trim circuit is discussed under "Voltage Reference."

When the voltage reference is not used for level shifting or when large offset adjustments are required, the circuit in Figure 3 can be used for offset adjustment. A low impedance on the Rcv Com pin is required to maintain high CMR.

ZERO ADJUSTMENT

Level shifting the RCV420 output voltage can be achieved using either the Ref In pin or the Rcv Com pin. The disadvantage of using the Ref In pin is that there is an 8:1 voltage attenuation from this pin to the output of the RCV420. Thus, use the Rcv Com pin for large offsets, because the voltage on this pin is seen directly at the output. Figure 4 shows the circuit used to level-shift the output of the RCV420 using the Rcv Com pin. It is important to use a low-output impedance amplifier to maintain high CMR. With this method of zero adjustment, the Ref In pin must be connected to the Rcv Com pin.

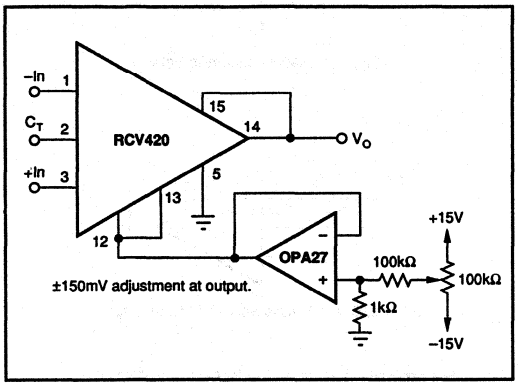


FIGURE 3. Optional Output Offset Nulling Using External Amplifier.

MAINTAINING COMMON-MODE REJECTION

Two factors are important in maintaining high CMR: (1) resistor matching and tracking (the internal resistor network does this) and (2) source impedance. CMR depends on the accurate matching of several resistor ratios. The high accuracies needed to maintain the specified CMR and CMR temperature coefficient are difficult and expensive to reliably achieve with discrete components. Any resistance imbalance introduced by external circuitry directly affects CMR. These imbalances can occur by: mismatching sense resistors when gain is decreased, adding resistance in the feedback path when gain is increased, and adding series resistance on the Rcv Com pin.

The two sense resistors are laser-trimmed to typically match within 0.01%; therefore, when adding parallel resistance to decrease gain, take care to match the parallel resistance on each sense resistor. To maintain high CMR when increasing the gain of the RCV420, keep the series resistance added to the feedback network as small as possible. Whether the Rcv Com pin is grounded or connected to a voltage reference for level shifting, keep the series resistance on this pin as low as possible. For example, a resistance of 20Ω on this pin degrades CMR from 86dB to approximately 80dB. For applications requiring better than 86dB CMR, the circuit shown in Figure 5 can be used to adjust CMR.

PROTECTING THE SENSE RESISTOR

The 75Ω sense resistors are designed for a maximum continuous current of 40mA, but can withstand as much as 250mA for up to 0.1s (see absolute maximum ratings). There are several ways to protect the sense resistor from overcur-

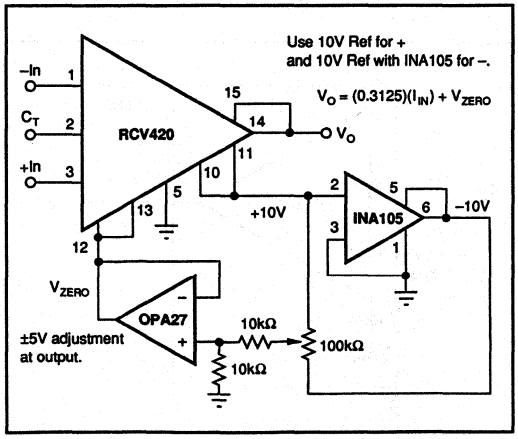


FIGURE 4. Optional Zero Adjust Circuit.

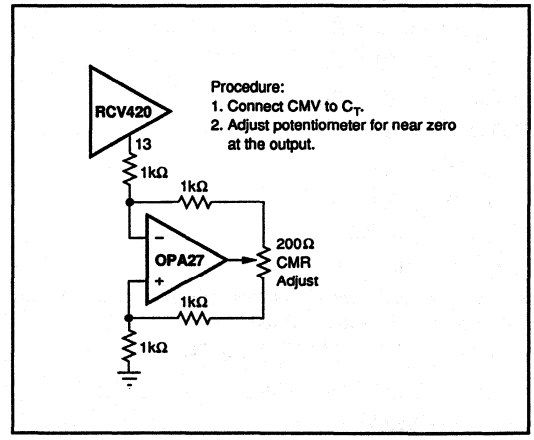


FIGURE 5. Optional Circuit for Externally Trimming CMR.

rent conditions exceeding these specifications. Refer to Figure 6. The simplest and least expensive method is a resistor as shown in Figure 6a. The value of the resistor is determined from the expression

$$R_X = V_{CC}/40mA - 75\Omega$$

and the full scale voltage drop is

$$V_{RX} = 20mA \times R_X.$$

For a system operating off of a 32V supply $R_X = 725\Omega$ and $V_{RX} = 14.5V$. In applications that cannot tolerate such a large voltage drop, use circuits 6b or 6c. In circuit 6b a power JFET and source resistor are used as a current limit. The 200Ω potentiometer, R_X, is adjusted to provide a current limit of approximately 30mA. This circuit introduces a 1–4V drop at full scale. If only a very small series voltage drop at full scale can be tolerated, then a 0.032A series 217 fast-acting fuse should be used, as shown in Figure 6c.

For automatic fold-back protection, use the circuit shown in Figure 19.

RESISTOR NOISE IN THE RCV420

The output voltage noise of the RCV420 is dominated by the thermal noise generated in the resistor network. Figure 7 shows the model for calculating resistor noise in the RCV420. The expression for resistor noise is:

$$e_N(rms) = \sqrt{2\pi KTRB}$$

where: K = Boltzman's constant (J/°K)

T = Absolute temperature (°K)

R = Resistance (Ω)

B = Bandwidth (Hz)

At room temperature, this noise becomes:

$$e_N = 1.3 \times 10^{-10} \sqrt{R} \quad (V/\sqrt{Hz})$$

The four noise sources in Figure 7 are:

$$e_{N1} = 1.3 \times 10^{-10} \sqrt{R_1}$$

$$e_{N2} = 1.3 \times 10^{-10} \sqrt{R_5}$$

$$e_{N3} = 1.3 \times 10^{-10} \sqrt{R_3}$$

$$e_{N4} = 1.3 \times 10^{-10} \sqrt{R_6}$$

Referred to output,

$$e_{NO1} = e_{N1}(A_D)$$

$$e_{NO2} = e_{N2}(A_D)$$

$$e_{NO3} = e_{N3}(R_4/R_3)$$

$$e_{NO4} = e_{N4}[(R_5 + R_6)/R_5](A_D)$$

where A_D is the differential voltage gain of amplifier. Adding as the root of the sums squared:

$$e_{NO} = \sqrt{(e_{NO1}^2 + e_{NO2}^2 + e_{NO3}^2 + e_{NO4}^2)}$$

e_{NO} at a 150kHz bandwidth

= 0.35mVrms

= 2.1mVp-p with a crest factor of 6 (statistically includes 99.7% of all noise peak occurrences).

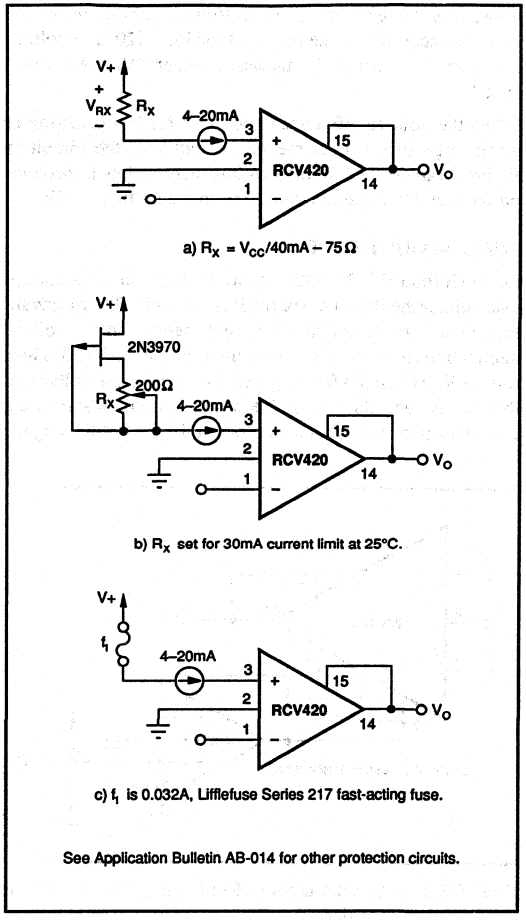


FIGURE 6. Protecting the Sense Resistors with a) Resistor, b) JFET, c) Fuse.

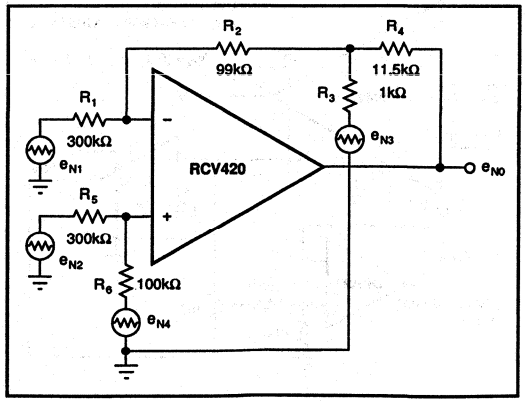


FIGURE 7. Resistor Noise Model.

VOLTAGE REFERENCE

The RCV420 contains a precision 10V reference. Figure 8 shows the circuit for output voltage adjustment. Trimming the output will change the voltage drift by approximately 0.007ppm/°C per mV of trimmed voltage. Any mismatch in TCR between the two sides of the potentiometer will also affect drift, but the effect is divided by approximately 5. The trim range of the voltage reference using this method is typically ±400mV. The voltage reference trim can be used to trim offset errors at the output of the RCV420. There is an 8:1 voltage attenuation from Ref In to RCV Out, and thus the trim range at the output of the receiver is typically ±50mV. The high-frequency noise (to 1MHz) of the voltage reference is typically 1mVp-p. When the voltage reference is used for level shifting, its noise contribution at the output of the receiver is typically 125µVp-p due to the 8:1 attenuation from Ref In to RCV Out. The reference noise can be reduced by connecting an external capacitor between the Noise Reduction pin and ground. For example, a 0.1µF capacitor reduces the high-frequency noise to about 200µVp-p at the output of the reference and about 25µVp-p at the output of the receiver.

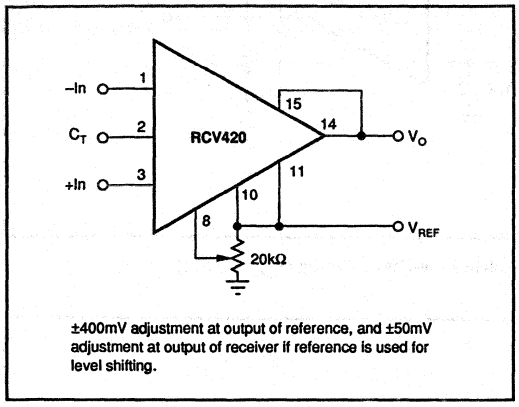


FIGURE 8. Optional Voltage Reference External Trim Circuit.

APPLICATIONS

The RCV420 is ideally suited for applications requiring precise current-to-voltage conversion and high CMR. The following figures show several typical application circuits.

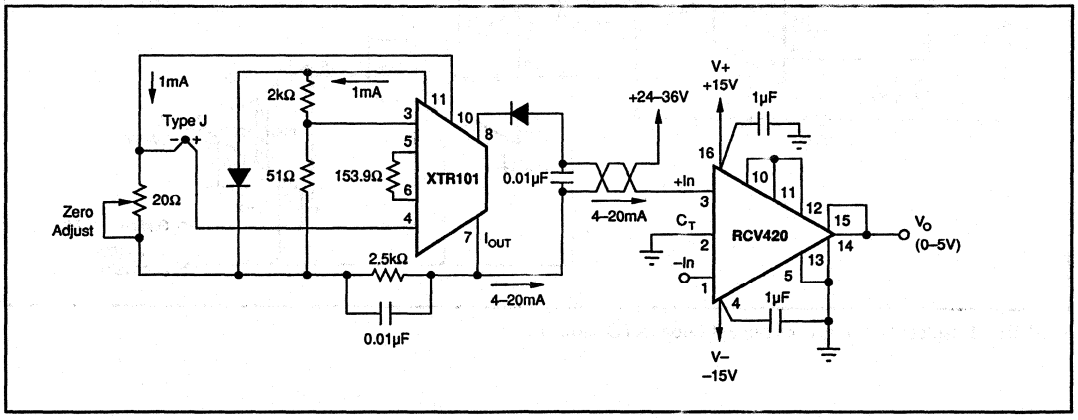


FIGURE 9. RCV420 Used in Conjunction with XTR101 to Form a Complete Solution for 4–20mA Loop.

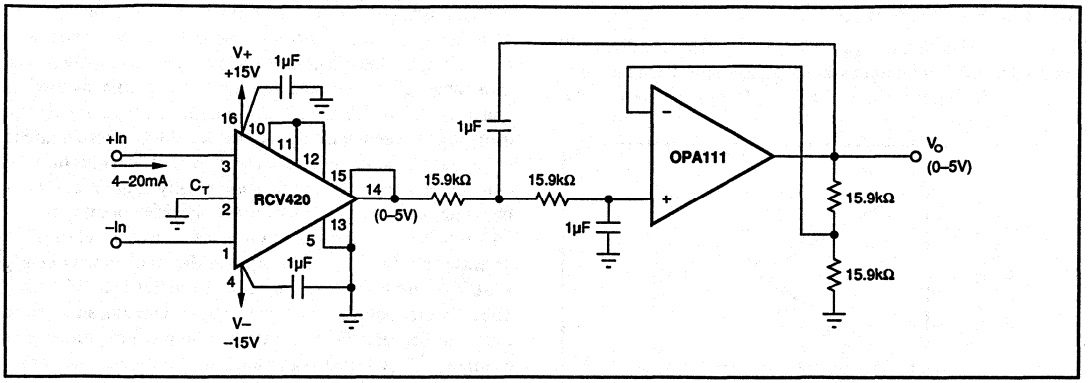


FIGURE 10. 4–20mA to 0-10V Conversion With Second-Order Active Low-Pass Filtering (f_{-3dB} = 10Hz).

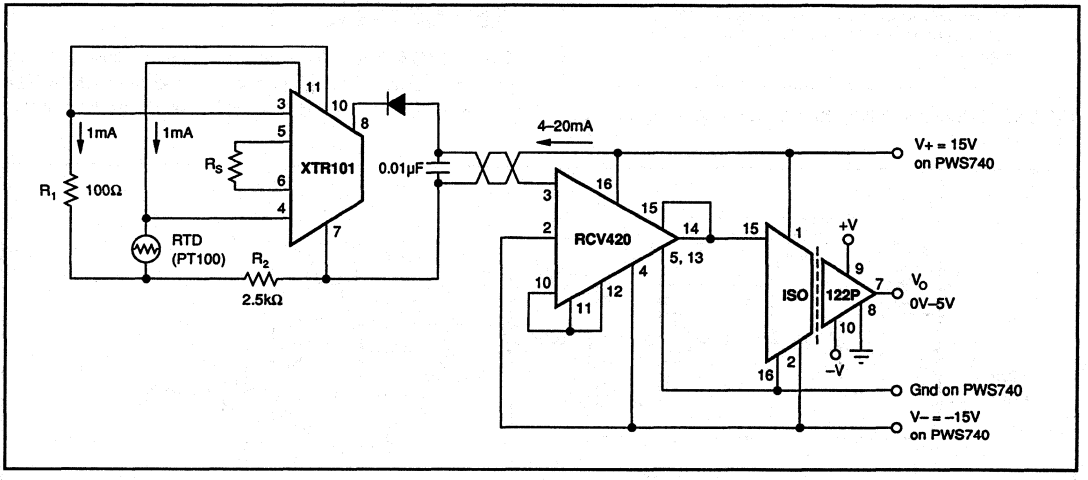
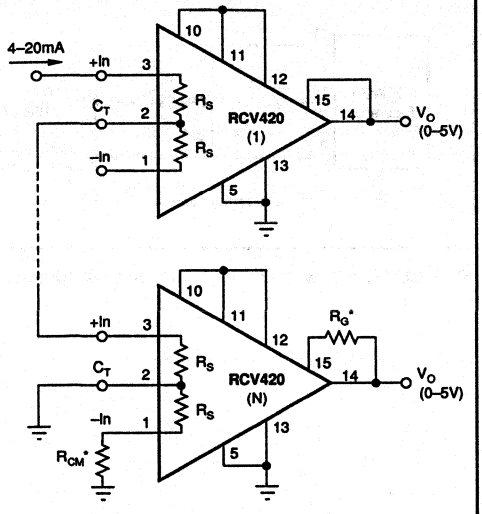


FIGURE 11. Isolated 4–20mA Instrument Loop (RTD shown).



*R_{CM} and R_G are used to provide a first order correction of CMR and Gain Error, respectively. Table 1 gives typical resistor values for R_{CM} and R_G when as many as three RCV420s are stacked. Table 2 gives typical CMR and Gain Error with no correction. Further improvement in CMR and Gain Error can be achieved using a 500kΩ potentiometer for R_{CM} and a 100Ω potentiometer for R_G.

RCV420	R_{CM} (kΩ)	R_G (Ω)
1	∞	0
2	200	7
3	67	23

TABLE 1. Typical Values for R_{CM} and R_G.

RCV420	CMR (dB)	GAIN ERROR %
1	94	0.025
2	68	0.075
3	62	0.200

TABLE 2. Typical CMR and Gain Error Without Correction.

FIGURE 12. Series 4–20mA Receivers.

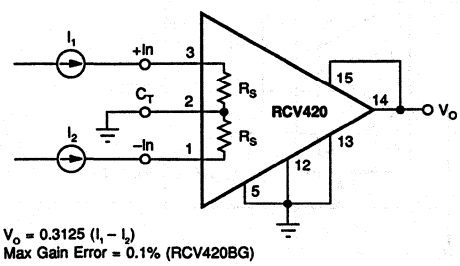


FIGURE 13. Differential Current-to-Voltage Converter.

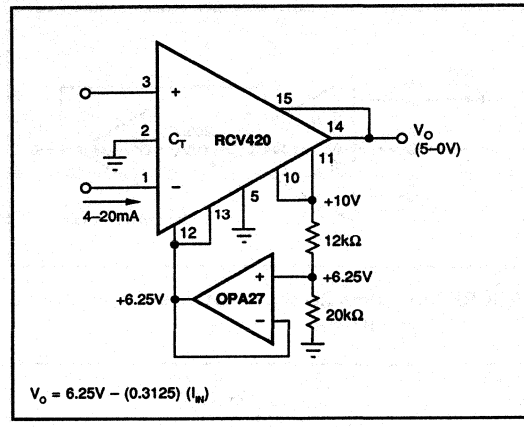


FIGURE 14. 4–20mA to 5–0V Conversion.

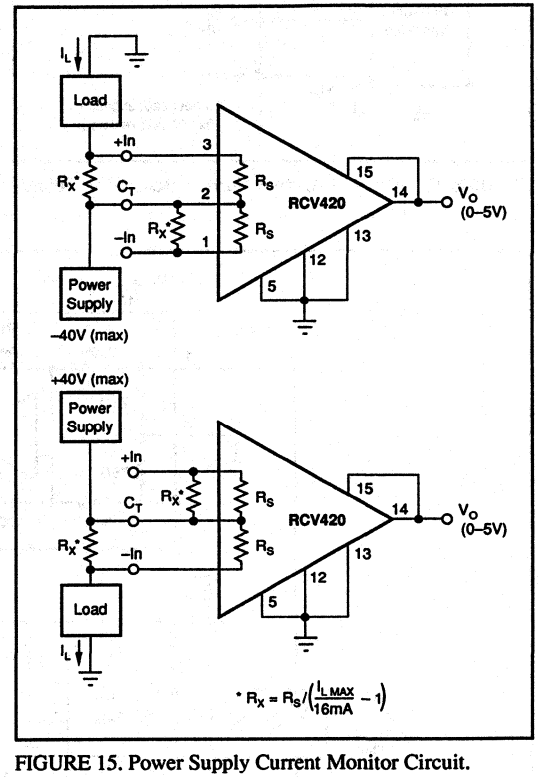


FIGURE 15. Power Supply Current Monitor Circuit.

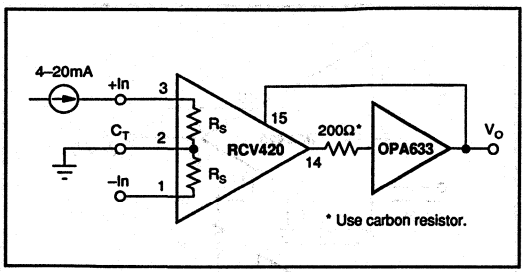


FIGURE 16. 4–20mA Receiver with Output Current Boosted to ±100mA.

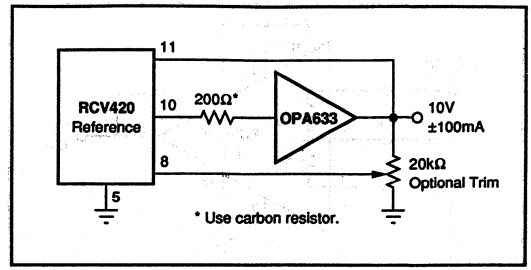


FIGURE 18. 10V with Output to Source/Sink 100mA.

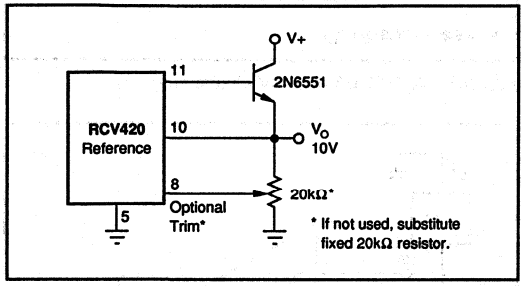


FIGURE 17. 10V with Output Current Boosted to 100mA max.

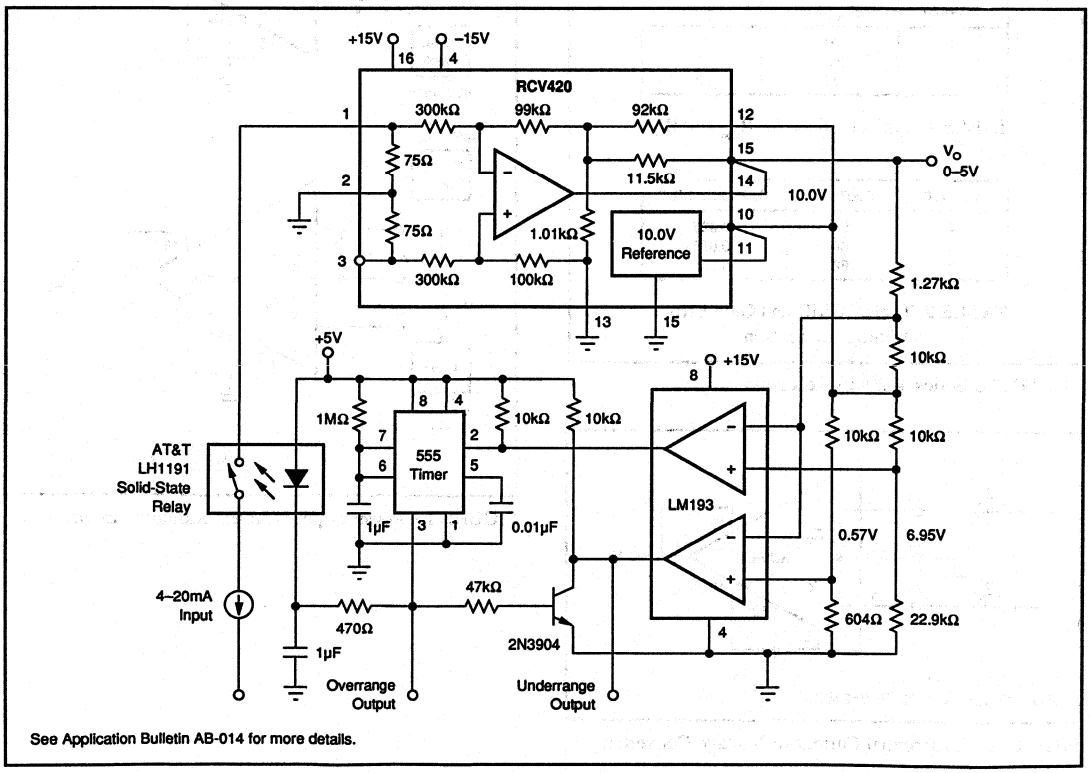


FIGURE 19. 4-20mA Current Loop Receiver with Input Overload Protection.

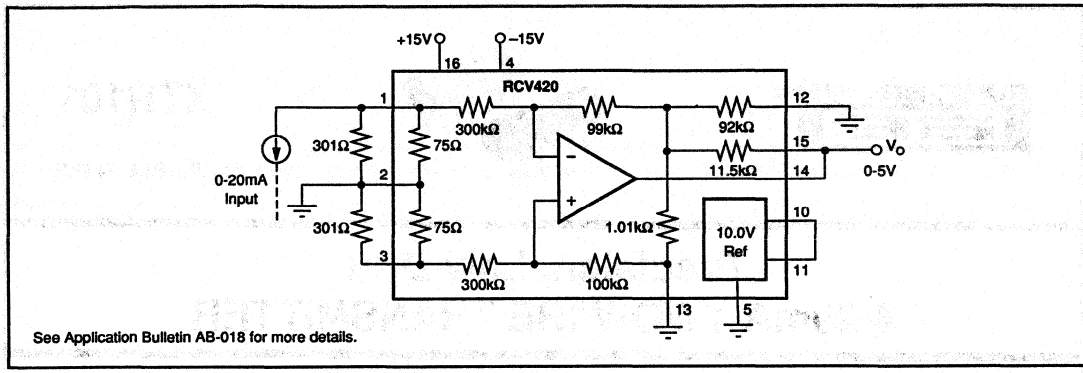


FIGURE 20. 0-20mA/0-5V Receiver Using RCV420.

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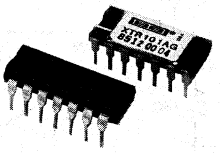


XTR101

AVAILABLE IN DIE

Precision, Low Drift 4-20mA TWO-WIRE TRANSMITTER

FEATURES

- **INSTRUMENTATION AMPLIFIER INPUT**
  Low Offset Voltage, 30µV max
  Low Voltage Drift, 0.75µV/°C max
  Low Nonlinearity, 0.01% max
- **TRUE TWO-WIRE OPERATION**
  Power and Signal on One Wire Pair
  Current Mode Signal Transmission
  High Noise Immunity
- **DUAL MATCHED CURRENT SOURCES**
- **WIDE SUPPLY RANGE, 11.6V to 40V**
- **–40°C to +85°C SPECIFICATION RANGE**
- **SMALL 14-PIN DIP PACKAGE, CERAMIC AND PLASTIC**

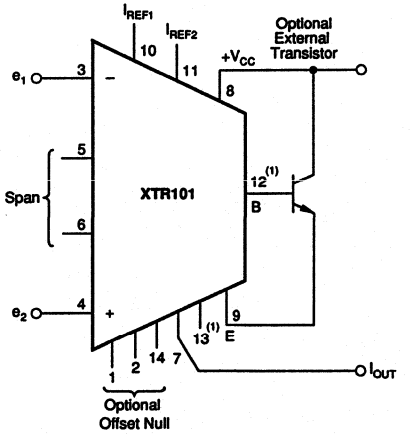
APPLICATIONS

- **INDUSTRIAL PROCESS CONTROL**
  Pressure Transmitters
  Temperature Transmitters
  Millivolt Transmitters
- **RESISTANCE BRIDGE INPUTS**
- **THERMOCOUPLE INPUTS**
- **RTD INPUTS**
- **CURRENT SHUNT (mV) INPUTS**
- **PRECISION DUAL CURRENT SOURCES**
- **AUTOMATED MANUFACTURING**
- **POWER/PLANT ENERGY SYSTEM MONITORING**

DESCRIPTION

The XTR101 is a microcircuit, 4-20mA, two-wire transmitter containing a high accuracy instrumentation amplifier (IA), a voltage-controlled output current source, and dual-matched precision current reference. This combination is ideally suited for remote signal conditioning of a wide variety of transducers such as thermocouples, RTDs, thermistors, and strain gauge bridges. State-of-the-art design and laser-trimming, wide temperature range operation and small size make it very suitable for industrial process control applications. In addition, the optional external transistor allows even higher precision.

The two-wire transmitter allows signal and power to be supplied on a single wire-pair by modulating the power supply current with the input signal source. The transmitter is immune to voltage drops from long runs and noise from motors, relays, actuators, switches, transformers, and industrial equipment. It can be used by OEMs producing transmitter modules or by data acquisition system manufacturers.



NOTE: (1) Pins 12 and 13 are used for optional BW control.

International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

PDS-627D

SPECIFICATIONS

ELECTRICAL

At T_A = +25°C, $+V_{CC}$ = 24VDC, R_L = 100Ω with external transistor connected, unless otherwise noted

PARAMETER	CONDITIONS	XTR101AG MIN	XTR101AG TYP	XTR101AG MAX	XTR101BG MIN	XTR101BG TYP	XTR101BG MAX	XTR101AP MIN	XTR101AP TYP	XTR101AP MAX	XTR101AU MIN	XTR101AU TYP	XTR101AU MAX	UNITS
OUTPUT AND LOAD CHARACTERISTICS														
Current	Linear Operating Region	4		20	*		*	*		*	*		*	mA
	Derated Performance	3.8		22	*		*	*		*	*		*	mA
Current Limit			28	38		*	*		31	*		31	*	mA
Offset Current Error	I_{OS}, I_O = 4mA		±3.9	±10		±2.5	±6		±8.5	±19		±8.5	±19	µA
vs Temperature	$\Delta I_{OS}/\Delta T$		±10.5	±20		±8	±15		±10.5	±20		*		ppm, FS/°C
Full Scale Output Current Error	Full Scale = 20mA		±20	±40		±15	±30		±30	±60		±30	±60	µA
Power Supply Voltage	V_{CC}, Pins 7 and 8, Compliance[1]	+11.6		±40	*		*	*		*	*		*	VDC
Load Resistance	At V_{CC} = +24V, I_O = 20mA			600			*			600			*	Ω
	At V_{CC} = +40V, I_O = 20mA			1400			*			1400			*	Ω
SPAN														
Output Current Equation	R_S in Ω, e_1 and e_2 in V					$i_O = 4mA + [0.016Ω + (40/R_S)] (e_2 - e_1)$								
Span Equation	R_S in Ω					$S = [0.016Ω + (40/R_S)]$								A/V
vs Temperature	Excluding TCR of R_S		±30	±100		*	*		*	*		*	*	ppm/°C
Untrimmed Error[2]	ε_{SPAN}	-5	-2.5	0	*	*	*	*	*	*	*	*	*	%
Nonlinearity	$\varepsilon_{NONLINEARITY}$			0.01			*			*			*	%
Hysteresis			0			*			*			*		%
Dead Band			0			*			*			*		%
INPUT CHARACTERISTICS														
Impedance: Differential			0.4 || 3			*			*			*		GΩ || pF
Common-Mode			10 || 3			*			*			*		GΩ || pF
Voltage Range, Full Scale	$\Delta e = (e_2 - e_1)$[3]	0		1	*		*	*		*	*		*	V
Offset Voltage	V_{OS}		±30	±60		±20	±30		*	±100		*	±100	µV
vs Temperature	$\Delta V_{OS}/\Delta T$		±0.75	±1.5		±0.35	±0.75		*	*		*	*	µV/°C
Power Supply Rejection	ΔV_{CC}/PSRR = V_{OS} Error	110	125		*	*		*	122		110	122		dB
Bias Current	I_B		60	150		*	*		*	*		*	*	nA
vs Temperature	$\Delta I_B/\Delta T$		0.30	1		*	*		*	*		*	*	nA/°C
Offset Current	I_{OSI}		10	±30		*	±20		*	*		*	*	nA
vs Temperature	$\Delta I_{OS}/\Delta T$		0.1	0.3		*	*		*	*		*	*	nA/°C
Common-Mode Rejection[4]	DC	90	100		*	*		*	*		*	*		dB
Common-Mode Range	e_1 and e_2 with Respect to Pin 7	4		6	*		*	*		*	*		*	V
CURRENT SOURCES														
Magnitude			1			*			*			*		mA
Accuracy	V_{CC} = 24V, $V_{PIN\ 8} - V_{PIN\ 10\ or\ 11}$ = 19V R_2 = 5kΩ, Fig. 5		±0.06	±0.17		±0.025	±0.075		±0.2	±0.37		±0.2	±0.37	%
vs Temperature			±50	±80		±30	±50		*	*		*	*	ppm/°C
vs V_{CC}			±3			*			*			*		ppm/V
vs Time			±8			*			*			*		ppm/month
Compliance Voltage	With Respect to Pin 7	0		V_{CC} - 3.5	*		*	*		*	*		*	V
Ratio Match	Tracking													
Accuracy	$(1 - I_{REF1}/I_{REF2})$ X 100%		±0.014	±0.06		±0.009	±0.04		±0.031	±0.088		±0.031	±0.088	%
vs Tempeature				±15			10			*			*	ppm/°C
vs V_{CC}			±10			*			*			*		ppm/V
vs Time			±1			*			*			*		ppm/month
Output Impedance		10	20		*	*		*	15		*	15		MΩ
TEMPERATURE RANGE														
Specification		-40		+85	*		*	-40		+85	*		*	°C
Operating		-55		+125	*		*	-40		+85	-40		+85	°C
Storage		-55		+165	*		*	-55		+125	-55		+125	°C

*Same as XTR101AG.

NOTES: (1) See Typical Performance Curves. (2) Span error shown is untrimmed and may be adjusted to zero. (3) e_1 and e_2 are signals on the –In and +In terminals with respect to the output, pin 7. While the maximum permissible Δe is 1V, it is primarily intended for much lower input signal levels, e.g., 10mV or 50mV full scale for the XTR101A and XTR101B grades respectively. 2mV FS is also possible with the B grade, but accuracy will degrade due to possible errors in the low value span resistance and very high amplification of offset, drift, and noise. (4) Offset voltage is trimmed with the application of a 5V common-mode voltage. Thus the associated common-mode error is removed. See Application Information section.

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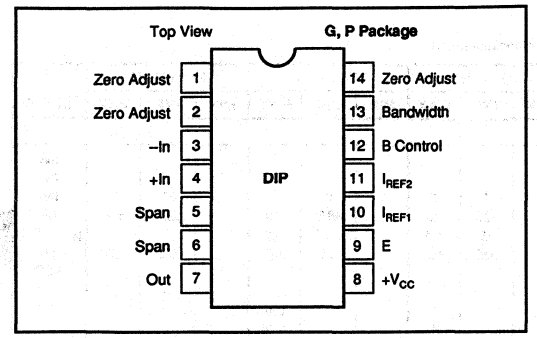
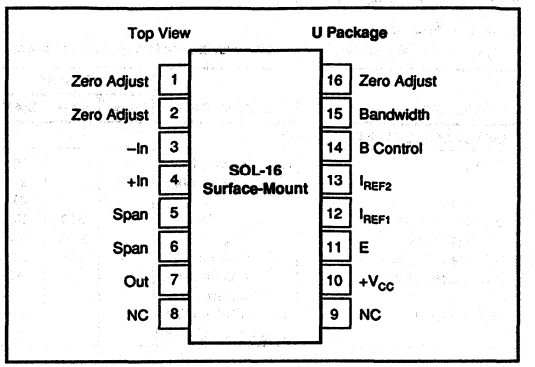
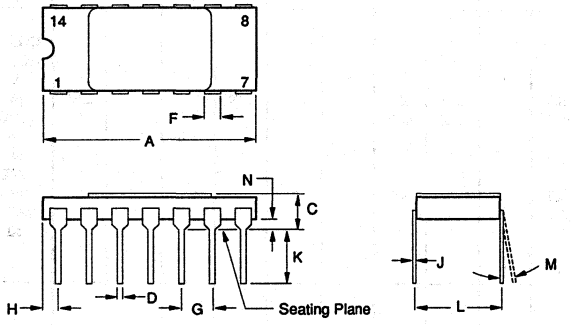
PIN CONFIGURATION





MECHANICAL

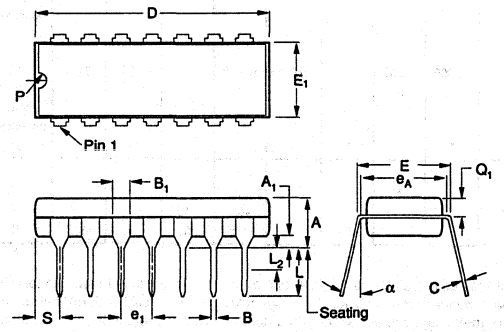
G Package — 14-Pin Ceramic DIP



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	.670	.710	17.02	18.03
C	.065	.170	1.65	4.32
D	.015	.021	0.38	0.53
F	.045	.060	1.14	1.52
G	.100 BASIC		2.54 BASIC	
H	.025	.070	0.64	1.78
J	.008	.012	0.20	0.30
K	.120	.240	3.05	6.10
L	.300 BASIC		7.62 BASIC	
M	—	10°	—	10°
N	.009	.060	0.23	1.52

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.

P Package — 14-Pin Plastic DIP



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	.120	.160	3.048	4.064
A_1	.015	.065	.381	1.651
B	.014	.020	.355	.508
B_1	.050	.065	1.270	1.651
C	.008	.012	.203	.304
D	.745	.770	18.923	19.558
E	.300	.325	7.620	8.255
E_1	.240	.260	6.096	6.604
e_1	.100 BASIC		2.540 BASIC	
e_A	.300 BASIC		7.620 BASIC	
L	.125	.150	3.175	3.810

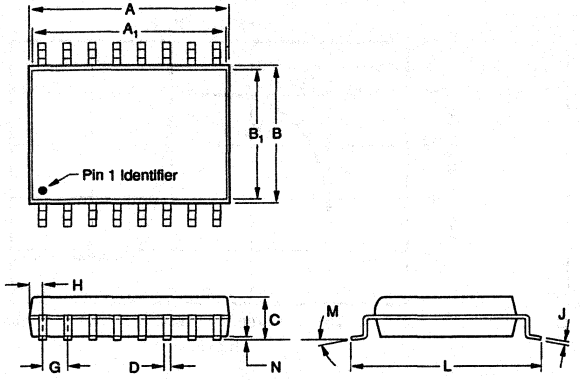
	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
L_2 (4)	0	.030	0	.762
α	0°	15°	0°	15°
N (1)	14		14	
N_1 (2)	0		0	
P	—	.050	—	1.270
Q_1	.050	.085	1.270	2.159
S (3)	.065	.090	1.651	2.286

(1) N = Total number of pins.
(2) N_1 = Total number of missing pins.
(3) Not per JEDEC Std.
(4) e_1 and e_A applies in zone L_2 when unit installed.

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

MECHANICAL

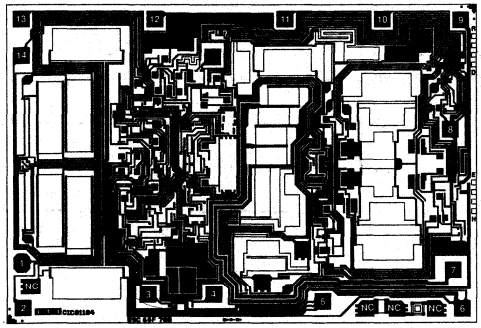
U Package — 16-Pin SOIC



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.400	.416	10.16	10.57
A1	.388	.412	9.86	10.46
B	.286	.302	7.26	7.67
B1	.268	.286	6.81	7.26
C	.093	.109	2.36	2.77
D	.015	.020	0.38	0.51
G	.050 BASIC		1.27 BASIC	
H	.022	.038	0.56	0.97
J	.008	.012	0.20	0.30
L	.391	.421	9.93	10.69
M	5° TYP		5° TYP	
N	.000	.012	0.00	0.30

NOTE: Leads in true position within 0.010" (0.25mm) R at MMC at seating plane.

DICE INFORMATION



XTR101 DIE TOPOGRAPHY

PAD	FUNCTION	PAD	FUNCTION
1	Zero Adjust	8	$+V_{CC}$
2	Zero Adjust	9	E
3	–In	10	I_{REF1}
4	+In	11	I_{REF2}
5	Span	12	B Control
6	Span	13	Bandwidth
7	Out	14	Zero Adjust

NC: No Connection
Substrate Bias: Electrically connected to V– supply.

MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	150 x 105 ±5	3.81 x 2.67 ±0.13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.10 x 0.10
Backing	Gold	

See "DICE PRODUCTS" Section 17 in Data Book Supplement Volume 33c, or contact Burr-Brown for current information.

ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE
XTR101AG	Ceramic DIP	–40°C to +85°C
XTR101BG	Ceramic DIP	–40°C to +85°C
XTR101AP	Plastic DIP	–40°C to +85°C
XTR101AU	Plastic SOIC	–40°C to +85°C

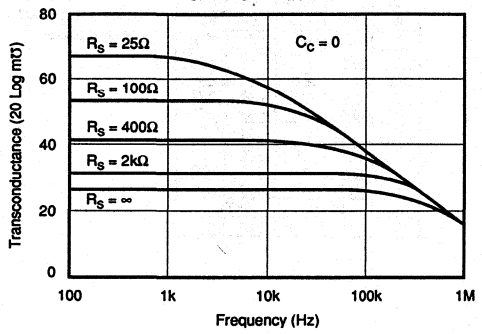
ABSOLUTE MAXIMUM RATINGS

Power Supply, $+V_{CC}$ 40V
Input Voltage, e, or e_2 ..... $\geq V_{OUT}$, $\leq +V_{CC}$
Storage Temperature Range, Ceramic ..... –55°C to +165°C
Plastic ..... –55°C to +125°C
Lead Temperature (soldering 10s) G, P ..... +300°C
(wave soldering, 3s) U ..... +260°C
Output Short-Circuit Duration ..... Continuous $+V_{CC}$ to I_{OUT}
Junction Temperature ..... +165°C

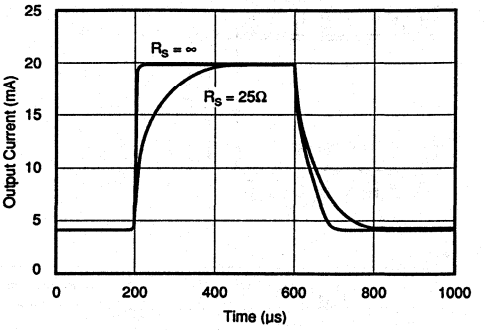
TYPICAL PERFORMANCE CURVES

T_A = +25°C, $+V_{CC}$ = 24VDC unless otherwise noted.

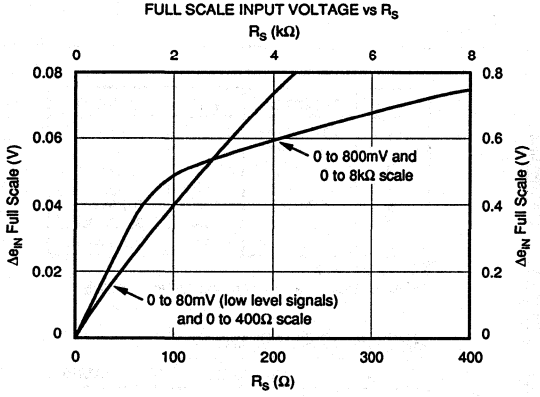
SPAN vs FREQUENCY



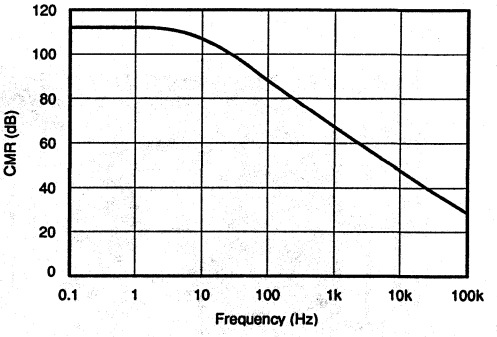
STEP RESPONSE



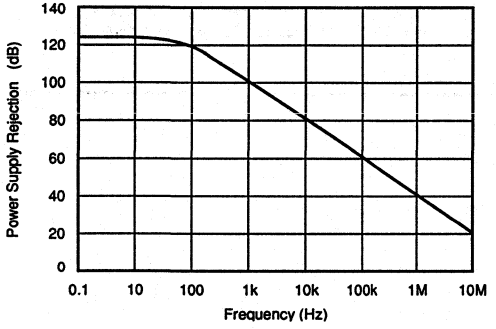
FULL SCALE INPUT VOLTAGE vs R_S



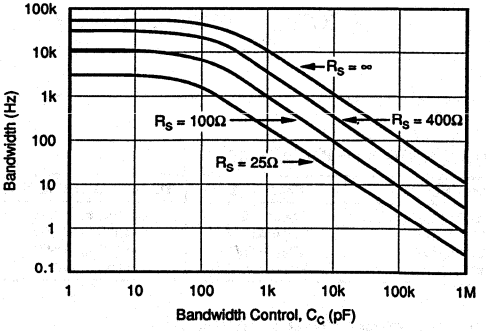
COMMON-MODE REJECTION vs FREQUENCY



POWER SUPPLY REJECTION vs FREQUENCY

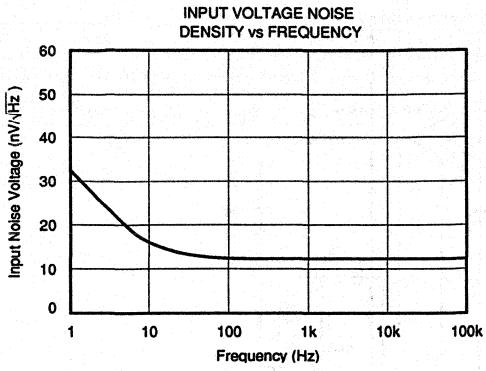


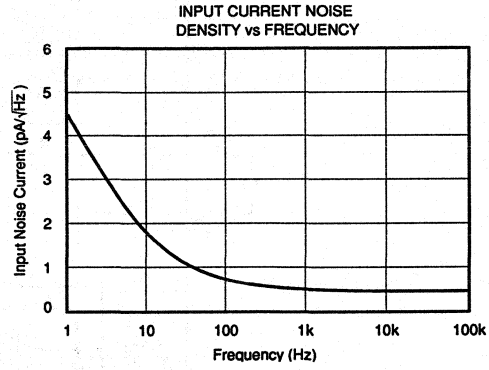
BANDWIDTH vs PHASE COMPENSATION

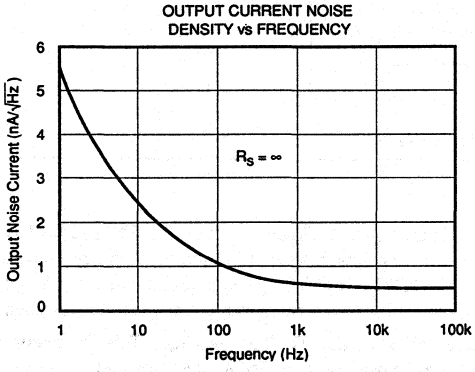


TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, $+V_{CC}$ = 24VDC unless otherwise noted.







THEORY OF OPERATION

A simplified schematic of the XTR101 is shown in Figure 1. Basically the amplifiers, A_1 and A_2, act as a single power supply instrumentation amplifier controlling a current source, A_3 and Q_1. Operation is determined by an internal feedback loop. e_1 applied to pin 3 will also appear at pin 5 and similarly e_2 will appear at pin 6. Therefore the current in R_S, the span setting resistor, will be $I_S = (e_2 - e_1)/R_S = e_{IN}/R_S$. This current combines with the current, I_3, to form I_1. The circuit is configured such that I_2 is 19 times I_1. From this point the derivation of the transfer function is straightforward but lengthy. The result is shown in Figure 1.

Examination of the transfer function shows that I_O has a lower range-limit of 4mA when $e_{IN} = e_2 - e_1 = 0V$. This 4mA is composed of 2mA quiescent current exiting pin 7 plus 2mA from the current sources. The upper range limit of I_O is set to 20mA by the proper selection of R_S based on the upper range limit of e_{IN}. Specifically R_S is chosen for a 16mA output current span for the given full scale input voltage span; i.e., $(0.016\Omega + 40/R_S)(e_{IN}$ full scale) = 16mA. Note that since I_O is unipolar e_2 must be kept larger than e_1; i.e., $e_2 \geq e_1$ or $e_{IN} \geq 0$. Also note that in order not to exceed the output upper range limit of 20mA, e_{IN} must be kept less than 1V when $R_S = \infty$ and proportionately less as R_S is reduced.

INSTALLATION AND OPERATING INSTRUCTIONS

BASIC CONNECTION

The basic connection of the XTR101 is shown in Figure 1. A difference voltage applied between input pins 3 and 4 will cause a current of 4-20mA to circulate in the two-wire output loop (through R_L, V_{PS}, and D_1). For applications requiring moderate accuracy, the XTR101 operates very cost-effectively with just its internal drive transistor. For more demanding applications (high accuracy in high gain) an external NPN transistor can be added in parallel with the internal one. This keeps the heat out of the XTR101 package and minimizes thermal feedback to the input stage. Also in

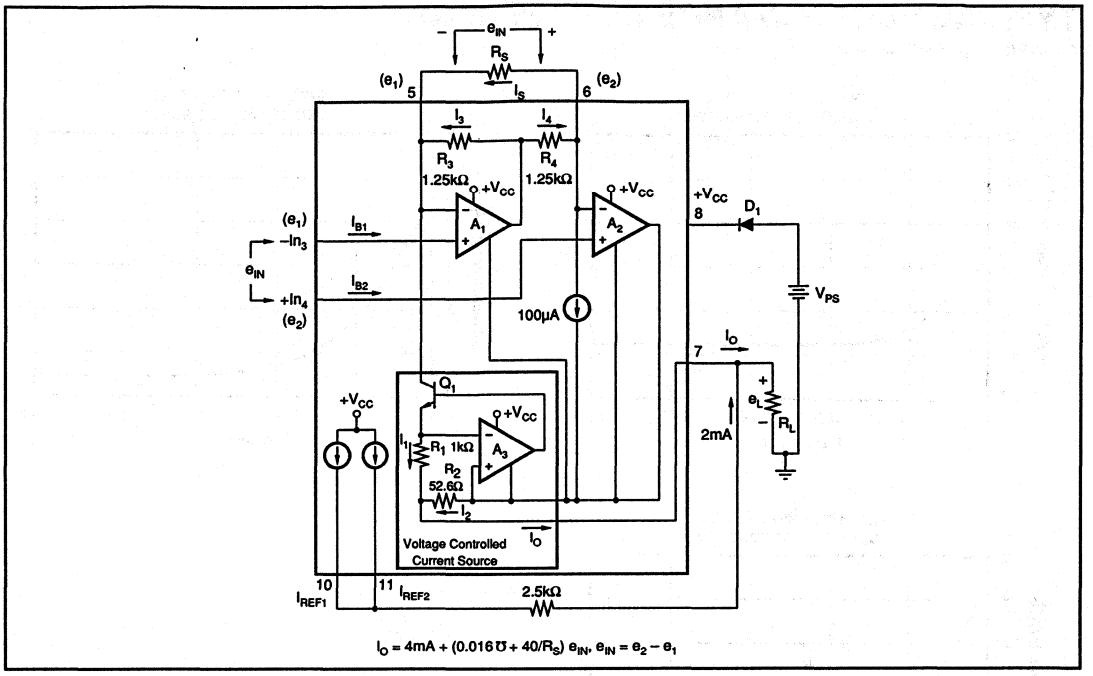


FIGURE 1. Simplified Schematic of the XTR101.

such applications where e_{IN} full scale is small (<50mV) and R_{SPAN} is small (<150Ω), caution should be taken to consider errors from the external span circuit plus high amplification of offset drift and noise.

OPTIONAL EXTERNAL TRANSISTOR

The optional external transistor, when used, is connected in parallel with the XTR101's internal transistor. The purpose is to increase accuracy by reducing heat change inside the XTR101 package as the output current spans from 4-20mA. Under normal operating conditions, the internal transistor is never completely turned off as shown in Figure 2. This maintains frequency stability with varying external transistor characteristics and wiring capacitance. The actual "current sharing" between internal and external transistors is dependent on two factors: (1) relative geometry of emitter areas and (2) relative package dissipation (case size and thermal conductivity). For best results, the external device should have a larger base emitter area and smaller package. It will, upon turn on, take about [0.95 (I_O – 3.3mA)]mA. However, it will heat faster and take a greater share after a few seconds.

Although any NPN of suitable power rating will operate with the XTR101, two readily available transistors are recommended for accuracy improvement:

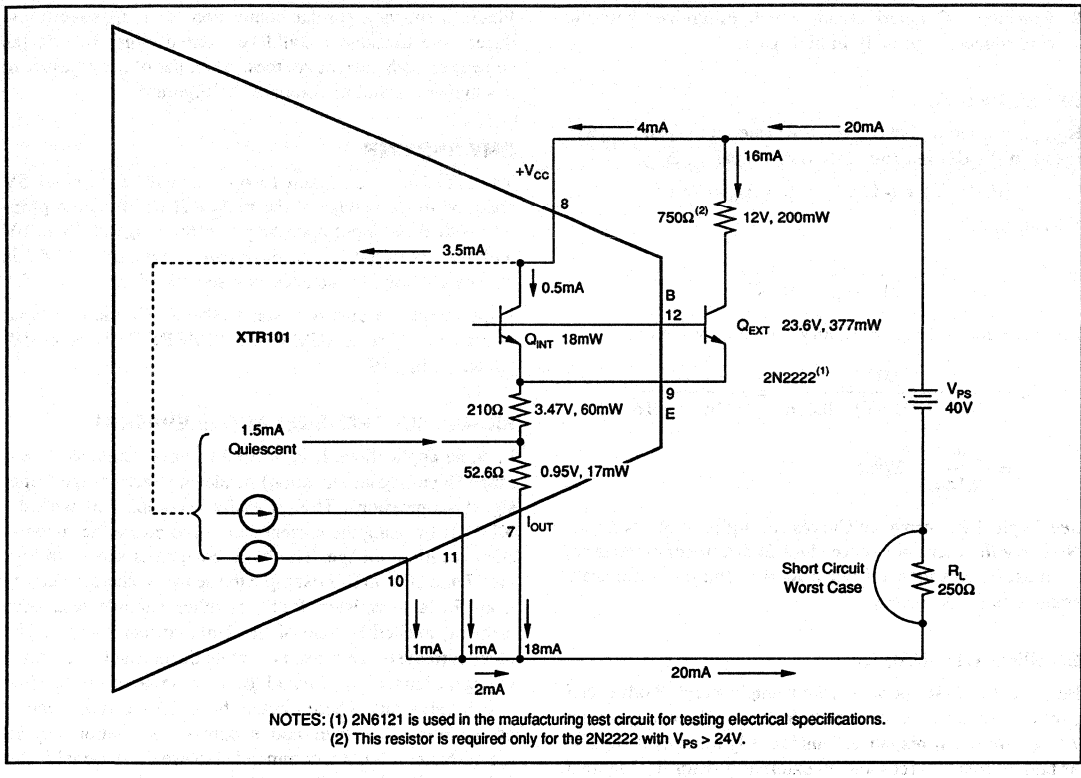
1. 2N2222 in the TO-18 package. For power supply voltages above 24V, a 750Ω, 1/2W resistor should be connected in series with the collector. This will limit the power dissipation to 377mW under the worst-case conditions shown in Figure 2. Thus the 2N2222 will safely operate below its 400mW rating at the upper temperature of +85°C. Heat sinking the 2N2222 will result in greatly reduced accuracy improvement and is not recommended.
2. 2N6121 in the TO-220 package. This transistor will operate over the specified temperature and output voltage range without a series collector resistor. Heat sinking the 2N6121 will result in slightly less accuracy improvement. It can be done, however, when mechanical constraints require it.

ACCURACY WITH AND WITHOUT EXTERNAL TRANSISTOR

The XTR101 has been tested in a circuit using a 2N6121 external transistor. The relative difference in accuracy with and without an external transistor is shown in Figure 3. Notice that a dramatic improvement in offset voltage change with supply voltage is evident for any value of load resistor.

MAJOR POINTS TO CONSIDER WHEN USING THE XTR101

1. The leads to R_S should be kept as short as possible to reduce noise pick-up and parasitic resistance.
2. +V_{CC} should be bypassed with a 0.01µF capacitor as close to the unit as possible (pin 8 to 7).
3. Always keep the input voltages within their range of linear operation, +4V to +6V (e_1 and e_2 measured with respect to pin 7).



NOTES: (1) 2N6121 is used in the maufacturing test circuit for testing electrical specifications.
(2) This resistor is required only for the 2N2222 with V_{PS} > 24V.

FIGURE 2. Power Calculation of XTR101 with External Transistor.

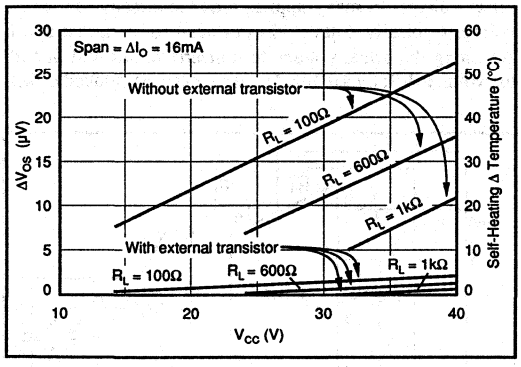


FIGURE 3. Thermal Feedback Due to Change in Output Current.

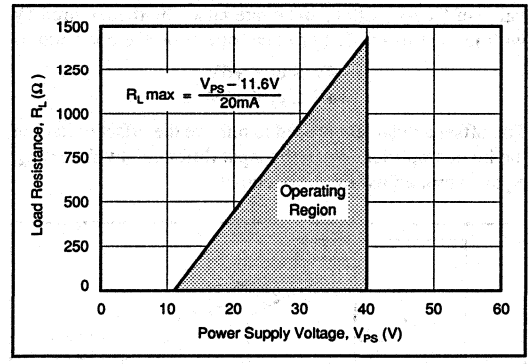


FIGURE 4. Power Supply Operating Range.

4. The maximum input signal level (e_{INFS}) is 1V with $R_S = \infty$ and proportionally less as R_S decreases.
5. Always return the current references (pins 10 and 11) to the output (pin 7) through an appropriate resistor. If the references are not used for biasing or excitation, connect them together to pin 7. Each reference must have between 0V and +(V_{CC} – 4V) with respect to pin 7.
6. Always choose R_L (including line resistance) so that the voltage between pins 7 and 8 (+V_{CC}) remains within the 11.6V to 40V range as the output changes between the 4-20mA range (see Figure 4).
7. It is recommended that a reverse polarity protection diode (D_1 in Figure 1) be used. This will prevent damage to the XTR101 caused by a momentary (e.g., transient) or long term application of the wrong polarity of voltage between pins 7 and 8.

8. Consider PC board layout which minimizes parasitic capacitance, especially in high gain.

SELECTING R_S

R_{SPAN} is chosen to that a given full scale input span e_{INFS} will result in the desired full scale output span of ΔI_{OFS},

$$[(0.016\Omega) + (40/R_S)]\ \Delta e_{IN} = \Delta I_O = 16mA.$$

Solving for R_S:

$$R_S = \frac{40}{\Delta I_O/\Delta e_{IN} - 0.016\Omega} \quad (1)$$

For example, if Δe_{INFS} = 100mV for ΔI_{OFS} = 16mA,

$$R_S = \frac{40}{16mA/100mV) - 0.016} = \frac{40}{0.16 - 0.016}$$

$$= \frac{40}{0.144} = 278\Omega$$

See Typical Performance Curves for a plot of R_S vs Δe_{INFS}. Note that in order not to exceed the 20mA upper range limit, e_{IN} must be less than 1V when $R_S = \infty$ and proportionately smaller as R_S decreases.

BIASING THE INPUTS

Because the XTR operates from a single supply both e_1 and e_2 must be biased approximately 5V above the voltage at pin 7 to assure linear response. This is easily done by using one or both current sources and an external resistor R_2. Figure 5 shows the simplest case— a floating voltage source e'_2. The 2mA from the current sources flows through the 2.5kΩ value of R_2 and both e_1 and e_2 are raised by the required 5V with respect to pin 7. For linear operation the constraint is

$$+4V \le e_1 \le +6V$$
$$+4V \le e_2 \le +6V$$

The offset adjustment is used to remove the offset voltage of the input amplifier. When the input differential voltage (e_{IN}) equals zero, adjust for 4mA output.

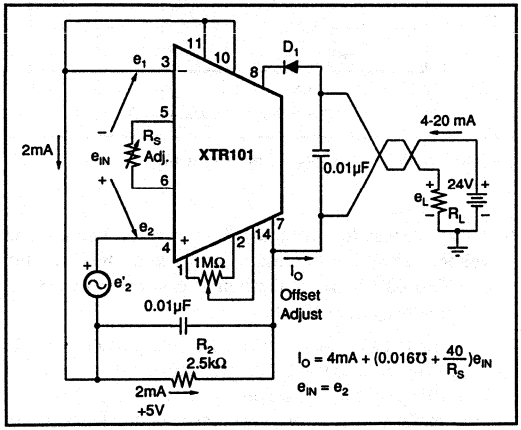


FIGURE 5. Basic Connection for Floating Voltage Source.

Figure 6 shows a similar connection for a resistive transducer. The transducer could be excited either by one (as shown) or both current sources. Also, the offset adjustment has higher resolution compared to Figure 5.

CMV AND CMR

The XTR101 is designed to operate with a nominal 5V common-mode voltage at the input and will function properly with either input operating over the range of 4V to 6V with respect to pin 7. The error caused by the 5V CMV is already included in the accuracy specifications.

If the inputs are biased at some other CMV then an input offset error term is (CMV – 5)/CMRR; CMR is in dB, CMRR is in V/V.

SIGNAL SUPPRESSION AND ELEVATION

In some applications it is desired to have suppressed zero range (input signal elevation) or elevated zero range (input signal suppression). This is easily accomplished with the XTR101 by using the current sources to create the suppression/elevation voltage. The basic concept is shown in Figures 7 and 8(a). In this example the sensor voltage is derived from R_T (a thermistor, RTD, or other variable resistance element) excited by one of the 1mA current sources. The other current source is used to create the elevated zero range voltage. Figures 8(b), (c) and (d) show some of the possible circuit variations. These circuits have the desirable feature of noninteractive span and suppression/elevation adjustments. Note: It is not recommended to use the optional offset voltage null (pins 1, 2 and 14) for elevation/suppression. This trim capability is used only to null the amplifier's input offset voltage. In many applications the already low offset voltage (typically 20µV) will not need to be nulled at all. Adjusting the offset voltage to nonzero values will disturb the voltage drift by ±0.3µV/°C per 100µV or induced offset.

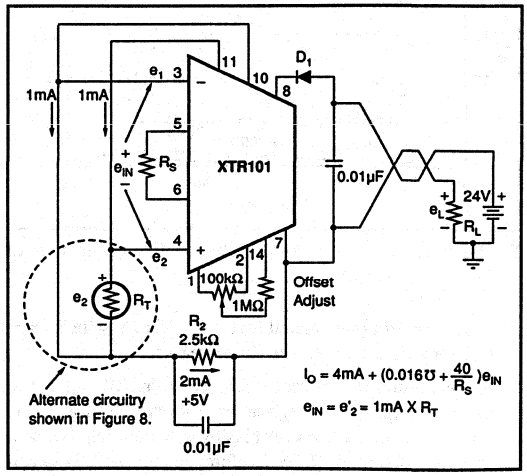


FIGURE 6. Basic Connection for Resistive Source.

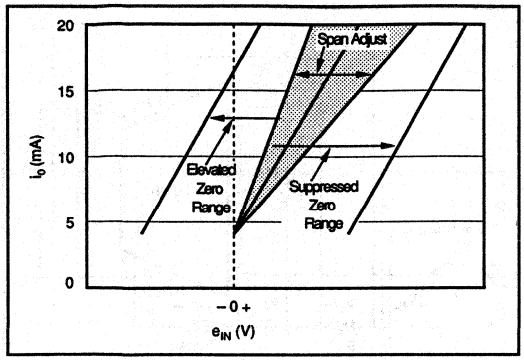


FIGURE 7. Elevation and Suppression Graph.

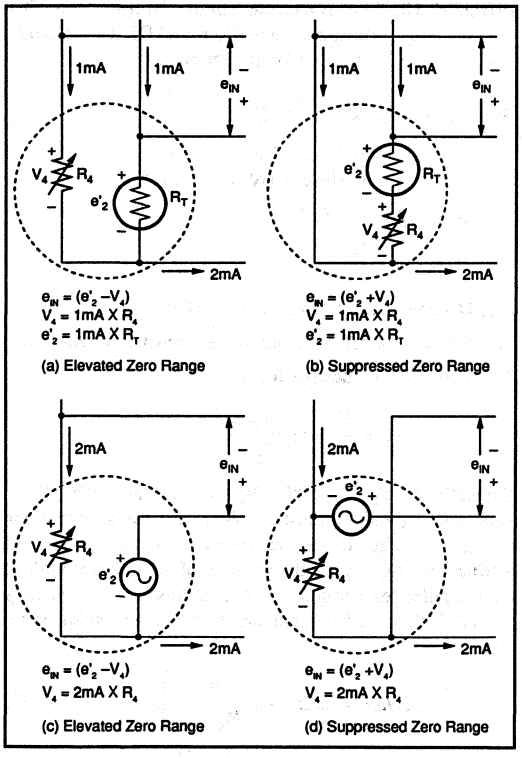


FIGURE 8. Elevation and Suppression Circuits.

APPLICATION INFORMATION

The small size, low offset voltage and drift, excellent linearity, and internal precision current sources, make the XTR101 ideal for a variety of two-wire transmitter applications. It can be used by OEMs producing different types of transducer transmitter modules and by data acquisition systems manufacturers who gather transducer data. Current mode transmission greatly reduces noise interference. The two-wire nature of the device allows economical signal conditioning at the transducer. Thus the XTR101 is, in general, very suitable for individualized and special purpose applications.

EXAMPLE 1

RTD Transducer shown in Figure 9.

Given a process with temperature limits of +25°C and +150°C, configure the XTR101 to measure the temperature with a platinum RTD which produces 100Ω at 0°C and 200Ω at +266°C (obtained from standard RTD tables). Transmit 4mA for +25°C and 20mA for +150°C.

COMPUTING R_S:

The sensitivity of the RTD is $\Delta R/\Delta T = 100\Omega/266°C$. When excited with a 1mA current source for a 25°C to 150°C range (i.e., 125°C span), the span of e_{IN} is 1mA X (100Ω/266°C) X 125°C = 47mV = Δe_{IN}.

$$\text{From equation 1, } R_S = \frac{40}{\Delta I_O/\Delta e_{IN} - 0.016\Omega}$$

$$R_S = \frac{40}{16mA/47mV - 0.016\Omega} = \frac{40}{0.3244} = 123.3\Omega$$

Span adjustment (calibration) is accomplished by trimming R_S.

COMPUTING R_4:

At +25°C, $e'_2 = 1mA\ (R_T + \Delta R_T)$

$$= 1mA\ [100\Omega + \frac{100\Omega}{266°C} \times 25°C]$$

$$= 1mA\ (109.4\Omega) = 109.4mV$$

In order to make the lower range limit of 25°C correspond to the output lower range limit of 4mA, the input circuitry shown in Figure 9 is used.

e_{IN}, the XTR101 differential input, is made 0 at 25°C or

$$e'_{2\ 25°C} - V_4 = 0$$

$$\text{thus, } V_4 = e'_{2\ 25°C} = 109.4mV$$

$$R_4 = \frac{V_4}{1mA} = \frac{109.4mV}{1mA} = 109.4\Omega$$

COMPUTING R_2 AND CHECKING CMV:

At +25°C, $e'_2 = 109.4mV$

At +150°C, $e'_2 = 1mA\ (R_T + \Delta R_T)$

$$= 1mA\ [100\Omega + (\frac{100\Omega}{266°C} \times 150°C)]$$

$$= 156.4mV$$

Since both e'_2 and V_4 are small relative to the desired 5V common-mode voltage, they may be ignored in computing R_2 as long as the CMV is met.

$R_2 = 5V/2mA = 2.5k\Omega$

e_2 min = 5V + 0.1094V
e_2 max = 5V + 0.1564V
e_1 = 5V + 0.1094V

} The +4V to +6V CMV requirement is met.

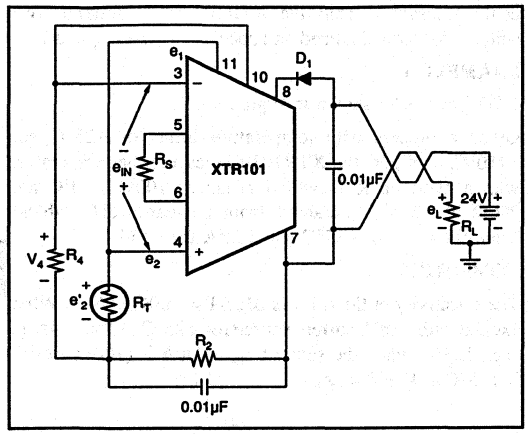


FIGURE 9. Circuit for Example 1.

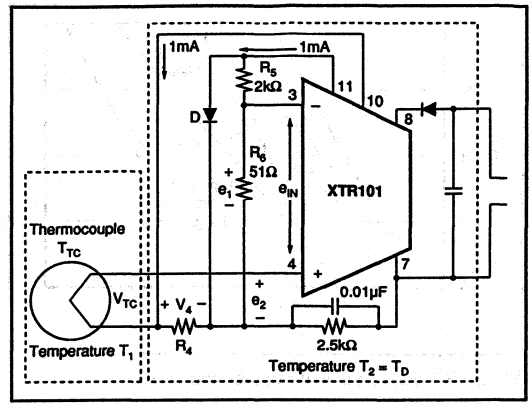


FIGURE 10. Thermocouple Input Circuit with Two Temperature Regions and Diode (D) Cold Junction Compensation.

EXAMPLE 2

Thermocouple Transducer shown in Figure 10.

Given a process with temperature (T_1) limits of 0°C and +1000°C, configure the XTR101 to measure the temperature with a type J thermocouple that produces a 58mV change for 1000°C change. Use a semiconductor diode for a cold junction compensation to make the measurement relative to 0°C. This is accomplished by supplying a compensating voltage, V_{R6}, equal to that normally produced by the thermocouple with its "cold junction" (T_2) at ambient. At a typical ambient of +25°C this is 1.28mV (obtained from standard thermocouple tables with reference junction of 0°C). Transmit 4mA for T_1 = 0°C and 20mA for T_1 = +1000°C. Note: $e_{IN} = e_2 - e_1$ indicates that T_1 is relative to T_2.

ESTABLISHING R_S:

The input full scale span is 58mV (Δe_{INFS} = 58mV).

R_S is found from equation (1)

$$R_S = \frac{40}{\Delta I_O/\Delta e_{IN} - 0.016\text{Ʊ}}$$

$$= \frac{40}{16\text{mA}/58\text{mV} - 0.016\text{Ʊ}} = \frac{40}{0.2599} = 153.9\Omega$$

SELECTING R_4:

R_4 is chosen to make the output 4mA at T_{TC} = 0°C (V_{TC}= –1.28mV) and T_D = +25°C (V_D = 0.6V). A circuit is shown in Figure 10.

V_{TC} will be –1.28mV when T_{TC} = 0°C and the reference junction is at +25°C. e_1 must be computed for the condition of T_D = +25°C to make e_{IN} = 0V.

$$V_{D\,25°C} = 600\text{mV}$$

$$e_{1\,25°C} = 600\text{mV}\ (51/2051) = 14.9\text{mV}$$

$$e_{IN} = e_2 - e_1 = V_{TC} + V_4 - e_1$$

With e_{IN} = 0 and V_{TC} = –1.28mV,

$$V_4 = e_1 + e_{IN} - V_{TC}$$

$$= 14.9\text{mV} + 0\text{V} - (-1.28\text{mV})$$

$$1\text{mA}\ (R_4) = 16.18\text{mV}$$

$$R_4 = 16.18\Omega$$

COLD JUNCTION COMPENSATION:

The temperature reference circuit is shown in Figure 11.

The diode voltage has the form

$$V_D = \frac{KT}{q}\ \ln\frac{I_{DIODE}}{I_{SAT}}$$

Typically at T_2 = +25°C, V_D = 0.6V and $\Delta V_D/\Delta T$ = –2mV/°C. R_5 and R_6 form a voltage divider for the diode voltage V_D. The divider values are selected so that the gradient $\Delta_V D/\Delta T$ equals the gradient of the thermocouple at the reference temperature. At +25°C this is approximately 52µV/°C (obtained from standard thermocouple table); therefore,

$$\Delta T_C/\Delta T = \Delta_V D/\Delta T\left[\frac{R_6}{R_5 + R_6}\right] \qquad (2)$$

$$52\mu\text{V/°C} = 200\mu\text{V/°C}\left[\frac{R_6}{R_5 + R_6}\right]$$

R_5 is chosen as 2kΩ to be much larger than the resistance of the diode. Solving for R_6 yields 51Ω.

THERMOCOUPLE BURN-OUT INDICATION

In process control applications it is desirable to detect when a thermocouple has burned out. This is typically done by forcing the two-wire transmitter current to either limit when

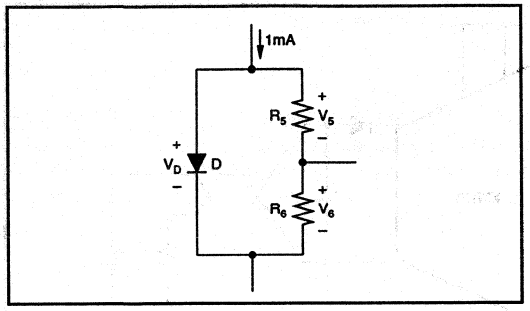


FIGURE 11. Cold Junction Compensation Circuit.

the thermocouple impedance goes very high. The circuits of Figures 16 and 17 inherently have down scale indication. When the impedance of the thermocouple gets very large (open) the bias current flowing into the + input (large impedance) will cause I_O to go to its lower range limit value (about 3.8mA). If up scale indication is desired the circuit of Figure 18 should be used. When the T_C opens the output will go to its upper range limit value (about 25mA or higher).

OPTIONAL INPUT OFFSET VOLTAGE TRIM

The XTR101 has provisions for nulling the input offset voltage associated with the input amplifiers. In many applications the already low offset voltages (30µV max for the B grade, 60µV max for the A grade) will not need to be nulled at all. The null adjustment can be done with a potentiometer at pins 1, 2 and 14 as shown in Figures 5 and 6. Either of these two circuits may be used. NOTE: It is not recommended to use this input offset voltage nulling capability for elevation or suppression. See the Signal Suppression and Elevation section for the proper techniques.

OPTIONAL BANDWIDTH CONTROL

Low-pass filtering is recommended where possible and can be done by either one of two techniques shown in Figure 12. C_2 connected to pins 3 and 4 will reduce the bandwidth with a cutoff frequency given by,

$$f_{CO} = \frac{15.9}{(R_1 + R_2 + R_3 + R_4)(C_2 + 3pF)}$$

This method has the disadvantage of having f_{CO} vary with R_1, R_2, R_3, R_4, and it may require large values of R_3 and R_4. The other method, using C_1, will use smaller values of capacitance and is not a function of the input resistors. It is, however, more subject to nonlinear distortion caused by slew rate limiting. This is normally not a problem with the slow signals associated with most process control transducers. The relationship between C_1 and f_{CO} is shown in the Typical Performance Curves.

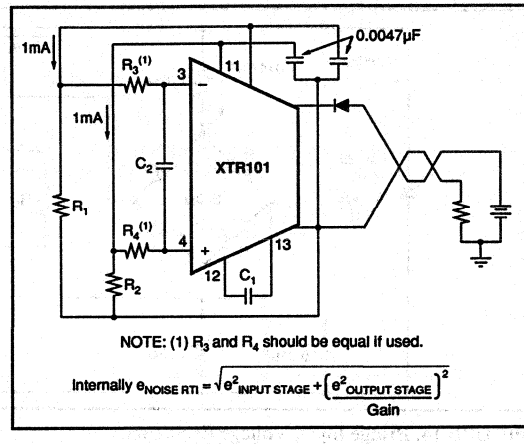


FIGURE 12. Optional Filtering.

APPLICATION CIRCUITS

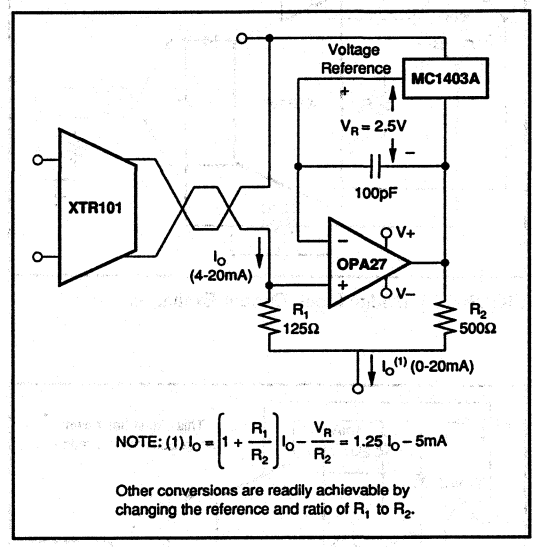


FIGURE 13. 0-20mA Output Converter.

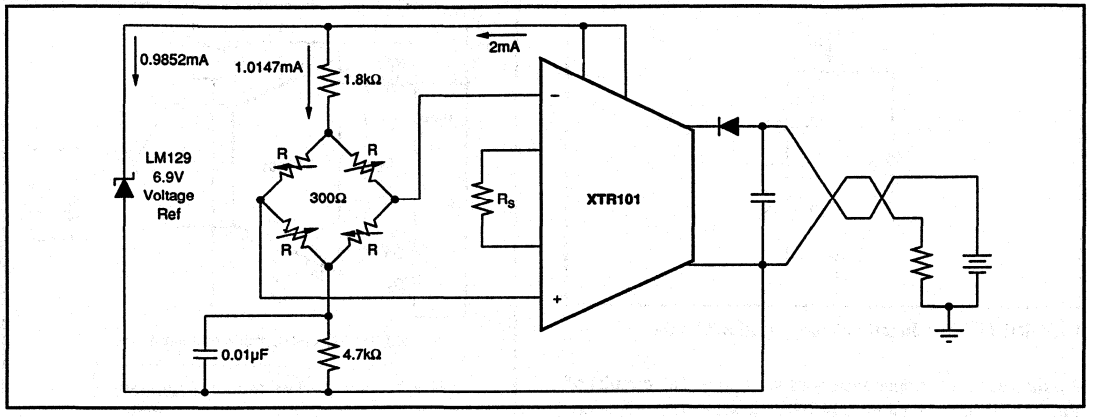


FIGURE 14. Bridge Input, Voltage Excitation.

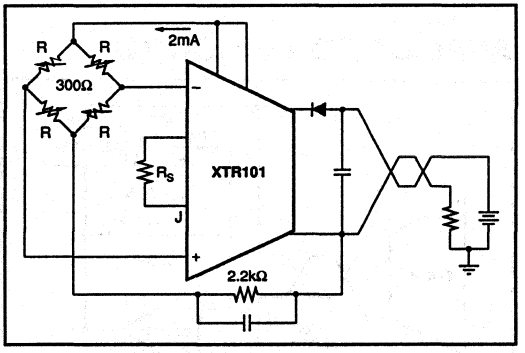


FIGURE 15. Bridge Input, Current Excitation.

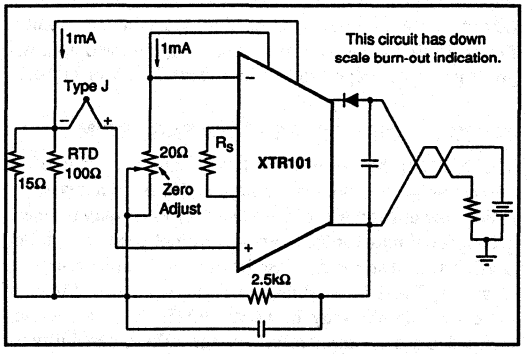


FIGURE 16. Thermocouple Input with RTD Cold Junction Compensation.

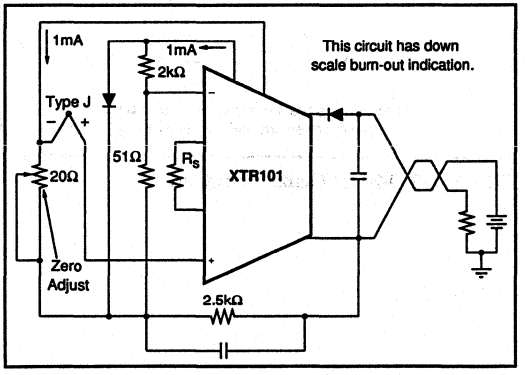


FIGURE 17. Thermocouple Input with Diode Cold Junction Compensation.

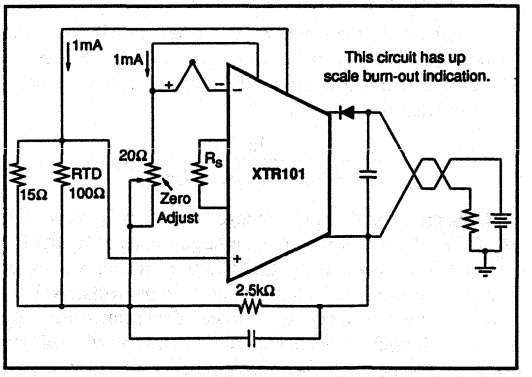


FIGURE 18. Thermocouple Input with RTD Cold Junction Compensation.

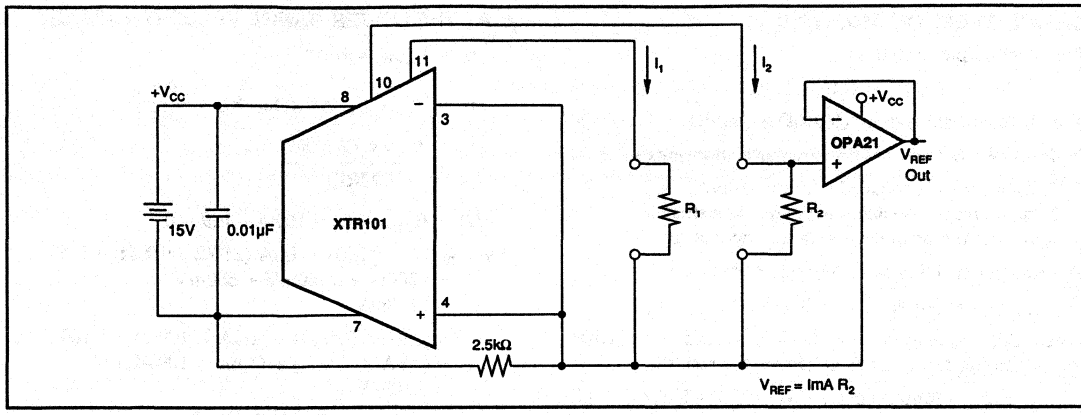


FIGURE 19. Dual Precision Current Sources Operated From One Supply.

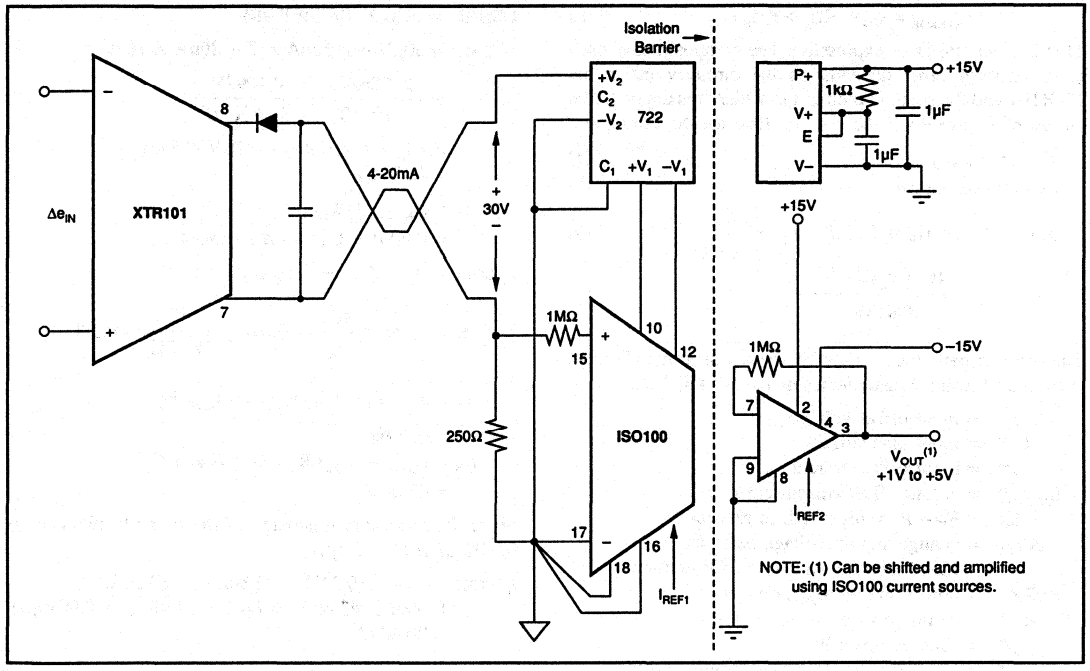


FIGURE 20. Isolated Two-Wire Current Loop.

DETAILED ERROR ANALYSIS

The ideal output current is

$$i_{O\ IDEAL} = 4mA + K\ e_{IN}$$

K is the span (gain) term, $(0.016\Omega + (40/R_S))$ (3)

In the XTR101 there are three major components of error:

1. σ_O = errors associated with the output stage.
2. σ_S = errors associated with span adjustment.
3. σ_I = errors associated with the input stage.

The transfer function including these errors is

$$i_{O\ ACTUAL} = (4mA + \sigma_O) + K\ (1 + \sigma_S)(e_{IN} + \sigma_I) \quad (4)$$

When this expression is expanded, second order terms ($\sigma_S\ \sigma_I$) dropped, and terms collected, the result is

$$i_{O\ ACTUAL} = (4mA + \sigma_O) + K\ e_{IN} + K\sigma_I + K\sigma_S\ e_{IN} \quad (5)$$

The error in the output current is $i_{O\ ACTUAL} - i_{O\ IDEAL}$ and can be found by subtracting equations (5) and (3).

$$i_{O\ ERROR} = \sigma_O + K\sigma_I + K\sigma_S\ e_{IN} \quad (6)$$

This is a general error expression. The composition of each component of error depends on the circuitry inside the XTR101 and the particular circuit in which it is applied. The circuit of Figure 9 will be used to illustrate the principles.

1. $\sigma_O = I_{OS\ RTO}$ (7)
2. $\sigma_S = \varepsilon_{NONLINEARITY} + \varepsilon_{SPAN}$ (8)
3. $$\sigma_I = V_{OSI} + (I_{B1} + R_4 - I_{B2}\ R_T) + \frac{\Delta V_{CC}}{PSRR} + \frac{(e_1 + e_2)/2 - 5V}{CMRR} \quad (9)$$

The term in parentheses may be written in terms of offset current and resistor mismatches as $I_{B1}\ \Delta R + I_{OS}'\ R_4$.

V_{OSI}* = input offset voltage
I_{B1}*, I_{B2}* = input bias current
I_{OSI}* = input offset current
$I_{OS\ RTO}$* = output offset current error
$\Delta R = R_T - R_4$ = mismatch in resistor
ΔV_{CC} = change supply voltage between pins 7 and 8 away from 24V nominal
PSRR* = power supply rejection ratio
CMRR* = common-mode rejection ratio
ε_{NONLIN}* = span nonlinearity
ε_{SPAN}* = span equation error. Untrimmed error = 5% max. May be trimmed to zero.

Items marked with an asterisk (*) can be found in the Electrical Specifications.

EXAMPLE 3

The circuit in Figure 9 with the XTR101BG specifications and the following conditions: $R_T = 109.4\Omega$ at 25°C, $R_T = 156.4\Omega$ at 150°C, $I_O = 4mA$ at 25°C, $I_O = 20mA$ at 150°C, $R_S = 123.3\Omega$, $R_4 = 109\Omega$, $R_L = 250\Omega$, $R_{LINE} = 100\Omega$, $V_{DI} = 0.6V$, $V_{PS} = 24V \pm 0.5\%$. Determine the % error at the upper and lower range values.

A. AT THE LOWER RANGE VALUE (T = +25°C).

$\sigma_O = I_{OS\ RTO} = \pm 6\mu A$

$$\sigma_I = V_{OSI} + (I_{B1}\ \Delta R + I_{OS1}\ R_4) + \frac{\Delta V_{CC}}{PSRR} + \frac{(e_1 + e_2)/2 - 5V}{CMRR}$$

$\Delta R = R_{T\ 25°C} - R_4 = 109.4 - 109 \approx 0$

$\Delta V_{CC} = (24\ X\ 0.005) + 4mA\ (250\Omega + 100\Omega) + 0.6V$
$= 120mV + 1400mV + 600mV$
$= 2120mV$

$e_1 = (2mA\ X\ 2.5k\Omega) + (1mA\ X\ 109\Omega) = 5.109V$
$e_2 = (2mA\ X\ 2.5k\Omega) + (1mA\ X\ 109.4\Omega)$
$= 5.1094V$

$(e_1 + e_2)/2 - 5 = 0.1092V$

$PSRR = 3.16\ X\ 10^5$ for 110dB

$CMRR = 31.6\ X\ 10^3$ for 90dB

$$\sigma_I = 30\mu V + (150nA\ X\ 0 + 20nA\ X\ 109\Omega) + \frac{2120mV}{3.16\ X\ 10^5} + \frac{0.1092V}{3.16\ X\ 10^3} \quad (10)$$
$= 30\mu V + 2.18\mu V + 6.7\mu V + 3.46\mu V$
$= 42.34\mu V$

$\sigma_S = \varepsilon_{NONLIN} + \varepsilon_{SPAN}$
$= 0.0001 + 0$ (assumes trim of R_S)

I_O error $= \sigma_O + K\ \sigma_I + K\ \sigma_S\ e_{IN}$

$$K = 0.016 + \frac{40}{R_S} = 0.016 + \frac{40}{123.3\Omega} = 0.340\text{℧}$$

$e_{IN} = e_2 - V_4 = I_{REF1}\ R_{T\ 25°C} - I_{REF2}\ R_4$

since $R_{T\ 25°C} = R_4$,

$e_{IN} = (I_{REF1} - I_{REF2})\ R_4 = 0.4\mu A\ X\ 109\Omega$
$= 43.6\mu V$

Since the maximum mismatch of the current references is 0.04% of 1mA = 0.4μA,

I_O error $= 6\mu A + (0.34\text{℧}\ X\ 42.34\mu V) + (0.34\ \text{℧}\ X\ 0.0001\ X\ 43.6\mu V) = 6\mu A + 14.40\mu A + 0.0015\mu A$
$= 20.40\mu A$

$$\%\ \text{error} = \frac{20.40\mu A}{16mA}\ X\ 100\%$$

0.13% of span at lower range value.

B. AT THE UPPER RANGE VALUE (T = +150°C).

$\Delta R = R_{T\ 150°C} - R_4 = 156.4 - 109.4 = 47\Omega$

$\Delta V_{CC} = (24\ X\ 0.005) + 20mA\ (250\Omega + 100\Omega) + 0.6V = 7720mV$

$e_1 = 5.109V$

$e_2 = (2mA\ X\ 2.5k\Omega) + (1mA\ X\ 156.4\Omega) = 5.156V$

$(e_1 + e_2)/2 - 5V = 0.1325V$

$$\sigma_O = 6\mu A$$

$$\sigma_I = 30\mu V + (150nA \times 47\Omega + 20nA \times 190\Omega) + \frac{7720mV}{3.16 \times 10^5} + \frac{0.1325V}{3.16 \times 10^3}$$
$$= 30\mu V + 9.23\mu V + 24\mu V + 4.19\mu V$$
$$= 67.42\mu V$$

$$\sigma_S = 0.0001$$

$$e_{IN} = e'_2 - V_4 = I_{REF1} R_{T\ 150°C} - I_{REF2} R_4$$
$$= (1mA \times 156.4\Omega) - (1mA \times 109\Omega) = 47mV$$

$$I_O \text{ error} = \sigma_O + K\,\sigma_I + K\,\sigma_S\,e_{IN} = 6\mu A + (0.34\,\mho \times 67.42\mu V) + (0.34\,\mho \times 0.0001 \times 47000\mu V) = 6\mu A + 22.92\mu A + 1.60\mu A$$
$$= 30.52\mu A$$

$$\%\text{ error} = \frac{30.52\mu A}{16mA} \times 100\%$$
$$= 0.19\% \text{ of span at upper range value.}$$

CONCLUSIONS

Lower Range: From equation (10) it is observed that the predominant error term is the input offset voltage (30µV for the B grade). This is of little consequence in many applications. $V_{OS\ RTI}$ can, however, be nulled using the pot shown in Figures 5 and 6. The result is an error of 0.06% of span instead of 0.13% if span.

Upper Range: From equation (11), the predominant errors are $I_{OS\ RTO}$ (6µA), $V_{OS\ RTI}$ (30µV), and I_B (150nA), max, B grade. Both I_{OS} and V_{OS} can be trimmed to zero; however, the result is an error of 0.09% of span instead of 0.19% span.

RECOMMENDED HANDLING PROCEDURES FOR INTEGRATED CIRCUITS

All semiconductor devices are vulnerable, in varying degrees, to damage from the discharge of electrostatic energy. Such damage can cause performance degradation or failure, either immediate or latent. As a general practice, we recommend the following handling procedures to reduce the risk of electrostatic damage.

1. Remove the static-generating materials, such as untreated plastic, from all areas that handle microcircuits.
2. Ground all operators, equipment, and work stations.
3. Transport and ship microcircuits, or products incorporat ing microcircuits, in static-free, shielded containers.
4. Connect together all leads of each device by means of a conductive material, when the device is not connected into a circuit.
5. Control relative humidity to as high a value as practical (50% recommended).

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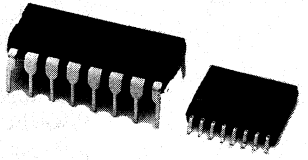


XTR103

4-20mA Current Transmitter with RTD EXCITATION AND LINEARIZATION

FEATURES

- LESS THAN ±1% TOTAL ADJUSTED ERROR, –40°C TO +85°C
- RTD EXCITATION AND LINEARIZATION
- TWO OR THREE-WIRE RTD OPERATION
- WIDE SUPPLY RANGE: 9V to 40V
- HIGH PSR: 110dB min
- HIGH CMR: 80dB min

APPLICATIONS

- INDUSTRIAL PROCESS CONTROL
- FACTORY AUTOMATION
- SCADA

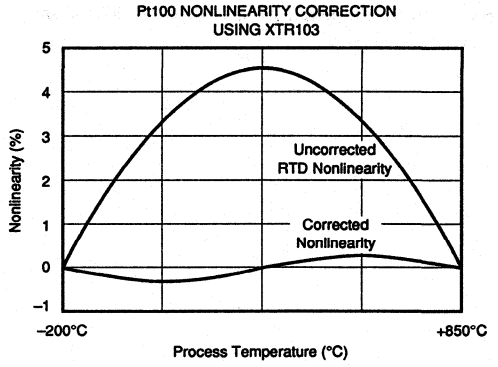
DESCRIPTION

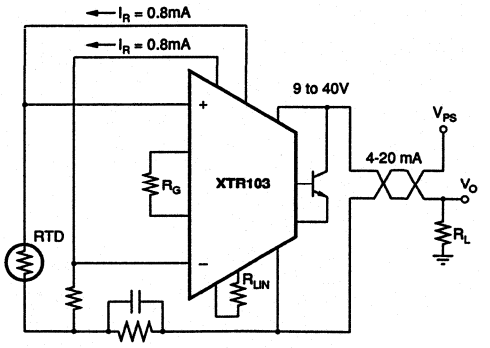
The XTR103 is a monolithic 4-20mA, two-wire current transmitter designed for Platinum RTD temperature sensors. It provides complete RTD current excitation, instrumentation amplifier, linearization, and current output circuitry on a single integrated circuit.

Versatile linearization circuitry provides a 2nd-order correction to the RTD, typically achieving a 40:1 improvement in linearity.

Instrumentation amplifier gain can be configured for a wide range of temperature measurements. Total adjusted error of the complete current transmitter, including the linearized RTD is less than ±1% over the full –40 to +85°C operating temperature range. This includes zero drift, span drift and nonlinearity. The XTR103 operates on loop power supply voltages down to 9V.

The XTR103 is available in 16-pin plastic DIP and SOL-16 surface-mount packages specified for the –40°C to +85°C temperature range. Dice are also available.





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PDS-1145

SPECIFICATIONS

ELECTRICAL

T_A = +25°C, V+ = 24V, and 2N6121 external transistor, unless otherwise noted.

PARAMETER	CONDITIONS	XTR103BP/BU MIN	XTR103BP/BU TYP	XTR103BP/BU MAX	XTR103AP/AU MIN	XTR103AP/AU TYP	XTR103AP/AU MAX	UNITS
OUTPUT								
Output Current Equation			$I_O = V_{IN} \cdot (0.016 + 40/R_G) + 4mA$, V_{IN} in Volts, R_G in Ω					A
Total Adjusted Error[1]	T_{MIN} to T_{MAX}			±1			±2	% of FS
Output Current, Specified Range		4		20	*		*	mA
Over-Scale Limit			34	40		*	*	mA
Under Scale-Limit			3.6	3.8		*	*	mA
Full Scale Output Error	V_{IN} = 1V, R_G = ∞		±15	±50		*	±100	µA
Noise: 0.1Hz to 1kHz	R_G = 40Ω		8			*		µAp-p
ZERO OUTPUT[2]	V_{IN} = 0, R_G = ∞		4			*		mA
Initial Error			±5	±50		*	100	µA
vs Temperature			±0.2	±0.5		*	±1	µA/°C
vs Supply Voltage, V+	V+ = 9V to 40V[3]		0.5	2		*	*	µA/V
vs Common-Mode Voltage	V_{CM} = 2V to 4V[3]		0.1	2		*	*	µA/V
SPAN								
Span Equation (Transconductance)			S = 0.016 + 40/R_G			*		A/V
Untrimmed Error	$R_G \geq 75Ω$		±0.1	±1		*	*	%
vs Temperature[4]			±20	±50		*	±100	ppm/°C
Nonlinearity: Ideal Input				0.01			*	%
RTD Input	Pt100: –200°C to +850°C R_{LIN} = 1127Ω		0.1				*	%
INPUT								
Differential Range	R_G = ∞			1			*	V
Common-Mode Range[3]		2		4	*		*	V
Common-Mode Rejection	V_{IN} = 2V to 4V[3]	80	100		*	*		dB
Impedance: Differential			3			*		GΩ
Common-Mode			0.5			*		GΩ
Offset Voltage			±0.5	±2.5		*	*	mV
vs Temperature			±1	±2.5		±2	±5	µV/°C
vs Supply Voltage, V+	V+ = 9V to 40V[3]	110	130		*	*		dB
Input Bias Current			100	250		*	*	nA
vs Temperature			0.1	2		*	*	nA/°C
Input Offset Current			2	20		*	*	nA
vs Temperature			0.01	0.25		*	*	nA/°C
CURRENT SOURCES[5]								
Current			0.8			*		mA
Accuracy			±0.25	±0.5		*	±1	%
vs Temperature			±25	±50		±50	±100	ppm/°C
vs Power Supply, V+	V+ = 9V to 40V[3]		50			*		ppm/V
Compliance Voltage[3]	(V^-_{IN}) – 0.2			(V+) – 5	*		*	V
Matching				±0.5			*	%
vs Temperature			±10	±25		*	±50	ppm/°C
vs Power Supply, V+	V+ = 9V to 40V[3]		10			*		ppm/V
POWER SUPPLY								
Voltage Range[3], V+		9		40	*		*	V
TEMPERATURE RANGE								
Specification, T_{MIN} to T_{MAX}		–40		85	*		*	°C
Operating		–40		125	*		*	°C
θ_{JA}			80			*		°C/W

* Specification same as XTR103BP.

NOTES: (1) Includes corrected Pt100 nonlinearity for process measurement spans grater than 100°C, and over-temperature zero and span effects. Does not include initial offset and gain errors which are normally trimmed to zero at 25°C. (2) Describes accuracy of the 4mA low-scale offset current. Does not include input amplifier effects. Can be trimmed to zero. (3) Voltage measured with respect to I_O pin. (4) Does not include TCR of gain-setting resistor, R_G. (5) Measured with R_{LIN} = ∞ to disable linearization feature.

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APPLICATION INFORMATION

Figure 1 shows the basic connection diagram for the XTR103. The loop power supply, V_{PS} provides power for all circuitry. Output loop current is measured as a voltage across the series load resistor, R_L.

Two matched 0.8mA current sources drive the RTD and zero-setting resistor, R_Z. The instrumentation amplifier input of the XTR103 senses the voltage difference between the RTD and R_Z. The value of R_Z is chosen to be equal to the resistance of the RTD at the low-scale (minimum) measurement temperature. R_Z can be adjusted to achieve 4mA output at the minimum measurement temperature to correct for input offset voltage of the XTR103.

R_{CM} provides an additional voltage drop to bias the inputs of the XTR103 within their common-mode range. Resistor, R_G, sets the gain of the instrumentation amplifier.

The transfer function through the complete instrumentation amplifier and voltage-to-current converter is:

$$I_O = V_{IN} \bullet (0.016 + 40/R_G) + 4mA,$$

(V_{IN} in volts, R_G in ohms)

where V_{IN} is the differential input voltage. With no R_G connected ($R_G = \infty$), a 0V to 1V input produces a 4-20mA output current. With $R_G = 25\Omega$, a 0V to 10mV input produces a 4-20mA output current. Other values for R_G can be calculated with the formula in Figure 1.

Negative input voltage, V_{IN}, will cause the output current to be less than 4mA. Increasingly negative input will cause the output current to limit at approximately 3.6mA.

Increasingly positive input voltage (greater than V_{FS}) will produce increasing output current according to the transfer function, up to the output current limit of approximately 34mA.

Transistor Q_1 conducts the majority of the signal-dependent 4-20mA loop current. Using an external transistor isolates the majority of the power dissipation from the precision input and reference circuitry of the XTR103, maintaining excellent accuracy. The XTR103 can be operated without this external transistor by connecting pin 11 to 14, however accuracy will be somewhat degraded by the additional internal power dissipation. This effect is most pronounced when the input stage is set for high gain (for low full-scale input voltage).

LINEARIZATION

Linearization circuitry creates a signal-dependent variation in the two matching excitation current sources. This varying excitation provides a 2nd-order term to the transfer function which can be tailored to correct for the nonlinearity of the RTD. The correction is controlled by resistor R_{LIN} which is chosen according to the desired temperature measurement range (see table of values in Figure 1.)

If no linearity correction is desired, do not connect a resistor to the R_{LIN} pins ($R_{LIN} = \infty$). This will cause the excitation current sources to remain a constant 0.8mA.

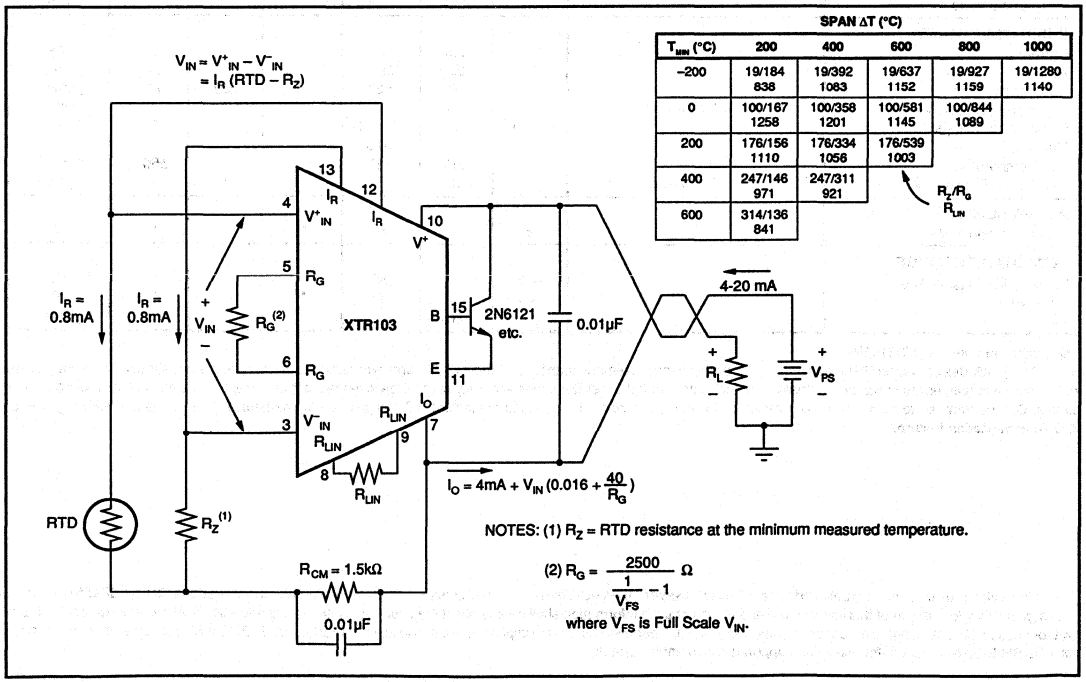

FIGURE 1. Basic RTD Temperature Measurement Circuit.

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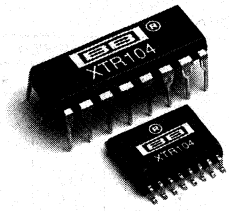


XTR104

4-20mA Current Transmitter with BRIDGE EXCITATION AND LINEARIZATION

FEATURES

- LESS THAN ±1% TOTAL ADJUSTED ERROR, –40°C TO +85°C
- BRIDGE EXCITATION AND LINEARIZATION
- WIDE SUPPLY RANGE: 9V to 40V
- LOW SPAN DRIFT: 50ppm/°C max
- HIGH PSR: 110dB min
- HIGH CMR: 80dB min

APPLICATIONS

- INDUSTRIAL PROCESS CONTROL
- FACTORY AUTOMATION
- SCADA
- WEIGHTING SYSTEMS
- ACCELEROMETERS

DESCRIPTION

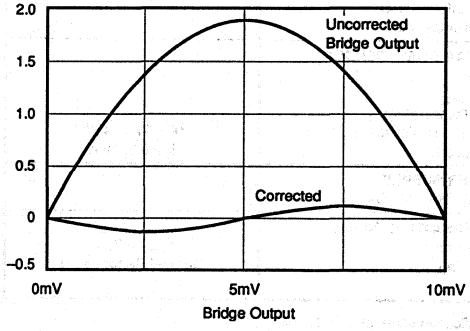
The XTR104 is a monolithic 4-20mA, two-wire current transmitter integrated circuit designed for bridge input signals. It provides complete bridge excitation, instrumentation amplifier, linearization, and current output circuitry necessary for high impedance strain gage sensors.

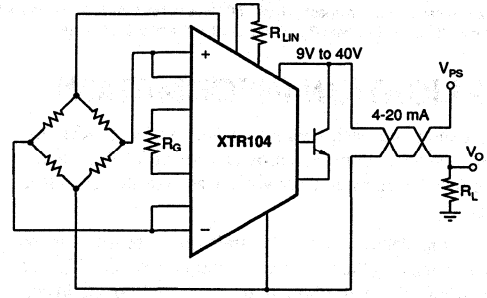
The instrumentation amplifier can be used over a wide range of gain, accommodating a variety of input signals and sensors. Total adjusted error of the complete current transmitter, including the linearized bridge is less than ±1% over the full –40 to +85°C temperature range. This includes zero drift, span drift and non-linearity for bridge outputs as low as 10mV. The XTR104 operates on loop power supply voltages down to 9V.

Versatile linearization circuitry consists of a fully independent instrumentation amplifier that controls the bridge excitation voltage. It provides a second-order correction term to the transfer function, typically achieving a 20:1 improvement in nonlinearity, even with low cost transducers.

The XTR104 is available in 16-pin plastic DIP and SOL-16 surface-mount packages specified for the –40°C to +85°C temperature range. Dice are also available.

BRIDGE NONLINEARITY CORRECTION
USING XTR104





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SPECIFICATIONS

T_A = +25°C, V+ = 24V, and 2N6121 external transistor, unless otherwise noted.

PARAMETER	CONDITIONS	XTR104BP/BU MIN	XTR104BP/BU TYP	XTR104BP/BU MAX	XTR104AP/AU MIN	XTR104AP/AU TYP	XTR104AP/AU MAX	UNITS
OUTPUT								
Output Current Equation			$I_O = V_{IN} \cdot (0.016 + 40/R_G) + 4mA$		V_{IN} in Volts, R_G in Ω			A
Total Adjusted Error[1]	T_{MIN} to T_{MAX}, $V_{FS} \geq 10mV$, $R_B = 5k\Omega$			±1			±2	% of FS
Current, Specified Range		4		20	*		*	mA
Over-Scale Limit			34	40		*	*	mA
Under Scale-Limit			3.6	3.8		*	*	mA
Full Scale Output Error	$V_{IN} = 1V$, $R_G = \infty$		±15	±50		*	±100	µA
Noise: 0.1Hz to 1kHz	$R_G = 40\Omega$		8			*		µAp-p
ZERO OUTPUT[2]	$V_{IN} = 0V$, $R_G = \infty$		4			*		mA
Initial Error			±5	±50		*	±100	µA
vs Temperature			±0.2	±0.5		*	±1	µA/°C
vs Supply Voltage, V+	V+ = 9V to 40V[3]		0.5	2		*	*	µA/V
vs Common-Mode Voltage	V_{CM} = 2V to 3V[3]		0.1	2		*	*	µA/V
SPAN								
Span Equation (Transconductance)			$S = 0.016 + 40/R_G$			*		A/V
Untrimmed Error	$R_G \geq 75\Omega$		±0.1	±1		*	*	%
vs Temperature[4]			±20	±50		*	±100	ppm/°C
Nonlinearity: Ideal Input				0.01			*	%
Bridge Input[5]			0.1			*		%
INPUT								
Differential Range				1			*	V
Common-Mode Range[3]		2		3	*		*	V
Common-Mode Rejection	V_{IN} = 2V to 3V[3]	80	100		*	*		dB
Impedance: Differential			3			*		GΩ
Common-Mode			0.5			*		GΩ
Offset Voltage			±0.5	±2.5		*	*	mV
vs Temperature			1	2.5		2	5	µV/°C
vs Supply Voltage, V+	V+ =9V to 40V[3]	110	130		*	*		dB
Input Bias Current			100	250		*	*	nA
vs Temperature			0.1	2		*	*	nA/°C
Input Offset Current			2	20		*	*	nA
vs Temperature			0.01	0.25		*	*	nA/°C
VOLTAGE REFERENCE[6]								
Voltage			5			*		V
Accuracy			±0.25	±0.5		*	±1	%
vs Temperature			±10	±50		*	±100	ppm/°C
vs Supply Voltage, V+	V+ = 9V to 40V[3]		5			*		ppm/V
vs Load	I_L = 0 to 2mA		50			*		ppm/mA
POWER SUPPLY								
Voltage Range[3], V+		9		40	*		*	V
TEMPERATURE RANGE								
Specification	(T_{MIN} to T_{MAX})	–40		85	*		*	°C
Operating	Derated Performance	–40		125	*		*	°C
θ_{JA}			80			*		°C/W

* Specification same as XTR104BP.

NOTES: (1) Includes corrected second-order nonlinearity of bridge, and over-temperature zero and span effects. Does not include initial offset and span errors which are normally trimmed to zero at 25°C. (2) Describes accuracy of the 4mA low-scale current. Does not include input amplifier effects. Can be trimmed to zero. (3) Voltage measured with respect to I_O pin. (4) Does not include TCR of gain-setting resistor, R_G. (5) When configured to correct for ≤2% second-order bridge sensor nonlinearity. (6) Measured with $R_{LIN} = \infty$ to disable linearization feature.

APPLICATION INFORMATION

Figure 1 shows the basic connection diagram for the XTR104. The loop power supply, V_{PS}, provides power for all circuitry. Loop current is measured as a voltage accross the series load resistor, R_L.

A high impedance (≥2750Ω) strain gage sensor can be excited directly by the 5V reference output terminal, V_R. The output terminals of the bridge are connected to the instrumentation amplifier inputs, V^+_{IN} and V^-_{IN}. The resistor, R_G, sets the gain of the instrumentation amplifier as required by the full-scale bridge voltage, V_{FS}.

The transfer function is:

$$I_O = V_{IN} \cdot (0.016 + 40/R_G) + 4mA,$$

(V_{IN} in Volts, R_G in ohms)

where V_{IN} is the differential input voltage. With no R_G connected ($R_G = \infty$), a 0V to 1V input produces a 4 to 20mA output current. With $R_G = 25\Omega$, a 0V to 10mV input produces a 4-20mA output current. Other values for R_G can be calculated with the formula in Figure 1.

Under-scale input voltage (negative) will cause the output current to decrease below 4mA. Increasingly negative input will cause the output current to limit at approximately 3.6mA.

Increasingly positive input voltage (above V_{FS}) will produce increasing output current according to the transfer function, up to the output current limit of approximately 34mA.

External transistor Q_1 conducts the majority of the signal-dependent 4 to 20mA loop current. An external transistor is used to isolate its power dissipation from the precision input and reference circuitry of the XTR104 to maintain excellent accuracy.

LINEARIZATION

Differential voltage applied to the linearization inputs, V^+_{LIN} and V^-_{LIN} causes the reference voltage, V_R, to vary according to the following equation:

$$V_R \approx 5V + V_{LIN} \bullet \frac{24000}{R_{LIN}}$$

(V_{LIN}, V_R in volts, R_{LIN} in ohms)

With V^+_{LIN} and V^-_{LIN} connected to the bridge output, the bridge excitation voltage can be made to vary as much as ±0.5V in response to the bridge output voltage.

Signal-dependent variation of the bridge excitation voltage provides a second-order term to the complete transfer function (including the bridge). This can be tailored to correct for bridge sensor nonlinearity. Either polarity of nonlinearity (bowing up or down) can be compensated by proper connection of the V_{LIN} inputs. Connecting V^+_{LIN} to V^+_{IN} and V^-_{LIN} to V^-_{IN} causes V_R to increase with bridge output which compensates for a positive bow in the bridge response.

R_{LIN} may be calculated (approximately) as follows:

$$R_{LIN} \approx \frac{120 \bullet V_{FS}}{B}$$

(V_{FS} in mV, B in %, R_{LIN} in ohms)

where B is the end-point nonlinearity to be corrected (in percent of full-scale span). For the example shown on the first page, with a 10mV full scale input, and 1.9% mid-scale nonlinearity, use $R_{LIN} = 632\Omega$.

If no linearity correction is desired, make no connections to the R_{LIN} pins ($R_{LIN} = \infty$). This will cause the V_R output to remain a constant +5V. The V^+_{LIN} and V^-_{LIN} inputs should remain connected to the bridge output to keep these inputs biased in their active region.

BRIDGE BALANCE

Figure 1 shows a bridge trim circuit (R_1, R_2). This adjustment can be used to compensate for the initial accuracy of the bridge and/or to trim the offset voltage of the XTR104. The values of R_1 and R_2 depend on the impedance of the bridge, and the trim range required. This trim circuit places an additional load on the V_R output. The effective load of the trim circuit is nearly equal to R_2. Total load on the V_R output terminal must not be greater than 2mA.

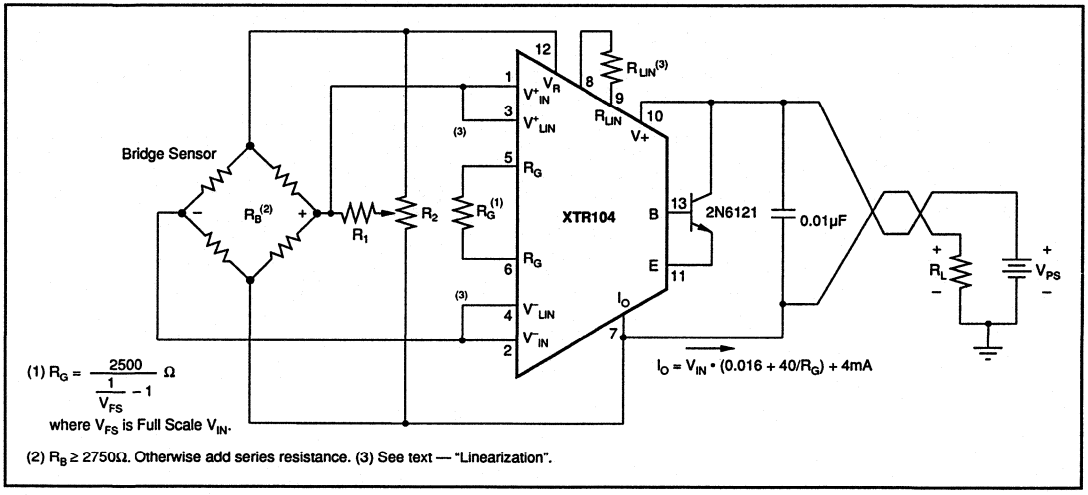

FIGURE 1. Basic Bridge Sensor Application.

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4 Isolation Products

When one or more of the following conditions/requirements are present in an application, an isolation amplifier would generally be the right choice as a signal conditioning device:

- When ohmic isolation between the signal source and the output is a requirement (isolation impedance between the input and the output is >10MΩ).
- When common-mode noise and voltage rejection requirements are >100dB.
- When necessary to process signals in the presence of, or riding on, high common-mode voltages (CMV >> 10V).

In general, most applications can be broadly categorized into the following four types:

- Amplifying and measuring low level signals in the presence of high common-mode voltages.
- Breaking ground loops and/or eliminating source ground connections. The isolation amplifier provides full floating input, eliminating the need for connections to source ground, and thus allowing two-wire hook-up to the signal sources.
- Providing an interface between medical patient monitoring equipment and the transducer/devices that may be in physical contact with the patients. Such applications require high isolation voltage levels and very low leakage currents.
- Providing isolation protection to electronic instruments/equipment. Large common-mode voltages occasionally cause hazardous electronic faults. The low leakage currents and high isolation voltage capabilities of isolation amplifiers help protect instruments against damage caused by such faults.

Isolation amplifier performance requirements vary significantly, depending on the type of requirement. In applications where bandwidth and speed of response are more important than gain accuracy and linearity, the optically or capacitively coupled amplifiers will be the best choice. For applications where gain accuracy and linearity are key parameters, Burr-Brown's family of transformer or capacitively coupled amplifiers are the suitable choice.

The following Selection Guides show parameters for the high grade. Models shown in **boldface** are products included in this supplement.

TRANSFORMER-COUPLED AMPLIFIERS

		Isolation Voltage (V)		Isolation Mode Rejection, typ		Leakage Current at Test	Iso Impedance		Gain Nonlinearity		Voltage Drift	Bias Current	±3dB Freq	Ext Iso Power		
Descrip	Model	Cont Peak	Pulse Test, Peak	DC (dB)	60Hz (dB)	Voltage (μA)	(Ω)	(pF)	max (%)	typ (%)	(±μV/°C) max	max	(kHz)	Req	Temp[1]	Page No.
High Isolation Voltage	3656G	3500	8000	160	125	0.5	10^{12}	6	±0.05	±0.03	5+ (1000/G_I)	100nA	30	No	Ind	4-108
Low Cost Self-Powered	ISO212P	1060	1200[2]	160	115	2	10^{10}	12	±0.025	±0.015	±30 (±30/G_I)	50nA	1	No	Com	S-4.63

NOTES: The package for the 3656G is a DIP, the package for the ISO212P is a SIP. (1) Ind = –25°C to +85°C, Com = 0°C to +70°C. (2) Partial discharge voltage.

OPTICALLY COUPLED AMPLIFIERS

Descrip	Model	Isolation Voltage (V) Cont Peak	Isolation Voltage (V) Pulse/ Test, Peak	Isolation Mode Rejection, typ DC (dB)	Isolation Mode Rejection, typ 60Hz (dB)	Leakage Current at Test Voltage (μA)	Iso Impedance (Ω)	Iso Impedance (pF)	Gain Nonlinearity max (%)	Gain Nonlinearity typ (%)	Voltage Drift (±μV/°C) max	Bias Current max	±3dB Freq (kHz)	Ext Iso Power Req	Temp[1]	Page No.
Balanced Current Input	3650G	2000	5000	140	120	0.35[2]	10^{12}	1.8	±0.05	±0.02	5	40nA	15	Yes	Ind	4-100
Balanced	3652G	2000	5000	140	120	0.35[2]	10^{12}	1.8	±0.1	±0.05	25	50pA	15	Yes	Ind	4-100
Low Drift Wide BW	ISO100P	750	2500	146[3]	108[3]	0.3[2]	10^{12}	2.5	0.07	0.02	2.5[3]	10nA	60	Yes	Ind	4-8

NOTES: All packages are DIPs. (1) Ind = –25°C to +85°C. (2) At 240V/60Hz. (3) R_{IN} = 10kΩ.

CAPACITOR COUPLED, HERMETICALLY SEALED AMPLIFIERS

Descrip	Model	Isolation Voltage (V) Cont Peak	Isolation Voltage (V) Pulse/ Test, Peak	Isolation Mode Rejection, typ DC (dB)	Isolation Mode Rejection, typ 60Hz (dB)	Leakage Current at Test Voltage (μA)	Iso Impedance (Ω)	Iso Impedance (pF)	Gain Nonlinearity max (%)	Gain Nonlinearity typ (%)	Voltage Drift (±μV/°C) max	Bias Current max	Ext ±3dB Freq (kHz)	Isol Power Req	Temp[1]	Page No.
1500VAC Isolation	ISO102B	2121	4000	160	120	1.0	10^{14}	6	±0.003	±0.002	±250	—	70	Yes	Ind	4-20
	ISO120B	**2121**	**2500[2]**	**160**	**115**	**0.5**	10^{14}	**2**	**±0.01**	**±0.005**	**±150**	**—**	**60**	**Yes**	**Ind**	**S-4.39**
	ISO122P	**2121**	**2400[2]**	**160**	**140**	**0.5**	10^{14}	**2**	**±0.02**	**±0.008**	**±200[4]**	**—**	**50**	**Yes**	**Com[3]**	**S-4.52**
3500VAC Isolation	ISO106B	4950	8000	160	130	1.0	10^{14}	6	±0.025	±0.007	±250	—	70	Yes	Ind	4-20
	ISO121B	**4950**	**5600[2]**	**160**	**115**	**0.5**	10^{14}	**2**	**±0.01**	**±0.005**	**±150**	**—**	**60**	**Yes**	**Ind**	**S-4.39**

NOTES: All packages are DIPs. (1) Ind = –25°C to +85°C. Com = 0°C to +70°C. (2) Partial discharge voltage. (3) Not Hermetic. (4) Typical.

ISOLATION POWER SUPPLIES[1]

Description	Model	Isolation Voltage (V) Cont Peak	Isolation Voltage (V) Pulse/ Test Peak	Input Voltage (VDC) min	Input Voltage (VDC) max	Leakage Current 240VAC 60Hz (μA)	Isolation Impedance (Ω)	Isolation Impedance (pF)	Current, Balanced Loads On All Outputs (mA) Rated	Current, Balanced Loads On All Outputs (mA) Max[1]	Sensitivity To Input Change (V/V)	Temp[2]	Page Pkg	No.
Single ±15V Output	700	1500	4200	10	18	1	10^{10}	5	±3-30	±60	1.08	Ind	Mod	4-86
	700U	2000	5000	10	18	1	10^{10}	3	±3-30	±60	1.08	Ind	Mod	4-86
	PWS725A	2121	4000	7	18	2	10^{12}	9	±15	±40	1.15	Ind	DIP	4-65
	PWS726A	4950	8000	7	18	2	10^{12}	9	±15	±40	1.15	Ind	DIP	4-65
Dual ±15V Output	722	4950	8000	5	16	1	10^{10}	6	±3-40	±50	1.13	Ind	Mod	4-92
	PWS727	**1060**	**1200[9]**	**10**	**18**	**1.5**	10^{12}	**8**	**±15**	**±30**	**1.13**	**Com**	**Mod**	**S-4.89**
	PWS728	**1060**	**1200[9]**	**4.5**	**6.0**	**1.5**	10^{12}	**8**	**±15**	**±30**	**3.8**	**Com**	**Mod**	**S-4.89**
Quad ±15V Output	710	1000	3100	10	18	1	10^{10}	8	±9.5	±60	1.08	Ind	Mod	4-88
Quad ±8V Output	724	1000	3000	5	16	1	10^{10}	6	±3-16	±60	0.63	Ind	Mod	4-96
Multiple Output (1-8)	PWS740	2121	4000	7	20	1.5	10^{12}	3	30[3]	60[3]	1.20	Ind	Sys[4]	4-76
	PWS745[8]	**1060**	**1200[9]**	**4.5[5]**	**18[6]**	**1.5**	10^{12}	**8**	**±15**	**30**	[7]	**Ind**	**Comp**	**S-4.96**
	PWS750	**1060**	**1200[9]**	**4.5[5]**	**18[6]**	**1.5**	10^{12}	**8**	**±15**	**30**	[7]	**Ind**	**Comp**	**S-4.105**

NOTES: (1) See complete Product Data Sheet for full specifications, especially regarding output current capabilities. (2) Ind = –25°C to +85°C. Com = 0°C to +70°C. (3) Per channel. (4) 1 TO-3 driver per 8 channels, plus 2 DIPs per channel. (5) 5V operation. (6) 15V operation. (7) 5V operation: 4.12; 15V operation: 1.2. (8) PWS745-1 driver may also be used with PWS740 and PWS750 components. (9) Partial discharge voltage.

CAPACITOR-COUPLED ISOLATION AMPLIFIER, WITH POWER

Description	Model	Isolation Voltage (V) Cont Peak	Isolation Voltage (V) Pulse/ Test, Peak	Isolation Mode Rejection, typ DC (dB)	Isolation Mode Rejection, typ 60Hz (dB)	Leakage Current at Test Voltage (μA)	Iso Impedance (Ω)	Iso Impedance (pF)	Gain Nonlinearity max (%)	Gain Nonlinearity typ (%)	Voltage Drift (±μV/°C) max	Bias Current	±3dB Freq (kHz)	Temp[1]	Page No.
1500VAC Input Power	ISO103	2121	5657	160	130	2.0	10^{12}	9	.05	.018	250	—	20	Ind	S-4.15
1500VAC Output Power	ISO113	2121	5657	160	130	2.0	10^{12}	9	0.02	0.012	250	—	20	Ind	S-4.31
2500VAC Input Power	ISO107	3500	8000	160	100	2.0	10^{12}	13	0.025	0.01	400	—	20	Ind	S-4.23

NOTES: All packages are DIPs. (1) Ind = –25°C to +85°C.

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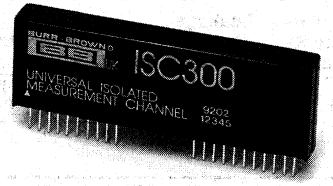


ISC300

ADVANCE INFORMATION
SUBJECT TO CHANGE

Universal Precision Isolated MEASUREMENT CHANNEL

FEATURES

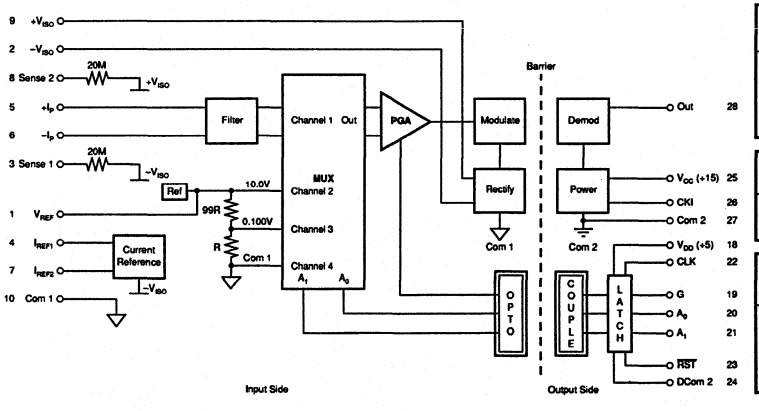
- CALIBRATION CAPABILITY
- INTEGRAL SENSOR EXCITATION
- OPEN CIRCUIT SENSOR DETECTION
- LOW POWER: 80mW
- INSTRUMENT AMPLIFIER INPUT
- PROGRAMMABLE GAIN
- 12-BIT LINEARITY
- TWO ISOLATED POWER SUPPLIES: ±13V at 5mA
- LOW DRIFT 10V REFERENCE

APPLICATIONS

- UNIVERSAL INPUT CHANNEL FOR PROCESS CONTROL SYSTEMS
- ISOLATED MEASUREMENT CHANNEL FOR THERMOCOUPLE, RTD AND VOLTAGE TRANSDUCERS
- CHANNEL TO CHANNEL ISOLATED MULTIPLEXED SYSTEMS
- ISOLATED 4 TO 20mA RECEIVER

DESCRIPTION

The ISC300 is an isolated measurement channel with open circuit sensor detection for use with RTD and thermocouple temperature sensors. In addition to temperature measurement, the ISC300 can accept full scale input voltages of ±100mV and ±10V which allows use with other sensors such as pressure, humidity and flow sensors. The low level resistance measurement capability also allows stimulus and measurement of strain gauges. The measurement channel has a highly stable internal reference which can be selected from the output side. This allows the user to calibrate each channel at the factory, record the calibration data and periodically recalibrate the system while in use over time and ambient temperature changes.



INPUT SELECT	A_1	A_0
Com,	0	0
+0.1V	0	1
+10V	1	0
Signal	1	1

GAIN SELECT	G
0.5	0
50	1

SELECT and GAIN	$\overline{RST}$	CLK
No Change	1	0
No Change	1	1
Latch	1	^
RESET	0	X

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Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL

At V_{CC} = 15V, V_{DD} = 5V, T_A = +25°C unless otherwise noted.

PARAMETER	CONDITIONS	ISC300 MIN	ISC300 TYP	ISC300 MAX	UNITS
ISOLATION					
Isolation Voltage (V_{ISO})	AC60Hz Continuous	500			Vrms
	AC60Hz Continuous	±700			V_{PEAK}
	V_{ISO}, DC	700			V
	Partial Discharge[1]	800			Vrms
Isolation Mode Rejection (IMR)	V_{ISO} = Rated 60Hz Cont[2]	110			dB
Barrier Impedance			2 || 15		GΩ || pF
Leakage Current (I_{ISO})	V_{ISO} = 240 Vrms 60Hz			4	µArms
GAIN					
Voltage Gains			50, 0.5		V/V
Resistance Conversion			10		mV/Ω
Initial Error				±3	%
vs Temperature	0°C to +70°C		±30	±50	ppm/°C
Nonlinearity	V_O = –5V to +5V[4]		±0.01	±0.025	%
INPUT OFFSET VOLTAGE					
Initial Offset (Input Referred)	V_{IN} = 0V G = 0.5			±200	mV
	V_{IN} = 0V G = 50			±5	mV
vs Temperature	0°C to +70°C G = 0.5			±200	µV/°C
	0°C to +70°C G = 50			±5	µV/°C
vs Supply (V_{CC})	V_{CC} = 14V to 16V		±1.5		mV/V
INPUT CURRENT					
Initial Bias			35	50	nA
vs Temperature	–40°C to +85°C		100		pA/°C
INPUT					
Voltage Range	Rated Operation G = 0.5V Input			±10	V
	Rated Operation G = 50V Input			±0.1	V
Resistance Range	Rated Operation G = 50 3-wire Resistance	0		500	Ω
Peak Voltage	Applied to Any Signal Input Wrt Com 1[5]			±380	V
Impedance: Differential		10			MΩ
Common Mode Rejection	CMR at DC Gain = 0.5[3]	66	75		dB
	CMR at DC Gain = 50[3]	75	100		dB
	CMR at 60Hz[3]	60	70		dB
Source Impedance Imbalance	For Normal Operation < 1kΩ Imbalance			10	kΩ
OUTPUT					
Voltage Range	Min Load = 1MΩ			±5	V
Overrange Voltage	During Input Fault (V_{IN} < –11V or V_{IN} > 11V)	±5.4			V
Output Impedance			3		kΩ
Ripple Voltage	f = 0 to 5kHz Min Load 1MΩ		0.5		mVrms
	f = 0 to 100kHz Min Load 1MΩ		10		mVp-p
FREQUENCY RESPONSE					
Input Bandwidth			3.5		Hz
Input Settling Time			0.5		s
Input Overload Recovery			5		s
Output Overload Settling Time	T_{SETT}, to within 5% for V_{IN} < 14V		1	5	ms
Output Overload Recovery			2		ms
VOLTAGE REFERENCE					
V_{REF1} (Internal and External)			10		V
Initial Accuracy	External Loading of 100nA		±0.1	±1	%
vs Temperature			±10	±20	ppm/°C
vs Time				±20	ppm/kHr
vs Supply (V_{CC})					%/V
V_{REF2} (Internal)			100		mV
Initial Accuracy[6]			±0.1	±1	%
vs Temperature			±10	±20	ppm/°C
vs Time				±20	ppm/kHr
vs Supply (V_{CC})					%/V

SPECIFICATIONS (CONT)

ELECTRICAL

At V_{CC} = 15V, V_{DD} = 5V, T_A = +25°C unless otherwise noted.

PARAMETER	CONDITIONS	ISC300 MIN	ISC300 TYP	ISC300 MAX	UNITS
POWER SUPPLIES					
Analog Supply Range	V_{CC} Pin	14		16	V
Supply Current	No External Load		5	10	mA
Digital Supply Range	V_{DD} Pin	4		6	V
Supply Current			1	3	mA
Total Power Dissipation	No External Load		80	184	mΩ
Isolated Supplies: Voltage	at 5mA Each Supply	11.5	13		V
Current			5		mA
INPUT O/C SENSE					
Sense Current	I_{S2}, Sense 1 = 0V		0.7		µA
	$-I_{S2}$, Sense 2 = 0V		0.7		µA
REFERENCE CURRENT					
Reference Current (I_{REF1})		199	200	201	µA
Reference Currents Ratio	I_{REF1} : I_{REF2}			±0.5	%
DIGITAL INPUTS A_0, A_1, G, CLK, $\overline{RST}$ (74HC EQUIVALENT)					
High-Level Input Voltage		3.5			V
Low-Level Input Voltage				1.5	V
Input Rise and Fall Times (t_R, t_f)	CLK $\overline{RST}$ A_0, A_1, G			450	ns
Pulse Width (t_W)	CLK, $\overline{RST}$	20			ns
Setup (t_{SU})	Data Change to CLK High	20			ns
Hold (t_{HO})	Data Change from CLK High	5			ns
Release (t_{REC})	$\overline{RST}$ High to CLK High	5			ns
CLOCK SYNC CKI					
Input Voltage - High Level	V_{CC} = 15V	11			V
Input Voltage - Low Level	V_{CC} = 15V			4	V
Input Current - High Level	V_{IL} = 11V V_{CC} = 15V		350		µA
Input Current - Low Level	V_{IL} = 4V V_{CC} = 15V		350		µA
Input Frequency		45	50	55	kHz
Input Duty Cycle		45		55	%
TEMPERATURE RANGE					
Specification		0		70	°C
Operating		0		70	°C
Storage		–40		85	°C

NOTES: (1) See "High Voltgage Testing" Section. (2) IMR is defined with respect to the voltage between Com 1 and Com 2 with both inputs tied to Com 1. (3) CMR is defined with respect to the input common, Com 1, only. (4) Deviation from a straight line between the end points of the output voltage. (5) Device output remains monotonic. (6) Limit referred to V_{REF1}.

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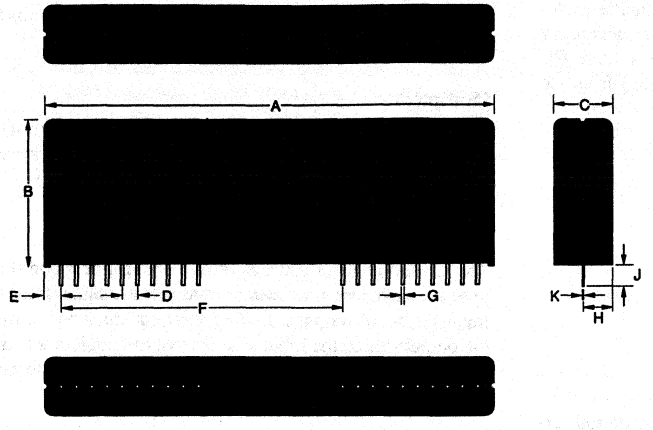
MECHANICAL



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	2.998	3.010	76.15	76.45
B	.994	1.006	25.25	25.55
C	.327	.350	8.30	8.90
D	.093	.106	2.35	2.70
E	.146	.158	3.71	4.01
F	1.693	1.707	43.00	43.35
G	.019	.021	0.48	0.53
H	.163	.175	4.15	4.45
J	.120	.160	3.05	4.06
K	.009	.011	0.23	0.28
L	.014	.026	0.35	0.65

PIN CONFIGURATION

Bottom View

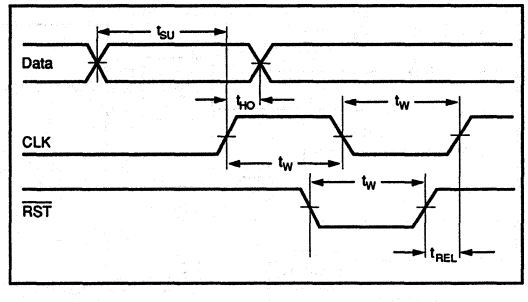
1	10V Ref
2	$-V_{SS1}$
3	Sense 1
4	I_{REF1}
5	+In
6	–In
7	I_{REF2}
8	Sense 2
9	$+V_{SS1}$
10	Com 1
18	V_{DD} (+5V)
19	G
20	A_0
21	A_1
22	CLK
23	$\overline{RST}$
24	DCom 2
25	V_{CC} (+15V)
26	CKI
27	Com 2
28	Out

ABSOLUTE MAXIMUM RATINGS

Signal Input Voltage	±380V
Analog Supply Voltage V_{CC}	18V
Digital Supply Voltage V_{DD}	7V
Voltage Across Barrier	800Vrms
Storage Temperature Range	–45°C to +100°C
Lead Temperature (soldering, 10s)	+300°C
Out Short Circuit Duration	Continuous to Com 2
Relative Humidity (non-condensing)	95% RH

NOTES: Stresses exceeding those listed above may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TIMING INFORMATION



THEORY OF OPERATION

The ISC300 has no galvanic connection between the input and output sections. The differential input signal is multiplied by the programmable gain amplifier and accurately transferred across the isolation barrier to the output. The output section demodulates the signal transferred from the input section and transfers power to the input section.

ISC300 DESIGN

The ISC300 consists of:

- A filtered differential high impedance input.
- Precision matched current sources.
- Fault detect bias resistors.
- Digitally selectable internal calibration references.
- Digitally selectable gain.
- Isolation of all digital and analog signals.
- Isolated DC/DC converter.
- Synchronizable internal oscillator.
- Two isolated power supplies available for external circuitry.
- Externally available 10V reference.

INPUT SECTION

Filter

Since the ISC300 is designed to measure slowly changing processes, the input filter is set for a cut off frequency of 2Hz. This gives good noise rejection at power frequencies of 50Hz and 60Hz.

Sense Lines

The two sense lines can be configured to detect short or open circuits e.g. transducer burn out. This would be indicated by an out of range output (see Input Configuration in Applications section).

Multiplexer

The multiplexer is used to route either the measurement channel or the precision voltage references (used in system calibration) to the programmable gain amplifier.

Isolation Barrier

The isolation barrier consists of two transformers and three opto couplers. One transformer transmits the signal from the input side to the output side. The other transmits power from the output side to the input side. The opto-couplers are used to isolate the logic used for mux select, gain and reference voltage control.

Voltage Reference

The voltage reference provides 10V, 0.1V and 0V references for channel calibration. The 10V reference is also available externally.

Current References

Two matched 200µA current references are available for the excitation of RTDs or for use in external signal conditioning circuitry.

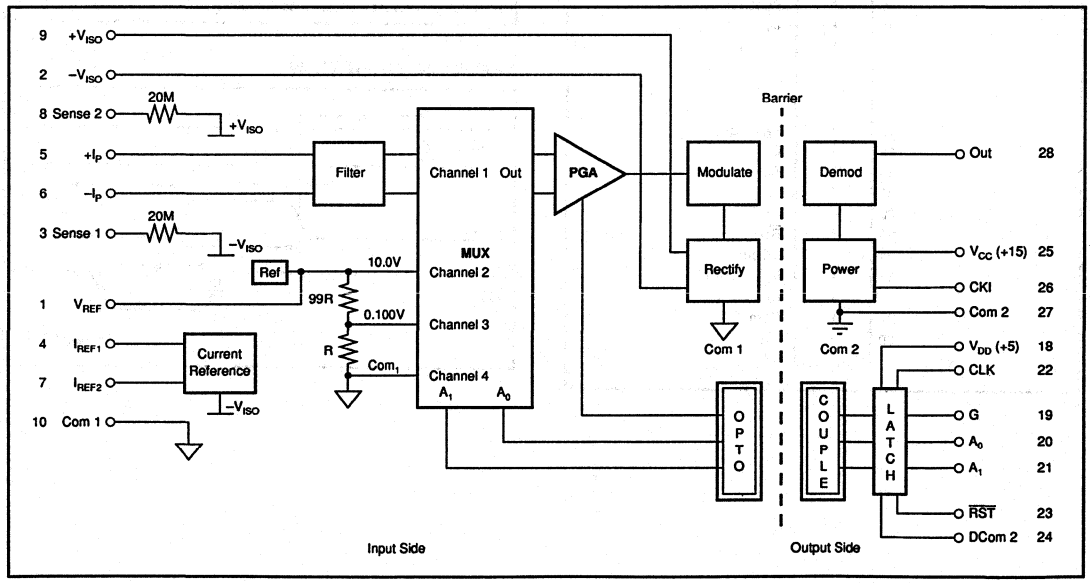


FIGURE 1. ISC300 Block Diagram.

PGA

The programmable gain amplifier allows the user to digitally select device gains of 0.5 and 50, allowing input ranges of ±0.1V or, ±10V full scale. When used in conjunction with the 0.1V, 10V and common references, channel calibration can be performed.

Isolated Supplies

Two 13V isolated supplies, capable of supplying 5mA each, are available to power signal conditioning circuitry.

OUTPUT SECTION

The output section passes power across the isolation barrier to provide the isolated supplies, and demodulates the signal transmitted back across the isolation barrier.

ABOUT THE BARRIER

For any isolation product, barrier integrity is of paramount importance in achieving high reliability. The ISC300 uses miniature transformers designed to give maximum isolation performance when encapsulated in a high dielectric strength material. The device is designed so that the barrier is located at the center of the package.

HIGH VOLTAGE TESTING

Burr-Brown Corporation has adopted a partial discharge test criterion that conforms to the German VDE0884 Optocoupler Standards. This method requires the measurement of minute current pulses (<5pC) while applying 800Vrms, 60Hz high-voltage stress across every device isolation barrier. During a two second test partial discharge must occur five times on five separate half cycles of 60Hz, and each time occurrence must not be separated by a line period of more than four half cycles in order to produce a partial discharge fail. This confirms transient overvoltage (1.6 x V_{rated}) protection without damage. Life-test results verify the absence of failure under continuous rated voltage and maximum temperature.

This new test method represents the "state-of-the-art" for nondestructive high voltage reliability testing. It is based on the effects of non-uniform fields existing in heterogeneous dielectric material during barrier degradation. In the case of void non-uniformities, electric field stress begins to ionize the void region before bridging the entire high voltage barrier.

The transient conduction of charge during and after the ionization can be detected externally as a burst of 0.01µs – 0.1µs current pulses that repeat on each AC voltage cycle. The minimum AC barrier voltage that initiates partial discharge is defined as the "inception voltage." Decreasing the barrier voltage to a lower level is required before partial discharge ceases and is defined as the "extinction voltage."

We have designed and characterized the package to yield an inception voltage in excess of 800Vrms so that transient overvoltages below this level will not cause any damage. The extinction voltage is above 500Vrms so that even overvoltage-induced partial discharge will cease once the barrier voltage is reduced to the rated level. Older high voltage test methods relied on applying a large enough overvoltage (above rating) to catastrophically break down marginal parts, but not so high as to damage good ones. Our new partial discharge testing gives us more confidence in barrier reliability than breakdown/no breakdown criteria.

BASIC OPERATION

SIGNAL AND SUPPLY CONNECTIONS

As with any mixed signal analog and digital signal component, correct decoupling and signal routing precautions must be observed to optimize performance. The ISC300 has an internal 0.1µF decoupling capacitor at V_{CC}, so additional V_{CC} decoupling will not be necessary. However, a ground plane will minimize potential noise problems. If a low impedance ground plane is not used, Com 2 should be tied directly to the ground at the supply. It is not necessary to connect DCom 2 and Com 2 at the device. Layout practices associated with isolation signal conditioners are very important. The capacitance associated with the barrier and series resistance in the signal and reference leads must be minimized. Any capacitance across the barrier will increase AC leakage, and in conjunction with ground line resistance, may degrade high frequency IMR, see Figure 2.

INPUT CONFIGURATION

The ISC300 allows easy configuration for temperature measurement using an RTD. Figure 3 shows the basic connections for RTD operation. The two reference currents excite the resistance transducer and a current-to-voltage conversion is made corresponding to the resistance value of the transducer. If a gain of 50 is selected, a 10Ω resistance value results in a (10 • 200µA) • 50 = 0.1V output; the 500Ω full scale value gives a (500 • 200µA) • 50 = 5V output. The connection of the sense line allows open circuit sensor detection. An open circuit will give a corresponding >5.1V output. A short circuit will give a corresponding <0.1V output. See the Applications section under Fault Conditions for more information.

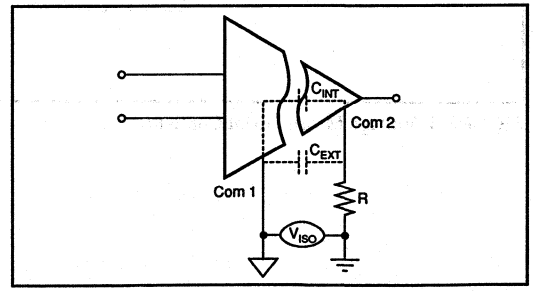


FIGURE 2. Barrier Capacitance.

Figure 4 shows the configuration for voltage measurement. A full scale input range of ±10V can be accepted by the ISC300. The two sense lines can be connected to give open or short circuit detection. An open circuit will result in an output of <–5.1V and a short circuit will give a <0.1V output. See the Applications section under Fault Conditions for more information.

Figure 7 shows a possible circuit configuration using jumpers to select voltage or RTD operation.

ISOLATED SUPPLIES

The two isolated supplies available on the input side are capable of supplying ±11.5V min at 5mA. These can be used to provide power for external front-end circuitry for additional signal processing. When using the isolated supplies, it is necessary to decouple them as close to the device as possible. 10µF tantalum capacitors should be used. This will also improve the signal-to-noise ratio.

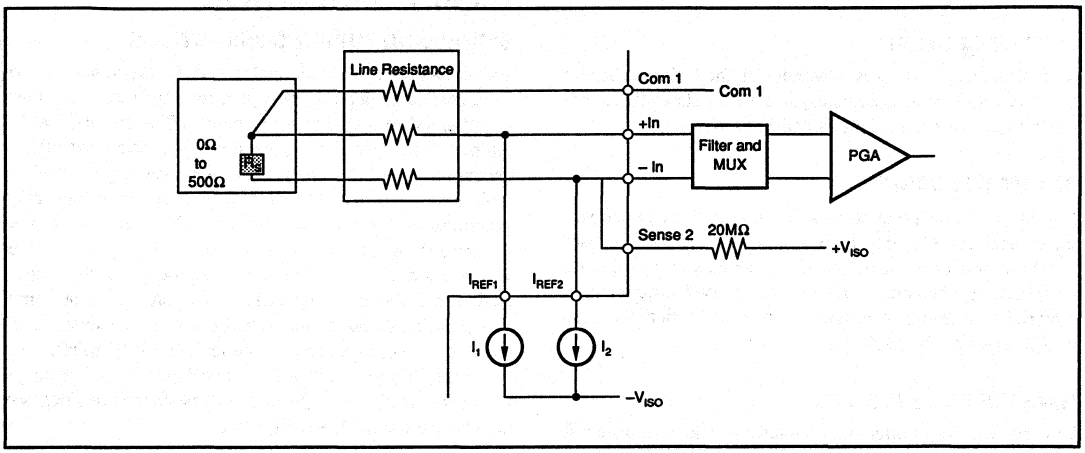


FIGURE 3. Resistance Measurement Configuration.

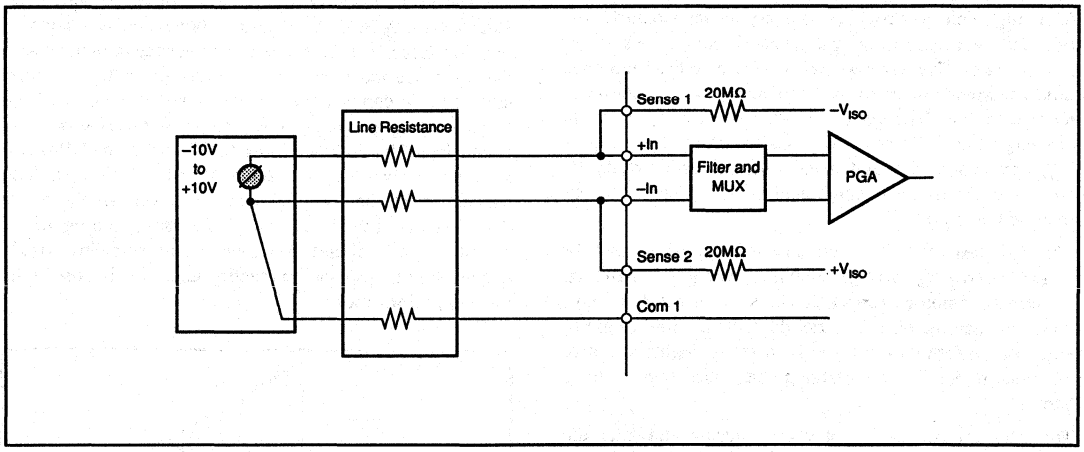


FIGURE 4. Voltage Measurement Configuration.

MEASUREMENT CHANNEL

CALIBRATION

The ISC300 is designed to allow easy system calibration using its internal voltage reference. Programming pins A_0, A_1 and G allows offset and full scale errors in gains of 0.5 and 50 to be measured.

INPUT SELECT	A_1	A_0	GAIN SELECT	G	SELECT AND GAIN	$\overline{RST}$	CLK
Com 1	0	0	0.5	0	No Change	1	0
+0.1V	0	1	50	1	No Change	1	1
+10V	1	0			Latch	1	^
Signal	1	1			RESET	0	X

System calibration would typically proceed as follows:

Lab Calibration

- Set ISC300 gain.
- Set input to 0V reference, measure Offset.
- Connect external precision V reference, measure Gain.
- Remove external V reference and set input to 10V or 0.1V reference.

Offset and Gain are now calibrated to an external precision reference—record the numbers.

Field Calibration

- Set ISC300 gain.
- Set input to 0V reference, measure Offset.
- Set input to 10V or 0.1V, measure Gain.
- Recalibrate system.

SYNCHRONIZATION

As the internal modulation frequencies of several ISC300s can be marginally different, 'beat' frequencies ranging from a few Hz to a few kHz can exist in multi ISC300 applications. The internal clock (see Figure 5) starts when power is applied and runs at typically 50kHz. The ISC300 design accommodates 'internal synchronous' noise which is caused by minute timing differences, but synchronous beat frequency noise will not be strongly attenuated, especially at low frequencies if it is introduced via the power, signal or ground paths. To overcome this problem, the design allows the synchronization of each oscillator in the system to one frequency. This is done by connecting the CKI (clock in) pins of each ISC300 in the system together (see Figure 6). The ISC300 can also be synchronized by an external clock driver.

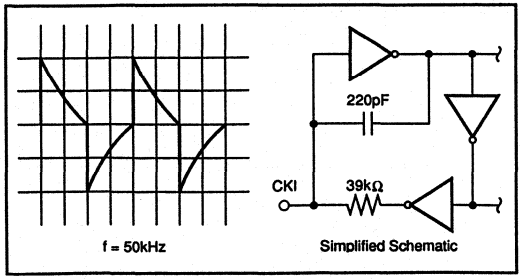


FIGURE 5. CKI Input.

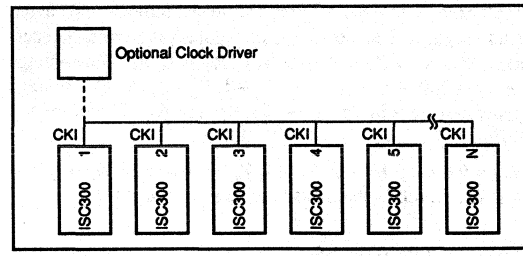


FIGURE 6. Synchronizing Multi-ISC300 Applications.

NOISE

Output noise is generated by the residual components of the 25kHz carrier that have not been removed from the signal. This noise may be reduced by adding an output low pass filter (see Figure 15 for an example of a 2 pole filter with amplification, giving a ±10V output). The filter time constants should be set below the carrier frequency. The output of the ISC300 is a switched capacitor and requires a high impedance load to prevent degradation of linearity. Loads of less than 1MΩ will cause an increase in noise at the carrier frequency and will appear as ripple in the output waveform.

APPLICATIONS

This section describes the design criteria of various applications of the ISC300.

2, 3 AND 4 WIRE RESISTANCE MEASUREMENTS

Two wire resistance measurements are prone to errors due to lead resistances. The voltage error can be significant since the voltmeter measures on the lines supplying the RTD

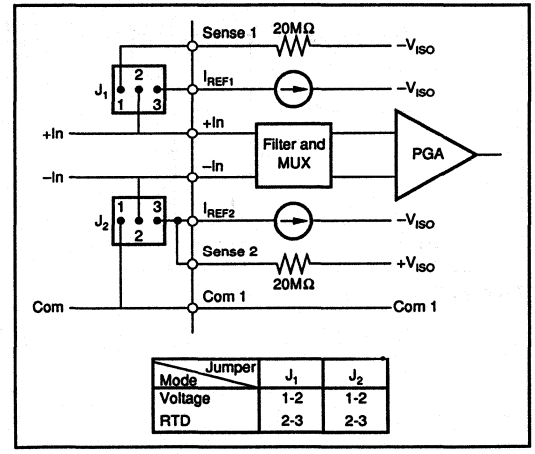


FIGURE 7. Mode Selection Jumpers.

excitation current. Four wire measurements avoid this problem by measuring the voltage generated across the RTD on a second pair of wires. Very little current flows through the voltmeter, therefore the lead resistance error contribution is negligible. Three wire resistance measurements also avoid lead length resistance errors. In Figure 3 the voltage generated at –In is $(I_1 + I_2)\ R_L + I_2\ R_S + I_2\ R_L$. The voltage generated at +In is $(I_1 + I_2)\ R_L + I_2\ R_S + I_1\ R_L$. The voltage generated at +In is $(I_1 + I_2)\ R_L + I_2\ R_L$. Therefore the difference voltage into the ISC300 is:

$V_{IN} = ((I_1 + I_2)\ R_L + I_2\ R_S + I_2\ R_L)) - ((I_1 + I_2)\ R_L + I_2\ R_L))$
$= I_2\ R_S$, which is the voltage across R_S, the RTD.

FAULT CONDITIONS

The ISC300 can be configured to detect line or transducer faults which may occur in a system. Figures 8 to 14 show how the output of the ISC300 will reflect these various fault conditions by giving corresponding out of range outputs.

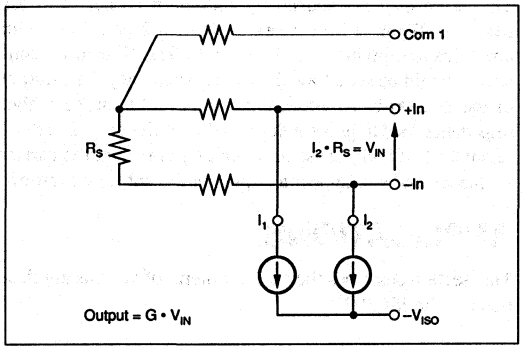


FIGURE 8. Normal Operation.

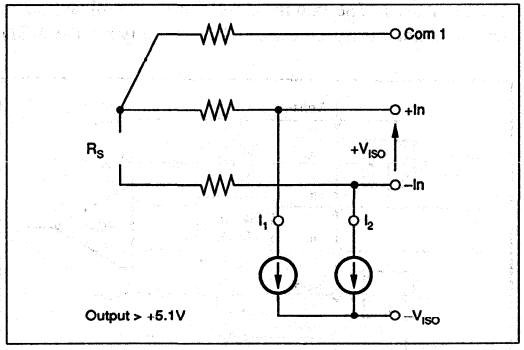


FIGURE 9. R_S Open Circuit.

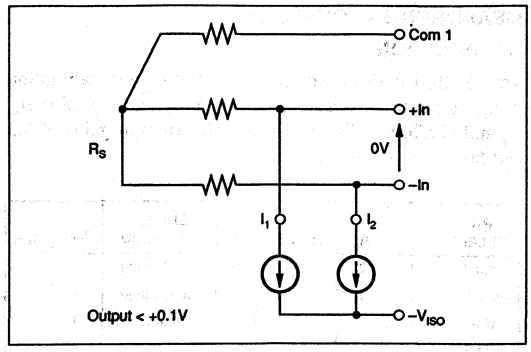


FIGURE 10. R_S Short Circuit.

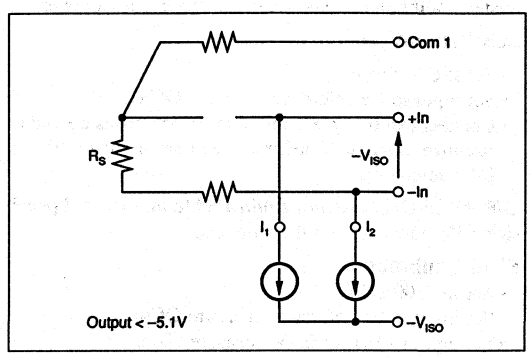


FIGURE 11. +In Open Circuit.

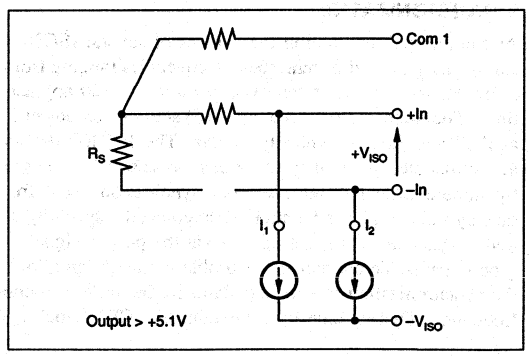


FIGURE 12. –In Open Circuit.

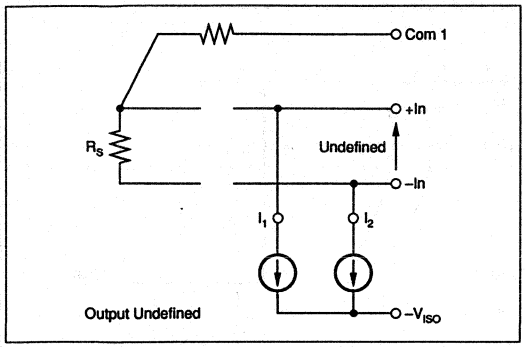


FIGURE 13. –In and +In Open Circuit.

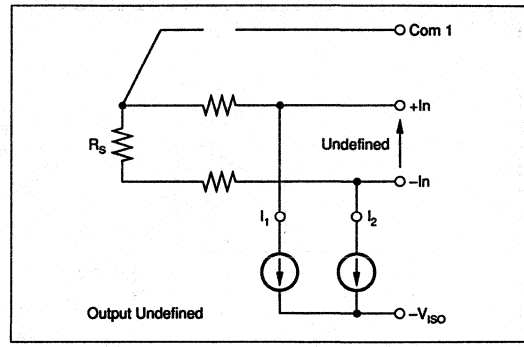


FIGURE 14. Com 1 Open Circuit.

APPLICATIONS FLEXIBILITY

ISOLATED VOLTAGE MEASUREMENT CHANNEL

Figure 15 shows the ISC300 configured for a ±10V input. With a few external components the ISC300 can accurately convert a ±10V input to an isolated ±10V output with no external adjustments. The primary function of the output circuitry is to add gain to convert the ±5V output of the ISC300 to ±10V, and to reduce output impedance. The addition of a few resistors and capacitors provides an active low pass filter with a cut off frequency of typically 200Hz. The filter response is flat to 1dB and rolls off from cut off at –12dB per octave.

ISOLATED MEASUREMENT BRIDGE CIRCUIT

Figure 16 shows a measurement bridge circuit using the ISC300. All the input circuitry is powered by the ISC300 isolated supplies. The OPA1013 dual op amp is used to excite the measurement bridge and the INA102 is used to amplify the bridge delta voltage. Connecting pins 4 and 7 together, and pins 5 and 6 together on the INA102 sets its gain to 1000.

ISOLATED 4 TO 20MA RECEIVER

In Figure 17, the ISC300 converts a 4 to 20mA current to an isolated 0 to 5V output. The 6.25Ω resistor converts the 4 to 20mA input to 0.025 to 0.125V. The 125Ω resistor in conjunction with the 200µA current source provides an offset of –0.025V. Fine offset and gain adjustment gives an accurate 0 to 0.1V input range.

Offset and Gain Adjustment

- Adjust R_1 for 5V change on the output corresponding to 16mA change on the input.
- Adjust R_2 with 4mA input for 0V output.

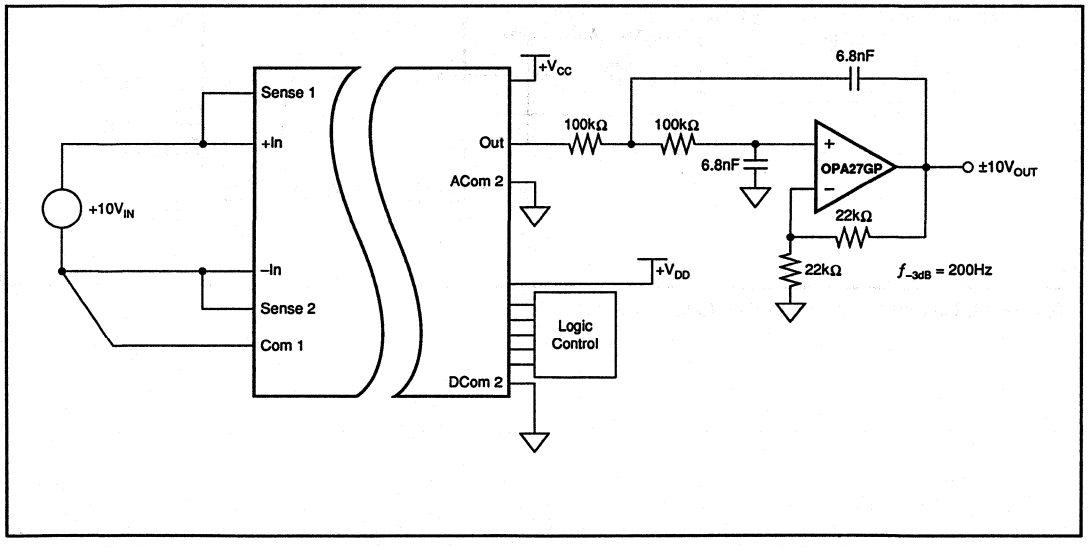


FIGURE 15. Isolated Voltage Measurement Channel with Output Filter.

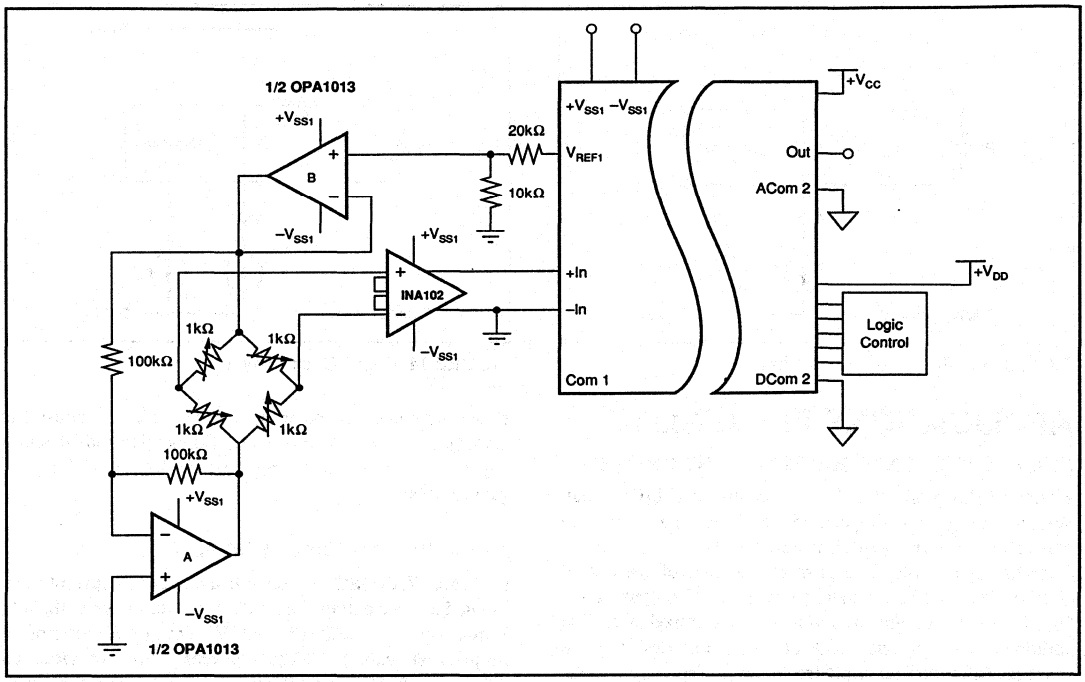


FIGURE 16. Isolated Instrument Bridge System.

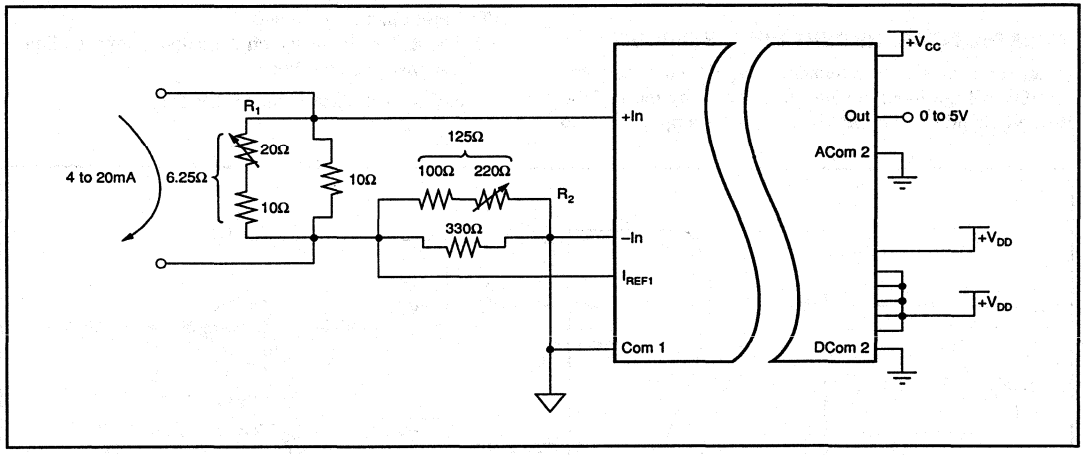


FIGURE 17. Isolated 4 to 20mA receiver (0 to 5V output).

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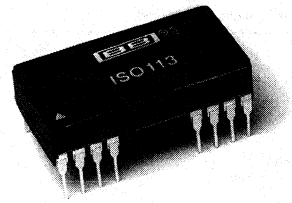


ISO103

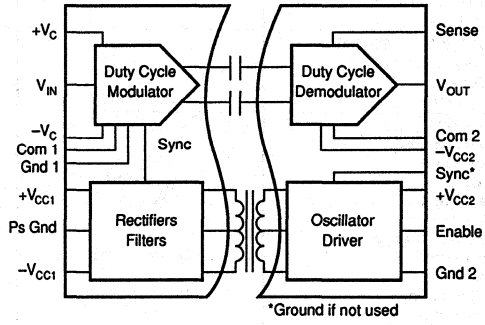
Low-Cost, Internally Powered ISOLATION AMPLIFIER

FEATURES

- SIGNAL AND POWER IN ONE DOUBLE-WIDE (0.6") SIDE-BRAZED PACKAGE
- 5600Vpk TEST VOLTAGE
- 1500Vrms CONTINUOUS AC BARRIER RATING
- WIDE INPUT SIGNAL RANGE: –10V to +10V
- WIDE BANDWIDTH: 20kHz Small Signal, 20kHz Full Power
- BUILT-IN ISOLATED POWER: ±10V to ±18V Input, ±50mA Output
- MULTICHANNEL SYNCHRONIZATION CAPABILITY (TTL)
- BOARD AREA ONLY 0.72in.² (4.6cm²)

APPLICATIONS

- MULTICHANNEL ISOLATED DATA ACQUISITION
- ISOLATED 4-20mA LOOP RECEIVER AND POWER
- POWER SUPPLY AND MOTOR CONTROL
- GROUND LOOP ELIMINATION



DESCRIPTION

The ISO103 isolation amplifier provides both signal and power across an isolation barrier. The ceramic non-hermetic hybrid package with side-brazed pins contains a transformer-coupled DC/DC converter and a capacitor-coupled signal channel.

Extra power is available on the isolated input side for external input conditioning circuitry. The converter is protected from shorts to ground with an internal current limit, and the soft-start feature limits the initial currents from the power source. Multiple-channel synchronization can be accomplished by applying a TTL clock signal to paralleled Sync pins. The Enable control is used to turn off transformer drive while keeping the signal channel demodulator active. This feature provides a convenient way to reduce quiescent current for low power applications.

The wide barrier pin spacing and internal insulation allow for the generous 1500Vrms continuous rating. Reliability is assured by 100% barrier breakdown testing that conforms to UL1244 test methods. Low barrier capacitance minimizes AC leakage currents.

These specifications and built-in features make the ISO103 easy to use, as well as providing for compact PC board layouts.

International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL

At T_A = +25°C and V_{CC2} = ±15V, ±15mA output current unless otherwise noted.

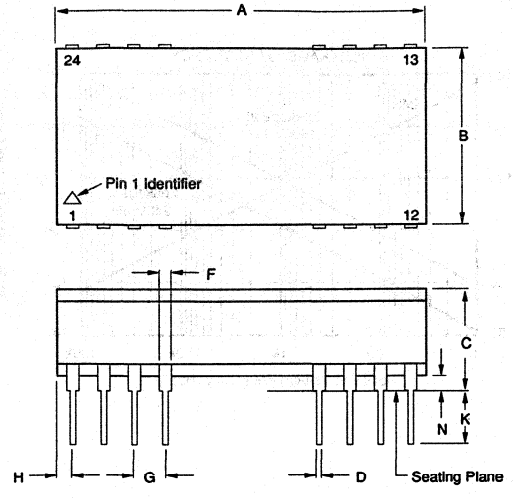
PARAMETER	CONDITIONS	ISO103 MIN	ISO103 TYP	ISO103 MAX	ISO103B MIN	ISO103B TYP	ISO103B MAX	UNITS
ISOLATION								
Rated Continuous Voltage[1]								
AC, 60Hz	T_{MIN} to T_{MAX}	1500			*			Vrms
DC	T_{MIN} to T_{MAX}	2121			*			VDC
Test Breakdown, 100% AC, 60Hz	10s	5657			*			Vpk
Isolation-Mode Rejection	1500Vrms, 60Hz		130			*		dB
	2121VDC		160			*		dB
Barrier Impedance			10^{12} || 9			*		Ω || pF
Leakage Current	240Vrms, 60Hz		1	2		*	*	µA
GAIN								
Nominal			1			*		V/V
Initial Error			±0.12	±0.3		±0.08	±0.15	% FSR
Gain vs Temperature			±60	±100		±20	±50	ppm/°C
Nonlinearity	V_O = –10V to 10V		±0.026	±0.05		±0.018	±0.025	% FSR
	V_O = –5V to 5V		±0.009			*		%FSR
INPUT OFFSET VOLTAGE								
Initial Offset			±20	±60		*	*	mV
vs Temperature			±300	±500		±100	±250	µV/°C
vs Power Supplies	V_{CC2} = ±10V to ±18V		0.9			*		mV/V
vs Output Supply Load	I_O = 0 to ±50mA		±0.3			*		mV/mA
SIGNAL INPUT								
Voltage Range	Output Voltage in Range	±10	±15		*	*		V
Resistance			200			*		kΩ
SIGNAL OUTPUT								
Voltage Range		±10	±12.5		*	*		V
Current Drive		±5	±20		*	*		mA
Ripple Voltage, 800kHz Carrier			25			*		mVp-p
400Ω/4.7nF (See Figure 4)			5			*		mVp-p
Capacitive Load Drive			1000			*		pF
Voltage Noise			4			*		µV/√Hz
FREQUENCY RESPONSE								
Small Signal Bandwidth			20			*		kHz
Slew Rate			1.5			*		V/µs
Settling Time	0.1%, –10/10V		75			*		µs
POWER SUPPLIES								
Rated Voltage, V_{CC2}			±15			*		V
Voltage Range		±10		±18	*		*	V
Input Current	I_O = ±15mA		+90/–4.5			*		mA
Ripple Current	No Filter		60			*		mAp-p
C_{IN} = 1µF			3			*		mAp-p
Rated Output Voltage		±14.25	±15	±15.75	*	*	*	V
Output Current	Balanced Load		±15	±50		*	*	mA
Single			30	100		*	*	mA
Load Regulation	Balanced Load		0.3			*		%/mA
Line Regulation			1.12			*		V/V
Output Voltage vs Temperature			2.5			*		mV/°C
Voltage Balance Error, $\pm V_{CC1}$			0.05			*		%
Voltage Ripple (800kHz)	No External Capacitors		50			*		mVp-p
C_{EXT} = 1µF			5			*		mVp-p
Output Capacitive Load				1			*	µF
Sync Frequency	TTL, 50% Duty Cycle	1.25	1.6	2	*	*	*	MHz
TEMPERATURE RANGE								
Specification		–25		+85	*		*	°C
Operating		–25		+85	*		*	°C
Storage		–25		+125	*		*	°C

* Specifications same as ISO103.

NOTE: (1) Conforms to UL1244 test methods. 100% tested at 1500Vrms for 1 minute.

MECHANICAL

G Package — 24-Pin Ceramic DIP



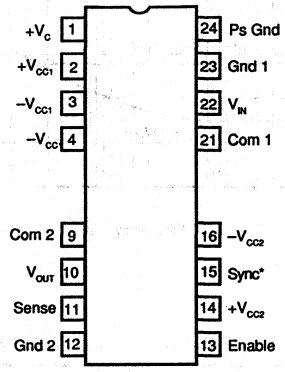
DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.180	1.220	29.97	30.99
B	.580	.600	14.73	15.24
C	.310	.370	7.87	9.40
D	.016	.020	0.41	0.51
F	.040 TYP		1.02 TYP	
G	.100 BASIC		2.54 BASIC	
H	.044	.056	1.12	1.42
J	.009	.012	0.23	0.30
K	.165	.185	4.19	4.70
L	.600	.620	15.24	15.75
N	.040	.060	1.02	1.52

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.

ABSOLUTE MAXIMUM RATINGS

Supply Without Damage	±18V
V_{IN}, Sense Voltage	±50V
Com 1 to Gnd 1 or Com 2 to Gnd 2	±200mV
Enable, Sync	0V to $+V_{CC2}$
Continuous Isolation Voltage	1500Vrms
V_{ISO}, dv/dt	20kV/µs
Junction Temperature	150°C
Storage Temperature	–25°C to +125°C
Lead Temperature,10s	300°C
Output Short to Gnd 2 Duration	Continuous
$\pm V_{CC1}$ to Gnd 1 Duration	Continuous

PIN CONFIGURATION



*Operation requires this pin be grounded or driven with TTL levels.

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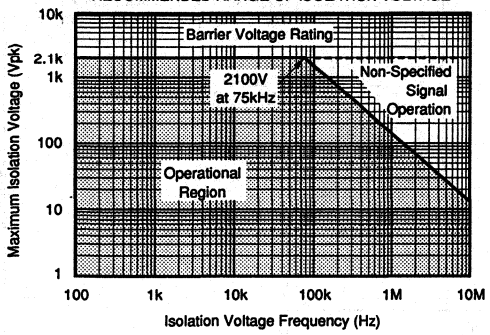
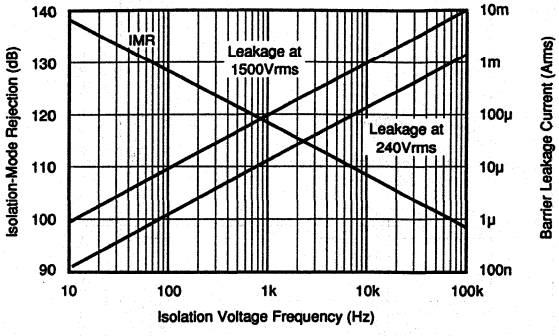
TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_{CC2} = ±15VDC, ±15mA output current unless otherwise noted.

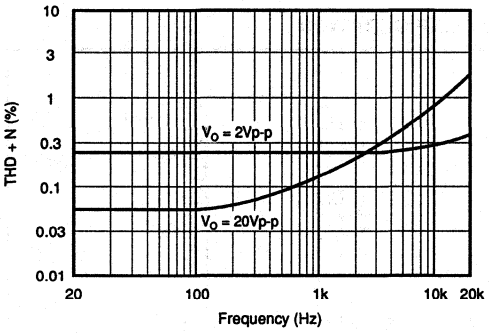
RECOMMENDED RANGE OF ISOLATION VOLTAGE



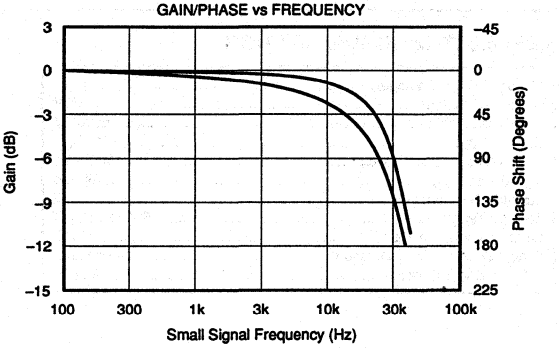
IMR/LEAKAGE vs FREQUENCY



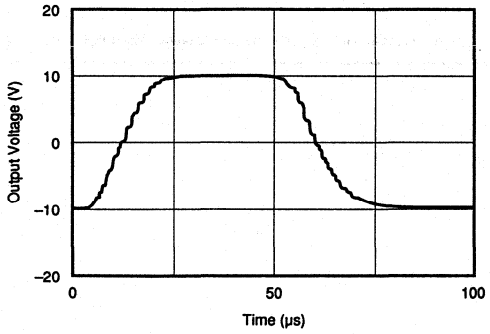
DISTORTION vs FREQUENCY



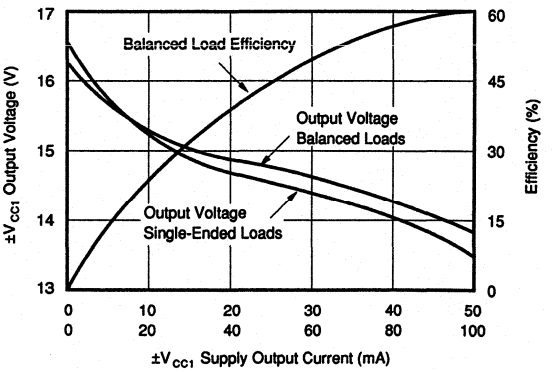
GAIN/PHASE vs FREQUENCY



LARGE SIGNAL TRANSIENT RESPONSE



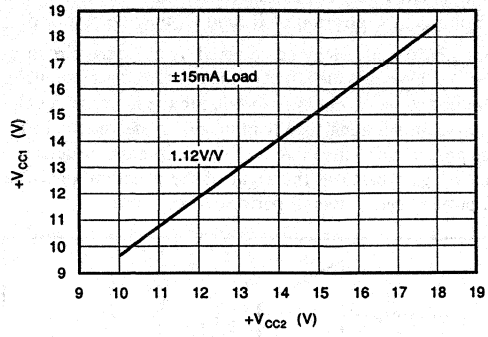
ISOLATED POWER SUPPLY
LOAD REGULATION AND EFFICIENCY



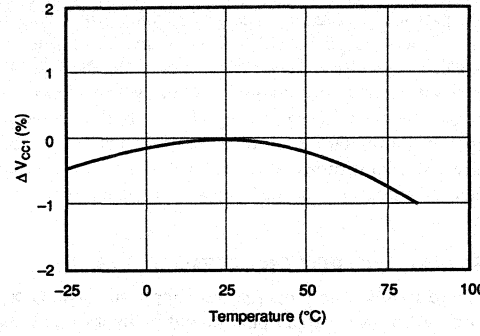
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_{CC2} = ±15VDC, ±15mA output current unless otherwise noted.

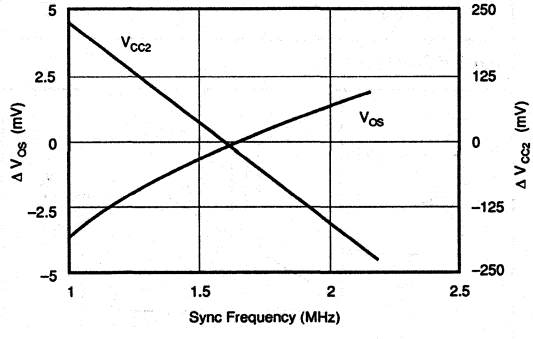
ISOLATED POWER SUPPLY LINE REGULATION



ISOLATION POWER SUPPLY VOLTAGE vs TEMPERATURE



ISOLATED SUPPLY VOLTAGE AND V_{OS} vs SYNC FREQUENCY



THEORY OF OPERATION

The block diagram on the front page shows the isolation amplifier's synchronized signal and power configuration, which eliminate beat frequency interference. A proprietary 800kHz oscillator chip, power MOSFET transformer drivers, patented square core wirebonded transformer, and single chip diode bridge provide power to the input side of the isolation amplifier as well as external loads. The signal channel capacitively couples a duty-cycle encoded signal across the ceramic high-voltage barrier built into the package. A proprietary transmitter-receiver pair of integrated circuits, laser trimmed at wafer level, and coupled through a pair of matched "fringe" capacitors, result in a simple, reliable design.

SIGNAL AND POWER CONNECTIONS

Figure 1 shows the proper power supply and signal connections. All power supply pins should be bypassed as shown with the π filter for $+V_{CC2}$, an option recommended if more than ±15mA are drawn from the isolated supply. Separate rectifier output pins ($\pm V_{CC1}$) and amplifier supply input pins ($\pm V_C$) allow additional ripple filtering and/or regulation. The separate input and output common pins and output sense are low current inputs tied to the signal source ground, output ground, and output load, respectively, to minimize errors due to IR drop in long conductors. Otherwise, connect Com 1 to Gnd 1, Com 2 to Gnd 2, and Sense to V_{OUT} at the ISO103 socket. The enable pin may be left open if the ISO103 is continuously operated. If not, a TTL low level will disable the internal DC/DC converter. The Sync input must be grounded for unsynchronized operation while a 1.25MHz to 2MHz TTL clock signal provides synchronization of multiple units.

OPTIONAL GAIN AND OFFSET ADJUSTMENTS

Rated gain accuracy and offset performance can be achieved with no external adjustments, but the circuit of Figure 2a may be used to provide a gain trim of ±0.5% for the values shown; greater range may be provided by increasing the size of R_1 and R_2. Every 2kΩ increase in R_1 will give an additional 1% adjustment range, with $R_2 \geq 2R_1$. If safety or convenience dictate location of the adjustment potentiometer on the other side of the barrier from the position shown in Figure 2a, the position of R_1 and R_2 may be reversed.

Gains greater than 1 may be obtained by using the circuit of Figure 2b. Note that the effect of input referred errors will be multiplied at the output in proportion to the increase in gain. Also, the small-signal bandwidth will be decreased in inverse proportion to the increase in gain. In most instances, a precision gain block at the input of the isolation amplifier will provide better overall performance.

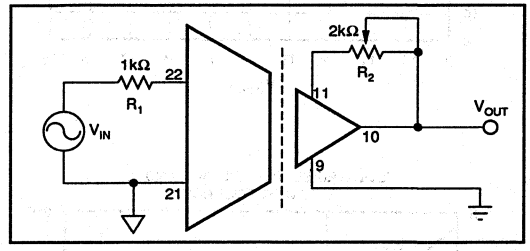


FIGURE 2a. Gain Adjust.

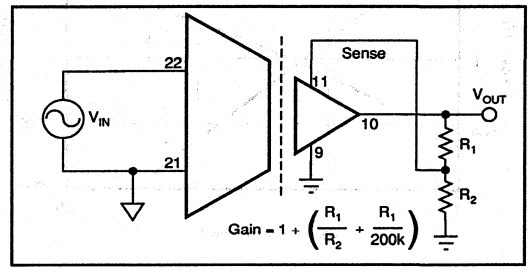


FIGURE 2b. Gain Setting.

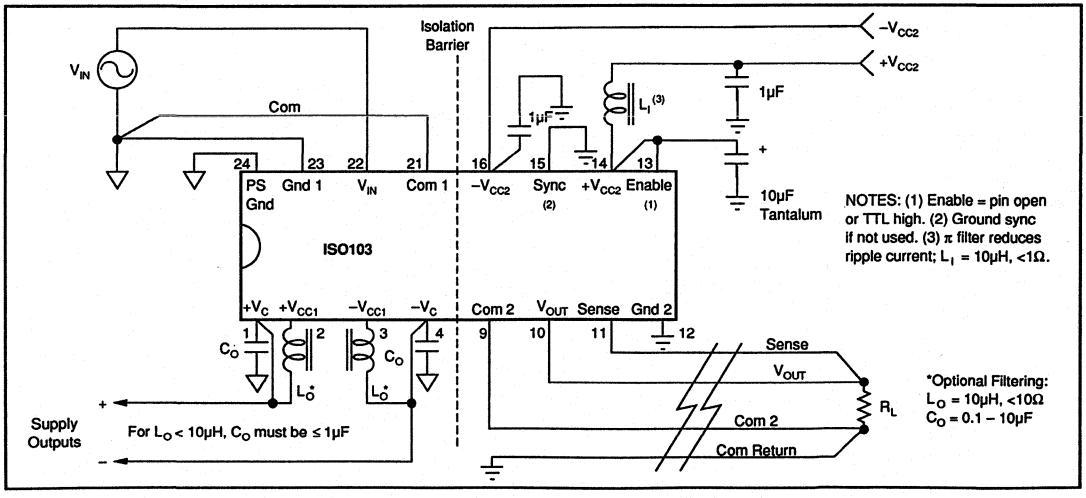


FIGURE 1. Signal and Power Connections.

Figure 3 shows a method for trimming V_{OS} of the ISO103. This circuit may be applied to either Signal Com (input or output) as desired for safety or convenience. With the values shown, ±15V supplies and unity gain, the circuit will provide ±150mV adjustment range and 0.25mV resolution with a typical trim potentiometer. The output will have some sensitivity to power supply variations. For a ±100mV trim, power supply sensitivity is 8mV/V at the output.

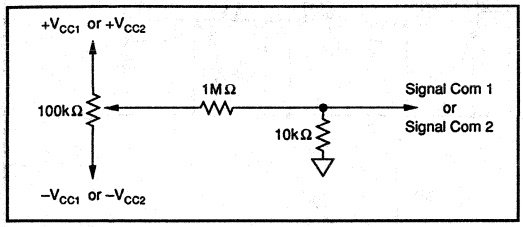


FIGURE 3. V_{OS} Adjust.

OPTIONAL OUTPUT FILTER

Figure 4 shows an optional output ripple filter that reduces the 800kHz ripple voltage to <5mVp-p without compromising DC performance. The small signal bandwidth is extended above 30kHz as a result of this compensation.

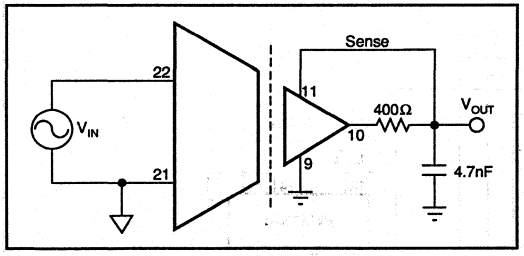


FIGURE 4. Ripple Reduction.

MULTICHANNEL SYNCHRONIZATION

Synchronization of multiple ISO103s can be accomplished by connecting pin 15 of each device to an external TTL level oscillator, as shown in Figure 7. The PWS750-1 oscillator is convenient because its nominal synchronizing output frequency is 1.6MHz, resulting in a 800kHz carrier in the ISO103 (its nominal unsynchronized value). The open collector output typically switches 7.5mA to a 0.2V low level so that the external pull-up resistor can be chosen for different pull-up voltages as shown in Figure 7. The number of channels synchronized by one PWS750-1 is determined by the total capacitance of the sync voltage conductors. They must be less than 1000pF to ensure TTL level switching at 800kHz. At higher frequencies the capacitance must be proportionally lower.

Customers can supply their own TTL level synchronization logic provided the frequency is between 1.25MHz and 2MHz, and the duty cycle is greater than 25%.

Multichannel synchronization with reduced power dissipation for applications requiring less than ±15mA from V_{CC1} is accomplished by driving both the Sync input pin (15) and Enable pin (13) with the TTL oscillator as shown in Figure 5.

ISOLATION BARRIER VOLTAGE

The typical performance of the ISO103 under conditions of barrier voltage stress is indicated in the first two performance curves—Recommended Range of Isolation Voltage and IMR/ Leakage vs Frequency. At low barrier modulation levels, errors can be determined by the IMRR characteristic. At higher barrier voltages, typical performance is obtained as long as the dv/dt across the barrier is below the shaded area in the first curve. Otherwise, the signal channel will be interrupted, causing the output to distort, and/or shift DC level. This condition is temporary, with normal operation resuming as soon as the transient subsides. Permanent damage to the integrated circuits occurs only if transients exceed 20kV/µs. Even in this extreme case, the barrier integrity is assured.

HIGH VOLTAGE TESTING

The ISO103 was designed to reliably operate with 1500Vrms continuous isolation barrier voltage. To confirm barrier integrity, a two-step breakdown test is performed on 100% of the units. First, a 5600V peak, 60Hz barrier potential is applied for 10s to verify that the dielectric strength of the insulation is above this level. Following this exposure, a 1500Vrms, 60Hz potential is applied for one minute to conform to UL1244. Life-test results show reliable operation under continuous rated voltage and maximum operating temperature conditions.

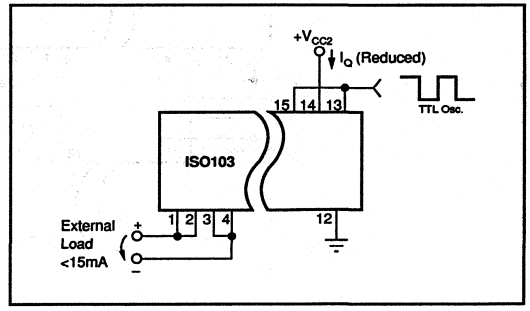


FIGURE 5. Reduced Power Dissipation.

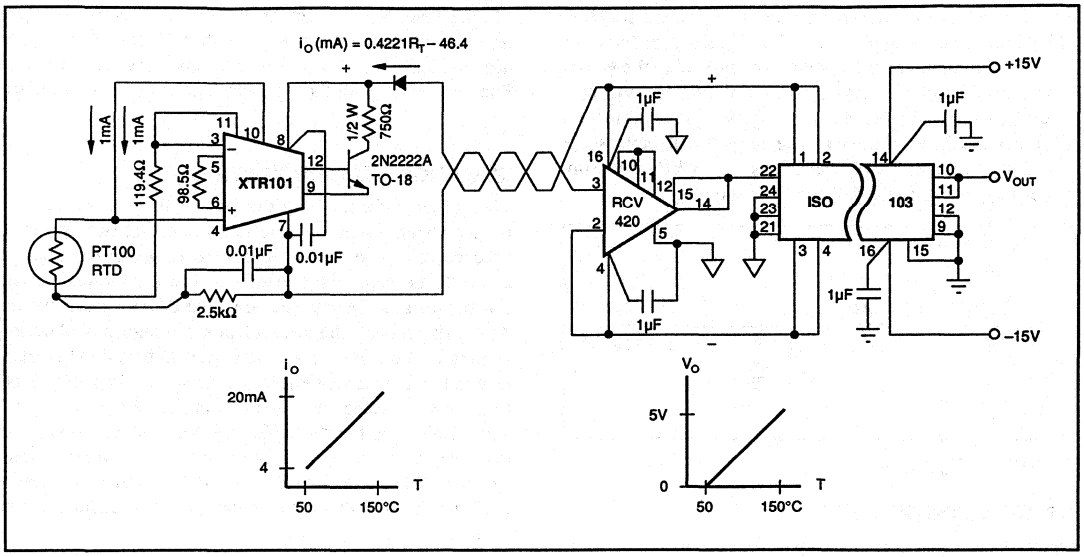


FIGURE 6. Isolated 4-20mA Instrument Loop.

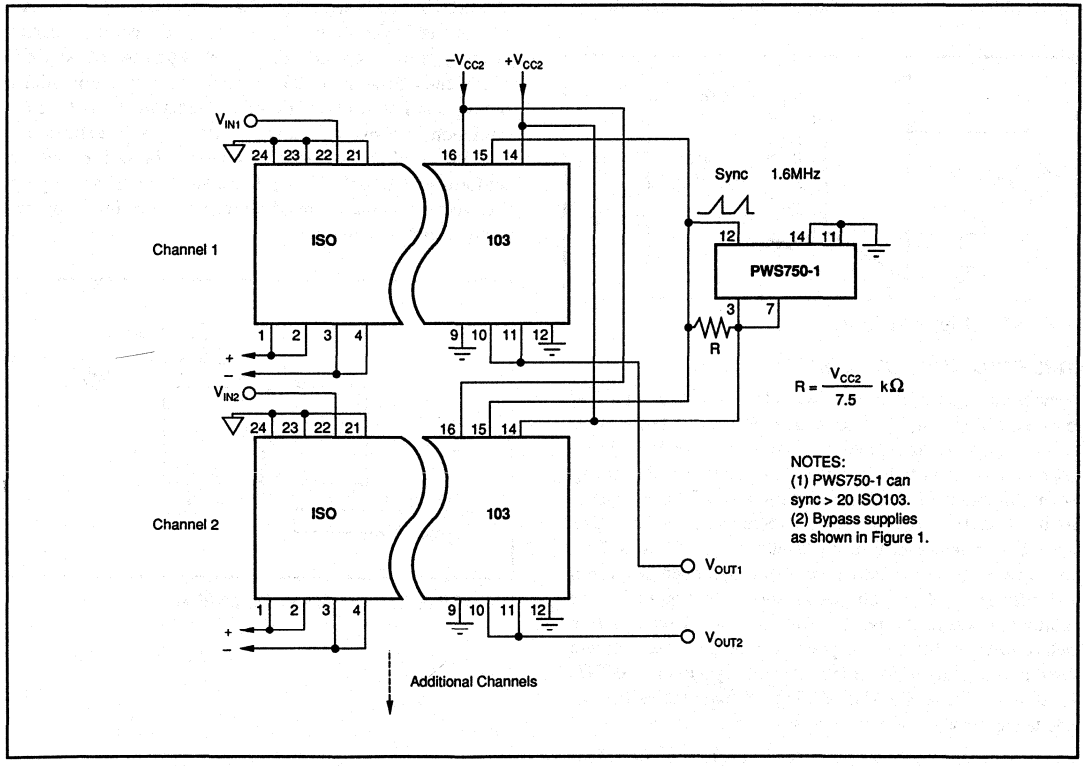


FIGURE 7. Synchronized-Multichannel Isolation.

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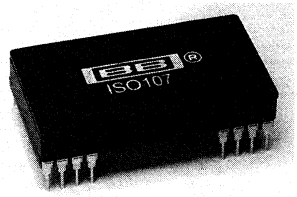


ISO107

High-Voltage, Internally Powered ISOLATION AMPLIFIER

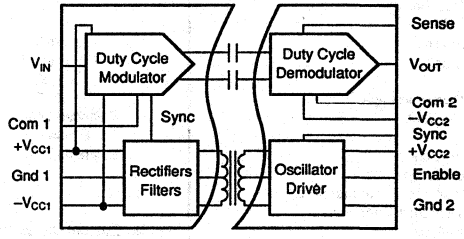
FEATURES

- SIGNAL AND POWER IN ONE TRIPLE-WIDE PACKAGE
- 8000Vpk TEST VOLTAGE
- 2500Vrms CONTINUOUS AC BARRIER RATING
- WIDE INPUT SIGNAL RANGE: –10V to +10V
- WIDE BANDWIDTH: 20kHz Small Signal, 20kHz Full Power
- BUILT-IN ISOLATED POWER: ±10V to ±18V Input, ±50mA Output
- MULTICHANNEL SYNCHRONIZATION CAPABILITY (TTL)

APPLICATIONS

- MULTICHANNEL ISOLATED DATA ACQUISITION
- BIOMEDICAL INSTRUMENTATION
- POWER SUPPLY AND MOTOR CONTROL
- GROUND LOOP ELIMINATION

ISO107 BLOCK DIAGRAM



DESCRIPTION

The ISO107 isolation amplifier provides both signal and power across an isolation barrier. The ceramic side-brazed hybrid package contains a transformer-coupled DC/DC converter and a capacitor-coupled signal channel.

Extra power is available on the isolated input side for external input conditioning circuitry. The converter is protected from shorts to ground with an internal current limit, and the soft-start feature limits the initial currents from the power source. Multiple-channel synchronization can be accomplished by applying a TTL clock signal to paralleled Sync pins. The Enable control is used to turn off transformer drive while keeping the signal channel demodulator active. This feature provides a convenient way to reduce quiescent current for low power applications.

The wide barrier pin spacing and internal insulation allow for the generous 2500Vrms continuous rating. Reliability is assured by 100% barrier breakdown testing that conforms to UL544 test methods. Low barrier capacitance minimizes AC leakage currents.

These specifications and built-in features make the ISO107 easy to use, as well as providing for compact PC board layouts.

International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL

T_A = +25°C and V_{CC2} = ±15V, ±15mA output current unless otherwise noted.

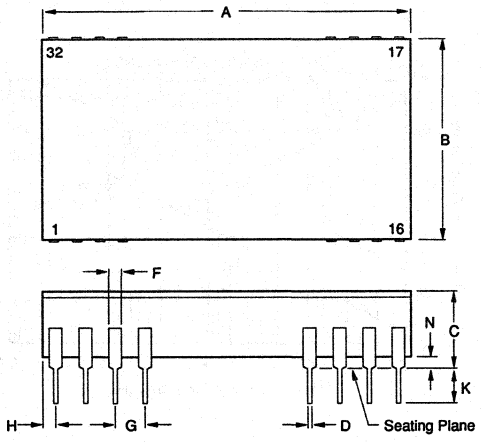
PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNITS
ISOLATION					
Rated Continuous Voltage [1]					
AC, 60Hz	T_{MIN} to T_{MAX}	2500			Vrms
DC	T_{MIN} to T_{MAX}	3500			VDC
Test Breakdown, AC, 60Hz	10s	8000			Vpk
Isolation-Mode Rejection	2500Vrms, 60Hz		100		dB
	2121VDC		160		dB
Barrier Impedance			10^{12} || 13		Ω || pF
Leakage Current	240Vrms, 60Hz		1.2	2	µA
GAIN					
Nominal			1		V/V
Initial Error			±0.1	±0.25	% FSR
Gain vs Temperature			±50	±120	ppm/°C
Nonlinearity			±0.01	±0.025	% FSR
INPUT OFFSET VOLTAGE					
Initial Offset			±20	±50	mV
vs Temperature			±150	±400	µV/°C
vs Power Supplies	V_{CC2} = ±10V to ±18V		±2		mV/V
INPUT					
Voltage Range	Output Voltage in Range	±10	±15		V
Resistance			200		kΩ
SIGNAL OUTPUT					
Voltage Range		±10	±12.5		V
Current Drive		±5	±20		mA
Ripple Voltage, 800kHz Carrier (See Figure 4)			20		mVp-p
Capacitive Load Drive			1000		pF
Voltage Noise			4		µV/√Hz
FREQUENCY RESPONSE					
Small Signal Bandwidth			20		kHz
Slew Rate			1.5		V/µs
Settling Time	0.1%, –10/10V		75		µs
POWER SUPPLIES					
Rated Voltage, V_{CC2}			±15		V
Voltage Range		±10		±18	V
Input Current	I_O = ±15mA[2]		+75/–4.5		mA
Ripple Current	No Filter		10		mAp-p
	C_{IN} = 1µF		3		mAp-p
Rated Output Voltage		±14.25	±15	±15.75	V
Output Current	Balanced Load		±15	±50	mA
	Single		30	100	mA
Load Regulation	Balanced Load		0.5		%/mA
Line Regulation			1.18		V/V
Output Voltage vs Temperature			10		mV/°C
Voltage Balance Error, ±V_{CC1}			0.05		%
Voltage Ripple	No External Capacitors		10		mVp-p
Output Capacitive Load (See Figure 1)				1	µF
Sync Frequency	TTL, 50% Duty Cycle	1.25	1.6	2	MHz
TEMPERATURE RANGE					
Specification		–25		+85	°C
Operating		–25		+85	°C
Storage		–25		+125	°C

NOTES: (1) Conforms to UL544 test methods. 100% tested at 2500Vrms for 1 minute. (2) For other conditions, see Performance Curve, Input Current (+V_{CC2}) vs Output Current. Input Current (–V_{CC2}) is constant at –4.5mA (typ) for all output currents.

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

MECHANICAL

P Package — 32-Pin Plastic DIP



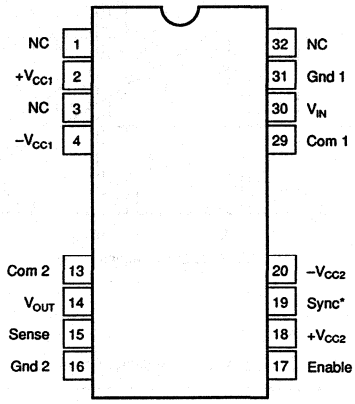
	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.580	1.620	40.13	41.15
B	.880	.900	22.35	22.86
C	.310	.370	7.87	9.40
D	.016	.020	0.41	0.51
F	.040 TYP		1.02 TYP	
G	.100 BASIC		2.54 BASIC	
H	.044	.056	1.12	1.42
J	.009	.012	0.23	0.30
K	.125	.180	3.18	4.57
L	.900	.920	22.86	23.37
N	.040	.060	1.02	1.52

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.

ABSOLUTE MAXIMUM RATINGS

Supply Without Damage	±18V
V_{IN}, Sense Voltage	±50V
Com 1 to Gnd 1 or Com 2 to Gnd 2	±200mV
Enable, Sync	0V to $+V_{CC2}$
Continuous Isolation Voltage	2500Vrms
V_{ISO} dv/dt	20kV/µs
Junction Temperature	150°C
Storage Temperature	–25°C to +125°C
Lead Temperature, 10s	300°C
Output Short to Gnd 2 Duration	Continuous
$\pm V_{CC1}$ to Gnd 1 Duration	Continuous

PIN CONFIGURATION



*Operation requires that this pin be grounded or driven with TTL levels.

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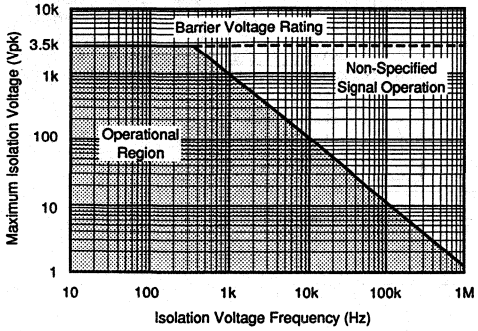
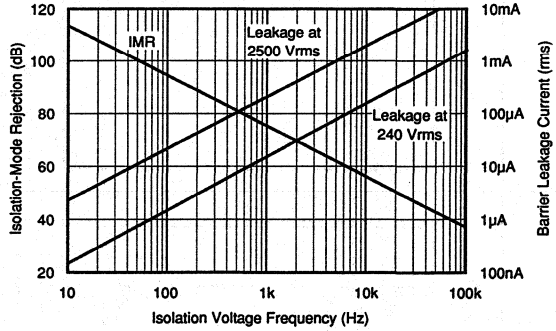
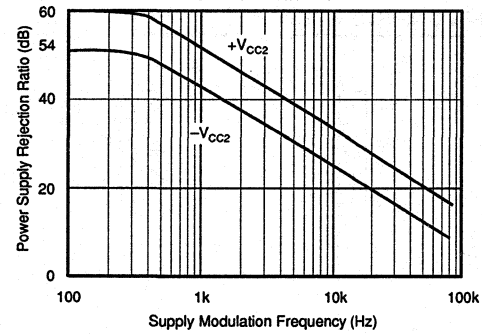
RECOMMENDED RANGE OF ISOLATION VOLTAGE



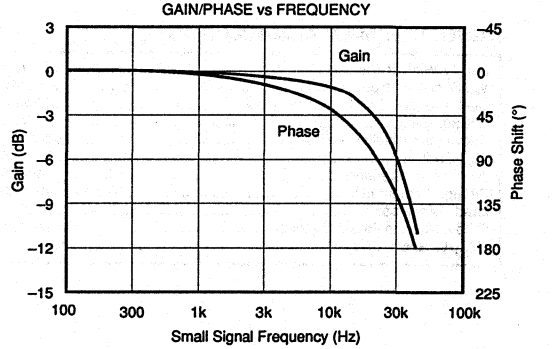
IMR/LEAKAGE vs FREQUENCY



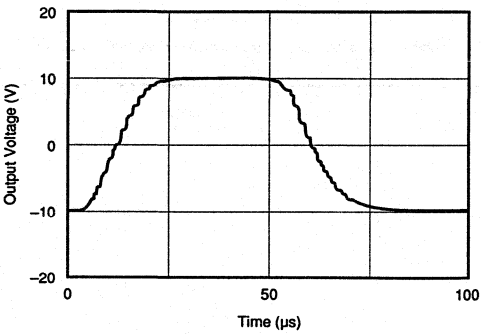
PSRR vs FREQUENCY



GAIN/PHASE vs FREQUENCY



LARGE SIGNAL TRANSIENT RESPONSE



ISOLATED POWER SUPPLY
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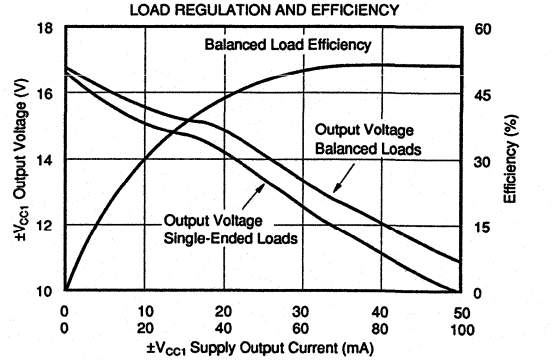

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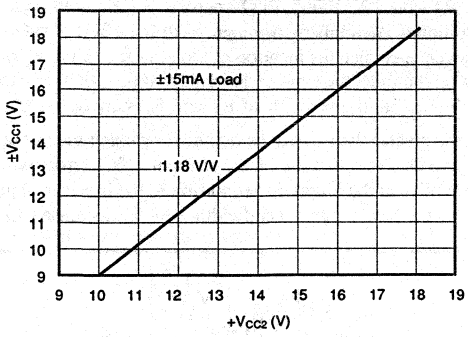
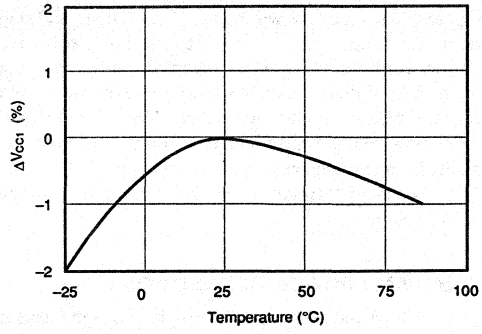


ISOLATED POWER SUPPLY VOLTAGE vs TEMPERATURE



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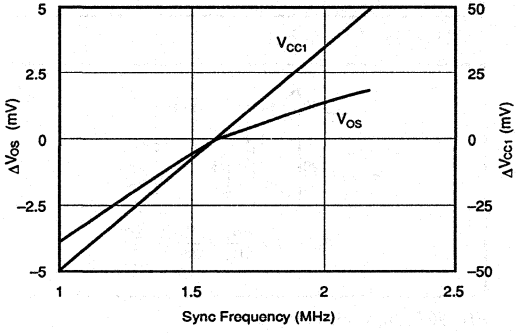
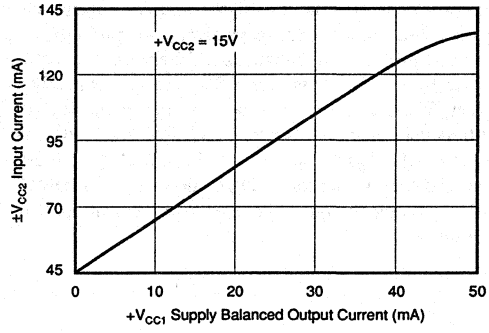


ISOLATED POWER SUPPLY INPUT CURRENT vs OUTPUT CURRENT



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OPTIONAL GAIN AND OFFSET ADJUSTMENTS

Rated gain accuracy and offset performance can be achieved with no external adjustments, but the circuit of Figure 2a may be used to provide a gain trim of ±0.5% for the values shown; greater range may be provided by increasing the size of R1 and R1. Every 2kΩ increase in R1 will give an additional 1% adjustment range, with R2 ≥ R1. If safety or convenience dictates location of the adjustment potentiometer on the other side of the barrier from the position shown in Figure 2a, the position of R1 and R2 may be reserved.

Gains greater than 1 may be obtained by using the circuit of Figure 2b. Note that the effect of input offset errors will be multiplied at the output in proportion to the increase in gain. Also, the small-signal bandwidth will be decreased in in-

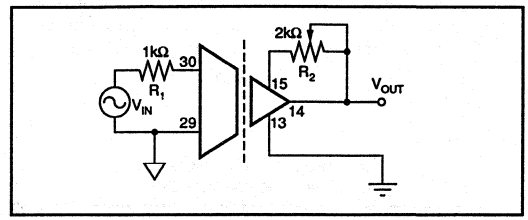

FIGURE 2a. Gain Adjust.

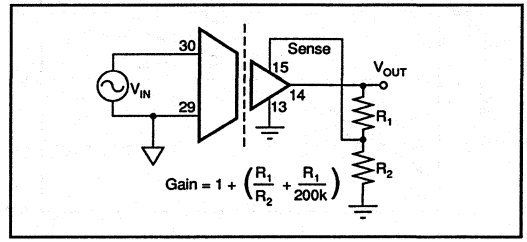

FIGURE 2b. Gain Setting.

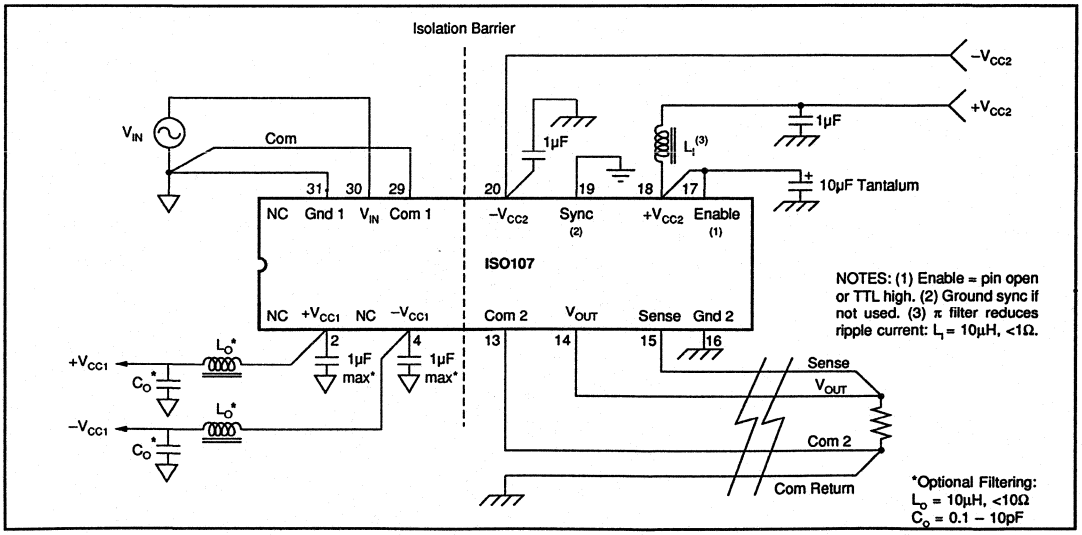

FIGURE 1. Signal and Power Connections.

verse proportion to the increase in gain. In most instances, a precision gain block at the input of the isolation amplifier will provide better overall performance.

Figure 3 shows a method for trimming V_{OS} of the ISO107. This circuit may be applied to either Signal Com (input or output) as desired for safety or convenience. With the values shown, ±15V supplies and unity gain, the circuit will provide ±150mV adjustment range and 0.25mV resolution with a typical trim potentiometer. The output will have some sensitivity to power supply variations. For a ±100mV trim, power supply sensitivity is 8mV/V at the output.

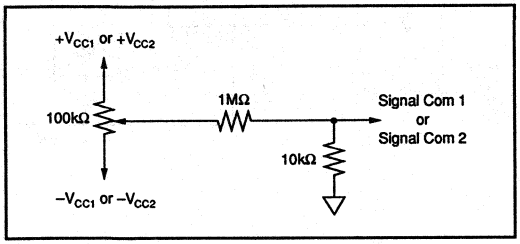

FIGURE 3. V_{OS} Adjust.

OPTIONAL OUTPUT FILTER

Figure 4 shows an optional output ripple filter that reduces the 800kHz ripple voltage to <3mVp-p without compromising DC performance. The small signal bandwidth is extended above 30kHz as a result of this compensation.

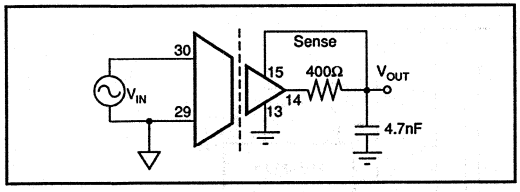

FIGURE 4. Ripple Reduction.

MULTICHANNEL SYNCHRONIZATION

Synchronization of multiple ISO107s can be accomplished by connecting pin 19 of each device to an external TTL level oscillator, as shown in Figure 6. The PWS750-1 oscillator is convenient because its nominal synchronizing output frequency is 1.6MHz, resulting in a 800kHz carrier in the ISO107 (its nominal unsynchronized value). The open collector output typically switches 7.5mA to a 0.2V low level so that the external pull-up resistor can be chosen for different pull-up voltages as shown in Figure 6. The number of channels synchronized by one PWS750-1 is determined by the total capacitance of the sync voltage conductors. They must be less than 1000pF to ensure TTL level switching at 800kHz. At higher frequencies the capacitance must be proportionally lower.

Customers can supply their own TTL level synchronization logic, provided the frequency is between 1.25MHz and 2MHz, and the duty cycle is greater than 25%.

ISOLATION BARRIER VOLTAGE

The typical performance of the ISO107 under conditions of barrier voltage stress is indicated in the first two performance curves—Recommended Range of Isolation Voltage and IMR/Leakage vs Frequency. At low barrier modulation levels, errors can be determined by the IMRR characteristic. At higher barrier voltages, typical performance is obtained as long as the dv/dt across the barrier is below the shaded area in the first curve. Otherwise, the signal channel will be interrupted, causing the output to distort, and/or shift DC level. This condition is temporary, with normal operation resuming as soon as the transient subsides. Permanent damage to the integrated circuits occurs only if transients exceed 20kV/µs. Even in this extreme case, the barrier integrity is assured.

HIGH VOLTAGE TESTING

The ISO107 was designed to reliably operate with 2500Vrms continuous isolation barrier voltage. To confirm barrier integrity, a two-step breakdown test is performed on 100% of the units. First, an 8000V peak, 60Hz barrier potential is applied for 10s to verify that the dielectric strength of the insulation is above this level. Following this exposure, a 2500Vrms, 60Hz potential is applied for one minute to conform to UL544. Life-test results show reliable operation under continuous rated voltage and maximum operating temperature conditions.

APPLICATIONS

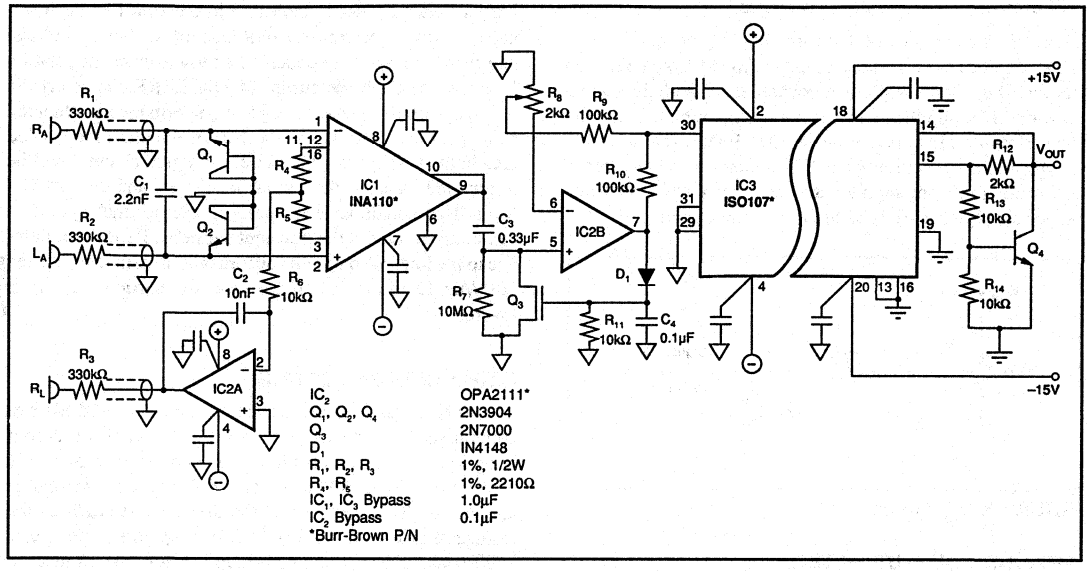

FIGURE 5. ECG Amplifier with Right Leg Drive, Defibrillator Protection, and E.S.U. Blanking.

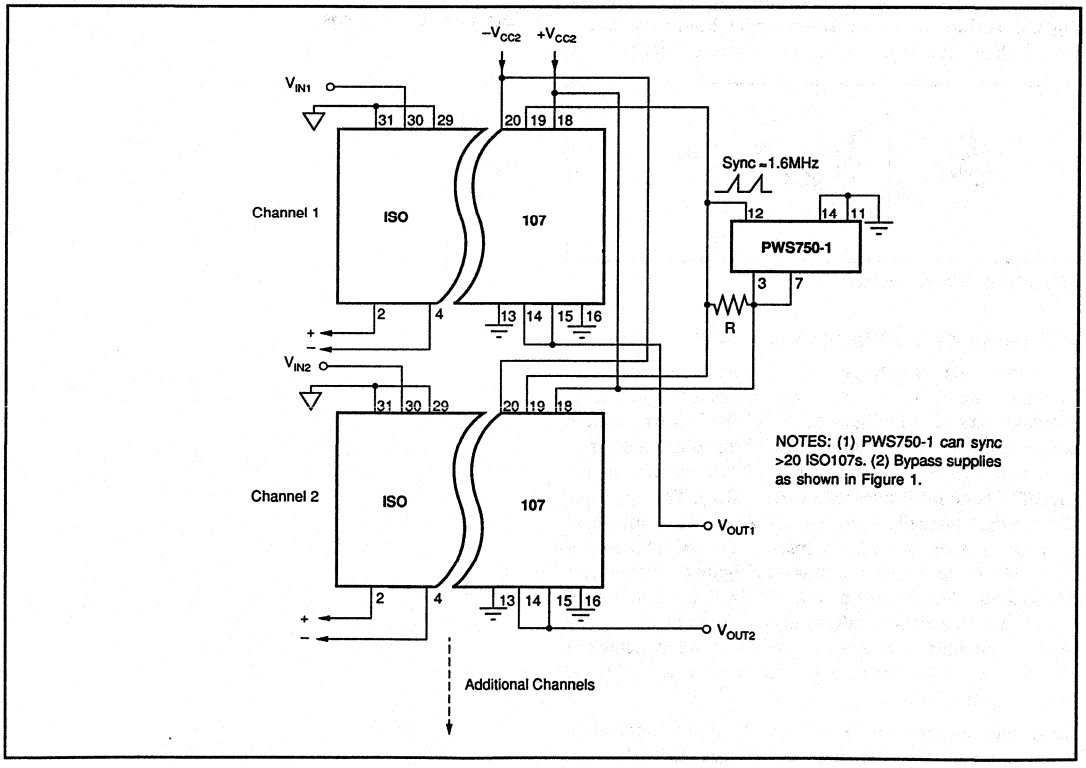

FIGURE 6. Synchronized-Multichannel Isolation.

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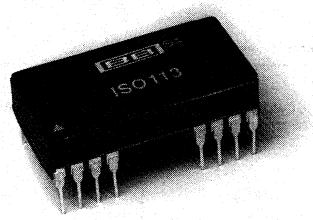


ISO113

Low-Cost, High-Voltage, Internally Powered OUTPUT ISOLATION AMPLIFIER

FEATURES

- SELF-CONTAINED ISOLATED SIGNAL AND OUTPUT POWER
- SMALL PACKAGE SIZE: Double-Wide (0.6") Sidebraze DIP
- CONTINUOUS AC BARRIER RATING: 1500Vrms
- WIDE BANDWIDTH: 20kHz Small Signal, 20kHz Full Power
- BUILT-IN ISOLATED OUTPUT POWER: ±10V to ±18V Input, ±50mA Output
- MULTICHANNEL SYNCHRONIZATION CAPABILITY
- BOARD AREA ONLY 0.72in.^{2} (4.6cm^2)

APPLICATIONS

- 4mA TO 20mA V/I CONVERTERS
- MOTOR AND VALVE CONTROLLERS
- ISOLATED RECORDER OUTPUTS
- MEDICAL INSTRUMENTATION OUTPUTS
- GAS ANALYZERS

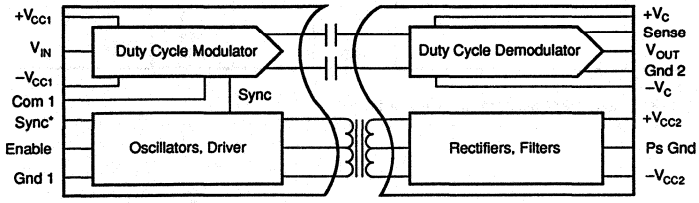
DESCRIPTION

The ISO113 output isolation amplifier provides both signal and output power across an isolation barrier in a small double-wide DIP package. The ceramic non-hermetic hybrid package with side-brazed pins contains a transformer-coupled DC/DC converter and a capacitor-coupled signal channel.

Extra power is available on the isolated output side for driving external loads. The converter is protected from shorts to ground with an internal current limit, and the soft-start feature limits the initial currents from the power source. Multiple-channel synchronization can be accomplished by applying a TTL clock signal to paralleled Sync pins. The Enable control is used to turn off transformer drive while keeping the signal channel modulator active. This feature provides a convenient way to reduce quiescent current for low power applications.

The wide barrier pin spacing and internal insulation allow for the generous 1500Vrms continuous rating. Reliability is assured by 100% barrier breakdown testing that conforms to UL1244 test methods. Low barrier capacitance minimizes AC leakage currents.

These specifications and built-in features make the ISO113 easy to use, and provides for compact PC board layout.



*Ground if not used

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Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL

At T_A = +25°C and V_{CC1} = ±15V, ±15mA output current unless otherwise noted.

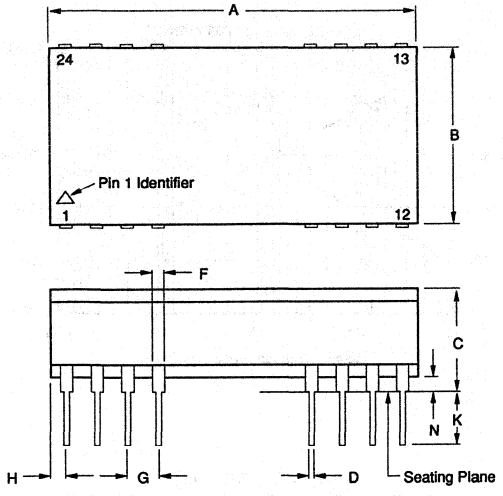
PARAMETER	CONDITIONS	ISO113 MIN	ISO113 TYP	ISO113 MAX	ISO113B MIN	ISO113B TYP	ISO113B MAX	UNITS
ISOLATION								
Rated Continuous Voltage								
AC, 60Hz	T_{MIN} to T_{MAX}	1500			*			Vrms
DC	T_{MIN} to T_{MAX}	2121			*			VDC
Test Breakdown, 100% AC, 60Hz	10s	5657			*			Vpk
Isolation-Mode Rejection	1500Vrms, 60Hz		130			*		dB
	2121VDC		160			*		dB
Barrier Impedance			10^{12} || 9			*		Ω || pF
Leakage Current	240Vrms, 60Hz		1	2		*	*	µA
GAIN								
Nominal			1			*		V/V
Initial Error			±0.3	±0.5		*	*	%FSR
Gain vs Temperature			±60	±100		±20	±50	ppm/°C
Nonlinearity	V_O = –10V to 10V		±0.05	±0.1		±0.03	±0.05	%FSR
	V_O = –5V to 5V		±0.02	±0.04		±0.012	±0.02	%FSR
INPUT OFFSET VOLTAGE								
Initial Offset			±20	±60		*	*	mV
vs Temperature			±300	±500		±100	±250	µV/°C
vs Power Supplies	V_{CC2} = ±10 to ±18V		0.9			*		mV/V
vs Output Supply Load	I_O = 0 to ±50mA		±0.3			*		mV/mA
SIGNAL INPUT								
Voltage Range	Output Voltage in Range	±10	±15		*	*		V
Resistance			200			*		kΩ
SIGNAL OUTPUT								
Voltage Range		±10	±12.5		*	*		V
Current Drive		±5	±20		*	*		mA
Ripple Voltage, 800kHz Carrier			25			*		mVp-p
	400Ω/4.7nF (See Figure 4)		5			*		mVp-p
Capacitive Load Drive			1000			*		pF
Voltage Noise			4			*		µV/√Hz
FREQUENCY RESPONSE								
Small Signal Bandwidth			20			*		kHz
Slew Rate			1.5			*		V/µs
Settling Time	0.1%, –10/10V		75			*		µs
POWER SUPPLIES								
Rated Voltage, V_{CC1}			±15			*		V
Voltage Range		±10		±18	*		*	V
Input Current	I_O = ±15mA		+90/–4.5			*		mA
Ripple Current	No Filter		60			*		mAp-p
	C_{IN} = 1µF		3			*		mAp-p
Rated Output Voltage		±14.25	±15	±15.75	*	*	*	V
Output Current	Balanced Load		±15	±50		*		mA
	Single		30	100		*		mA
Load Regulation	Balanced Load		0.3			*		%/mA
Line Regulation			1.12			*		V/V
Output Voltage vs Temperature			2.5			*		mV/°C
Voltage Balance, ±V_{CC2}			0.05			*		%
Voltage Ripple (800kHz)	No External Capacitors		50			*		mVp-p
	C_{EXT} = 1µF		5			*		mVp-p
Output Capacitive Load				1			*	µF
Sync Frequency	TTL, 50% Duty Cycle	1.25	1.6	2	*	*	*	MHz
TEMPERATURE RANGE								
Specification		–25		+85	*		*	°C
Operating		–25		+85	*		*	°C
Storage		–25		+125	*		*	°C

*Specifications same as ISO113.

NOTE: (1) Conforms to UL1244 test methods. 100% tested at 1500Vrms for 1 minute.

MECHANICAL

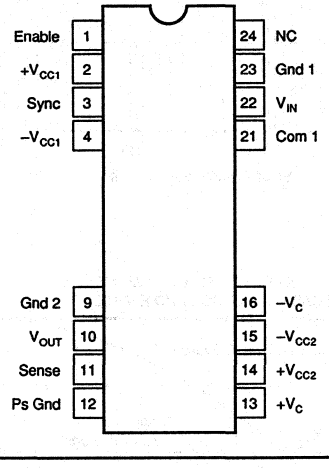
24-Pin Double-Wide DIP



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.180	1.220	29.97	30.99
B	.580	.600	14.73	15.24
C	.310	.370	7.87	9.40
D	.016	.020	0.41	0.51
F	.040 TYP		1.02 TYP	
G	.100 BASIC		2.54 BASIC	
H	.044	.056	1.12	1.42
J	.009	.012	0.23	0.30
K	.165	.185	4.19	4.70
L	.600	.620	15.24	15.75
N	.040	.060	1.02	1.52

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Supply Without Damage	±18V
V_{IN}, Sense Voltage	±50V
Com to Gnd (either input or output)	±200mV
Enable, Sync	Gnd to $+V_{CC1}$
Continuous Isolation Voltage	1500Vrms
V_{ISO}, dv/dt	20kV/µs
Junction Temperature	+150°C
Storage Temperature	–25°C to +125°C
Lead Temperature,10s	+300°C
Output Short to Gnd Duration	Continuous
$\pm V_{CC2}$ to Gnd 2 Duration	Continuous

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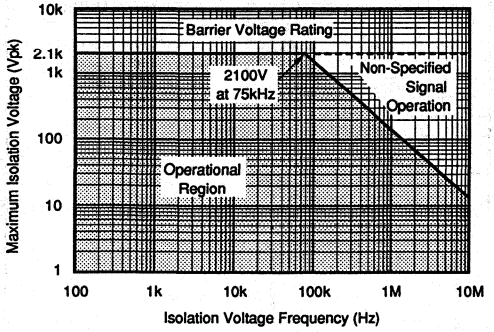
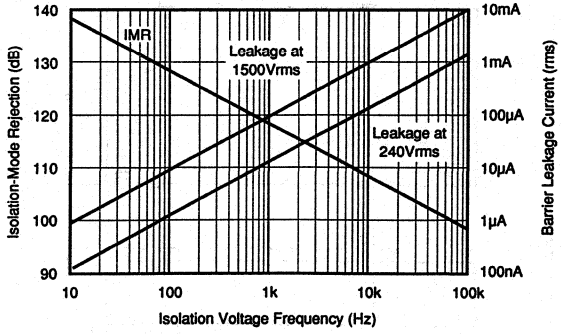
TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_{CC1} = ±15VDC, ±15mA output current unless otherwise noted.

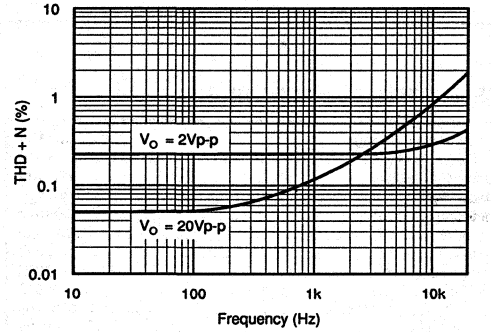
RECOMMENDED RANGE OF ISOLATION VOLTAGE



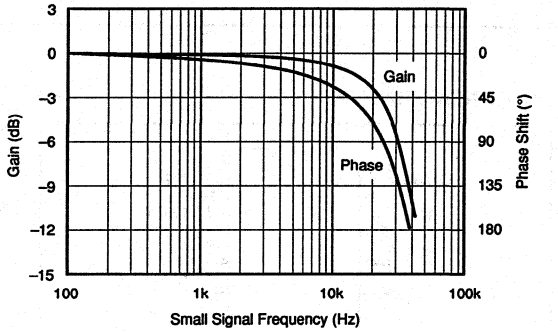
IMR/LEAKAGE vs FREQUENCY



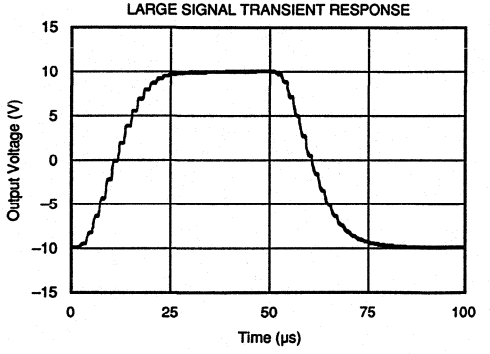
DISTORTION vs FREQUENCY



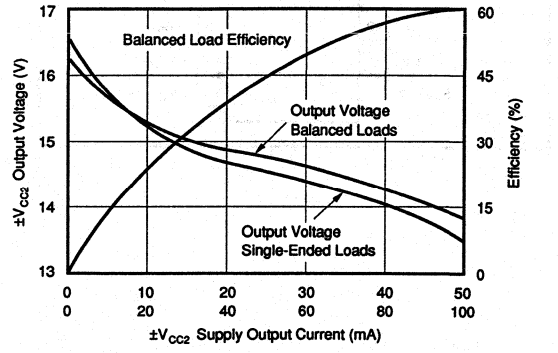
GAIN/PHASE vs FREQUENCY



LARGE SIGNAL TRANSIENT RESPONSE



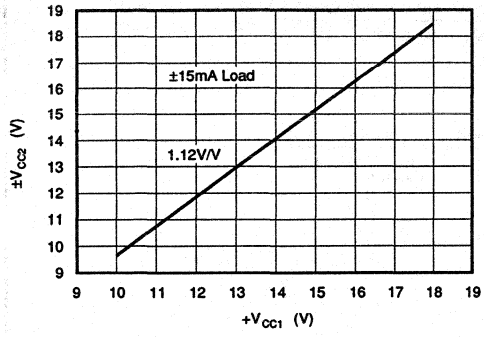
ISOLATED POWER SUPPLY
LOAD REGULATION AND EFFICIENCY



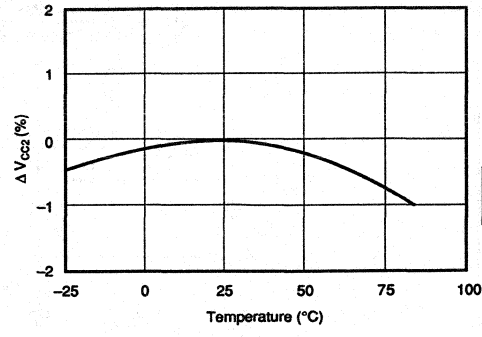
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_{CC1} = ±15VDC, ±15mA output current unless otherwise noted.

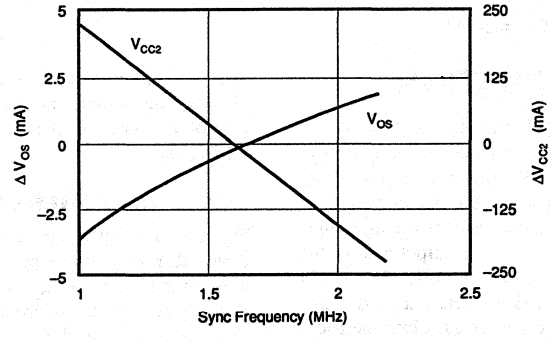
ISOLATED POWER SUPPLY LINE REGULATION

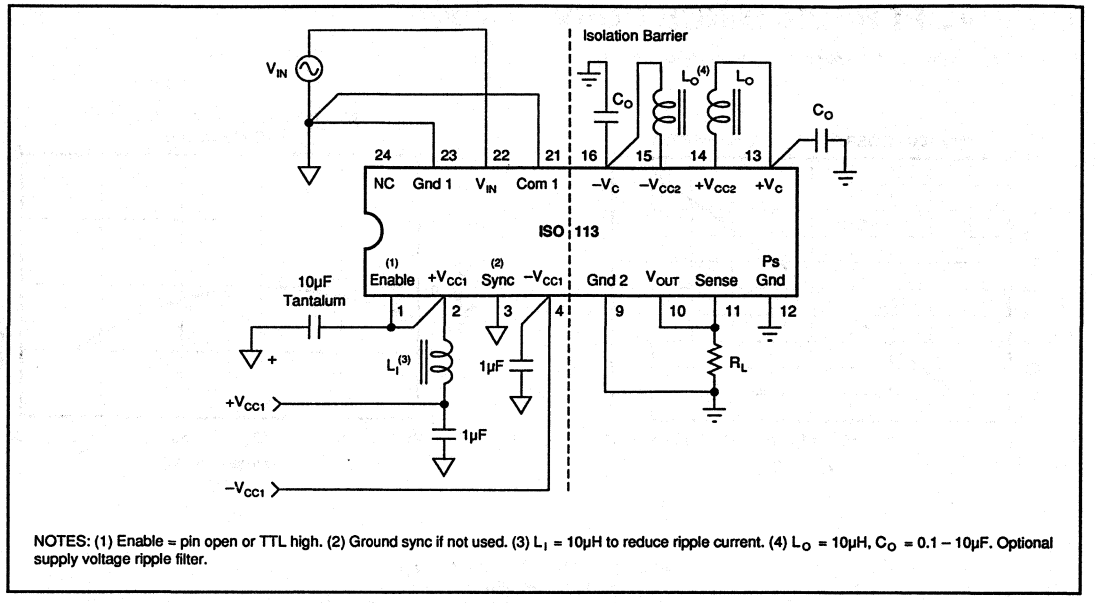


ISOLATION POWER SUPPLY VOLTAGE vs TEMPERATURE



ISOLATED SUPPLY VOLTAGE AND V_{OS} vs SYNC FREQUENCY





NOTES: (1) Enable = pin open or TTL high. (2) Ground sync if not used. (3) L_1 = 10µH to reduce ripple current. (4) L_O = 10µH, C_O = 0.1 – 10µF. Optional supply voltage ripple filter.

FIGURE 1. Signal and Power Connections.

THEORY OF OPERATION

The block diagram on the front page shows the isolation amplifier's synchronized signal and power configuration, which eliminate beat frequency interference. A proprietary 800kHz oscillator chip, power MOSFET transformer drivers, patented square core wirebonded transformer, and single chip diode bridge provide power to the output side of the isolation amplifier as well as external loads. The signal channel capacitively couples a duty-cycle encoded signal across the ceramic high-voltage barrier built into the package. A proprietary transmitter-receiver pair of integrated circuits, laser trimmed at wafer level, and coupled through a pair of matched "fringe" capacitors, results in a simple, reliable design.

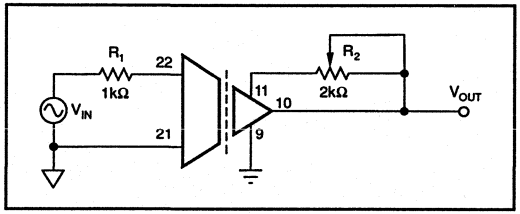


FIGURE 2a. Gain Adjust.

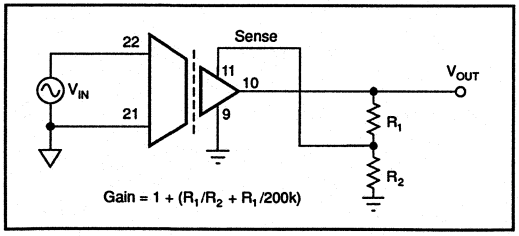


FIGURE 2b. Gain Setting.

SIGNAL AND POWER CONNECTIONS

Figure 1 shows the proper power supply and signal connections. All power supply pins should be bypassed as shown with the π filter for $+V_{CC1}$, an option recommended if more than ±15mA are drawn from the isolated supply. Separate rectifier output pins ($\pm V_{CC2}$) and amplifier supply input pins ($\pm V_C$) allow additional ripple filtering and/or regulation. The separate input common pin and output sense are low current inputs tied to the signal source ground, and output load, respectively, to minimize errors due to IR drop in long conductors. Otherwise, connect Com 1 to Gnd 1, and Sense to V_{OUT} at the ISO113 socket. The enable pin may be left open if the ISO113 is continuously operated. If not, a TTL low level will disable the internal DC/DC converter. The Sync input must be grounded for unsynchronized operation while a 1.25MHz to 2MHz TTL clock signal provides synchronization of multiple units.

OPTIONAL GAIN AND OFFSET ADJUSTMENTS

Rated gain accuracy and offset performance can be achieved with no external adjustments, but the circuit of Figure 2a may be used to provide a gain trim of ±0.5% for the values shown. Greater range may be provided by increasing the size of R_1 and R_2. Every 2kΩ increase in R_1 will give an additional 1% adjustment range, with $R_2 \geq 2R_1$. If safety or convenience dictate location of the adjustment potentiometer on the other side of the barrier from the position shown in Figure 2a, the position of R_1 and R_2 may be reversed.

Gains greater than 1 may be obtained by using the circuit of Figure 2b. Note that the effect of input referred errors will be multiplied at the output in proportion to the increase in gain. Also, the small-signal bandwidth will be decreased in inverse proportion to the increase in gain. In most instances, a precision gain block at the input of the isolation amplifier will provide better overall performance.

Figure 3 shows a method for trimming V_{OS} of the ISO113. This circuit may be applied to either Signal Com1 or Gnd2 as desired for safety or convenience. With the values shown, ±15V supplies and unity gain, the circuit will provide ±150mV adjustment range and 0.25mV resolution with a typical trim potentiometer. The output will have some sensitivity to power supply variations. For a ±100mV trim, power supply sensitivity is 8mV/V at the output.

OPTIONAL OUTPUT FILTER

Figure 4 shows an optional output ripple filter that reduces the 800kHz ripple voltage to <5mVp-p without compromising DC performance. The small signal bandwidth is extended above 30kHz as a result of this compensation.

MULTICHANNEL SYNCHRONIZATION

Synchronization of multiple ISO113s can be accomplished by connecting pin 3 of each device to an external TTL level oscillator, as shown in Figure 7. The PWS750-1 oscillator is convenient because its nominal synchronizing output frequency is 1.6MHz, resulting in a 800kHz carrier in the ISO113 (its nominal unsynchronized value). The open collector output typically switches 7.5mA to a 0.2V low level so that the external pull up resistor can be chosen for different pull-up voltages as shown in Figure 7. The number of channels synchronized by one PWS750-1 is determined by the total capacitance of the sync voltage conductors. They must be less than 1000pF to ensure TTL level switching at 800kHz. At higher frequencies the capacitance must be proportionally lower.

Customers can supply their own TTL level synchronization logic, provided the frequency is between 1.25MHz and 2MHz, and the duty cycle is greater than 25%.

Single or multichannel synchronization with reduced power dissipation for applications requiring less than ±15mA from V_{CC1} is accomplished by driving both the Sync input pin (3) and Enable pin (1) with the TTL oscillator as shown in Figure 5.

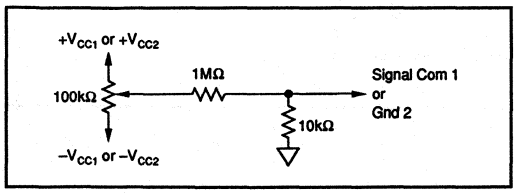


FIGURE 3. V_{OS} Adjust.

ISOLATION BARRIER VOLTAGE

The typical performance of the ISO113 under conditions of barrier voltage stress is indicated in the first two performance curves—Recommended Range of Isolation Voltage and IMR/ Leakage vs Frequency. At low barrier modulation levels, errors can be determined by the IMRR characteristic. At higher barrier voltages, typical performance is obtained as long as the dv/dt across the barrier is below the shaded area in the first curve. Otherwise, the signal channel will be interrupted, causing the output to distort, and/or shift DC level. This condition is temporary, with normal operation resuming as soon as the transient subsides. Permanent damage to the integrated circuits occurs only if transients exceed 20kV/µs. Even in this extreme case, the barrier integrity is assured.

HIGH VOLTAGE TESTING

The ISO113 was designed to reliably operate with 1500Vrms continuous isolation barrier voltage. To confirm barrier integrity, a two-step breakdown test is performed on 100% of the units. First, an 5657V peak, 60Hz barrier potential is applied for 10s to verify that the dielectric strength of the insulation is above this level. Following this exposure, a 1500Vrms, 60Hz potential is applied for one minute to conform to UL1244. Life-test results show reliable operation under continuous rated voltage and maximum operating temperature conditions.

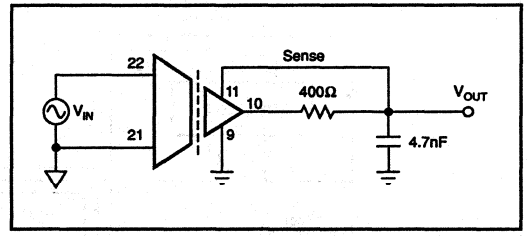


FIGURE 4. Ripple Reduction.

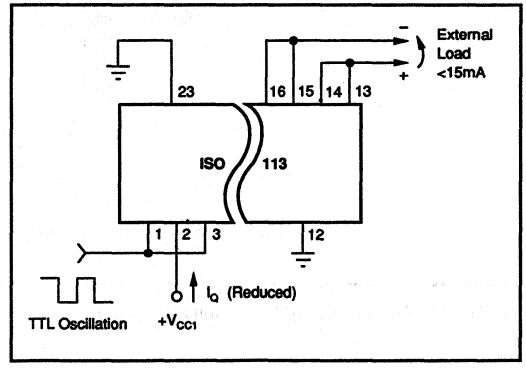


FIGURE 5. Reduced Power Dissipation.

APPLICATIONS

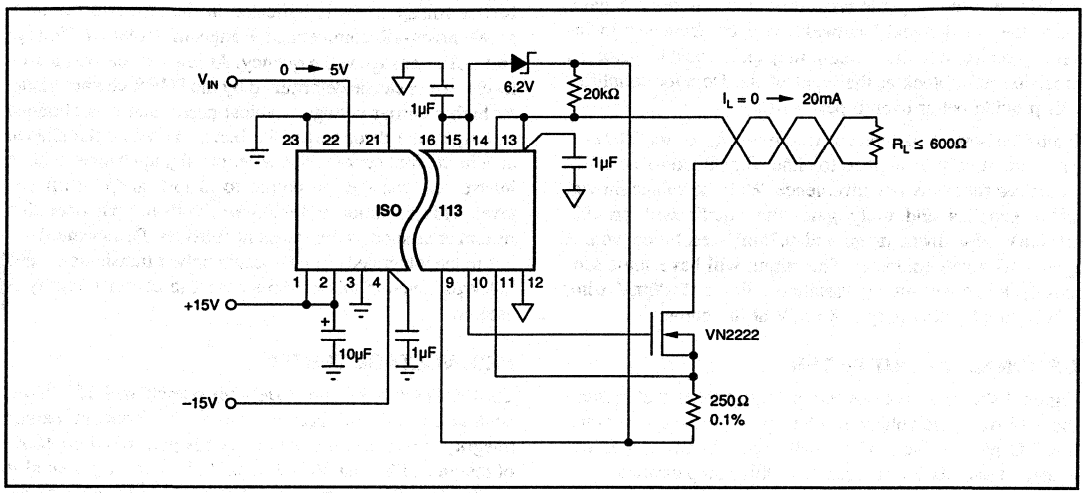


FIGURE 6. Isolated Current Loop Driver.

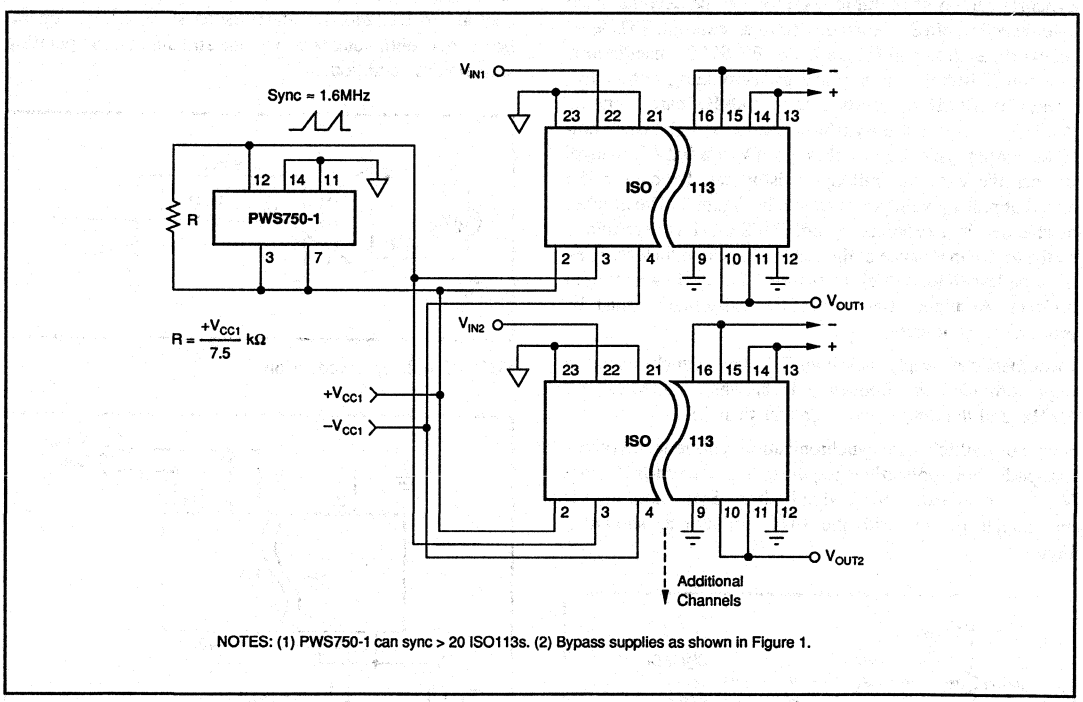


FIGURE 7. Synchronized-Multichannel Isolation.

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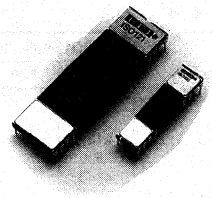


ISO120
ISO121

Precision Low Cost ISOLATION AMPLIFIER

FEATURES

- 100% TESTED FOR PARTIAL DISCHARGE
- ISO120: Rated 1500Vrms
- ISO121: Rated 3500Vrms
- HIGH IMR: 115dB at 60Hz
- USER CONTROL OF CARRIER FREQUENCY
- LOW NONLINEARITY: ±0.01% max
- BIPOLAR OPERATION: V_O = ±10V
- 0.3"-WIDE 24-PIN HERMETIC DIP, ISO120
- SYNCHRONIZATION CAPABILITY
- WIDE TEMP RANGE: –55°C to +125°C (ISO120)

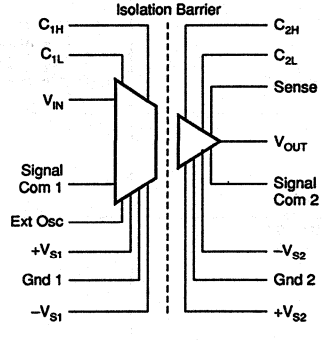
APPLICATIONS

- INDUSTRIAL PROCESS CONTROL: Transducer Isolator for Thermocouples, RTDs, Pressure Bridges, and Flow Meters, 4mA to 20mA Loop Isolation
- GROUND LOOP ELIMINATION
- MOTOR AND SCR CONTROL
- POWER MONITORING
- ANALYTICAL MEASUREMENTS
- BIOMEDICAL MEASUREMENTS
- DATA ACQUISTION
- TEST EQUIPMENT

DESCRIPTION

The ISO120 and ISO121 are precision isolation amplifies incorporating a novel duty cycle modulation-demodulation technique. The signal is transmitted digitally across a 2pF differential capacitive barrier. With digital modulation the barrier characteristics do not affect signal integrity, which results in excellent reliability and good high frequency transient immunity across the barrier. Both the amplifier and barrier capacitors are housed in a hermetic DIP. The ISO120 and ISO121 differ only in package size and isolation voltage rating.

These amplifiers are easy to use. No external components are required for 60kHz bandwidth. With the addition of two external capacitors, precision specifications of 0.01% max nonlinearity and 150µV/°C max V_{OS} drift are guaranteed with 6kHz bandwidth. A power supply range of ±4.5V to ±18V and low quiescent current make these amplifiers ideal for a wide range of applications.



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Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL

At T_A = +25°C: V_{S1} = V_{S2} = ±15V: and R_L = 2kΩ, unless otherwise noted.

PARAMETER	CONDITIONS	ISO120BG, ISO121BG			ISO120G, ISO120SG[4], ISO121G			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
ISOLATION								
Voltage Rated Continuous ISO120: AC 60Hz	T_{MIN} to T_{MAX}	1500			*			Vrms
DC	T_{MIN} to T_{MAX}	2121			*			VDC
ISO121: AC 60Hz	T_{MIN} to T_{MAX}	3500			*			Vrms
DC	T_{MIN} to T_{MAX}	4950			*			VDC
100% Test (AC 60Hz): ISO120	1s; Partial Discharge ≤ 5pC	2500			*			Vrms
ISO121	1s; Partial Discharge ≤ 5pC	5600			*			Vrms
Isolation Mode Rejection ISO 120: AC 60Hz	1500Vrms		115			*		dB
DC			160			*		dB
ISO121: AC60Hz	3500Vrms		115			*		dB
DC			160			*		dB
Barrier Impedance			10^{14} ‖ 2			*		Ω ‖ pF
Leakage Current	V_{ISO} = 240Vrms, 60Hz		0.18	0.5		*	*	µArms
GAIN[4]	V_O = ±10V							
Nominal Gain	C_1 = C_2 = 1000pF		1			1		V/V
Gain Error			±0.04	±0.1		±0.05	±0.25	%FSR
Gain vs Temperature			±5	±20		±10	±40	ppm/°C
Nonlinearity			±0.005	±0.01		±0.01	±0.05	%FSR
Nominal Gain	C_1 = C_2 = 0		1			1		V/V
Gain Error			±0.04	±0.25		±0.05	±0.25	%FSR
Gain vs Temperature			±40			±40		ppm/°C
Nonlinearity			±0.02	±0.1		±0.04	±0.1	%FSR
INPUT OFFSET VOLTAGE[4]								
Initial Offset	C_1 = C_2 = 1000pF		±5	±25		±10	±50	mV
vs Temperature			±100	±150		±150	±400	µV/°C
Initial Offset	C_1 = C_2 = 0		±25	±100		±40	±100	mV
vs Temperature			±250			±500		µV/°C
Initial Offset								
vs Supply	±V_{S1} or ±V_{S2} = ±4.5V to ±18V		±2			±2		mV/V
Noise			4			4		µV/√Hz
INPUT								
Voltage Range[1]		±10	±15		*	*		V
Resistance			200			*		kΩ
OUTPUT								
Voltage Range		±10	±12.5		*	*		V
Current Drive		±5	±20		*	*		mA
Capacitive Load Drive			0.1			*		µF
Ripple Voltage[2]			10			*		mVp-p
FREQUENCY RESPONSE								
Small Signal Bandwith	C_1 = C_2 = 0		60			*		kHz
	C_1 = C_2 = 1000pF		6			*		kHz
Slew Rate			2			*		V/µs
Settling Time	V_O = ±10V							
0.1%	C_2 = 100pF		50			*		µs
0.01%	C_1 = C_2 = 1000pF		350			*		µs
Overload Recovery Time[3]	50% Output Overload, C_1 = C_2 = 0		150			*		µs
POWER SUPPLIES								
Rated Voltage			15			*		V
Voltage Range		±4.5		±18	*		*	V
Quiescent Current: V_{S1}			±4.0	±5.5		*	*	mA
V_{S2}			±5.0	±6.5		*	*	mA
TEMPERATURE RANGE								
Specification: BG and G		–25		85	–25		85	°C
SG[4]		–25		85	–55		125	°C
Operating		–55		125	–55		125	°C
Storage		–65		150	–55		150	°C
θ_{JA}: ISO120			40			40		°C/W
ISO121			25			25		°C/W

*Specifications same as ISO120BG, ISO121BG.

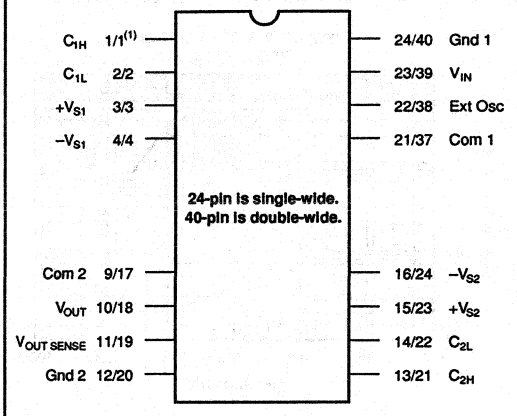
NOTE: (1) Input voltage range = ±10V for V_{S1}, V_{S2} = ±4.5VDC to ±18VDC. (2) Ripple frequency is at carrier frequency. (3) Overload recovery is approximately three times the settling time for other values of C_2. (4) The SG-grade is specified –55°C to +125°C; performance of the SG in the –25°C to +85°C temperature range is the same as the BG-grade.

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (any supply)	18V
V_{IN}, Sense Voltage	±100V
External Oscillator Input	±25V
Signal Common 1 to Ground 1	±1V
Signal Common 2 to Ground 2	±1V
Continuous Isolation Voltage: ISO120	1500Vrms
ISO121	3500Vrms
V_{ISO}, dv/dt	20kV/µs
Junction Temperature	150°C
Storage Temperature	–65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C
Output Short Duration	Continuous to Common

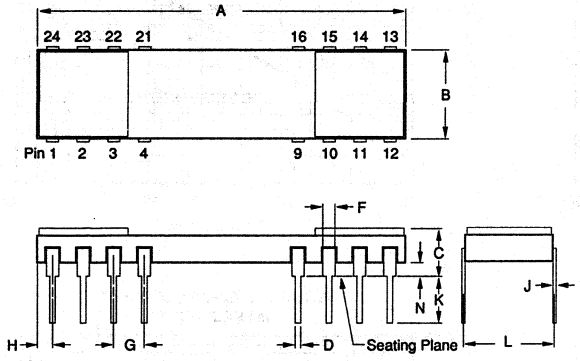
CONNECTION DIAGRAM



NOTE: (1) First pin number is for ISO120. Second pin number is for ISO121.

MECHANICAL

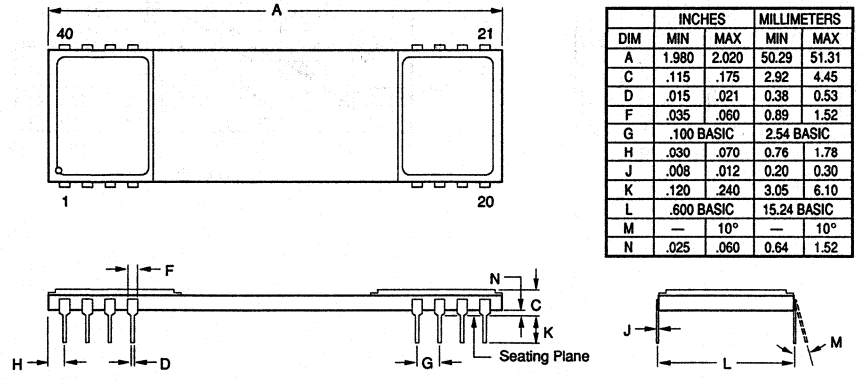
ISO120 — 24-Pin Single-Wide Hermetic Dip



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.190	1.210	30.23	30.73
B	.280	.300	7.11	7.62
C	.140	.185	3.56	4.70
D	.016	.020	0.41	0.51
F	.030	.050	0.76	1.27
G	.100 BASIC		2.54 BASIC	
H	.035	.065	0.89	1.65
J	.009	.012	0.23	0.30
K	.125	.180	3.18	4.57
L	.300 BASIC		7.62 BASIC	
N	.040	.060	1.02	1.52

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.

ISO121—40-Pin Double-Wide Hermetic DIP



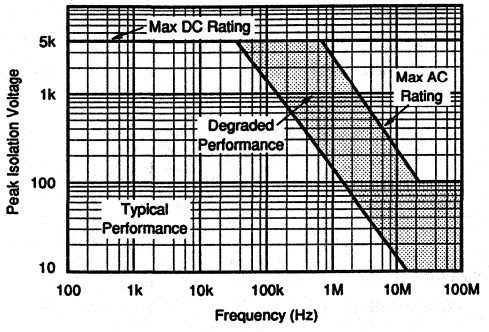
DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.980	2.020	50.29	51.31
C	.115	.175	2.92	4.45
D	.015	.021	0.38	0.53
F	.035	.060	0.89	1.52
G	.100 BASIC		2.54 BASIC	
H	.030	.070	0.76	1.78
J	.008	.012	0.20	0.30
K	.120	.240	3.05	6.10
L	.600 BASIC		15.24 BASIC	
M	—	10°	—	10°
N	.025	.060	0.64	1.52

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.

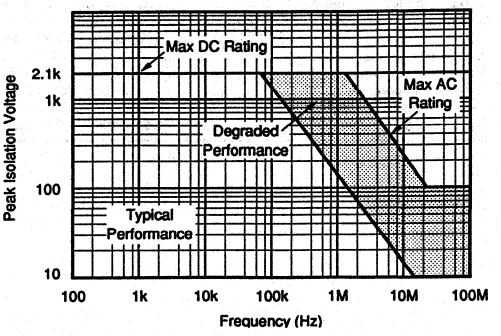
TYPICAL PERFORMANCE CURVES

T_A = +25°C; V_{S1} = V_{S2} = ±15V; and R_L = 2kΩ, unless otherwise noted.

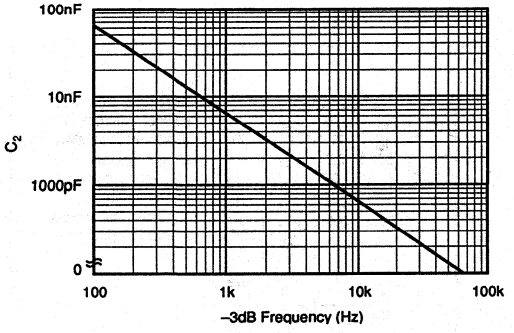
ISOLATION MODE VOLTAGE vs FREQUENCY ISO121



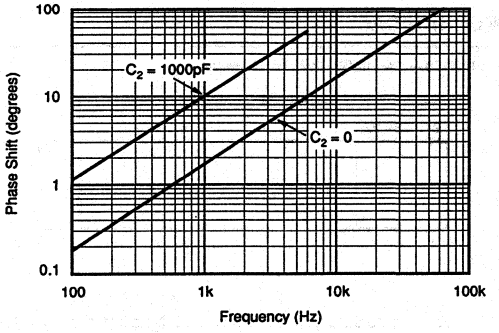
ISOLATION MODE VOLTAGE vs FREQUENCY ISO120



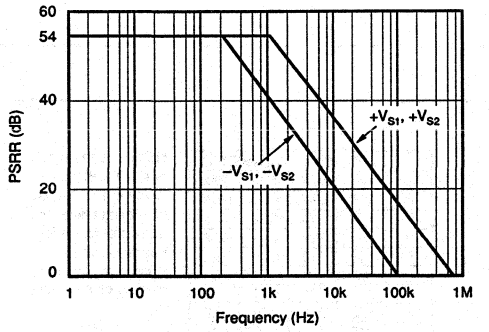
BANDWIDTH vs C_2



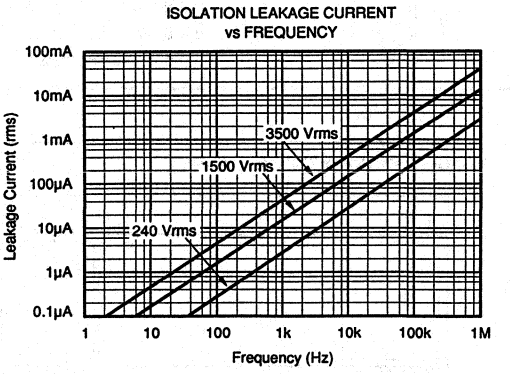
PHASE SHIFT vs C_2



PSRR vs FREQUENCY



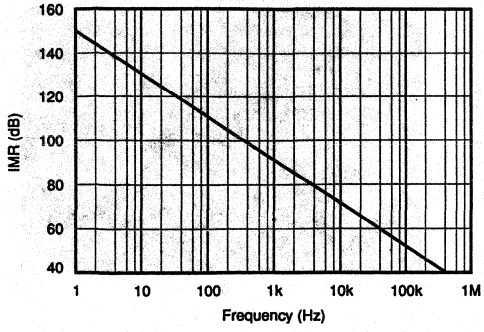
ISOLATION LEAKAGE CURRENT vs FREQUENCY



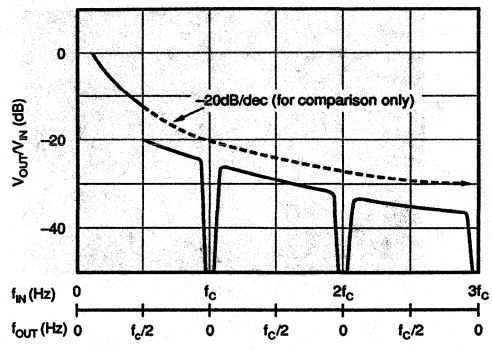
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C; V_{S1} = V_{S2} = ±15V; and R_L = 2kΩ, unless otherwise noted.

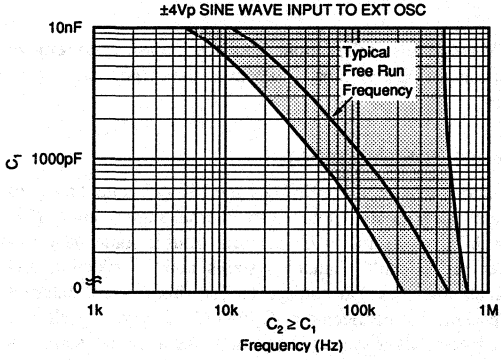
IMR vs FREQUENCY



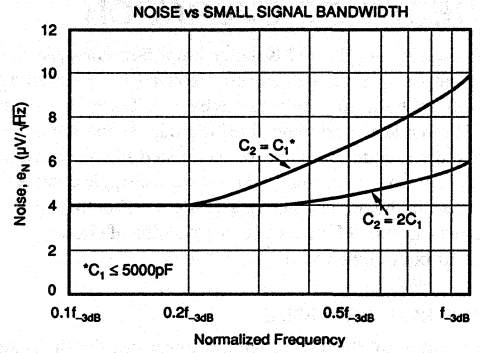
SIGNAL RESPONSE vs CARRIER FREQUENCY



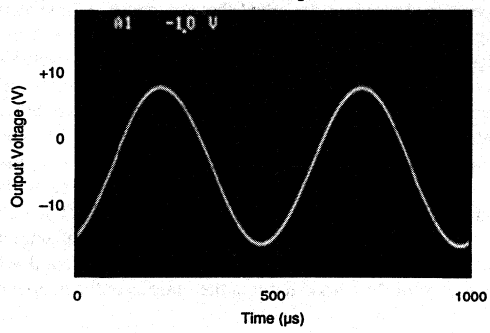
SYNCHRONIZATION RANGE at 25°C
±4Vp SINE WAVE INPUT TO EXT OSC



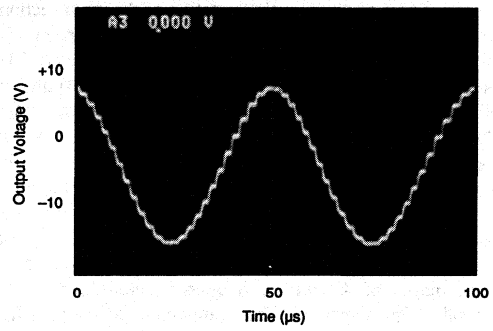
NOISE vs SMALL SIGNAL BANDWIDTH



SINE RESPONSE
(f = 2kHz, C_2 = 0)

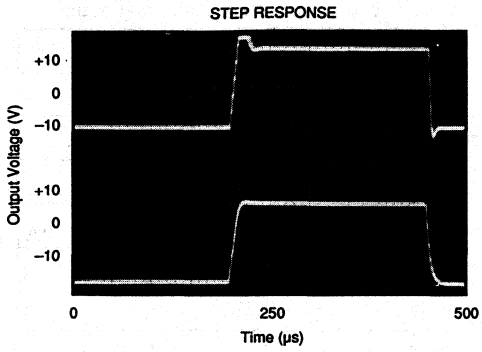


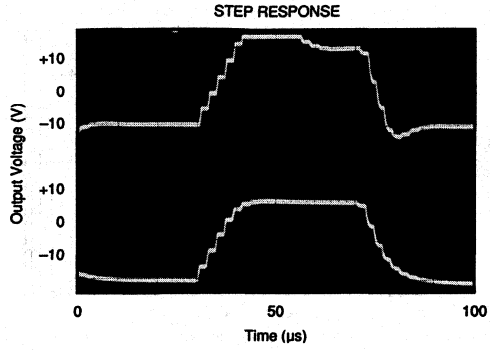
SINE RESPONSE
(f = 20kHz, C_2 = 0)



TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C; V_{S1} = V_{S2} = ±15V; and R_L = 2kΩ, unless otherwise noted.





THEORY OF OPERATION

The ISO120 and ISO121 isolation amplifiers comprise input and output sections galvanically isolated by matched 1pF capacitors built into the ceramic barrier. The input is duty-cycle modulated and transmitted digitally across the barrier. The output section receives the modulated signal, converts it back to an analog voltage and removes the ripple component inherent in the demodulation. The input and output sections are laser-trimmed for exceptional matching of circuitry common to both input and output sections.

FREE-RUNNING MODE

An input amplifier (A1, Figure1) integrates the difference between the input current (V_{IN}/200kΩ) and a switched ±100µA current source. This current source is implemented by a switchable 200µA source and a fixed 100µA current sink. To understand the basic operation of the input section, assume that V_{IN} = 0. The integrator will ramp in one direction until the comparator threshold is exceeded. The comparator and sense amp will force the current source to switch; the resultant signal is a triangular waveform with a 50% duty cycle. If V_{IN} changes, the duty cycle of the integrator will change to keep the average DC value at the output of A1 near zero volts. This action converts the input voltage to a duty-cycle modulated triangular waveform at the output of A1 near zero volts. This action converts the input voltage to a duty-cycle modulated triangular waveform at the output of A1 with a frequency determined by the internal 150pF capacitor. The comparator generates a fast rise time square wave that is simultaneously fed back to keep A1 in charge balance and also across the barrier to a differential sense amplifier with high common-mode rejection characteristics. The sense amplifier drives a switched current source surrounding A2. The output stage balances the duty-cycle modulated current against the feedback current through the 200kΩ feedback resistor, resulting in an average value at the Sense pin equal to V_{IN}. The sample and hold amplifiers in the output feedback loop serve to remove undesired ripple voltages inherent in the demodulation process.

SYNCHRONIZED MODE

A unique feature of the ISO120 and ISO121 is the ability to synchronize the modulator to an external signal source. This capability is useful in eliminating trouble-some beat frequencies in multi-channel systems and in rejecting AC signals and their harmonics. To use this feature, external capacitors are connected at C_1 and C_2 (Figure1) to change the free-running carrier frequency. An external signal is applied to the Ext Osc pin. This signal forces the current source to switch at the frequency of the external signal. If V_{IN} is zero, and the external source has a 50% duty cycle, operation proceeds as described above, except that the switching frequency is that of the external source. If the external signal has a duty cycle other than 50%, its average value is not zero. At start-up, the current source does not switch until the integrator establishes an output equal to the average DC value of the external signal. At this point, the external signal is able to trigger the current source, producing a triangular waveform, symmetrical about the new DC value, at the output of A1. For V_{IN} = 0, this waveform has a 50% duty cycle. As V_{IN} varies, the waveform retains its DC offset, but varies in duty cycle to maintain charge balance around A1. Operation of the demodulator is the same as outlined above.

BASIC OPERATION

Signal and Power Connections

Figure 2 shows proper power and signal connections. Each power supply pin should be bypassed with 1µF tantalum capacitor located as close to the amplifier as possible. All ground connections should be run independently to a common point if possible. Signal Common on both input and

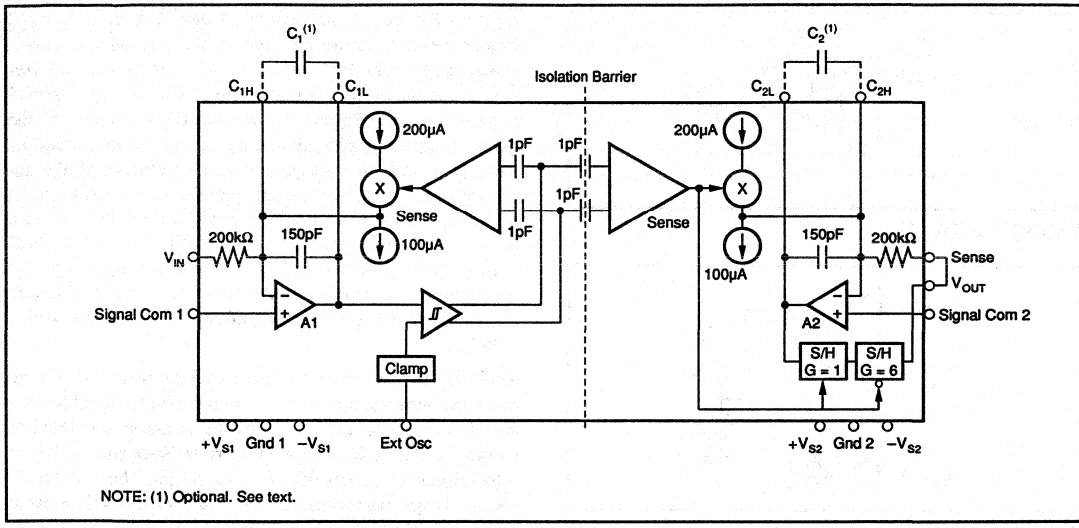


FIGURE 1. Block Diagram.

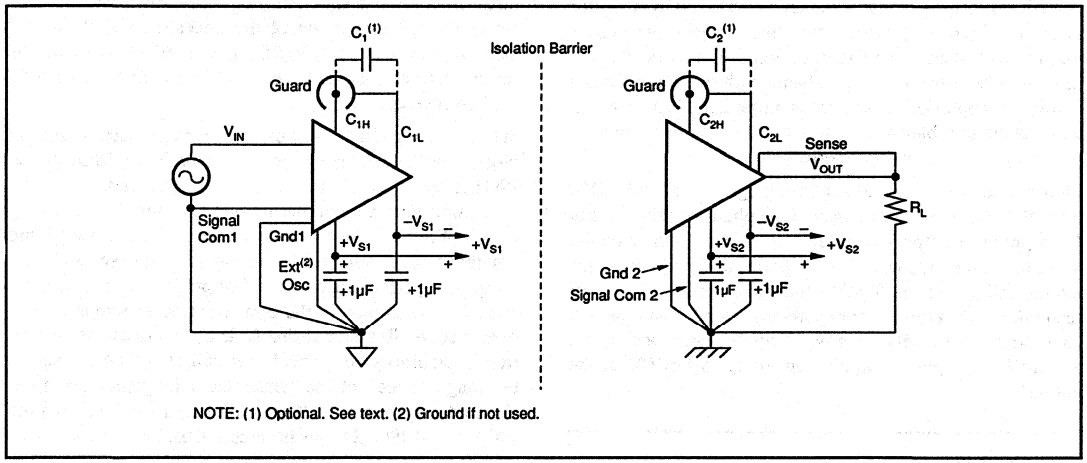


FIGURE 2. Power and Signal Connections.

output sections provide a high-impedance point for sensing signal ground in noisy applications. Signal Common must have a path to ground for bias current return and should be maintained within ±1V of Gnd. The output sense pin may be connected directly to V_{OUT} or may be connected to a remote load to eliminate errors due to IR drops. Pins are provided for use of external integrator capacitors. The C_{1H} and C_{2H} pins are connected to the integrator summing junctions and are therefore particularly sensitive to external pickup. This sensitivity will most often appear as degraded IMR or PSR performance. AC or DC currents coupled into these pins results in $V_{ERROR} = I_{ERROR} \times 200k\Omega$ at the output. Guarding of these pins to their respective Signal Common, or C_{1L} and C_{2L} is strongly recommended. For similar reasons, long traces or physically large capacitors are not desirable. If wound-foil capacitors are used, the outside foil should be connected to C_{1L} and C_{2L}, respectively.

Optional Gain and Offset Adjustments

Rated gain accuracy and offset performance can be achieved with no external adjustments, but the circuit of Figure 3a may be used to provide a gain trim of ±0.5% for values shown; greater range may be provided by increasing the size of R_1 and R_2. Every 2kΩ increase in R_1 will give an additional 1% adjustment range, with $R_2 \geq 2R_1$. If safety or convenience dictates location of the adjustment potentiometer on the other side of the barrier from the position shown in Figure 3a, the positions of R_1 and R_2 may be re-

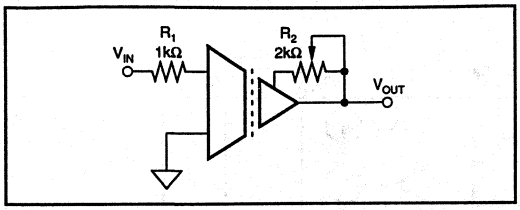


FIGURE 3a. Gain Adjust.

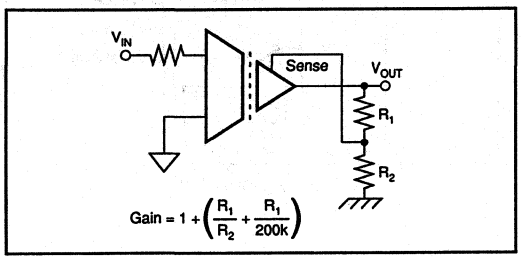


FIGURE 3b. Gain Setting.

versed. Gains greater than one may be obtained by using the circuit of Figure 3b. Note that the effect of input offset errors will be multiplied at the output in proportion to the increase in gain. Also, the small-signal bandwidth will be decreased in inverse proportion to the increase in gain. In most instances, a precision gain block at the input of the isolation amplifier will provide better overall performance.

Figure 4 shows a method for trimming V_{OS} of the ISO120 and ISO121. This circuit may be applied to either Signal Com (input or output) as desired for safety or convenience. With the values shown, ±15V supplies and unity gain, the circuit will provide ±150mV adjustment range and 0.25mV resolution with a typical trim potentiometer. The output will have some sensitivity to power supply variations. For a ±100mV trim, power supply sensitivity is 8mV/V at the output.

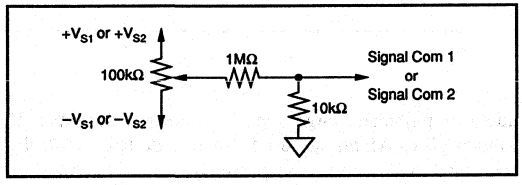


FIGURE 4. V_{OS} Adjust.

CARRIER FREQUENCY CONSIDERATIONS

As previously discussed, the ISO120 and ISO121 amplifiers transmit the signal across the iso-barrier by a duty-cycle modulation technique. This system works like any linear amplifier for input signals having frequencies below one half the carrier frequency, f_C. For signal frequencies above $f_C/2$, the behavior becomes more complex. The Signal Response vs Carrier Frequency performance curve describes this behavior graphically. The upper curve illustrates the response for input signals varying from DC to $f_C/2$. At input frequencies at or above $f_C/2$, the device generates an output signal component that varies in both amplitude and frequency, as shown by the lower curve. The lower horizontal scale shows the periodic variation in the frequency of the output component. Note that at the carrier frequency and its harmonics, both the frequency and amplitude of the response go the zero. These characteristics can be exploited in certain applications. It should be noted that when C_1 is zero, the carrier frequency is nominally 500kHz and the –3dB point of the amplifier is 60kHz. Spurious signals at the output are not significant under these circumstances unless the input signal contains significant components above 250kHz.

There are two ways to use these characteristics. One is to move the carrier frequency low enough that the troublesome signal components are attenuated to an acceptable level as shown in Signal Response vs Carrier Frequency. This in effect limits the bandwidth of the amplifier. The Synchronization Range performance curve shows the relationship between carrier frequency and the value of C_1. To maintain stability, C_2 must also be connected and must be equal to or larger in value than C_1. C_2 may be further increased in value for additional attenuation of the undesired signal components and provides the additional benefit of reducing the residual carrier ripple at the output. See the Bandwidth vs C_2 performance curve.

When periodic noise from external sources such as system clocks and DC/DC converters are a problem, ISO120 and ISO121 can be used to reject this noise. The amplifier can be synchronized to an external frequency source, f_{EXT}, placing the amplifier response curve at one of the frequency and amplitude nulls indicated in the Signal Response vs Carrier Frequency performance curve. For proper synchronization, choose C_1 as shown in the Synchronization Range performance curve. Remember that $C_2 \geq C_1$ is a necessary condition for stability of the isolation amplifier. This curve shows the range of lock at the fundamental frequency for a 4V sinusoidal signal source. The applications section shows the ISO120 and ISO121 synchronized to isolation power sup-

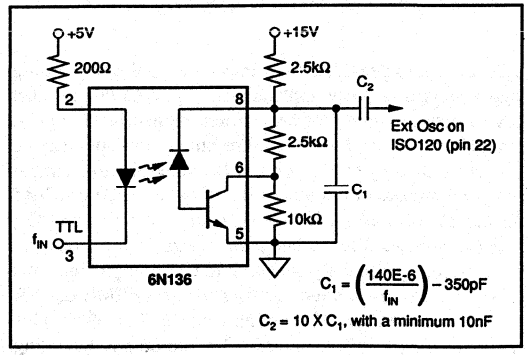


FIGURE 5. Synchronization with Isolated Drive Circuit for Ext Osc Pin.

plies, while Figure 5 shows circuitry with opto-isolation suitable for driving the Ext Osc input from TTL levels.

ISOLATION MODE VOLTAGE

Isolation mode voltage (IMV) is the voltage appearing between isolated grounds Gnd 1 and Gnd 2. IMV can induce error at the output as indicated by the plots of IMV vs Frequency. It should be noted that if the IMV frequency exceeds $f_C/2$, the output will display spurious outputs in a manner similar to that described above, and the amplifier response will be identical to that shown in the Signal Response vs Carrier Frequency performance curve. This occurs because IMV-induced errors behave like input-referred error signals. To predict the total IMR, divide the isolation voltage by the IMR shown in IMR vs Frequency performance curve and compute the amplifier response to this input-referred error signal from the data given in the Signal Response vs Carrier Frequency performance curve. Due to effects of very high-frequency signals, typical IMV performance can be achieved only when dV/dT of the isolation mode voltage falls below 1000V/µs. For convenience, this is plotted in the typical performance curves for the ISO120 and ISO121 as a function of voltage and frequency for sinusoidal voltages. When dV/dT exceeds 1000V/µs but falls below 20kV/µs, performance may be degraded. At rates of change above 20kV/µs, the amplifier may be damaged, but the barrier retains its full integrity. Lowering the power supply voltages below ±15V may decrease the dV/dT to 500V/µs for typical performance, but the maximum dV/dT of 20kV/µs remains unchanged.

Leakage current is determined solely by the impedance of the 2pF barrier capacitance and is plotted in the Isolation Leakage Current vs Frequency curve.

ISOLATION VOLTAGE RATINGS

Because a long-term test is impractical in a manufacturing situation, the generally accepted practice is to perform a production test at a higher voltage for some shorter time. The relationship between actual test voltage and the continuous derated maximum specification is an important one. Historically, Burr-Brown has chosen a deliberately conservative one: V_{TEST} = (2 X ACrms continuous rating) + 1000V for 10 seconds, followed by a test at rated ACrms voltage for one minute. This choice was appropriate for conditions where system transients are not well defined.

Recent improvements in high-voltage stress testing have produced a more meaningful test for determining maximum permissible voltage ratings, and Burr-Brown has chosen to apply this new technology in the manufacture and testing of the ISO120 and ISO121.

Partial Discharge

When an insulation defect such as a void occurs within an insulation system, the defect will display localized corona or ionization during exposure to high-voltage stress. This ionization requires a higher applied voltage to start the discharge and lower voltage to maintain it or extinguish it once started. The higher start voltage is known as the inception voltage, while the extinction voltage is that level of voltage stress at which the discharge ceases. Just as the total insulation system has an inception voltage, so do the individual voids. A voltage will build up across a void until its inception voltage is reached, at which point the void will ionize, effectively shorting itself out. This action redistributes electrical charge within the dielectric and is known as partial discharge. If, as is the case with AC, the applied voltage gradient across the device continues to rise, another partial discharge cycle begins. The importance of this phenomenon is that, if the discharge does not occur, the insulation system retains its integrity. If the discharge begins, and is allowed to continue, the action of the ions and electrons within the defect will eventually degrade any organic insulation system in which they occur. The measurement of partial discharge is still useful in rating the devices and providing quality control of the manufacturing process. Since the ISO120 and ISO121 do not use organic insulation, partial discharge is non-destructive.

The inception voltage for these voids tends to be constant, so that the measurement of *total charge* being redistributed within the dielectric is a very good indicator of the size of the voids and *their likelihood of becoming an incipient failure.* The *bulk inception voltage*, on the other hand, varies with the insulation system, and the number of ionization defects and directly establishes the *absolute maximum voltage* (transient) that can be applied across the test device before destructive partial discharge can begin. Measuring the *bulk extinction voltage* provides a lower, more conservative voltage from which to derive a *safe continuous rating.* In production, measuring at a level somewhat below the expected inception voltage and then derating by a factor related to expectations about system transients is an accepted practice.

Partial Discharge Testing

Not only does this test method provide far more qualitative information about stress-withstand levels than did previous stress tests, but it provides quantitative measurements from which quality assurance and control measures can be based. Tests similar to this test have been used by some manufacturers, such as those of high-voltage power distribution equipment, for some time, but they employed a simple measurement of RF noise to detect ionization. This method was not quantitative with regard to energy of the discharge, and was not sensitive enough for small components such as isolation amplifiers. Now, however, manufacturers of HV test equipment have developed means to quantify partial discharge. VDE, the national standards group in Germany and an acknowledged leader in high-voltage test standards, has developed a standard test method to apply this powerful technique. Use of partial discharge testing is an improved method for measuring the integrity of an isolation barrier.

To accommodate poorly-defined transients, the part under test is exposed to voltage that is 1.6 times the continuous-rated voltage and must display ≤5pC partial discharge level in a 100% production test.

BURN-IN SCREENING

Burn-in screening is an option available for the ISO120 and ISO121 products. Burn-in duration is 160 hours at +125°C (or equivalent combination of time and temperature).

All units are tested after burn-in to ensure that grade specifications are met. To order burn-in, add "-BI" to the base model number.

APPLICATIONS

The ISO120 and ISO121 isolation amplifiers are used in three categories of applications:

1. Accurate isolation of signals from high voltage ground potentials,
2. Accurate isolation of signals from severe ground noise and,
3. Fault protection from high voltages in analog measurements.

Figures 6 through 11 show a variety of Application Circuits.

APPLICATION CIRCUITS

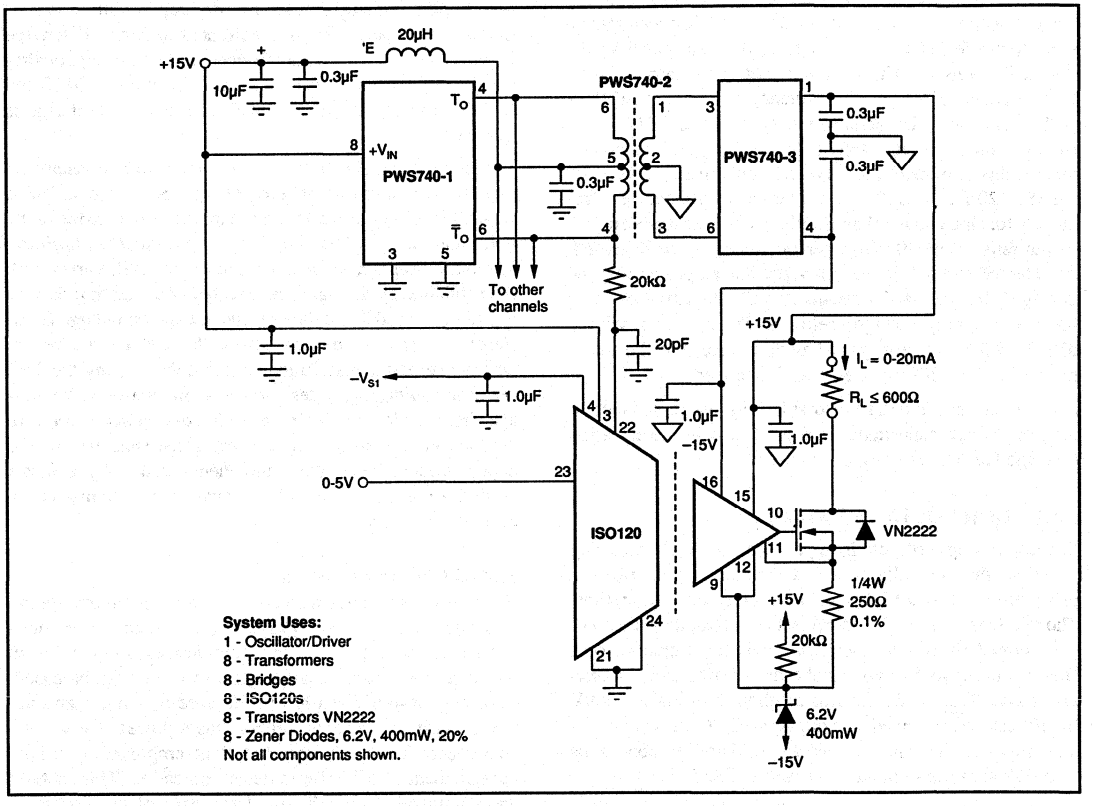


FIGURE 6. Eight-channel Isolated 0-20mA Loop Driver.

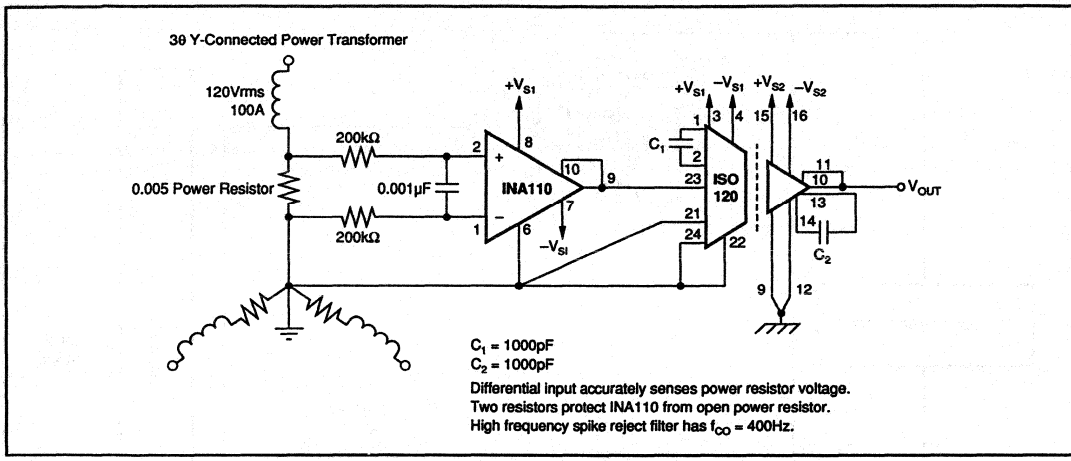


FIGURE 7. Isolated Powerline Monitor.

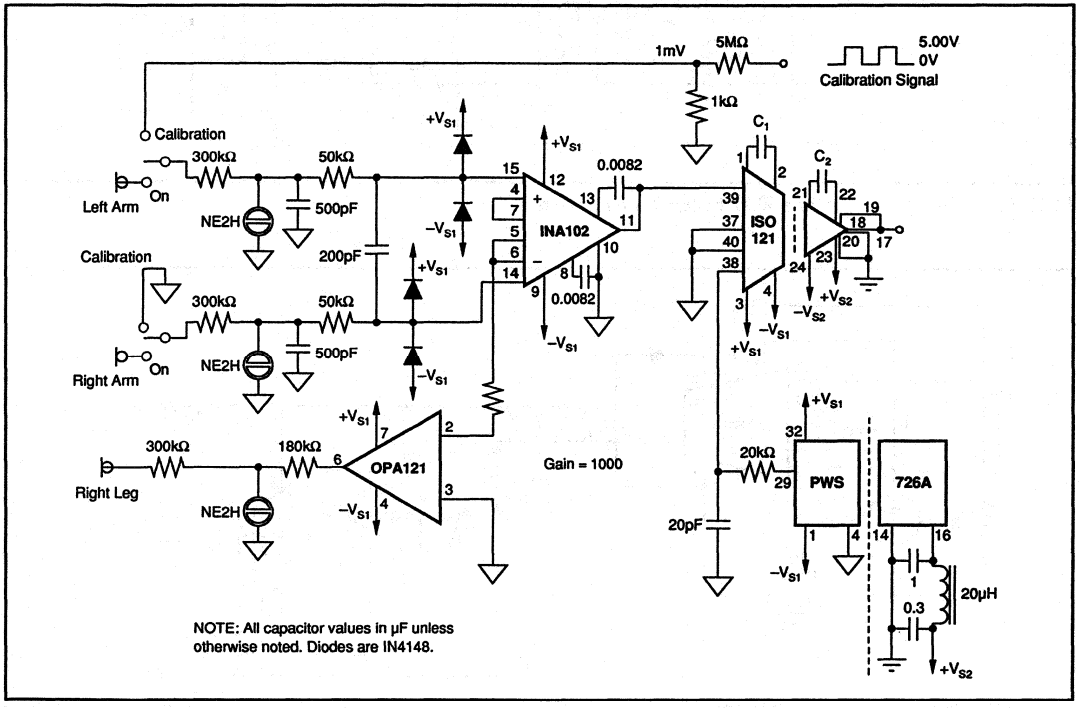


FIGURE 8. Right-Leg Driven ECG Amplifier (with defibrillator protection and calibration).

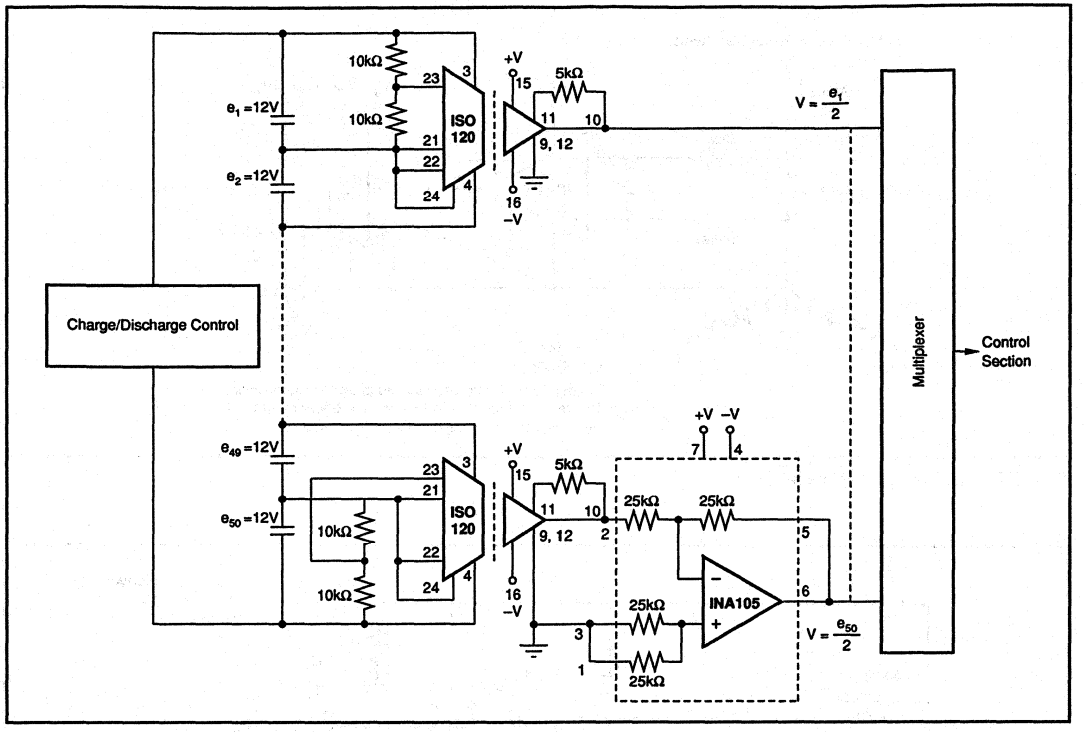


FIGURE 9. Battery Monitor for a 600V Battery Power System.

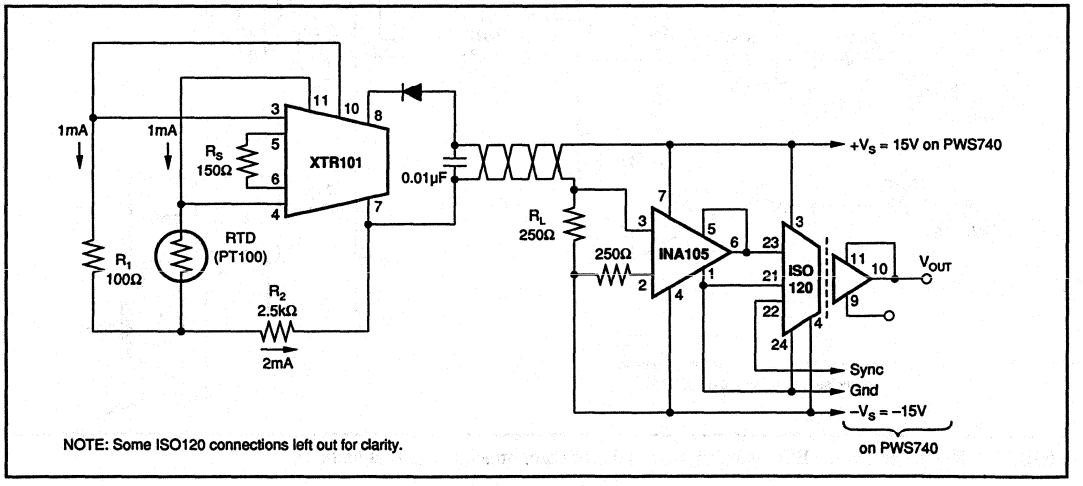


FIGURE 10. Isolated 4-20mA Instrument Loop. (RTD shown).

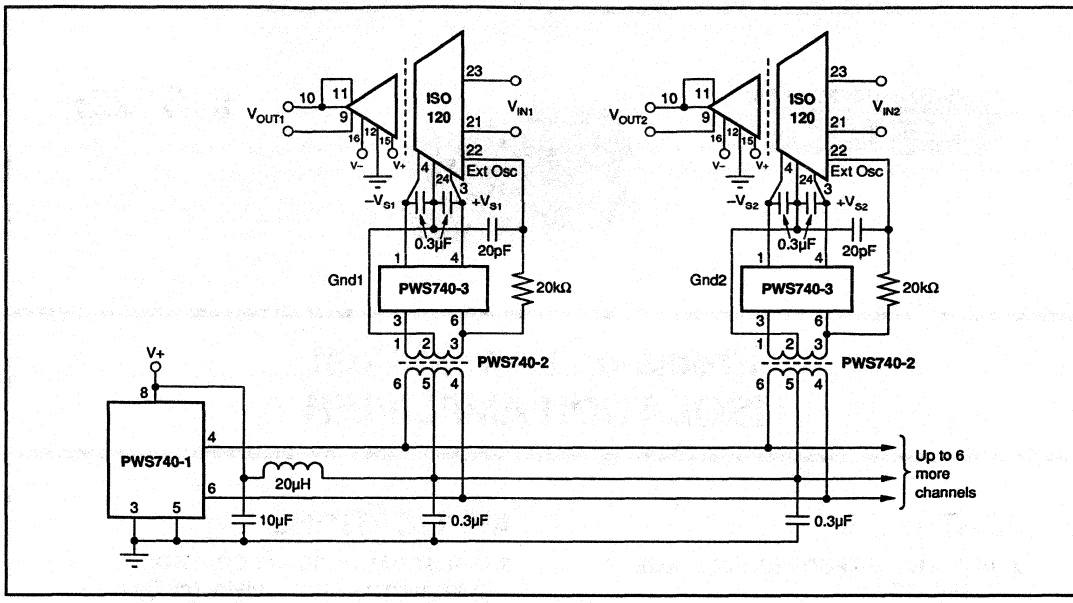
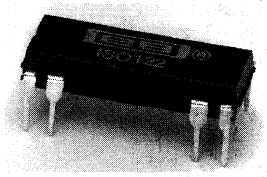


FIGURE 11. Synchronized-Multichannel Isolation System.

ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

BURR-BROWN®



ISO122P

Precision Lowest Cost ISOLATION AMPLIFIER

FEATURES

- 100% TESTED FOR HIGH-VOLTAGE BREAKDOWN
- RATED 1500Vrms
- HIGH IMR: 140dB at 60Hz
- BIPOLAR OPERATION: $V_O = \pm 10V$
- SINGLE-WIDE 16-PIN PLASTIC DIP
- EASE OF USE: Fixed Unity Gain Configuration
- 0.020% max NONLINEARITY
- ±4.5V to ±18V SUPPLY RANGE

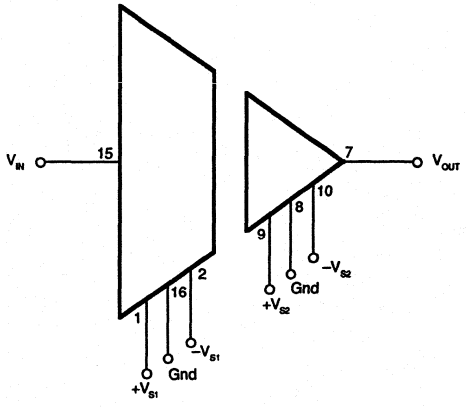
APPLICATIONS

- INDUSTRIAL PROCESS CONTROL: Transducer Isolator, Isolator for Thermocouples, RTDs, Pressure Bridges, and Flow Meters, 4mA to 20mA Loop Isolation
- GROUND LOOP ELIMINATION
- MOTOR AND SCR CONTROL
- POWER MONITORING
- PC-BASED DATA ACQUISITION
- TEST EQUIPMENT
- VENDING MACHINES

DESCRIPTION

The ISO122P is a precision isolation amplifier incorporating a novel duty cycle modulation-demodulation technique. The signal is transmitted digitally across a 2pF differential capacitive barrier. With digital modulation the barrier characteristics do not affect signal integrity, resulting in excellent reliability and good high frequency transient immunity across the barrier. Both barrier capacitors are imbedded in the plastic body of the package.

The ISO122P is easy to use. No external components are required for operation. The key specifications are 0.020% max nonlinearity, 50kHz signal bandwidth, and 200µV/°C V_{OS} drift. A power supply range of ±4.5V to ±18V and quiescent currents of ±4.5mA on V_{S1} and ±5.0mA on V_{S2} make these amplifiers ideal for a wide range of applications.



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Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

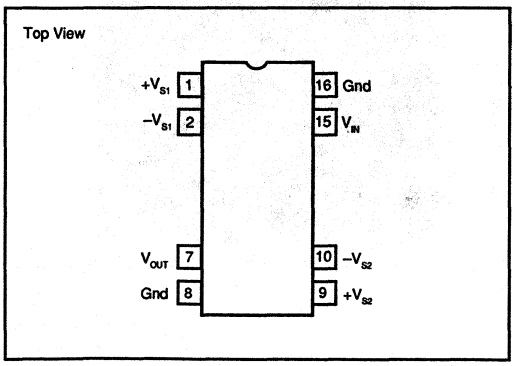
SPECIFICATIONS

At T_A = +25°C , V_{S1} = V_{S2} = ±15V, and R_L = 2kΩ unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
ISOLATION					
Voltage Rated Continuous AC 60Hz		1500			VAC
100% Test [1]	1s, 5pc PD	2400			VAC
Isolation Mode Rejection	60Hz		140		dB
Barrier Impedance			10^{14} || 2		Ω || pF
Leakage Current at 60Hz	V_{ISO} = 240Vrms		0.18	0.5	µArms
GAIN	V_O = ±10V				
Nominal Gain			1		V/V
Gain Error			±0.05	±0.50	%FSR
Gain vs Temperature			±10		ppm/°C
Nonlinearity P			±0.008	±0.020	%FSR
JP			±0.020	±0.050	%FSR
INPUT OFFSET VOLTAGE					
Initial Offset			±5	±50	mV
vs Temperature			±200		µV/°C
vs Supply			±2		mV/V
Noise			4		µV/√Hz
INPUT					
Voltage Range[2]		±10	±12.5		V
Resistance			200		kΩ
OUTPUT					
Voltage Range		±10	±12.5		V
Current Drive		±5	±20		mA
Capacitive Load Drive			0.1		µF
Ripple Voltage[3]			20		mVp-p
FREQUENCY RESPONSE					
Small Signal Bandwidth			50		kHz
Slew Rate			2		V/µs
Settling Time	V_O = ±10V				
0.1%			50		µs
0.01%			350		µs
Overload Recover Time			150		µs
POWER SUPPLIES					
Rated Voltage			±15		V
Voltage Range		±4.5		±18	V
Quiescent Current: V_{S1}			±4.5	±7.0	mA
V_{S2}			±5.0	±7.0	mA
TEMPERATURE RANGE					
Specification		0		70	°C
Operating		–25		85	°C
Storage		–25		85	°C
θ_{JA}			100		°C/W

NOTES: (1) Tested at 1.6 X rated, fail on 5pC partial discharge. (2) Input Range is ±10V independent of input ±V_{S1}. (3) Ripple frequency is at carrier frequency (500kHz).

CONNECTION DIAGRAM

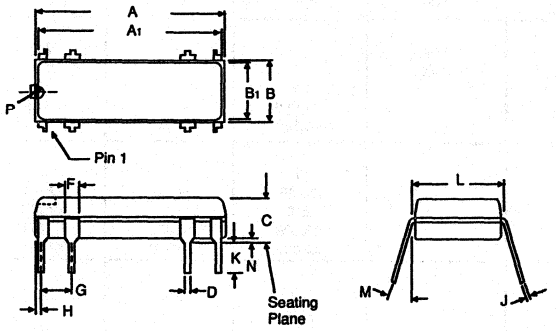


ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18V
V_{IN}	±100V
Continuous Isolation Voltage	1500Vrms
Junction Temperature	+150°C
Storage Temperature	+85°C
Lead Temperature (soldering, 10s)	+300°C
Output Short to Common	Continuous

MECHANICAL

P Package — Single-Wide 16-Pin Plastic DIP



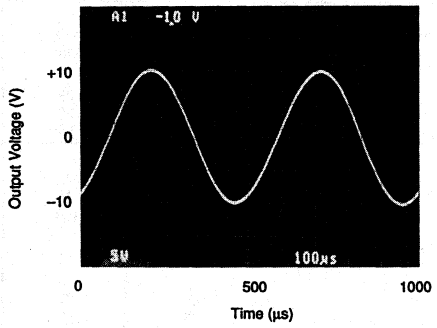
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.740	.800	18.80	20.32
A1	.725	.785	18.42	19.94
B	.230	.290	5.85	7.38
B1	.200	.250	5.09	6.36
C	.120	.200	3.05	5.09
D	.015	.023	0.38	0.59
F	.030	.070	0.76	1.78
G	.100 BASIC		2.54 BASIC	
H	0.20	.050	0.51	1.27
J	.008	.015	0.20	0.38
K	.070	.150	1.78	3.82
L	.300 BASIC		7.63 BASIC	
M	0°	15°	0°	15°
N	.010	.030	0.25	0.76
P	.025	.050	0.64	1.27

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.

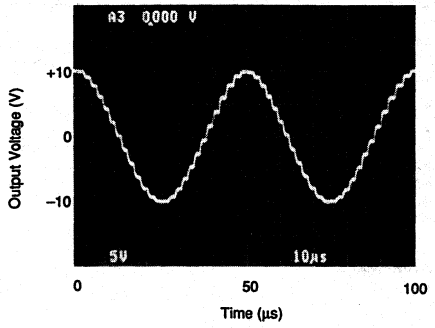
TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_S = ±15V unless otherwise noted.

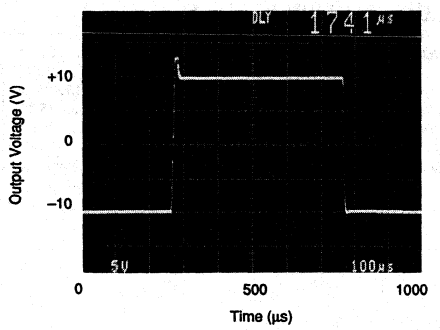
SINE RESPONSE
(f = 2kHz)



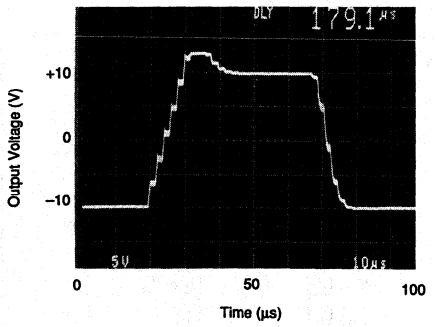
SINE RESPONSE
(f = 20kHz)



STEP RESPONSE

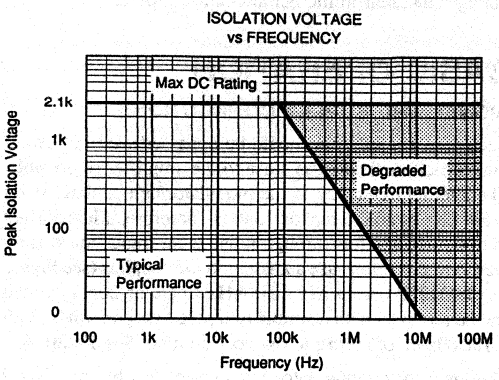


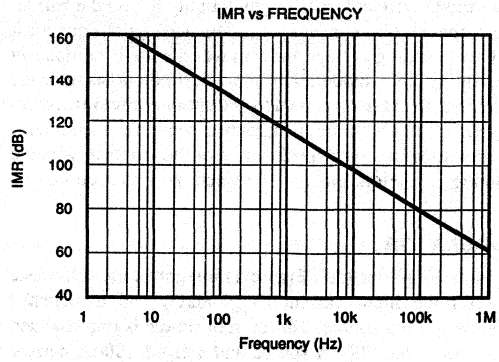
STEP RESPONSE

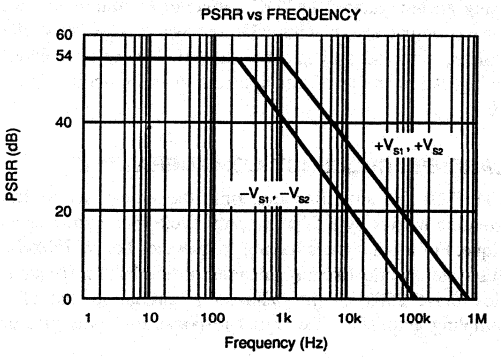


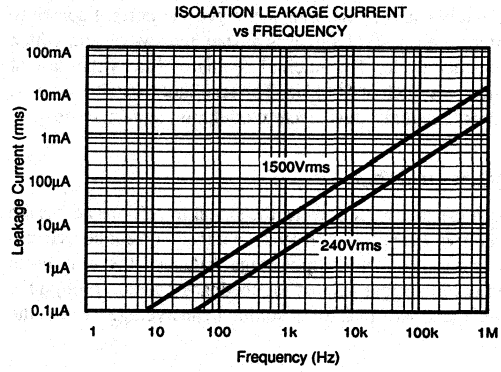
TYPICAL PERFORMANCE CURVES

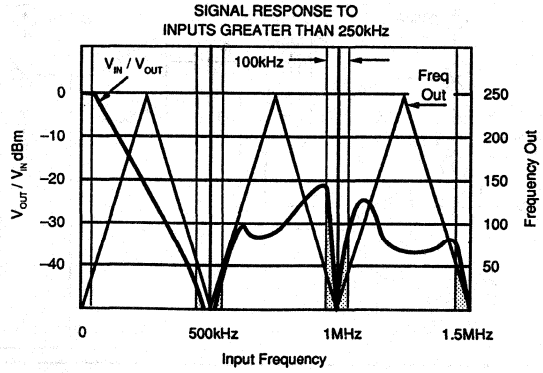
T_A = +25°C, V_S = ±15V unless otherwise noted.











(NOTE: Shaded area shows aliasing frequencies that cannot be removed by a low-pass filter at the output.)

THEORY OF OPERATION

The ISO122P isolation amplifier uses an input and an output section galvanically isolated by matched 1pF isolating capacitors built into the plastic package. The input is duty-cycle modulated and transmitted digitally across the barrier. The output section receives the modulated signal, converts it back to an analog voltage and removes the ripple component inherent in the demodulation. Input and output sections are fabricated, then laser trimmed for exceptional circuitry matching common to both input and output sections. The sections are then mounted on opposite ends of the package with the isolating capacitors mounted between the two sections.

MODULATOR

An input amplifier (A1, Figure 1) integrates the difference between the input current (V_{IN}/200kΩ) and a switched ±100µA current source. This current source is implemented by a switchable 200µA source and a fixed 100µA current sink. To understand the basic operation of the modulator, assume that V_{IN} = 0.0V. The integrator will ramp in one direction until the comparator threshold is exceeded. The comparator and sense amp will force the current source to switch; the resultant signal is a triangular waveform with a 50% duty cycle. The internal oscillator forces the current source to switch at 500kHz. The resultant capacitor drive is a complementary duty-cycle modulation square wave.

DEMODULATOR

The sense amplifier detects the signal transitions across the capacitive barrier and drives a switched current source into integrator A2. The output stage balances the duty-cycle modulated current against the feedback current through the 200kΩ feedback resistor, resulting in an average value at the V_{OUT} pin equal to V_{IN}. The sample and hold amplifiers in the output feedback loop serve to remove undesired ripple voltages inherent in the demodulation process.

BASIC OPERATION

SIGNAL AND SUPPLY CONNECTIONS

Each power supply pin should be bypassed with 1µF tantalum capacitors located as close to the amplifier as possible. The internal frequency of the modulator/demodulator is set at 500kHz by an internal oscillator. Therefore, if it is desired to minimize any feedthrough noise (beat frequencies) from a DC/DC converter, use a π filter on the supplies (see Figure 4). ISO122P output has a 500kHz ripple of 20mV, which can be removed with a simple two pole low-pass filter with a 100kHz cutoff using a low cost op amp. See Figure 4.

The input to the modulator is a current (set by the 200kΩ integrator input resistor) that makes it possible to have an input voltage greater than the input supplies, as long as the output supply is at least ±15V. It is therefore possible when using an unregulated DC/DC converter to minimize PSR related output errors with ±5V voltage regulators on the isolated side and still get the full ±10V input and output swing. An example of this application is shown in Figure 10.

CARRIER FREQUENCY CONSIDERATIONS

The ISO122P amplifier transmits the signal across the isolation barrier by a 500kHz duty cycle modulation technique. For input signals having frequencies below 250kHz, this system works like any linear amplifier. But for frequencies above 250kHz, the behavior is similar to that of a sampling amplifier. The signal response to inputs greater

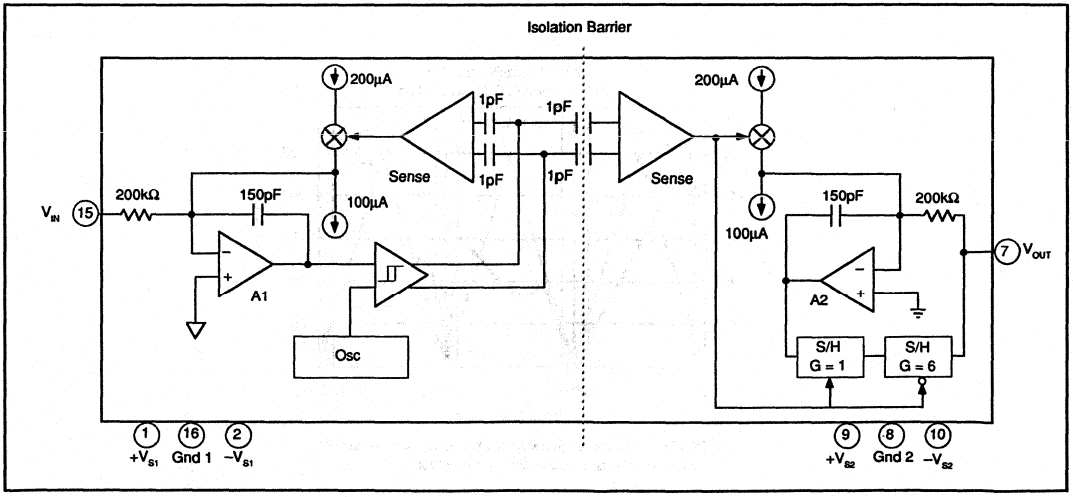


FIGURE 1. Block Diagram.

than 250kHz performance curve shows this behavior graphically; at input frequencies above 250kHz the device generates an output signal component of reduced magnitude at a frequency below 250kHz. This is the aliasing effect of sampling at frequencies less than 2 times the signal frequency (the Nyquist frequency). Note that at the carrier frequency and its harmonics, both the frequency and amplitude of the aliasing go to zero.

ISOLATION MODE VOLTAGE INDUCED ERRORS

IMV can induce errors at the output as indicated by the plots of IMV vs Frequency. It should be noted that if the IMV frequency exceeds 250kHz, the output also will display spurious outputs (aliasing), in a manner similar to that for V_{IN} > 250kHz and the amplifier response will be identical to that shown in the Signal Response to Inputs Greater Than 250kHz performance curve. This occurs because IMV-induced errors behave like input-referred error signals. To predict the total error, divide the isolation voltage by the IMR shown in the IMR vs Frequency curve and compute the amplifier response to this input-referred error signal from the data given in the Signal Response to Inputs Greater than 250kHz performance curve. For example, if a 800kHz 1000Vrms IMR is present, then a total of [(–60dB) + (–30dB)] x (1000V) = 32mV error signal at 200kHz plus a 1V, 800kHz error signal will be present at the output.

HIGH IMV dV/dt ERRORS

As the IMV frequency increases and the dV/dt exceeds 1000V/µs, the sense amp may start to false trigger, and the output will display spurious errors. The common mode current being sent across the barrier by the high slew rate is the cause of the false triggering of the sense amplifier. Lowering the power supply voltages below ±15V may decrease the dV/dt to 500V/µs for typical performance.

HIGH VOLTAGE TESTING

Burr-Brown Corporation has adopted a partial discharge test criterion that conforms to the German VDE0884 Optocoupler Standards. This method requires the measurement of minute current pulses (<5pC) while applying 2400Vrms, 60Hz high voltage stress across every ISO122 isolation barrier. No partial discharge may be initiated to pass this test. This criterion confirms transient overvoltage (1.6 x 1500Vrms) protection without damage to the ISO122. Lifetest results verify the absence of failure under continuous rated voltage and maximum temperature.

This new test method represents the "state of the art" for non-destructive high voltage reliability testing. It is based on the effects of non-uniform fields that exist in heterogeneous dielectric material during barrier degradation. In the case of void non-uniformities, electric field stress begins to ionize the void region before bridging the entire high voltage barrier. The transient conduction of charge during and after the ionization can be detected externally as a burst of 0.01-0.1µs current pulses that repeat on each AC voltage cycle. The minimum AC barrier voltage that inititates partial discharge is defined as the "inception voltage." Decreasing the barrier voltage to a lower level is required before partial discharge ceases and is defined as the "extinction voltage." We have characterized and developed the package insulation processes to yield an inception voltage in excess of 2400Vrms so that transient overvoltages below this level will not damage the ISO122. The extinction voltage is above 1500Vrms so that even overvoltage induced partial discharge will cease once the barrier voltage is reduced to the 1500Vrms (rated) level. Older high voltage test methods relied on applying a large enough overvoltage (above rating) to break down marginal parts, but not so high as to damage good ones. Our new partial discharge testing gives us more confidence in barrier reliability than breakdown/no breakdown criteria.

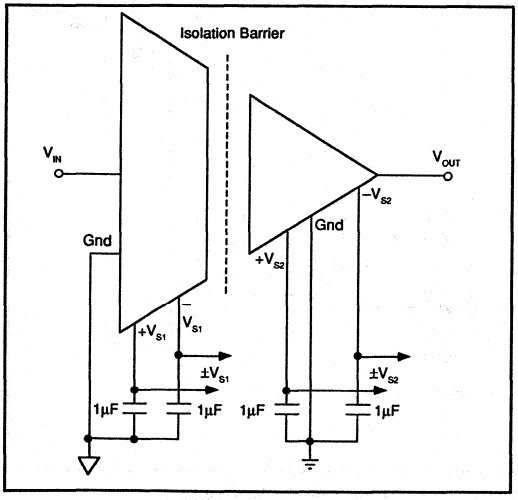


FIGURE 2. Basic Signal and Power Connections.

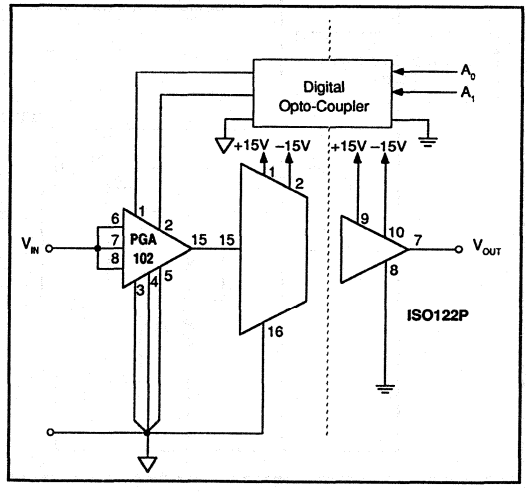


FIGURE 3. Programmable-Gain Isolation Channel with Gains of 1, 10, and 100.

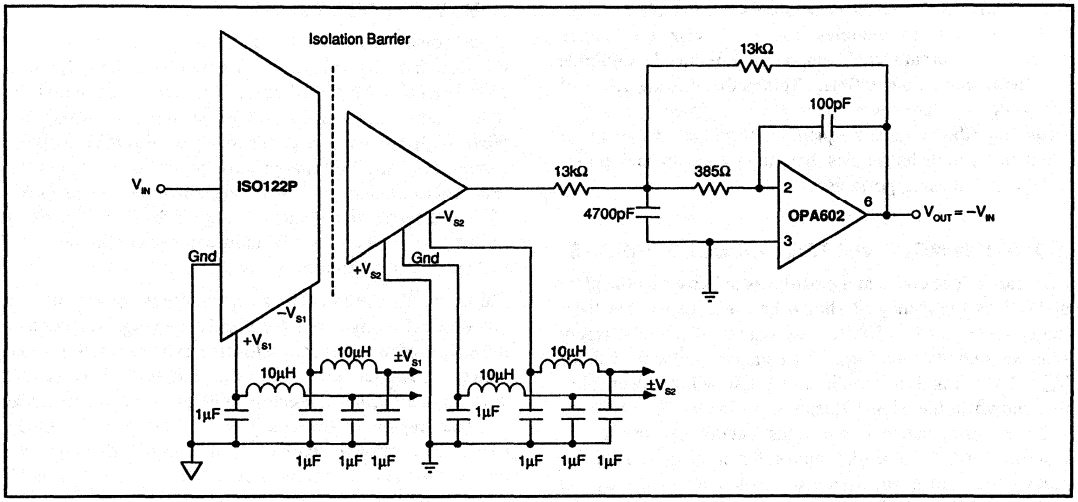


FIGURE 4. Optional π Filter to Minimize Power Supply Feedthrough Noise; Output Filter to Remove 500kHz Carrier Ripple.

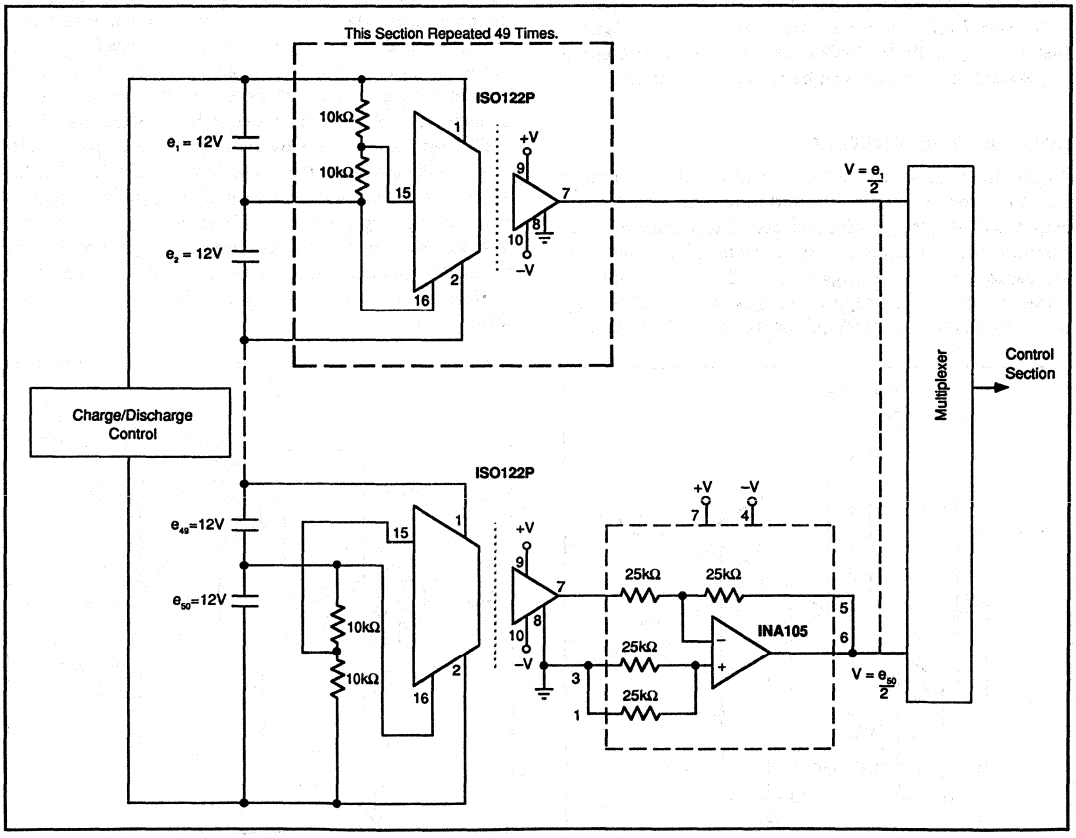
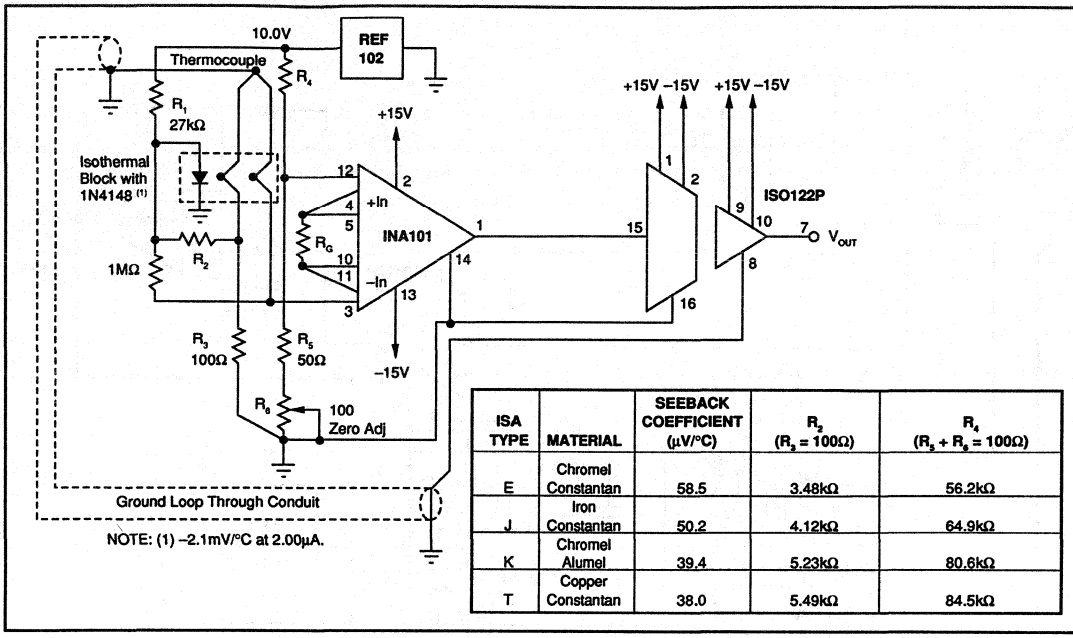


FIGURE 5. Battery Monitor for a 600V Battery Power System. (Derives Input Power from the Battery.)



ISA TYPE	MATERIAL	SEEBACK COEFFICIENT (μV/°C)	R_2 (R_3 = 100Ω)	R_4 (R_5 + R_6 = 100Ω)
E	Chromel Constantan	58.5	3.48kΩ	56.2kΩ
J	Iron Constantan	50.2	4.12kΩ	64.9kΩ
K	Chromel Alumel	39.4	5.23kΩ	80.6kΩ
T	Copper Constantan	38.0	5.49kΩ	84.5kΩ

FIGURE 6. Thermocouple Amplifier with Ground Loop Elimination, Cold Junction Compensation, and Up-scale Burn-out.

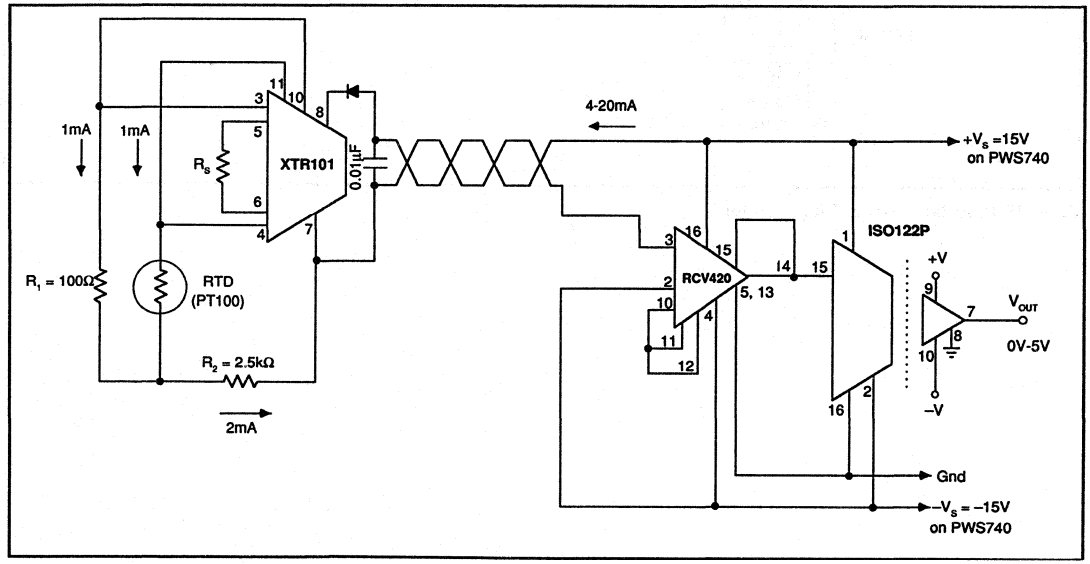


FIGURE 7. Isolated 4-20mA Instrument Loop. (RTD shown.)

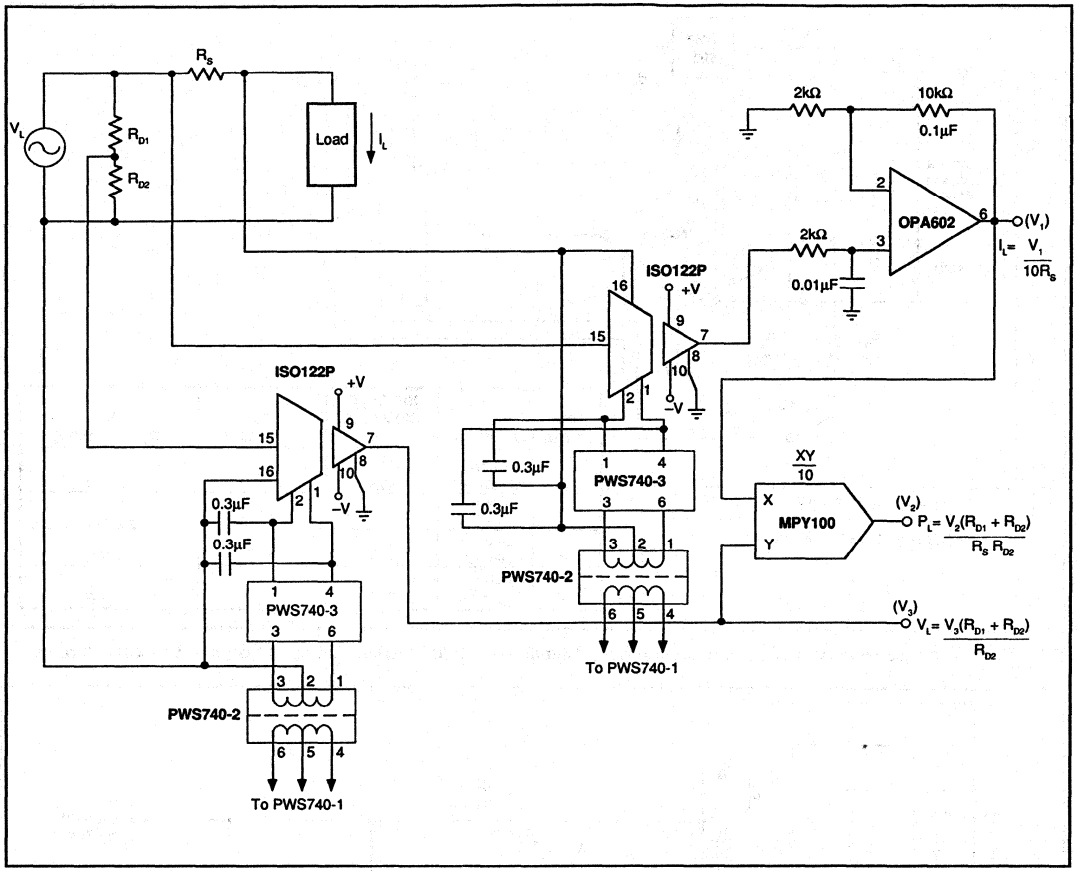


FIGURE 8. Isolated Power Line Monitor.

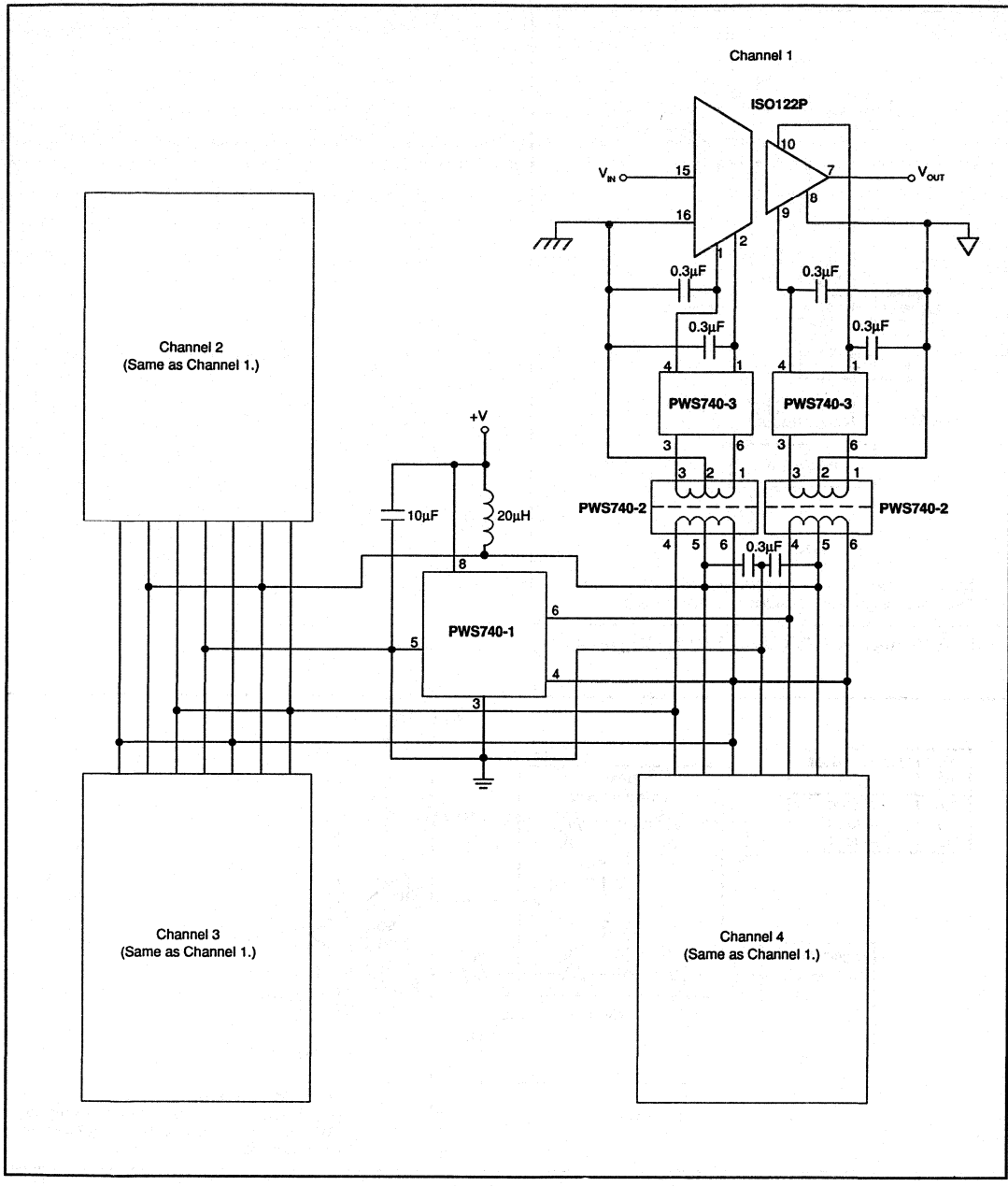


FIGURE 9. Three-Port, Low-Cost, Four-Channel Isolated, Data Acquisition System.

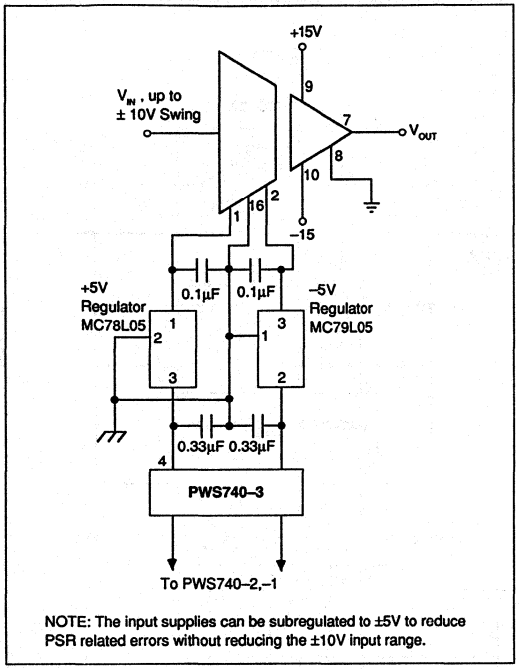


FIGURE 10. Improved PSR Using External Regulator.

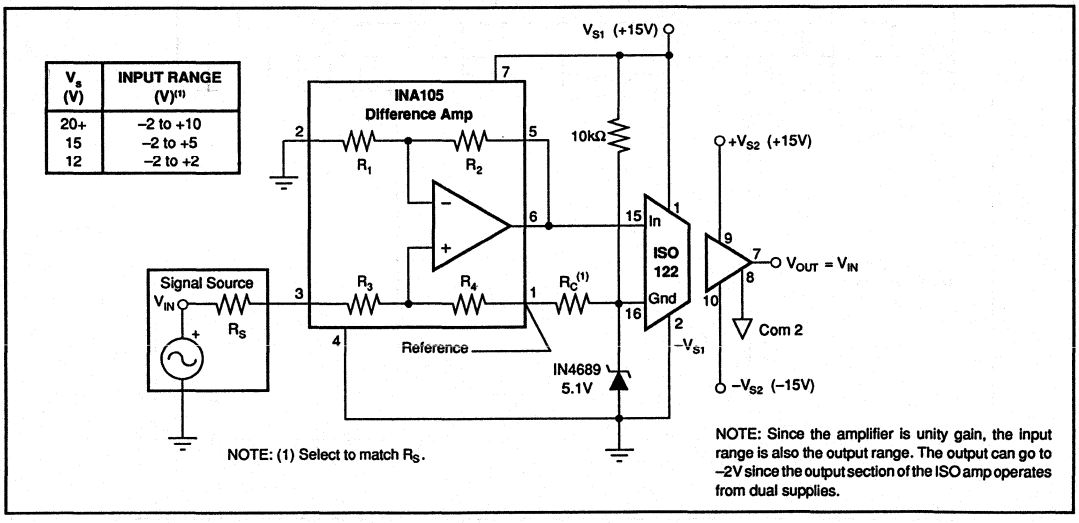


FIGURE 11. Single Supply Operation of the ISO122 Isolation Amplifier.

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

BURR-BROWN®

ISO212P

Low Cost, Two-Port Isolated, Low Profile ISOLATION AMPLIFIER

FEATURES

- 12-BIT ACCURACY
- LOW PROFILE (LESS THAN 0.5" HIGH)
- SMALL FOOTPRINT
- EXTERNAL POWER CAPABILITY (±8V at 5mA)
- "MASTER/SLAVES" SYNCHRONIZATION CAPABILITY
- INPUT OFFSET ADJUSTMENT
- LOW POWER (75mW)
- SINGLE 10V TO 15V SUPPLY OPERATION

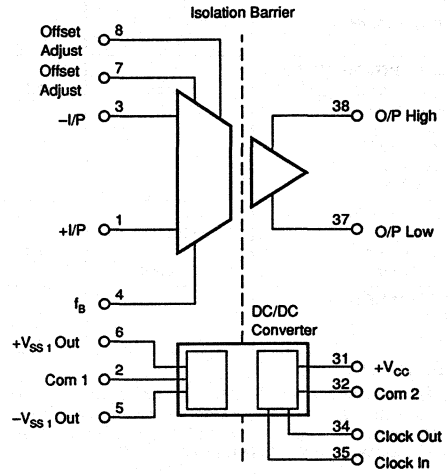
APPLICATIONS

- INDUSTRIAL PROCESS CONTROL: Transducer Channel Isolator for Thermocouples, RTDs, Pressure Bridges, Flow Meters
- 4mA TO 20mA LOOP ISOLATION
- MOTOR AND SCR CONTROL
- GROUND LOOP ELIMINATION
- ANALYTICAL MEASUREMENTS
- POWER PLANT MONITORING
- DATA ACQUISITION/TEST EQUIPMENT ISOLATION
- MULTIPLEXED SYSTEMS WITH CHANNEL TO CHANNEL ISOLATION

DESCRIPTION

The ISO212P signal isolation amplifier is a member of a series of low-cost isolation products from Burr-Brown. The low-profile SIL plastic package allows PCB spacings of 0.5" to be achieved, and the small footprint results in efficient use of board space.

To provide isolation, the design uses high-efficiency, miniature toroidal transformers in both the signal and power paths. An uncommitted input amplifier and an isolated external bipolar supply ensure the majority of input interfacing or conditioning needs can be met. The ISO212P accepts an input voltage range of ±5V for single 15V supply operation or ±3.0V for single 10V supply operation.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL

At T = +25°C and V_{CC} = +15V unless otherwise noted.

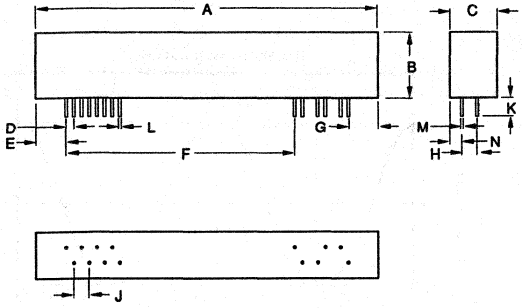
PARAMETER	CONDITIONS	ISO212JP MIN	ISO212JP TYP	ISO212JP MAX	ISO212KP MIN	ISO212KP TYP	ISO212KP MAX	UNITS
ISOLATION								
Voltage								
Rated Continuous								
AC, 60Hz	T_{MIN} to T_{MAX}	750			*			Vrms
DC	T_{MIN} to T_{MAX}	1060			*			VDC
100% Test (AC, 60Hz)	Partial Discharge 1s : <5pC	1200			*			Vrms
Isolation-Mode Rejection[1]	V_{ISO} = Rated Continuous 60Hz							
AC			115			*		dB
DC			160			*		dB
Barrier Resistance			10^{10}			*		Ω
Barrier Capacitance			12			*		pF
Leakage Current	V_{ISO} = 240Vrms, 60Hz		1	2		*	*	µArms
	V_{ISO} = 240Vrms, 50Hz			1.6			*	µArms
GAIN								
Initial Error			±1	±2		*	*	% FSR[2]
Gain vs Temperature			20	50		*	*	ppm of FSR/°C
Nonlinearity[3]	V_O = –5V to +5V		0.04	0.05		0.015	0.025	%FSR
INPUT OFFSET VOLTAGE								
Initial Offset	V_{IN} = 0V			±10 ±10/G			±7.5 ±7.5/G	mV
vs Temperature			±30 ±30/G			*		µV/°C
vs Power Supply[4]	V_{CC} = 14V to 16V		±1.5			*		mV/V
Adjustment Range		±20			*			mV
INPUT CURRENT								
Bias				50			*	nA
Offset				4			*	nA
INPUT								
Voltage Range [5]	Rated Operation, G = 1	±5			*			V
Resistance			10^{12}			*		Ω
OUTPUT								
Voltage Range	Out Hi to Out Lo Min Load = 1MΩ	±5			*			V
Ripple Voltage [6]	f = 0 to 100kHz		8			*		mVp-p
	f = 0 to 5kHz		0.4			*		mVrms
FREQUENCY RESPONSE								
Small Signal Bandwidth	I/P = 1Vp-p, –3dB G = 1		1			*		kHz
Full Signal Bandwidth	I/P = 10Vp-p, G = 1		200			*		Hz
ISOLATED POWER OUTPUTS								
Voltage Outputs ($\pm V_{SS+}$) [7]	No Load	±7.5	±8		*	*		VDC
vs Temperature			–8			*		mV/°C
vs Load			90			*		mV/mA
Current Output [7]								
(Both Loaded)				5			*	mA
(One Loaded)				8			*	mA
POWER SUPPLIES								
Rated Voltage	Rated Performance		15			*		V
Voltage Range [5]		11.4		16	*		*	V
Quiescent Current	No Load		4.3	7		*	*	mA
TEMPERATURE RANGE								
Specification		0		+70	*		*	°C
Operating		–25		+85	*		*	°C

*Same as ISO212JP.

NOTES: (1) Isolation-mode rejection is the ratio of the change in output voltage to a change in isolation barrier voltage. It is a function of frequency. (2) FSR = Full Scale Range = 10V. (3) Nonlinearity is the peak deviation of the output voltage from the best-fit straight line. It is expressed as the ratio of deviation to FSR. (4) Power Supply Rejection is the change in V_{OS}/Supply Change. (5) At V_{CC} = +10.0V, input voltage range = ±3.0V min. (6) Ripple is the residual component of the barrier carrier frequency generated internally. (7) Derated at V_{CC} < +15V.

MECHANICAL ISO212P

P Package —38-Pin Plastic SIP

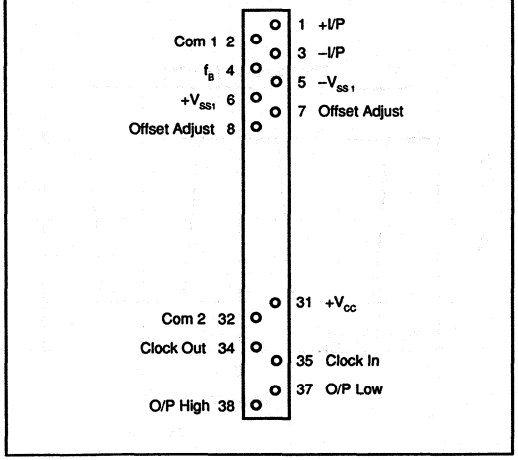


	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	56.39	57.05	2.220	2.246
B	10.54	11.76	0.415	0.463
C	7.49	8.26	0.295	0.325
D	1.27 TYP		0.050 TYP	
E	4.95 TYP		0.195 TYP	
F	38.10 TYP		1.500 TYP	
G	4.78 TYP		0.188 TYP	
H	2.54 TYP		0.100 TYP	
J	2.54 TYP		0.100 TYP	
K	3.18 TYP		0.125 TYP	
L	0.46 TYP		0.018 TYP	
M	0.25 TYP		0.010 TYP	
N	2.03	—	0.08	—

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

PIN CONFIGURATION

Bottom View



ABSOLUTE MAXIMUM RATINGS

Supply Voltage Without Damage	18V
Continuous Isolation Voltage Across Barrier	750Vrms
Storage Temperature Range	–25°C to 100°C
Lead Temperature (soldering, 10s)	+300°C
Amplifier Output Short-Circuit Duration	Continuous to Common
Output Voltage Hi or Lo to Com 2	$\pm V_{CC}/2$

ORDERING INFORMATION

MODEL	PACKAGE	OPERATING TEMPERATURE RANGE
ISO212JP	Plastic SIP	–25°C to +85°C
ISO212KP	Plastic SIP	–25°C to +85°C

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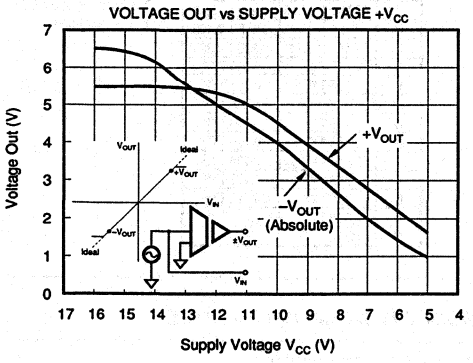
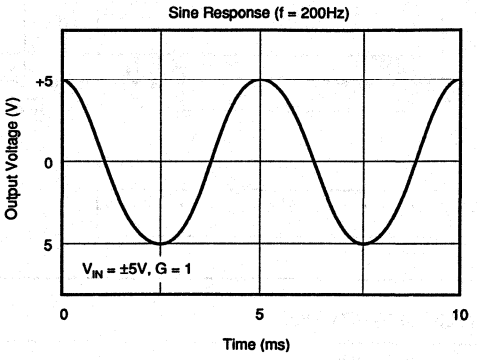
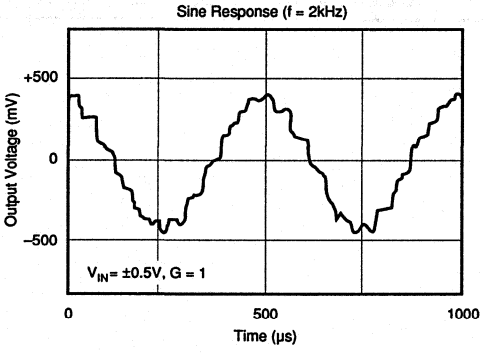
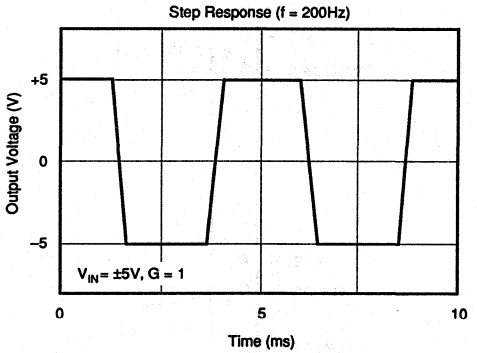
TYPICAL PERFORMANCE CURVES

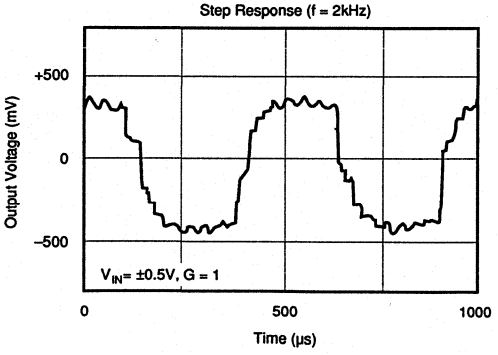
T_A = +25°C, V_S = ±15V unless otherwise noted.

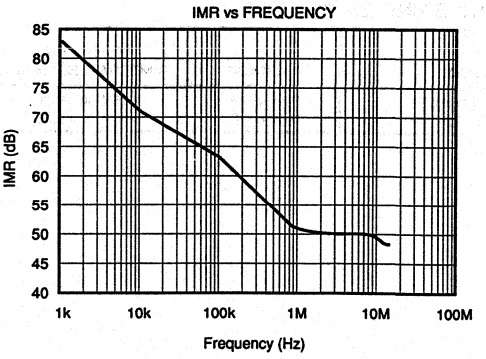






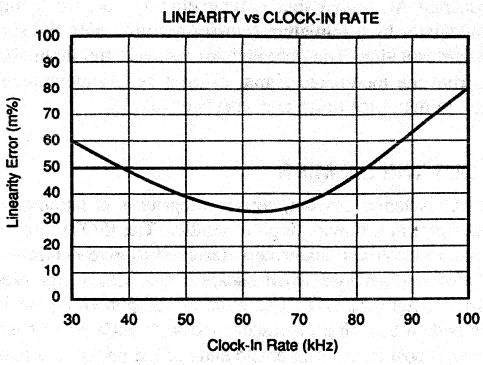


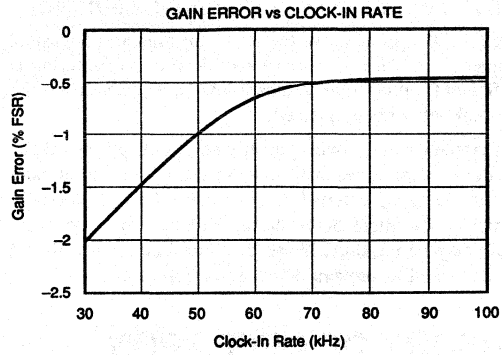




TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_S = ±15V unless otherwise noted.





DISCUSSION OF SPECIFICATIONS

The ISO212P is intended for applications where isolation and input signal conditioning are required. Best signal-to-noise performance is obtained when the input amplifier gain setting is such that the f_B pin has a full scale range of ±5V. The bandwidth is internally limited to typically 1kHz, making the device ideal for use in conjunction with sensors that monitor slowly varying processes. To power external functions or networks, 5mA at ±8V typical is available at the isolated port.

LINEARITY PERFORMANCE

The ISO212P offers non-linearity performance compatible with 12-bit resolution systems (0.025%). Note that the specification is based on a best-fit straight line.

OPTIONAL OFFSET VOLTAGE ADJUSTMENT

In many applications, the untrimmed input offset voltage will be adequate. For situations where it is necessary to trim the offset, a potentiometer can be used. See Figure 1 for details. It is important to keep the traces to the offset adjust pins as short as practical, because noise can be injected into the input op amp via this route.

INPUT PROTECTION

If the ISO212P is used in systems where a transducer or sensor does not derive its power from the isolated power available from the device, then some input protection must be present to prevent damage to the input op amp when the ISO212P is not powered. A resistor of 5kΩ should be included to limit the output impedance of the signal source. Where the op amp is configured for an inverting gain, then R_{IN} of the gain setting network can be used. For non-

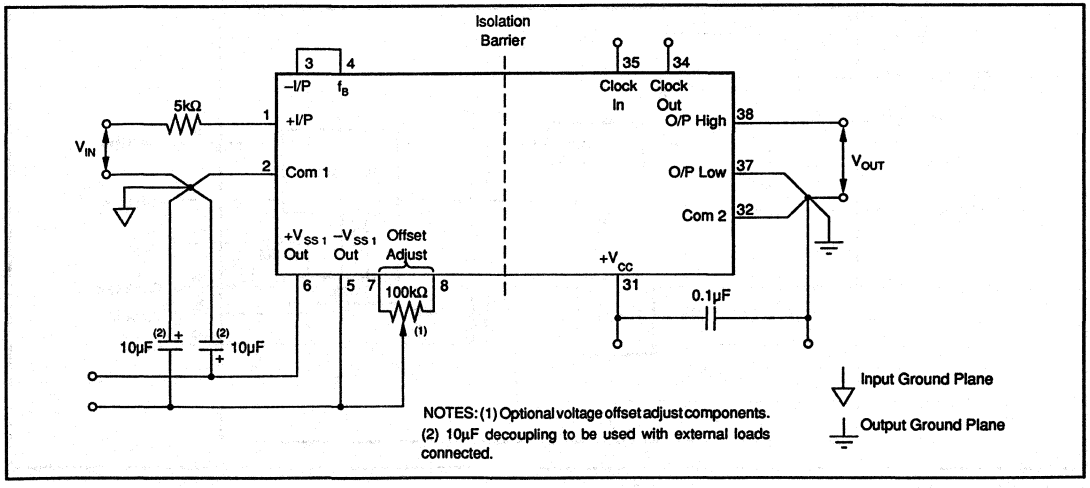


FIGURE 1. Power Supply and Signal Connections Shown for Non-Inverting, Unity Gain Configuration.

inverting configurations, a separate resistor is required. Neglecting this point may also lead to problems when powering on the ISO212P.

USING $\pm V_{SS1}$ TO POWER EXTERNAL CIRCUITRY

The DC/DC converter in the ISO212P runs at a switching frequency of 25kHz. Internal rectification and filtering is sufficient for most applications at low frequencies or with no external networks connected.

The ripple on $\pm V_{SS1}$ will typically be 100mVp-p at 25kHz. Loading the supplies will increase the ripple unless extra filtering is added externally; a capacitor of 1µF is normally sufficient for most applications, although in some cases 10µF may be required. Noise introduced onto $\pm V_{SS1}$ should be decoupled to prevent degraded performance.

THEORY OF OPERATION

The ISO212P has no galvanic connection between the input and output. The analog input signal referenced to the input common (Com 1) is multiplied by the gain of the input amplifier and accurately reproduced at the output. The output section uses a differential design so either the Hi or Lo pin may be referenced to the output common (Com 2). This allows simple input signal inversion while maintaining the high impedance input configuration. A simplified diagram of the ISO212P is shown in Figure 2. The design consists of a DC/DC converter, an uncommitted input operational amplifier, a modulator circuit and a demodulator circuit. Magnetic isolation is provided by separate transformers in the power and signal paths.

The DC/DC converter provides power and synchronization signals across the isolation barrier to operate the operational amplifier and modulator circuitry. It also has sufficient capacity to power external input signal conditioning networks. The uncommitted operational amplifier may be configured for signal buffering or amplification, depending on the application.

The modulator converts the input signal to an amplitude-modulated AC signal that is magnetically coupled to the demodulator by a miniature transformer providing the signal-path isolation. The demodulator recovers the input signal from the modulated signal using a synchronous technique to minimize noise and interference.

ABOUT THE BARRIER

For any isolation product, barrier integrity is of paramount importance in achieving high reliability. The ISO212P uses miniature toroidal transformers designed to give maximum isolation performance when encapsulated with a high-dielectric-strength material. The internal component layout is designed so that circuitry associated with each side of the barrier is positioned at opposite ends of the package. Areas where high electric fields can exist are positioned in the center of the package. The result is that the dielectric strength of the barrier typically exceeds 3kVrms.

ISOLATION VOLTAGE RATINGS

Because a long term test is impractical in a manufacturing situation, the generally accepted practice is to perform a production test at a high voltage for some shorter time. The relationship between actual test voltage and the continuous derated maximum specification is an important one. Historically, Burr-Brown has chosen a deliberately conservative one: V_{TEST} = (2 x ACrms continuous rating) + 1000V for ten seconds, followed by a test at rated ACrms voltage for one minute. This choice was appropriate for conditions where system transients were not well defined.

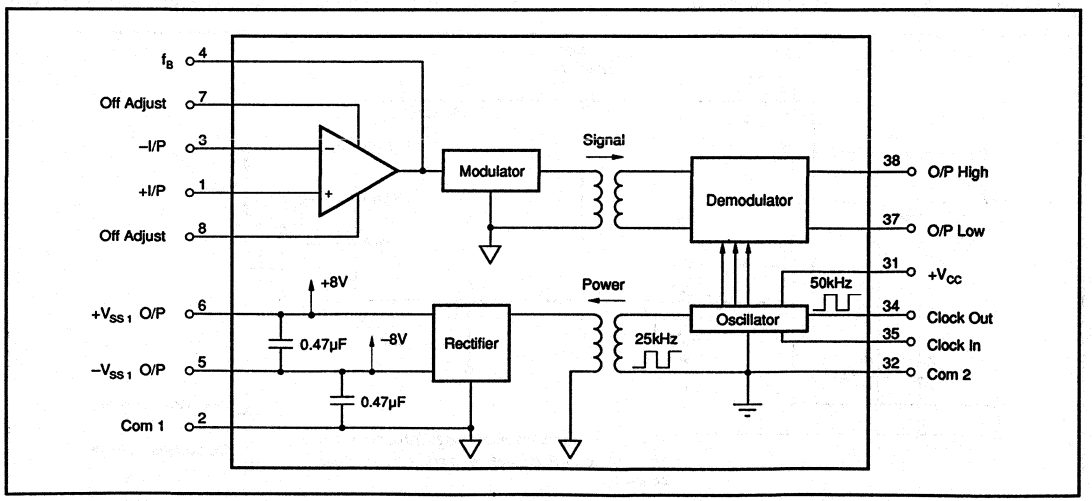


FIGURE 2. Simplified Diagram of Isolation Amplifier.

Recent improvements in high voltage stress testing have produced a more meaningful test for determining maximum permissible voltage ratings, and Burr-Brown has chosen to apply this new technology in the manufacture and testing of the ISO212P.

PARTIAL DISCHARGE

When an insulation defect such as a void occurs within an insulation system, the defect will display localized corona or ionization during exposure to high voltage stress. This ionization requires a higher applied voltage to start the discharge and a lower voltage to extinguish it once started. The higher start voltage is known as the inception voltage and the lower voltage is called the the extinction voltage. Just as the total insulation system has an inception voltage, so do the individual voids. A voltage will build up across a void until its inception voltage is reached. At this point, the void will ionize, effectively shorting itself out. This action redistributes electrical charge within the dielectric and is known as partial discharge. If the applied voltage gradient across the device continues to rise, another partial discharge cycle begins. The importance of this phenomenon is that if the discharge does not occur, the insulation system retains its integrity. If the discharge begins and is allowed to continue, the action of the ions and electrons within the defect will eventually degrade any organic insulation system in which they occur. The measurement of partial discharge is both useful in rating the devices and in providing quality control of the manufacturing process. The inception voltage of these voids tends to be constant, so that the measurement of total charge being re-distributed within the dielectric is a very good indicator of the size of the voids and their likelihood of becoming an incipient failure.

The bulk inception voltage, on the other hand, varies with the insulation system and the number of ionization defects. This directly establishes the absolute maximum voltage (transient) that can be applied across the test device before destructive partial discharge can begin.

Measuring the bulk extinction voltage provides a lower, more conservative, voltage from which to derive a safe continuous rating. In production, it's acceptable to measure at a level somewhat below the expected inception voltage and then de-rate by a factor related to expectations about the system transients. The isolation amplifier has been extensively evaluated under a combination of high temperatures and high voltage to confirm its performance in this respect. The ISO212P is free of partial discharges at rated voltages.

PARTIAL DISCHARGE TESTING IN PRODUCTION

Not only does this test method provide far more qualitative information about stress withstand levels than did previous stress tests, but it also provides quantitative measurements from which quality assurance and control measures can be based. Tests similar to this test have been used by some manufacturers such as those of high voltage power distribution equipment for some time, but they employed a simple measurement of RF noise to detect ionization. This method was not quantitative with regard to energy of the discharge and was not sensitive enough for small components such as isolation amplifiers. Now, however, manufacturers of HV test equipment have developed means to measure partial discharge, and VDE, the German standards group, has adopted use of this method for the testing of opto-couplers. To accommodate poorly defined transients, the part under test is exposed to a voltage that is 1.6 times the continuous rated voltage and must display <5pC partial discharge level in a 100% production test.

INSTALLATION AND OPERATING INSTRUCTIONS

POWER SUPPLY AND SIGNAL CONNECTIONS

As with any mixed analog and digital signal component, correct decoupling and signal routing precautions must be used to optimize performance. Figure 1 shows the proper power supply and signal connections. V_{CC} should be bypassed to Com 2 with a 0.1µF ceramic capacitor as close to the device as possible. Short leads will minimize lead inductance. A ground plane will also reduce noise problems. If a low impedance ground plane is not used, signal common lines, and either O/P High or O/P Low pin should be tied directly to the ground at the supply and Com 2 returned via a separate trace to the supply ground.

To avoid gain and isolation mode (IMR) errors introduced by the external circuit, connect grounds as indicated in Figure 3. Layout practices associated with isolation amplifiers are very important. In particular, the capacitance associated with the barrier, and series resistance in the signal and reference leads, must be minimized. Any capacitance across the barrier will increase AC leakage and, in conjunction with ground line resistance, may degrade high frequency IMR.

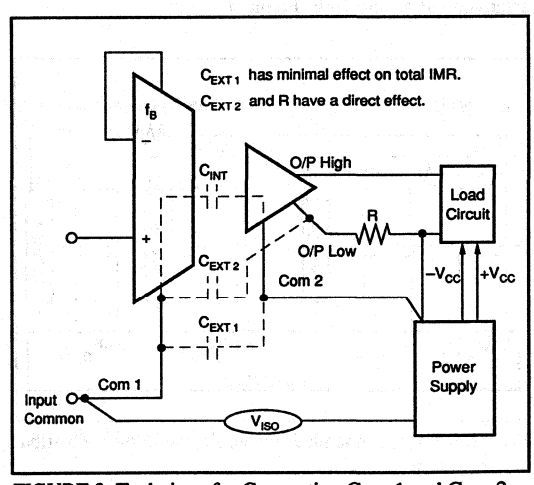


FIGURE 3. Technique for Connecting Com 1 and Com 2.

VOLTAGE GAIN MODIFICATIONS

The uncommitted operational amplifier at the input can be used to provide gain, signal inversion, active filtering or current to voltage conversion. The standard design approach for any op-amp stage can be used, provided that the full scale voltage appearing on f_B does not exceed ±5V.

If the input op-amp is overdriven, ripple at the output will result. To prevent this, the feedback resistor should have a minimum value of 10kΩ.

Also, it should be noted that the current required to drive the equivalent impedance of the feedback network is supplied by the internal DC/DC converter and must be taken into account when calculating the loading added to $\pm V_{SS\,1}$.

Since gain inversion can be incorporated in either the input or output stage of the ISO212P, it is possible to use the input amplifier in a non-inverting configuration and preserve the high impedance this configuration offers. Signal inversion at the output is easily accomplished by connecting O/P High to Com 2 instead of O/P Low.

ISOLATED POWER OUTPUT DRIVE CAPABILITY

On the input side of the ISO212P, there are two power supplies capable of delivering 5mA at ±8V to power external circuitry. When using these supplies with external loads, it is recommended that additional decoupling in the form of 10µF tantalum bead capacitors be added to improve the voltage regulation. Loss of linearity will result if additional filtering is not used with an output load. Again, power dissipated in the feedback loop around the input op amp must be subtracted from the available power output at $\pm V_{SS\,1}$.

If the ISO212P is to be used in multiple applications, care should be taken in the design of the power distribution network, especially when all ISO212Ps are synchronized. It is best to use a well decoupled distribution point and to take power to individual ISO212Ps from this point in a star arrangement as shown in Figure 4.

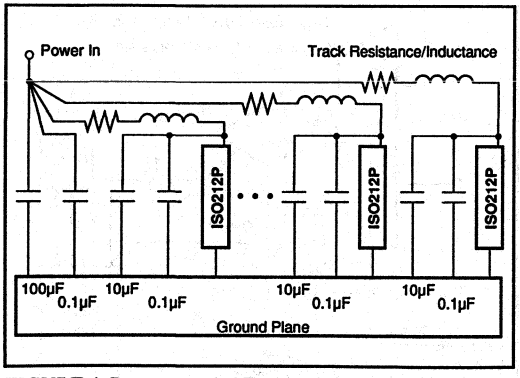


FIGURE 4. Recommended Decoupling and Power Distribution.

NOISE

Output noise is generated by residual components of the 25kHz carrier that have not been removed from the signal. This noise may be reduced by adding an output low pass filter (see Figure 8). The filter time constants should be set below the carrier frequency. The output from the ISO212P is a switched capacitor and requires a high impedance load to prevent degradation of linearity. Loads of less than 1MΩ will cause an increase in noise at the carrier frequency and will appear as ripple in the output waveform. Since the output signal power is generated from the input side of the barrier, decoupling of the $\pm V_{SS\,1}$ outputs will improve the signal to noise ratio.

SYNCHRONIZATION OF THE INTERNAL OSCILLATOR

The ISO212P has an internal oscillator and associated timing components, which can be synchronized, incorporated into the design. This alleviates the requirement for an external high-power clock driver. The typical frequency of oscillation is 50kHz. The internal clock will start when power is applied to the ISO212P and Clk In is not connected.

Because the frequencies of several ISO212Ps can be marginally different, "beat" frequencies ranging from a few Hz to a few kHz can exist in multiple amplifier applications. The design of the ISO212P accommodates "internal synchronous" noise, but a synchronous beat frequency noise will not be strongly attenuated, especially at very low frequencies if it is introduced via the power, signal, or potential grounding paths. To overcome this problem in systems where several ISO212Ps are used, the design allows synchroniztion of each oscillator in a system to one frequency. Do this by forcing the timing node on the internal oscillator with an external driver connected to Clk In. See Figure 5. The driver may be an external component with Series 4000 CMOS characteristics, or one of the ISO212Ps in the system can be used as the master clock for the system. See Figure 6 and 7 for connections in multiple ISO212P installations.

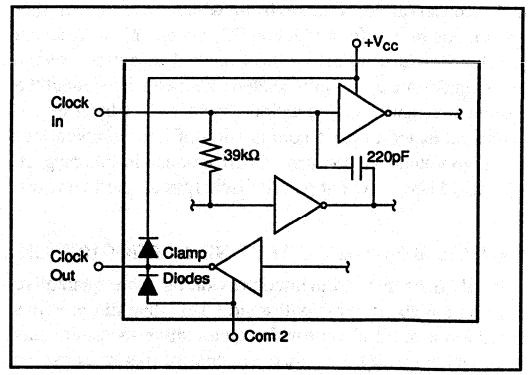


FIGURE 5. Equivalent Circuit, Clock Input/Output. Inverters are CMOS.

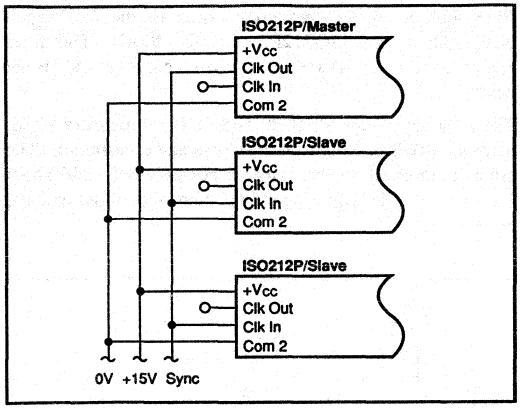


FIGURE 6. Oscillator Connections for Synchronous Operation in Multiple ISO212P Installations.

CHARGE ISOLATION

When more than one ISO212P is used in synchronous mode, the charge which is returned from the timing capacitor (220pF in Figure 5) on each transition of the clock becomes significant. Figure 7 illustrates a method of isolating the "Clk Out" clamp diodes (Figure 5) from this charge.

A 22kΩ resistor (recommended maximum to use) together with the 39kΩ internal oscillator timing resistor (Figure 5) forms a potential divider. The ratio of these resistors should be greater than 0.6 which ensures that the input voltage triggers the inverter connected to "Clk In". If using a single resistor, then account must be taken of the paralleled timing resistors. This means that the 22kΩ resistor must be halved to drive two ISO212Ps, or divided by 8 if driving 8 ISO212Ps to insure that the ratio of greater than 0.6 is maintained. The series resistors shown in Figure 7 reduce the high frequency content of the power supply current.

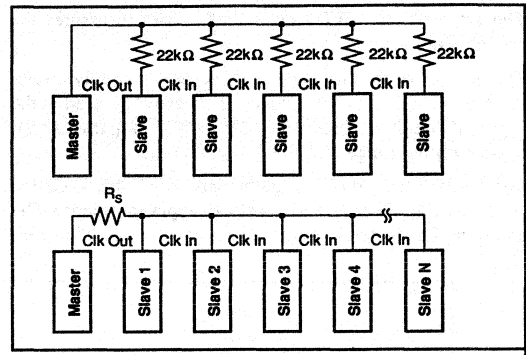


FIGURE 7. Isolating the Clk Out Node.

APPLICATIONS

The ISO212P isolation amplifier, together with a few low cost components, can isolate and accurately convert a 4-to-20mA input to a ±10V output with no external adjustment. Its low height (0.43" (11mm)) and small footprint (2.5" x 0.33" (57mm x 8mm)) make it the solution of choice in 0.5" board spacing systems and in all applications where board area savings are critical.

The ISO212P operates from a single +15V supply and offers low power consumption and 12-bit accuracy. On the input side, two isolated power supplies capable of supplying 5mA at ±8V are available to power external circuitry.

APPLICATIONS FLEXIBILITY

In Figure 8, the ISO212P's $+V_{ss\,1}$ isolated supply powers a REF200 to provide an accurate 100µA current source. This current is opposed by an equal but opposite current through the 75kΩ feedback resistor to establish an offset of –7.5V at I_{in} = 0mA. With I_{in} = 4-to-20mA, the output is –5 to +5V.

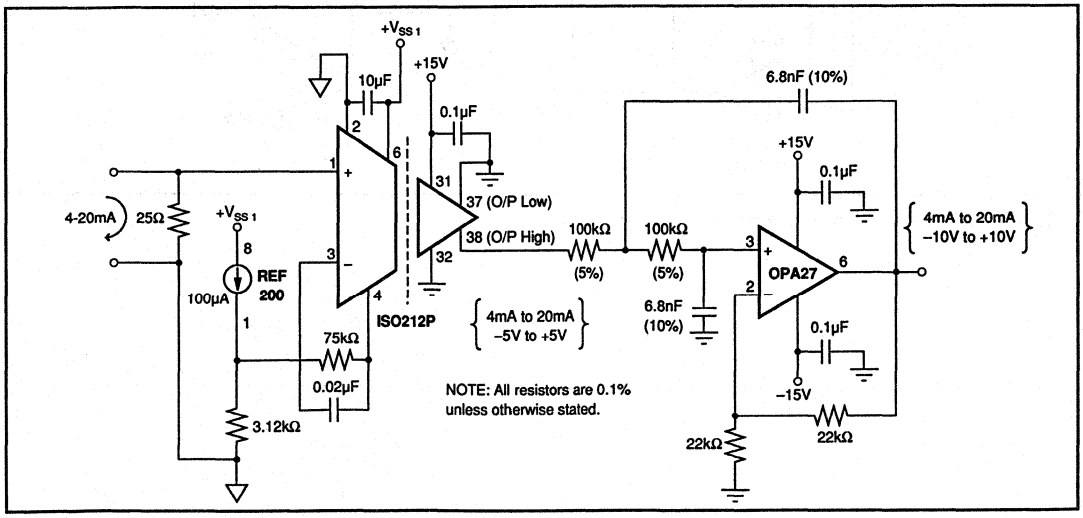


FIGURE 8. Isolated 4-20mA Current Receiver with Output Filter.

The ratio of the 75kΩ and 3.12kΩ resistors assures the correct gain.

The polarity of the output can be reversed by simply reversing the O/P HI and O/P LO pins. This could be used in the Figure 8 circuit to change the –5V to +5V output to a +5V to –5V output range.

The primary function of the output circuitry is to add gain to produce a ±10V output and to reduce output impedance. The addition of a few resistors and capacitors provides a low pass filter with a cut-off frequency equal to the full signal bandwidth of the ISO212P, typically 200Hz. The filter response is flat to 1dB and rolls off from cut off at –12dB per octave.

The accuracy of the REF200 and external resistors eliminates the need for expensive trim pots and adjustments. The errors introduced by the external circuitry only add about 10% of the ISO212P's specified gain and offset voltage error.

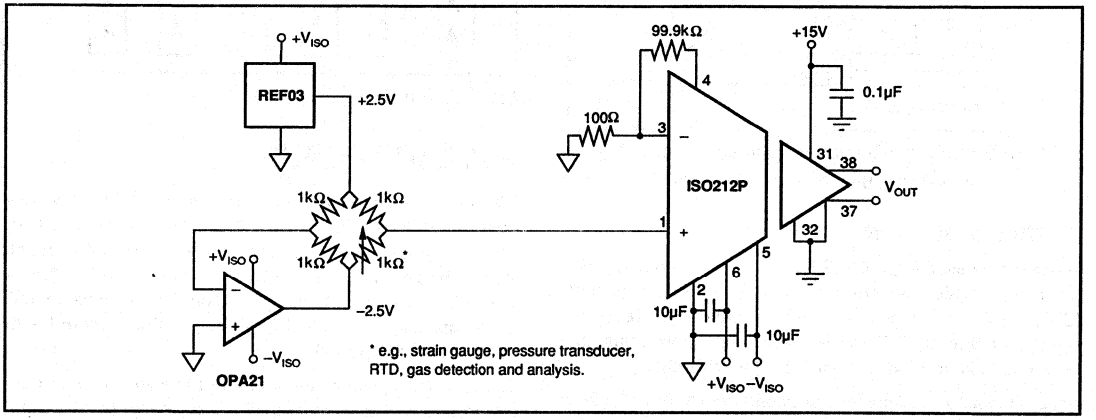


FIGURE 9. Instrument Bridge Isolation Amplifier.

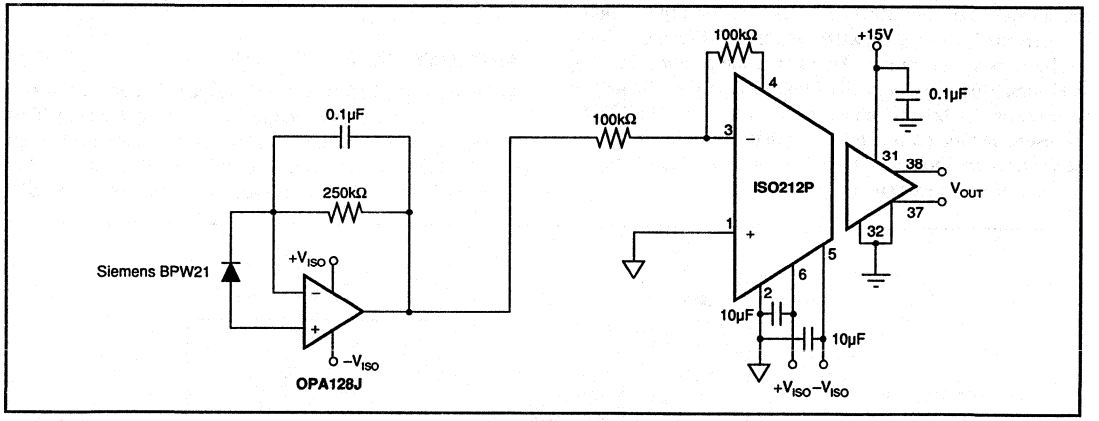


FIGURE 10. Photodiode Isolation Amplifier.

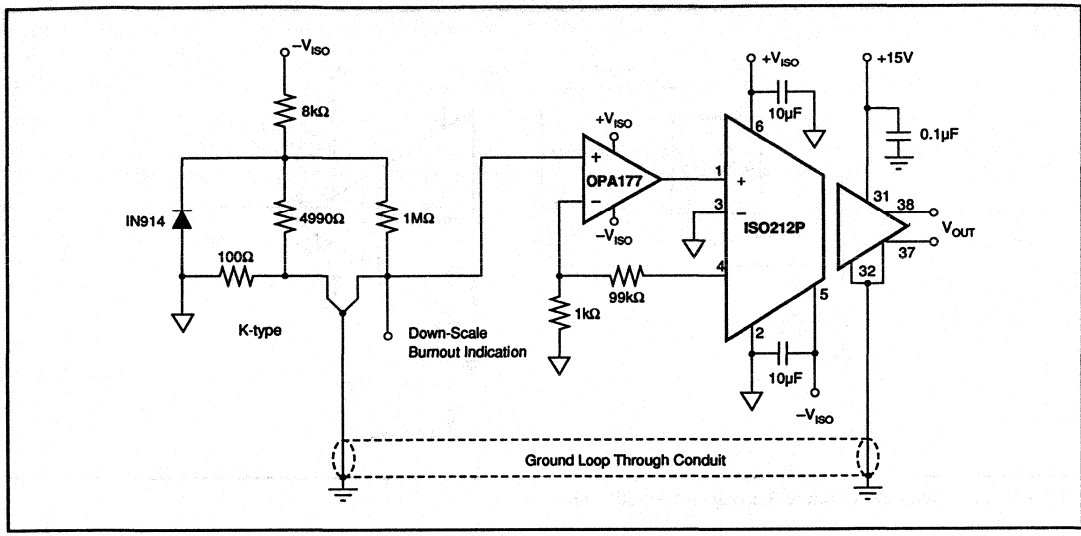


FIGURE 11. Thermocouple Amplifier with Ground Loop Elimination, Cold Junction Compensation and Down-Scale Burn-Out.

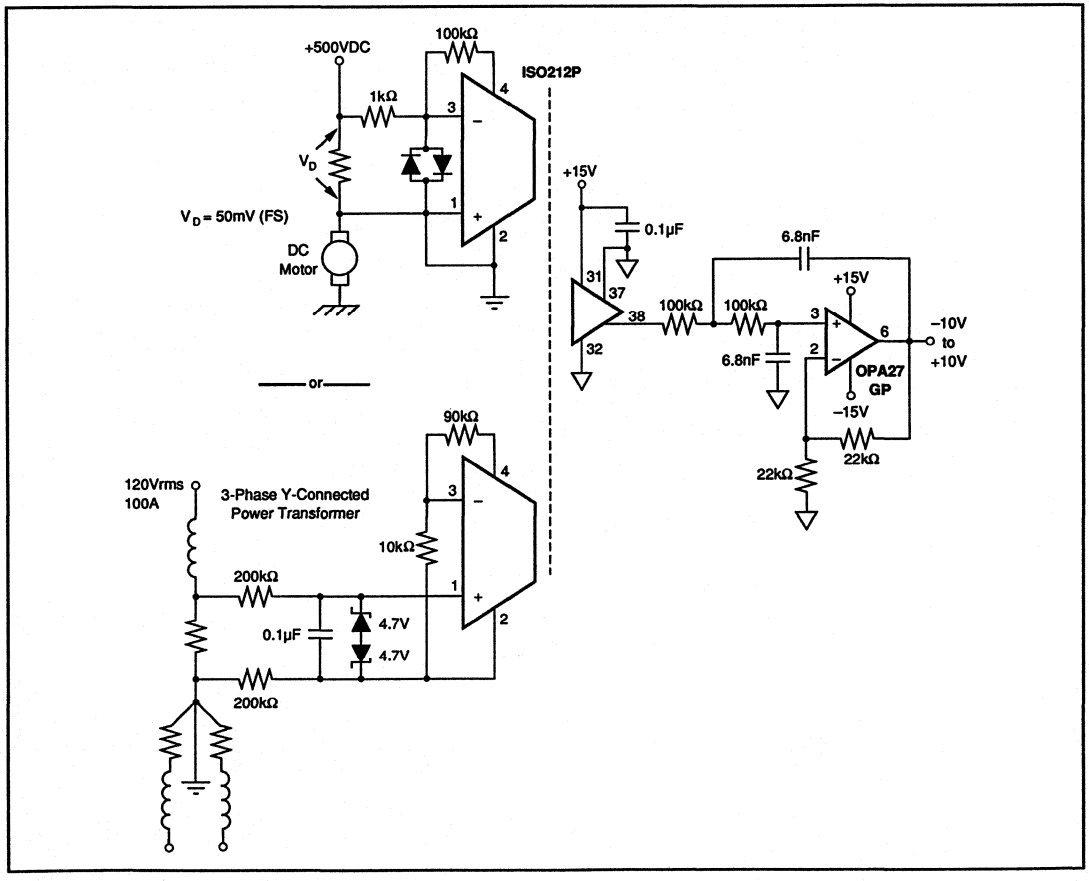


FIGURE 12. Isolated Current Monitoring Applications.

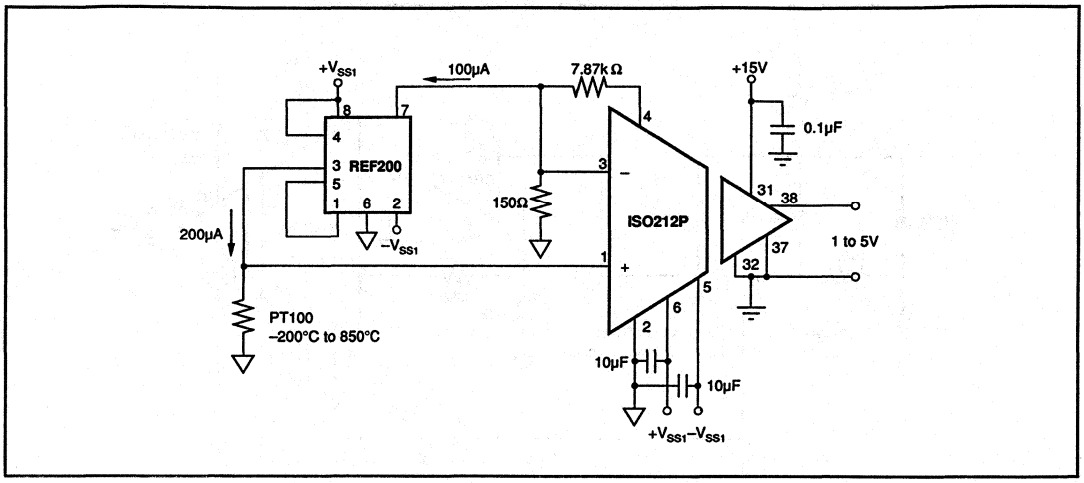


FIGURE 13. Isolated Temperature Sensing and Amplification.

BURR-BROWN®

IXR100

ADVANCED INFORMATION
SUBJECT TO CHANGE

Isolated, Self-Powered, Temperature Sensor Conditioning 4-20mA TWO-WIRE TRANSMITTER

FEATURES

- 1500Vrms ISOLATION
- TRUE TWO-WIRE OPERATION : Power and Signal on One Wire Pair
- RESISTANCE OR VOLTAGE INPUT
- DUAL MATCHED CURRENT SOURCES: 400μA at 7V
- WIDE SUPPLY RANGE 12V TO 36V
- PT100 RTD LINEARIZATION

APPLICATIONS

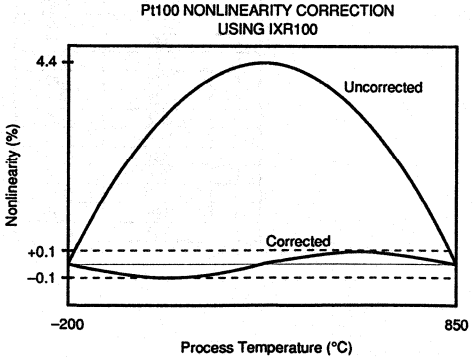
- INDUSTRIAL PROCESS CONTROL:
  All Types of Isolated Transmitters;
  Pt100 RTD
  Thermocouple Inputs
  Current Shunt (mV) Inputs
- ISOLATED DUAL CURRENT SOURCES
- AUTOMATED MANUFACTURING
- POWER PLANT/ENERGY MONITORING
- GROUND LOOP ELIMINATION

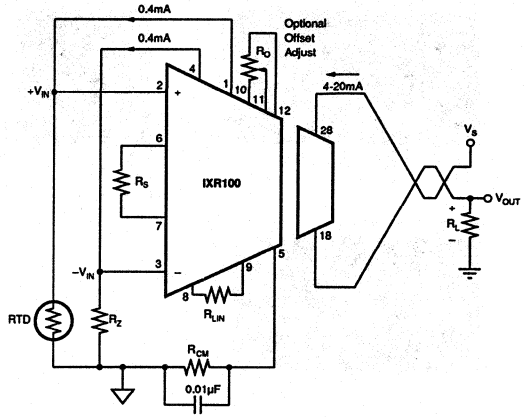
DESCRIPTION

The IXR100 is an isolated 2-wire transmitter featuring loop powered operation and resistive temperature sensor conditioning (excitation and linearization). It contains a DC/DC convertor, high accuracy instrumentation amplifier with single resistor programmable span and linearization, and dual matched excitation current sources. This combination is ideally suited to a range of transducers such as thermocouples, RTDs, thermistors and strain gages. The small size makes it ideal for use in head mounted isolated temperature transmitters as well as rack and rail mounted equipment.

The isolated two-wire transmitter allows signal transmission and device power to be supplied on a single wire-pair by modulating the power supply current with the isolated signal source. The transmitter is resistant to voltage drops from long runs and noise from motors, relays, actuators, switches, transformers and industrial equipment.

It can be used by OEMs producing isolated transmitter modules or by data acquisition system manufacturers. The IXR100 is also useful for general purpose isolated current transmission where the elimination of ground loops is important.





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Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

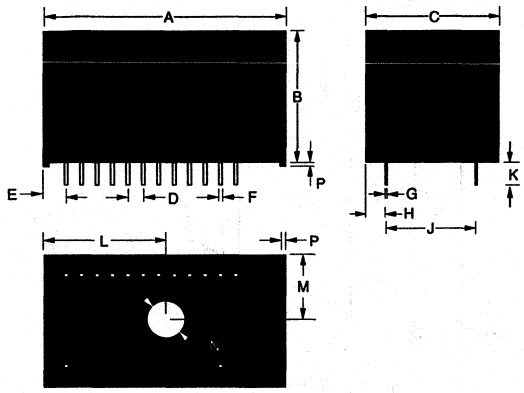
ELECTRICAL

V_S = +24V, T_A = +25°C, unless otherwise noted.

PARAMETER	CONDITIONS	IXR100 MIN	IXR100 TYP	IXR100 MAX	UNITS
OUTPUT AND LOAD CHARACTERISTICS					
Output Current	Linear Operating Region	4		20	mA
Output Current Limit			32		mA
Loop Supply Voltage		11.6		36	VDC
Load Resistance		$R_{LOAD} = (V_S - 11.6)/I_O$			Ω
ZERO					
Initial Error (1)	V_{IN} = 0, R_S = ∞			300	µA
vs Temperature				200	ppm/°C
SPAN					
Output Current Equation	R_S in Ω, V_{IN} in V		$I_O = 4mA + [0.016 + (40/R_S)] (V_{IN})$		
Span Equation			$S = [0.016 + (40/R_S)]$		A/V
Untrimmed Error	(1)	–2.5		0	%
vs Temperature	Excluding TCR of R_S		50	100	ppm/°C
Nonlinearity : EMF Input	(2)		0.01	0.025	%FSR
: Pt100 Input	(3)		0.1		%FSR
INPUT					
Voltage Range	R_S = ∞		1		V
Common-Mode Range	V_{IN+}, V_{IN-} with Respect to COM	2		4	V
Offset Voltage			150	500	µV
vs Temperature			3	5	µV/°C
vs Supply			100		dB
CURRENT SOURCES					
Magnitude			0.4		mA
Accuracy				1	%
vs Temperature			50	100	ppm/°C
Match				0.5	%
vs Temperature			25	50	ppm/°C
DYNAMIC RESPONSE					
Settling Time	To 0.1% of Span		500		ms
TEMPERATURE RANGE					
Operating		–20		+70	°C
Storage		–40		+85	°C
ISOLATION					
Isolation Voltage	V_{ISO}	1500			Vrms

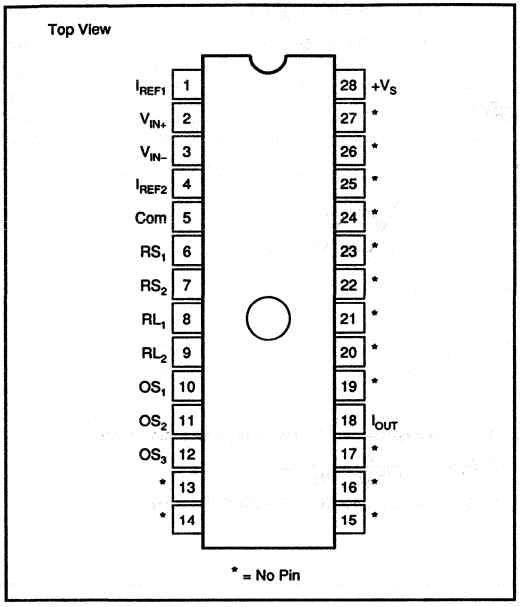
NOTES: (1) Can be adjusted to zero. (2) End point span non-linearity. (3) End point, corrected span non-linearity with a Pt100 RTD input operated from –200°C to +850°C.

MECHANICAL



DIM	MILLIMETERS TYP	INCHES TYP
A	40.00	1.58
B	22.00	0.87
C	22.60	0.89
D	2.54	0.10
E	3.49	0.14
F	0.58	.023
G	0.25	.011
H	3.38	0.13
J	15.24	0.60
K	3.81	0.15
L	20.00	0.79
M	11.30	0.44
N	6.00	0.24
P	0.60	0.024

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Power Supply ($+V_S$ $-I_{OUT}$)	40V
Input Voltage (Com to V_{IN})	9V
Storage Temperature Range	–40°C to +85°C
Lead Temperature (soldering 10s)	+300°C
Output Current Limit Duration	Continuous
Power Dissipation	500mW

ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that this integrated circuit be handled and stored using appropriate ESD protection methods.

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

DISCUSSION OF PERFORMANCE

The IXR100 makes the design of isolated two wire 4 to 20mA transmitters easy and provides exceptional performance at very low cost. It combines several unique features not previously available in a single package. These include galvanic isolation, sensor excitation and linearization, excellent DC performance, and low zero and span drift. The IXR100 functions with voltages as low as 11.6V at the device. This allows operation with power supplies at or below 15V. When used with the RCV420 the complete 4 to 20mA current loop requires only 13.1V. If series diode protection is desired the minimum loop supply voltage is still only about 13.7V. This is especially useful in systems where the available supplies are only 15V.

BASIC CONNECTION

The basic connection of the IXR100 is shown in Figure 1. A differential voltage applied between pins 2 and 3 will cause a current of 4 to 20mA to circulate in the two wire output loop pins 28 and 18. Pins 1 and 4 supply the current excitation for resistive sensors. Pins 6 and 7 are provided for the connection of an external span resistor which increases the gain. Pins 8 and 9 provide linearity correction. Pins 10, 11 and 12 adjust the output offset current.

FUNCTIONAL DESCRIPTION

The IXR100 comprises of several functions:

- Sensor excitation
- Internal voltage regulator
- Input amplifier and V/I converter
- Linearization circuit
- DC/DC Converter

SENSOR EXCITATION

Sensor Excitation consists of two matched 0.4mA current sources. One is used to excite the resistive sensor and the other is used to excite the zero balance resistor R_Z. When the linearity correction feature is used these current sources are modulated together so that three wire operation of a Pt100 RTD is possible.

INTERNAL VOLTAGE REGULATOR

The circuitry within the IXR100 regulates the supply voltage to the DC/DC Converter, Input Amplifier, Linearization Amplifier and V/I Converter and removes the normal variations in V_S from these stages as the output spans from 4 to 20mA.

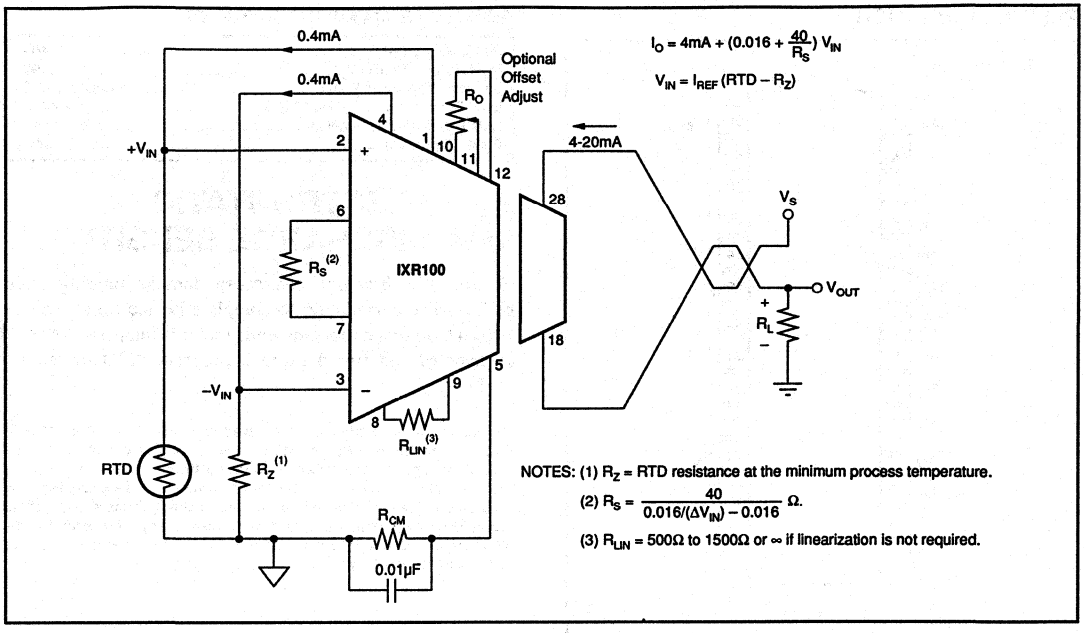


FIGURE 1. Basic Connection for RTD.

INPUT AMPLIFIER AND V/I CONVERTER

The Input Amplifier is an instrumentation amplifier whose gain is set by R_S, it drives the V/I Converter to produce a 4 to 20mA output current. The Input Amplifier has a common mode voltage range of 2 to 4V with respect to COM (pin 5). Normally this requirement is satisfied by returning the currents from the RTD and zero balance resistor R_Z to COM through a common mode resistor R_{CM}. For most applications a single value of 3.9kΩ may be used. When used with RTDs having large values of resistance R_{CM} must be chosen so that the inputs of the amplifier remain within its rated common mode range. R_{CM} should be bypassed with a 0.01µF or larger capacitor.

LINEARIZATION CIRCUIT

The Linearity Correction Circuit is unique in several ways. A single external resistor will provide up to 50 times improvement in the basic RTD linearity. Terminal based non-linearity can be reduced to less than ±0.1% for all RTD temperature spans. The Linearization circuit also contains an instrumentation amplifier internally connected to the $\pm V_{IN}$ pins. The gain of this stage is set by R_{LIN}. The output controls the excitation current sources to produce an increasing excitation current as V_{IN} increases. An important feature is that the Linearity Correction is made directly to the RTD output independent of the gain of the Input Amplifier. This provides minimal interaction between R_S and R_Z. This feature can be useful at the systems level by reducing data acquisition system processor overhead previously used to linearize sensor response in software/firmware.

DC/DC CONVERTER

The DC/DC Converter transfers power from the 2 wire current loop across the barrier to the circuitry used on the input side of the isolation barrier.

PIN DESCRIPTIONS

I_{REF1}, I_{REF2}

These pins provide a matched pair of current sources for sensor excitation. These current sources provide excellent thermal tracking, and when the linearization feature is used, are modulated by an equal amount. Their nominal current value is 0.4mA and their compliance voltage is:

$$V_{IN}+ < V_{IREF} < (Com + 7V)$$

+V_{IN}, –V_{IN}

These are the inputs to both the input amplifier and the linearization amplifier. Because the IXR100 has been optimized for RTD applications, the two sets of inputs are internally connected.

R_{S1}, R_{S2}

The resistor connected across these terminals determines the gain of the IXR100. For normal 4-20mA outputs:

$$R_S = \frac{40}{0.016/(\Delta V_{IN}) - 0.016}\ \Omega \qquad —(1)$$

R_{L1}, R_{L2}

The resistor connected between these terminals determines the gain of the linearization circuit and the amount of correction applied to the RTD. Its value may be determined in several ways. Two of which are shown as follows.

1. Empirically by interactively adjusting R_{LIN}, R_S and R_Z to achieve best fit 4 to 20mA output. R_Z is used to set 4mA at minimum input, R_S is adjusted for 12mA with a half span input, and R_{LIN} is adjusted to give 20mA with a full span input. This may require a few iterations but is probably the most practical method for field calibration. R_{LIN} will range between 500Ω and 1500Ω for 100Ω sensors (Pt100, D100, SAMA). Initially it may seem a little strange adjusting R_S for 12mA and R_{LIN} for 20mA. However, convergence is achieved much more quickly as the linearized curve passes through zero and has less effect at the mid span and the linearity trim resistor tends to adjust the transfer function more at the full span than the mid point.
2. Using Table I and linear interpolation for values of span not given in the table. This will yield very accurate results for the Pt100 sensor and acceptable results for D100 and SAMA sensors.

ZERO ADJUST (OPTIONAL) O_{S1}, O_{S2}, O_{S3}

The IXR100 has provision for adjusting the output offset current as shown in Figure 2. In many applications the already low offset will not need to be known at all. This trim effects the V/I converter stage and does not introduce V_{OS} drift errors that occur when the trim is performed at the input stage. If possible use R_Z to trim sensor output error to zero and use the offset control to trim the output to 4mA when V_{IN} = 0V. The offset adjustment can be made with a

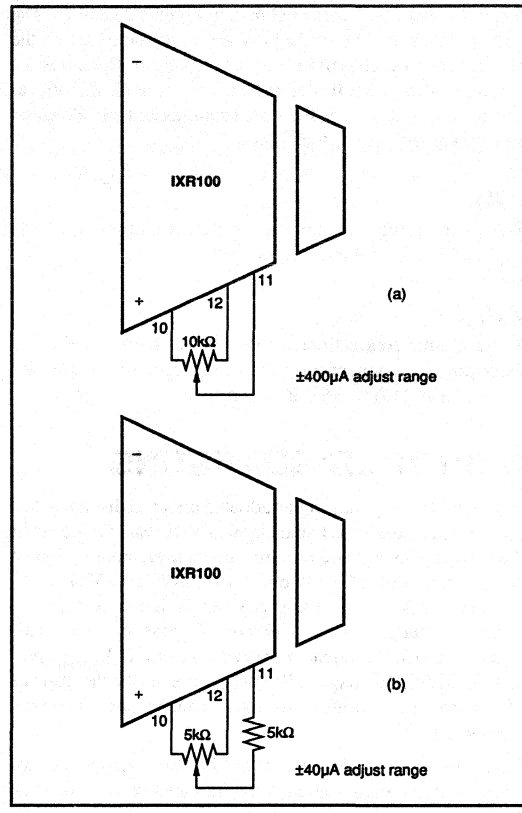


FIGURE 2. Basic Connection for Zero Adjust.

SPAN ΔT (°C)

T_{MIN} (°C)	50	100	200	300	400	500	600	700	800	900	1000
–200	573	653	839	995	1083	1131	1152	1159	1159	1154	1140
–150	745	855	1059	1158	1197	1206	1205	1196	1175	1151	1127
–100	983	1105	1228	1251	1249	1231	1207	1182	1156	1129	
–50	1233	1284	1286	1262	1236	1208	1180	1152	1125	1097	
0	1302	1287	1273	1229	1201	1173	1145	1117	1089		
50	1263	1249	1220	1192	1164	1136	1108	1081	1054		
100	1225	1211	1183	1155	1127	1100	1073	1046			
150	1188	1174	1146	1119	1091	1064	1038	1011			
200	1151	1137	1110	1083	1056	1030	1003				
250	1114	1101	1074	1048	1021	995	969				
300	1079	1066	1039	1013	987	962					
350	1044	1031	1005	979	954	928					
400	1009	996	971	946	921						
450	975	963	938	913	888						
500	942	930	905	881							
550	909	897	873	849							
600	877	865	841								
650	845	834	810								
700	814	803									
750	784	773									
800	754										

NOTES: (1) Linear interpolation between two horizontal or vertical values yields acceptable values. (2) Although not optimum, these values will also yield acceptable results with D100 and SAMA 100Ω nominal sensors. (3) Double R_{LIN} value for PT200.

TABLE I. R_{LIN} Values for Pt100 Sensor.

potentiometer connected as shown in Figures 2a and 2b. The circuit shown in Figure 2a provides more range while the circuit in Figure 2b provides better resolution. Note, it is not recommended to use this adjusting procedure for zero elevation or suppression. See the signal suppression and elevation section for the proper techniques.

COM

This is the return for the two excitation currents I_{REF1} and I_{REF2} and is the reference point for the inputs.

V_S, I_{OUT}

These are the connections for the current loop V_S being the most positive connection. For correct operation these pins should have 11.6 to 36V between them.

HIGH VOLTAGE TESTING

Burr-Brown Corporation has adopted a partial discharge test criterion that conforms to the German VDE0884 Optocoupler Standards. This method requires the measurement of minute current pulses (<5pC) while applying 2400rms, 60Hz high-voltage stress across every devices isolation barrier. No partial discharge may be initiated to pass this test. This criterion confirms transient overvoltage (1.6 X V_{RATED}) protection without damage. Life-test results verify the absence of failure under continuous rated voltage and maximum temperature.

This new test method represents the "state-of-the-art" for nondestructive high voltage reliability testing. It is based on the effects of non-uniform fields existing in heterogeneous dielectric material during barrier degradation. In the case of void non-uniformities, electric field stress begins to ionize the void region before bridging the entire high voltage barrier.

The transient conduction of charge during and after the ionization can be detected externally as a burst of 0.01µs-0.1µs current pulses that repeat on each AC voltage cycle. The minimum AC barrier voltage that initiates partial discharge is defined as the "inception voltage". Decreasing the barrier voltage to a lower level is required before partial discharge ceases and is defined as the "extinction voltage".

We have designed and characterized the package to yield an inception voltage in excess of 2400Vrms so that transient overvoltages below this level will not cause any damage. The extinction voltage is above 1500Vrms so that even overvoltage-induced partial discharge will cease once the barrier voltage is reduced to the rated level. Older high voltage test methods relied on applying a large enough overvoltage (above rating) to catastrophically break down marginal parts, but not so high as to damage good ones. Our new partial discharge testing gives us more confidence in barrier reliability than breakdown/no breakdown criteria.

APPLYING THE IXR100

The IXR100 has been designed primarily to correct nonlinearities inherent in RTD sensors. It may also be used in other applications where its excellent performance makes it superior to other devices available. Examples are shown in the Applications Section.

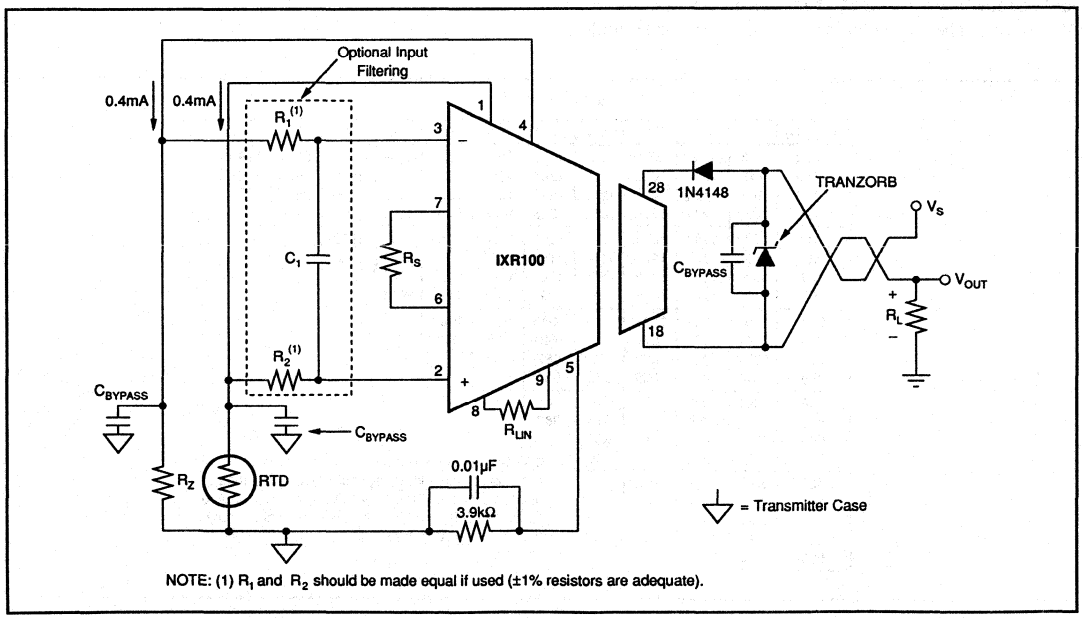


FIGURE 3. Transient and RFI Protection Circuit.

RFI AND TRANSIENT SUPPRESSION

Radio frequency interference and transients are a common occurrence in 4-20mA loops, especially when long wiring lengths are involved. RFI usually appears as a temporary change in output and results from rectification of the radio signal by one or more stages in the amplifier. For sensors which are closely coupled to the IXR100 and are contained in a common metal housing, the usual entry for RFI is via the 4-20mA loop wiring. Coaxial bypass capacitors may be used with great effectiveness to bring these leads into the transducer housing while suppressing the RFI. Values of 100 to 1000pF are generally recommended. For sensors remote from the IXR100, coaxial capacitors can also be used to filter the excitation and signal leads. Additional low-pass filtering at the IXR100 input helps suppress RFI. The easiest way to do this is with the optional differential RC filter shown in Figure 4. Typical values for R_1 and R_2 are 100-1000Ω, and for C_1 are 100-1000pF.

Transient suppression for negative voltages can be provided by the reverse-polarity protection diodes discussed later. However, positive transients cannot be handled by these diodes and do frequently occur in field-mounted loops. A shunt zener diode is of some help, but most zener diodes suffer from limited current-handling capacity and slow turn-on. Both of these characteristics can lead to device failure before the zener conducts. One type of zener, called the TRANZORB and available from General Semiconductor Industries, is especially effective in protecting against high-energy transients such as those induced by lightning or motor contactors. Choose a TRANZORB with a voltage rating close to, but exceeding, the maximum V_S which the IXR100 will see. In combination, the coaxial bypass capacitors and TRANZORB provide a very high level of protection against transients and RFI.

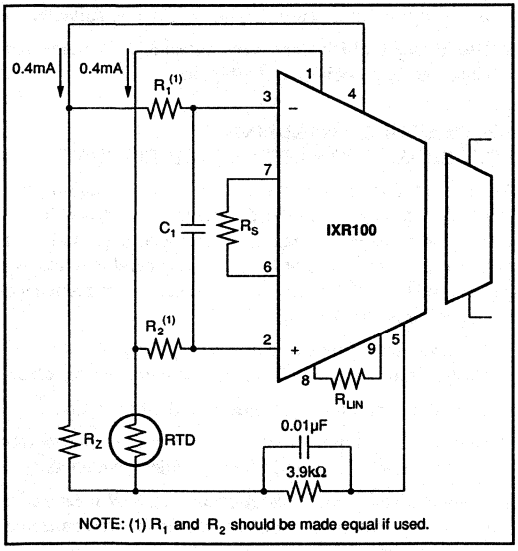


Figure 4. Optional Bandwidth-Limiting Circuitry.

INPUT BANDWIDTH LIMITING

Filtering at the input to the IXR100 is recommended where possible and can be done as shown in Figure 4. C_1 connected to pins 3 and 4 will reduce the bandwidth with a f_{-3dB} frequency given by:

$$f_{-3dB} = 0.159/(R_1 + R_2 + RTD + R_Z)\ (C_1 + 3pF)$$

This method has the disadvantage of having f_{-3dB} vary with R_1, R_2, RTD, and R_Z may require large values of R_1, and R_2. R_1 and R_2 should be matched to prevent zero errors due to input bias current.

SIGNAL SUPPRESSION AND ELEVATION

In some applications it is desired to have suppressed zero range (span elevation) or elevated zero range (span suppression). This is easily accomplished with the IXR100 by using the current sources to create the suppression/elevation voltage. The basic concept is shown in Figure 5. In this example the sensor voltage is derived from RT (a thermistor, RTD or other variable resistance element) excited by one of the 0.4mA current sources. The other current source is used to create the elevated zero range voltage. Figures 6a, 6b, 6c and 6d show some of the possible circuit variations. These circuits have the desirable feature of noninteractive span and suppression/elevation adjustments.

NOTE: Use of the optional offset null (pins 10, 11, and 12) for elevation or suppression is not recommended. This trim technique is used only to trim the IXR100's output offset current.

MAJOR POINTS TO CONSIDER WHEN USING THE IXR100

1. The leads to R_S and R_{LIN} should be kept as short as possible to reduce noise pick-up and parasitic resistance. If the linearity correction feature is not desired, the R_{LIN} pins are left open.
2. $+V_S$ should be bypassed with a 0.01µF capacitor as close to the unit as possible (pins 18 to 28).
3. Always keep the input voltages within their range of linear operation, +2V to +4V ($\pm V_{IN}$ measured with respect to pin 5).

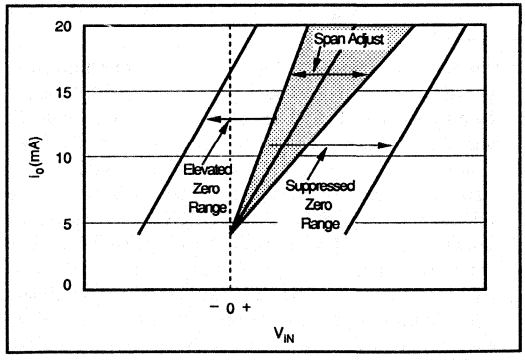


Figure 5. Elevation and Suppression Graph.

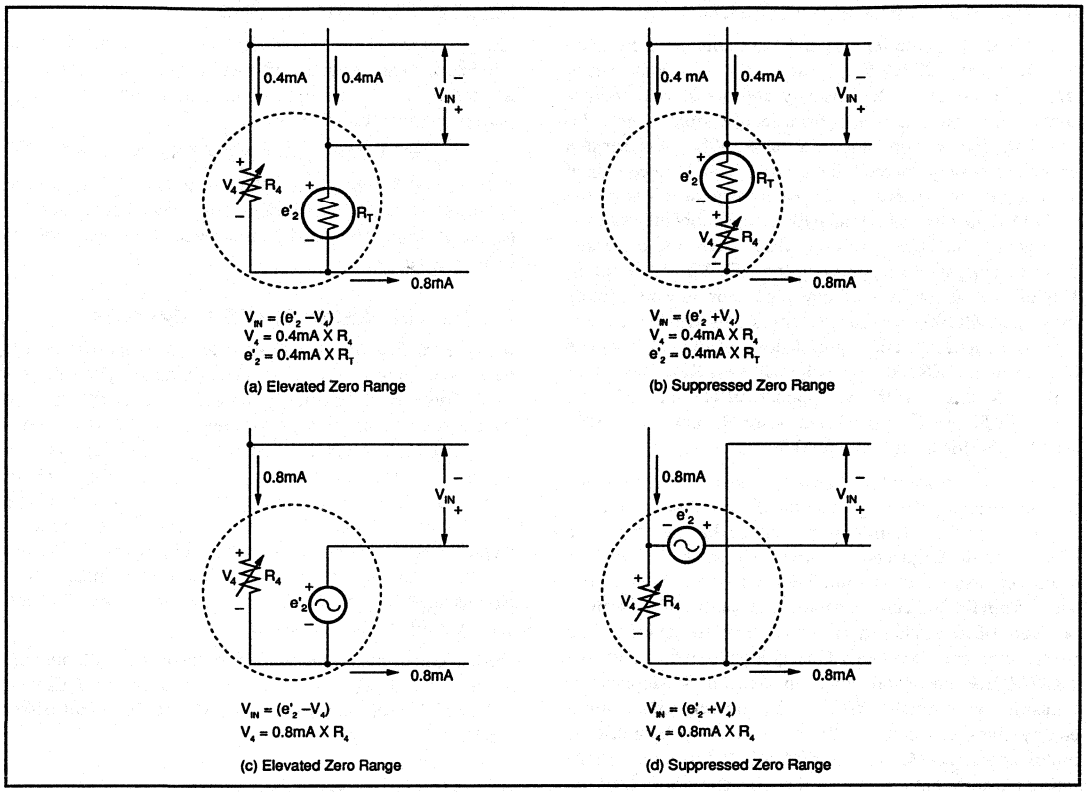


FIGURE 6. Elevation and Suppression Circuits.

4. The maximum input signal level (ΔV_{IN}) is 1V with R_S open and is less as R_S decreases in value.
5. Always return the current references to COM (pin 5) through an appropriate value of R_{CM} to keep V_{CM} within its operating range. Also, operate the current sources within their rated compliance voltage:

$$V_{IN} + \leq V_{IREF} \leq (Com + 7V)$$

6. Always choose R_L, (including line resistance) so that the voltage between pins 18 and 28 ($+V_S$) remains within the 11.6V to 36V range as the output changes between 4mA and 20mA.
7. It is recommended that a reverse polarity protection diode be used. This will prevent damage to the IXR100 caused by a transient or long-term reverse bias between pins 18 and 28. This diode can be connected in either of the two positions shown in Figure 7, but each connection has its trade-off. The series-connected diode will add to the minimum voltage at which the IXR100 will operate but offers loop and device protection against both reverse connections and transients. The reverse-biased diode in parallel with the IXR100 preserves 11.6V minimum operation and offers device protection, but could allow excessive current flow in the receiving instrument if the field leads are accidently reversed. This is particularly important if the receiving equipment has particularly low resistance or uses higher voltage supplies. In general, the series diode is recommended unless 12V operation is necessary. In either case a 1N4148 diode is suitable.
8. Use a layout which minimizes parasitic inductance and capacitance, especially in high gain.

RECOMMENDED HANDLING PROCEDURES FOR INTEGRATED CIRCUITS

All semiconductor devices are vulnerable, in varying degrees, to damage from the discharge of electrostatic energy. Such damage can cause performance degradation or failure, either immediate or latent. As a general practice, we recommend the following handling procedures to reduce the risk of electrostatic damage.

1. Remove static-generating materials, such as untreated plastic, from all areas where microcircuits are handled.
2. Ground all operators, equipment, and work stations.
3. Transport and ship microcircuits, or products incorporating microcircuits, in static-free, shielded containers.
4. Connect together all leads of each device by means of a conductive material, when the device is not connected into a circuit.

5. Control relative humidity to as high a value as practical (50% recommended).

RTD APPLICATIONS

The IXR100 has been designed with RTD applications specifically in mind. The following information provides additional information for those applications.

TWO- AND THREE-WIRE CONNECTIONS

The IXR100 performs well with two-wire and three-wire RTD connections commonly encountered in industrial monitoring and control.

In two-wire applications, the voltage drop between the RTD and the IXR100 can be nulled by proper adjustment of R_Z, but care must be taken that this voltage drop does not vary with ambient conditions. Such variation will appear as an apparent variation in the RTD resistance and therefore as a change in measured temperature. Also, the linearity correction will interpret this change as a variation and attempt to linearize both the actual RTD signal and the resistance changes in the signal lines. For these reasons, the line resistance between the RTD and the IXR100 should be minimized by keeping line lengths short and/or using large-gauge wires. This limitation does not apply for three-wire connections.

In three-wire applications, shown in Figure 7, the RTD and R_Z lead arrangements set up a pseudo-Kelvin connection to the RTD. This occurs because the currents through the three wires are set up in opposing directions and cancel IR drops in the RTD leads. The current sources are both modulated equally, so that use of the linearity correction does not affect the cancellation. This action is true so long as the three wires are of the same length and gauge. Because most RTD leads are twisted and bundled, this requirement is usually met with no difficulty. Care must be taken that intermediate connections such as screw terminals do not violate this assumption by introducing unequal line resistances.

RTD ZERO ELEVATION AND SUPPRESSION

The IXR100 may be operated in zero-elevated and zero-suppressed ranges by simply offsetting R_Z. It may also be used in increase-decrease applications by interchanging the physical locations of the RTD and R_Z as shown in Figure 8. Use the same values of R_Z, R_{LIN} and R_S. Again, because the current sources are matched and are modulated equally, this connection has no effect on IXR100 performance, especially in three-wire applications.

OPEN CIRCUIT DETECTION

In some applications of the IXR100, the RTD will be located remotely. In these cases, it is possible for open circuits to develop. The IXR100 responds in the following manner to breaks in each lead. The following connections refer to the RTD connections shown in Figure 7.

TERMINAL OPEN	I_{OUT}*
1	32mA
2	3.6mA
3	32mA

*approximate value

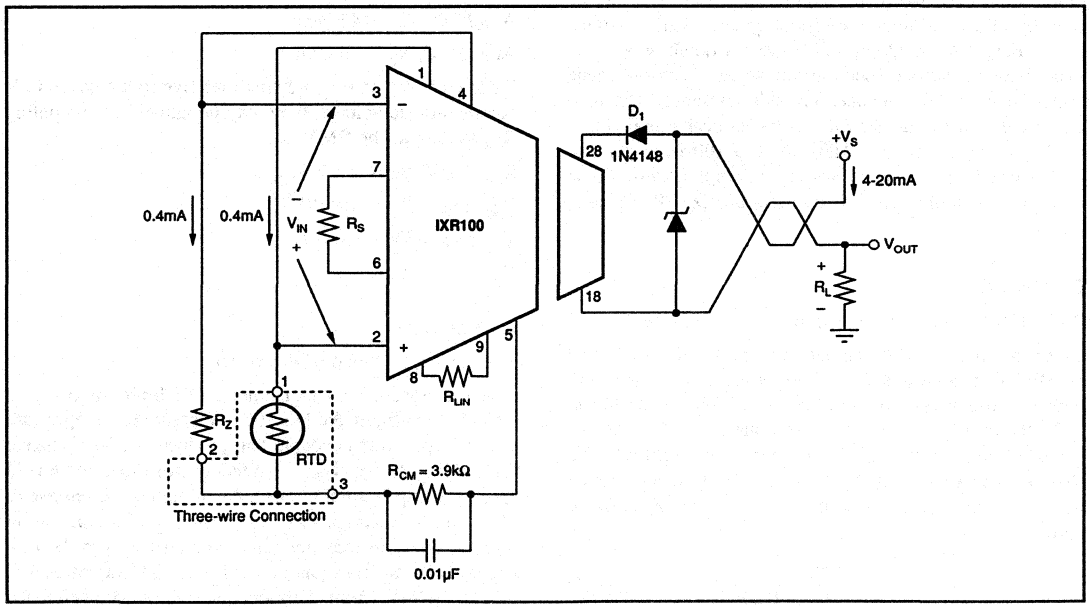


FIGURE 7. Basic 3-Wire RTD Connection for Increase-Increase Action.

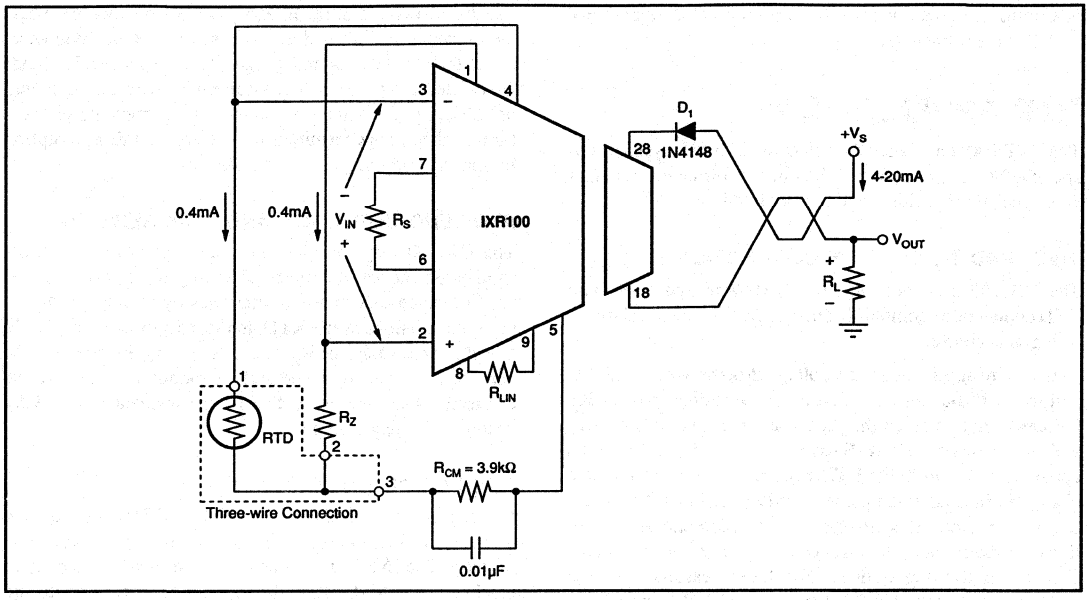


FIGURE 8. Basic 3-Wire RTD Connection for Increase-Decrease Action.

OTHER APPLICATIONS

In instances where the linearization capability of the IXR100 is not required, it can still provide improved performance in several applications. Its small size, wide compliance voltage, low zero and span drift, high PSRR, high CMRR and excellent linearity makes the IXR100 ideal for a variety of other isolated two-wire transmitter applications. It can be used by OEMs producing different types of isolated transducer transmitter modules and by data acquisition systems manufacturers who gather transducer data. Current mode transmission greatly reduces noise interference. The two-wire nature of the device allows economical signal conditioning at the transducer. Thus, the IXR100 is, in general, very suitable for a wide variety of applications. Some examples, including an isolated non-linearized Pt100 case, follow.

EXAMPLE 1

Pt100 RTD without linearization shown in Figure 9.

Given a process with temperature limits of +25°C and +150°C, configure the IXR100 to measure the temperature with a Pt100 RTD which produces 109.73Ω at 25°C and 157.31Ω at 150°C (obtained from standard RTD tables). Transmit 4mA for +25°C and 20mA for +150°C. The change in resistance of the RTD is 47.6Ω. When excited with a 0.4mA current source ΔV_{IN} is 0.4mA X 47.6Ω = 19mV.

$$R_S = \frac{40}{0.016/(\Delta V_{IN}) - 0.016}\ \Omega \qquad -(1)$$

From Equation (1), R_S = 48.5Ω. Span adjustment (calibration) is accomplished by trimming R_S.

In order to make the lower range limit of 25°C correspond to the output lower range limit at 4mA, the input circuitry shown in Figure 9 is used. V_{IN} must be 0V at 25°C and R_Z is chosen to be equal to the RTD resistance at 25°C, or 109.73Ω. Computing R_{CM} and checking CMV:

At +25°C, V_{IN+} = 43.9mV

At +150°C, V_{IN+} = 62.9mV

Since both V_{IN+} and V_Z are small relative to the desired 2V common-mode voltage, they may be ignored in computing R_{CM} as long as the CMV is met.

R_{CM} = 3V/0.8mA = 3.75kΩ

V_{IN+} min = 3V + 0.0439V

V_{IN+} max = 3V + 0.0629V

V_{IN-} = 3V + 0.0439V

EXAMPLE 2

Thermocouple shown in Figure 10.

Given a process with temperature (T_1) limits of 0°C and +1000°C, configure the IXR100 to measure the temperature with a Type J thermocouple that produces a 58mV change for 1000°C change. Use a semiconductor diode for a cold junction compensation to make the measurement relative to 0°C. This is accomplished by supplying a compensating voltage, equal to that normally produced by the thermocouple with its "cold junction" (T_2) at ambient. At +25°C this is 1.28mV (from thermocouple tables with reference junction at 0°C). Typically, at T_2 = +25°C, V_D = 0.6V and

$\Delta V_D/\Delta T = -2mV/°C$. R_5 and R_6 form a voltage divider for the diode voltage V_D. The divider values are selected so that the gradient $\Delta V_D/\Delta T$ equals the gradient of the thermocouple at the reference temperature. At +25°C this is approximately $-52\mu V/°C$ (obtained from standard thermocouple table); therefore,

$$\Delta V_{TC}/\Delta T = (\Delta V_D/\Delta T)(R_6/(R_5 + R_6)) \quad (2)$$

$$-52\mu V/°C = (-2000\mu V/°C)(R_6/(R_5+R_6))$$

R_5 is chosen as 3.74kΩ to be much larger than the resistance of the diode. Solving for R_6 yields 100Ω.

Transmit 4mA for T_1 = 0°C and 20mA for T_1 = +1000°C. Note: $V_{IN} = V_{IN+} - V_{IN-}$ indicates that T_1 is relative to T_2. The input full scale span is 58mV. R_S is found from Equation (1) and equals 153.9Ω.

R_4 is chosen to make the output 4mA at T_{TC} = 0°C (V_{TC} = 1.28mV) and T_D = 25°C (V_D = 0.6V).

V_{TC} will be −1.28mV when T_{TC} = 0°C and the reference junction is at +25°C. V_4 must be computed for T_D = +25°C to make V_{IN} = 0V.

$V_{D(25°C)}$ = 600mV

$V_{IN(25°C)}$ = 600mV (100/3740) = 16.0mV

$V_{IN} = V_{IN+} - V_{IN-} = V_{TC} + V_4 - V_{IN-}$

With V_{IN} = 0 and V_{TC} = −1.28mV,

$V_4 = V_{IN+} - V_{TC}$

V_4 = 16.0mV − (−1.28mV)

0.4mA (R_4) = 17.28mV

R_4 = 43.2Ω

THERMOCOUPLE BURN-OUT INDICATION

In process control applications it is desirable to detect when a thermocouple has burned out. This is typically done by forcing the two-wire transmitter current to the upper or lower limit when the thermocouple impedance goes very high. The circuits of Figures 10, 11 and 12 inherently have down scale indication. When the impedance of the thermocouple gets very large (open) the bias current flowing into the + input (large impedance) will cause I_O to go to its lower range limit value (about 3.6mA). If up scale indication is desired, the circuit of Figure 13 should be used. When the T_C opens, the output will go to its upper range limit value (about 32mA or higher).

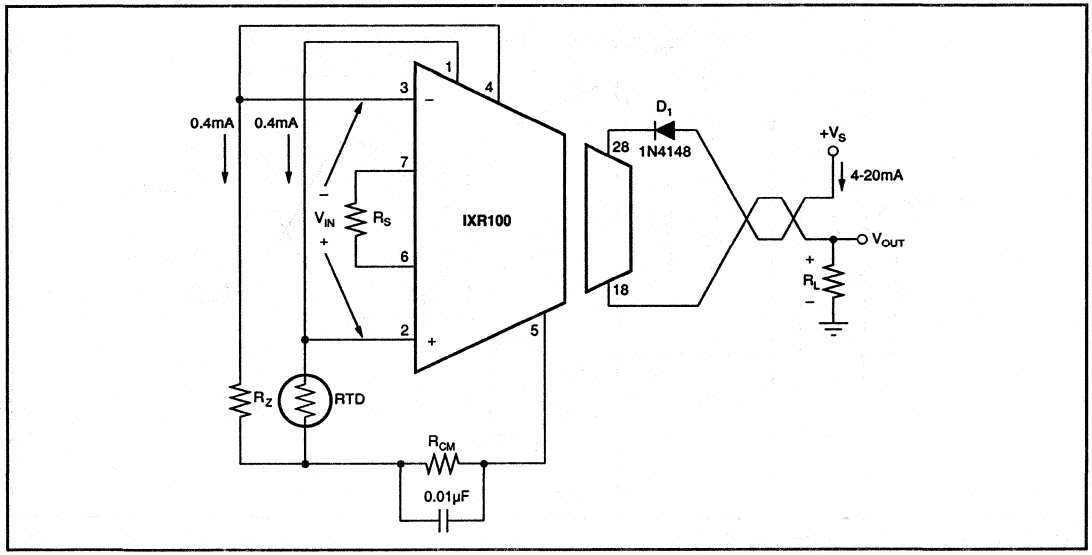


FIGURE 9. Pt100 RTD Without Linearization.

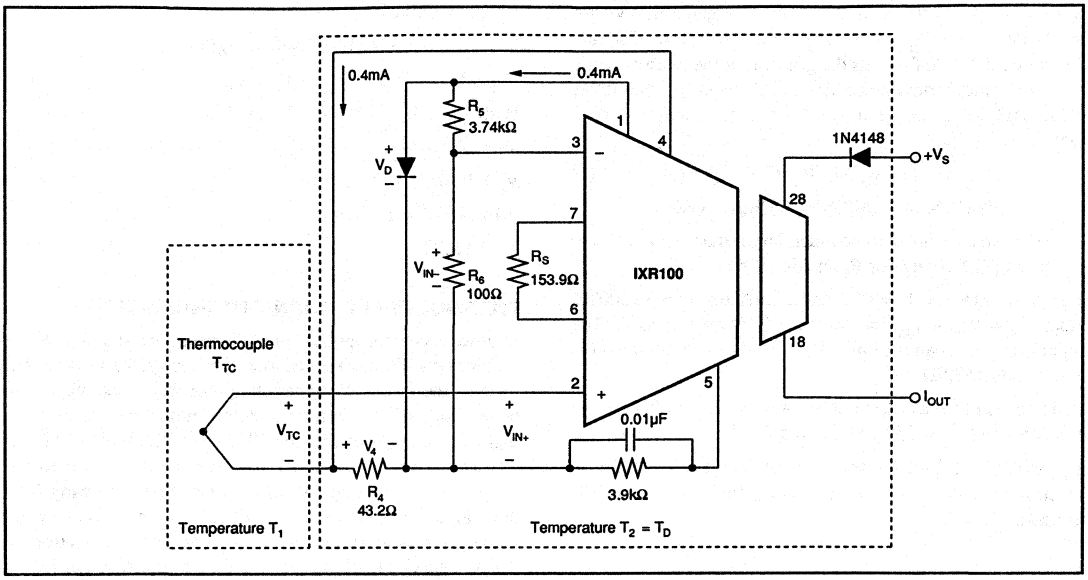


FIGURE 10. Thermocouple Input Circuit with Two Temperature Regions and Diode (D) Cold Junction Compensation.

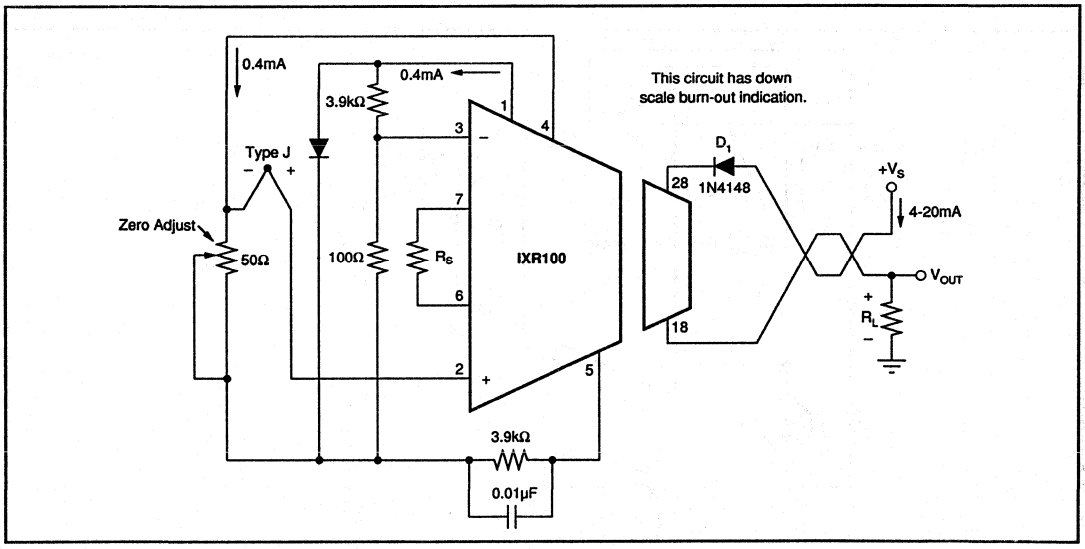


FIGURE 11. Thermocouple Input with Diode Cold Junction Compensation and Down Scale Burn-out Indication.

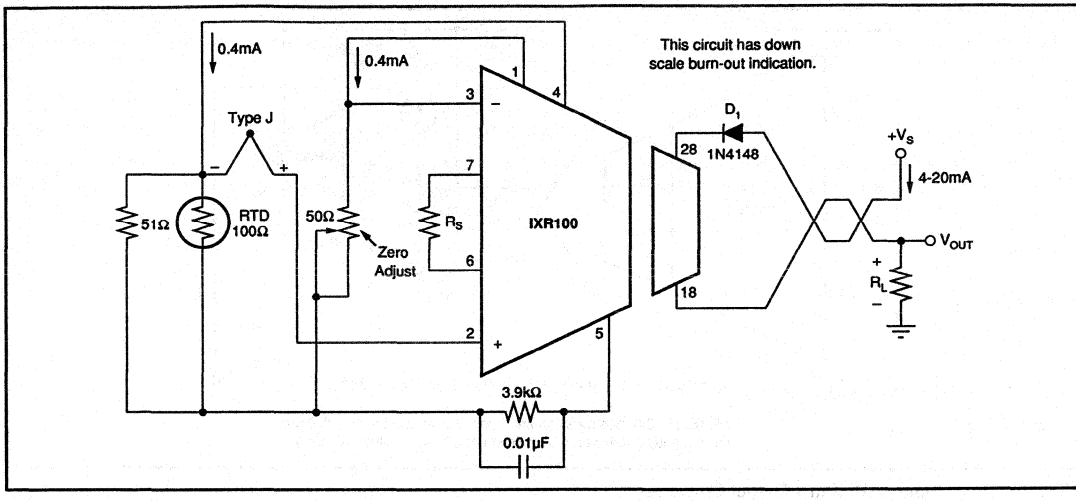


FIGURE 12. Thermocouple Input with RTD Cold Junction Compensation and Down Scale Burn-out Indication.

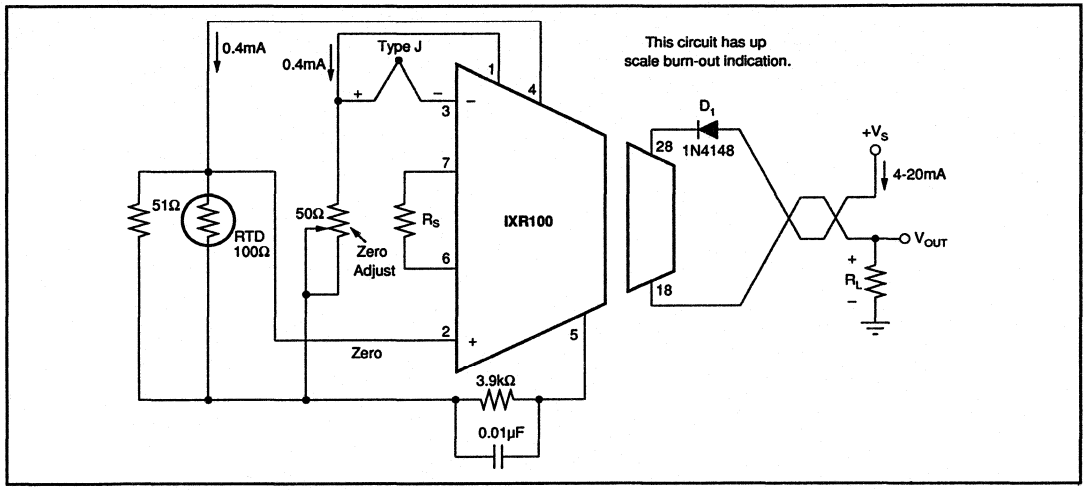


FIGURE 13. Thermocouple Input with RTD Cold Junction Compensation and Up Scale Burn-out Indication.

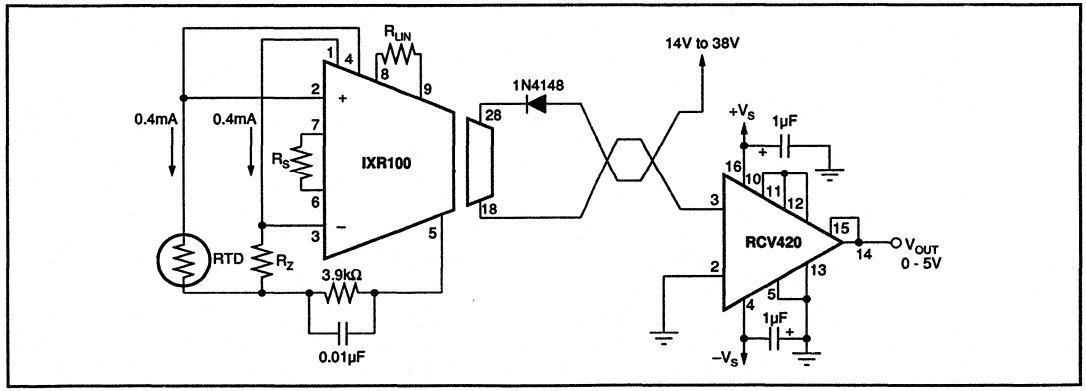


FIGURE 14. Isolated 4-20mA Instrument Loop.

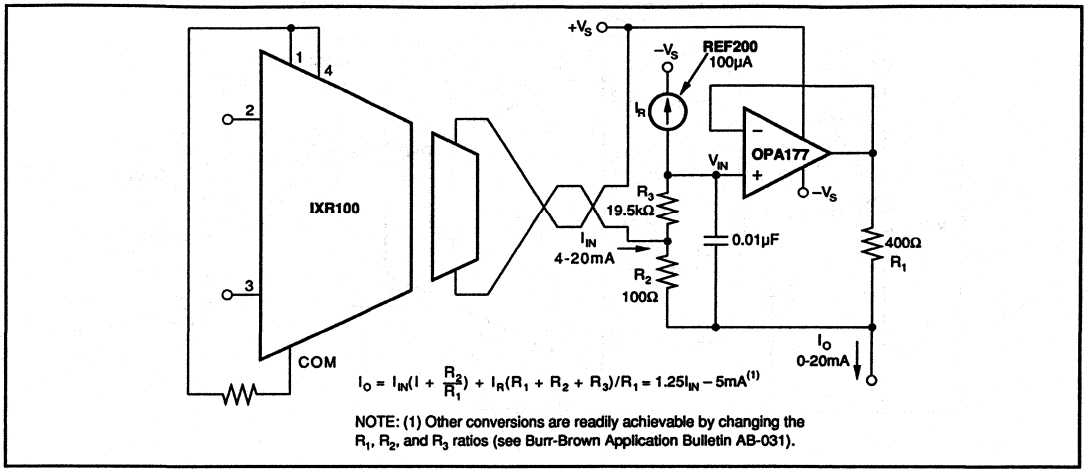


FIGURE 15. 4-20mA to 0-20mA Output Converter.

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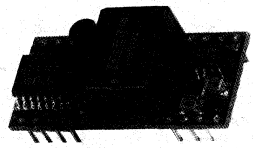


PWS727
PWS728

Isolated, Unregulated DC/DC CONVERTERS

FEATURES

- 100% TESTED FOR HIGH VOLTAGE BREAKDOWN
- COMPACT (28-pin DIP)
- 5V OR 15V INPUT OPTIONS
- SYNCHRONIZABLE (TTL)

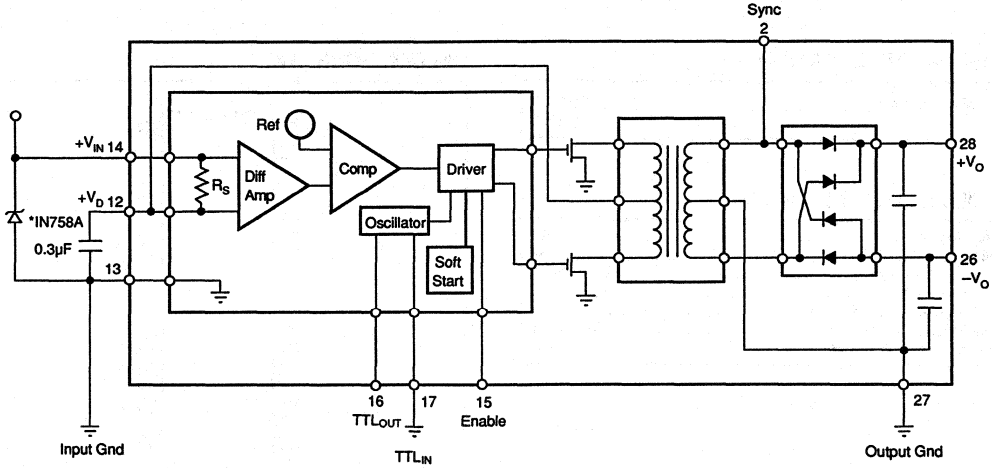
APPLICATIONS

- INDUSTRIAL PROCESS CONTROL
- GROUND LOOP ELIMINATION
- POINT-OF-USE ANALOG POWER

DESCRIPTION

The PWS727 is a DC/DC converter which uses minimal PC board space and converts a single input 10 to 18VDC to bipolar voltages of the same value as the input. The PWS728 converts a 4.7 to 6VDC to bipolar voltages three times the value of the input. The converters are capable of providing ±15mA (PWS727) or ±12mA (PWS728) at rated voltage and up to ±30mA.

The PWS727 and PWS728 use a high-frequency (800kHz nominal) surface mount oscillator that makes it possible to minimize the transformer size. The transformer is composed of a split bobbin isolation transformer using a ferrite core and is encapsulated in a plastic package, allowing a higher isolation voltage rating. The design minimizes high frequency radiated noise on the output by using a ground plane directly under the high frequency components.



* Use a 10V zener on PWS728 to prevent input spikes overstressing the diode bridge.

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SPECIFICATIONS

ELECTRICAL

At V_{IN} =15VDC, Output Load = ±15mA (PWS727) and T_A = +25°C unless otherwise noted. Or V_{IN} = 5VDC, Output Load = ±12mA (PWS728) and T_A = +25°C unless otherwise noted

PARAMETER	CONDITIONS	PWS727			PWS728			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
ISOLATION								
Voltage Rated Continuous AC 60Hz		750			*			Vrms
100% Test[1]	60Hz, 1s, <5pC PD	1200			*			Vrms
Barrier Impedance			10^{12} || 8			*		Ω || pF
Leakage Current at 60Hz	V_{ISO} = 240Vrms, 60Hz		1	1.5		*	*	µArms
INPUT								
Rated Voltage			15			5		V
Voltage Range		10		18	4.5		6	V
Current			55	65		110	130	mA
Current Ripple			2.5			7.5		mAp-p
Current Limit				250			*	mAp-p
TTL_{IN}, I_{IH}				10			*	nA
I_{IL}			–1			*		µA
V_{IH}		2.0			*			V
V_{IL}				.8			*	V
Frequency Range		1	1.6	2.5	*	*	*	MHz
TTL_{OUT}, I_{OL}				15			15	mA
OUTPUT								
Rated Output Voltage		14.25	15.0	15.75	*	*	*	VDC
Current			15	30		12	30	mA
Regulation								
(single ended load change)	$+I_O$ = 7.5 –15mA, $–I_O$ = 15mA		45			135		mV/mA
Sensitivity	V_{IN} = 10 to 18 V		1.13			3.8		V/V
Balance				15			25	mV
Ripple Voltage	At Switching Frequency		10			*		mVpp
Output Switching Noise	>800kHz		20			*		mVpp
Output Voltage Temp Coefficient			.05			*		V/°C
Sync	Loading			20 || 40			*	kΩ || pF
Sync Frequency[2]		725	800	875	*	*	*	kHz
TEMPERATURE RANGE								
Specification		0		70	*		*	°C
Operation		–40		85	*		*	°C
Storage		–40		85	*		*	°C

* Specifications the same as PWS727.

NOTE: (1) Tested at 1.6 x rated, fail on 5pC partial discharge leakage current on 5 successive pulses. (2) Nominal with pin 17 grounded.

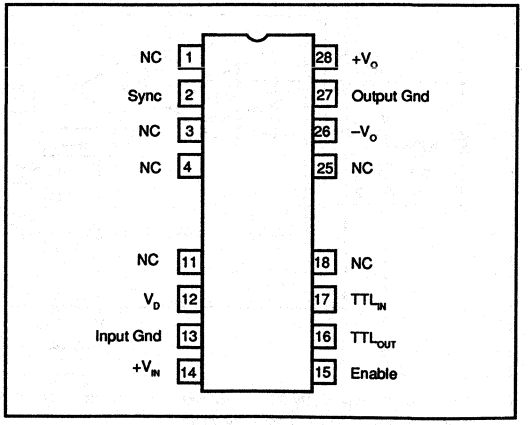
ORDERING INFORMATION

Basic Model Number	PWS727 PWS728

ABSOLUTE MAXIMUM RATINGS

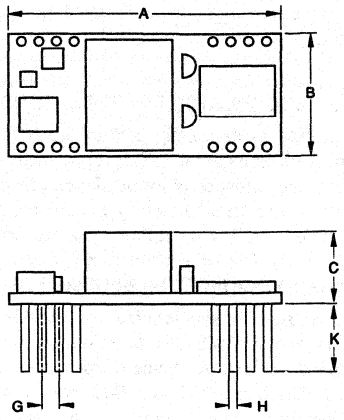
Supply Voltage	18V
Continuous Isolation Voltage	750Vrms
Junction Temperature	+150°C
Storage Temperature	85°C
Lead Temperature (Solder, 10s)	300°C
Output Short to Common	Continuous
Max Load, Sum of Both Outputs	60mA

PIN CONFIGURATION



MECHANICAL

28-Pin Double — Wide DIP

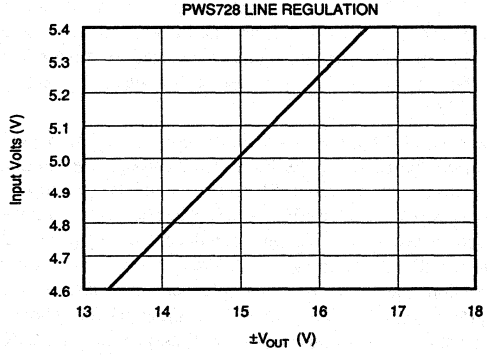


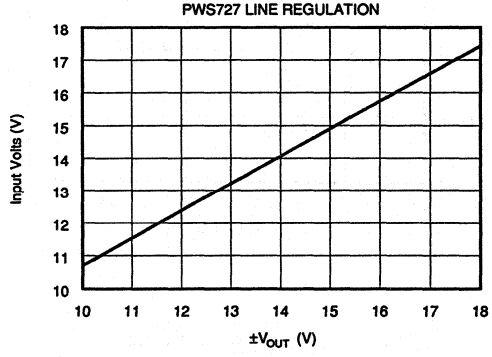
DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.440	1.460	36.58	37.08
B	.690	.710	17.53	18.03
C	.390	.410	9.91	10.41
G	.100 BASIC		2.54 BASIC	
H	.020 BASIC		0.51 BASIC	
K	.190	.210	4.83	5.33
L	.600 BASIC		15.24 BASIC	

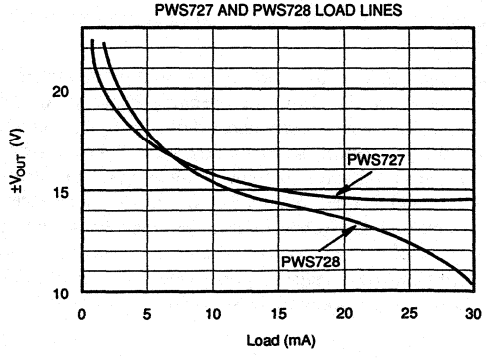
NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

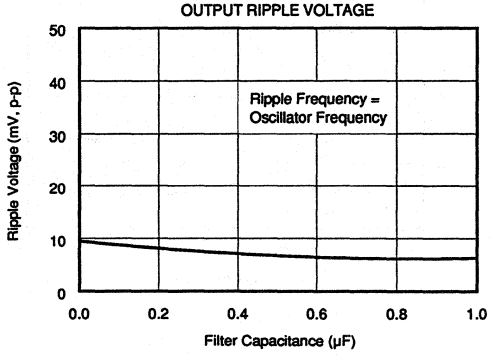
TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_{IN} = 15VDC, I_{LOAD} = ±15mA (PWS727), or V_{IN} = 5VDC, output load = ±12mA (PWS728) unless otherwise noted.





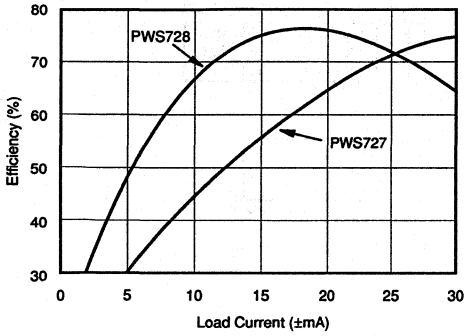




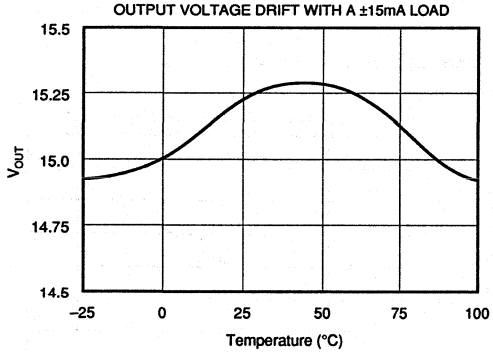
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_{IN} = 15VDC, I_{LOAD} = ±15mA (PWS727), or V_{IN} = 5VDC, output load = ±12mA (PWS728) unless otherwise noted.

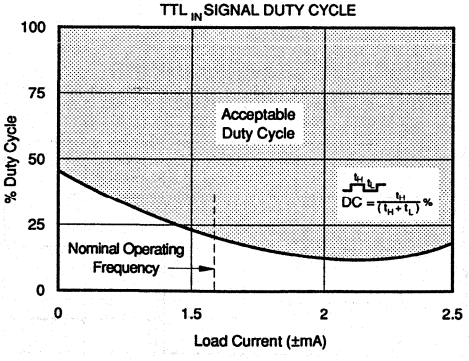
EFFICIENCY/LOAD CURVE



OUTPUT VOLTAGE DRIFT WITH A ±15mA LOAD



TTL$_{IN}$ SIGNAL DUTY CYCLE



THEORY OF OPERATION

The PWS727 and PWS728 are composed of the PWS750 building blocks which are assembled along with some standard components to build an isolated push pull DC/DC converter.

PWS727 AND PWS728 PIN FUNCTIONS

TTL_{IN} is used to optionally control the frequency of the oscillator with an external TTL level frequency source. The input frequency must be twice the desired driver frequency, since there is an internal divide by 2 circuit to produce a 50% duty cycle output. The input duty cycle can vary from 12% to 95%, (see the Typical Performance Curves). **When in the free running mode the TTL_{IN} pin must be tied to ground.**

TTL_{OUT} is used to synchronize the outputs of multiple PWS727s and/or PWS728s to minimize beat frequency problems if desired. A standard open collector output is provided, therefore a 330 to 3.3kΩ resistor will be necessary, depending on the amount of stray capacitance on the TTL_{IN} line. A maximum of 8 PWS727s or PWS728s can be connected without the use of an external TTL buffer. Connect the TTL_{OUT} of a master unit to the TTL_{IN} of the slave units.

An Enable pin is provided so that the driver can be shut down to minimize power use if required. A TTL low applied to the pin will shut down the driver within one cycle (1.25µs). A TTL high will enable driver outputs within one cycle. The TTL_{OUT} will still have an 800kHz signal when a master driver is disabled, so other synchronized drivers will not be shut down. The pin can be left open for normal operation.

The $+V_{IN}$ pin supplies power to the converter. The V_D pin connects the power to the transformer through the internal overcurrent sense resister. The other end of the overcurrent sense resister is tied to $+V_{IN}$. A 0.3µF bypass capacitor must be connected to the V_D pin to reduce the ripple current through the shunt resistor, otherwise false current limit conditions can occur due to ripple voltage peaks. During overload conditions the output drive shuts off for approximately 80µs, then turns back on for 20µs, resulting in a 25% power up duty cycle. If the overload condition still exists, then the output will shut off again. When the fault or the excessive load is removed, the converter resumes normal operation.

The Sync pin can be used to synchronize the internal oscillator of an ISO120 to the operating frequency of the converter. The Sync pin is connected directly to the secondary of the transformer, so an 800kHz square wave of twice the output magnitude is present. Minimum pc board trace length should be used to minimize loading the transformer. When making the connection to the ISO120, a simple frequency divider circuit (see Figure 3) is necessary to match the 400kHz nominal frequency required by the ISO120. If this function is not used, leave the pin disconnected.

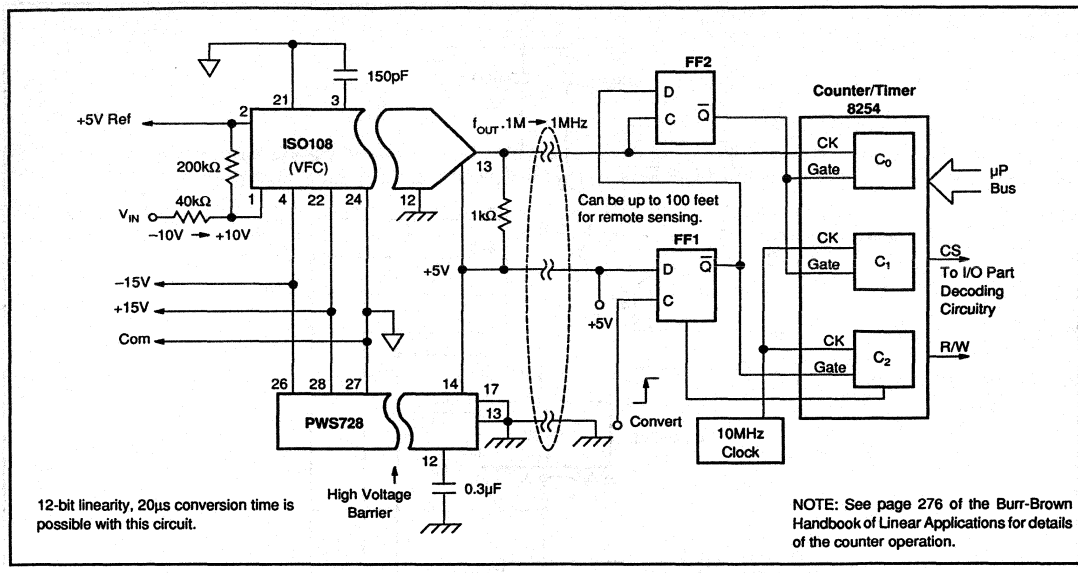


FIGURE 1. Isolated Integrated A/D Conversion System Using Ratiometric Counting and Microprocessor Interface, Operating from a Single 5V Supply.

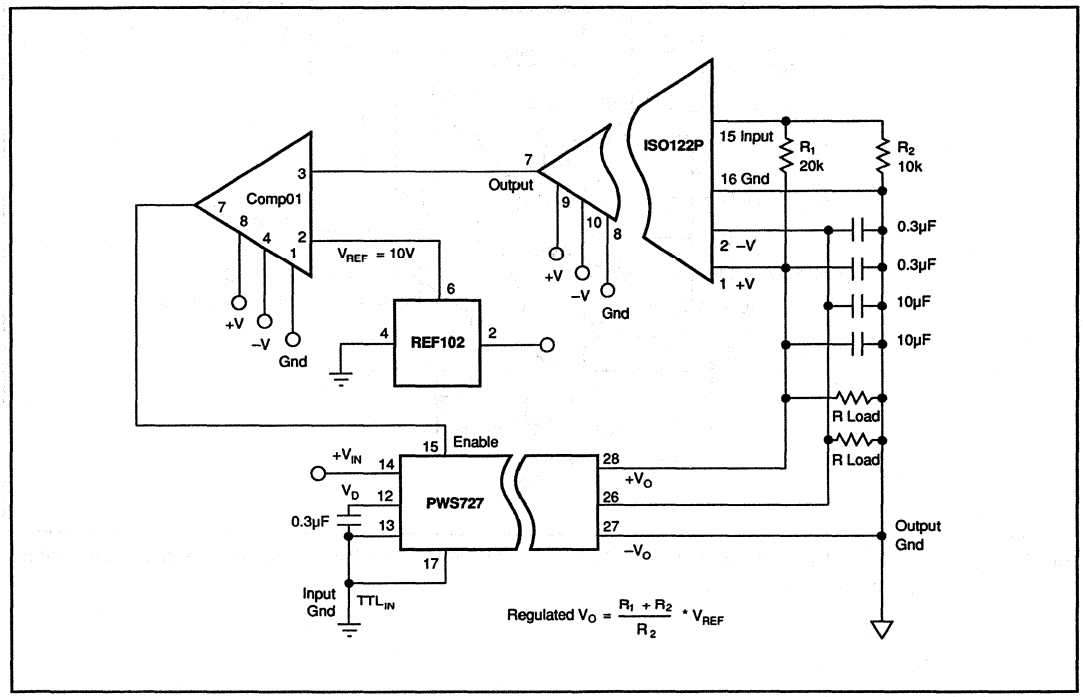


FIGURE 2. Regulated Output Using the Enable Pin to Cycle the Converter Output On and Off.

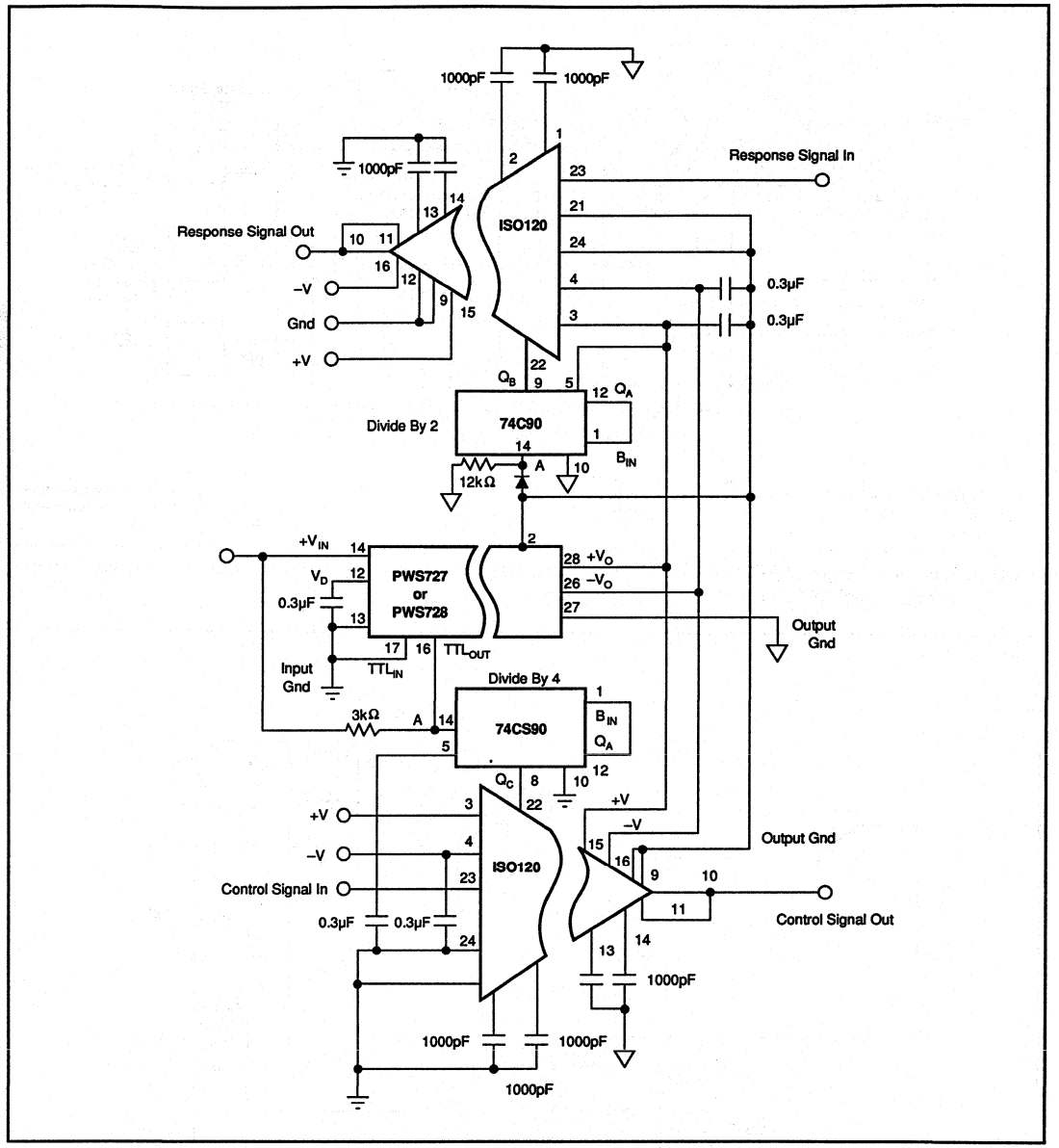


FIGURE 3. The PWS727 or PWS728 Can Be Used to Synchronize the ISO120. The Output Sync Must be Divided by 2 and the TTL_{OUT} Must Be Divided by 4.

BASIC OPERATION

PC BOARD LAYOUT CONSIDERATIONS

These converters have low output ripple so that standard layout methods are all that is necessary for good circuit performance. Bypass capacitors should be placed close to each device powered by the converters. To minimize the noise pickup by sensitive (12 bit resolution) circuits, a 10Ω resistor can be placed in series with the isolated power traces. The resistor in conjunction with the bypass capacitor acts as a low pass filter, to minimize isolation amplifier PSRR related ripple voltage feedthrough. A π filter can also be used at the input ($+V_{IN}$) to minimize input supply ripple current.

5V OPERATION

With 5V operation (PWS728) the transformer winding ratio is 3:1, therefore generating much greater currents in the primary. The input ripple will be larger, so an input π filter will be necessary to isolate the supply noise from the rest of the circuit. For example, when the output load is ± 15mA the input current will be approximately 120mA.

OUTPUT CURRENT RATING

The PWS727 and PWS728 contain soft start circuitry to protect the FETs from high inrush currents during turn on. The internal input current limit is 250mA peak to prevent thermal overload of the MOSFETs. The maximum output current rating is ±30mA. Total current, which can be drawn from each isolation channel, is the total of the of the power being drawn from both the +V and –V outputs. For example, if one output is not used, then maximum current can be drawn from the other output. In all cases the maximum current that can be drawn from any individual channel is:

$$(+I_{OUT}) + (-I_{OUT}) < 60mA$$

It should be noted that many analog circuit functions do not simultaneously draw equal current from both the positive and negative supplies.

HIGH VOLTAGE TESTING

Burr Brown Corporation has adopted a partial discharge test criterion that is similar to the German VDE0884 optocoupler standard. This method requires that less than 5pC partial discharge across the isolation barrier with 1200 Vrms 60Hz applied. This criterion confirms transient overvoltage (1.6 x 750 Vrms) protection without damage to the PWS727 or PWS728. Lifetest results verify the absence of high-voltage breakdown under continuous rated voltage and maximum temperature.

The minimum AC barrier voltage that initiates partial discharge above 5pC is defined as the "inception voltage". Decreasing the barrier voltage to a lower level is required before partial discharge ceases and is known as "extinction voltage". We have developed a package insulation system to yield an inception voltage greater than 1200 Vrms so that transient voltages below this level will not damage the isolation barrier. The extinction voltage is above 750 Vrms so that even overvoltage-induced partial discharge will cease once the barrier voltage is reduced to the rated value. Previous high voltage test methods relied on applying a large enough overvoltage (above rating) to break down marginal devices, but not so high as to damage good ones. Our partial discharge testing gives us more confidence in barrier reliability than breakdown/no breakdown criteria.

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

BURR-BROWN®

PWS745

Multi-Channel DC/DC CONVERTER COMPONENTS

FEATURES

- COMPACT SIZE
- LOW COST PER CHANNEL
- DRIVES UP TO 8 CHANNELS
- 750/1500VAC ISOLATION
- FLEXIBLE USE WITH PWS740/PWS750 COMPONENTS
- 0.4 IN. MAXIMUM MOUNTING HEIGHT

APPLICATIONS

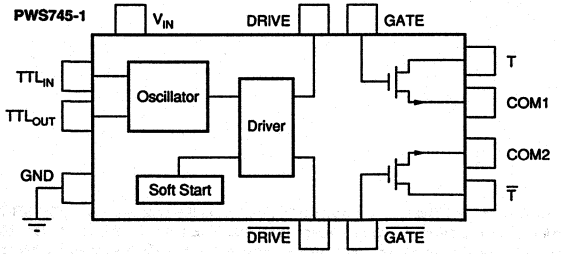
- INDUSTRIAL CONTROL
- GROUND-LOOP ELIMINATION
- PC-BASED DATA ACQUISITION
- POINT-OF-USE POWER CONVERSION
- 5V TO ±15V FROM DIGITAL SUPPLIES

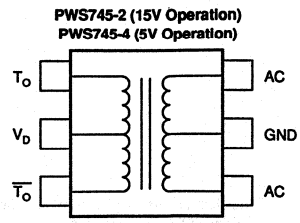
DESCRIPTION

The PWS745 is a set of componets useful in the construction of single or multi-channel isolated DC/DC converters. By themselves, or in combination with the PWS740 and PWS750 families of components, they allow compact, optimal, and low-cost solutions to many power supply problems.

The PWS745-1 DIP oscillator/driver can be used to drive up to eight channels of independently isolated power. The switching MOSFETs are built into the driver to allow simple low-cost assembly of the multi-channel converter. The PWS745-1 also is capable of operating at 5VDC and can be easily synchronized with TTL level signals. While offering the user an alternative to the TO-3 package of the PWS740, the PWS745-1 also allows the user to select varying levels of power, isolation voltage, mounting technology and system configuration by choosing among the several component families. For example, the PWS745-1 can directly drive the PWS740, PWS745, or PWS750 transformers. It also can drive the FETs of a PWS750 distributed power system. The operating frequency is compatible with the ISO120 family of isolation amplifiers and is capable of multi-channel synchronized operation to eliminate troublesome beat frequencies.

The PWS745-2 is a 15V to ±15V output version, while the PWS745-4 is the 5V to ±15V output version. The PWS740-3 high-speed bridge provides a convenient rectifier for the selected transformer output.





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PDS-1095

SPECIFICATIONS

ELECTRICAL

At V_{IN} = 15VDC, Output Load = ±15mA (PWS745-2) and T_A = 25°C unless otherwise noted.
Or V_{IN} = 5VDC, Output Load = ±12mA (PWS745-4) and T_A = 25°C unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
PWS745-1 OSCILLATOR/DRIVER					
Frequency: Internal OSC	TTL_{IN} = 0V	550	600	650	kHz
External OSC		500	600	1000	kHz
Supply: 15V Operation		10	15	18	V
5V Operation		4.5	5	5.5	V
Current	No Load		10		mA
	Max Load		650		mA
Current Ripple	C_{BYPASS} = 1µF		2.5		mAp-p
TTL_{IN}: I_{IH}				10	nA
I_{IL}			–1		µA
V_{IH}		2			V
V_{IL}				0.8	V
Frequency		1		2	MHz
TTL_{OUT}: I_{OL}				15	mA
Frequency			600		kHz
T, $\overline{T}$ Drive Current				50	mA
T, $\overline{T}$ Drive Voltage: High		3		7	V
Low				0.7	V
PWS745-2					
Voltage, Rated Continuous AC 60Hz		750			Vrms
100% Test(1)	60Hz, 1s	1200			Vrms
Barrier Impedance			10^{12} || 8		Ω || pF
Leakage Current at 60Hz	V_{ISO} = 240Vrms, 60Hz			150	µArms
PWS745-4					
Voltage, Rated Continuous AC 60Hz		750			Vrms
100% Test(1)	60Hz, 1s	1200			Vrms
Barrier Impedance			10^{12} || 8		Ω || pF
Leakage Current at 60Hz	V_{ISO} = 240Vrms, 60Hz			150	µArms
TEMPERATURE RANGE					
Specification		–40		85	°C
Operation		–40		85	°C
Storage		–40		85	°C

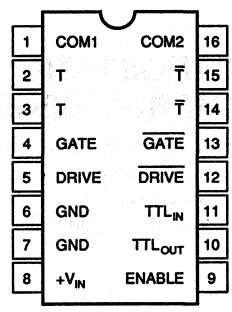
NOTES: (1) Tested at 1.6 rated, fail on 5pc partial discharge leakage current on five successive pulses.

ABSOLUTE MAXIMUM RATINGS

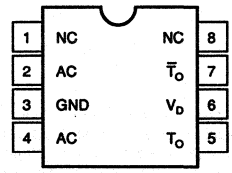
Supply Voltage 18V
Continuous Isolation Voltage 750Vrms
Junction Temperature ..... 150°C
Storage Temperature ..... 85°C
Lead Temperature (soldering, 10s) ..... 300°C
Transformer Output Short to Common ..... Continuous
Max Load, Sum of All Transformer Outputs 500mA
Stresses above these ratings may permanently damage the device.

PIN CONFIGURATIONS

PWS745-1

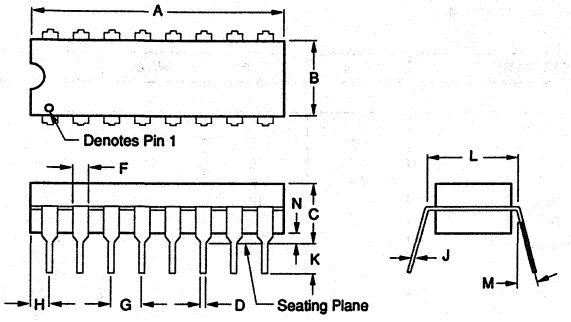


PWS745-2/PWS745-4



MECHANICAL

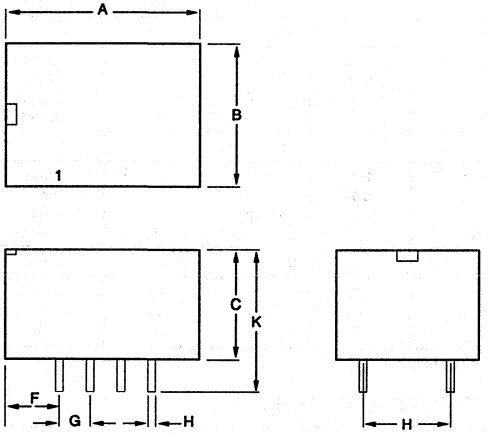
PWS745-1 — 16-Pin Plastic DIP



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.760	.885	19.30	22.48
B	.220	.280	5.59	7.11
C	—	.200	—	5.08
D	.015	.023	0.38	0.58
F	.030	.070	0.76	1.78
G	.100 BASIC		2.54 BASIC	
H	.030	.095	0.76	2.41
J	.008	.015	0.20	0.38
K	.100	—	2.54	—
L	.300 BASIC		7.62 BASIC	
M	—	15°	—	15°
N	.020	.050	0.51	1.27

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

Package — 8-Pin Plastic



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.620	.640	15.78	16.26
B	.465	.485	11.81	12.32
C	.350	.370	8.89	9.40
F	.165	.185	4.19	4.70
G	.100 BASIC		2.54 BASIC	
H	.025 SQ.		.635 SQ.	
K	.470	.490	11.94	12.45
L	.280	.300	7.11	7.62

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.

ELECTROSTATIC DISCHARGE SENSITIVITY

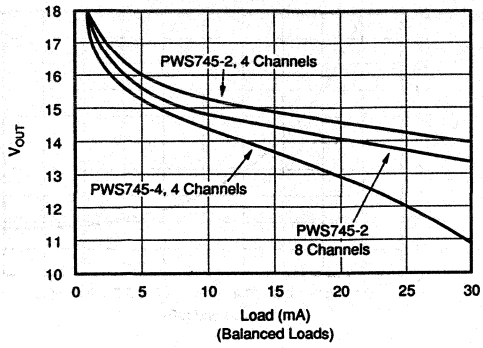
Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

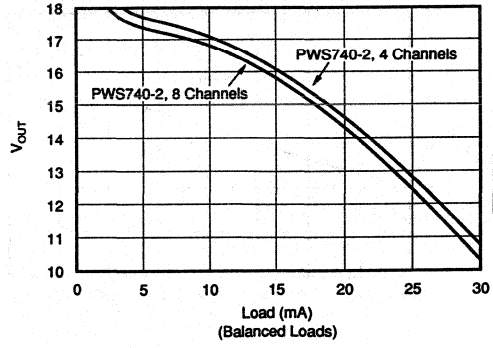
TYPICAL PERFORMANCE CURVES

T_A = 25°C, +15VDC or +5VDC unless otherwise specified.

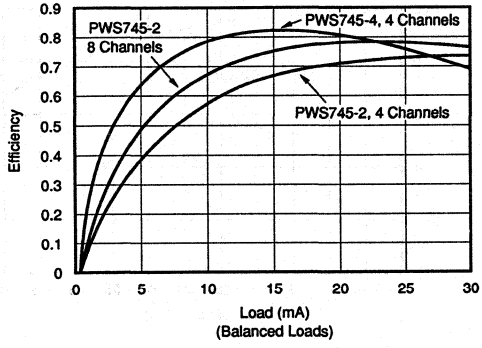
LOADLINE, PWS745



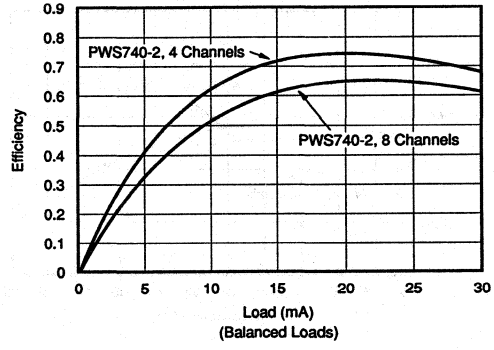
LOADLINE, PWS740



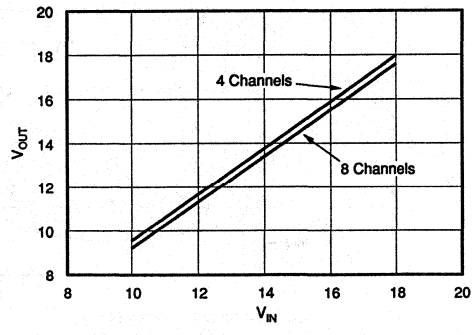
EFFICIENCY, PWS745



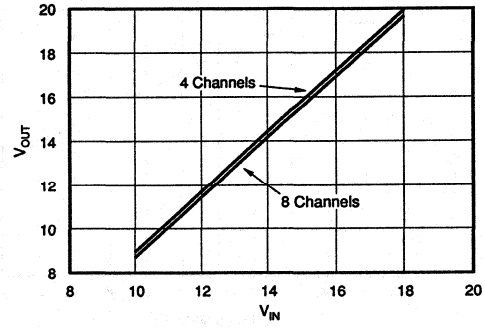
EFFICIENCY, PWS740



LINE REGULATION USING PWS745-2 TRANSFORMERS



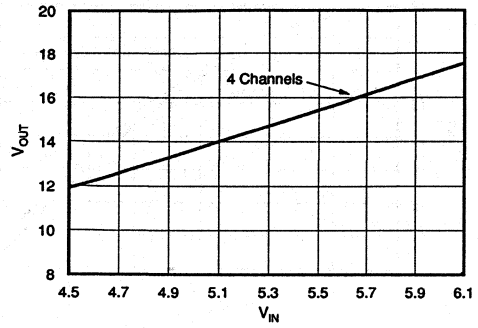
LINE REGULATION USING PWS740-2 TRANSFORMERS



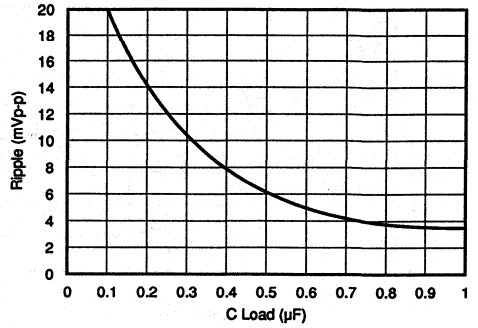
TYPICAL PERFORMANCE CURVES (CONT)

T_A = 25°C, +15VDC or +5VDC unless otherwise specified.

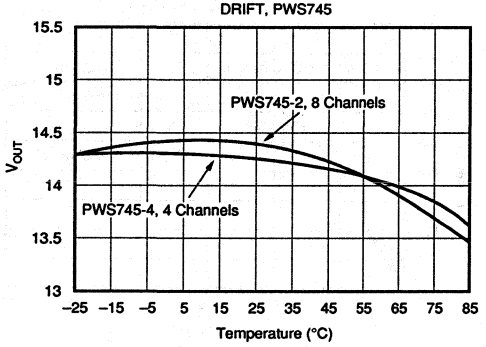
LINE REGULATION USING PWS745-4 TRANSFORMERS



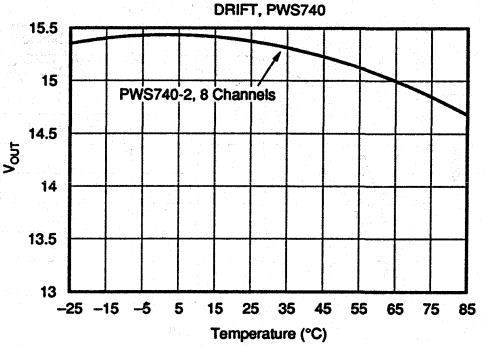
OUTPUT RIPPLE VOLTAGE



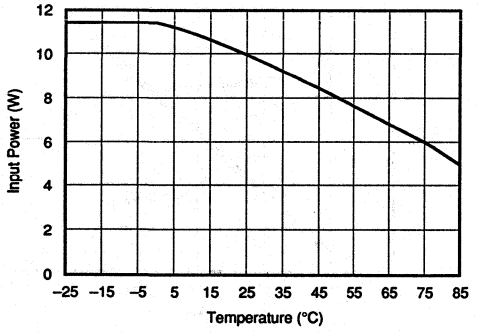
DRIFT, PWS745



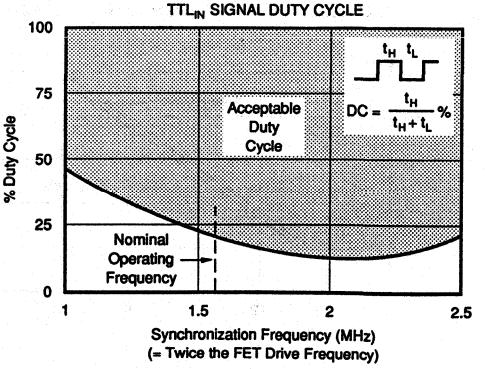
DRIFT, PWS740



PWS745-1 MAXIMUM INPUT POWER



TTL_{IN} SIGNAL DUTY CYCLE



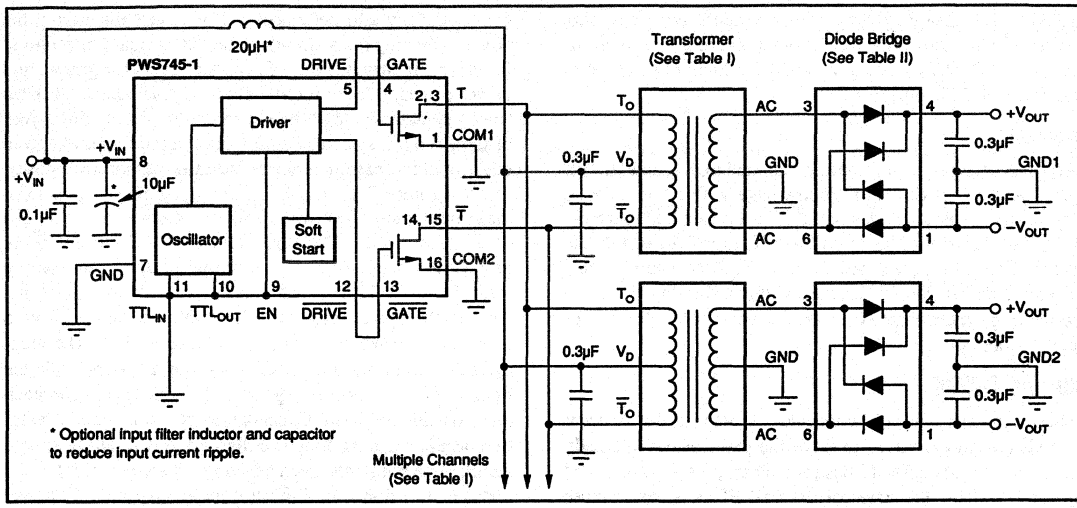


FIGURE 1. Typical Connections.

BASIC OPERATION

The PWS745 components are used to build a multichannel DC/DC converter. The oscillator runs at 600kHz nominal, making it possible to reduce the size of the transformer and lower the output ripple voltage. The PWS745-1 is a power oscillator/switch able to directly drive the primary side of an isolation transformer. The small size of the driver is achieved by using a multiple chip transfer molding process. The power components are mounted directly on the copper leadframe, utilizing two pins directly connected to each die pad to maximize heat sink area. The output of the transformer is rectified with a high speed diode bridge. The PWS740-2 is used when 1500Vrms isolation is required. The PWS745-2 or PWS750-2 is used when 750Vrms isolation is required. With these transformers, the output voltages directly track the input voltage. The PWS745-4 or PWS750-4 is used to step up the input voltage from 5V to ±15V. Operation at 5V makes it possible to build an isolated system for powering the analog components when only a logic supply is available. Using the PWS745-2 or -4 allows the user 0.5in. PCB spacing. The possible component combinations are summarized in Figure 1 and Tables I and II. The 600kHz operating frequency enables direct synchronization with products such as the ISO120 and ISO121. See Figure 3. The use of synchronization makes it possible to eliminate any power-supply induced ripple in the output of the isolation amplifiers and to minimize beats falling in the signal path bandwidth.

PIN DESCRIPTIONS

$+V_{IN}$ AND GND

The $+V_{IN}$ pin supplies power to the oscillator. The GND pins are used for the return currents of the driver chip.

TRANSFORMER	ISOLATION	CHANNELS	I/O	TECHNOLOGY
PWS745-2	750VAC	8	1:1	Thru-hole
PWS745-4	750VAC	4	1:3	Thru-hole
PWS740-2	1500VAC	8	1:1	Thru-hole
PWS750-2U	750VAC	8	1:1	Surface-mount
PWS750-4U	750VAC	4	1:3	Surface-mount

TABLE I.

DIODE BRIDGE	TECHNOLOGY
PWS740-3	Thru-hole
PWS750-3U	Surface-mount

TABLE II.

COM1, COM2

The COM pins are connected to the the sources of theinternal MOSFETs and each pin must be tied to ground. The current from the primary windings of the transformers flows in through the T and $\overline{T}$ pins and then out through the COM pins.

TTL_{IN}

This pin must be tied to ground, except when it is desired to control the driver frequency with an external TTL level frequency source. The duty cycle can vary from 12% to 95% (see Typical Performance Curves). The input frequency must be twice the desired operating frequency, because an internal flip-flop is used produce a precise 50% duty cycle signal to the drivers.

TTL_{OUT}

When multiple PWS745-1 drivers must be synchronized to minimize beat frequencies in the output, a single driver is used to synchronize with the remaining drivers. The TTL_{OUT} pin is used as the synchronizing signal from the master controller and is connected to the TTL_{IN} of the slave drivers. A standard open collector output is provided, therefore a

330Ω to 3.3kΩ pull-up resistor will be necessary, depending on the stray capacitance on the synchronizing line. A maximum of 8 PWS745-1s can be connected without the use of an external TTL buffer.

ENABLE

An ENABLE pin is provided so that the DRIVE and $\overline{\text{DRIVE}}$ pins can be shut down to the low state within one cycle to minimize power use if desired. A TTL low applied to the pin will shut down the driver and a TTL high will enable the driver. The TTL_{OUT} will still have the 1.2MHz signal so that a master driver can be disabled without shutting down the remaining synchronized drivers. The pin can be left open for normal operation.

DRIVE, $\overline{\text{DRIVE}}$

These pins are normally connected directly to the adjacent GATE pin and are used to drive the gates of the internally packaged MOSFETs. If desired, these pins may be used instead to drive the gates of external FETs, such as those used in the PWS750 series of power components. It is important to minimize the capacitance on these nodes to insure the rapid charging of the MOSFET gates.

GATE, $\overline{\text{GATE}}$

These pins are are normally connected directly to the adjacent DRIVE pins, which are internally connected to the gates of the MOSFETs.

T, $\overline{\text{T}}$

The T and $\overline{\text{T}}$ pins are the complementary transformer drive connections. The signals on these pins are 600kHz complementary square waves with twice the amplitude of the input voltage. These lines connect MOSFET switches to the isolation transformers through the T_O and $\overline{T}_O$ pins. Without proper printed circuit board layout techniques, these lines could generate interference to analog circuits. Refer to the section on layout techniques.

T_O, $\overline{T}_O$

These pins are the primary terminals of the transformer and are connected to the T and $\overline{\text{T}}$ pins of the PWS745-1.

V_D

The center tap of the primary of the transformer is tied directly to the supply. A 0.3µF bypass capacitor must be located as close to this pin as possible.

AC

The output of the isolation transformer which is connected to the AC inputs on the PWS740-3 or PWS750-3 diode bridge.

PC BOARD LAYOUT CONSIDERATIONS

Multilayer printed circuit boards are recommended for PWS745 systems. Two-layer boards are certainly possible with satisfactory operation; however, three layers provide greater density and better control of interference from the power switching lines. Should a four-layer board be required for other circuitry, the use of seperate layers for ground and power planes, a layer for switching signals and a layer for analog signals would allow the most straightforward layout of the PWS745 system. Critical consideration should go to minimizing electromagnetic radiation from the power switching lines T-T_O and $\overline{\text{T}}$-$\overline{T}_O$. The dynamic component of the current is supplied by the bypass capacitor on the V_D pin of the transformer. The high frequency AC current flows through the transformer, T_O, returning in the T pin, passing through the MOSFET and exiting through the COM pin back to the bypass capacitor. This current path defines a magnetic loop which transmits a magnetic field. The magnetic field lines reinforce at the center of the loop, while the field lines from opposite points of the loop oppose each other outside the loop. Cancellation of the magnetic radiation occurs when the loop is collapsed to two tightly spaced parallel line segments, each carrying the same current in the opposite direction. All of the current in the ground or power plane will flow directly under the T-T_O traces because this is the path of least inductance or impedance. Another potential problem with the T-T_O lines is electric field radiation. Here, the power plane is effective in terminating most of the field lines because of its proximity. Additional shielding can be obtained by running ground trace(s) along the T-T_O lines, facilitating a minimum loop area for the transformer's center-tap bypass capacitor.

The connection between the outputs of the transformer and the diode bridge should be kept as short as possible. Unnecessary stray capacitance on these lines could cause resonant peaking to occur, resulting in a slight increase in output voltage.

EXTERNAL FILTER COMPONENTS

Filter components are necessary to reduce the input ripple current and output voltage noise. Without any input filtering, the sawtooth curents of the switching power lines T-T_O and $\overline{\text{T}}$-$\overline{T}_O$ would flow in the supply line. Since this AC current can be as great as 1A peak, voltage interference with other components using this supply line would likely occur. Use of a pi-filter can reduce the input ripple current to about 1mA peak. Recommended values are a 20µH inductor prior to the connection of the supply to the power plane. A 10µF tantalum capacitor with a 0.33µF ceramic capacitor is adequate for the input bypassing . The inductor must be rated for at least 2A or a DC resistance of 0.1Ω. An example of a low-cost inductor is part number 51591 from Pulse Engineering. Output voltage filtering is achieved with a 0.33µF capacitor connecting each V_{OUT} pin of the diode bridge to ground. Short leads and close placement of the capacitors to the bridge provide optimum high frequency bypassing. Using correct bypassing techniques, 600kHz ripple of less than 5mVp-p is achievable. High frequency noise bursts coinciding with the switch times are approximately 20mVp-p. Inductance of 20µH in series with the output loads will significantly reduce the noise seen by the loads.

5V OPERATION

With 5V operation, the transformer winding ratio is 3-to-1, generating much greater currents in the primary. Therefore, four channels are the maximum that can be powered directly by the PWS745-1.

OUTPUT CURRENT RATING

The PWS745-1 driver contains "soft start" driver circuitry to protect the driver MOSFETs and eliminate high in-rush currents during turn-on. Impedance limiting by the isolation transformers provides short circuit protection on the secondary side and limits the primary side current to a safe value.

The total current which can be drawn from each isolation channel at rated voltage is a function of total power being drawn from both V+ and V– outputs. For example, if one output is not used, then maximum current can be drawn from the other output. In all cases, the maximum total current that can be drawn from any individual channel is:

$$|I_L+| + |I_L-| < 60mA$$

It should be noted that many analog circuit functions do not simultaneously draw full rated current from both the positive and negative supplies. Thus the PWS745 system can power more circuits per channel than is first apparent. For example, if a circuit draws 10mA from the positive supply and 3mA from the negative supply, the PWS745 could power (60/13), or about four devices per channel.

HIGH VOLTAGE TESTING

Burr Brown Corporation has adopted a partial discharge test criterion that conforms to the German VDE0884 optocoupler standard. This method requires that less than 5pc partial discharge crosses the isolation barrier with 1200Vrms 60Hz applied. This criterion confirms transient overvoltage (1.6 x 750Vrms) protection without damage to the PWS745-2 or PWS745-4. Lifetest results verify the absence of high voltage breakdown under continuous rated voltage and maximum temperature. The minimum AC voltage that initiates partial discharge above 5pc is defined as the "inception voltage." Decreasing the barrier voltage to a lower level is required before partial discharge ceases and is known as "extinction voltage." We have developed a package insulation system to yield an inception voltage greater than 1200Vrms so that transient voltages below this level will not damage the isolation barrier. The extinction voltage is above 750Vrms so that even overvoltage induced partial discharge will cease once the barrier is reduced to the rated value. Previous high voltage test methods relied on applying a large enough overvoltage (above rated) to break down marginal units, but not so high as to permanently damage good ones. Our partial discharge testing gives us more confidence in barrier reliability than breakdown criterial.

APPLICATIONS

The PWS745 components form part of a versatile collection of isolation power supply components from Burr-Brown. The following diagrams illustrate only a few of the many possible combinations.

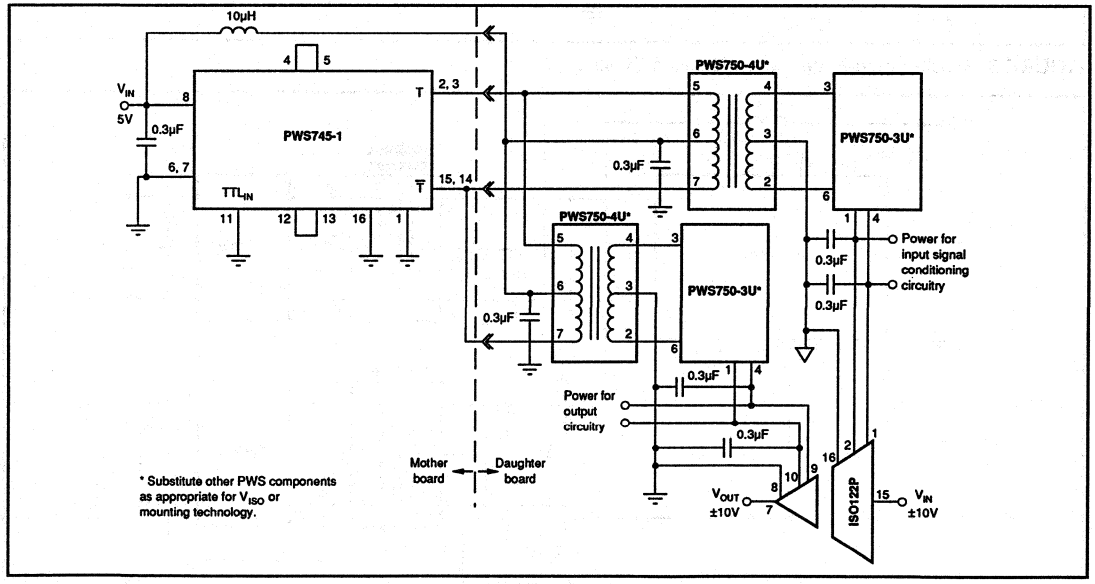


FIGURE 2. Complete ±10V Signal Acquisition System Operating from a Single 5V Supply.

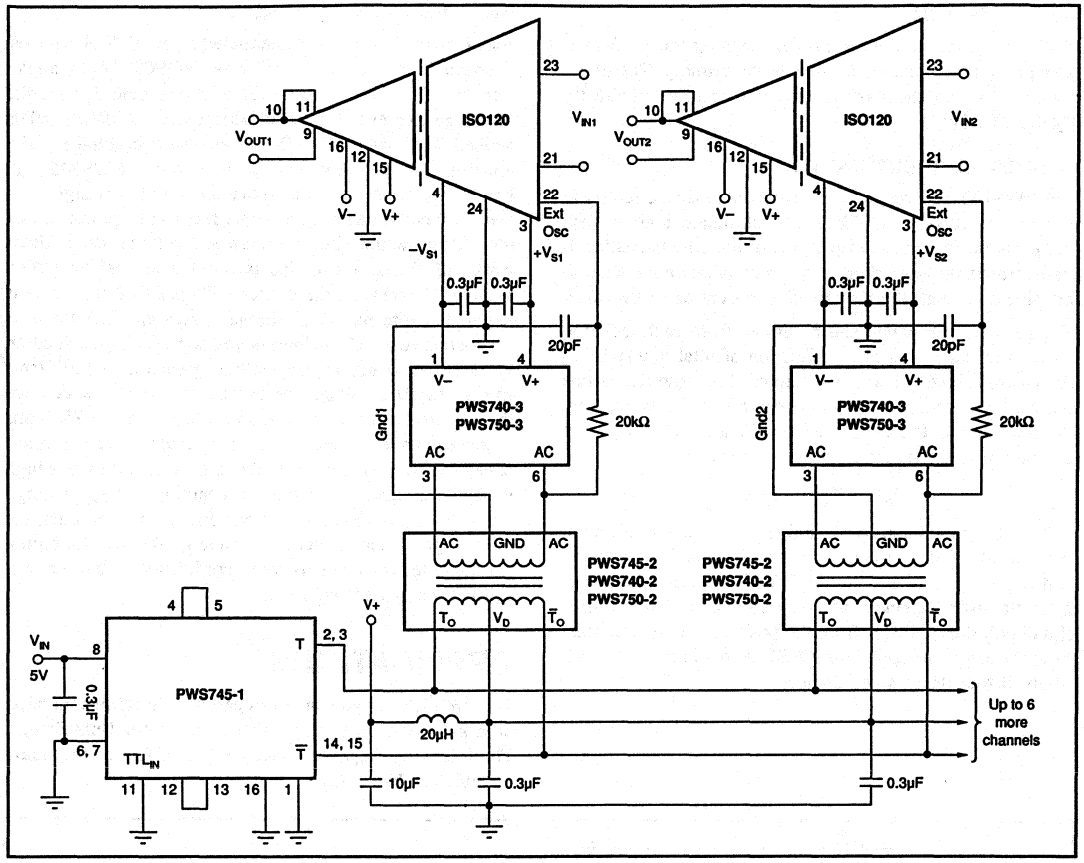


FIGURE 3. Synchronized-Multichannel Isolation System.

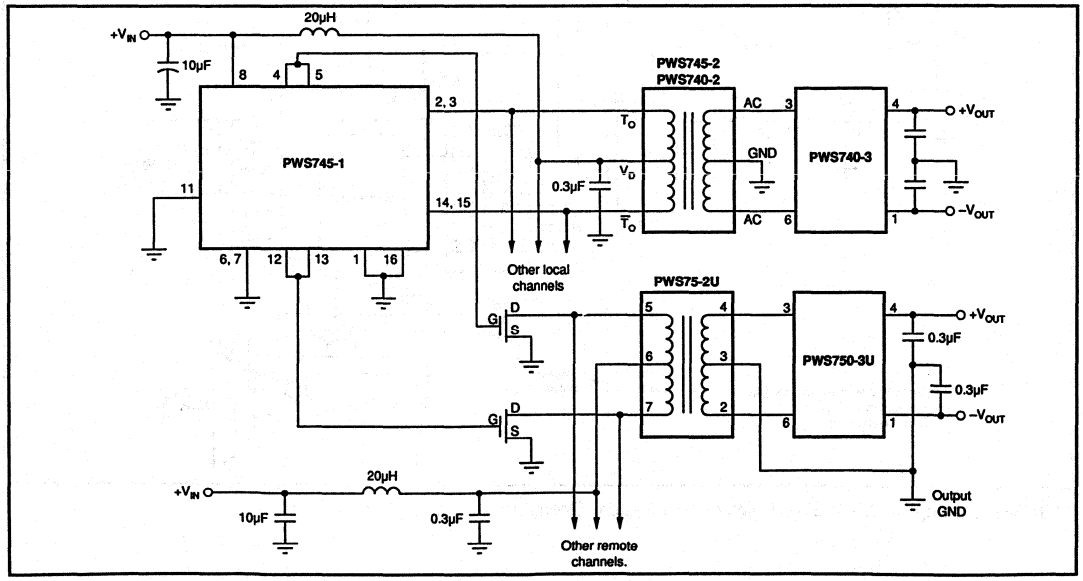
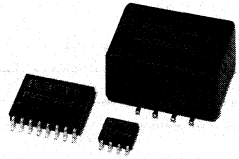


FIGURE 4. Remote and Local Operation of Isolated Power Channels.

BURR-BROWN®



PWS750

Isolated, Unregulated DC/DC CONVERTER COMPONENTS

FEATURES

- 100% TESTED FOR HIGH-VOLTAGE BREAKDOWN
- COMPACT-SURFACE MOUNT
- MULTICHANNEL OPERATION
- 5V OR 15V INPUT OPTIONS

APPLICATIONS

- INDUSTRIAL PROCESS CONTROL EQUIPMENT
- GROUND-LOOP ELIMINATION
- PC-BASED DATA ACQUISITION
- VENDING MACHINES

DESCRIPTION

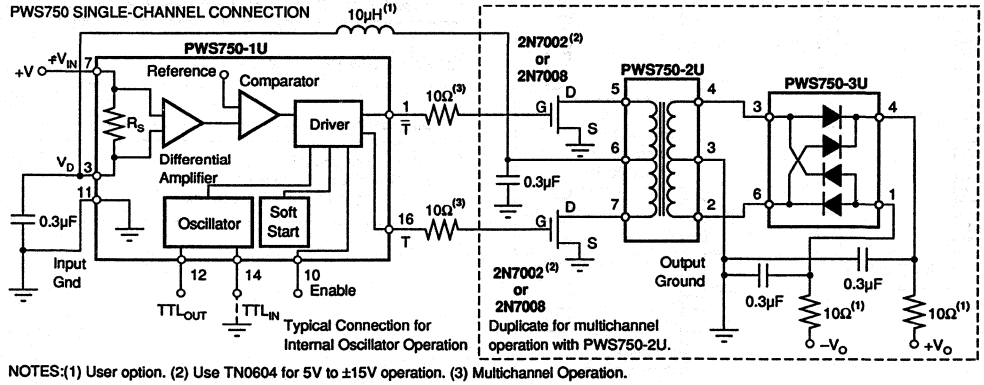
The PWS750 consists of three building blocks for building a low cost DC/DC converter. With them you can optimize DC/DC converter PC board layout or build a multichannel isolated DC/DC converter. All parts are surface mount, requiring minimal space to build the converter. The modular design minimizes the cost of isolated power.

The PWS750-1U is a high-frequency (800kHz nominal) driver that can drive N-channel MOSFETs up to the size of a 1.3A 2N7010. The recommended MOSFET for individual transformer drivers is the 2N7008. The PWS750-1U is supplied in a 16-pin double-wide SO package.

The PWS750-2U and PWS750-4U are split-bobbin wound isolation transformers using a ferrite core. They are encapsulated in plastic packages, allowing a high isolation voltage rating.

The PWS750-3U is a high-speed monolithic diode bridge in a plastic 8-pin SO package.

One PWS750-1U can be used to drive up to four channels (15V nominal operation). One PWS750-2U and PWS750-3U and two 2N7002 (surface mount) or 2N7008 (TO-92) MOSFETs made by Siliconix are used per isolated channel. When a PWS750-4U is used as the transformer (5V input), then two TN0604s made by Supertex must be used, due to the higher currents of the primary (lower RDS on) and the lower V_{GS} threshold. With 5V operation only one channel can be directly driven by the PWS750-1U (a simple FET booster circuit can be used for multichannel operation; see Figure 3).



NOTES:(1) User option. (2) Use TN0604 for 5V to ±15V operation. (3) Multichannel Operation.

International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

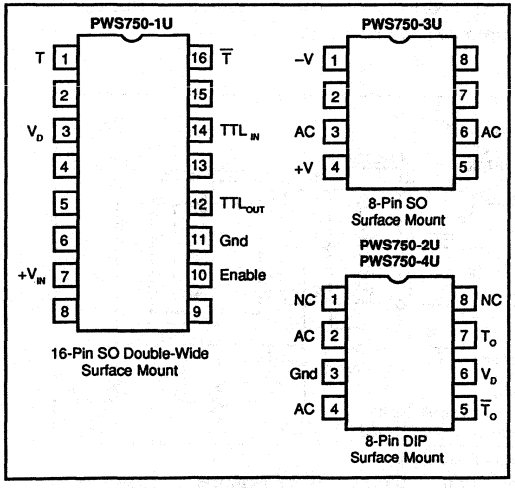
ELECTRICAL

At T_A = 25°C; $+V_{IN}$ = +15V; and I_{OUT} = ±15mA balanced loads unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
PWS750-1U OSCILLATOR					
Frequency: Internal OSC	TTL_{IN} = 0V	725	800	875	kHz
External OSC		1		2.5	MHz
Supply: 15V Operation		10	15	18	V
5V Operation		4.5	5	5.5	V
T, $\overline{T}$ Drive Current				50	mApk
T, $\overline{T}$ Drive Voltage, High		3		7	V
Low				0.7	V
TTL_{IN}, I_{IH}			10		nA
I_{IL}			–1		µA
V_{IH}		2			V
V_{IL}				0.8	V
TTL_{OUT}, I_{OL}				15	mA
PWS750-2U +V_{IN} TO ±V_{OUT} ISOLATION TRANSFORMER					
ISOLATION					
Voltage Rated Continuous AC 60Hz		750			Vrms
100% Test (1)	60Hz, 1s, <5pC PD	1200			Vrms
Barrier Impedance			10^{12} || 8		Ω || pF
Leakage Current at 60Hz	V_{ISO} = 240Vrms		1	1.5	µArms
Winding Ratio	Primary/Secondary		48/48		
PWS750-3U DIODE BRIDGE					
Reverse Recovery	I_F = I_R = 50mA		40		ns
Reverse Breakdown	I_R = 100µA	55			V
Reverse Current	V_R = 40V			1.5	µA
Forward Voltage	I_F = 100mA			1.6	V
PWS750-4U +$5V_{IN}$ to ±$15V_{OUT}$ ISOLATION TRANSFORMER					
ISOLATION					
Voltage Rated Continuous AC 60Hz		750			Vrms
100% Test (1)	60Hz, 1s, <5pC PD	1200			Vrms
Barrier Impedance			10^{12} || 8		Ω || pF
Leakage Current at 60Hz	V_{ISO} = 240Vrms		1	1.5	µArms
Winding Ratio	Primary/Secondary		24/70		
TEMPERATURE RANGE					
Specification		0		+70	°C
Operating	Derated performance	–40		+85	°C
Srorage		–40		+85	°C

NOTES: (1) Tested at 1.6 x rated, fail on 5pC partial discharge leakage current on five successive pulses at 60HZ.

PIN CONFIGURATIONS



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	18V
Junction Temperature	150°C
Storage Temperature	–40°C to +85°C
Lead temperature (soldering, SOIC, 3s)	+260°C
Max Load, Sum of Both Outputs (PWS750-2U, 4U)	60mA

ORDERING INFORMATION

PWS750-XU

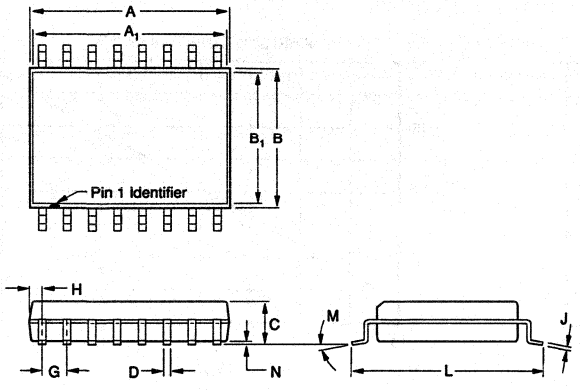
Basic Model Number

Components

1U : High-Frequency Driver
2U, 4U : Isolation Transformer
3U : High-Speed Monolithic Diode Bridge

MECHANICAL

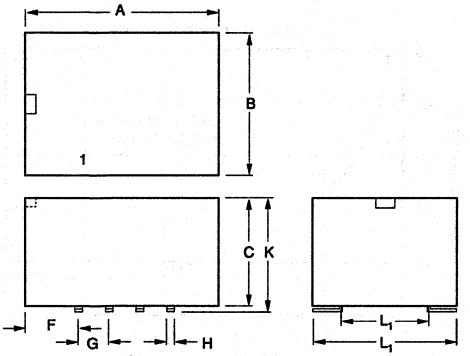
U Package — 16-Pin SOIC



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	.400	.416	10.16	10.57
A1	.388	.412	9.86	10.46
B	.286	.302	7.26	7.67
B1	.268	.286	6.81	7.26
C	.093	.109	2.36	2.77
D	.015	.020	0.38	0.51
G	.0.50 BASIC		1.27 BASIC	
H	.022	.038	0.56	0.97
J	.008	.012	0.20	0.30
L	.391	.421	9.93	10.69
M	5° TYP		5° TYP	
N	.000	.012	0.00	0.30

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

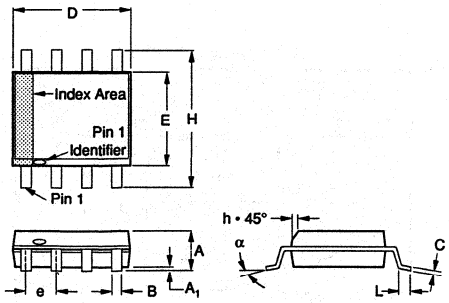
U Package — 8-Pin Plastic DIP



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	.620	.640	15.78	16.26
B	.465	.485	11.81	12.32
C	.350	.370	8.89	9.40
F	.165	.185	4.19	4.70
G	.100 BASIC		2.54 BASIC	
H	.025 SQ		.635 SQ	
K	.370	.390	9.40	9.91
L1	.280	.300	7.11	7.62
L2	.465	.485	11.81	12.32

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.

U Package — 8-Pin SO-8 Surface Mount



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	.054	.068	1.37	1.73
A1	.004	.009	0.10	0.23
B	.014	.019	0.36	0.48
C	.008	.0098	0.20	0.25
D	.189	.196	4.80	4.98
E	.150	.157	3.81	3.99
e	.050 BASIC		1.27 BASIC	
H	.229	.244	5.82	6.20
h	.010	.019	0.25	0.48
L	.016	.050	0.41	1.27
N	8		8	
α	0°	8°	0°	8°

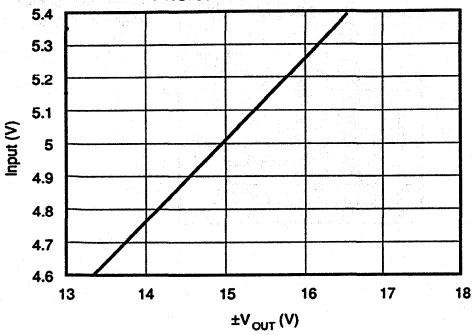
NOTES:
1. Dimensioning and tolerancing per ANSI Y14.5M–1982.
2. "D" and "E" are reference datums and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm (.086 in.)
3. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the cross-hatched area.
4. "L" is the length of the terminal for soldering to a substrate.
5. "N" is the number of terminal positions.

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

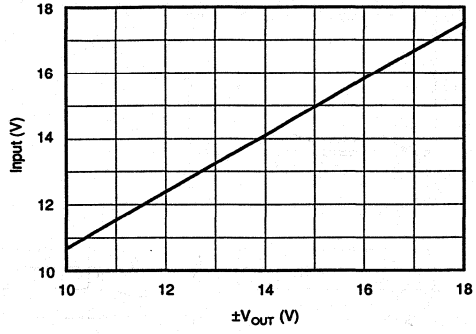
TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_{IN} = 15VDC, I_{LOAD} = ±15mA unless otherwise noted.

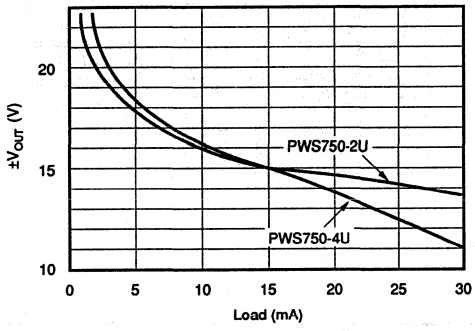
PWS750-4U LINE REGULATION



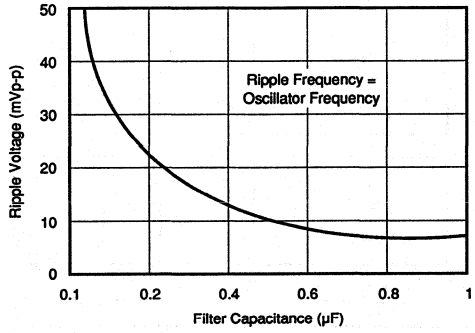
PWR750-2U LINE REGULATION



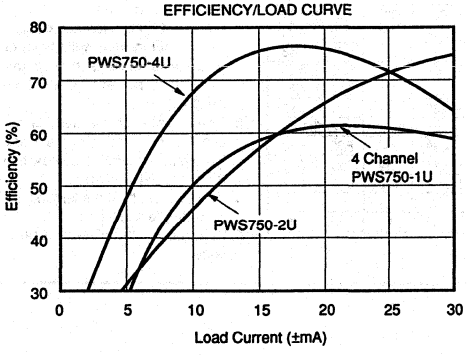
PWR750-2U AND PWS70-4U LOAD LINES



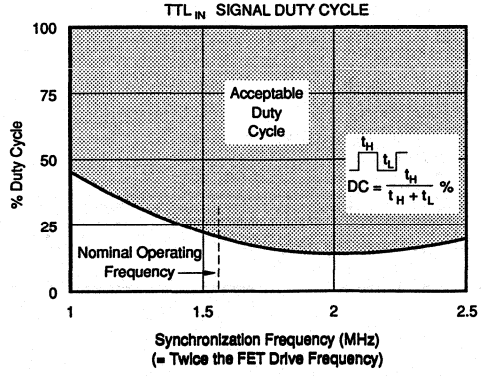
OUTPUT RIPPLE VOLTAGE



EFFICIENCY/LOAD CURVE



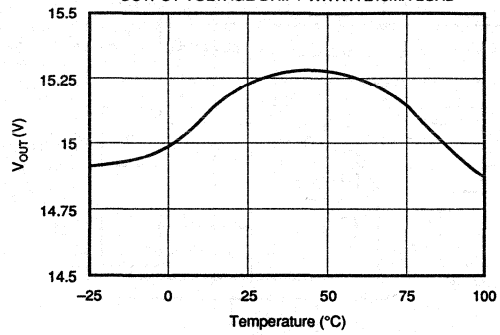
TTL$_{IN}$ SIGNAL DUTY CYCLE



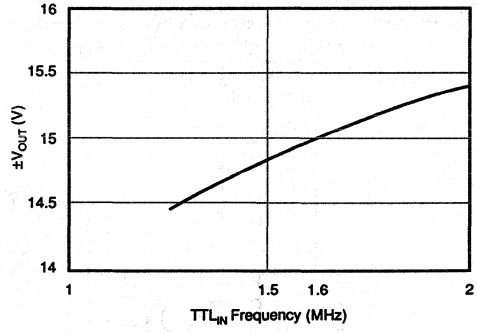
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_{IN} = 15VDC, I_{LOAD} = ±15mA unless otherwise noted.

OUTPUT VOLTAGE DRIFT WITH A ±15mA LOAD



THE OUTPUT VOLTAGE CAN BE ADJUSTED ±3% BY VARYING THE DRIVER FREQUENCY



THEORY OF OPERATION

The PWS750 components are basic building blocks to be used with other standard components to build an isolated push-pull DC/DC converter. The oscillator runs at 800kHz nominal, making it possible to reduce the size of the transformer and lower the output ripple voltage.

PWS750-1U OSCILLATOR PIN FUNCTIONS

TTL_{IN} is used to control the driver frequency with an external TTL level frequency source. The input frequency must be twice the desired driver frequency, since there is an internal divide-by-2 circuit to produce a 50% duty cycle output. The input duty cycle can vary from 12% to 95% (see Typical Performance Curves). When in the free running mode, the TTL_{IN} pin must be tied to ground.

TTL_{OUT} is used when it is desired to synchronize the outputs of multiple PWS750-1Us to minimize beat frequency problems. A standard open collector output is provided, therefore a 330Ω to 3.3kΩ pull-up resistor will be necessary depending on stray capacitance on the sync line. A maximum of eight PWS750-1Us can be connected without the use of an external TTL buffer.

An Enable pin is provided so that the driver (T, $\overline{T}$) can be shut down to minimize power use if required. A TTL low applied to the pin will shut down the driver within one cycle. A TTL high will enable the driver within one cycle. The TTL_{OUT} will still have an 800kHz signal when a master driver is disabled, so other synchronized drivers will not be shut down. The pin can be left open for normal operation.

The $+V_{IN}$ pin supplies power to the oscillator. The V_D pin connects the power to the transformer through the internal overcurrent sense resistor. The other end of the overcurrent sense resistor is tied to $+V_{IN}$. A 0.3µF bypass capacitor must be connected to the V_D pin to reduce the ripple current through the shunt resistor; otherwise false current limit conditions can occur due to ripple voltage peaks.

During overload conditions the output drive shuts off for approximately 80µs, then turns back on for 20µs, resulting in a 25% power up duty cycle. If the overload condition still exists, then the output will shut off again. When the fault or the excessive load is removed, the converter resumes normal operation.

The T and $\overline{T}$ pins are the complementary FET drive outputs and are tied directly to the corresponding FET gate. The connection must be as short as possible. For multiple channel operation they cannot be located above any ground or power planes, because capacitive loading will not allow fast enough charging of the FET gate.

PWS750-2U AND PWS750-4U TRANSFORMER PIN FUNCTIONS

On the primary side the V_D pin of the PWS750-2U is tied directly to the V_D pin of the PWS750-1U. Remember to place a 0.1µF capacitor as close to the PWS750-2U V_D pin as possible. The T_O and $\overline{T}_O$ pins are connected to the drains of the corresponding FETs, whose sources are connected to ground. On the secondary side of the transformer, the Gnd pin is tied directly to the isolated ground. AC pins are 800kHz square wave signals at twice the output voltage, and are connected directly to the corresponding pin on the PWS750-3U. Pins 2 and 4 can be interchanged for ease of hook up. The connection to the diode bridge must be as direct as possible to minimize radiated noise.

The winding ratio for the PWS750-2U is 1:1. This means that the output would normally be less than the input due to voltage drops in the FETs, transformer and diode bridge. Since the DC/DC converter is operating at 800kHz, the transformer is starting to operate close to the resonant frequency, which causes the output to increase in magnitude.

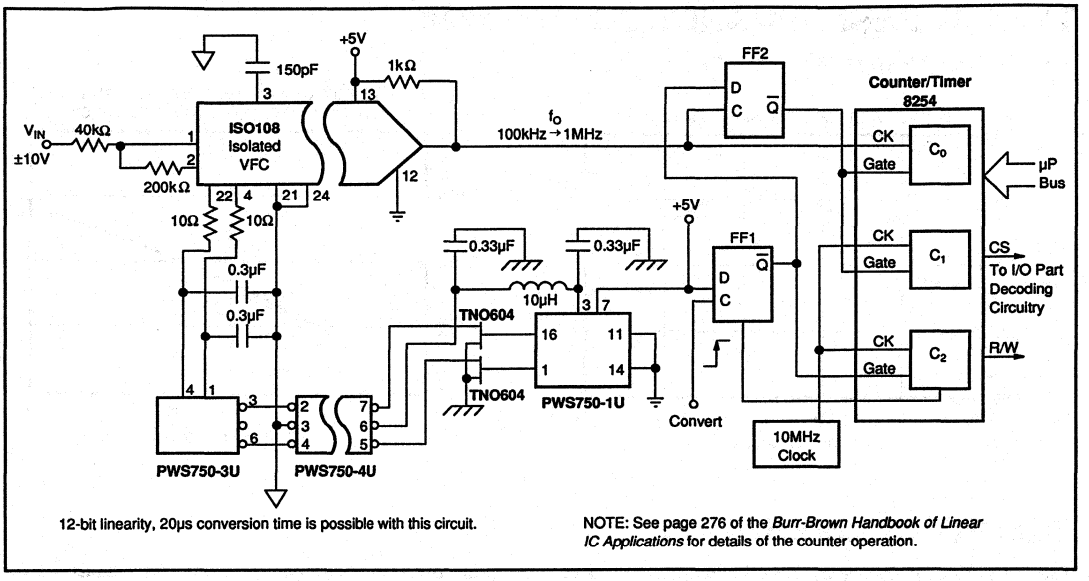


FIGURE 1. Isolated Integrating A/D Conversion System Using Ratiometric Counting and Microprocessor Interface.

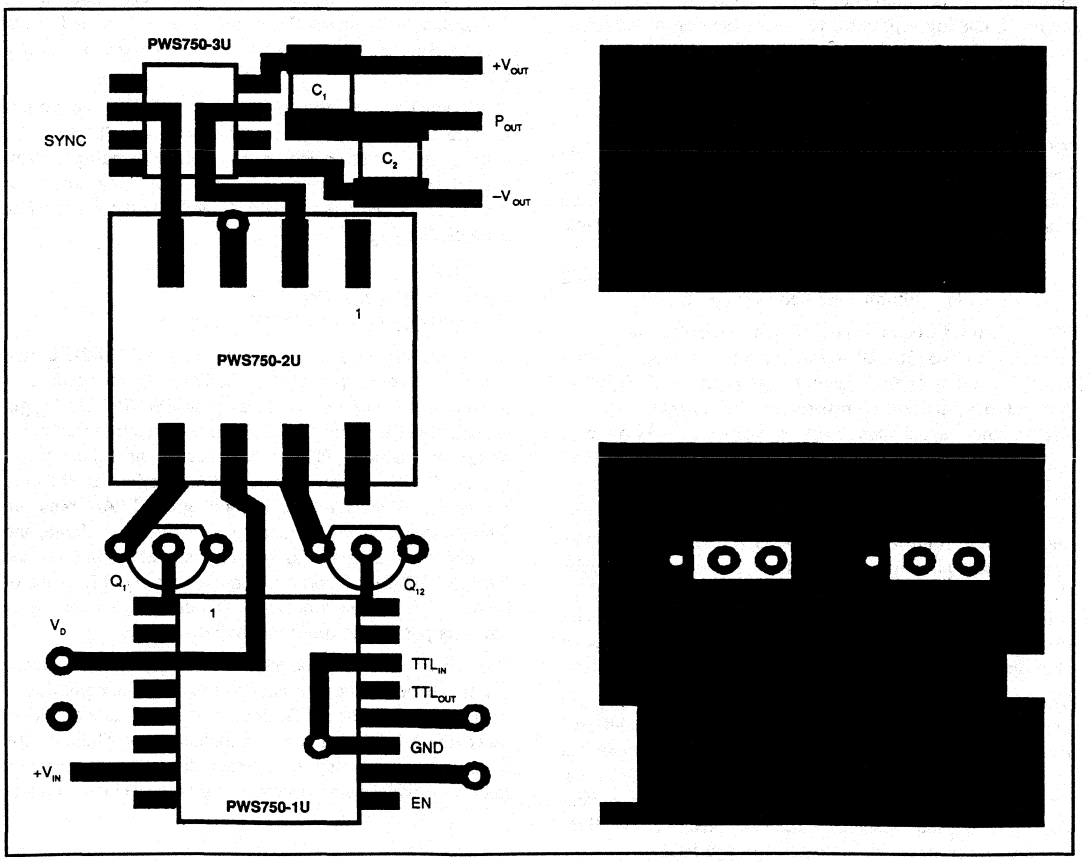


FIGURE 2. Sample PC Board Layout, 4:1.

PWS750-3U HIGH SPEED DIODE BRIDGE PIN FUNCTIONS

The AC pins are tied directly to the AC pins of the PWS750-2U. The +V and –V pins are rectified output voltages. The filter capacitors must be located as close as possible to these pins to minimize series inductance and therefore noise. Bypass capacitors will be needed at each device in the circuit.

BASIC OPERATION

SINGLE CHANNEL OPERATION, PC BOARD LAYOUT CONSIDERATIONS

A simple two-layer board can be used on single channel applications to create a DC/DC converter with low radiated noise. A ground plane should be located directly under both the input and the output components for optimum ground return paths. The surface mount components make it easy to design with a ground plane. The output filter capacitors should be located as close to the PWS750-3U as possible. A sample layout is shown in Figure 2.

For multiple channel applications, T and $\overline{T}$ traces must have minimum capacitive loading. Therefore, there should be no ground plane (or power plane) under these two traces. The driver signal is a 4-6V low current 800kHz signal, which will generate little radiated noise if the traces are kept short.

To minimize the noise pickup for sensitive 12-bit resolution circuits, place a 10Ω resistor in series with the isolated power traces. The resistor, in conjunction with the bypass capacitor, acts as a low pass filter to minimize isolation amplifier PSRR-related ripple voltage feedthrough. A pi filter with a 10µH inductor can also be used at the input ($+V_{IN}$) to minimize input supply ripple current; see Figure 1.

MULTIPLE CHANNEL OPERATION

The oscillator can drive up to four-channels (eight FETs) directly when operating at 10-18V. A 10Ω resistor must be placed in series with T and $\overline{T}$ to stabilize the FET gate charging. For more than four-channel operation, or 5V-multiple-channel operation, the driver circuit needs a FET booster circuit, as shown in Figure 3. Large gate drive surge currents (>100mA) are needed to turn on the gates.

If the total output current drawn by all the channels exceeds 250mA, then it will be necessary to circumvent the current limit circuit by leaving the V_D pin of the PWS750-1U open, and connect the V_D pin of the PWS750-2U directly to the supply.

5V OPERATION

With 5V operation, the transformer winding current ratio is 3:1, therefore generating much greater currents in the primary. The input ripple voltage will be larger, so an input pi filter will be necessary to isolate the converter noise from the rest of the circuit. For example, when the output is ±15mA the input current will be at least 120mA.

MOSFET	MAX DRIVE CURRENT	PACKAGE	BREAKDOWN
TN0604	4A	TO-92	40V
2N7002	115mA	SO-T23	60V
2N7008	500mA	TO-92	60V
2N7010	1.3A	TO-237	60V
2N7012	1.2A	4-Pin DIP	60V

TABLE 1. MOSFET Selector Guide.

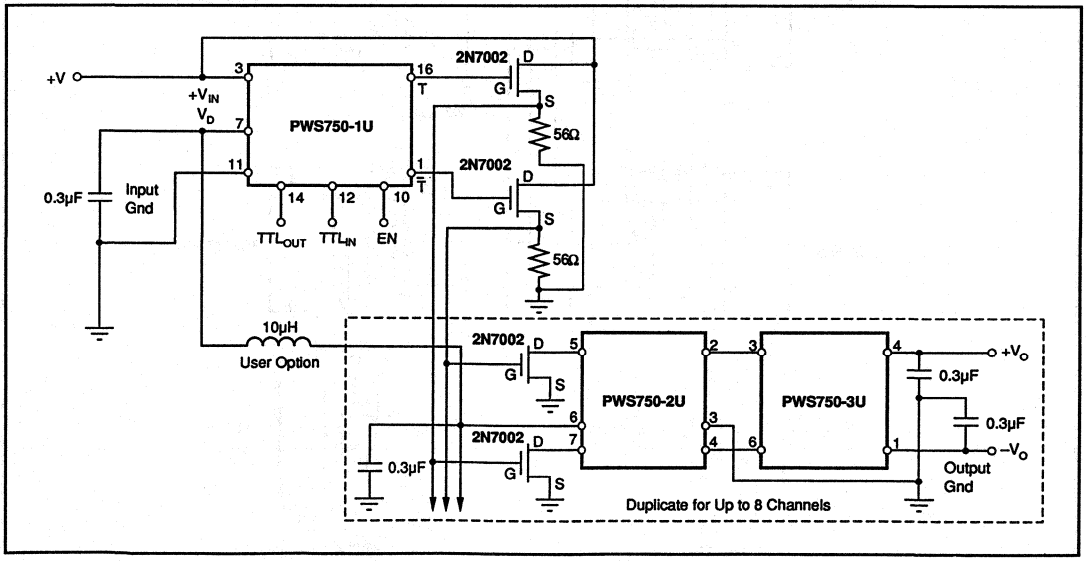


FIGURE 3. MOSFET Driver Booster Circuits.

OUTPUT CURRENT RATING

The PWS750-1U oscillator contains soft start circuitry to protect the FETs from high inrush currents during turn on. The internal input current limit is 250mA peak to prevent thermal overload of the MOSFETs. The maximum output rating is ±30mA. Total current, which can be drawn from each isolation channel, is the total of the power being drawn from both the +V and –V outputs. For example, if one output is not used, then maximum current can be drawn from the other output. In all cases the maximum current that can be drawn from any individual channel is:

$$|+I_{OUT}| + |-I_{OUT}| < 60mA$$

It should be noted that many analog circuit functions do not simultaneously draw equal current from both the positive and negative supplies.

When multiple channel operation is used, the maximum current of all channels must be reduced to prevent the overcurrent limit to trip. Alternately, bypass the overcurrent by leaving the V_D pin of the PWS750-1U open and connecting the V_D pin of the PWS750-2U directly to the supply.

HIGH VOLTAGE TESTING

Burr-Brown Corporation has adopted a partial discharge test criterion that conforms to the German VDE0884 optocoupler standard. This method requires that less than 5pC partial discharge crosses the isolation barrier with 1200Vrms 60Hz applied. This criterion confirms transient overvoltage (1.5 x 750Vrms) protection without damage to the PWS750-2U or PWS750-4U. Life test results verify the absence of high voltage breakdown under continuous rated voltage and maximum temperature.

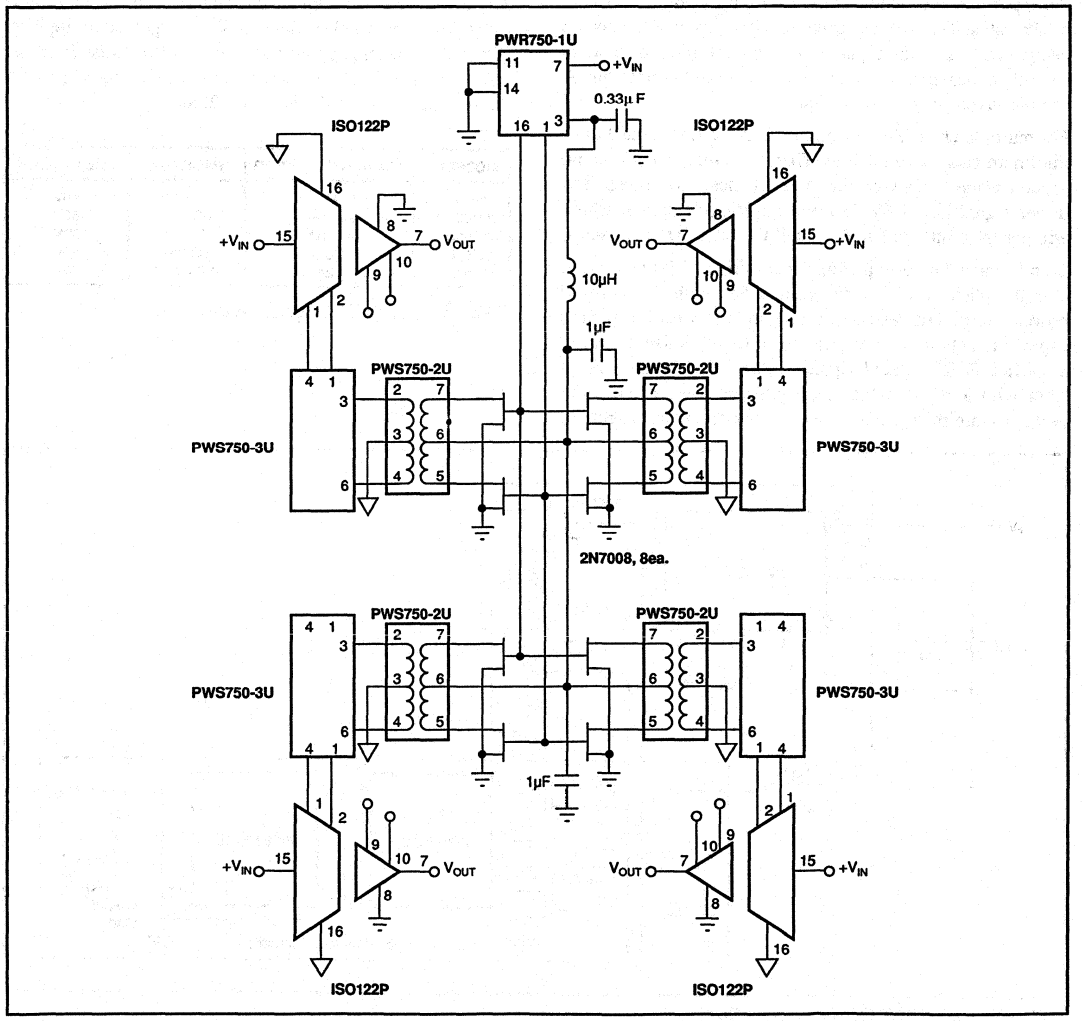


FIGURE 4. Four-Channels of ±10V Signal Isolation with Channel-to-Channel Isolation.

The minimum AC barrier voltage that initiates partial discharge above 5pC is defined as the "inception voltage." Decreasing the barrier voltage to a lower level is required before partial discharge ceases; this is known as "extinction voltage." We have developed a package insulation system to yield an inception voltage greater than 1200Vrms so that transient voltages below this level will not damage the isolation barrier. The extinction voltage is above 750Vrms so that even overvoltage-induced partial discharge will cease once the barrier voltage is reduced to the rated value. Previous high voltage test methods relied on applying a large enough overvoltage (above rating) to break down marginal units, but not so high as to permanently damage good ones. Our partial discharge testing gives us more confidence in barrier reliability than breakdown/no breakdown criteria.

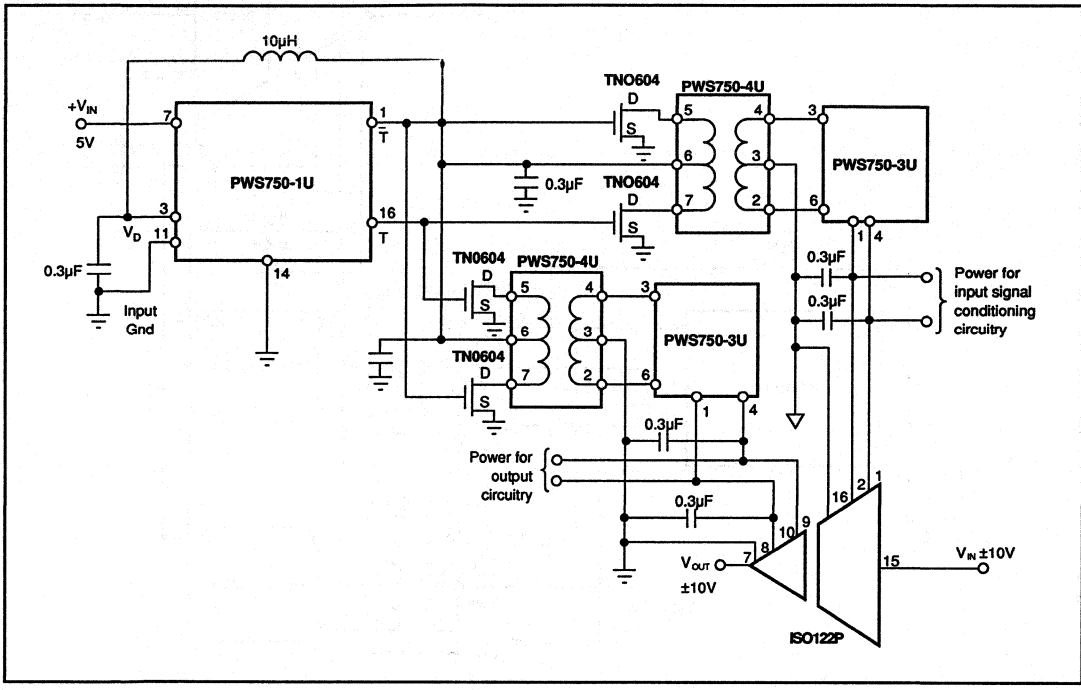


FIGURE 5. A Complete ±10V Signal Acquisition System Operating From a Single 5V Supply.

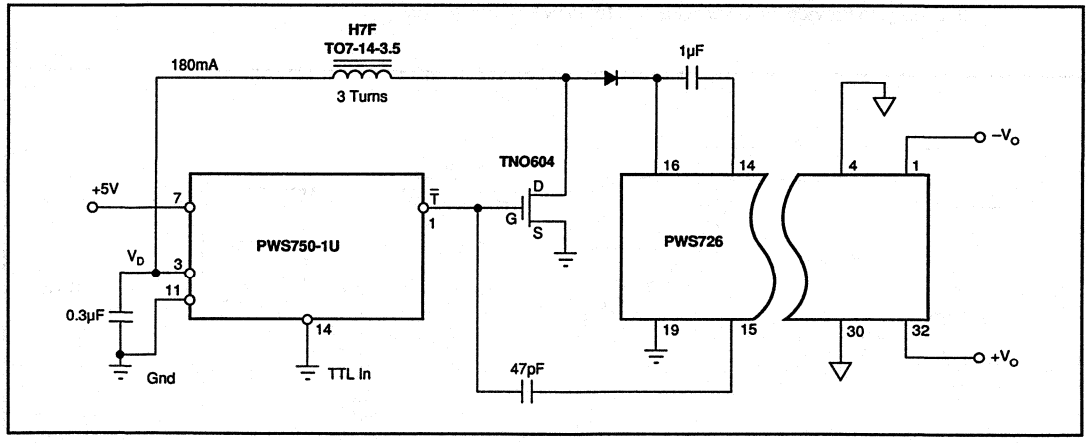


FIGURE 6. A PWS750 Driver Can Be Used to Boost the Input Voltage to 15V to Power a PWS726 From a 5V Supply.

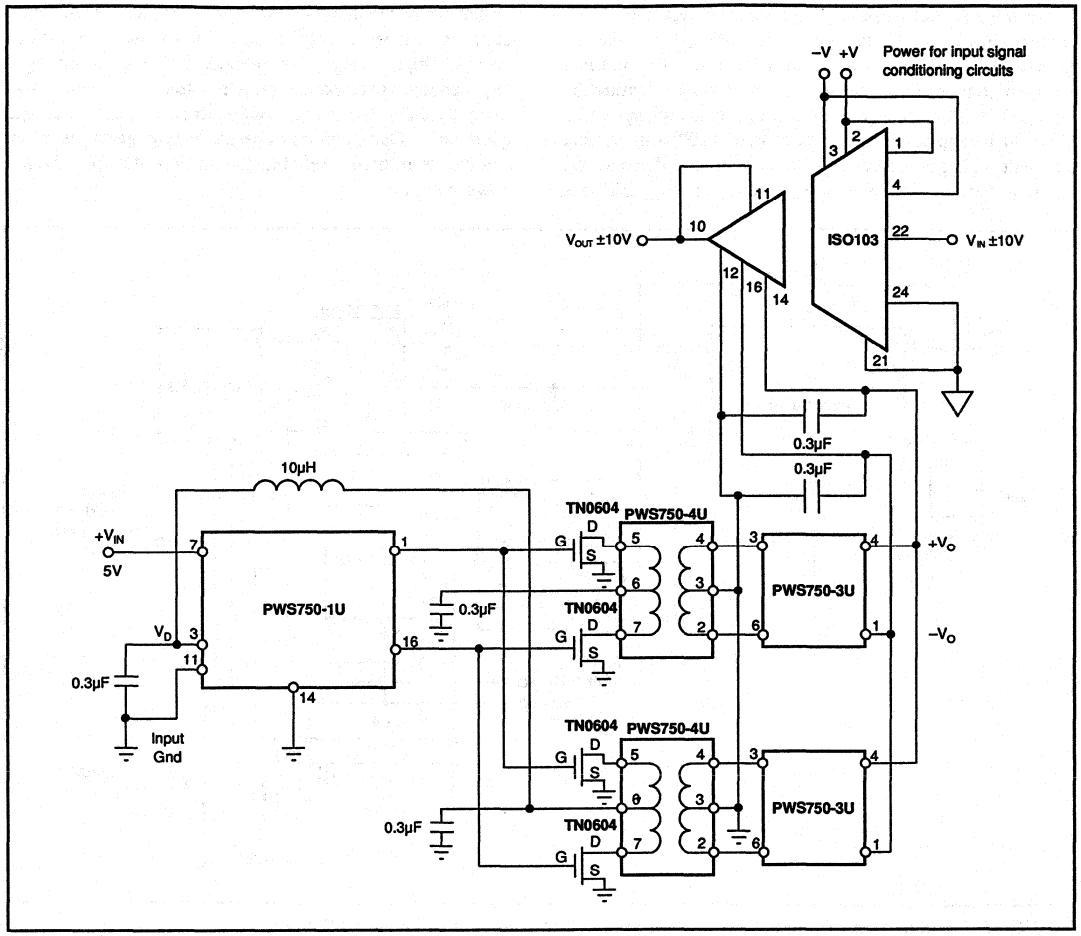


FIGURE 7. Powering the Internally Powered ISO103 Isolation Buffer From a Single 5V Supply. Two Power Channels Are Necessary to Provide the 80mA Nominal for the +V of the ISO103.

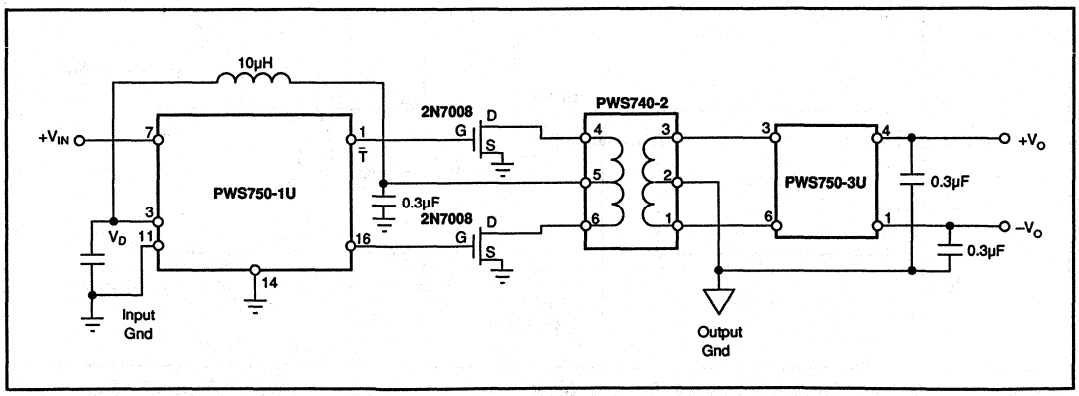


FIGURE 8. 1500VAC Isolation Using PWS740-2 Transformer.

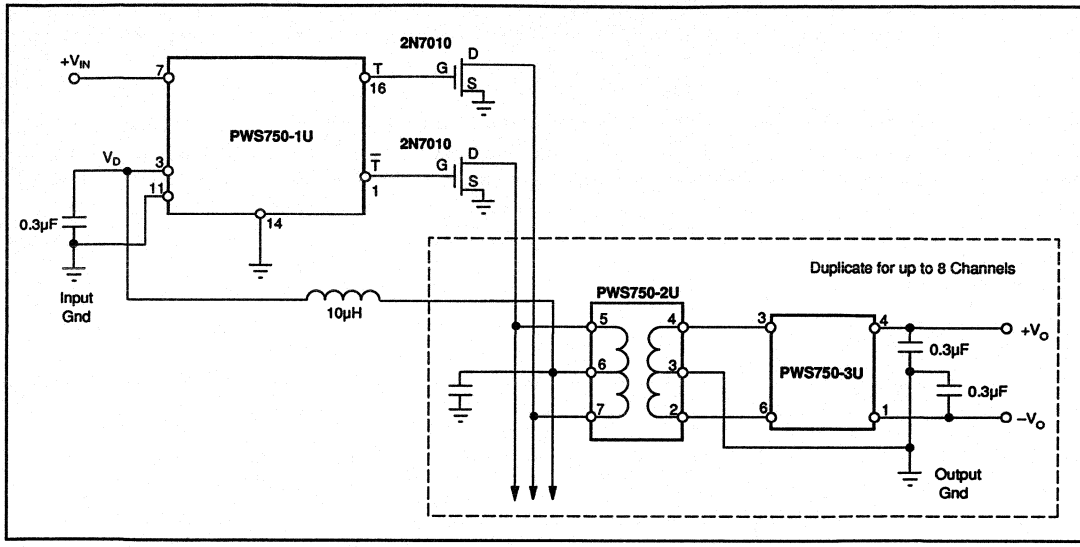


FIGURE 9. FET Pair Driving Up to Eight-Channels.

5 Analog Circuit Functions

Analog circuits act as building blocks with which to perform a variety of instrumentation, computation, and control functions. They provide a broad range of versatile, proven, and ready to use computational functions for the designer to use in developing simple or complex systems. The analog circuit functions include multipliers, dividers, multifunction converters, true rms-to-DC converters, logarithmic amplifiers, voltage and window comparators, peak detectors, precision oscillators, and filters. The multifunction converters also provide multiply, divide, square root, exponentiation, roots, sine, cosine, arctangent, vector magnitude rms-to-DC and logarithmic amplifier functions.

The availability of these relatively complex functions as precise, versatile, easy-to-use, low-cost building blocks has broadened the scope of practical analog circuit systems and greatly simplified analog circuit designs.

The functions are used mostly for processing and/or conditioning of analog signals, and for simulation of algebraic and/or trigonometric analog computations. The variety of applications these functions are effectively used for is limited only by the designer's creative imagination. Some of the interesting applications for which analog circuit functions have found wide acceptance are listed in the table on the following page.

The Selection Guides show parameters for the high grade. Models shown in **boldface** are products included in this supplement.

MULTIPLIERS/DIVIDERS

You can select accuracy from 0.25% max and up from this complete line of integrated circuit multipliers. Most provide full four-quadrant multiplication. All are laser-trimmed for accuracy—no trim pots are needed to meet specified performance. These compact models bring the cost of high performance down to acceptable levels.

MULTIPLIERS/DIVIDERS

Model	Transfer Function	Error at +25°C max (%)	Temp Coeff (%/°C)	Feed-through (mV)	Offset Voltage (mV)	1% BW (kHz)	Temp Range[1]	Pkg	Page No.
MPY100	$[(X_1-X_2)(Y_1-Y_2)/10]+Z_2$	±0.5	0.008	30	7	70	Ind	TO-100	5-26
MPY534	$[(X_1-X_2)(Y_1-Y_2)/10]+Z_2$	±0.25	0.008	0.05%	2	3MHz	Com	TO-100	5-34
MPY600AP	$[(X_1-X_2)(Y_1-Y_2)/2]+Z_2$	**±0.25**	**0.02**	**2**	**5**	**10MHz**	**Ind**	**DIP**	**S-5.27**
MPY634M	$[(X_1-X_2)(Y_1-Y_2)/10]+Z_2$	±0.5	0.015	0.15%	2	10MHz	Ind	TO-100	5-41
MPY634P, U	$[(X_1-X_2)(Y_1-Y_2)/10]+Z_2$	±2.0	0.03	0.3%	25	10MHz	Ind	DIP,SOIC	5-41
AD632	$[(X_1-X_2)(Y_1-Y_2)/10]+Z_2$	±0.5	0.01	0.15	15	50	Mil	TO-100, DIP	5-6

NOTE: (1) Com = 0°C to +70°C, Ind = –25°C to +85°C, Mil = –55°C to +125°C.

SPECIAL FUNCTIONS

This group of models offers many different functions that are the quick, easy way to solve a wide variety of analog computational problems. Most are in integrated circuit packages and are laser-trimmed for excellent accuracy.

SPECIAL FUNCTIONS

Function	Model	Description	Comments	Temp Range[1]	Pkg	Page No.
Multifunction Converter	4302	$Y = (Z/X)^m$ This function may be used to multiply, divide, raise to powers, take roots and form sine and cosine functions.	Plastic Package.	Ind	DIP	5-109
	LOG100	$K \log (I_1/I_2)$	Optimized for log ratio of current inputs. Specified over six decades of input (1nA to 1mA), 55mV total error, 0.25% log conformity.	Com	DIP	5-18
Logarithmic Amplifier	4127G	$K \log (I_1/I_{REF})$	A more versatile part that contains an internal reference and a current inverter. 1% and 0.5% accuracy.	Com	DIP	5-102
$\sqrt{\frac{1}{T}\int_0^T E_{IN}^2(t)dt}$	4341	True rms-to-DC conversion based on a log-antilog occupational approach. Pin compatible with 4340.	Some external trimming required. Lower cost in plastic package.	Ind	DIP	5-115
High Speed Window Comparator, ATE Pin Receiver	**CMP100**	**A dual comparator with high common-mode input range. Latched ECL outputs, ±5V supplies.**	**Propagation delay: 5ns, max for 100mV overdrive**	**Ind**	**DIP, SOIC**	**S-5.16**
Switched Integrator	**ACF2101**	**This is a dual, integrating, transimpedance amplifier that converts an input current to an output voltage by integrating the current for a user determined period of time. Eliminates large feedback resistor of traditional I to V converters.**	**Includes HOLD and RESET switches and output multiplexer.** $V_{OUT} = -\frac{1}{C}\int i_{IN}\,dt$	**Ind**	**DIP, SOIC**	**S-5.4**

NOTE: (1) Com = 0°C to +70°C, Ind = –25°C to +85°C.

DIVIDERS

Using a special log/antilog committed divider design overcomes the major problem encountered when trying to use a multiplier in a divider circuit. Outstanding accuracy is maintained even at very low denominator voltages.

DIVIDERS

Model	Transfer Function	Input Range	Accuracy D = 250mV max (%)	Temp Coeff (%/°C)	0.5% BW (kHz)	Rated Output, min	Temp Range[1]	Pkg	Page No.
DIV100P	10 x N/D	250mV to 10V	0.25	0.2	15	±10V, ±5mA	Com	DIP	5-10

NOTE: (1) Com = 0°C to +70°C.

FREQUENCY PRODUCTS

This group of products consists of precision oscillators and active filters for both signal generation and attenuation. Both fixed frequency and user-selected frequency units are available.

FREQUENCY PRODUCTS

Function	Model	Description	Comments	Temp Range[1]	Pkg	Page No.
Oscillator	4423	Very low cost in plastic package. Provides resistor-programmable quadrature outputs (sine and cosine wave outputs simultaneously available).	Frequency range: 0.002Hz to 20kHz. Frequency stability: 0.01%/°C. Quadrature phase error: ±0.1%.	Com	DIP	5-119
Universal Active Filter	**UAF42** UAF41 UAF21	**These filters provide a complex pole pair. Based on state variable approach, low-pass, high-pass, and bandpass outputs are available.**	**Add only resistors to determine pole location (frequency and Q). Easily cascaded for complex filter responses.**	**Ind** Ind Ind	**DIP** DIP DIP	**S-5.64** 5-82 5-74

NOTE: Com = 0°C to +70°C, Ind = –25°C to +85°C.

VOLTAGE REFERENCE

These products are precision voltage references that provide a +10V output. The output can be adjusted with minimal effect on drift or stability.

VOLTAGE REFERENCE Boldface = NEW

Model	Output (V)	Min Output (mA)	Max Drift (ppm/°C)	Power Supply (V)	Power Supply (mA)	Temp Range[1]	Pkg	Page No.
REF10M	±10.00 ±0.005	10	1	+13.5/35	4.5	Com	TO-99	5-49
REF101M	±10.00 ±0.005	10	1	+13.5/35	4.5	Com	TO-99	5-55
REF102M	**±10.00 ±0.0025**	**10**	**2.5**	**+11.4/36**	**1.4**	**Ind, Mil**	**TO-99**	**S-5.39**
REF102P, U	**±10.00 ±0.005**	**10**	**5**	**+11.4/36**	**1.4**	**Ind**	**DIP, SOIC**	**S-5.39**

NOTE: (1) Com = 0°C to +70°C. Ind = –25°C to +85°C, Mil = –55°C to +125°C.

CURRENT REFERENCE

Model	Output I (μA)	Max Drift Compliance	(ppm/°C)	Comments	Temp Range[1]	Pkg	Page No.
REF200P, U	**Dual 100 ±0.5**	**2.5V to 40V**	**25**	**Includes 0.5% accurate current mirror**	**Ind**	**DIP, SOIC**	**S-5.48 S-5.48**

NOTE: (1) Ind = –25°C to +85°C.

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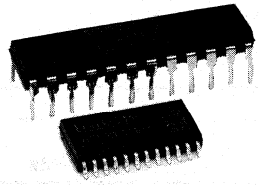


ACF2101

Low Noise, Dual SWITCHED INTEGRATOR

FEATURES

- INCLUDES INTEGRATION CAPACITOR, RESET AND HOLD SWITCHES, AND OUTPUT MULTIPLEXER
- LOW NOISE: 10μVrms
- LOW CHARGE TRANSFER: 0.1pC
- WIDE DYNAMIC RANGE: 120dB
- LOW BIAS CURRENT: 100fA

APPLICATIONS

- CURRENT TO VOLTAGE CONVERSION
- PHOTODIODE INTEGRATOR
- CURRENT MEASUREMENT
- CHARGE MEASUREMENT
- CT SCANNER FRONT END
- MEDICAL, SCIENTIFIC, AND INDUSTRIAL INSTRUMENTATION

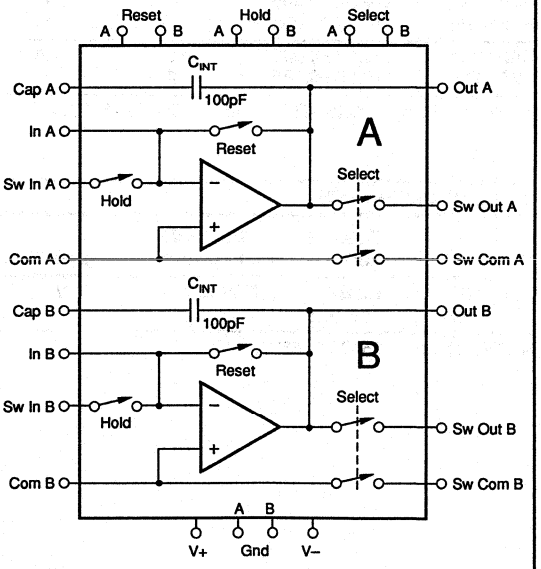
DESCRIPTION

The ACF2101 is a dual switched integrator for precision applications. Each channel can convert an input current to an output voltage by integration, using either an internal or external capacitor. Included on the chip are precision 100pF integration capacitors, hold and reset switches, and output multiplexers.

As a complete circuit on a single chip, the ACF2101 eliminates many of the problems commonly encountered in discrete designs, such as leakage current errors and noise pickup. The integrating approach can provide lower noise than conventional transimpedance amplifier designs and also eliminates the need for high performance, high value feedback resistors.

The extremely low bias current and low noise of the ACF2101's ***Difet***® amplifiers, along with active laser trimming of both offset and drift, assure precision current to voltage conversion.

Although designed for +5V, –15V supplies, the ACF2101 can be operated on supplies up to ±18VDC. It is available in both 24-pin plastic DIP and SOIC packages.



Difet® Burr-Brown Corp.

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Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

PDS-1078

SPECIFICATIONS

ELECTRICAL

At T_A = +25°C, V+ = +5V, V– = –15V, Internal C_{INT} = 100pF, unless otherwise noted.

PARAMETER	CONDITIONS	ACF2101BP, BU MIN	TYP	MAX	UNITS
ANALOG INPUT					
INPUT RANGE					
Input Current Range					
Switched Input (Sw In A, Sw In B)				±100	µA
Direct Input (In A, In B)				±100	µA
INPUT IMPEDANCE					
Switched Input					
Hold Switch OFF			1000		GΩ
Hold Switch ON			1.5		kΩ
Direct Input			Virtual Ground		
HOLD SWITCH VOLTAGE					
Hold Switch Withstand Voltage	Hold Switch OFF	–10		+0.5	V
OFFSET VOLTAGE					
Input Offset Voltage			±0.5	±2	mV
Average Drift			±1	±5	µV/°C
DIGITAL INPUTS					
Logic Family	TTL Compatible				
V_{IH} (Logic 1 = Switch OFF)		2		5.5	V
V_{IL} (Logic 0 = Switch ON)		–0.5		0.8	V
I_{IH}	V_{IH} = +5V		2		µA
I_{IL}	V_{IL} = 0V		0		µA
Switching Speed (All Switches)					
Switch ON			200		ns
Switch OFF			200		ns
TRANSFER CHARACTERISTICS					
TRANSFER FUNCTION			$V_{OUT} = -\frac{1}{C_{INT}} \int I_{IN} dt$		V
DYNAMIC CHARACTERISTICS					
Integrate Mode					
Slew Rate		1	3		V/µs
Reset Mode					
Slew Rate			3		V/µs
Settling Time to 0.01%FSR[1]	10V Step		5	10	µs
Overload Recovery	Positive or Negative		5		µs
Output Multiplexer (Select Switches)					
Settling Time to 0.01%FSR	C_{LOAD} < 1000pF		6.5		µs
Settling Time to 0.01%FSR	C_{LOAD} < 100pF		2		µs
INTEGRATION CAPACITOR (C_{INT})					
Internal Capacitor					
Value			100		pF
Accuracy			0.5	2	%
Temperature Coefficient		–50	–25	0	ppm/°C
Memory			30	100	ppm of FSR
RESET SWITCH					
Impedance					
Reset OFF			1000		GΩ
Reset ON			1.5		kΩ
MODES OF OPERATION					
Switch	Hold / Reset				
Integrate Mode	ON / OFF				
Hold Mode	OFF / OFF				
Reset Mode	ON/OFF / ON				
(Logic 1 = OFF, Logic 0 = ON)					

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

ELECTRICAL (CONT)

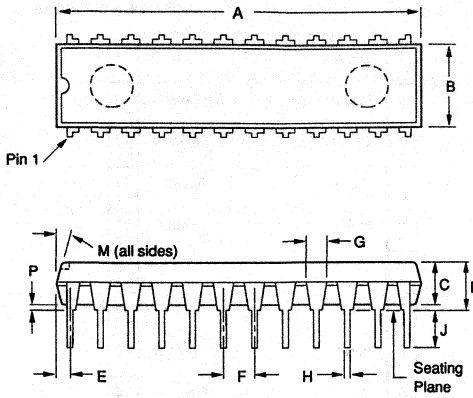
At T_A = +25°C, V+ = +5V, V– = –15V, internal C_{INT} = 100pF, unless otherwise noted.

PARAMETER	CONDITIONS	ACF2101BP, BU MIN	ACF2101BP, BU TYP	ACF2101BP, BU MAX	UNITS
OUTPUT					
Voltage Output Range (All Outputs)		–10	–13.5, +1.0	+0.5	V
Current Output, Direct Output (Out A, Out B)		±5			mA
Short Circuit Current					
Direct Output			±25		mA
Switched Output (Sw Out A, Sw Out B)		±2	±8		mA
Select Switch Withstand Voltage					
Switched Output		–10		+0.5	V
Switched Common (Sw Com A, Sw Com B)		–0.5		+0.5	V
Output Impedance					
Direct Output			0.1		Ω
Switched Output					
Select Switch ON			250 ‖ 5		Ω ‖ pF
Select Switch OFF			1000 ‖ 4		GΩ ‖ pF
Leakage Current	Select Switch OFF		10	100	pA
Load Capacitance Stability					
Direct Output			500		pF
Switched Output			Any		pF
OUTPUT ACCURACY					
Nonlinearity			±0.005	±0.01	%FSR
Channel Separation			–80		dB
Op Amp Bias Current					
Value			100	1000	fA
Temperature Coefficient			Doubles Each +10°C		
Hold Mode Droop			1	10	nV/µs
Integrate Mode Droop			1	10	nV/µs
Voltage Offset[2]					
Value			3		mV
Temperature Coefficient			5		µV/°C
Power Supply Rejection	V_S = +4.5V to +18V, –10V to –18V	80	100		dB
OUTPUT NOISE					
Total Output Noise[3]	BW = 0.1Hz to 10Hz		2		µVrms
Integrate Mode[4]	BW = 0.1Hz to 250kHz		$10(1 + C_{IN}/C_{INT})$		µVrms
Hold Mode	BW = 0.1Hz to 250kHz		10		µVrms
Reset Mode	BW = 0.1Hz to 250kHz		10		µVrms
CHARGE TRANSFER ERRORS[5]					
Reset to Integrate Mode[6]					
Charge Transfer			0.1	0.5	pC
Charge Transfer TC			0.2		fC/°C
Charge Offset Error			1	5	mV
Charge Offset TC			2		µV/°C
Integrate to Hold Mode	C_{IN} > 50pF				
Charge Transfer			0.2	1	pC
Charge Transfer TC			0.4		fC/°C
Charge Offset Error			2	10	mV
Charge Offset TC			4		µV/°C
Hold to Integrate Mode	C_{IN} > 50pF				
Charge Transfer			0.2	1	pC
Charge Transfer TC			0.4		fC/°C
Charge Offset Error			2	10	mV
Charge Offset TC			4		µV/°C
POWER SUPPLY					
Specified Operating Voltage			+5, –15		V
Operating Voltage Range					
Positive Supply		+4.5		+18	V
Negative Supply		–10		–18	V
Current					
Positive Supply	For Dual		12	15	mA
Negative Supply	For Dual		3	4	mA
TEMPERATURE RANGE					
Specification		–40		+85	°C
Operation		–40		+125	°C
Storage		–40		+125	°C
Thermal Resistance (both packages)	Junction to Ambient		100		°C/W

NOTES: (1) FSR is Full Scale Range = 10V (0 to –10V). (2) Includes offset errors from all modes of operation. (3) Total noise is rms total of noise for the modes of operation used. (4) C_{IN} = capacitance of sensor connected to ACF2101 input; C_{INT} = integration capacitance. (5) Errors created when the internal switches are driven from one mode to another. (6) The charge transfer is 0.1pC; for an integration capacitance of 100pF, the resultant charge offset voltage error is 1mV.

MECHANICAL

P Package — 24-Pin Single Wide Plastic DIP

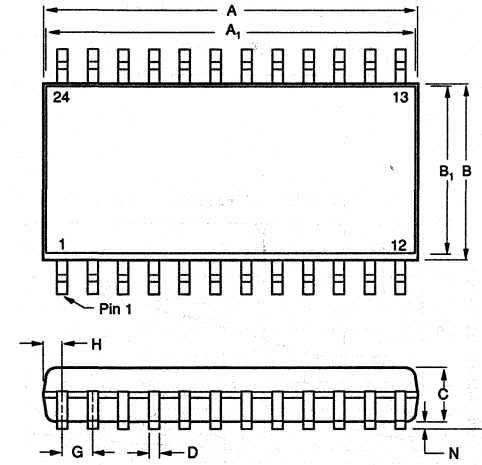


DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.125	1.255	28.58	31.88
B	.250	.290	6.35	7.37
C	—	—	—	—
D	.150	.170	3.81	4.32
E	.010	.080	0.25	2.03
F	.100 BASIC		2.54 BASIC	
G	.050	.070	1.27	1.78

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
H	.016	.020	0.41	0.51
J	.125	N/A	3.18	N/A
K	.300 BASIC		7.62 BASIC	
L	—	—	—	—
M	0°	15°	0°	15°
N	.008	.015	0.20	0.38
P	.010	.030	0.25	0.76

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only.

U Package — 24-Pin SOIC



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.602	.618	15.29	15.70
A1	.595	.618	15.11	15.70
B	.286	.302	7.26	7.67
B1	.270	.285	6.86	7.24
C	.093	.108	2.36	2.74
D	.015	.019	0.38	0.48
G	.050 BASIC		1.27 BASIC	
H	.026	.034	0.66	0.86
J	.008	.012	0.20	0.30
L	.390	.422	9.91	10.72
M	0°	10°	0°	10°
N	.000	.012	0.00	0.30

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only.

NOTE: DIP and SOIC package have different pinouts.

ABSOLUTE MAXIMUM RATINGS

Supply	±18V
Input Current	±5mA
Output Short Circuit Duration	Continuous to Ground
Power Dissipation	500mW
Operating Temperature	–40°C to +125°C
Storage Temperature	–40°C to +125°C
Junction Temperature	+150°C
Lead Temperature (soldering, 10s)	+300°C

ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE
ACF2101BP	Plastic DIP	–40°C to +85°C
ACF2101BU	Plastic SOIC	–40°C to +85°C

PIN CONFIGURATION
DIP and SOIC package have different pinouts.

Top View — ACF210IBU-SOIC Pinout

SOIC

1	Sw In B	Sw In A	24
2	In B	In A	23
3	Cap B	Cap A	22
4	Com B	Com A	21
5	Gnd B	Gnd A	20
6	Out B	Out A	19
7	Sw Out B	Sw Out A	18
8	Sw Com B	Sw Com A	17
9	Select B	Select A	16
10	Reset B	Reset A	15
11	Hold B	Hold A	14
12	V–	V+	13

Top View — ACF210IBP-DIP Pinout

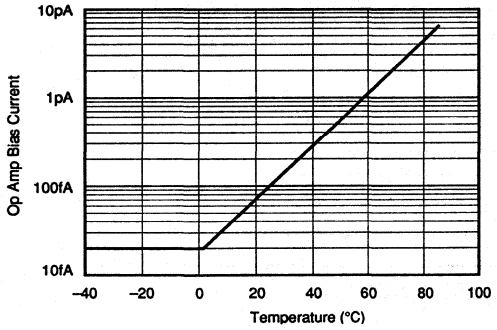
DIP

1	Out A	Sw Out A	24
2	Gnd A	Sw Com A	23
3	Com A	Select A	22
4	Cap A	Reset A	21
5	In A	Hold A	20
6	Sw In A	V+	19
7	Sw In B	V–	18
8	In B	Hold B	17
9	Cap B	Reset B	16
10	Com B	Select B	15
11	Gnd B	Sw Com B	14
12	Out B	Sw Out B	13

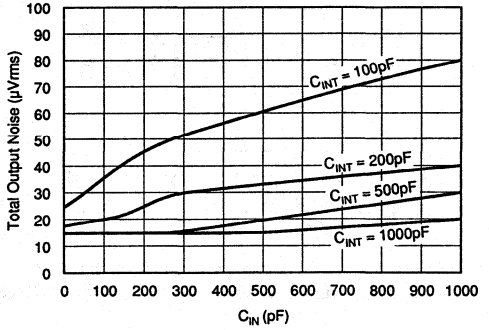
TYPICAL PERFORMANCE CURVES

At T_A = +25°C, V+ = +5V, V– = –15V, C_{INT} = 100pF, unless otherwise noted.

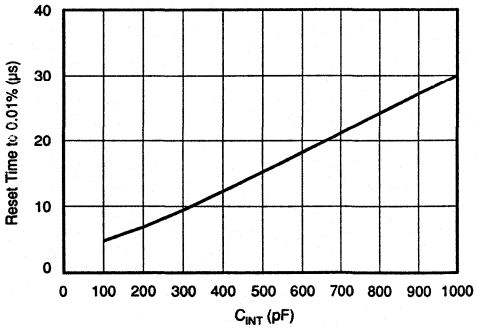
BIAS CURRENT vs TEMPERATURE



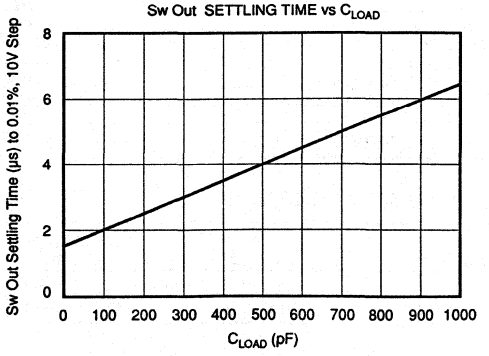
TOTAL OUTPUT NOISE vs C_{IN} and C_{INT}



RESET TIME vs C_{INT}



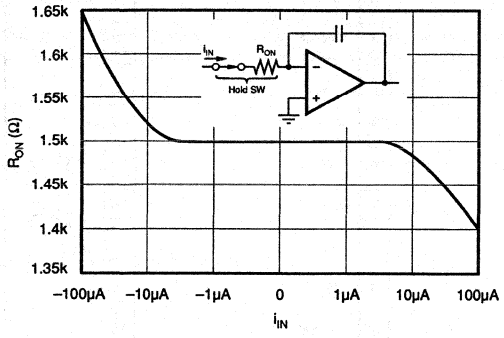
Sw Out SETTLING TIME vs C_{LOAD}



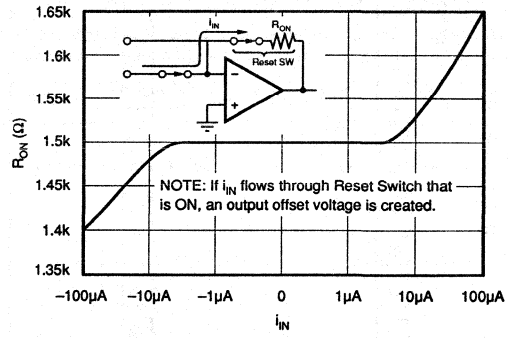
TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C, V+ = +5V, V– = –15V, C_{INT} = 100pF, unless otherwise noted.

HOLD SWITCH R_{ON} vs INPUT CURRENT



RESET SWITCH R_{ON} vs INPUT CURRENT



ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

APPLICATIONS INFORMATION

BASIC CIRCUIT CONNECTION

Basic Layout

As with any precision circuit, careful layout will ensure best performance. Make short, direct interconnections and avoid stray wiring capacitance—especially at the analog and digital input pins.

Figures 1a and 1b illustrate the basic connections needed for operation. Figures 1c and 1d illustrate the addition of external integration capacitors and input guards.

Leakage currents between printed circuit board traces can easily exceed the input bias current of the ACF2101. A circuit board "guard" pattern reduces leakage effects by surrounding critical high impedance input circuitry with a low impedance circuit connection at the same potential. Leakage will flow harmlessly to the low impedance node. Figure 2a and 2b show printed circuit patterns that can be used to guard critical pins. Note that traces leading to these pins should also be guarded.

Improper handling or cleaning may increase droop. Contamination from handling parts and circuit boards can be removed with cleaning solvents and de-ionized water.

Pinout

The pinout for the DIP and SOIC package of the ACF2101 is different. The pinouts for the different packages are shown in several figures in this data sheet.

Power Supplies

The ACF2101 can operate from supplies that range from +4.5V and –10V to ±18V. Since the output voltage integrates negatively from ground, a positive supply of +5V is sufficient to attain specified performance. Using +5V and –15V power supplies reduces power dissipation by one-half of that at ±15V.

Power supply connections should be bypassed with good high-frequency capacitors, such as 1µF solid tantalum capacitors, positioned close to the power supply pins.

MODES OF OPERATION

The three basic modes of operation of each integrator are controlled by the Hold and Reset switches. In Integrate mode, the output voltage integrates negatively toward –10V. In Hold mode, the output voltage remains at the present value, except for output droop. In Reset mode, the integration capacitor is discharged and the output voltage is driven to analog common. See Figure 4.

SWITCHES

Each integrator includes four switches: a Hold switch, a Reset switch, and two output Select switches. See Figure 3.

Hold and Reset Switches

To use the Hold switch, connect the input current to the "Sw In" pin. The Hold switch disconnects the input current, and holds the output voltage at a fixed level. For direct input, connect the input current to the "In" pin that bypasses the

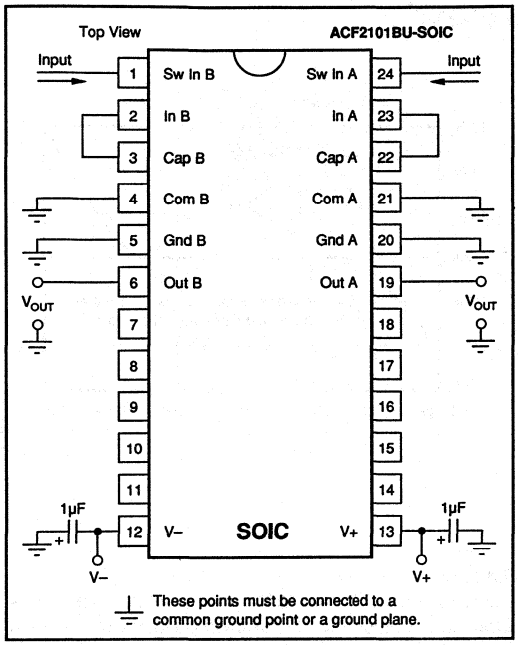


FIGURE 1a. Basic Circuit Connections, **SOIC package.**

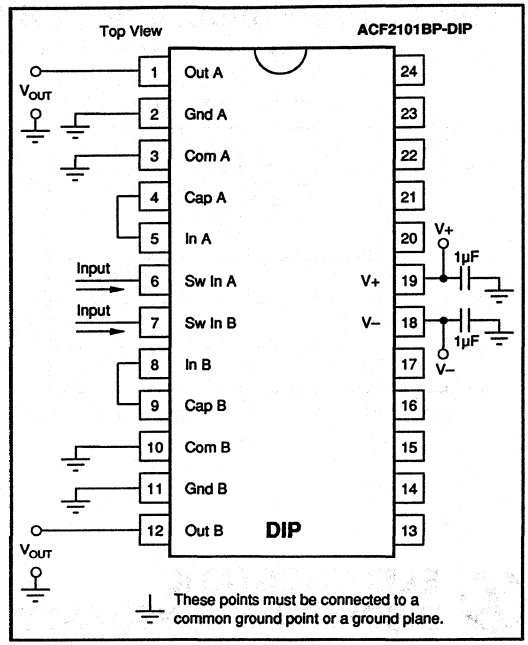


FIGURE 1b. Basic Circuit Connections, **DIP.**

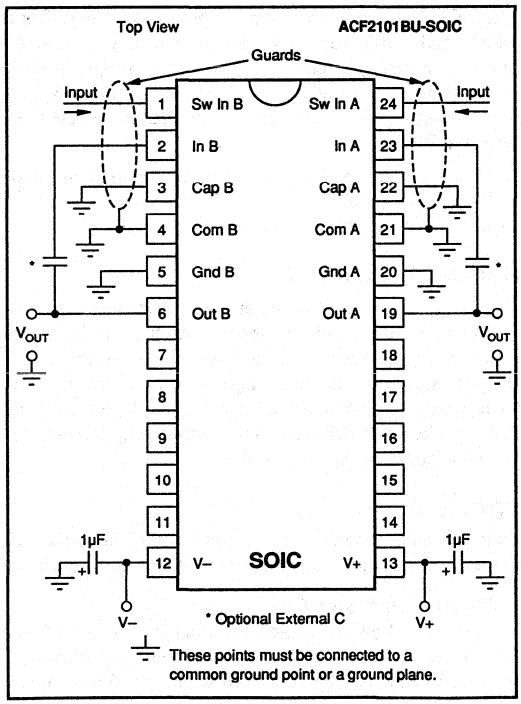


FIGURE 1c. Circuit Connections with External Capacitors and Guarding, **SOIC package.**

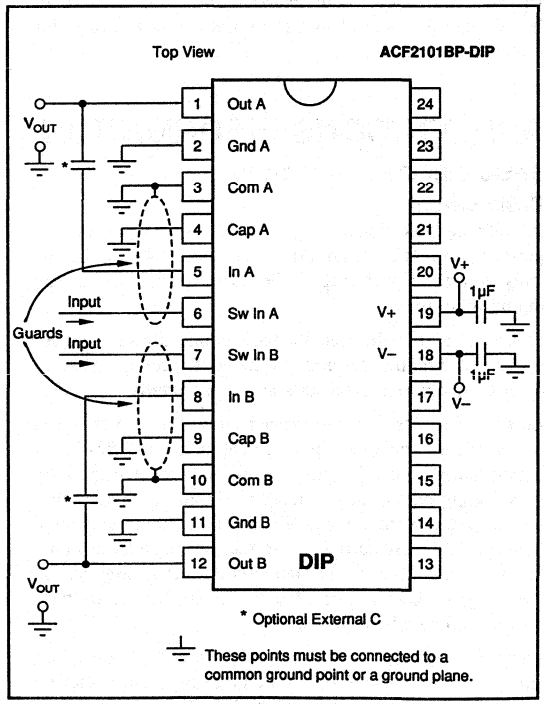


FIGURE 1d. Circuit Connections with External Capacitors and Guarding, **DIP.**

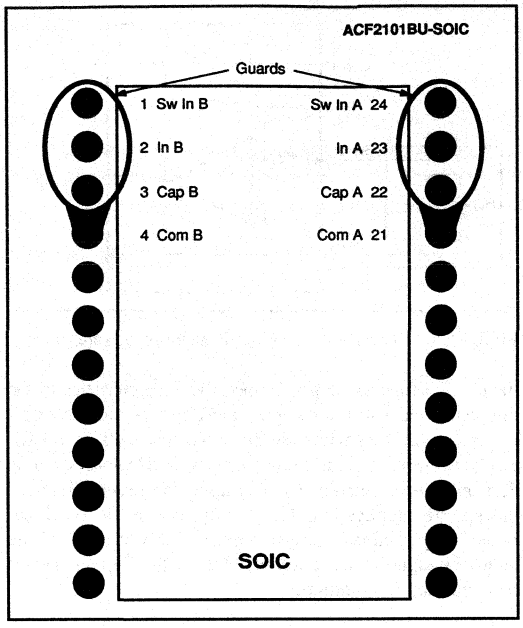


FIGURE 2a. PC Board Layout Showing "Guard" Traces for Input, **SOIC package**. Both top and bottom of board should be guarded.

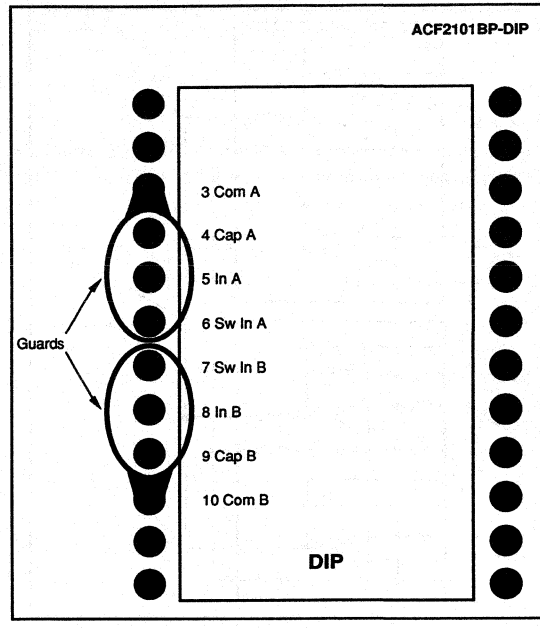


FIGURE 2b. PC Board Layout Showing "Guard" Traces for Input, **DIP**. Both top and bottom of board should be guarded.

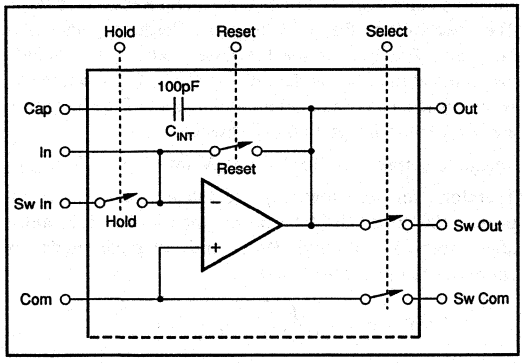
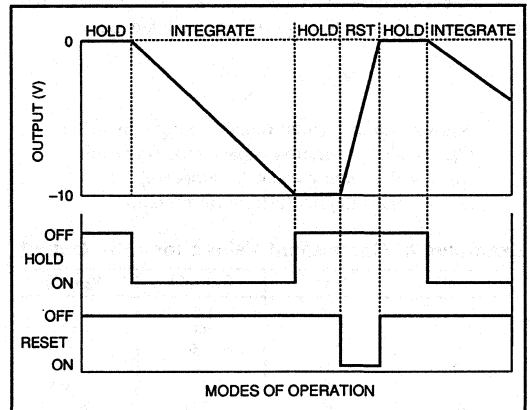


FIGURE 3. Switch Control Lines on One Channel of Two in ACF2101.



SWITCH	MODE OF OPERATION Integrate	Hold	Reset
Hold Switch	ON	OFF	ON/OFF
Reset Switch	OFF	OFF	ON

ON: Switch shorted; Logic 0 input. OFF: Switch open; Logic 1 input.

FIGURE 4. Modes of Operation.

Hold switch and connects directly to the input summing junction. If the Hold switch is not used, the switch should be in the off mode and the "Sw In" pin should be connected to analog common.

The Reset switch is used to discharge the integration capacitor before the start of a new integration period. See Typical Perfomance Curve showing Reset Time vs C_{INT}.

Select Switches

The two Select switches can be used to multiplex the outputs when multiple integrators are connected to a common bus. Figure 5 shows a number of ACF2101s multiplexed together into an A/D converter. The output settling time is determined by the Select switch "on" resistance of 250Ω and the total output capacitance. The total output capacitance includes the ACF2101 output capacitances plus the capacitance of the interconnections to the A/D converter.

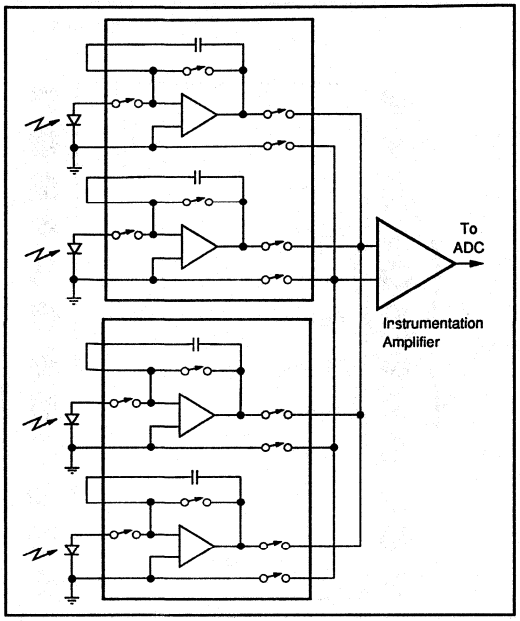


FIGURE 5. ACF2101s in Multiplexed Operation.

OUTPUT VOLTAGE

The integrator output voltage range is from +0.5V to –10V. The output voltage (V_{OUT}) can be calculated as:

$$V_{OUT} = \frac{i_{IN} \times \Delta t}{C_{INT}}$$

V_{OUT} = the maximum output voltage (in volts)
C_{INT} = the integration capacitance (in farads)
i_{IN} = the input current (in amperes)
Δt = the integration time (in seconds)

Examples of Component Values for –10V Output

I_{IN} (μA)	Δt (s)	C_{INT} (pF)	V_{OUT} (V)
0.01	100m	100	–10
0.1	10m	100	–10
1	1m	100	–10
10	100μ	100	–10
100	10μ	100	–10
10	1m	1000	–10
100	100μ	1000	–10

OUTPUT OVERLOAD

When the output to the ACF2101 integrates to the negative limit, the output voltage smoothly limits at approximately 1.5V from the negative power supply, and reset time will increase by approximately 5μs for overload recovery. For fastest reset time avoid integrating to the negative limit.

EXTERNAL CAPACITOR

An external integration capacitor may be used instead of or in addition to the internal 100pF integration capacitor. Since the transfer function depends upon the characteristics of the integration capacitor, it must be carefully selected. An external integration capacitor should have low voltage coefficient, temperature coefficient, memory, and leakage current. The optimum selection depends upon the requirements of the specific application. Suitable types include NPO ceramic, polycarbonate, polystyrene, and silver mica. If the internal integration capacitor is not used, the Cap pin should be connected to common.

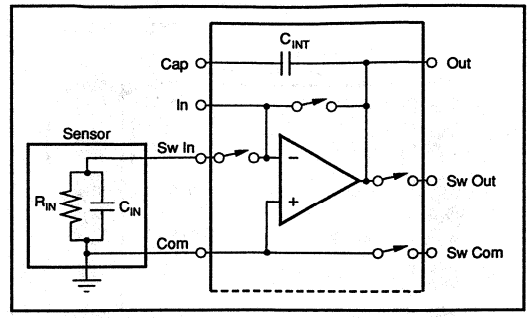


FIGURE 6. Capacitance of Circuit at Input of Integrator.

NOISE

The total output noise for a specific application of the ACF2101 is the rms total of the noise in the modes used: Integrate noise (e_{nI}), Hold noise (e_{nH}) and Reset noise (e_{nR}). The noise in both the Hold (e_{nH}) and Reset (e_{nR}) modes is 10μVrms. The noise in the Integrate mode (e_{nI}) is directly proportional to one plus the ratio of C_{IN} to C_{INT}, where C_{IN} is the capacitance of the circuit at the input of the integrator and C_{INT} is the integration capacitance:

Integrate output noise (e_{nI}) = (10μVrms) x ($1 + C_{IN}/C_{INT}$)

Therefore, for very low C_{IN}, the Integrate noise will approach 10μVrms. The total noise when in the Hold mode after proceeding through Reset and Integrate modes is approximated as shown below.

$$\text{Total Noise} = \sqrt{e_{nI}^2 + e_{nH}^2 + e_{nR}^2}$$

See Typical Performance Curve showing Total Output Noise vs C_{IN} and C_{INT} for more accurate noise data under specific circumstances. If only the Integrate and Reset modes are used, the total noise is the rms sum of the noise of the two modes as shown below.

$$\text{Total Noise} = \sqrt{e_{nI}^2 + e_{nR}^2}$$

DYNAMIC CHARACTERISTICS

Frequency Response

The ACF2101 switched integrator is a sampled system controlled by the sampling frequency (fs), which is usually dominated by the integration time. Input signals above the Nyquist frequency (fs/2) create errors by being aliased into

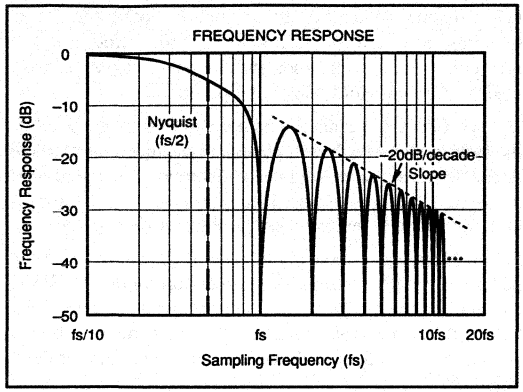


FIGURE 7. Frequency Response.

the sampled frequency bandwidth. The sampled frequency bandwidth of the switched integrator has a –3dB characteristic at fs/2.26 and a null at fs and harmonics 2fs, 3fs, 4fs, etc. This characteristic is often used to eliminate known interference.

Charge Transfer

Charge transfer is the charge that is coupled from the logic control inputs through circuit capacitance to the integration capacitor when the Hold and Reset switches change mode. Careful printed circuit layout must be used to minimize external coupling from digital to analog circuitry and the resulting charge transfer. Charge transfer results in a DC charge offset error voltage. The ACF2101 switches are compensated to reduce charge transfer errors.

Since the ACF2101 switches contribute equal and opposite charge for positive and negative logic input transitions, the total error due to charge transfer is determined by the switching sequence. For each switch, a logic transition results in a specific charge (and offset voltage) while an opposite going logic transition results in an opposite charge (and opposite offset voltage). Thus, if the Hold switch is turned on and off during one integration cycle, the total charge transfer at the end of the sequence due to the Hold switch is essentially zero.

The amount of charge transfer to the integration capacitor is constant for each switch. Therefore, the charge offset error voltage is lower for larger integration capacitors. The ACF2101's 0.1pC charge transfer results in a 1mV charge offset voltage when using the 100pF internal integration capacitor. The offset voltage will change linearly with the integration capacitance. That is, 50pF will result in a 2mV charge offset and 200pF in a 0.5mV charge offset.

Droop

Droop is the change in the output voltage over time as a result of the bias current of the amplifier, leakage of the integration capacitor and leakage of the Reset and Hold switches. Droop occurs in both the Integrate and Hold modes of operation. Careful printed circuit layout must be used to minimize external leakage currents as discussed previously.

The droop is calculated by the equation:

$$\text{Droop} = \frac{100fA}{C_{INT}}$$

where C_{INT} is the integration capacitance in farads and the result is in volts per second. For the internal integration capacitance of 100pF, the droop is calculated as:

$$\text{Droop} = \frac{100 \times 10^{-15}}{100 \times 10^{-12}} = 1\text{mV/s or } 1\text{nV/}\mu\text{s}$$

Droop increases by a factor of 2 for each 10°C increase above 25°C. See the typical performance curve showing Bias Current vs Temperature.

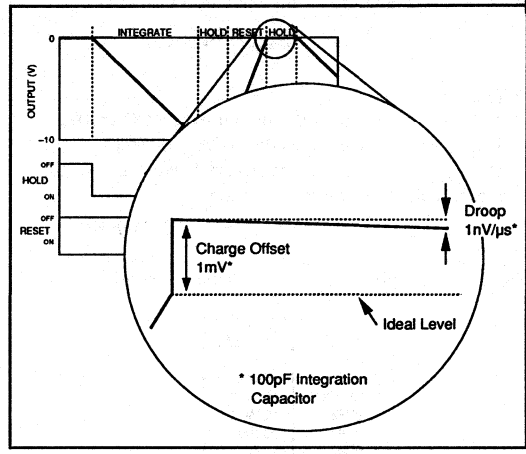


FIGURE 8. Droop and Charge Offset Effects.

Capacitive Loads

Any capacitive load can be safely driven through the multiplexed output of the ACF2101. As with any op amp, however, best dynamic performance of the ACF2101 can be achieved by minimizing the capacitive load. See the typical performance curve showing settling time as a function of capacitive load for more information. A large capacitive load is often useful in reducing the noise of systems not requiring the full bandwidth of the ACF2101.

PROGRAMMABLE I TO V CONVERTER EXAMPLE

Figure 10 illustrates the use of the ACF2101 as a programmable current to voltage converter. The output of the circuit, V_{OUT}, is a DC level for a constant current input. The timing diagram shown in Figure 9 shows V_{OUT} for an input current that varies from one sample to the next. This circuit offers wide dynamic range without the use of extremely large resistors. An ACF2101 and an OPA2107 op amp are configured to convert a low level input current to an output voltage.

The equivalent gain of the converter is determined by the frequency of the digital input signal, f_S. The inherent integrating function of the ACF2101 is very useful for rejection of noise such as power line pickup.

The ACF2101 integrates the current signal for the period of f_S. The magnitude of the ramp voltage at the output of the ACF2101 is a function of the frequency of f_S and the value of the integration capacitor, C_{INT}. The ACF2101's 100pF internal capacitor is used for C_{INT} in this example. The effect is that f_S controls the equivalent feedback resistance of a transconductance (current-to-voltage) amplifier. The equivalent feedback resistance range can vary over a large range of at least 1MΩ to 1GΩ as illustrated in the accompanying table. Larger equivalent feedback resistances can be obtained if internal capacitances smaller than 100pF are used with the ACF2101.

A simplified equation for the operation of this circuit is:

$$V_{OUT} = I_{SENSOR} \times R_{PROGRAM}$$

Where:

V_{OUT} is the voltage at the output of the OPA2107,
I_{SENSOR} is the current into the ACF2101, and
$R_{PROGRAM}$ is the equivalent feedback resistance of the circuit calculated by the equation,

$$R_{PROGRAM} = 1/(f_S \times C_{INT}) = 1/(f_S \times 100pF)$$

For C_{INT} = 100pF, $R_{PROGRAM}$ is calculated below:

f_S	$R_{PROGRAM}$
10kHz	1MΩ
1kHz	10MΩ
100Hz	100MΩ
60Hz	167MΩ
50Hz	200MΩ
10Hz	1GΩ

At the end of the integration cycle, the Hold switch of the ACF2101 is opened to hold a constant value at the output of the ACF2101. The constant value output voltage of the ACF2101 is transferred onto a 10nF capacitor by closing the ACF2101's Select switch. The Select switch is then opened which holds the voltage on the 10nF capacitor during the next integration cycle and creates a DC output. With this operation, the Select switch of the ACF2101 and the 10nF capacitor form a Sample/Hold (S/H) circuit. The OPA2107 is used to buffer the Sample/Hold output. The charge injection of the Select switch creates a small offset voltage, of approximately 1mV in this example. The 10nF capacitor was chosen as a large value to minimize this offset voltage.

After the Select switch opens, the ACF2101 is reset by momentarily closing the Reset switch. The ACF2101's Hold switch is then closed to begin another integration cycle. During the period of time that the Hold switch is open, the input signal current is stored on the input capacitance of the sensor (C_{IN}). During this time, the input signal current creates a voltage across the sensor. This voltage should be kept below 500mV. When the Hold switch is closed, the charge that has collected on C_{IN} will be transferred to the integraintegration cycle ends and the next integration cycle begins when the Hold switch is opened.

If 100% of signal acquisition is not required, or not wanted, the Hold switch may be left closed, or the direct input to the ACF2101 used. In this mode of operation, an integration cycle ends when the Select switch is opened and the next integration cycle begins when the Reset switch is opened.

Figure 11 shows a simple digital pattern generator which can be used to create the timing signals to control the ACF2101 circuit of Figure 10. This circuit creates signals to control the Select, Reset and Hold switches at a rate controlled by the frequency of f_S. Figure 9 shows the timing diagram for these circuits.

In a sampled data system, the output of the ACF2101 at the output of the Select switch can be converted to digital when the ACF2101 is in the Hold mode. In this situation, of course, the 10nF capacitor and the OPA2107 op amp are not required

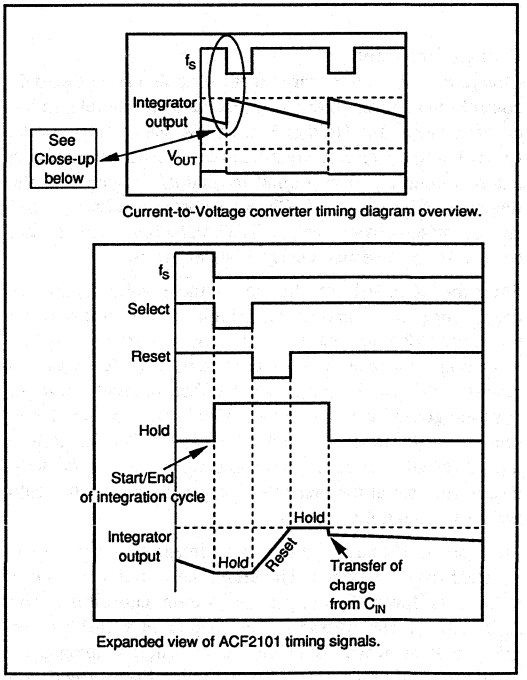


FIGURE 9. ACF2101 Current-to-Voltage Converter Timing Diagram.

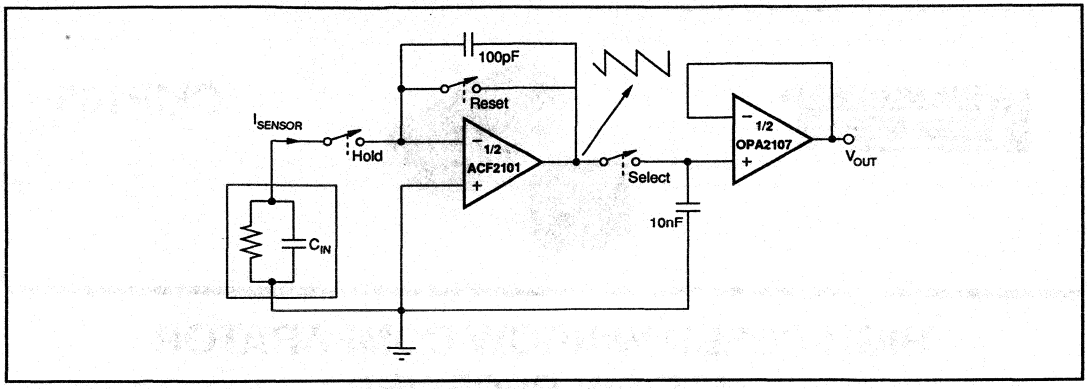


FIGURE 10. Programmable Current-to-Voltage Converter.

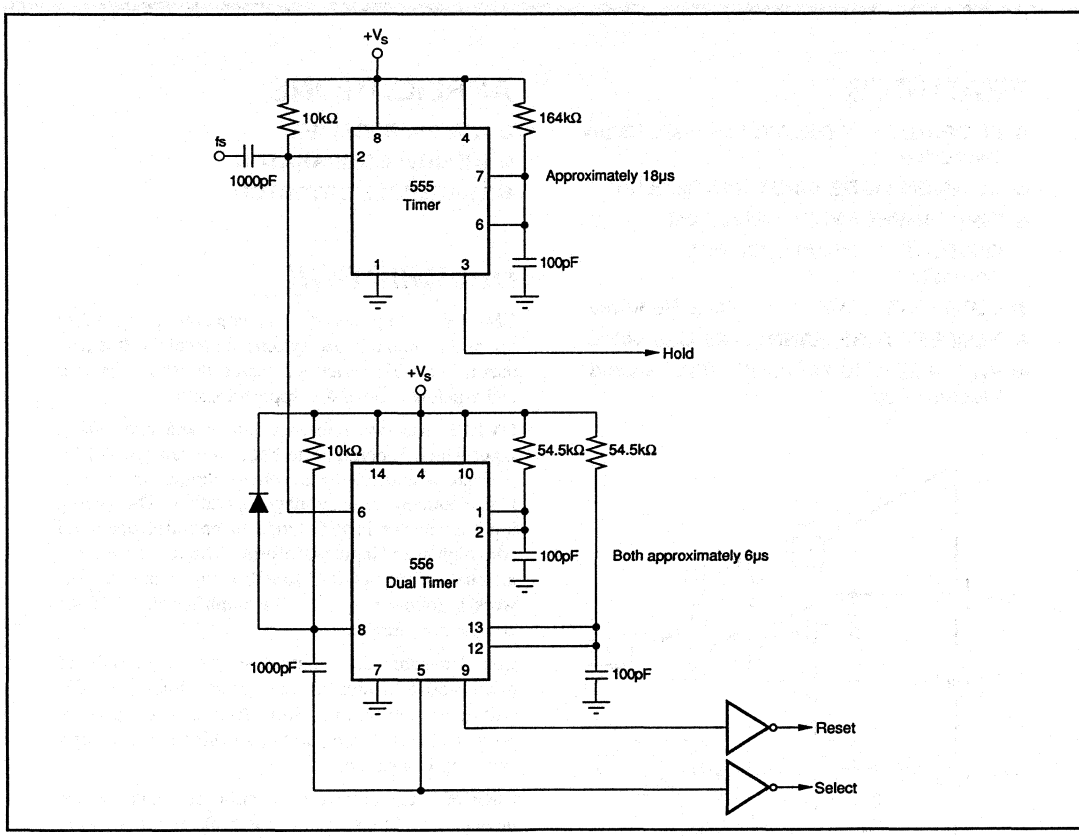


FIGURE 11. Timing Generator.

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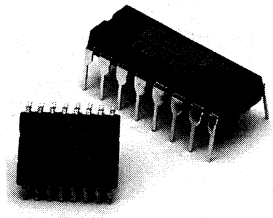
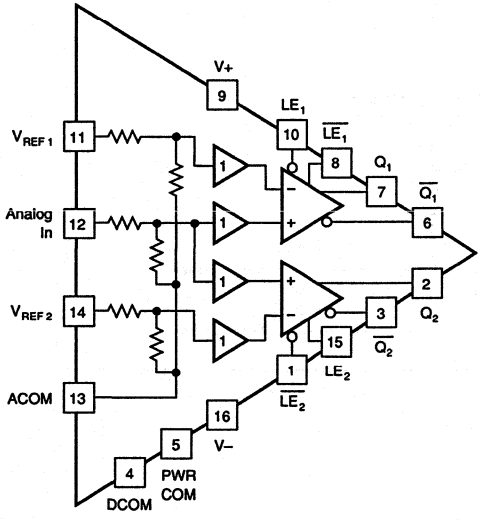


CMP100

HIGH-SPEED WINDOW COMPARATOR ATE PIN RECEIVER

FEATURES

- **PROPAGATION DELAY: 5ns max, 100mV Overdrive**
- **COMMON MODE INPUT RANGE: ±12V**
- **INPUT IMPEDANCE: 120kΩ || 2pF**
- **OUTPUTS: Latchable, 10k ECL Compatible**
- **COMPLETE: No External Parts Required**
- **TEMPERATURE RANGE: –25°C to +85°C**
- **PACKAGES: 16-Pin Plastic DIP, 16-Lead Plastic SOIC**



APPLICATIONS

- **ATE PIN RECEIVER**
- **WINDOW COMPARATOR**
- **THRESHOLD DETECTOR**

DESCRIPTION

CMP100 is a high-speed dual comparator designed for use as an automatic test system pin receiver. It is also useful in a wide variety of analog threshold detector and window comparator applications.

CMP100 has two reference inputs and one analog input which is common to both comparators. All inputs are attenuated by a voltage divider to provide high common mode voltage operation. The analog input attenuator is R-C tuned to optimize operation with high-speed input waveforms. The reference input attenuators are not R-C tuned. Each attenuator network is followed by a buffer amplifier ahead of the comparator circuits.

Complementary ECL output stages are capable of driving 50Ω terminated transmission lines to a –2V pull-down voltage. In addition, latch-enable inputs are provided for each comparator, allowing operation as a sampling comparator.

CMP100 is available as an industrial temperature range device, –25°C to +85°C, and is packaged in a 16-pin plastic DIP and in a 16-lead plastic SOIC.

International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

PDS-1075A

SPECIFICATIONS

ELECTRICAL

T_A = 25°C and at rated supplies: V+ = +5V, V– = –5.2V unless otherwise noted.

PARAMETER	CMP100AP, AU MIN	CMP100AP, AU TYP	CMP100AP, AU MAX	UNITS
ANALOG INPUTS				
Differential Input Voltage Range		24		V
Common Mode Voltage Range		±12		V
Resistance				
Reference Inputs: $V_{REF\,1}$, $V_{REF\,2}$	45	60	75	kΩ
Analog Input	90	120	150	kΩ
Capacitance, All Inputs		2		pF
TRANSFER CHARACTERISTICS				
ACCURACY				
Input Offset Voltage, V_{OS} (1)		10	20	mV
Common Mode Error			10	mV/V
Voltage Offset Drift		100	250	µV/°C
Power Supply Sensitivity of Offset: $\Delta V_{OS}/\Delta V+$			±10	µV/V
$\Delta V_{OS}/\Delta V-$			±10	µV/V
RESPONSE TIME				
Propagation Delay, t_{PD} (2, 3)				
100mV Overdrive, Latch Disabled		3.6	5	ns
DIGITAL SIGNALS (4) (Over Specification Temperature Range)				
Inputs (Latch Controls)				
Logic Levels: V_{IH}	–1.1			V
V_{IL}			–1.5	V
I_{IH} (V_I = –1.1V)			50	µA
I_{IL} (V_I = –1.5V)			5	µA
Outputs (Balanced)				
Logic Levels: V_{OL} (50Ω Load to –2V)			–1.5	V
V_{OH} (50Ω Load to –2V)	–1.1			V
POWER SUPPLY REQUIREMENTS				
Supply Voltage				
V+	+4.75	+5	+5.25	VDC
V–	–5.45	–5.2	–4.95	VDC
Supply Current (5)				
V+		+30	+40	mA
V–		–40	–50	mA
Power Dissipation (6)		360	460	mW
TEMPERATURE RANGE				
Specification	–25		+85	°C
Storage	–65		+150	°C

NOTES: (1) Defined as half the magnitude between low-to-high and high-to-low transition input voltages. (2) See section on "Measuring CMP100 Performance." (3) See "Discussion of Specifications" for exact conditions. (4) 10k ECL compatible. (5) Maximum supply current is specified at typical supply voltages. (6) Maximum Power Dissipation is calculated with typical supply voltages and maximum currents. Note that dissipation in the output transistors from driving 50Ω ECL loads will increase the total power dissipation by about 50mW.

ABSOLUTE MAXIMUM RATINGS

V+ to Digital Common and Power Common ..... +6V
V– to Digital Common and Power Common ..... –6V
(V+) – (V–) 12V
Digital Inputs to Digital Common
  Differential ..... ±4V
  Common Mode ..... V– to V+
Differential Analog Input Voltage ..... ±25V
Package Power Dissipation 750mW
Storage Temperature ..... –60°C to +150°C
Lead Temperature (soldering, 10s) ..... +300°C

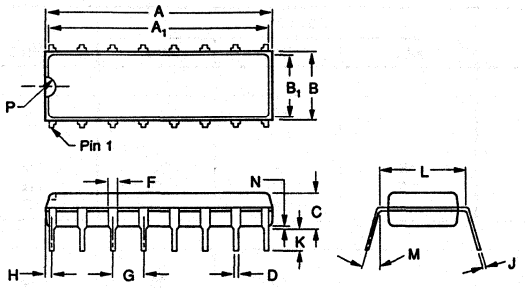
Stresses exceeding those listed above may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN DEFINITIONS

PIN	NAME	DESCRIPTION
1, 15	$\overline{LE2}$, LE2	LATCH or UNLATCH comparator 1 outputs
2, 3	Q2, $\overline{Q2}$	ECL outputs of comparator 2
4	DCOM	Return for comparator circuits
5	PWRCOM	Return for ECL output transistor currents
6, 7	$\overline{Q1}$, Q1	ECL outputs of comparator 1
8, 10	$\overline{LE1}$, LE1	LATCH or UNLATCH comparator 2 outputs
9	V+	Positive Supply Voltage, +5V
11	$V_{REF\,1}$	Reference Voltage for comparator 1
12	Analog In	Analog Signal Input
13	ACOM	Return for Analog In, $V_{REF\,1}$, $V_{REF\,2}$
14	$V_{REF\,2}$	Reference voltage for comparator 2
16	V–	Negative Supply Voltage: (ECL Supply, –5.2V)

MECHANICAL

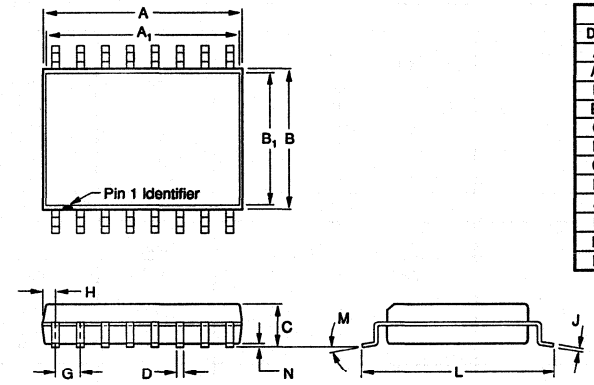
P Package — 16-Pin Plastic DIP



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.740	.800	18.80	20.32
A1	.725	.785	18.42	19.94
B	.230	.290	5.85	7.38
B1	.200	.250	5.09	6.36
C	.120	.200	3.05	5.09
D	.015	.023	0.38	0.59
F	.030	.070	0.76	1.78
G	.100 BASIC		2.54 BASIC	
H	0.20	.050	0.51	1.27
J	.008	.015	0.20	0.38
K	.070	.150	1.78	3.82
L	.300 BASIC		7.63 BASIC	
M	0°	15°	0°	15°
N	.010	.030	0.25	0.76
P	.025	.050	0.64	1.27

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

U Package — 16-Pin SOIC



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.400	.416	10.16	10.57
A1	.388	.412	9.86	10.46
B	.286	.302	7.26	7.67
B1	.268	.286	6.81	7.26
C	.093	.109	2.36	2.77
D	.015	.020	0.38	0.51
G	.050 BASIC		1.27 BASIC	
H	.022	.038	0.56	0.97
J	.008	.012	0.20	0.30
L	.391	.421	9.93	10.69
M	5° TYP		5° TYP	
N	.000	.012	0.00	0.30

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

ORDERING INFORMATION

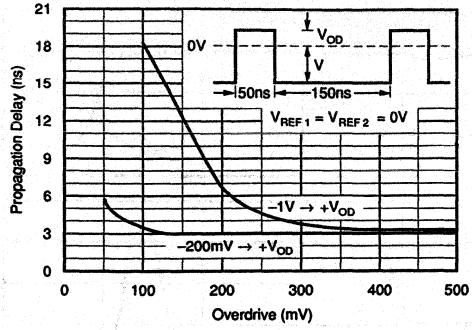
MODEL	PACKAGE
CMP100AP	16-Pin DIP
CMP100AU	16-Lead SOIC

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

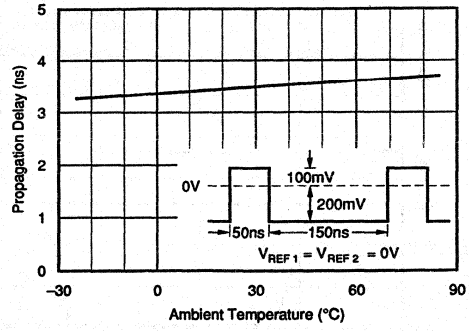
TYPICAL PERFORMANCE CURVES

T_A = 25°C and at rated supplies: V+ = +5V, V– = –5.2V unless otherwise noted.

PROPAGATION DELAY vs OVERDRIVE

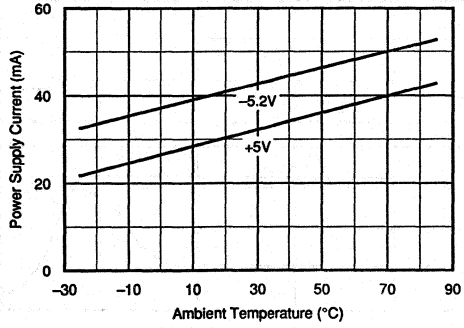


PROPAGATION DELAY vs AMBIENT TEMPERATURE

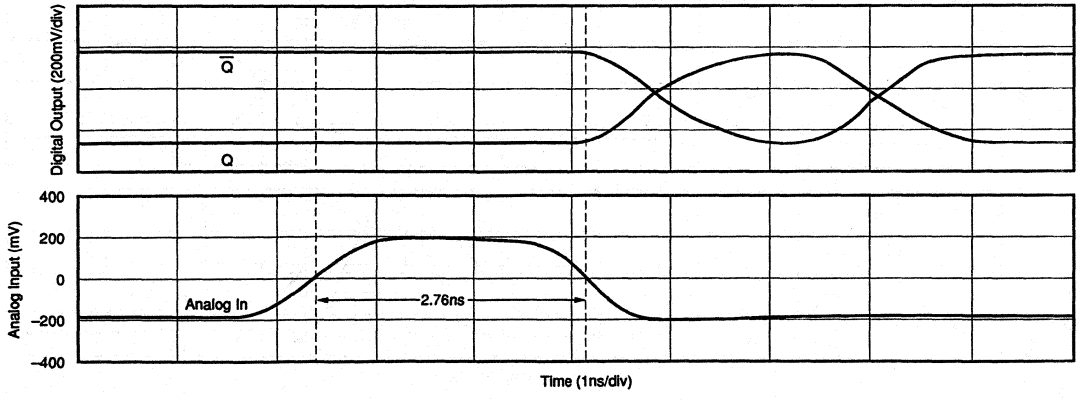


NOTE: Propagation Delay vs Overdrive is shown for two amplitudes of input pulse: from –200mV → $+V_{OD}$ (0.2nV/ns slew rate) and –1V → $+V_{OD}$ (1V/ns slew rate). For an inverse input waveform: from +1V → $–V_{OD}$ and from +200mV → $–V_{OD}$, propagation delays identical to those above are produced.

POWER SUPPLY CURRENT vs AMBIENT TEMPERATURE



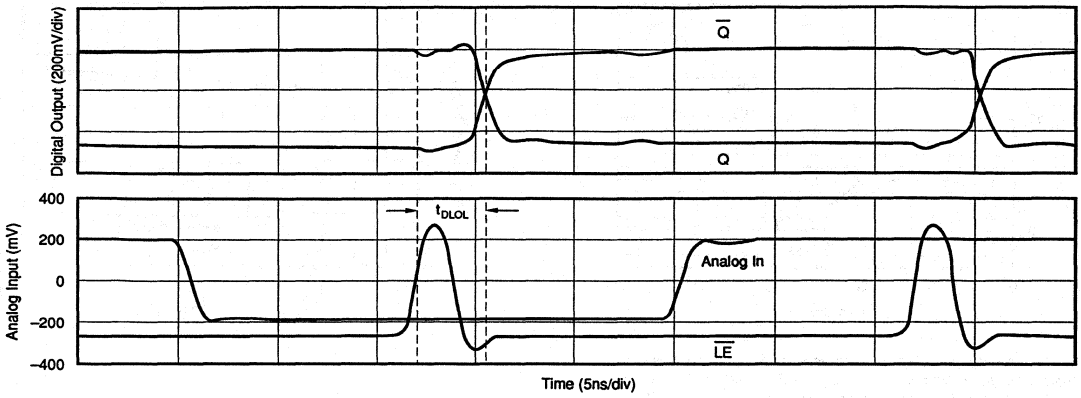
RESPONSE TO A 3ns ANALOG INPUT PULSE



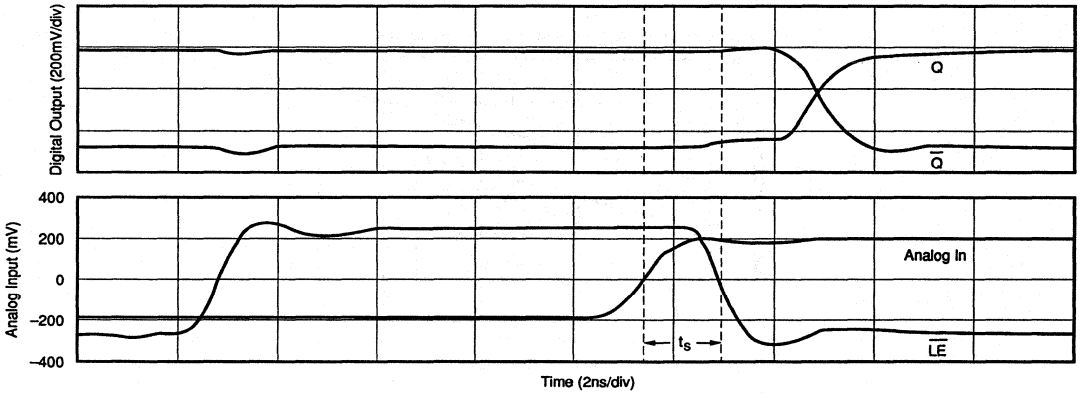
TYPICAL PERFORMANCE CURVES (CONT)

T_A = 25°C and at rated supplies: V+ = +5V, V– = –5.2V unless otherwise noted.

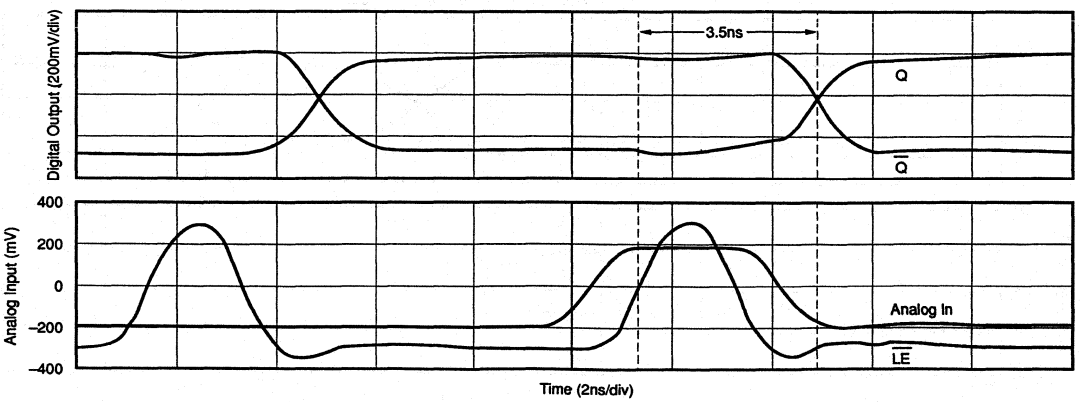
RESPONSE TO A 2ns LATCH ENABLE PULSE



SETUP TIME, t_S



CAPTURING A NARROW ANALOG PULSE



DISCUSSION OF SPECIFICATIONS

ANALOG INPUT

Offset Voltage, V_{OS}

The value of the the comparison threshold for V_{REF1} or V_{REF2} = 0V. V_{OS} and maximum drift vs temperature of V_{OS} are guaranteed.

Common Mode Error

As V_{REF} varies over its range, there is a small gain error which manifests itself as a change in the comparison level. Common mode error drifts typically –15µV/°C.

DYNAMIC PERFORMANCE

Figure 1 illustrates the following analog and logic performance definitions.

Input to Output High Propagation Delay, t_{PDH}

t_{PDH} is the propagation delay measured from the time the input signal crosses the input offset voltage to the 50% point of an output (Q output) Low-to-High transition. Output logic is not latched for this definition.

Input to Output Low Propagation Delay, t_{PDL}

t_{PDL} is the propagation delay measured from the time the input signal crosses the input offset voltage to the 50% point of an output (Q output) High-to-Low transition. Output logic is not latched for this definition.

The propagation delay of the CMP100 is virtually identical for negative going and positive going analog input edges.

Differential Propagation Delay (Skew), t_{DIFF}

t_{DIFF} is the difference in propagation delay from one comparator to another. The skew between each half of one CMP100 is no greater than 200ps.

Propagation Delay Dispersion

Propagation Delay Dispersion is the variation in propagation delay versus input overdrive. Note that propagation delay may also be a function of input slew rate and of the previous level.

The input waveform for the propagation delay specification is illustrated in the first typical performance curve, Propagation Delay vs Overdrive. The Propagation Delay listed in the Electrical Specifications table is specified using an input waveform with 100mV overdrive, a previous level of –200mV and a slew rate of 200V/µs. A typical propagation delay curve is also shown for a previous level of –1V. The outputs are not latched for this specification.

Overdrive

Overdrive is the voltage by which the input exceeds $V_{REF} \pm V_{OS}$.

Minimum Set-Up Time, t_S

t_S is the minimum time before the positive transition of the Latch Enable (LE) that an analog input signal change must be present in order to be acquired and held at the outputs.

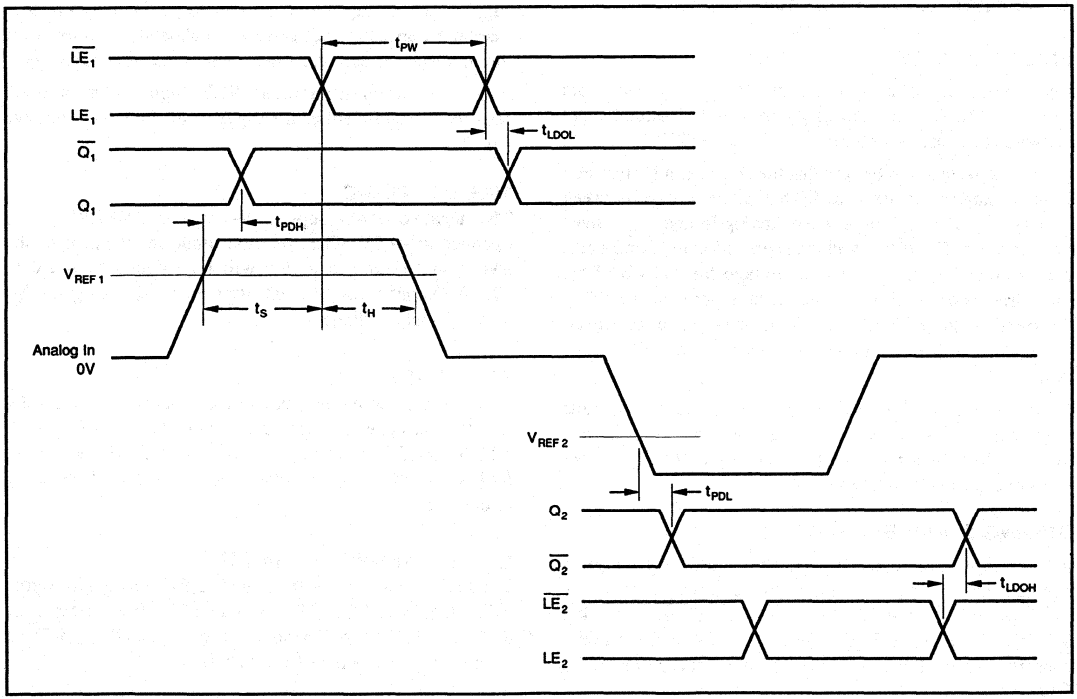


FIGURE 1. Analog and Logic Timing Definitions.

The t_S performance of CMP100 is illustrated in the Typical Performance Curves.

Minimum Hold Time, t_H

t_H is the minimum time after the positive transition of the Latch Enable (LE) that an analog input signal must remain unchanged in order to be acquired and held at the outputs. t_H = 0 for CMP100.

LOGIC PERFORMANCE DEFINITIONS

Latch Enable to Output High Delay, t_{DLOH}

t_{DLOH} is the propagation delay of latch logic circuits measured from the 50% point of the Latch Enable signal (LE) High-to-Low transition to the 50% point of an output (Q) Low-to-High transition.

Latch Enable to Output Low Delay, t_{DLOL}

t_{DLOL} is the propagation delay of latch logic circuits measured from the 50% point of the Latch Enable signal High-to-Low transition to the 50% point of an output (Q) High-to-Low transition.

Minimum Latch Enable Pulse Width, t_{PW}

t_{PW} is the minimum time that the Latch Enable (LE) must be High in order to acquire and hold an input signal change.

The actual timing performance of CMP100 is illustrated in the Typical Performance Curves.

OPERATING CONSIDERATIONS

INPUT VOLTAGE

Input reference voltages $V_{REF\,1}$ and $V_{REF\,2}$ may vary from –12V to +12V. The frequency-compensated analog input network can also swing from –12V to +12V.

Care must be taken to be sure that the Maximum Differential Input Voltage is not exceeded. That is, the voltage between Analog In and $V_{REF\,1}$ or between Analog In and $V_{REF\,2}$ must not exceed ±25V. If this voltage is exceeded by 1 or 2 volts, even momentarily, emitter-base voltage breakdown of the input transistors will occur and cause a permanent shift of the offset voltage, V_{OS}, to an out-of-spec value. However, the CMP100 will continue to function and will not be destroyed.

Input voltages to the CMP100 of uncontrolled magnitude may occur during system power-up. Take care to assure that the Absolute Maximum Differential Input Voltage is not exceeded during power-up.

DRIVING SOURCE IMPEDANCE

An apparent slow response of the CMP100 may be due a combination of high source impedance and stray capacitance to ground at the analog input. An R-C combination of 1kΩ source resistance and 10pF to ground results in a 10ns time constant—more than double the typical response time of the CMP100.

THE LATCH FUNCTION

The latch function is used for sampling the state of the outputs and holding them until the output can be processed.

Figure 1 shows a timing diagram for differential input latch enable controls, LE and $\overline{LE}$. The latches of the CMP100 are transparent type latches. If LE is Low ($\overline{LE}$ is High), the Q outputs indicate the sign of the input difference voltage. When LE goes High ($\overline{LE}$ Low), the comparator outputs are held at the current state.

When the analog input signal passes through the reference level, the comparator output Q changes, after a time of t_{PDH} or t_{PDL}. However, if the output is to be latched, the input signal must have crossed the threshold for a time t_S (set-up time) before the rising edge of LE occurs in order to capture the correct output state. On the other hand, in order to capture a correct output state just before it changes, it is necessary to maintain that output state for t_H, (hold time) after the rising edge of LE. t_H = 0 for CMP100.

A minimum latch pulse width of t_{PW} is needed to capture the state of narrow pulses. See the Typical Performance Curves for an example of sampling a narrow pulse.

10k ECL LOGIC

If the latching function is not used, the Latch Enable inputs ($\overline{LE_1}$ and $\overline{LE_2}$) should be returned to an ECL High voltage (–0.8V) or to Digital Common (0V). LE_1 and LE_2 should be returned to an ECL Low level (–1.8V), to an ECL bias voltage (–1.3V) or to the –2V 50Ω load pull-down power supply. Connecting an ECL input to –5.2V may create a marginal transistor emitter-base breakdown situation over the ambient temperature range and is not recommended.

If a single (non-differential) ECL logic input is used, connect the complementary input to an ECL bias voltage (–1.3V).

100k ECL LOGIC

The negative power supply, V–, of the CMP100 can be operated at –4.5V. The common mode input range of the analog and reference inputs will be reduced to +12V to –7.5V. Output levels are not affected by changing the V– power supply voltage to –4.5V.

TTL INPUTS

The operating common mode range of a logic input is –2V to +2V. Thus one can bias the logic inputs to use them with TTL inputs if the High input level is maintained below +2V. In this case, the complementary logic input should be biased at the TTL threshold of +1.4V.

LEVEL SHIFTING ECL to TTL

The ECL outputs can be translated to TTL using a Motorola MC10125 Quad ECL-TTL translator. The logic delay t_{DLOH} and t_{DLOL} and the propagation delay t_{PDL} and t_{PDH} will be increased by the delay of the translator.

INSTALLATION

TERMINATING ECL OUTPUTS

The best performance will be achieved with the use of proper ECL terminations. Such a configuration is illustrated in Figure 3. The open-emitter outputs of the CMP100 are designed to be terminated through 50Ω resistors to –2V or any other equivalent termination. If high-speed ECL signals must be routed more than a few centimeters, MicroStrip or StripLine techniques may be required to insure proper transition times and prevent output ringing.

POWER SUPPLY SELECTION

Linear power supplies are preferred. Although switching power supply rms specifications may appear to indicate low noise output, voltage spikes generated by switchers may be hard to filter. Their high-frequency components may be extremely difficult to keep out of the power supply return system. If switchers must be used, their outputs must be carefully filtered and the power supply itself should be shielded and located as far away as possible from precision analog circuits.

PRINTED CIRCUIT LAYOUT CONSIDERATIONS

Power Supply Wiring

Use heavy power supply and power supply common (ground) wiring. A ground plane under the part is usually the best solution for preserving dynamic performance and reducing noise coupling into sensitive circuits.

When passing power through a connector, use every available spare pin for making power supply return connections, and use some of the pins as a Faraday shield to separate the Analog and Digital Common lines.

Power Supply Returns (ACOM, DCOM and PWRCOM)

For best performance, connect ACOM (pin 13) and DCOM (pin 4) to the ground plane under the comparator. PWRCOM (pin 5), which is connected to the collectors of the ECL outputs, can be returned by separate printed circuit trace but its inductance should be kept low to avoid ringing. Do not connect ACOM and DCOM together at the end of a long printed circuit trace and then run a single wire to the power supply. To use separate ACOM and DCOM return printed circuit traces, connect a 1µF to 47µF tantalum capacitor between DCOM and ACOM pins as close to the package as possible.

Power Supply Bypassing

Every power supply line leading into the comparator must be bypassed to the Common pins. The bypass capacitor should be located as close to the comparator package as possible and tied to a solid return, preferably to the ground plane under the device. If the capacitors are not close enough to the package, DC resistance and inductance may be above acceptable levels. Use tantalum capacitors with values of from 1µF to 10µF. Parallel them with smaller ceramic

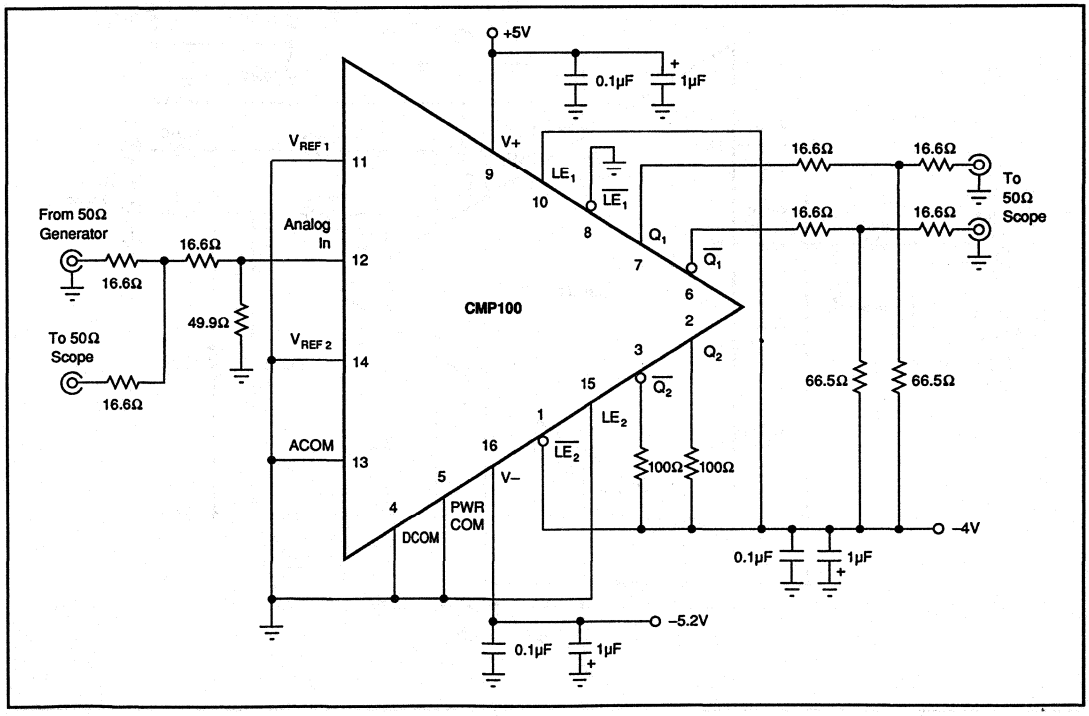


FIGURE 2. Circuit for Evaluating Analog Propagation Delay, t_{PDH}, t_{PDL}.

capacitors for high frequency filtering if necessary. Electrolytic capacitors are not recommended because their high frequency response is poor.

Separate the Analog and Digital Signals

Digital signal paths entering or leaving the layout should have minimum length to minimize crosstalk to analog wiring. Stray capacitive feedback from digital outputs to the analog input may cause the outputs to appear fuzzy well after the outputs have changed. Keep analog signals as far away as possible from digital signals. If they must cross, cross them at right angles. Coaxial cable may be necessary for analog inputs in some situations.

MEASURING CMP100 PERFORMANCE

USING AN OSCILLOSCOPE

Oscilloscope probes should be matched to the oscilloscope. Use an oscilloscope with at least 400MHz bandwidth.

Be sure the probe compensation is adjusted properly. Improper compensation will result in apparent overshoot and/or ringing if undercompensated, and an apparent slow edge if overcompensated. If the probe ground lead is too long, the output may appear distorted and oscillatory. Use probes with short (less than one inch) ground straps or use a coaxial cable connection instead of a probe. Do not use X1 or "straight" probes. Their bandwidth is 20MHz or less and capacitive loading is high. The best method is to use 50Ω matched terminations as shown in Figures 2 and 3.

MEASURING PROPAGATION DELAY

Figure 2 shows a circuit configuration used for evaluating propagation delay. It uses 50Ω matched terminations between the instruments and the CMP100 for best signal integrity. An HP8130A Pulse Generator is used for the analog input and for the latching signals. The oscilloscope is an HP54503A 500MHz Digitizing Oscilloscope. This setup was used to generate the dynamic performance waveforms in the Typical Performance Curves section.

MEASURING LOGIC TIMING

Figure 3 shows the circuit configuration used for evaluating logic propagation delay. The logic input LE1 has been added to the circuit of Figure 2.

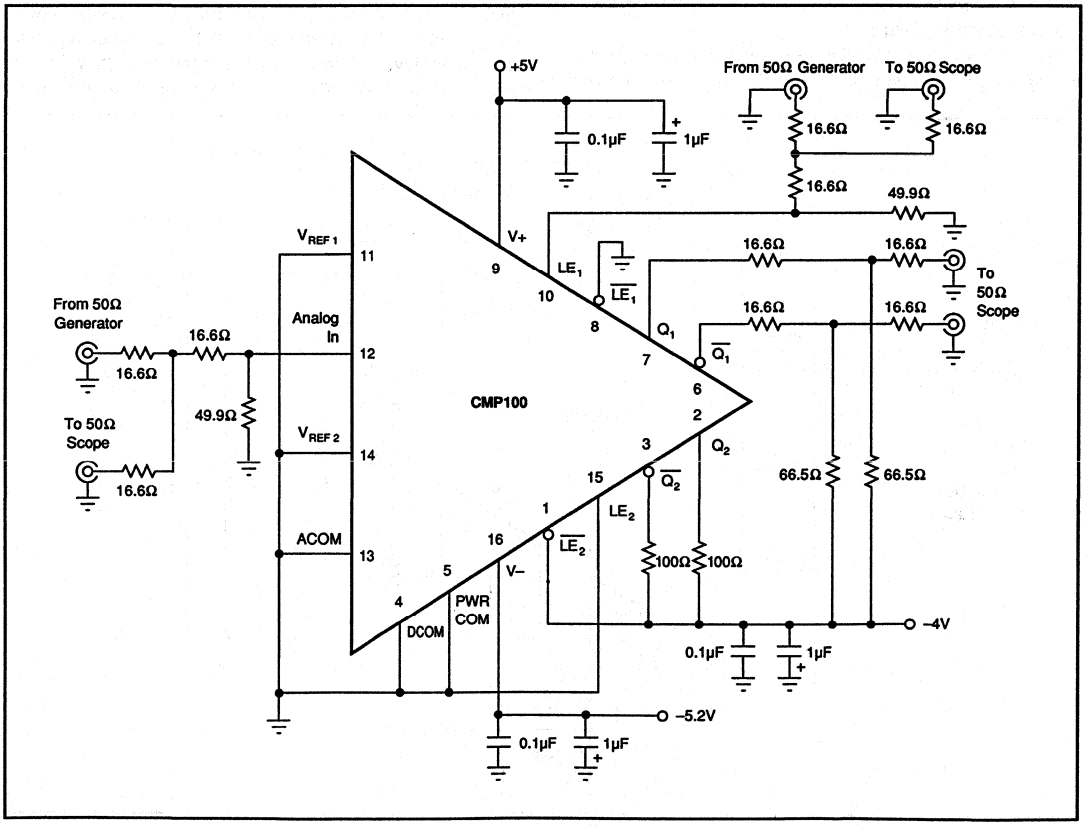


FIGURE 3. Circuit for Evaluating Logic Timing.

CMP100 APPLICATIONS

ATE PIN RECEIVER

A typical ATE pin receiver application using CMP100 is illustrated in Figure 4. The reference inputs, $V_{REF\,1}$ and $V_{REF\,2}$ are driven by D/A converters (Figure 5) while analog input is driven directly from the device under test (DUT).

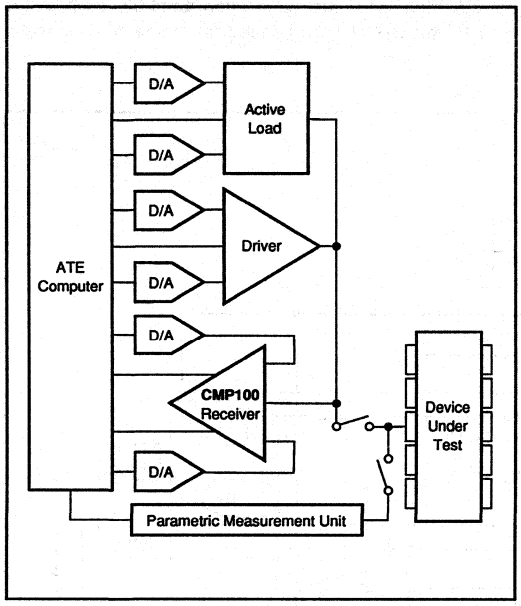


FIGURE 4. Typical ATE Pin Receiver Application.

WINDOW COMPARATOR

Because of its high speed, the CMP100 can be used to make timing measurements on modest-speed digital or high-speed analog waveforms. When the outputs of the CMP100 are combined with a NOR gate, a true window comparator function is implemented. Refer to gate G3 of Figure 6. The output pulse width generated by an input signal passing through the reference levels can be measured. This could be for a rise-time/fall-time measurement (setting the reference levels at 10% and 90% of the signal height) of a modest speed digital waveform, or for the width (and hence the value) of an analog ramp moving between two values from an integrating type signal detector.

PULSE RECOVERY

The window comparator function can also be used to reconstruct pulses that have been degraded. Positive and/or negative reference levels can be set up to detect both High and Low levels of the pulse.

A plot of the response of CMP100 to a narrow pulse with V_{REF1} = 0V is shown in the Typical Performance Curves section.

DETECTING TRANSIENTS

CMP100 can be connected to Detect and Hold transient occurrences above and below threshold voltages set by $V_{REF\,1}$ and $V_{REF\,2}$ as illustrated in Figure 6. The outputs of comparator 1 and comparator 2 are fed back to their LE inputs in order to self-latch their outputs. The Reset control is used to "unlock" the outputs after the transient occurrence has been read. The output NOR gate G3 combines CMP100 outputs into a single-output window comparator function.

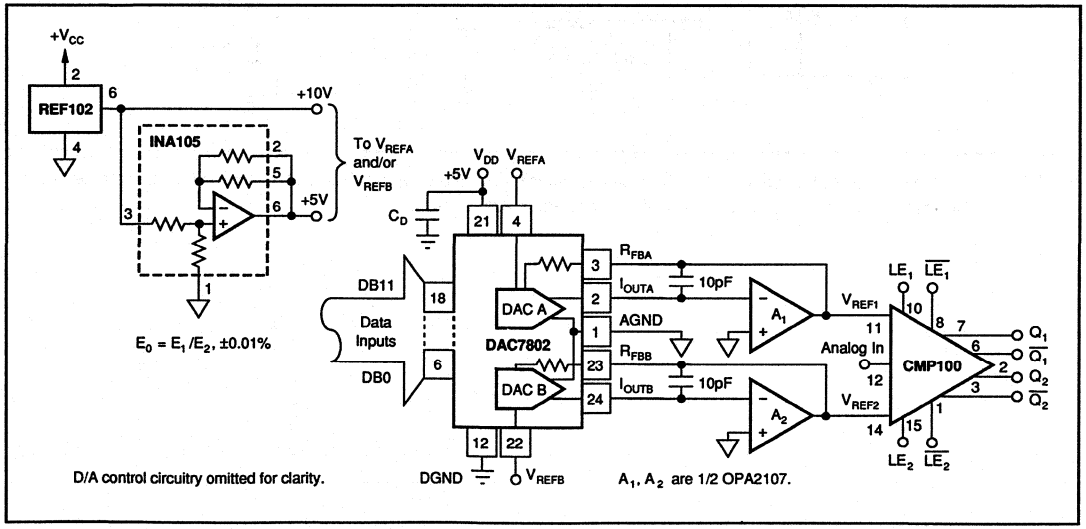


FIGURE 5. Dual DAC7802 (12-bit port), DAC7801 (8-bit port) or DAC7800 (serial port) D/A Converters Supply Reference Inputs to the CMP100. For higher resolution use DAC725, dual 16-bit D/A converter.

Note that the transient being detected must remain above $V_{REF\,1}$ (or below $V_{REF\,2}$) longer than the propagation delay of the CMP100 plus the propagation delay of gates G1 and G2.

In an application where only one polarity of transient needs to be captured, comparator 2 (not latched) can be used as the source of the Reset control signal to unlock comparator 1 based on a different threshold condition (defined by $V_{REF\,2}$) on the analog input signal. This connection will stretch the transient occurrence for the time the $V_{REF\,2}$ condition is present.

WIDE-BAND AMPLIFIERS FOR ANALOG INPUT SIGNAL CONDITIONING

In a component test application the analog input of the CMP100 is usually driven directly from the DUT output. Other applications may require a high-speed buffer or voltage gain ahead of the CMP100. Recommended wide-bandwidth amplifiers are Burr-Brown OPA603 for up to ±10V signals, or OPA620/OPA621 for very wide-band ±3V signals. A high speed instrumentation amplifier such as the Burr-Brown INA110 can be used for common mode rejection.

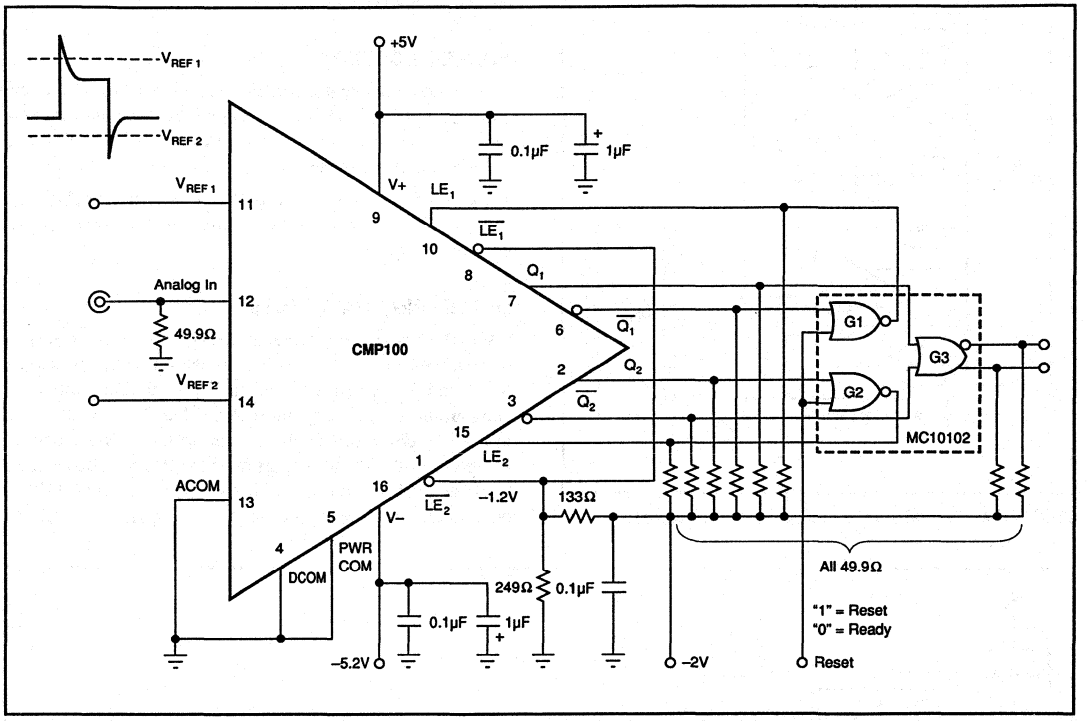
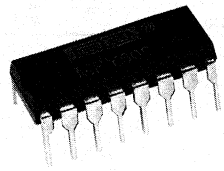


FIGURE 6. CMP100 Used to Detect and Hold Transient Occurrences on the Output Pulse of a Device Under Test, or Out-of-Limits Conditions in a Process-Variable Monitoring Application.

BURR-BROWN®



MPY600

Wide Bandwidth SIGNAL MULTIPLIER

FEATURES

- WIDE BANDWIDTH:
  75MHz — Current Output
  30MHz — Voltage Output
- LOW NOISE
- LOW FEEDTHROUGH: –60dB (5MHz)
- GROUND-REFERRED OUTPUT
- LOW OFFSET VOLTAGE

APPLICATIONS

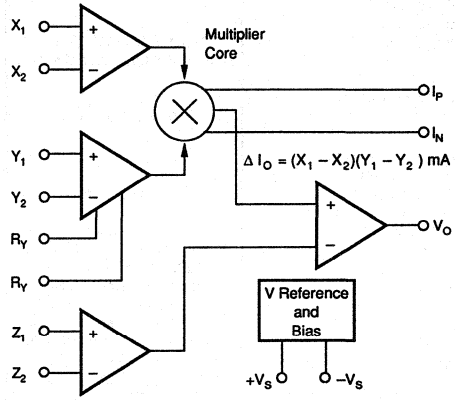
- MODULATOR/DEMODULATOR
- VIDEO SIGNAL PROCESSING
- CRT GEOMETRY CORRECTION
- CRT FOCUS CORRECTION
- VOLTAGE-CONTROLLED CIRCUITS

DESCRIPTION

The MPY600 is a wide-bandwidth four-quadrant signal multiplier. Its output voltage is equal to the algebraic product of the X and Y input voltages. For signals up to 30MHz, the on-board output op amp provides the complete multiplication function with a low-impedance voltage output. Differential current outputs extend multiplier bandwidth to 75MHz.

The MPY600 offers improved performance compared to common semiconductor modulator or multiplier circuits. It can be used for both two-quadrant (voltage-controlled amplifier) and four-quadrant (double-balanced) applications. While previous devices required cumbersome circuitry for trimming, balance and level-shifting, the MPY600 requires no external components. A single external resistor can be used to program the conversion gain for optimum spurious-free dynamic range. When used as a modulator, carrier feedthrough measures –60dB at 5MHz.

Differential X, Y and Z inputs can be connected in a variety of useful configurations, including squarer, divider, and square-rooter circuits. The MPY600 is available in 16-pin plastic DIP, specified for the industrial temperature range.



$$V_O = A\left[\frac{(X_1 - X_2)(Y_1 - Y_2)}{2V} + Z_2 - Z_1\right]$$

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Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

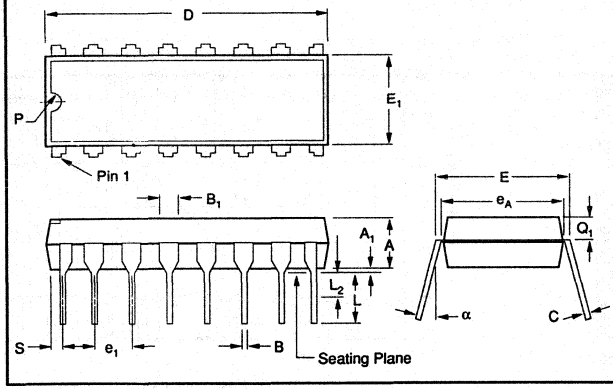
At $V_S = \pm5V$, $T_A = +25°C$ unless otherwise noted.

SPECIFICATION	CONDITIONS	MPY600AP MIN	MPY600AP TYP	MPY600AP MAX	UNITS
INPUTS (X, Y, Z)					
Full-Scale Differential Input					
X_1-X_2		±1			V
Y_1-Y_2		±2			V
Z_1-Z_2		±2			V
Input Voltage Range			±2.2		V
Differential Input Range			±2.5		V
Input Impedance			100 || 1.5		kΩ || pF
Input Offset Voltage			±0.5	±5	mV
Drift			25		µV/°C
CMRR	V_{CM} = ±2V		70		dB
PSRR			70		dB
Input Bias Current (X, Y)			+15		µA
Z Input			–15		µA
VOLTAGE OUTPUT					
Transfer Function			$V_O = \frac{(X_1-X_2)(Y_1-Y_2)}{2} + Z_2$		
Total Multiplier Error[1]	–1V ≤ X ≤ 1V, –2V ≤ Y ≤ 2V		±15	±25	mV
	–2V ≤ X ≤ 2V, –2V ≤ Y ≤ 2V		±25		mV
Gain Error			±1		%
Gain Temperature Drift			±200		ppm/°C
Power Supply Rejection	V_S = ±4 to ±6V		70		dB
Noise	f = 1kHz to 30MHz		120		nV/√Hz
Output Voltage Swing	R_L = 100Ω	±2.2	±3		V
Output Current		±22	±30		mA
Short-Circuit Limit			50		mA
Bandwidth	Small Signal		30		MHz
Slew Rate			150		V/µs
Settling Time to 0.1%	4V Step		150		ns
Differential Gain Error	3.58MHz, 0 to 0.7V		0.2		%
Differential Phase Error	3.58MHz, 0 to 0.7V		0.2		Degrees
Capacitive Load, Max	Stable Operation		100		pF
Feedthrough, X	X = 0dBm, f = 500kHz; Y Nulled		–65		dB
	X = 0dBm, f = 5MHz; Y Nulled		–60		dB
Feedthrough, Y	Y = 0dBm, f = 500kHz; X Nulled		–70		dB
	Y = 0dBm, f = 5MHz; X Nulled		–50		dB
Distortion, X	X = 0dBm, f = 500kHz, Y = 2V		–60		dB
	X = 0dBm, f = 5MHz, Y = 2V		–55		dB
Distortion, Y	Y = 0dBm, f = 500kHz, X = 2V		–65		dB
	Y = 0dBm, f = 5MHz, X = 2V		–55		dB
CURRENT OUTPUT					
Transfer Function			$\Delta I_O = (X_1 - X_2)(Y_1 - Y_2)$		mA
Total Multiplier Error[1]	–1V ≤ X ≤ 1V, –2V ≤ Y ≤ 2V		±20	±80	µA
	–2V ≤ X ≤ 2V, –2V ≤ Y ≤ 2V		±80		µA
Gain Error			±1		%
Gain Temperature Drift			±200		ppm/°C
Power Supply Rejection	V_S = ±4 to ±6V		50		dB
Noise, Output			100		pA/√Hz
Voltage Compliance Range			±2.5		V
Peak Output Current			5		mA
Noise, Input-Referred	f = 1kHz to 75MHz		50		nV/√Hz
Bandwidth, Small-Signal			75		MHz
Settling Time to 0.1%	4mA Step		150		ns
Feedthrough, X	X = 0dBm, f = 1MHz; Y Nulled		–65		dB
	X = 0dBm, f = 10MHz; Y Nulled		–45		dB
Feedthrough, Y	Y = 0dBm, f = 1MHz; X Nulled		–75		dB
	Y = 0dBm, f = 10MHz; X Nulled		–55		dB
Distortion, X	X = 0dBm, f = 1MHz, Y = 2V		–55		dB
	X = 0dBm, f = 10MHz, Y = 2V		–50		dB
Distortion, Y	Y = 0dBm, f = 1MHz, X = 2V		–65		dB
	Y = 0dBm, f = 10MHz, X = 2V		–50		dB
POWER SUPPLY					
Rated Performance			±5		V
Operating		±4.75		±8	V
Current			±30	±35	mA
TEMPERATURE RANGE					
Specified Temperature Range		–25		+85	°C
Storage Temperature Range		–40		+125	°C
Thermal Resistance, θ_{J-A}			50		°C/W

NOTE: (1) Deviation from ideal transfer function referred to full scale output. Includes gain, nonlinearity and offset errors.

MECHANICAL

P Package — 16-Pin Plastic DIP



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.155	.200	3.94	5.08
A1(1)	.015	0.50	0.38	1.27
B	.014	.020	0.36	0.51
B1	.035	.065	0.89	1.65
C	.008	.012	0.20	0.30
D	.745	.785	19.00	19.94
E	.300	.325	7.62	8.26
E1	.240	.260	6.10	6.60
e1	.100 BASIC		2.54 BASIC	
eA	.300 BASIC		7.62 BASIC	
L	.125	.150	3.18	3.81
L2	.000	.030	0.00	0.76
a	0°	15°	0°	15°
P	.015	.050	0.38	1.27
Q1	.040	.075	1.02	1.91
S	.015	.060	0.38	1.52

(1) Not JEDEC Std.

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

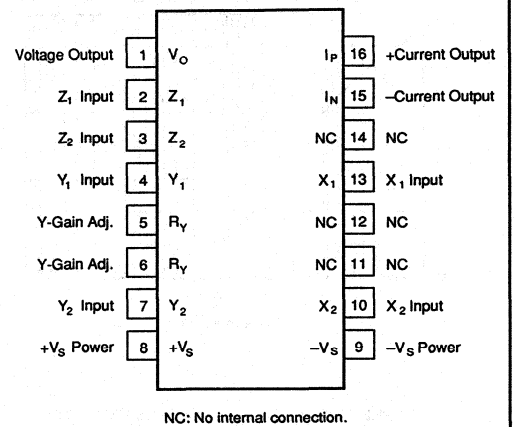
ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18V
Input Voltage Range	$\pm V_S$
Op Amp Output Current	100mA
Operating Temperature	+125°C
Storage Temperature	+150°C
Junction Temperature	+150°C
Lead Temperature (soldering, 10s)	+300°C

ORDERING INFORMATION

MODEL	PACKAGE	SPECIFIED TEMPERATURE RANGE
MPY600AP	Plastic DIP	–25°C to +85°C

PIN CONFIGURATION

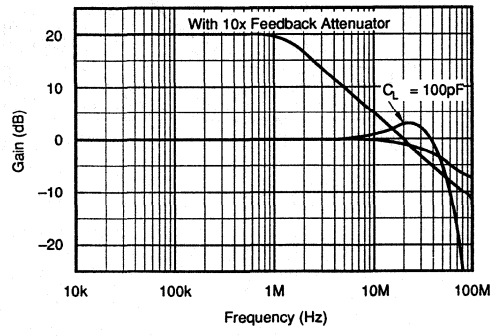


NC: No internal connection.

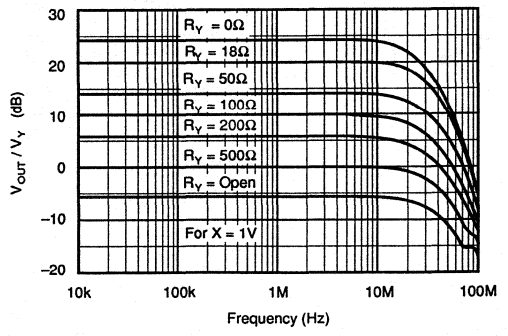
TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_S = ±5V unless otherwise noted.

MULTIPLIER GAIN vs FREQUENCY



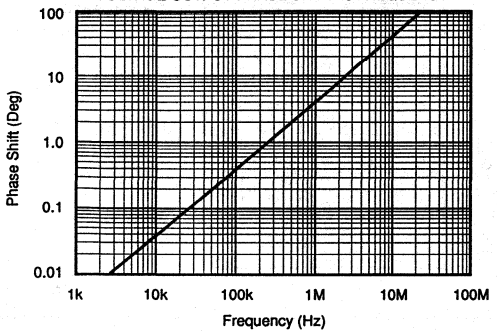
VOLTAGE OUTPUT FREQUENCY RESPONSE



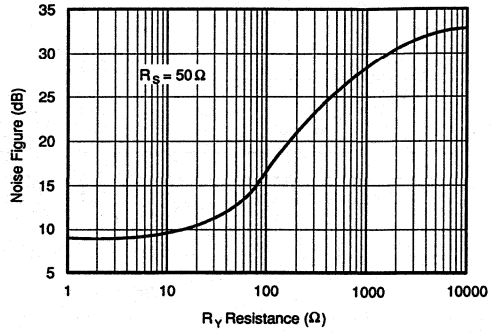
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_S = ±5V unless otherwise noted.

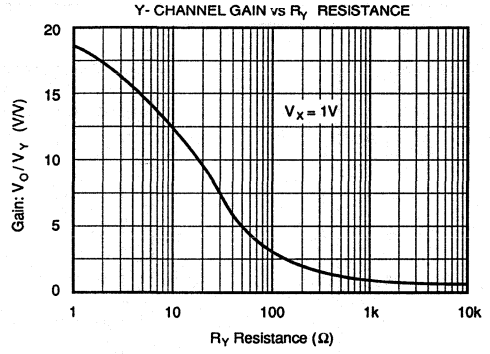
VOLTAGE OUTPUT PHASE SHIFT vs FREQUENCY



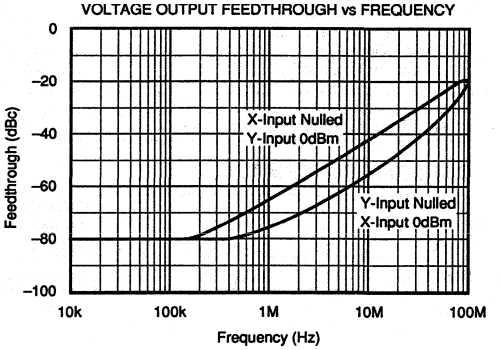
NOISE FIGURE vs R_Y RESISTANCE



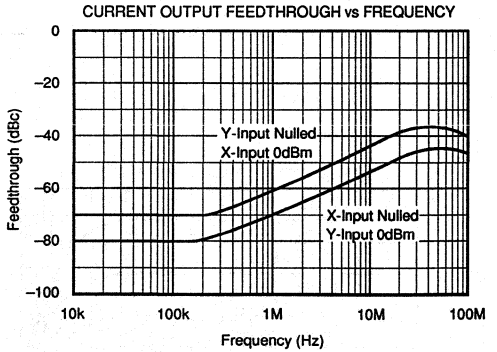
Y- CHANNEL GAIN vs R_Y RESISTANCE



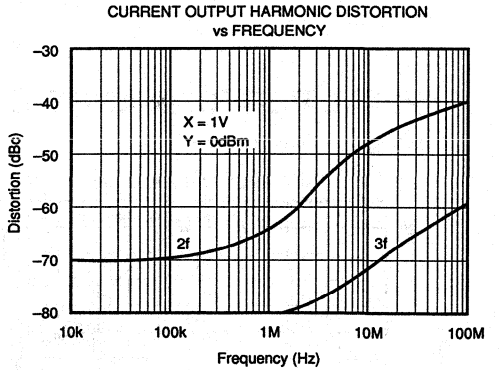
VOLTAGE OUTPUT FEEDTHROUGH vs FREQUENCY



CURRENT OUTPUT FEEDTHROUGH vs FREQUENCY



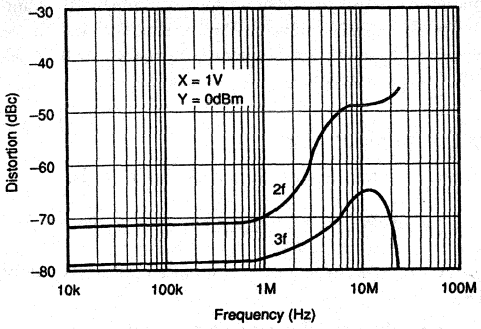
CURRENT OUTPUT HARMONIC DISTORTION vs FREQUENCY



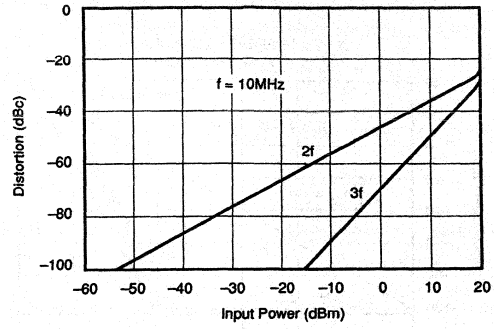
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_S = ±5V unless otherwise noted.

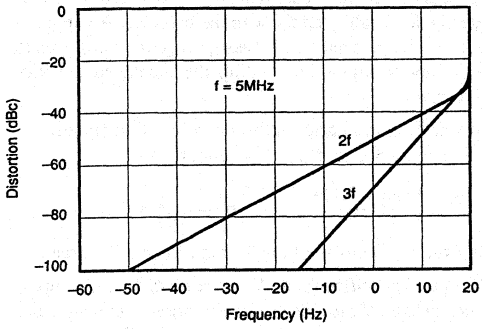
VOLTAGE OUTPUT HARMONIC DISTORTION vs FREQUENCY



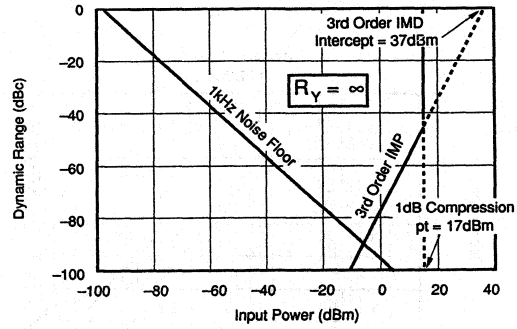
CURRENT OUTPUT HARMONIC DISTORTION vs INPUT POWER



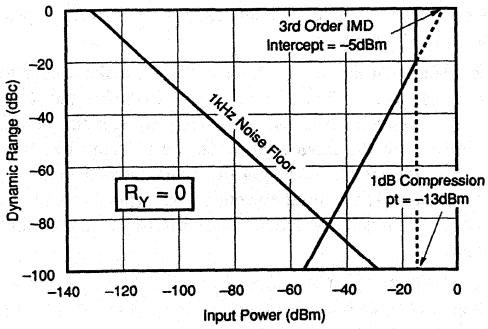
VOLTAGE OUTPUT HARMONIC DISTORTION vs INPUT POWER



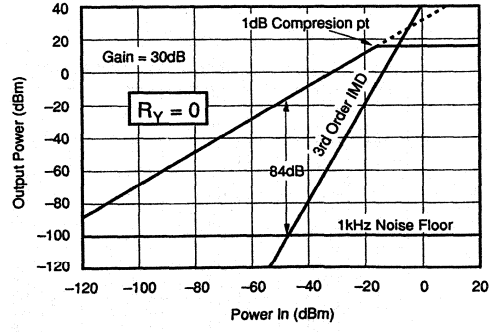
INPUT-REFERRED DYNAMIC RANGE vs INPUT POWER



INPUT-REFERRED DYNAMIC RANGE vs INPUT POWER



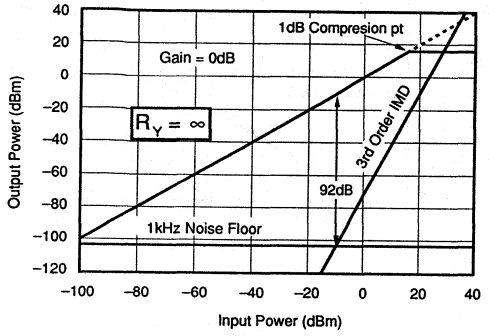
OUTPUT-REFERRED DYNAMIC RANGE vs INPUT POWER



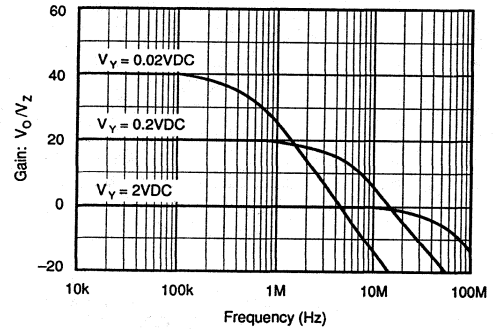
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_S = ±5V unless otherwise noted.

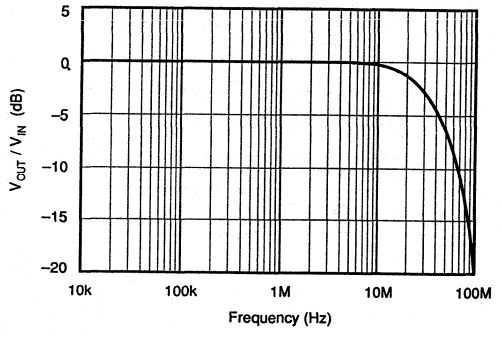
OUTPUT-REFERRED DYNAMIC RANGE vs INPUT POWER



DIVIDER RESPONSE vs FREQUENCY



VOLTAGE OUTPUT SQUARER FREQUENCY RESPONSE



POWER SUPPLIES

The MPY600 may be operated from power supplies from ±4.75V to ±8V. Operation from ±5V supplies is recommended. Since input and output levels are ±2V, larger supply voltage is not required for full output voltage swing. Furthermore, power dissipation can be minimized by using lower power supply voltage. Power supplies should be bypassed with good high-frequency capacitors such as ceramic or solid tantalum.

TRANSFER FUNCTION

The open-loop transfer function of the MPY600 is:

$$V_O = A\left[\frac{(X_1 - X_2) \bullet (Y_1 - Y_2)}{2V} - (Z_1 - Z_2)\right]$$

where A = open-loop gain of the output amplifier (typically 70dB).

X, Y, Z are differential input voltages— ±2V max.

An intuitive understanding of the transfer function can be gained by analogy to an op amp. Assuming that the open-loop gain is infinite, any output voltage can be created by an infinitesimally small quantity with the brackets. An applications circuit can be analyzed by assigning circuit voltages to the X, Y and Z inputs and setting the bracketed quantity equal to zero.

For example, in the basic multiplier connection (Figure 1), $Z_1 = V_O$ and $Z_2 = 0$. Setting this equal to zero:

$$\left[\frac{(X_1 - X_2) \bullet (Y_1 - Y_2)}{2V} - V_O\right] = 0$$

Solving for V_O yields the transfer function of the circuit.

The X input is specified for ±1V full-scale differential input. X inputs up to ±2V provide useful operation with somewhat reduced accuracy and distortion performance. The Y input is rated for ±2V full-scale input. The Y input gain (and therefore its full-scale range) can be varied with an external resistor connected to the R_Y terminals—see "Modulator/Demodulator." Full-scale inputs (X = ±1V, Y = ±2V) produce a ±1V output.

The differential inputs, X_1, X_2, and Y_1, Y_2, make it easy to trim offset voltage. The trim voltage is applied to the X_2 or Y_2 input, which is otherwise grounded (see X_2 input, Figure 5). Polarity of the input signals can be reversed by interchanging the inputs (reversing the connections X_1 and X_2, for instance). The unused current outputs (pins 15 and 16) must be grounded (or loaded—see discussion on current outputs).

The output amplifier is operated in unity gain. The output voltage can be increased (for small input signals) by placing the internal output op amp in higher gain (Figure 2). This reduces bandwidth and increases output offset voltage errors.

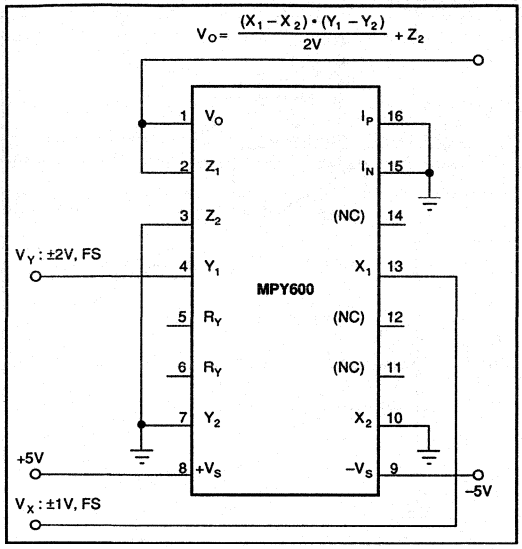


FIGURE 1. Basic Multiplier Connection.

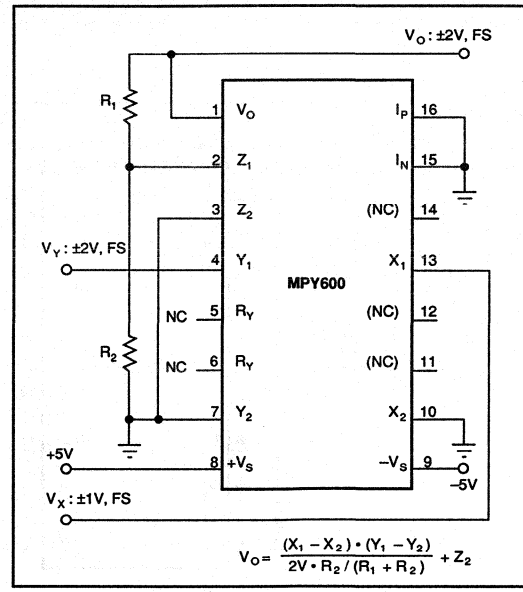


FIGURE 2. Adjusting the Scale Factor with Feedback.

CURRENT OUTPUT

The current output connections of the MPY600 can achieve wider bandwidth multiplier operation (Figure 3). The current output is determined by the X and Y inputs only, so applications which use the Z input to modify the transfer function (e.g., divider and square-root modes) cannot be used. A full-scale input of ±1V on the X and ±2V on the Y inputs produces a 2mA differential current at the current outputs. This consists of approximately 2.5mA quiescent current ±1mA signal current on each output. The current outputs may be used to drive any load impedance which maintains the voltage on the current outputs within their compliance range. This compliance limit is approximately 2.5V from the power supply voltages. The current outputs and voltage output may be used simultaneously, if desired.

Output capacitance and stray capacitance at the current output terminals will limit the multiplier bandwidth. This makes large output resistors (greater than approximately 1kΩ) impractical. The current outputs can be used to drive 50Ω or 75Ω loads directly.

The circuit shown in Figure 4 uses the current outputs to drive an external OPA621 op amp configured as a current-difference amplifier. It operates in a noise gain of 3.5. The OPA621 is stable in a noise gain of two or greater and has a 500MHz gain-bandwidth product. It achieves the full bandwidth performance of the MPY600. R_1 determines the transfer function gain. R_3 provides a proper load to optimize high-frequency effects. R_4 is made equal to the parallel combination of R_1 and R_3.

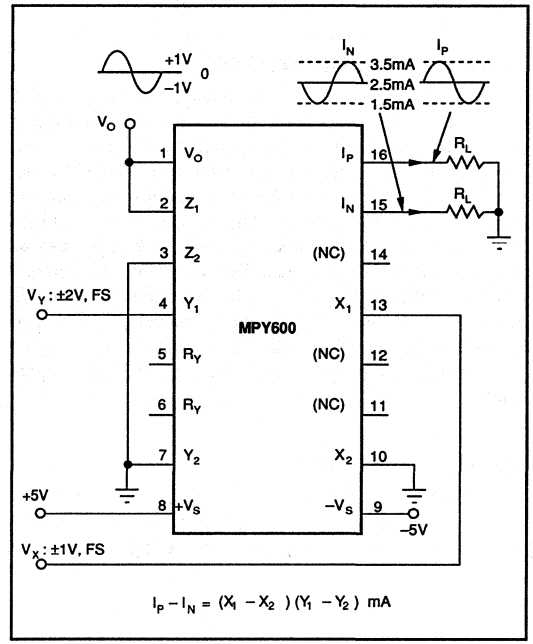


FIGURE 3. Current Output Connection.

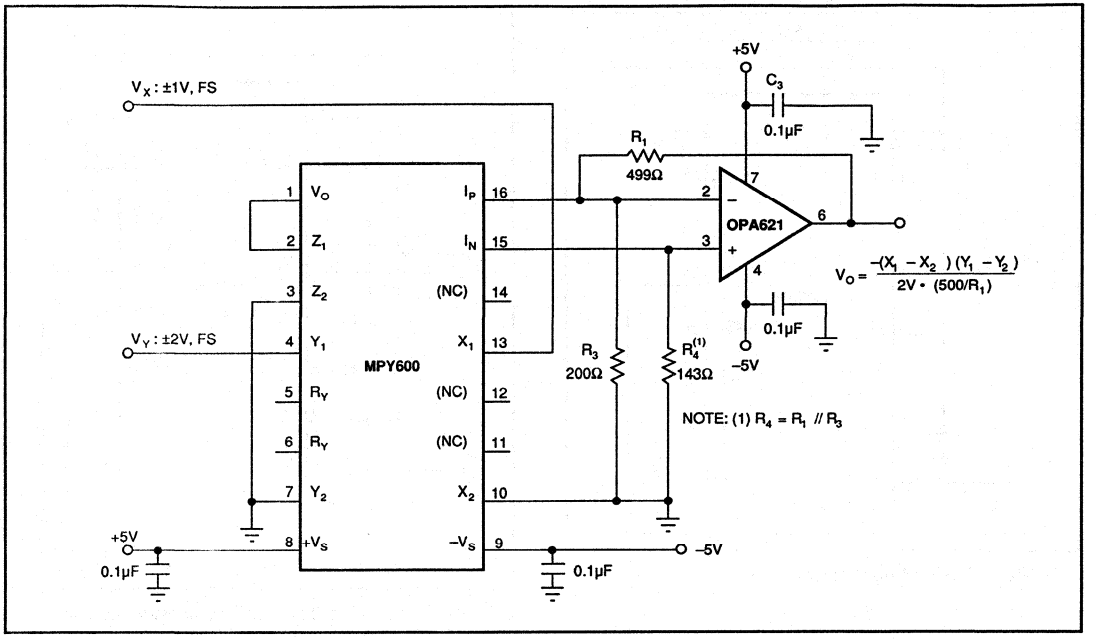


FIGURE 4. 75MHz DC-Coupled Multiplier.

MODULATOR/DEMODULATOR

The balanced modulator or demodulator shown in Figure 5 uses the basic multiplier configuration. It shows the offset of the X input trimmed to null carrier feedthrough. It also illustrates the use of R_Y to change the gain of the Y input. This can be used to optimize the spurious-free dynamic range for a given input level. The Y input is optimized for ±2V inputs. For lower input signals, the Y input can be programmed for higher gain by connecting an external resistor to the R_Y terminals. The conceptual diagram in Figure 6 reveals why varying the Y-channel gain can yield improved dynamic range. The R_Y selection curve in Figure 5 shows the optimum value of R_Y for a given Y-input signal level.

DIVIDER OPERATION

The MPY600 can be configured as a divider as shown in Figure 7. Numerator voltage is applied to the Z inputs; denominator voltage is applied to the X inputs. Since the feedback connection is made to a multiplying input, the effective gain of the output amplifier varies as a function of the denominator input. This causes the bandwidth to vary with denominator (see Typical Performance Curves for divider bandwidth performance). Accuracy in divider operation is approximately 3% for a 10:1 denominator range. Errors grow large and will eventually saturate the output as the denominator voltage approaches 0V.

SQUARE-ROOT CIRCUIT

The circuit in Figure 8 provides an output voltage proportional to the square-root of the input (for positive input voltages). Diode D_1 prevents latch-up if the input should go negative. The circuit can be configured for negative input and positive output by reversing the polarity of both the X and Y differential inputs. The output polarity can be inverted by reversing the X input polarity and the diode. Accuracy can be improved by trimming the offset at the Z input.

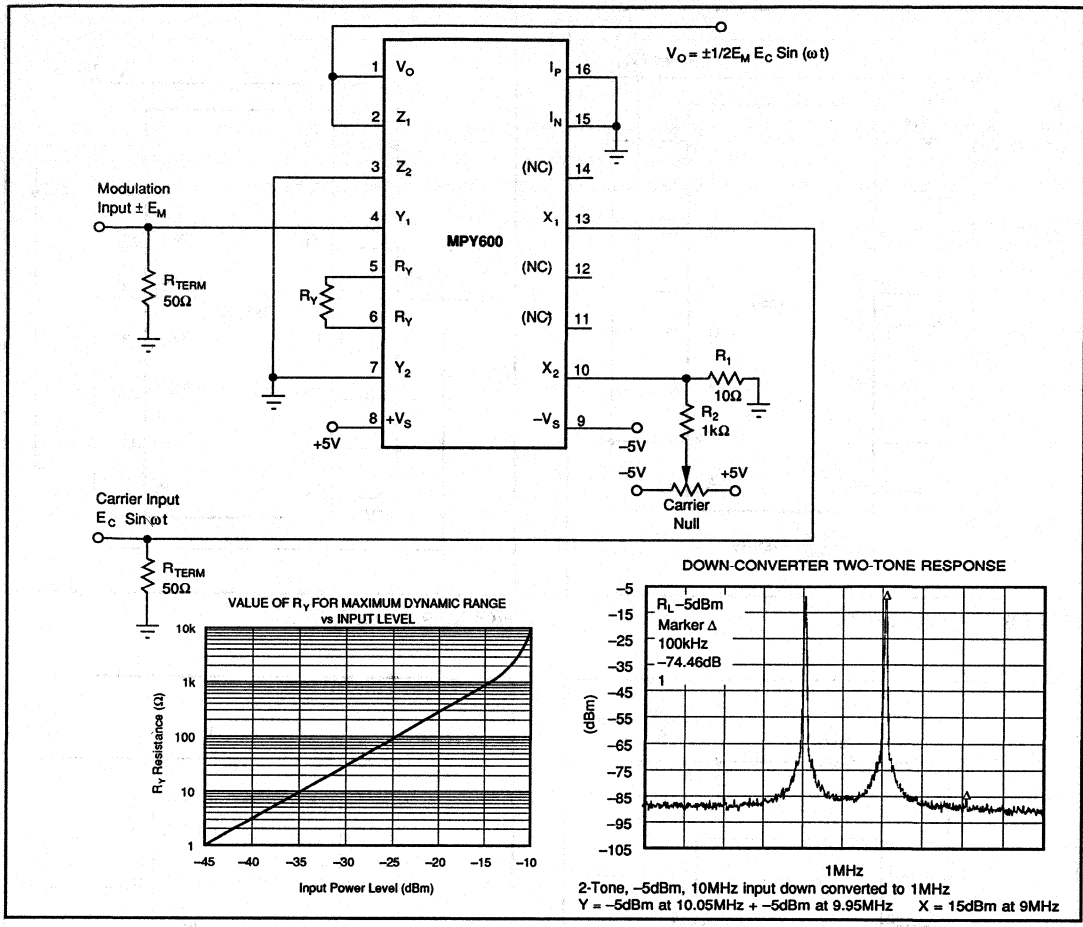


FIGURE 5. Balanced Modulator.

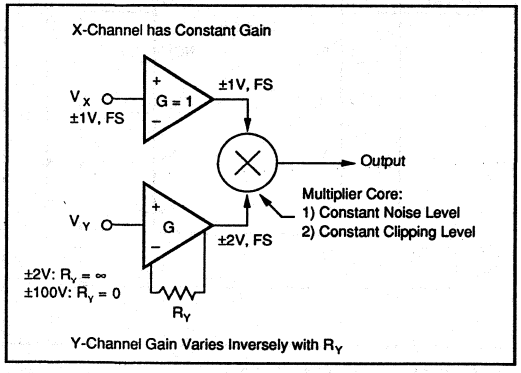


FIGURE 6. Variable Y-Channel Gain—Conceptual Model.

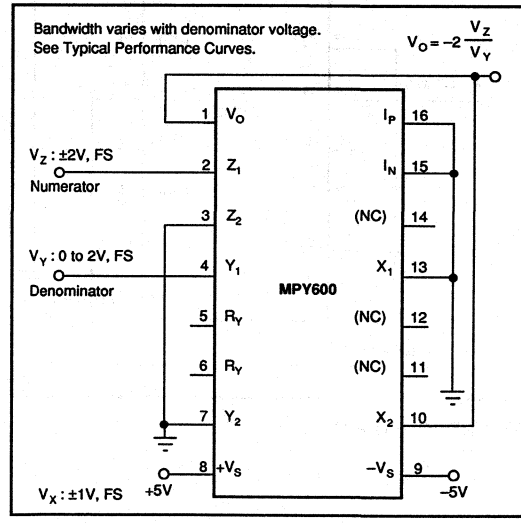


FIGURE 7. Divider Circuit.

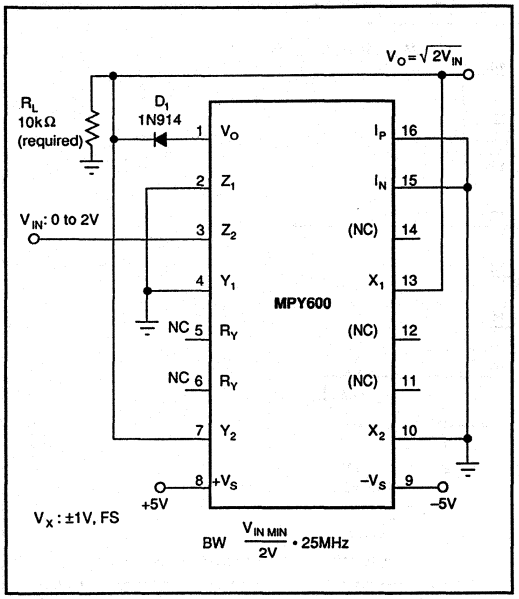


FIGURE 8. Square-Root Circuit.

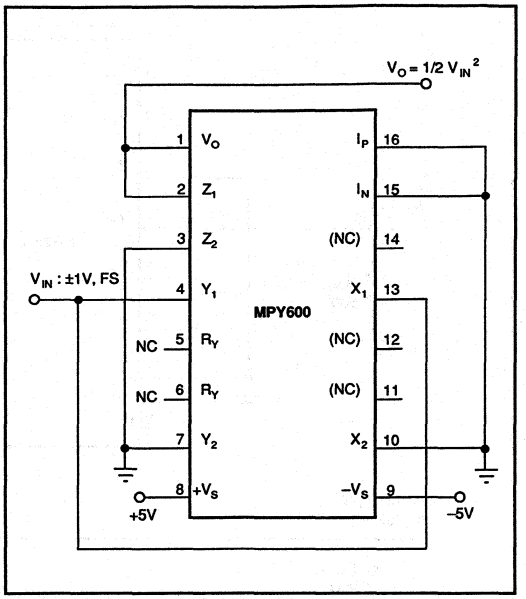


FIGURE 9. Squaring Circuit.

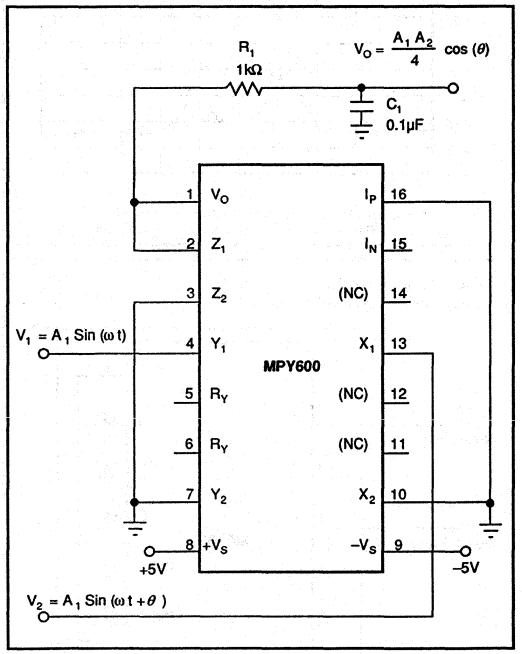


FIGURE 10. Phase Detector.

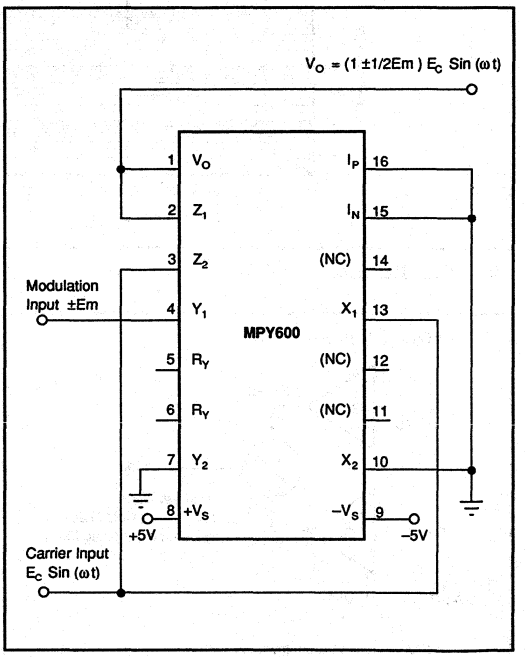


FIGURE 11. Linear AM Modulator.

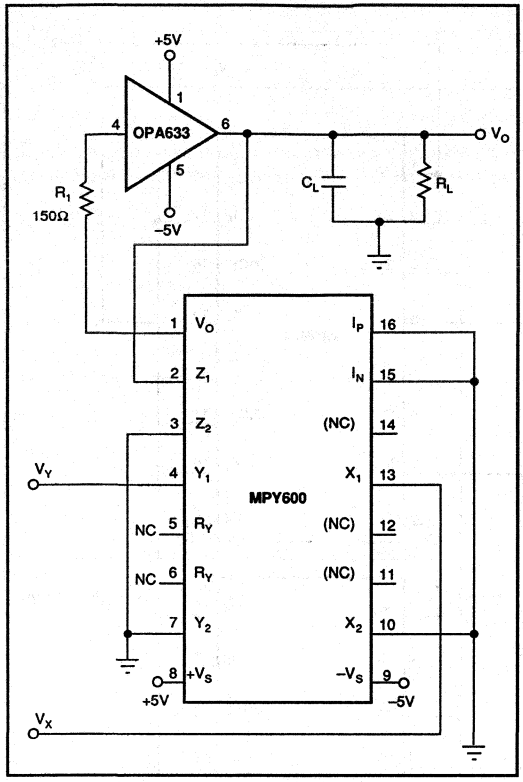


FIGURE 12. 25MHz Multiplier with Improved Load Driving Capability.

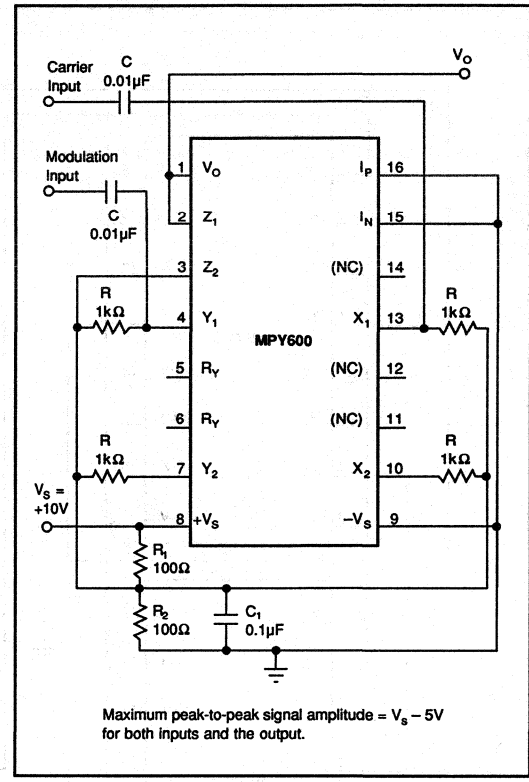


FIGURE 13. Single-Supply Balanced Modulator.

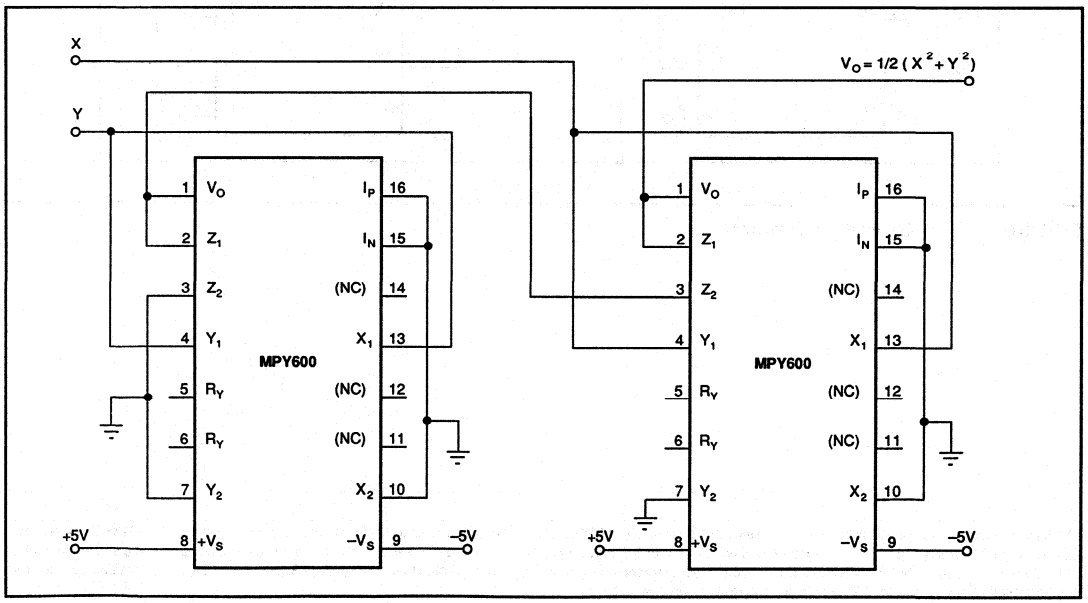


FIGURE 14. CRT Focus Correction.

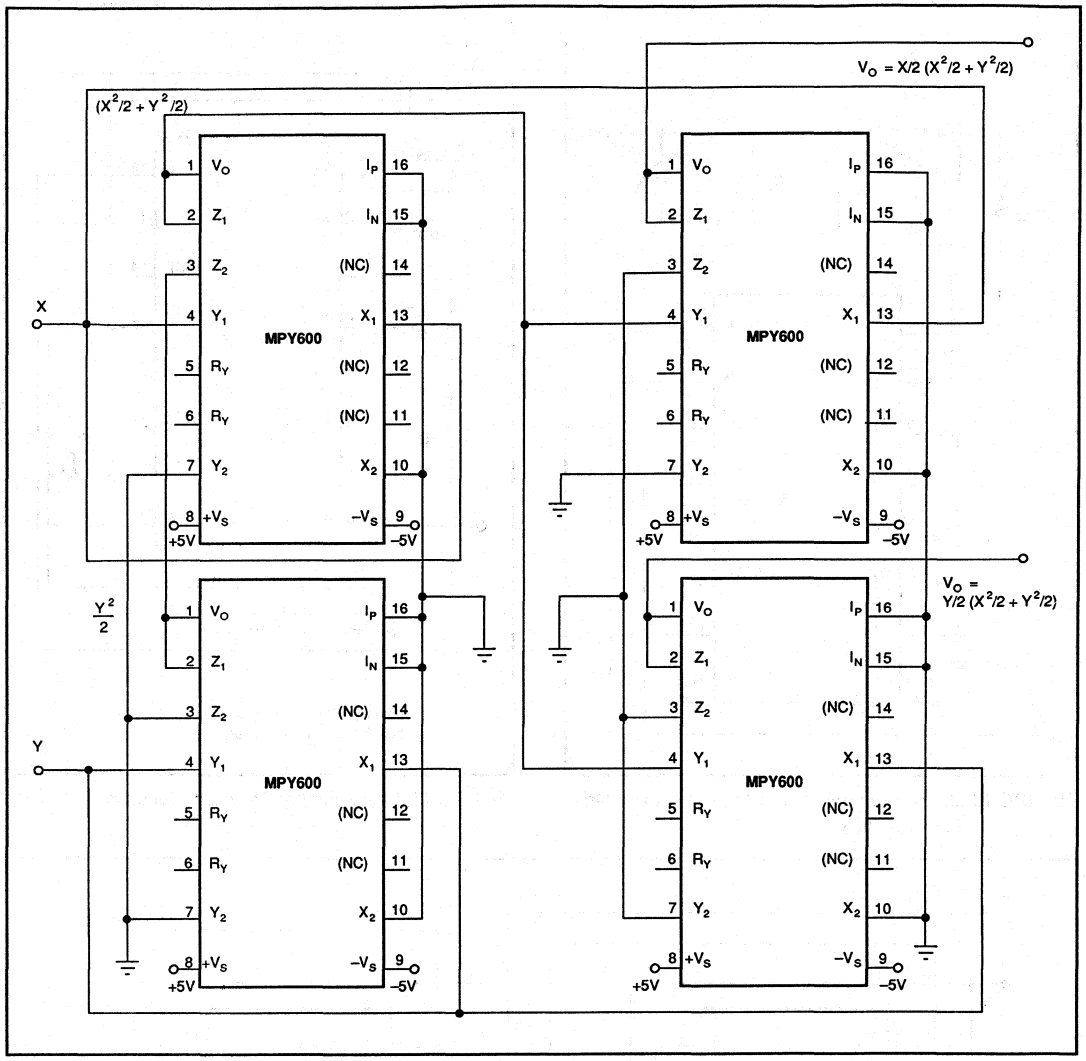


FIGURE 15. CRT Geometry Correction.

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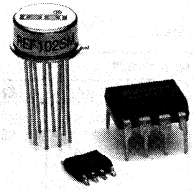


REF102

AVAILABLE IN DIE

Precision VOLTAGE REFERENCE

FEATURES

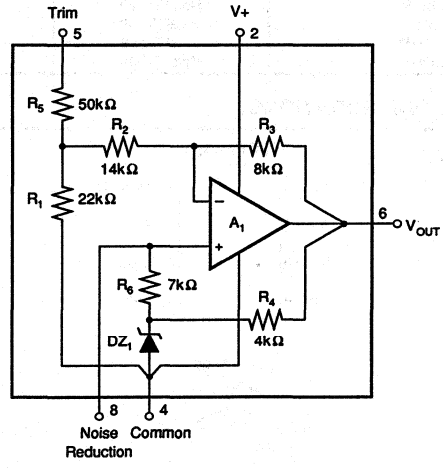
- +10V ± 0.0025V OUTPUT
- VERY LOW DRIFT: 2.5ppm/°C max
- EXCELLENT STABILITY: 5ppm/1000hr typ
- EXCELLENT LINE REGULATION: 1ppm/V max
- EXCELLENT LOAD REGULATION: 10ppm/mA max
- LOW NOISE: 5μVp-p typ, 0.1Hz to 10Hz
- WIDE SUPPLY RANGE: 11.4VDC to 36VDC
- LOW QUIESCENT CURRENT: 1.4mA max
- PACKAGE OPTIONS: HERMETIC TO-99, PLASTIC DIP, SOIC, DIE

APPLICATIONS

- PRECISION-CALIBRATED VOLTAGE STANDARD
- D/A AND A/D CONVERTER REFERENCE
- PRECISION CURRENT REFERENCE
- ACCURATE COMPARATOR THRESHOLD REFERENCE
- DIGITAL VOLTMETERS
- TEST EQUIPMENT
- PC-BASED INSTRUMENTATION

DESCRIPTION

The REF102 is a precision 10V voltage reference. The drift is laser-trimmed to 2.5ppm/°C max (CM grade) over the industrial temperature range and 5ppm/°C max (SM grade) over the military temperature range. The REF102 achieves its precision without a heater. This results in low-power, fast warm-up, excellent stability, and low noise. The output voltage is extremely insensitive to both line and load variations and can be externally adjusted with minimal effect on drift and stability. Single supply operation from 11.4V to 36V and excellent overall specifications make the REF102 an ideal choice for demanding instrumentation and system reference applications. The REF102 is also available in die form.



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Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL

At T_A = +25°C and V_S = +15V power supply unless otherwise noted.

PARAMETER	CONDITIONS	REF102A/R			REF102B/S			REF102CM			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
OUTPUT VOLTAGE											
Initial	T_A = 25°C	9.99		10.01	9.995		10.005	9.9975		10.0025	V
vs Temperature [1]				10			5			2.5	ppm/°C
vs Supply (Line Regulation)	V_S = 11.4V to 36V			2			1			1	ppm/V
vs Output Current (Load Regulation)	I_L = 0mA to +10mA			20			10			10	ppm/mA
	I_L = 0mA to −5mA			40			20			20	ppm/mA
vs Time	T_A = 25°										
M Package			5			•			•		ppm/1000hr
P, U Packages [2]			20			•					ppm/1000hr
Trim Range [3]		±3			•			•			%
NOISE	(0.1Hz to 10Hz)		5			•			•		µVp-p
OUTPUT CURRENT		+10, −5			•			•			mA
INPUT VOLTAGE RANGE		+11.4		+36	•		•	•		•	V
QUIESCENT CURRENT	(I_{OUT} = 0)			+1.4			•			•	mA
WARM-UP TIME [4]	(To 0.1%)		15			•			•		µs
TEMPERATURE RANGE											
Specification											
REF102A, B, C		−25		+85	•		•	•		•	°C
REF102R, S		−55		+125	•		•				°C

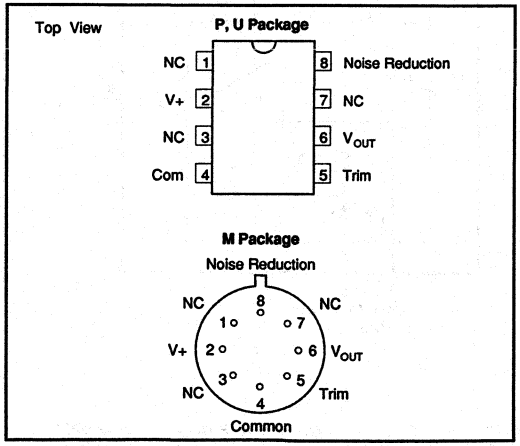
*Specifications same as REF102A/R.

NOTES: (1) The "box" method is used to specify output voltage drift vs temperature. See the Discussion of Performance section. (2) Typically 5ppm/1000hrs after 168hr powered stabilization. (3) Trimming the offset voltage affects drift slightly. See Installation and Operating Instructions for details. (4) With noise reduction pin floating. See Typical Performance Curves for details.

ORDERING INFORMATION

MODEL	PACKAGE	TEMP RANGE	MAX INITIAL ERROR (mV)	MAX DRIFT (ppm/°C)
REF102AU	SOIC	−25 to +85°C	±10	±10
REF102AP	Plastic DIP	−25 to +85°C	±10	±10
REF102BP	Plastic DIP	−25 to +85°C	±5	±5
REF102AM	Metal TO-99	−25 to +85°C	±10	±10
REF102BM	Metal TO-99	−25 to +85°C	±5	±5
REF102CM	Metal TO-99	−25 to +85°C	±2.5	±2.5
REF102RM	Metal TO-99	−55 to +125°C	±10	±10
REF102SM	Metal TO-99	−55 to +125°C	±5	±5

PIN CONFIGURATIONS



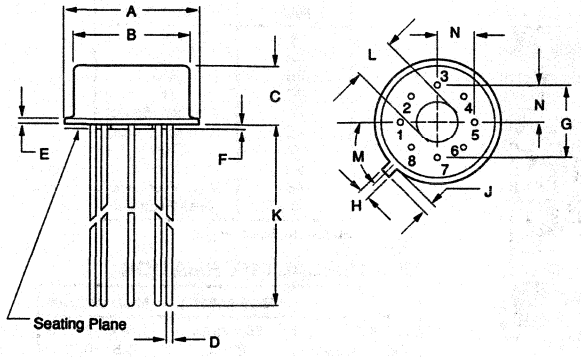
ABSOLUTE MAXIMUM RATINGS

Input Voltage	+40V
Operating Temperature	
P,U	−25°C to +85°C
M	−55°C to +125°C
Storage Temperature Range	
P,U	−40°C to +85°C
M	−65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C
(SOIC 3s)	+260°C
Short-Circuit Protection to Common or V+	Continuous

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

MECHANICAL

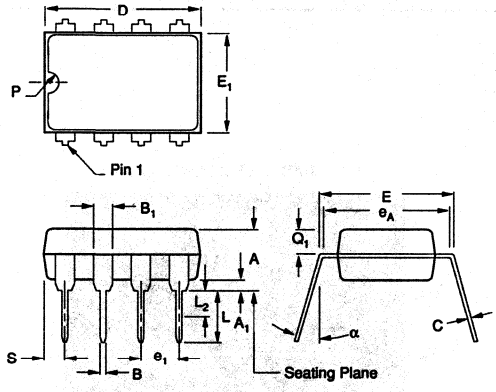
M Package — Metal TO-99



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.335	.370	8.51	9.40
B	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.200 BASIC		5.08 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500	—	12.7	—
L	.110	.160	2.79	4.06
M	45° BASIC		45° BASIC	
N	.095	.105	2.41	2.67

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.

P Package — 8-Pin Plastic DIP



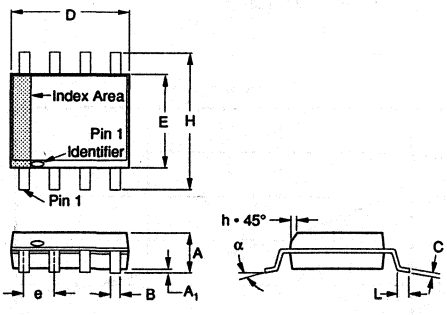
DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.155	.200	3.94	5.08
A1	.020	.050	0.51	1.27
B	.014	.020	0.36	0.51
B1	.045	.065	1.14	1.65
C	.008	.012	0.20	0.30
D (1)	.370	.400	9.40	10.16
E	.300	.325	7.62	8.26
E1	.240	.260	6.10	6.60
e1	.100 BASIC		2.54 BASIC	
eA	.300 BASIC		7.62 BASIC	
L	.125	.150	3.18	3.81

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
L2(2)	0	.030	0.00	0.76
α	0°	15°	0°	15°
P	.015	.050	0.38	1.270
Q1	.040	.075	1.02	1.91
S (1)	.015	.050	0.38	1.27

(1) Not JEDEC Std.
(2) e1 and e_A applies in zone L_2 when unit installed.

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

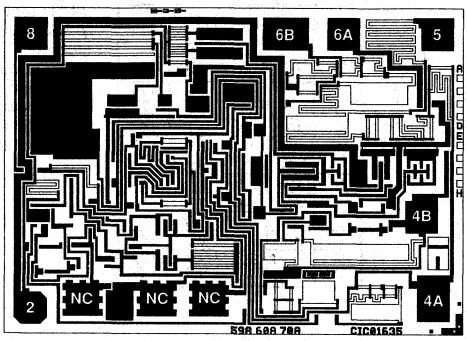
U Package — 8-Pin SO-8 Surface Mount



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.054	.068	1.37	1.73
A1	.004	.009	0.10	0.23
B	.014	.019	0.36	0.48
C	.008	.0098	0.20	0.25
D	.189	.196	4.80	4.98
E	.150	.157	3.81	3.99
e	.050 BASIC		1.27 BASIC	
H	.229	.244	5.82	6.20
h	.010	.019	0.25	0.48
L	.016	.050	0.41	1.27
N	8		8	
α	0°	8°	0°	8°

NOTES:
1. Dimensioning and tolerancing per ANSI Y14.5M–1982.
2. "D" and "E" are reference datums and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm (.086 in.)
3. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the cross-hatched area.
4. "L" is the length of the terminal for soldering to a substrate.
5. "N" is the number of terminal positions.

DICE INFORMATION



REF102 DIE TOPOGRAPHY

PAD	FUNCTION
2	V_{CC}
3A	NC
3B	NC
3C	NC
4A	Common (Sense)
4B	Common (Force)
5	Trim
6A	V_{OUT}
6B	V_{OUT} (Feedback)
8	Noise Reduction

Substrate Bias: $-V_{CC}$.

MECHANICAL INFORMATION

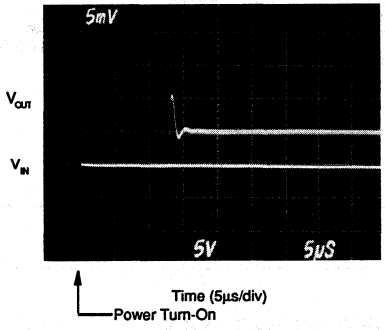
	MILS (0.001")	MILLIMETERS
Die Size	55 x 75 ±5	1.40 x 1.91 ±13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.10 x 0.10
Backing	Gold	

See "DICE PRODUCTS" Section 17 in Data Book Supplement Volume 33c, or contact Burr-Brown for current information.

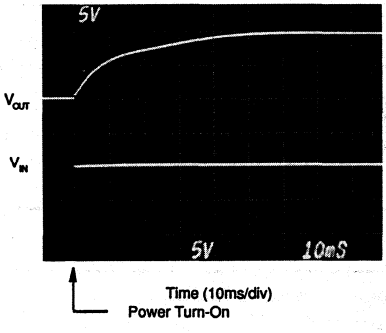
TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_S = +15V unless otherwise noted.

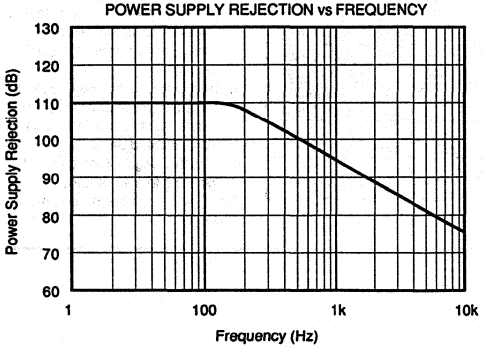
POWER TURN-ON RESPONSE



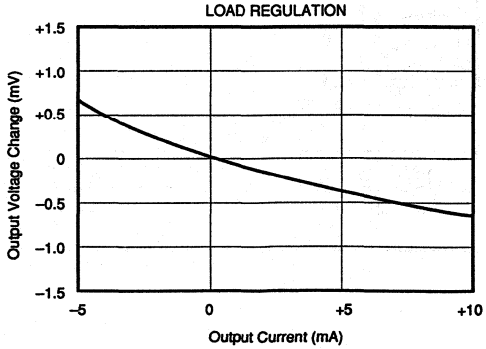
POWER TURN-ON RESPONSE with 1µF Cn



POWER SUPPLY REJECTION vs FREQUENCY



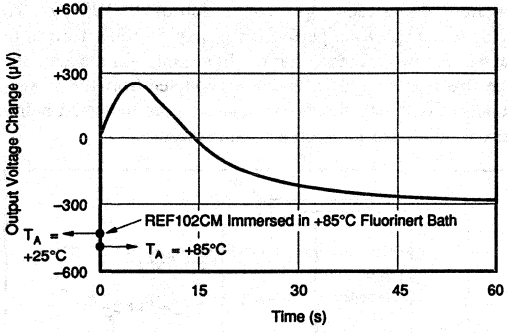
LOAD REGULATION



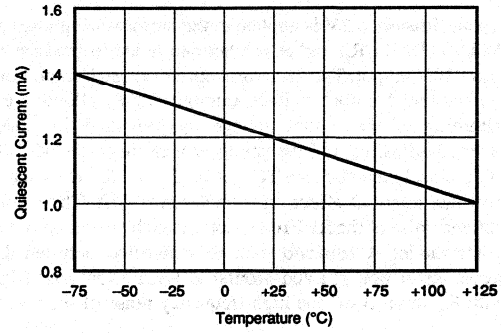
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_S = +15V unless otherwise noted.

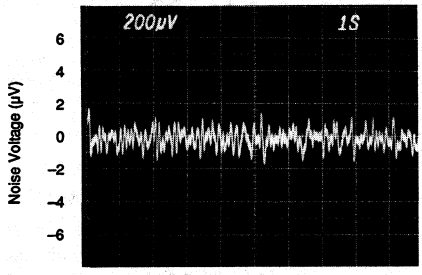
RESPONSE TO THERMAL SHOCK



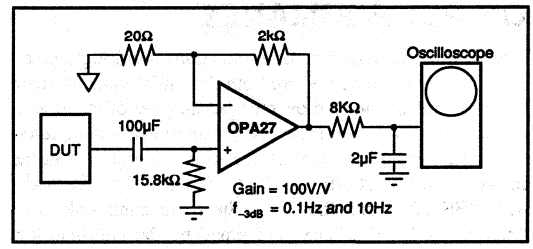
QUIESCENT CURRENT vs TEMPERATURE



TYPICAL REF102 REFERENCE NOISE



Low Frequency Noise (1s /div)
(See Noise Test Circuit)



Noise Test Circuit.

THEORY OF OPERATION

Refer to the diagram on the first page of this data sheet. The 10V output is derived from a compensated buried zener diode DZ_1, op amp A_1, and resistor network R_1–R_6.

Approximately 8.2V is applied to the non-inverting input of A_1 by DZ_1. R_1, R_2, and R_3 are laser-trimmed to produce an exact 10V output. The zener bias current is established from the regulated output voltage through R_4. R_5 allows user-trimming of the output voltage by providing for small external adjustment of the amplifier gain. Because the TCR of R_5 closely matches the TCR of R_1, R_2 and R_3, the voltage trim has minimal effect on the reference drift. The output voltage noise of the REF102 is dominated by the noise of the zener diode. A capacitor can be connected between the Noise Reduction pin and ground to form a low-pass filter with R_6 and roll off the high-frequency noise of the zener.

DISCUSSION OF PERFORMANCE

The REF102 is designed for applications requiring a precision voltage reference where both the initial value at room temperature and the drift over temperature are of importance to the user. Two basic methods of specifying voltage reference drift versus temperature are in common usage in the industry—the "butterfly method" and the "box method." The REF102 is specified with the more commonly used "box method." The "box" is formed by the high and low specification temperatures and a diagonal, the slope of which is equal to the maximum specified drift.

Since the shape of the actual drift curve is not known, the vertical position of the box is not exactly known either. It is, however, bounded by $V_{UPPER\ BOUND}$ and $V_{LOWER\ BOUND}$ (see Figure 1). Figure 1 uses the REF102CM as an example. It has a drift specification of 2.5ppm/°C maximum and a specification temperature range of –25°C to +85°C. The "box" height, V_1 to V_2, is 2.75mV.

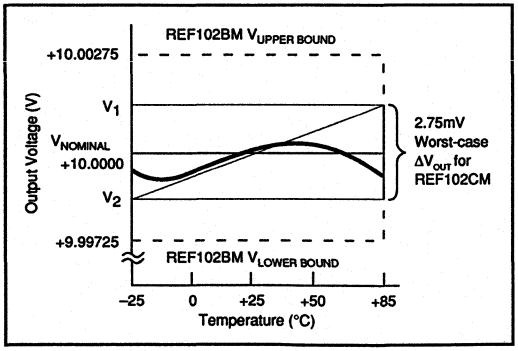


FIGURE 1. REF102CM Output Voltage Drift.

INSTALLATION AND OPERATING INSTRUCTIONS

BASIC CIRCUIT CONNECTION

Figure 2 shows the proper connection of the REF102. To achieve the specified performance, pay careful attention to layout. A low resistance star configuration will reduce voltage errors, noise pickup, and noise coupled from the power-supply. Commons should be connected as indicated being sure to minimize interconnection resistances.

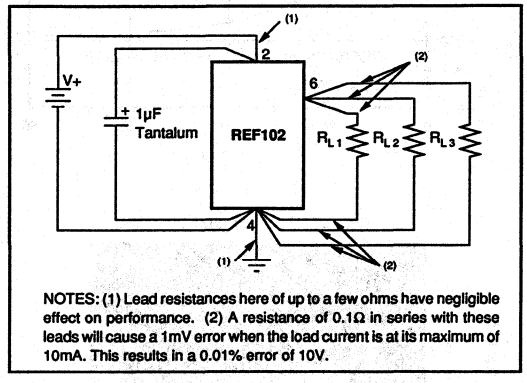


FIGURE 2. REF102 Installation.

OPTIONAL OUTPUT VOLTAGE ADJUSTMENT

Optional output voltage adjustment circuits are shown in Figures 3 and 4. Trimming the output voltage will change the voltage drift by approximately 0.008ppm/°C per mV of trimmed voltage. In the circuit in Figure 3, any mismatch in TCR between the two sections of the potentiometer will also affect drift, but the effect of the ΔTCR is reduced by a factor of five by the internal resistor divider. A high quality potentiometer, with good mechanical stability, such as a cermet, should be used. The circuit in Figure 3 has a minimum trim range of ±300mV. The circuit in Figure 4 has less range but provides higher resolution. The mismatch in TCR between R_S and the internal resistors can introduce some slight drift. This effect is minimized if R_S is kept significantly larger than the 50kΩ internal resistor. A TCR of 100ppm/°C is normally sufficient.

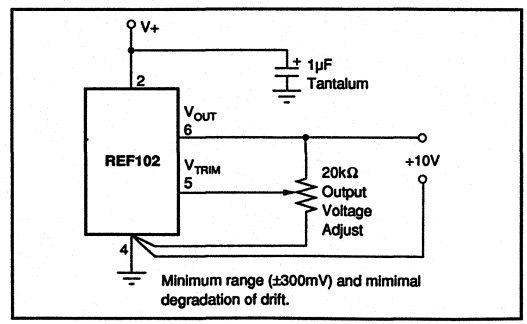


FIGURE 3. REF102 Optional Output Voltage Adjust.

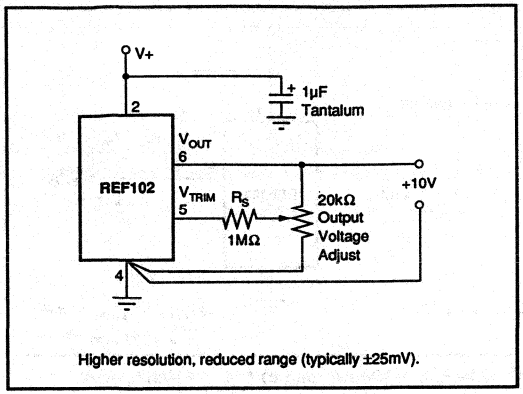


FIGURE 4. REF102 Optional Output Voltage Fine Adjust.

OPTIONAL NOISE REDUCTION

The high-frequency noise of the REF102 is dominated by the zener diode noise. This noise can be greatly reduced by connecting a capacitor between the Noise Reduction pin and ground. The capacitor forms a low pass filter with R_6 (refer to the figure on the first page of the data sheet) and attenuates the high-frequency noise generated by the zener. Figure 5 shows the effect of a 1µF noise reduction capacitor on the high frequency noise of the REF102. R_6 is typically 7kΩ so the filter has a –3dB frequency of about 22Hz. The result is a reduction in noise from about 800µVp-p to under 200µ Vp-p. If further noise reduction is required, use the circuit in Figure 14.

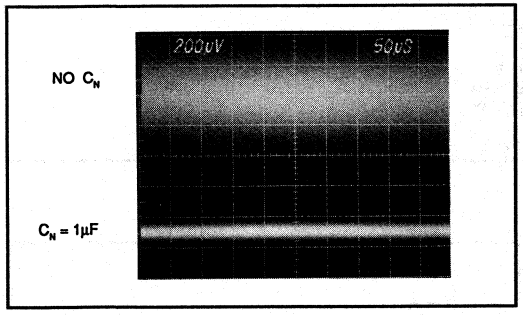


FIGURE 5. Effect of 1µF Noise Reduction Capacitor on Broadband Noise (f_{-3dB} = 1MHz).

APPLICATIONS INFORMATION

High accuracy, extremely low drift, outstanding stability, and low cost make the REF102 an ideal choice for all instrumentation and system reference applications. Figures 6 through 14 show a variety of useful application circuits.

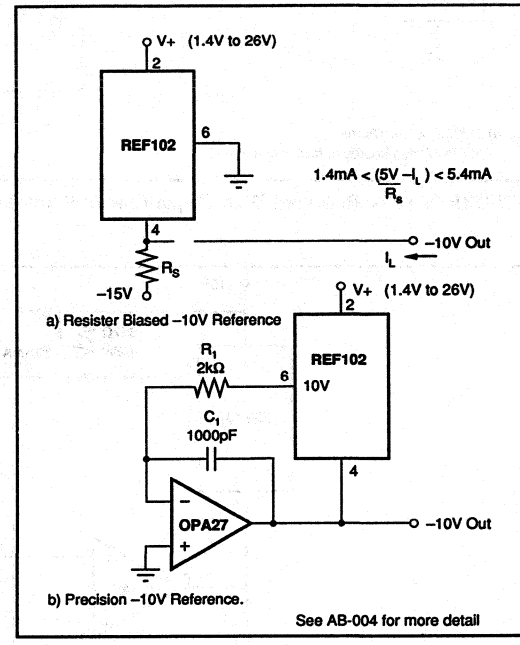


FIGURE 6. –10V Reference Using a) Resistor or b) OPA27.

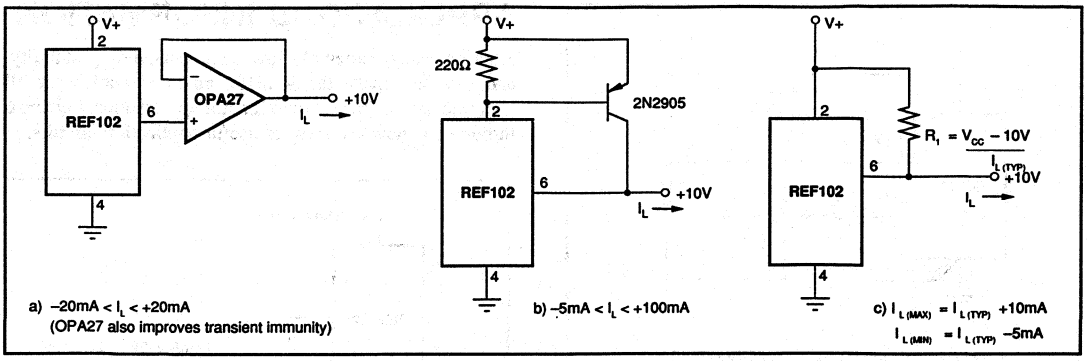


FIGURE 7. +10V Reference With Output Current Boosted to: a) ±20mA, b) +100mA, and c) $I_{L(TYP)}$ +10mA, –5A.

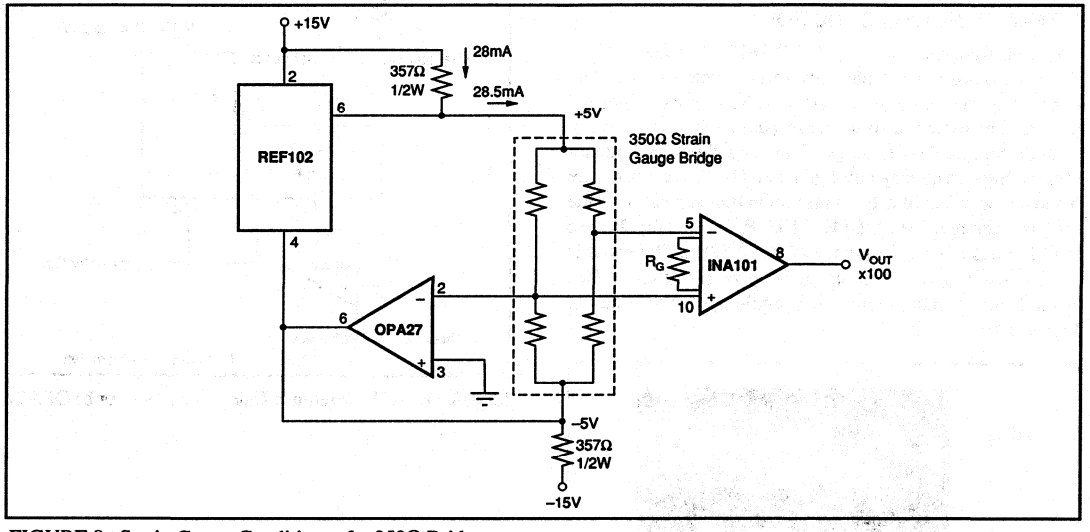


FIGURE 8. Strain Gauge Conditioner for 350Ω Bridge.

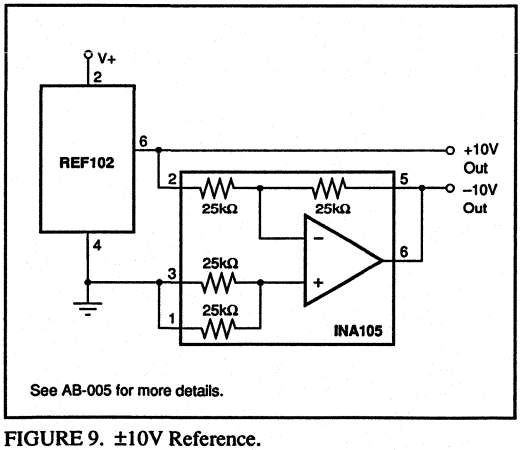


FIGURE 9. ±10V Reference.

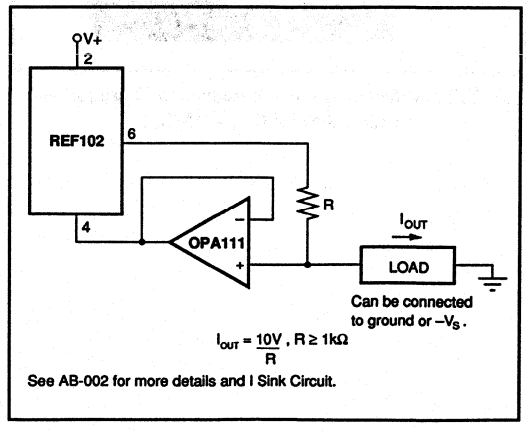
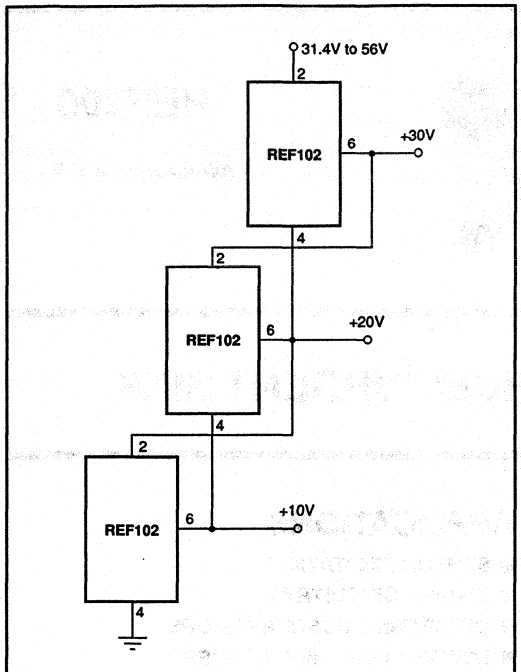


FIGURE 10. Positive Precision Current Source.



NOTES: (1) REF102s can be stacked to obtain voltages in multiples of 10V. (2) The supply voltage should be between 10n + 1.4 and 10n + 26 where n is the number of REF102s. (3) Output current of each REF102 must not exceed its rated output current of +10, –5mA. This includes the current delivered to the lower REF102.

FIGURE 11. Stacked References.

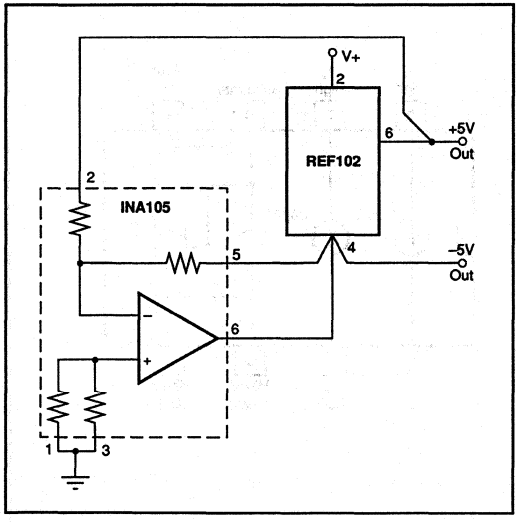


FIGURE 12. ±5V Reference.

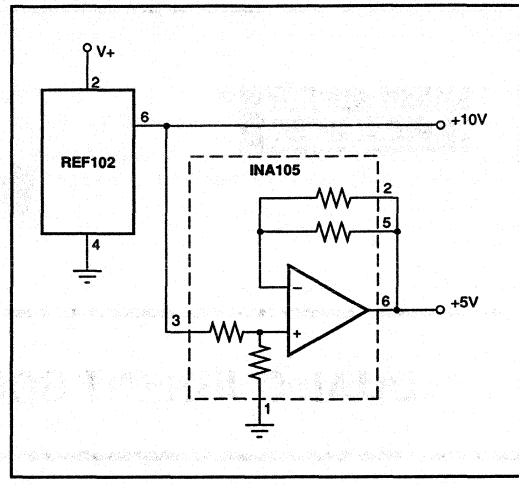


FIGURE 13. +5V and +10V Reference.

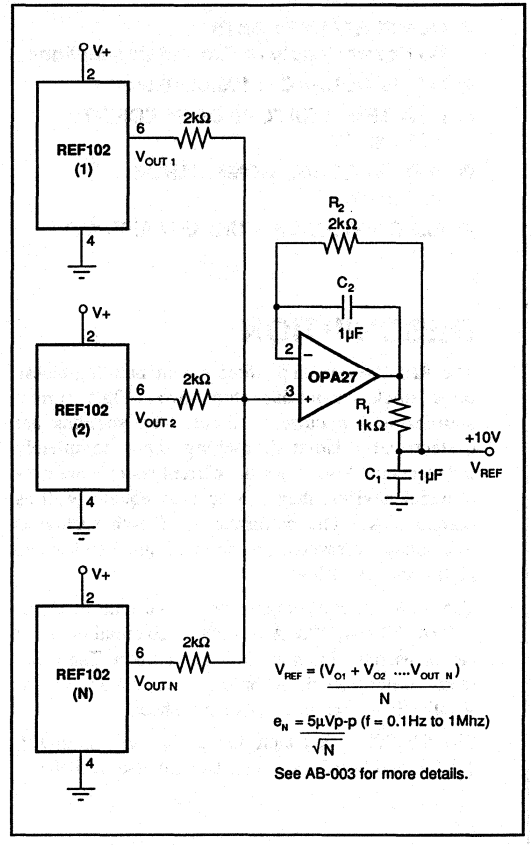


FIGURE 14. Precision Voltage Reference with Extremely Low Noise.

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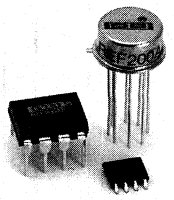


REF200

AVAILABLE IN DIE

DUAL CURRENT SOURCE/CURRENT SINK

FEATURES

- **COMPLETELY FLOATING: No Power Supply or Ground Connections**
- **HIGH ACCURACY: 100µA ±0.5%**
- **LOW TEMPERATURE COEFFICIENT: ±25ppm/°C**
- **WIDE VOLTAGE COMPLIANCE: 2.5V to 40V**
- **ALSO INCLUDES CURRENT MIRROR**

APPLICATIONS

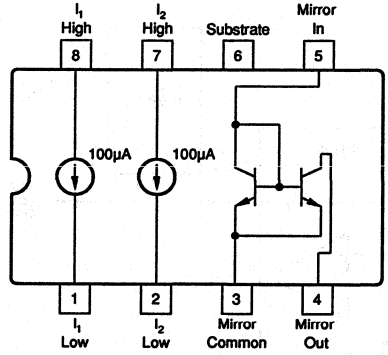
- **SENSOR EXCITATION**
- **BIASING CIRCUITRY**
- **OFFSETTING CURRENT LOOPS**
- **LOW VOLTAGE REFERENCES**
- **CHARGE-PUMP CIRCUITRY**
- **HYBRID MICROCIRCUITS**

DESCRIPTION

The REF200 combines three circuit building-blocks on a single monolithic chip—two 100µA current sources and a current mirror. The sections are dielectrically isolated, making them completely independent. Also, since the current sources are two-terminal devices, they can be used equally well as current sinks. The performance of each section is individually measured and laser-trimmed to achieve high accuracy at low cost.

The sections can be pin-strapped for currents of 50µA, 100µA, 200µA, 300µA or 400µA. External circuitry can be used to obtain virtually any current. These and many other circuit techniques are shown in the Applications section of this Data Sheet.

The REF200 is available in plastic 8-pin mini-DIP, TO-99, and SOIC packages. Die are also available.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

PDS-851A

SPECIFICATIONS

ELECTRICAL

T_A = +25°C, V_S = 15V unless otherwise noted.

PARAMETER	CONDITION	REF200AM MIN	REF200AM TYP	REF200AM MAX	REF200AP, AU MIN	REF200AP, AU TYP	REF200AP, AU MAX	UNITS
CURRENT SOURCES								
Current Accuracy			±0.1	±0.5		±0.25	±1	%
Current Match			±0.05	±0.5		±0.25	±1	%
Temperature Drift	Specified Temp Range		25			*		ppm/°C
Output Impedance	2.5V to 40V	20	100		*	*		MΩ
	3.5V to 30V	200	500		*	*		MΩ
Noise	BW = 0.1Hz to 10Hz		1			*		nAp-p
	f = 10kHz		20			*		pA/√Hz
Voltage Compliance (1%)	T_{MIN} to T_{MAX}		See Curves					
Capacitance			10			*		pF
CURRENT MIRROR	I = 100µA Unless Otherwise Noted							
Gain		0.995	1	1.005	*	*	*	
Temperature Drift			25			*		ppm/°C
Impedance (output)	2V to 40V	40	100		*	*		MΩ
Nonlinearity	I = 0µA to 250µA		0.05			*		%
Input Voltage			1.4			*		V
Output Compliance Voltage			See Curves					
Frequency Response (–3dB)	Transfer		5			*		MHz
TEMPERATURE RANGE								
Specification		–25		+85	*		*	°C
Operating		–55		+125	–40		+85	°C
Storage		–60		+150	–40		+125	°C

*Specification same as REF200AM.

ORDERING INFORMATION

MODEL[1]	TEMPERATURE PACKAGE	RANGE
REF200AM	TO-99	–25°C to +85°C
REF200AP	Plastic DIP	–25°C to +85°C
REF200AU	Plastic SOIC	–25°C to +85°C

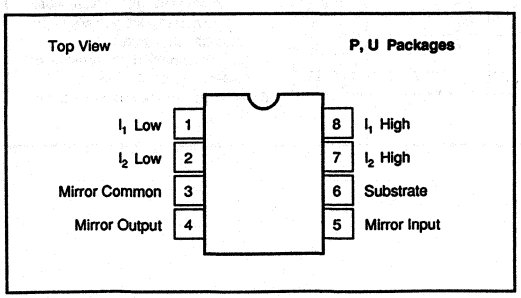
NOTE: (1) Grade designation "A" may not be marked. Absence of grade designation indicates A grade.

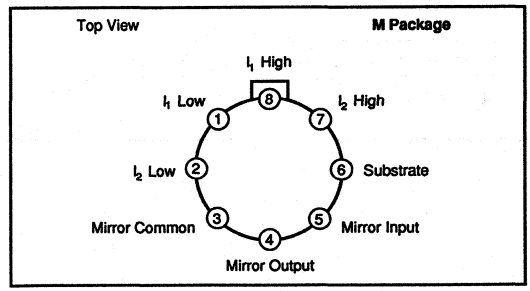
ABSOLUTE MAXIMUM RATINGS

Applied Voltage ..... –6V to +40V
Reverse Current ..... –350µA
Voltage Between Any Two Sections ..... ±80V
Operating Temperature
  M Package ..... –55°C to +125°C
  P and U Packages ..... –40°C to +85°C
Storage Temperature
  M Package ..... –60°C to +150°C
  P and U Packages ..... –40°C to +125°

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

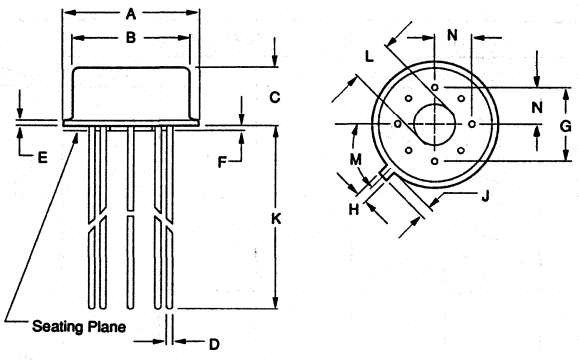
PIN CONFIGURATION





MECHANICAL

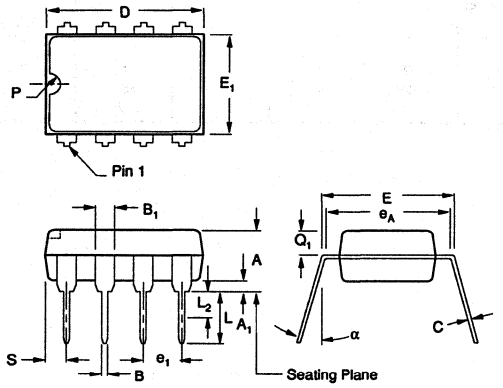
M Package — Metal TO-99



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.335	.370	8.51	9.40
B	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.200 BASIC		5.08 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500	—	12.7	—
L	.110	.160	2.79	4.06
M	45° BASIC		45° BASIC	
N	.095	.105	2.41	2.67

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Tab is pin 8.

P Package — 8-Pin Plastic DIP

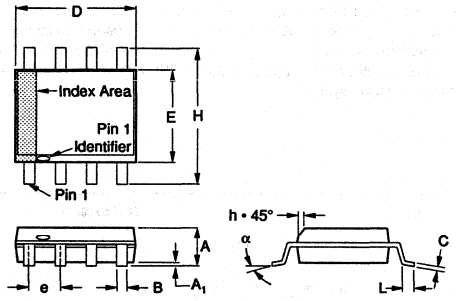


DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.155	.200	3.94	5.08
A1	.020	.050	0.51	1.27
B	.014	.020	0.36	0.51
B1	.045	.065	1.14	1.65
C	.008	.012	0.20	0.30
D (1)	.370	.400	9.40	10.16
E	.300	.325	7.62	8.26
E1	.240	.260	6.10	6.60
e1	.100 BASIC		2.54 BASIC	
eA	.300 BASIC		7.62 BASIC	
L	.125	.150	3.18	3.81

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
L2(2)	0	.030	0.00	0.76
α	0°	15°	0°	15°
P	.015	.050	0.38	1.270
Q1	.040	.075	1.02	1.91
S (1)	.015	.050	0.38	1.27

(1) Not JEDEC Std.
(2) e_1 and e_A apply in zone L_2 when unit installed.
NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

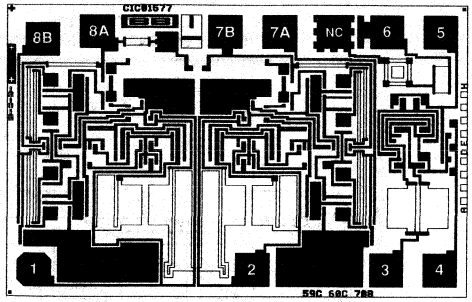
U Package — 8-Pin SO-8 Surface Mount



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.054	.068	1.37	1.73
A1	.004	.009	0.10	0.23
B	.014	.019	0.36	0.48
C	.008	.0098	0.20	0.25
D	.189	.196	4.80	4.98
E	.150	.157	3.81	3.99
e	.050 BASIC		1.27 BASIC	
H	.229	.244	5.82	6.20
h	.010	.019	0.25	0.48
L	.016	.050	0.41	1.27
N	8		8	
α	0°	8°	0°	8°

NOTES:
1. Dimensioning and tolerancing per ANSI Y14.5M–1982.
2. "D" and "E" are reference datums and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm (.086 in.)
3. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the cross-hatched area.
4. "L" is the length of the terminal for soldering to a substrate.
5. "N" is the number of terminal positions.

DICE INFORMATION



REF200 DIE TOPOGRAPHY

PAD	FUNCTION	PAD	FUNCTION
1	I_1 Low	6	Substrate
2	I_2 Low	7A	I_2 High
3	Mirror Common	7B	I_1 High
4	Mirror Output	8A	I_1 High
5	Mirror Input	8B	I_2 High

Substrate Bias: $+V_{CC}$. (Major change anticipated in near future, contact factory for recommendation.)

MECHANICAL INFORMATION

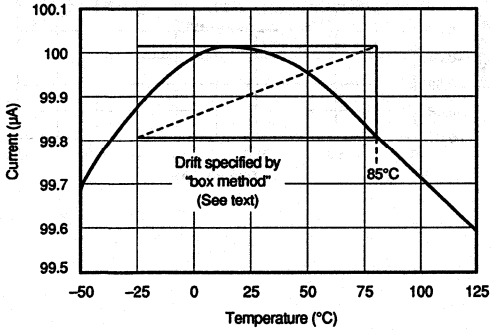
	MILS (0.001")	MILLIMETERS
Die Size	48 x 72 ±5	1.22 x 1.83 ±13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.10 x 0.10
Backing	None	

See "DICE PRODUCTS" Section 17 in Data Book Supplement Volume 33c, or contact Burr-Brown for current information.

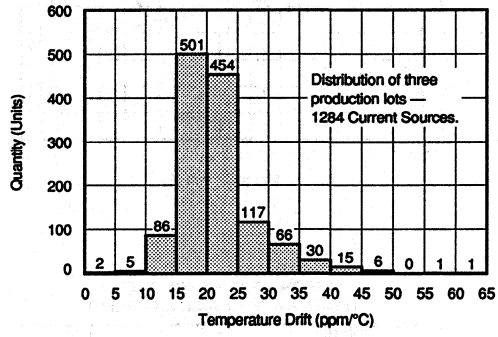
TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_S = +15V unless otherwise noted.

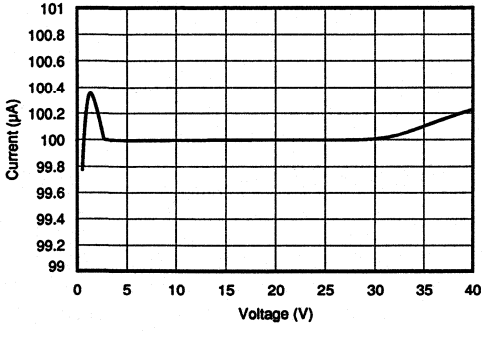
CURRENT SOURCE
TYPICAL DRIFT vs TEMPERATURE



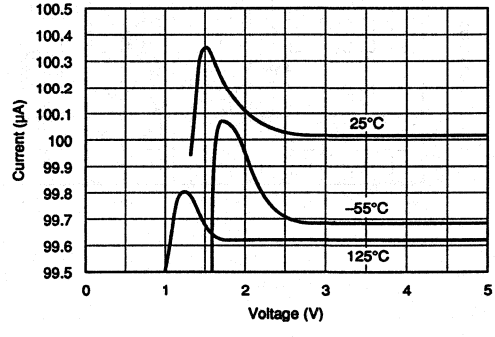
CURRENT SOURCE
TEMPERATURE DRIFT DISTRIBUTION



CURRENT SOURCE
OUTPUT CURRENT vs VOLTAGE



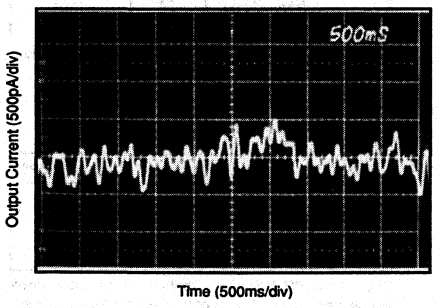
CURRENT SOURCE
OUTPUT CURRENT vs VOLTAGE



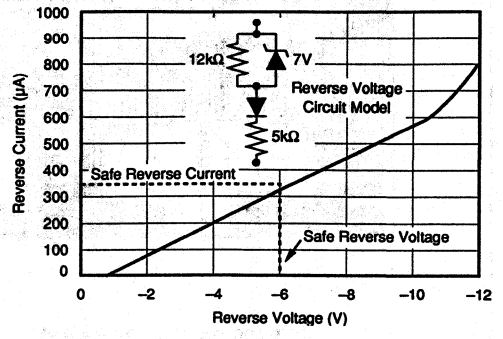
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_S = +15V unless otherwise noted.

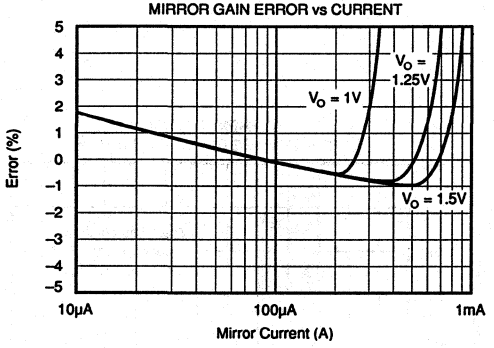
CURRENT SOURCE
CURRENT NOISE (0.1Hz to 10Hz)



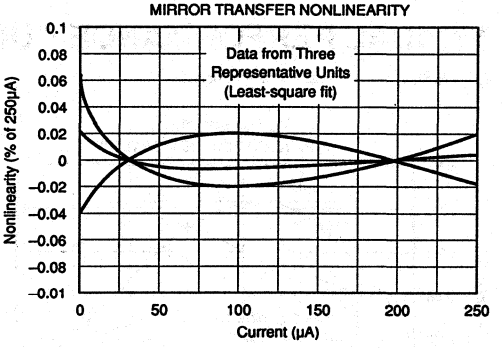
CURRENT SOURCE
REVERSE CURRENT vs REVERSE VOLTAGE



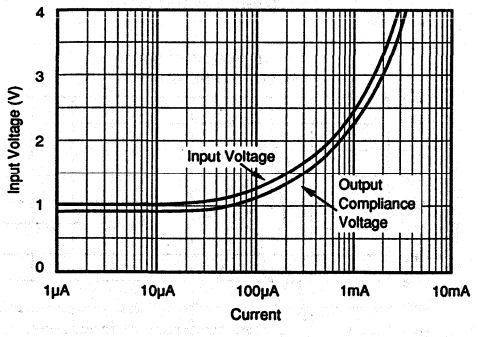
MIRROR GAIN ERROR vs CURRENT



MIRROR TRANSFER NONLINEARITY



MIRROR INPUT VOTAGE/OUTPUT
COMPLIANCE VOLTAGE vs CURRENT



APPLICATIONS INFORMATION

The three circuit sections of the REF200 are electrically isolated from one another using a dielectrically isolated fabrication process. A substrate connection is provided (pin 6), which is isolated from all circuitry. This pin should be connected to a defined circuit potential to assure rated DC performance. The preferred connection is to the most positive constant potential in your system. In most analog systems this would be $+V_S$. For best AC performance, leave pin 6 open and leave unused sections unconnected.

Drift performance is specified by the "box method," as illustrated in the Current vs Temperature plot of the typical performance curves. The upper and lower current extremes measured over temperature define the top and bottom of the box. The sides are determined by the specified temperature range of the device. The drift of the unit is the slope of the diagonal—typically 25ppm/°C from –25°C to +85°C.

If the current sources are subjected to reverse voltage, a protection diode may be required. A reverse voltage circuit model of the REF200 is shown in the Reverse Current vs Reverse Voltage curve. If reverse voltage is limited to less than 6V *or* reverse current is limited to less than 350µA, no protection circuitry is required. A parallel diode (Figure 2a) will protect the device by limiting the reverse voltage across the current source to approximately 0.7V. In some applications, a series diode may be preferable (Figure 2b) because it allows no reverse current. This will, however, reduce the compliance voltage range by one diode drop.

Applications for the REF200 are limitless. Application guide AN-165 shows additional REF200 circuits as well as other related current source techniques. A collection of circuits is shown to illustrate some techniques. Also, see AN-165A.

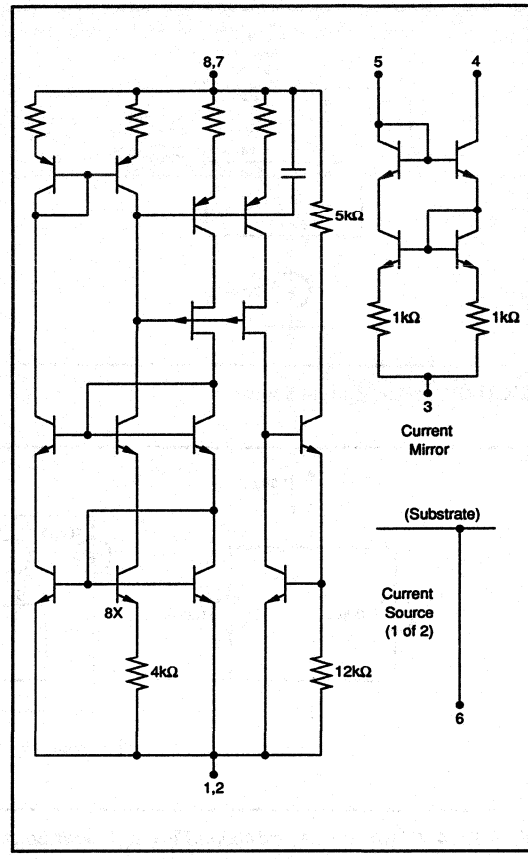


FIGURE 1. Simplified Circuit Diagram.

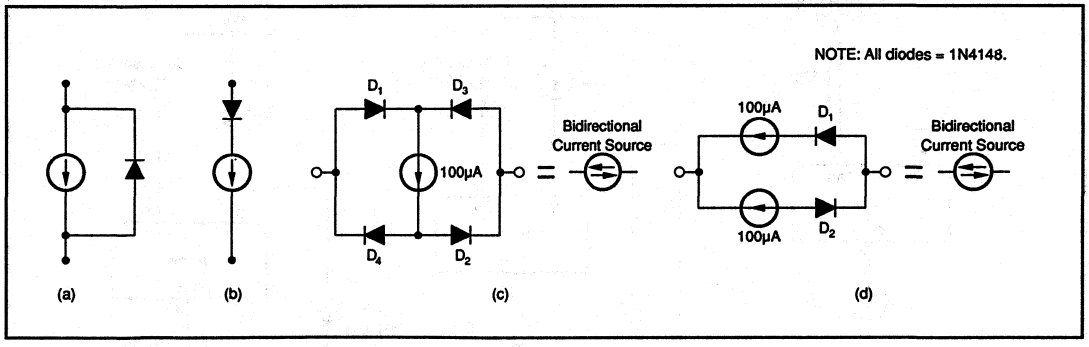


FIGURE 2. Reverse Voltage Protection.

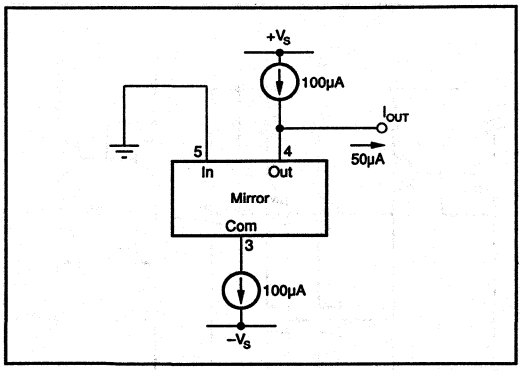


FIGURE 3. 50µA Current Source.

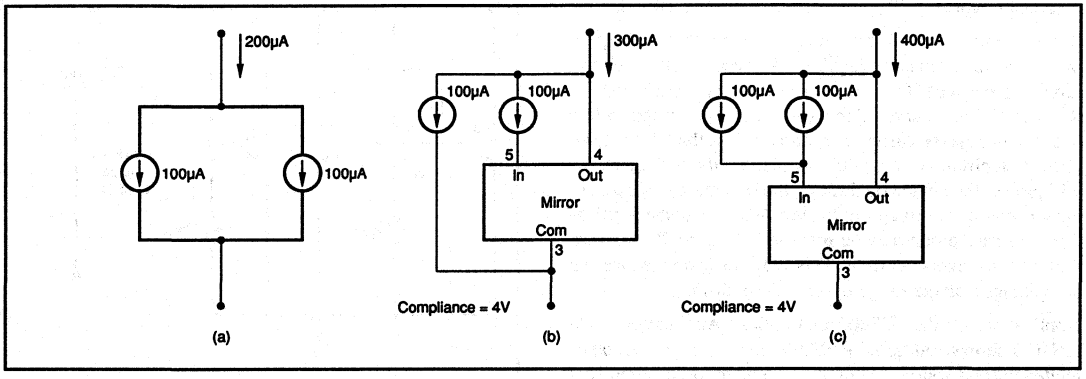


FIGURE 4. 200µA, 300µA, and 400µA Floating Current Sources.

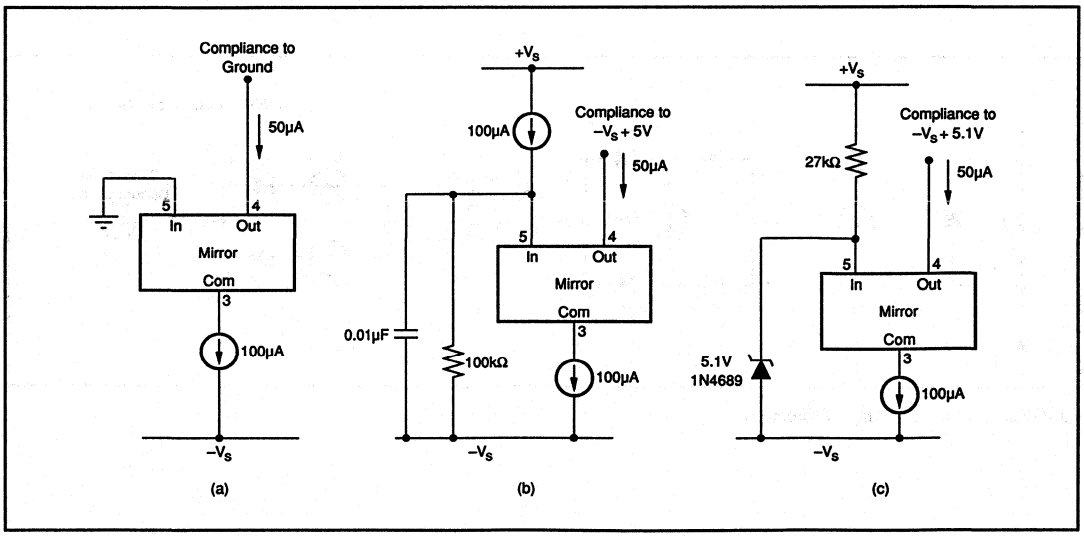


FIGURE 5. 50µA Current Sinks.

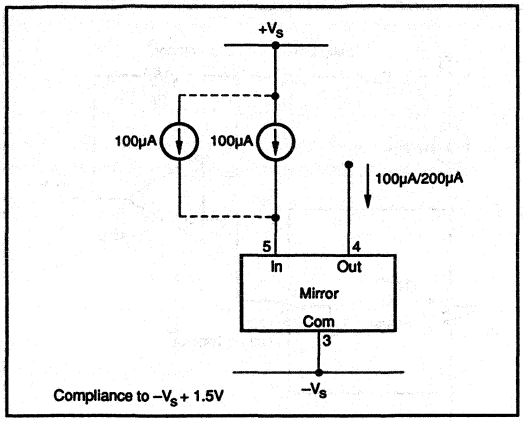


FIGURE 6. Improved Low-Voltage Compliance.

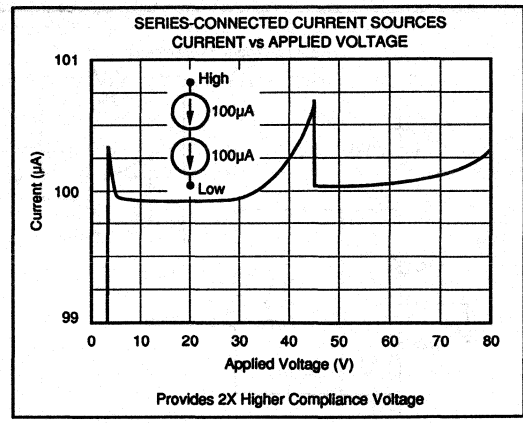


FIGURE 7. 100µA Current Source—80V Compliance.

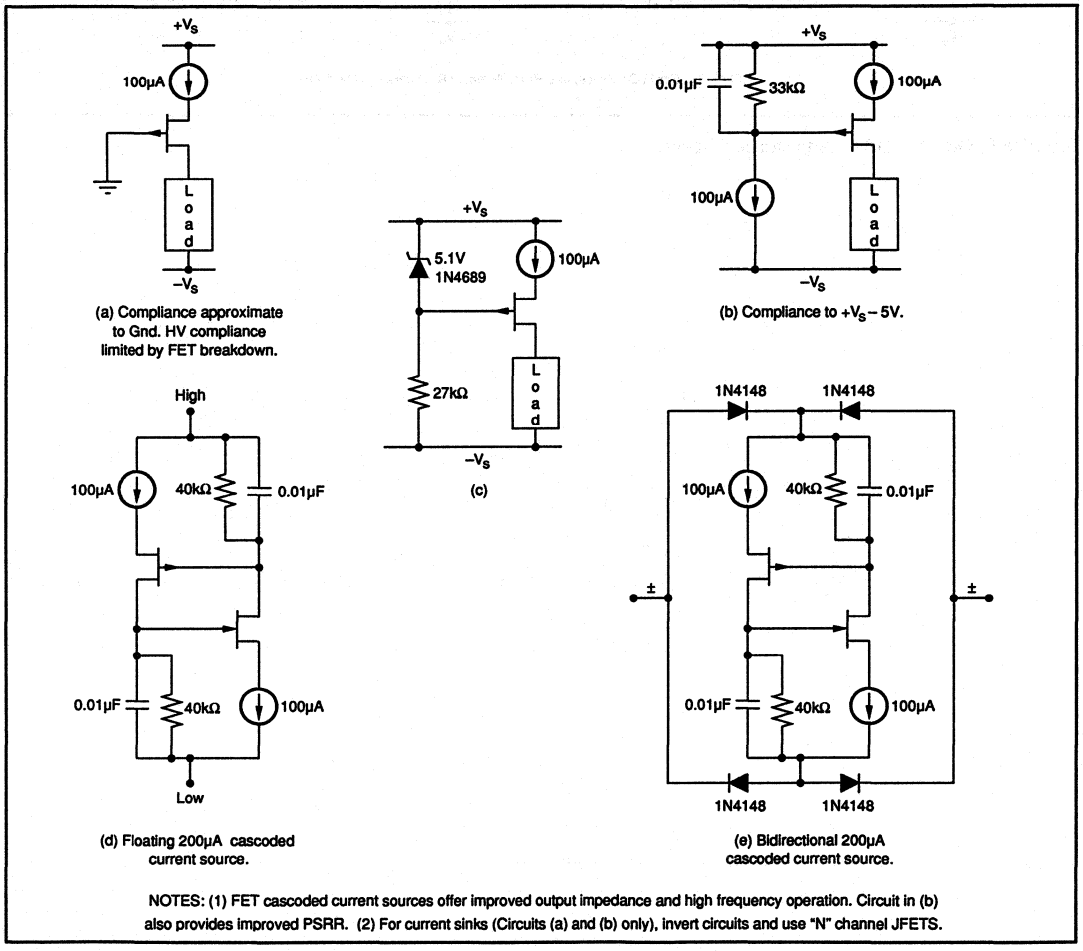


FIGURE 8. FET Cascode Circuits.

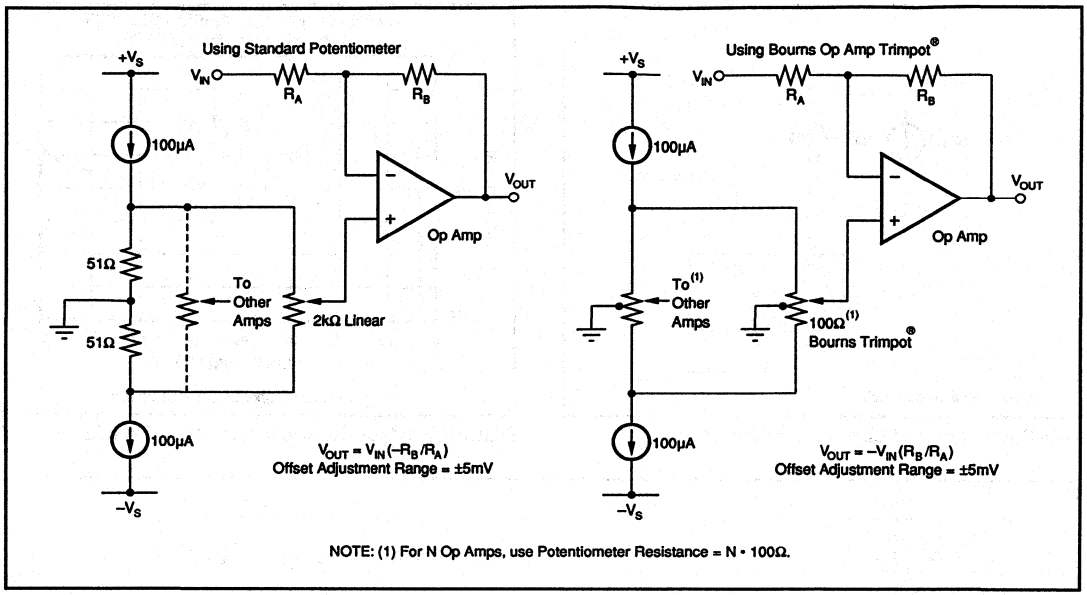


FIGURE 9. Op Amp Offset Adjustment Circuits.

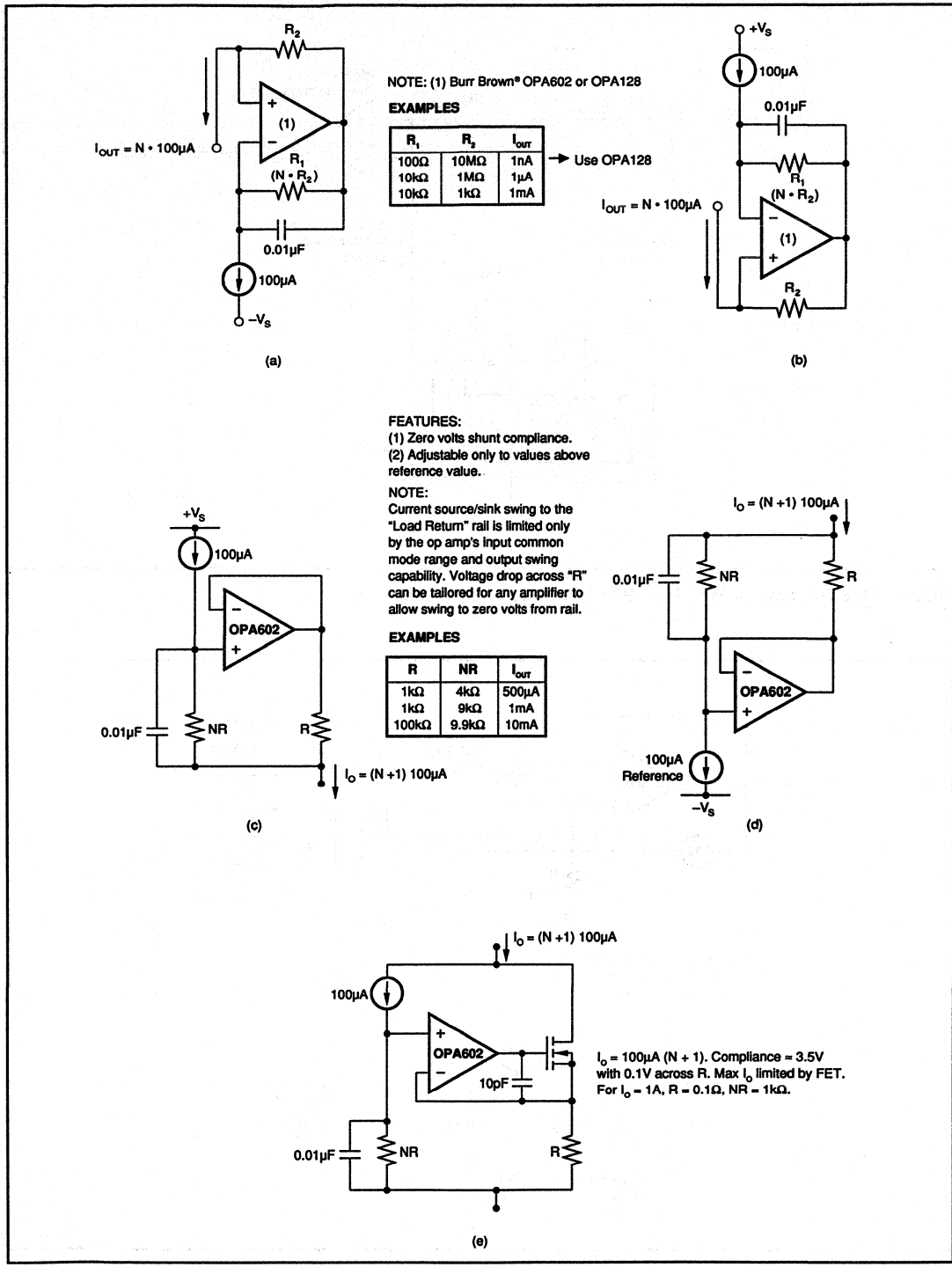


FIGURE 10. Adjustable Current Sources.

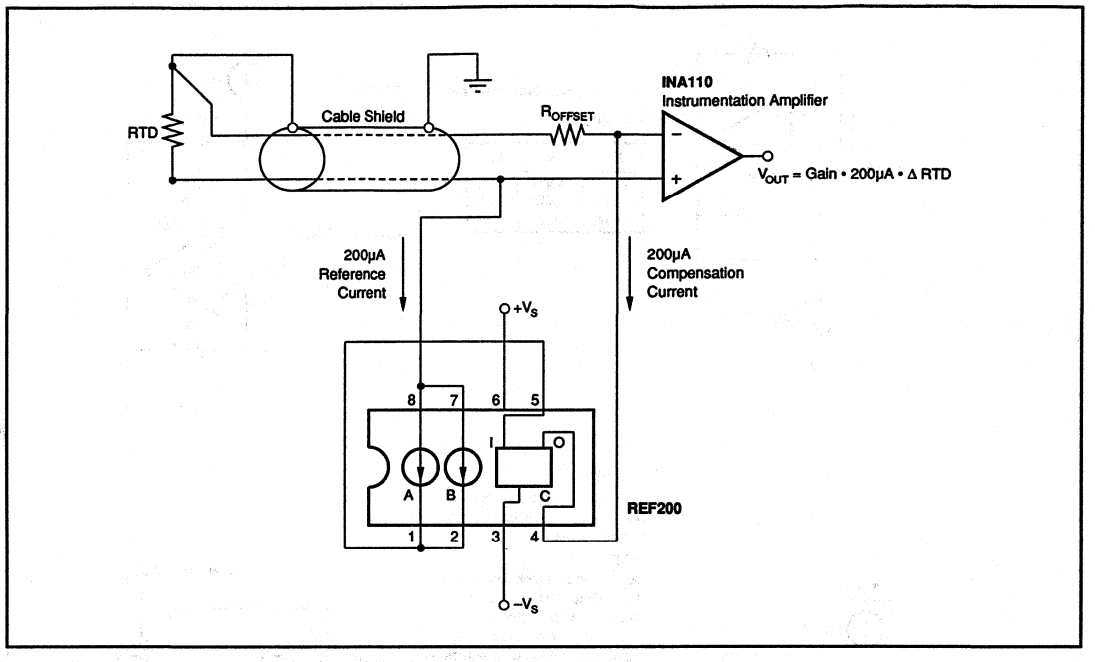


FIGURE 11. RTD Excitation With Three Wire Lead Resistance Compensation.

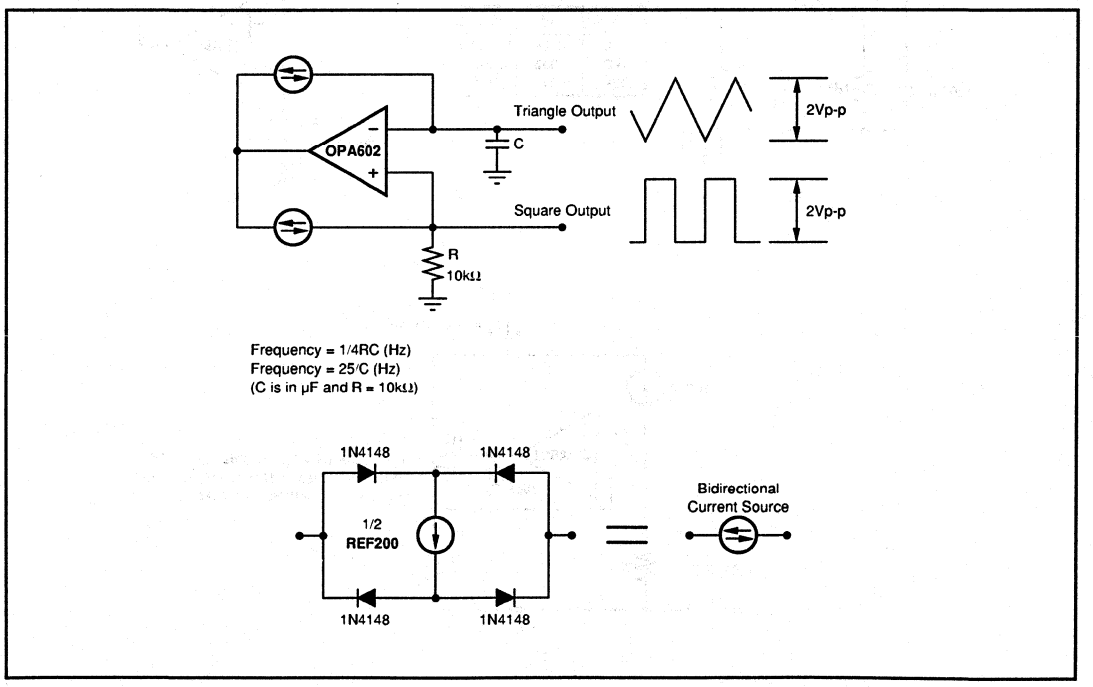


FIGURE 12. Precision Triangle Waveform Generator.

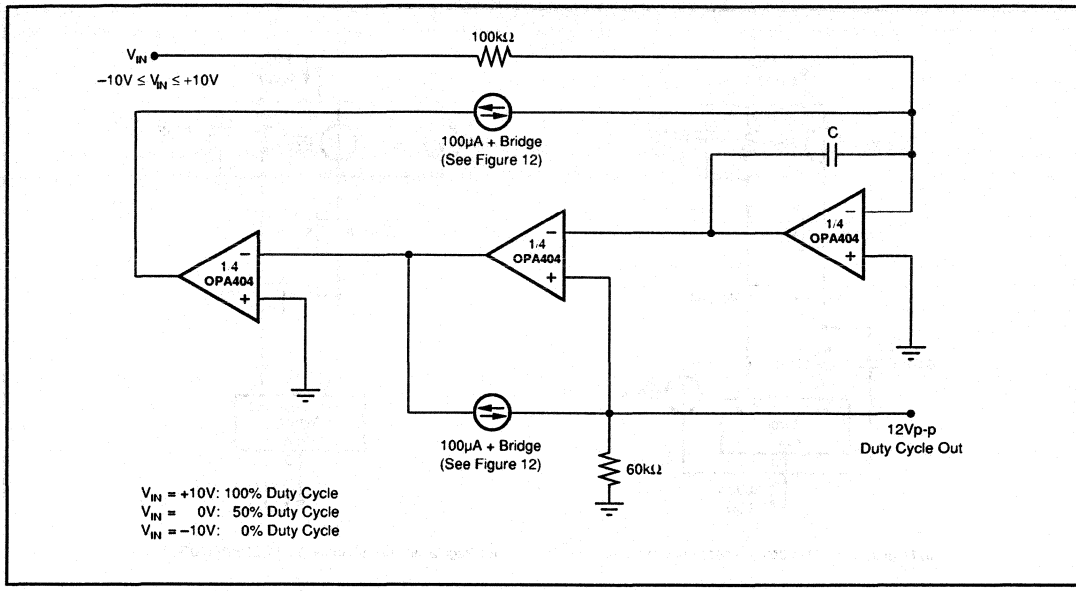


FIGURE 13. Precision Duty-Cycle Modulator.

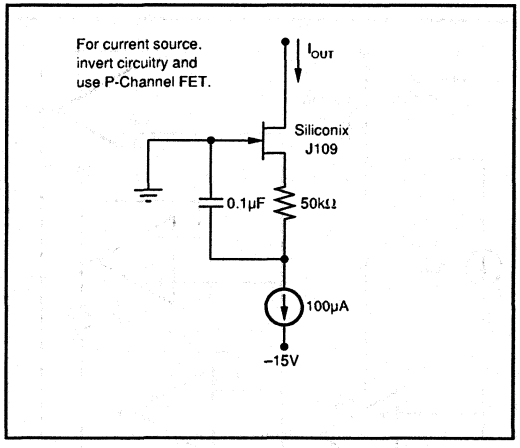


FIGURE 14. Low Noise Current Sink.

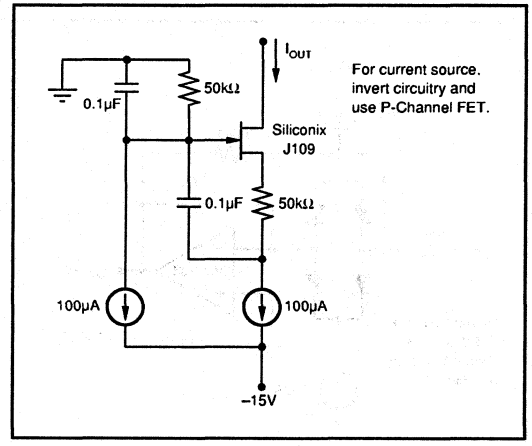


FIGURE 15. Low Noise Current Sink with Compliance Below Ground.

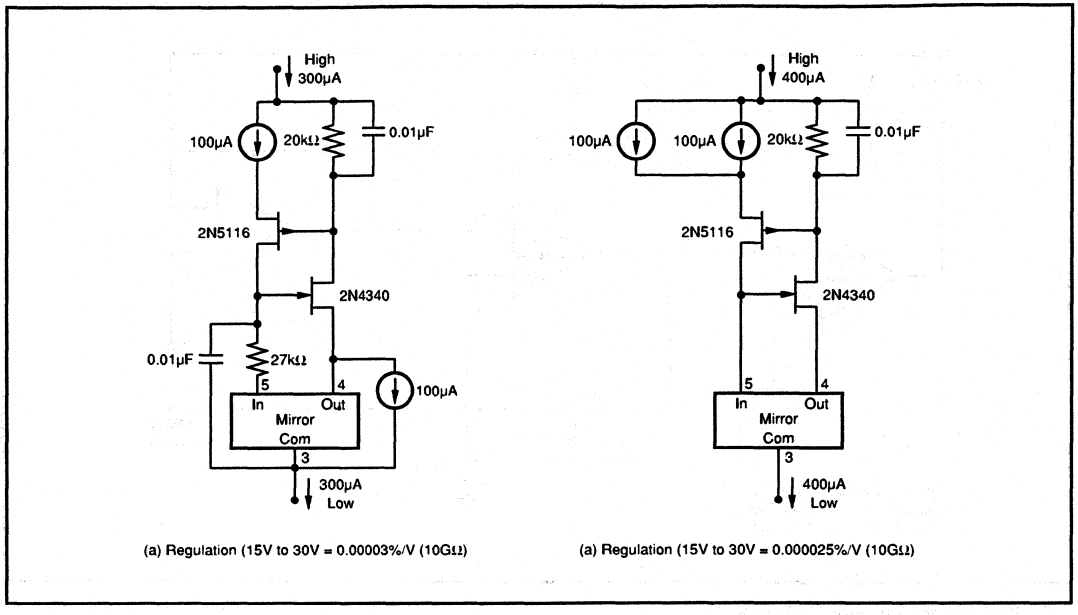


FIGURE 16. Floating 300µA and 400µA Cascoded Current Sources.

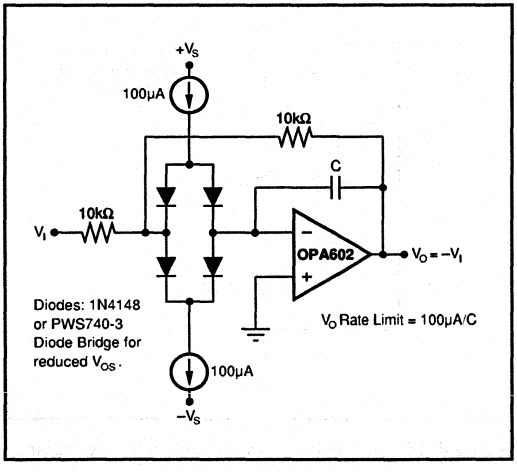


FIGURE 17. Rate Limiter.

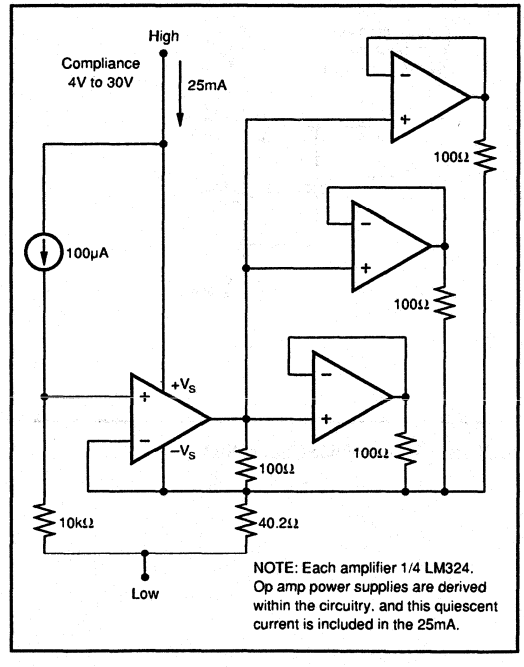


FIGURE 18. 25mA Floating Current Source.

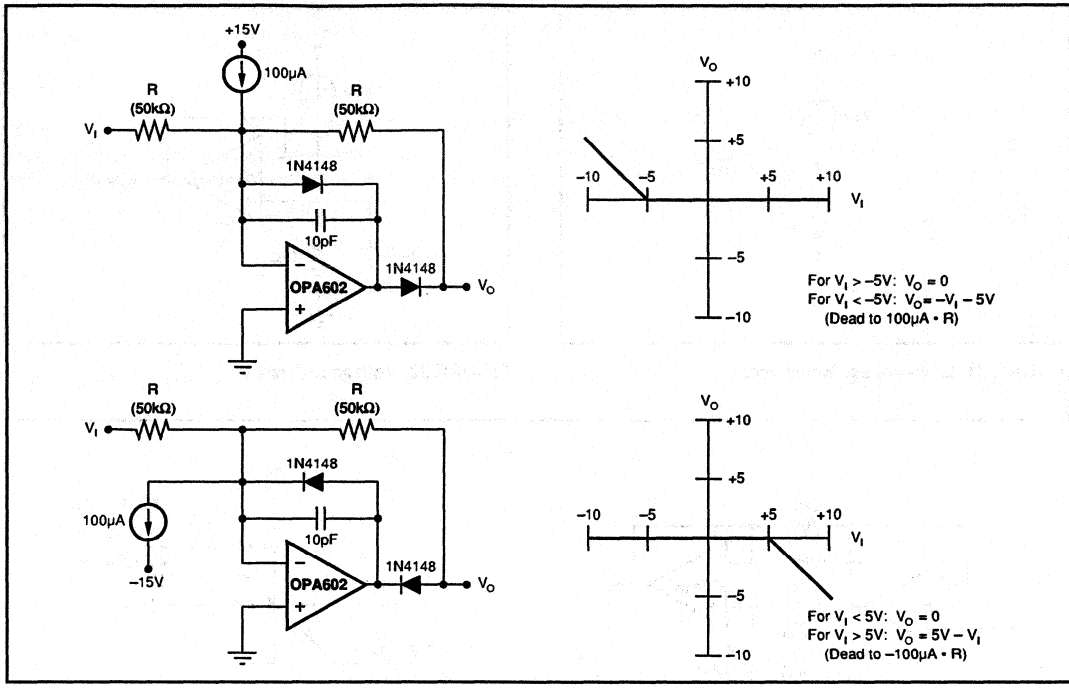


FIGURE 19. Dead-Band Circuit.

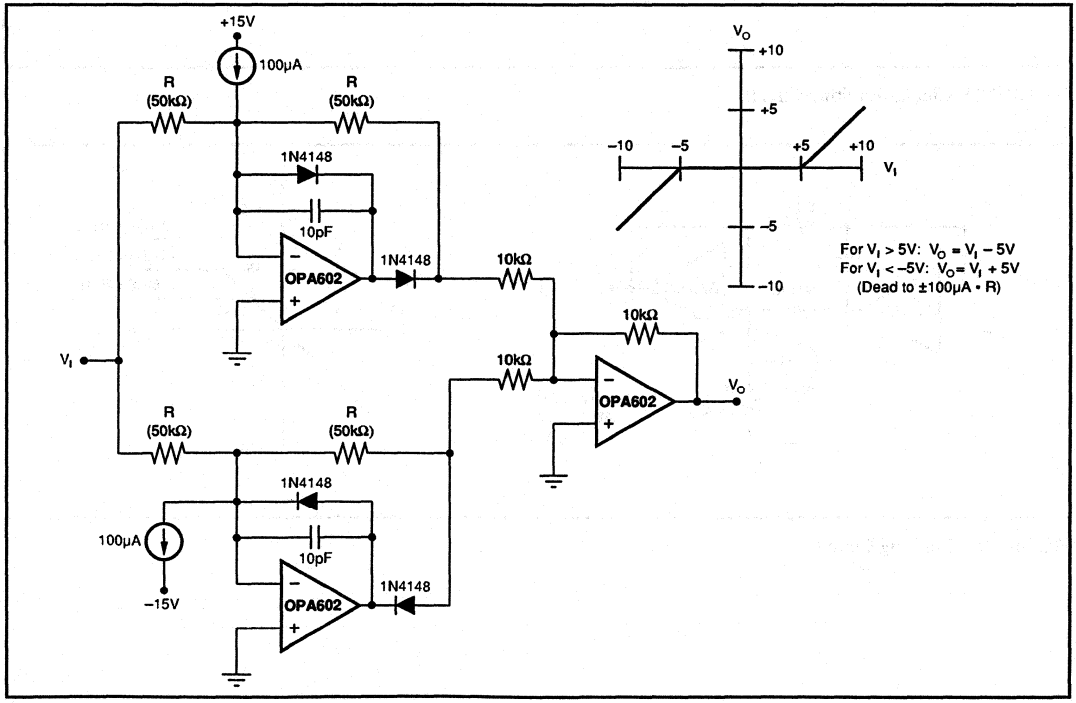


FIGURE 20. Double Dead-Band Circuit.

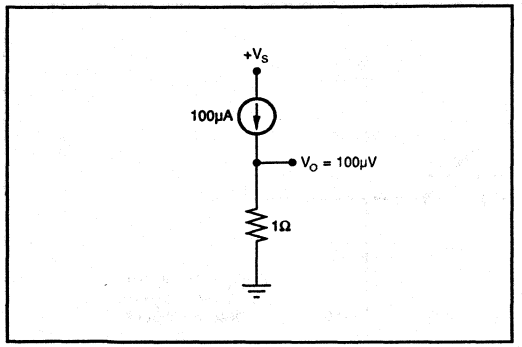


FIGURE 21. Low-Voltage Reference.

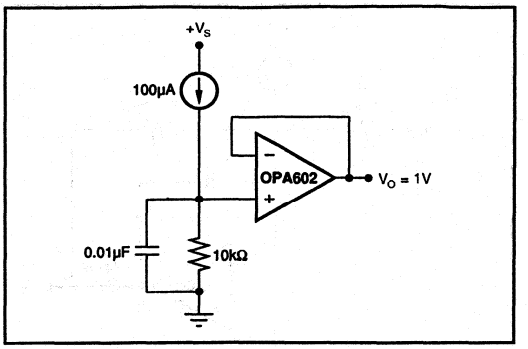


FIGURE 22. Voltage Reference.

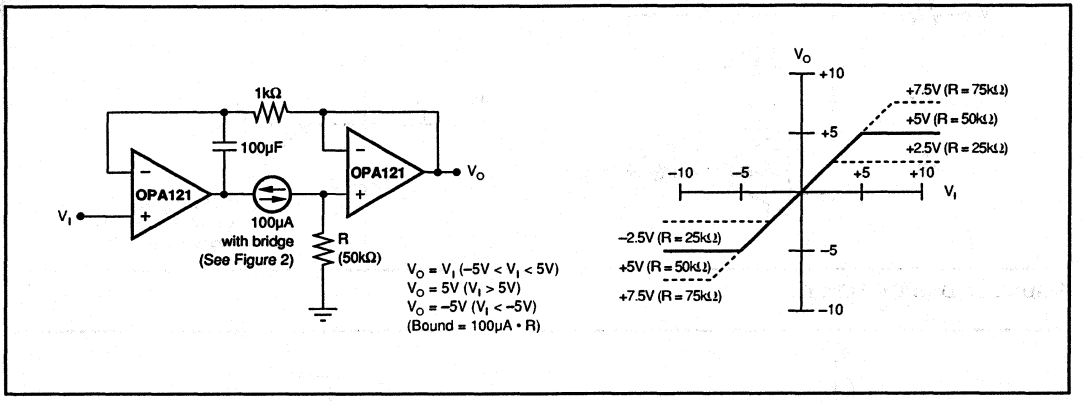


FIGURE 23. Bipolar Limiting Circuit.

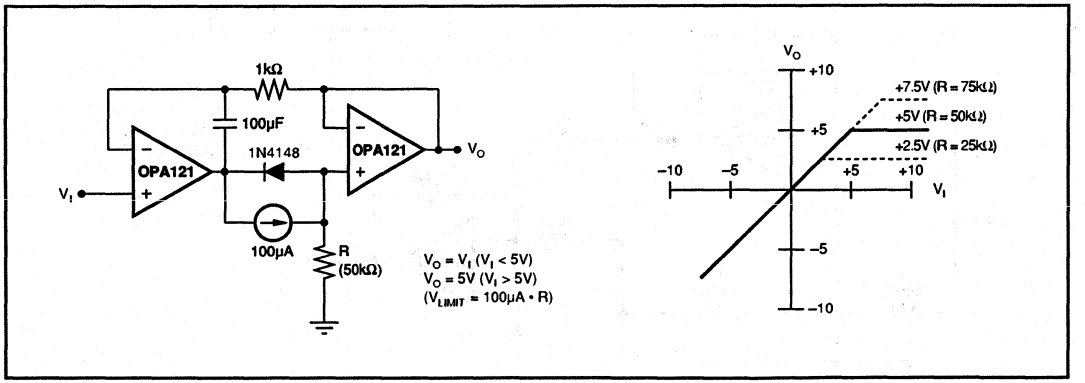


FIGURE 24. Limiting Circuit.

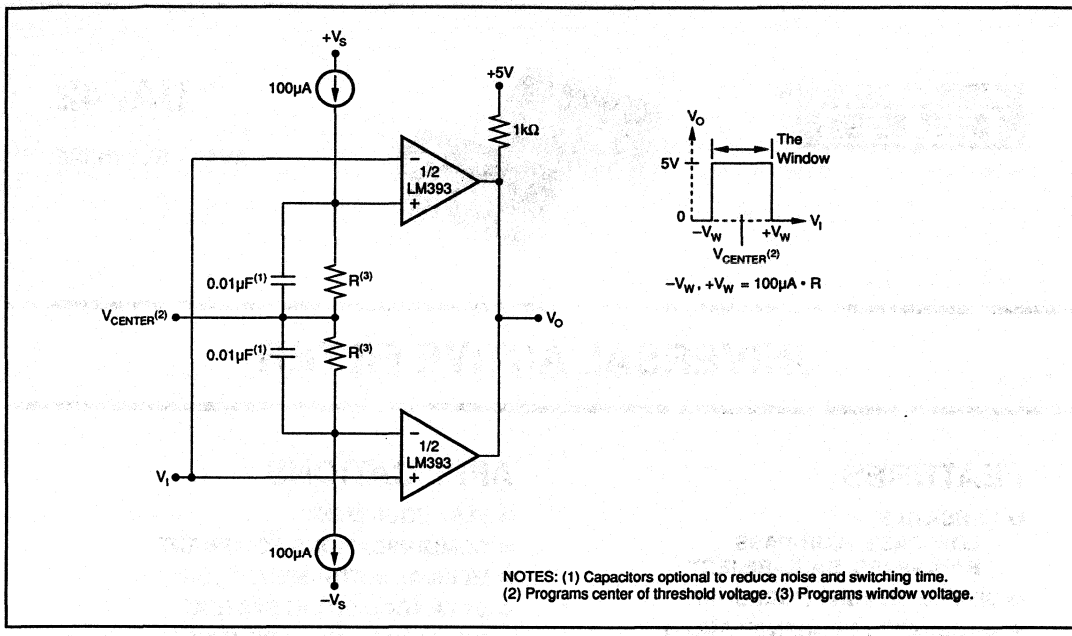


FIGURE 25. Window Comparator.

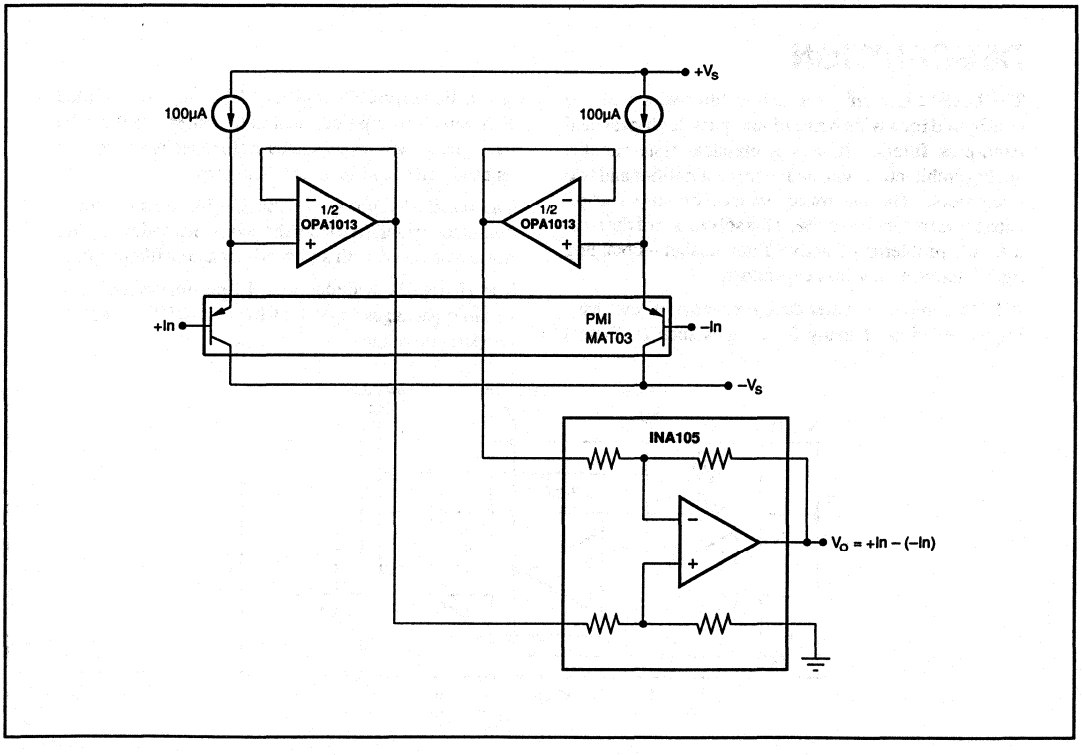


FIGURE 26. Instrumentation Amplifier with Compliance to $-V_S$.

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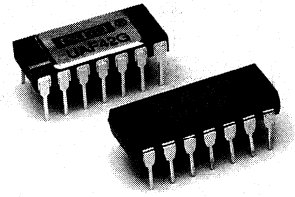


UAF42

AVAILABLE IN DIE

UNIVERSAL ACTIVE FILTER

FEATURES

- VERSATILE—
  LOW-PASS, HIGH-PASS
  BAND-PASS, BAND-REJECT
- SIMPLE DESIGN PROCEDURE
- ACCURATE FREQUENCY AND Q
  INCLUDES ON-CHIP 1000pF ±0.5%
  CAPACITORS

APPLICATIONS

- TEST EQUIPMENT
- COMMUNICATIONS EQUIPMENT
- MEDICAL INSTRUMENTATION
- DATA ACQUISITION SYSTEMS
- MONOLITHIC REPLACEMENT FOR UAF41

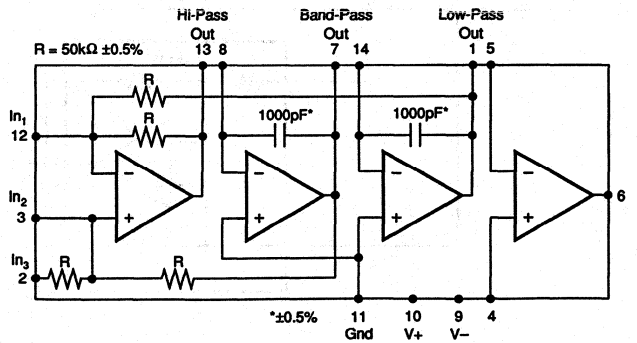
DESCRIPTION

The UAF42 is a universal active filter which can be configured for a wide range of low-pass, high-pass, and band-pass filters. It uses a classical state-variable analog architecture with an inverting amplifier and two integrators. The integrators include on-chip 1000pF capacitors trimmed to 0.5%. This solves one of the most difficult problems of active filter design—obtaining tight tolerance, low-loss capacitors.

A DOS-compatible filter design program allows easy implementation of many filter types such as Butterworth, Bessel, and Chebyshev. A fourth, uncommitted FET-input op amp (identical to the other three) can be used to form additional stages, or for special filters such as band-reject and Inverse Chebyshev.

The classical topology of the UAF42 forms a time-continuous filter, free from the anomalies and switching noise associated with switched-capacitor filter types.

The UAF42 is available in a 14-pin plastic DIP and ceramic packages, specified for the –25°C to +85°C temperature range.



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Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

PDS-1070C

SPECIFICATIONS

T_A = +25°C, V_S = ±15V unless otherwise noted.

PARAMETER	CONDITION	UAF42AP MIN	UAF42AP TYP	UAF42AP MAX	UAF42AG MIN	UAF42AG TYP	UAF42AG MAX	UNITS
FILTER PERFORMANCE								
Frequency Range, fn			0 to 100			*		kHz
Frequency Accuracy	f = 1kHz			1			2	%
vs Temperature			0.01			*		%/°C
Maximum Q			400			*		—
Maximum (Q • Frequency) Product			500			*		kHz
Q vs Temperature	$(f_0 \cdot Q) < 10^4$		0.01			*		%/°C
	$(f_0 \cdot Q) < 10^5$		0.025			*		%/°C
Q Repeatability	$(f_0 \cdot Q) < 10^5$		2			*		%
Offset Voltage, Low-Pass Output				±5			*	mV
Resistor Accuracy			0.5	1%		*	*	%
OFFSET VOLTAGE[1]								
Input Offset Voltage			±0.5	±5		*	*	mV
vs Temperature			±3			*		µV/°C
vs Power Supply	V_S = ±6 to ±18V	80	96		*	*		dB
INPUT BIAS CURRENT[1]								
Input Bias Current	V_{CM} = 0V		10	50		*	*	pA
Input Offset Current	V_{CM} = 0V		5			*		pA
NOISE[1]								
Input Voltage Noise								
Noise Density: f = 10Hz			25			*		nV/√Hz
f = 10kHz			10			*		nV/√Hz
Voltage Noise: BW = 0.1 to 10Hz			2			*		µVp-p
Input Bias Current Noise								
Noise Density: f = 10kHz			2			*		fA/√Hz
INPUT VOLTAGE RANGE[1]								
Common-Mode Input Range			±11.5			*		V
Common-Mode Rejection	V_{CM} = ±10V	80	96		*	*		dB
INPUT IMPEDANCE[1]								
Differential			10^{13} || 2			*		Ω || pF
Common-Mode			10^{13} || 6			*		Ω || pF
OPEN-LOOP GAIN[1]								
Open-Loop Voltage Gain	V_O = ±10V, R_L = 2kΩ	90	126		*	*		dB
FREQUENCY RESPONSE[1]								
Slew Rate			10			*		V/µs
Gain-Bandwidth Product	G = +1		4			*		MHz
Total Harmonic Distortion	G = +1, f = 1kHz		0.0004			*		%
OUTPUT[1]								
Voltage Output	R_L = 2kΩ	±11	±11.5		*	*		V
Short Circuit Current			±25			*		mA
POWER SUPPLY								
Specified Operating Voltage			±15			*		V
Operating Voltage Range		±6		±18	*		*	V
Current			±6	±7		*	*	mA
TEMPERATURE RANGE								
Specification		–25		+85	*		*	°C
Operating		–25		+85	–55		+125	°C
Storage		–40		+125	–65		+150	°C
Thermal Resistance, θ_{J-A}			100			*		°C/W

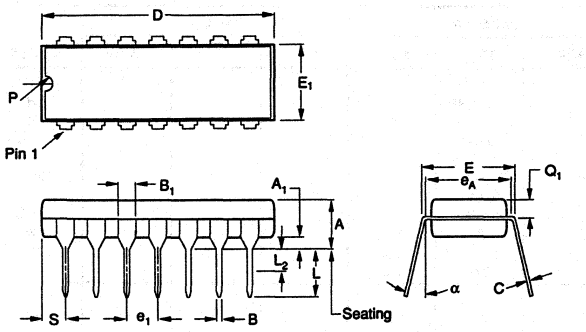
*Same as specification for UAF42AP.

NOTES: (1) Specifications apply to uncommitted op amp, A_4. The three op amps forming the filter are identical to A_4 but are tested as a complete filter.

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

MECHANICAL

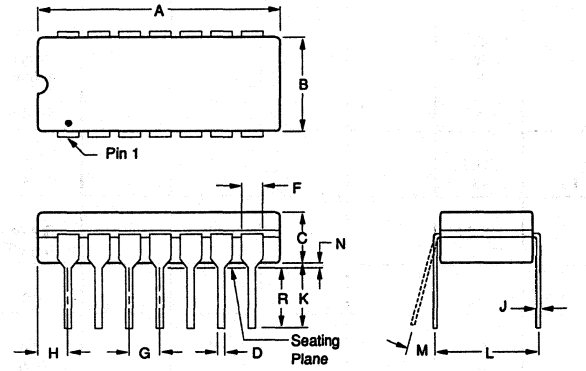
P Package — 14-Pin Plastic Package



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.120	.160	3.048	4.064
A_1	.015	.065	.381	1.651
B	.014	.020	.355	.508
B_1	.050	.065	1.270	1.651
C	.008	.012	.203	.304
D	.745	.770	18.923	19.558
E	.300	.325	7.620	8.255
E_1	.240	.260	6.096	6.604
e_1	.100 BASIC		2.540 BASIC	
e_A	.300 BASIC		7.620 BASIC	
L	.125	.150	3.175	3.810
L_2[1]	0	.030	0	.762
α	0°	15°	0°	15
P	—	.050	—	1.270
Q_1	.050	.085	1.270	2.159
S[2]	.065	.090	1.651	2.286

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.
(1) e_1 and e_A apply in zone L_2 when unit is installed.
(2) Not per JEDEC

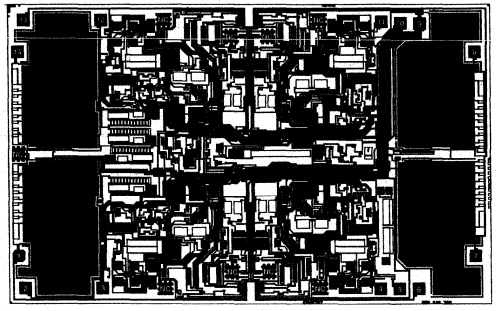
G Package — 14-Pin Ceramic DIP



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	—	.790	—	20.07
B	.220	.310	5.59	7.87
C	—	.185	—	4.70
D	.014	.023	0.36	0.58
F	.030	.070	0.76	1.78
G	.100 BASIC		2.54 BASIC	
H	—	.098	—	2.49
J	.008	.012	0.20	0.30
K	.140	.260	3.56	6.60
L	.290	.320	7.37	8.13
M	0°	15°	0°	15°
N	.015	.060	0.38	1.52
R	.125	.200	3.18	5.08

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

DICE INFORMATION



UAF42 DIE TOPOGRAPHY

PAD	FUNCTION	PAD	FUNCTION
1	Low Pass V_O	7	Bandpass V_O
2	V_{IN3}	8	Frequency Adj_1
3	V_{IN2}	9	V–
4	Aux. Op Amp, +In	10	V+
		11	Ground
5	Aux. Op Amp, –In	12	V_{IN1}
		13	High-Pass V_O
6	Aux. Op Amp, V_O	14	Frequency Adj_2

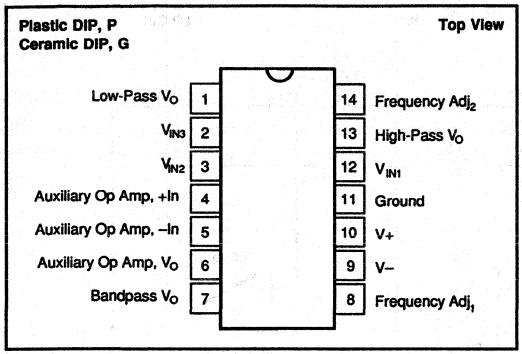
NC: No Connection.
Substrate Bias: Electrically connected to V– supply.

MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	205 x 130 ±5	5.21 x 3.30 ±13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.10 x 0.10
Backing	Gold	

See "DICE PRODUCTS" Section 17 in Data Book Supplement Volume 33c, or contact Burr-Brown for current information.

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage	±18V
Input Voltage	$\pm V_S$ ±0.7V
Output Short Circuit	Continuous
Operating Temperature:	
Plastic DIP, P	–40°C to +85°C
Ceramic DIP, G	–55°C to +125°C
Storage Temperature:	
Plastic DIP, P	–40°C to +125°C
Ceramic DIP, G	–65°C to +150°C
Junction Temperature:	
Plastic DIP, P	+125°C
Ceramic DIP, G	+150°C
Lead Temperature (soldering, 10s)	+300°C

ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE
UAF42AP	Plastic 14-Pin DIP	–25°C to +85°C
UAF42AG	Ceramic 14-Pin DIP	–25°C to +85°C

APPLICATION INFORMATION

The UAF42 is a monolithic implementation of the proven state-variable analog filter topology. Pin-compatible with the popular UAF41 Analog Filter, it provides several improvements.

Slew Rate of the UAF42 has been increased to 10V/µs versus 1.6V/µs for the UAF41. Frequency • Q product of the UAF42 has been improved, and the useful natural frequency extended by a factor of four to 100kHz. FET-input op amps on the UAF42 provide very low input bias current. The monolithic construction of the UAF42 provides lower cost and improved reliability.

DESIGN PROGRAM

Application Bulletin AB-035 and a computer-aided design program, available from Burr-Brown, make it easy to design and implement many kinds of active filters. The DOS-compatible program guides you through the design process and automatically calculates component values.

Low-pass, high-pass, band-pass and band-reject (notch) filters can be designed. The program supports the three most commonly used all-pole filter types: Butterworth, Chebyshev and Bessel. The less-familiar Inverse Chebyshev is also supported, providing a smooth passband response with ripple in the stop-band.

With each data entry, the program automatically calculates and displays filter performance. This allows a spreadsheet-like "what if" design approach. For example, you can quickly determine, by trial and error, how many poles are required for a desired attenuation in the stopband. Gain/phase plots may be viewed for any response type.

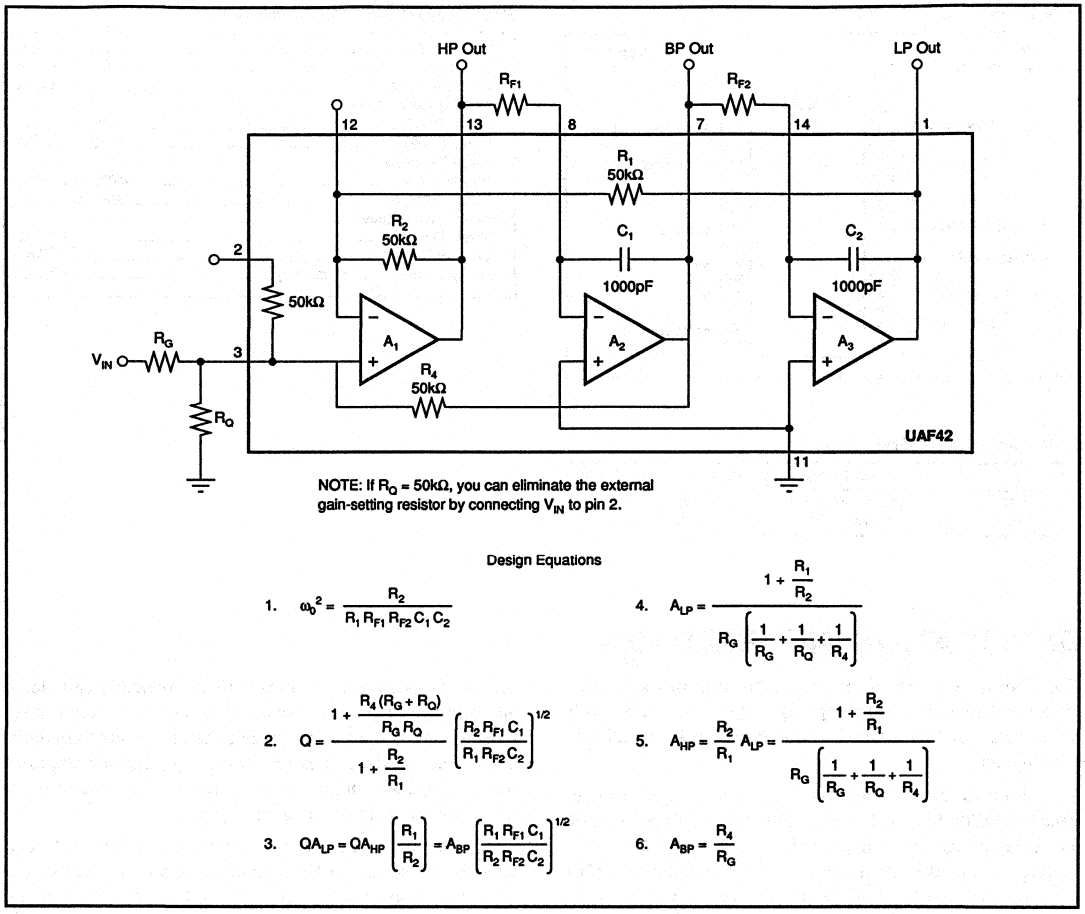
The basic building element of the most commonly used filter types is the second-order section. This section provides a complex-conjugate pair of poles. The natural frequency, ω, and damping factor, Q, of the pole pair determines the characteristic response of the section. The low-pass transfer function is

$$\frac{V_O(s)}{V_I(s)} = \frac{K\,\omega_n^2}{s^2 + s\,\omega_n/Q + \omega_n^2}$$

The high-pass transfer function adds a pair of zeros at the origin.

The most commonly used filter types are formed with one or more cascaded second-order sections. Each section is designed for ω and Q according to the filter type (Butterworth, Bessel, Chebyshev, etc.) and cutoff frequency. While tabulated data can be found in virtually any filter design text, the design program eliminates this tedious procedure.

Second-order sections may be non-inverting (Figure 1) or inverting (Figure 2). Design equations for these two basic configurations are shown for reference. The design program solves these equations, providing complete results, including component values.



Design Equations

1. $\omega_0^2 = \dfrac{R_2}{R_1 R_{F1} R_{F2} C_1 C_2}$

2. $Q = \dfrac{1 + \dfrac{R_4 (R_G + R_Q)}{R_G R_Q}}{1 + \dfrac{R_2}{R_1}} \left(\dfrac{R_2 R_{F1} C_1}{R_1 R_{F2} C_2} \right)^{1/2}$

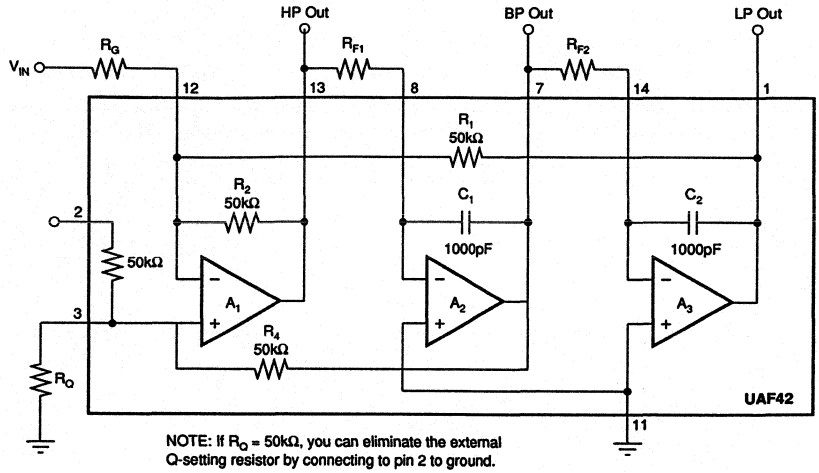
3. $QA_{LP} = QA_{HP} \left(\dfrac{R_1}{R_2} \right) = A_{BP} \left(\dfrac{R_1 R_{F1} C_1}{R_2 R_{F2} C_2} \right)^{1/2}$

4. $A_{LP} = \dfrac{1 + \dfrac{R_1}{R_2}}{R_G \left(\dfrac{1}{R_G} + \dfrac{1}{R_Q} + \dfrac{1}{R_4} \right)}$

5. $A_{HP} = \dfrac{R_2}{R_1} A_{LP} = \dfrac{1 + \dfrac{R_2}{R_1}}{R_G \left(\dfrac{1}{R_G} + \dfrac{1}{R_Q} + \dfrac{1}{R_4} \right)}$

6. $A_{BP} = \dfrac{R_4}{R_G}$

Figure 1. Non-Inverting Pole-Pair.



Design Equations

1. $\omega_0^2 = \dfrac{R_2}{R_1 R_{F1} R_{F2} C_1 C_2}$

2. $Q = \left(1 + \dfrac{R_4}{R_Q}\right) \dfrac{1}{\left(\dfrac{1}{R_1} + \dfrac{1}{R_2} + \dfrac{1}{R_G}\right)} \left(\dfrac{R_{F1} C_1}{R_1 R_2 R_{F2} C_2}\right)^{1/2}$

3. $QA_{LP} = QA_{HP} \left(\dfrac{R_1}{R_2}\right) = A_{BP} \left(\dfrac{R_1 R_{F1} C_1}{R_2 R_{F2} C_2}\right)^{1/2}$

4. $A_{LP} = \dfrac{R_1}{R_G}$

5. $A_{HP} = \dfrac{R_2}{R_1} A_{LP} = \dfrac{R_2}{R_G}$

6. $A_{BP} = \left(1 + \dfrac{R_4}{R_Q}\right) \dfrac{1}{R_G \left(\dfrac{1}{R_1} + \dfrac{1}{R_2} + \dfrac{1}{R_G}\right)}$

Figure 2. Inverting Pole-Pair.

6 Digital-to-Analog Converters

Burr-Brown offers a broad variety of Digital-to-Analog (D/A) converter products engineered to meet the most critical requirements for stability and reliability.

General purpose instrumentation D/As range in resolution from 12 to 18 bits. These models include industry standard products—many originated by Burr-Brown—as well as more complete, higher accuracy solutions. Burr-Brown's products are carefully designed and manufactured to minimize product variations, making them ideal for test equipment, process control, and other industrial and analytical applications.

PCM D/A converters are designed and tested to deliver excellent dynamic performance. The resolutions of these products are 16 and 18 bits. Typical applications are compact disc players, digital frequency synthesis, and telecommunications systems.

High-speed D/A converters offer very fast settling current output. Models are available with TTL or ECL logic inputs. These products are ideal for very high frequency synthesis and control systems.

The Selection Guides show parameters for the high grade. Models shown in **boldface** are products included in this supplement.

INSTRUMENTATION DIGITAL-TO-ANALOG CONVERTERS

Description	Model	Resolution (Bits)	Linearity Error (%FSR)	Settling Time (µs)	Output Range	Temp Range[1]	Pkg[2]	Q, Bl[3] Screen	Page No.
Very High Resolution	DAC729	18	±0.00075	5	±1mA, –2mA; +5V, +10V, ±5V, ±10V	Com	DDIP	Bl	6.1-80
General Purpose	**DAC700**	**16**	**±0.0015**	**1**	**–2mA**	**Com, Ind, Mil**	**DDIP**	**Q, Bl**	**S-6.1.13**
	DAC701	**16**	**±0.0015**	**8**	**+10V**	**Com, Ind, Mil**	**DDIP**	**Q, Bl**	**S-6.1.13**
	DAC702	**16**	**±0.0015**	**1**	**±1mA**	**Com, Ind, Mil**	**DDIP**	**Q, Bl**	**S-6.1.13**
	DAC703	**16**	**±0.0015**	**8**	**±10V**	**Com, Ind, Mil**	**DDIP, SO**	**Q, Bl**	**S-6.1.13**
Low DLE	DAC710	16	±0.0015	8 typ	±1mA	Com	DDIP	—	6.1-65
Around Zero	DAC711	16	±0.0015	8 typ	±10V	Com	DDIP	—	6.1-65
Lowest Cost	DAC1600	16	±0.003	8 typ	±10V	Com	DDIP	—	6.1-108
Bus Interface:									
16-Bit Parallel	**DAC707**	**16**	**±0.003**	**8**	**±10V**	**Com, Ind, Mil**	**DDIP**	**Q, Bl**	**S-6.1.24**
Serial/8-bit Parallel	**DAC708**	**16**	**±0.003**	**1**	**±1mA, –2mA**	**Com, Ind, Mil**	**DDIP**	**Q, Bl**	**S-6.1.24**
Serial/8-bit Parallel	**DAC709**	**16**	**±0.003**	**8**	**±5V, ±10V, +10V**	**Com, Ind, Mil**	**DDIP**	**Q, Bl**	**S-6.1.24**
Dual,Ser./8-bit Par.	DAC725	16	±0.003	8	±10V	Com, Ind	DDIP	Bl	6.1-72
Industry Standard,	DAC70BH	16	±0.003	1	±1mA, –2mA	Ind	DDIP	Bl	6.1-5
General Purpose	DAC71	16	±0.003	8	±1mA, –2mA; +10V, ±10V	Com	DDIP	Bl	6.1-13
	DAC72BH	16	±0.003	1	"	Ind	DDIP	Bl	6.1-5
Industry Standard	DAC7541A	12	±0.012	1	0 to 1mA	Com, Ind, Mil	DIP, SO	Bl	6.1-112
Ind. Std. w/Latch	DAC7545	12	±0.012	2	0 to 1mA	Com, Ind, Mil	DIP, SO	Bl	6.1-120
Dual w/Bus Interface:									
Serial Input	**DAC7800**	**12**	**±0.012**	**0.8**	**0 to 1mA**	**Ind**	**DIP, SO**	**—**	**S-6.1.93**
8-bit Port Interface	**DAC7801**	**12**	**±0.012**	**0.8**	**0 to 1mA**	**Ind**	**DIP, SO**	**—**	**S-6.1.93**
12-bit Port Interface	**DAC7802**	**12**	**±0.012**	**0.8**	**0 to 1mA**	**Ind**	**DIP, SO**	**—**	**S-6.1.93**

(Continued on next page)

INSTRUMENTATION DIGITAL-TO-ANALOG CONVERTERS (Continued)

Description	Model	Resolution (Bits)	Linearity Error (%FSR)	Settling Time (µs)	Output Range	Temp Range[1]	Pkg[2]	Q, BI[3] Screen	Page No.
Flexible Bus Interface:									
Industry Standard Pinout	**DAC667**	**12**	**±0.006**	**4**	**±2.5V, ±5V,±10V +5V, +10V**	**Com, Ind, Mil**	**DIP**	**—**	**S-6.1.4**
	DAC811	12	±0.006	4	±5V, ±10V, +10V	Com, Ind, Mil	DDIP, SO	BI	6.1-90
Small, Low Cost	**DAC813**	**12**	**±0.006**	**4**	**±5V, ±10V, +10V**	**Com, Ind, Mil**	**DIP, SO**	**—**	**S-6.1.37**
Lowest Cost	DAC1201	12	±0.018	4 typ	±5V, ±10V, +10V	Com	DDIP	—	6.1-103
Industry Standard, General Purpose	DAC80	12	±0.012	0.3, 3 typ	±1mA, –2mA; +5V, +10V, ±5V, ±10V	Com	DDIP	BI	6.1-27
	DAC85H	12	±0.012	"	"	Ind	DDIP	Q, BI	6.1-35
	DAC87H	12	±0.012	"	"	Mil	DDIP	Q, BI	6.1-35
Dual, 12-bit Port	DAC2813	12	±0.006	4	±10, 0 to 10	Ind	DDIP		
Dual, Multiplying Serial Port	**DAC2814**	**12**	**±0.012**	**10**	**+V_S, –1.4V –V_S, +1.4V**	**Ind**	**DDIP**		**S-6.1.48**
Dual Multiplying 8-bit Port	**DAC2815**	**12**	**±0.012**	**10**	**+V_S, –1.4V –V_S, +1.4V**	**Ind**	**DDIP**		**S-6.1.59**
QUAD, Multiplying Serial Port	**DAC4814**	**12**	**±0.012**	**10**	**+V_S, –1.4V –V_S, +1.4V**	**Ind**	**DDIP**		**S-6.1.70**
Dual Multiplying 8-bit Port	**DAC4815**	**12**	**±0.012**	**10**	**+V_S, –1.4V –V_S, +1.4V**	**Ind**	**DDIP**		**S-6.1.82**

NOTES: (1) Temperature Range: Com = 0°C to +70°C, Ind = (–25°C to +85°C) or (–40°C to +85°C), Mil = –55°C to +125°C. (2) DIP = 0.3" wide DIP, DDIP = 0.6" wide DIP, SO = small outline surface mount. (3) Q inidcates that optional reliability screening is available for the model. BI indicates that an optional 160 hour burn-in is available for the model.

AUDIO, VIDEO AND COMMUNICATIONS DIGITAL-TO-ANALOG CONVERTERS

Model	Resolution (Bits)	Max Update Rate	Max THD + N (V_{OUT} = FS)	Output Range	Input Format	Power Supply (V)	Package[1]	Power Dissipation (mW)	Page No.
DAC65	**12**	**50MHz**	**70dB THD**	**±1.25V, ±625mA**	**Parallel**	**±15**	**DDIP**	**1.2W**	**S-6.2.107**
DAC650	**12**	**500MHz**	**65dB THD**	**±1V, ±20mA**	**Parallel**	**±15, ±5**	**68 LEAD**	**2.0W**	**S-6.2.119**
PCM53	16	500kHz	–88dB (JP) –92dB (KP)	±10V, ±1mA	Parallel	±15, +5	DDIP	600	6.2-152
PCM54	16	500kHz	–82dB (HP) –88dB (JP) –92dB (KP)	±3V, ±1mA	Parallel	±5 to ±12	DDIP	300	6.2-164
PCM55	16	500kHz	–82dB (HP) –88dB (JP)	±3V, ±1mA	Parallel	±5	SO	125	6.2-164
PCM56	**16**	**800kHz**	**–82dB (P) –88dB (P-J) –92dB (P-K)**	**±3V, ±1mA**	**Serial Latched**	**±5 to ±12**	**DIP**	**260**	**S-6.2.158**
PCM66	**16**	**200kHz**	**–82dB (P) 2-Channel**	**2.8Vp-p, Latched**	**Serial**	**+5**	**SO**	**50**	**S-6.2.167**
PCM1700 (Dual DAC)	**18**	**800kHz**	**–82dB (P) –88dB (P-J) –92dB (P-K)**	**±3V, ±0.67mA**	**Serial Latched**	**±5**	**DDIP**	**380**	**S-9.2.227**
PCM58	18	1MHz	–92dB (P) –94dB (P-J) –96dB (P-K)	±1mA	Serial Latched	+5, –12	DDIP	400	6.2-180

(Continued on next page)

AUDIO, VIDEO AND COMMUNICATIONS DIGITAL-TO-ANALOG CONVERTERS (Continued)

Model	Resolution (Bits)	Max Update Rate	Max THD + N (V_{OUT} = FS)	Output Range	Input Format	Power Supply (V)	Package[1]	Power Dissipation (mW)	Page No.
PCM61	**18**	**800kHz**	**–82dB (P)** **–88dB (P-J)** **–92dB (P-K)**	**±3V, ±1mA**	**Serial Latched**	**±5 to ±12**	**DDIP**	**200**	**S-6.2.175**
PCM63	**20**	**1MHz**	**–88dB (P)** **–92dB (P-J)** **–96dB (P-K)**	**±2mA**	**Latched**	**±5**	**DDIP**	**200**	**S-6.2.179**
PCM64	18	1.5MHz	–96dB	±1mA	Parallel	+5, –15	DIP	400	6.2-194
PCM67 (Dual DAC)	**18**	**1Mhz**	**–82 (P)** **–88 (P-J)** **–92 (P-K)**	**1.2mA**	**Serial**	**+5V**	**DIP, SO**	**105**	**S-6.2.189**

NOTES: (1) DIP = 0.3" wide DIP, DDIP = 0.6" wide DIP, SO = Small Outline Surface Mount.

DIGITAL SIGNAL PROCESSING DIGITAL-TO-ANALOG CONVERTERS

Model	Resolution (Bits)	Linearity Error (%FSR)	Settling Time (µs)	Output Range	Signal-to-Noise + Distortion Ratio (dB)	Total Harmonic Distortion (dB)	Temp Range[1]	Pkg[2]	Page No.
DSP-Compatible Digital Interface (Single—DSP201, Dual—DSP202):									
DSP201	**18**	**±0.006**	**—**	**±3V**	**86, f_{OUT} = 2kHz**	**–90**	**Ind**	**DDIP**	**S-6.2.139**
DSP202	**18**	**±0.006**	**—**	**±3V**	**86, f_{OUT} = 2kHz**	**–90**	**Ind**	**DDIP**	**S-6.2.139**
DAC65	**12**	**±0.012**	**40ns**	**±1.2V, ±6.35mA**	**70, f_{OUT} = 1MHz**	**–68**	**Com**	**DDIP**	**S-6.2.107**
DAC63	12	±0.012	50ns	±5mA, 0 to –10mA ±0.5V, 0 to +1.5V with internal resistor	—	—	Ind	DDIP	6.2-135
Ultra-Fast Settling, TTL Input:									
DAC812	12	±0.012	50ns	±5mA, 0 to –10mA ±0.5V, 0 to –1.5V with internal resistor	—	—	Ind	DDIP	6.2-146

NOTES: (1) Com = 0°C to +70°C, Ind = (–25°C to +85°C) or (–40°C to +85°C). (2) DDIP = 0.6" wide DIP.

MODELS STILL AVAILABLE BUT NOT FEATURED IN THIS BOOK

DAC800-CBI-V
DAC800-CBI-I

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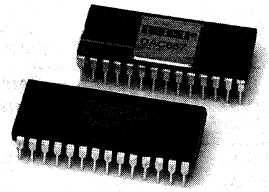


DAC667

Microprocessor-Compatible 12-BIT DIGITAL-TO-ANALOG CONVERTER

FEATURES

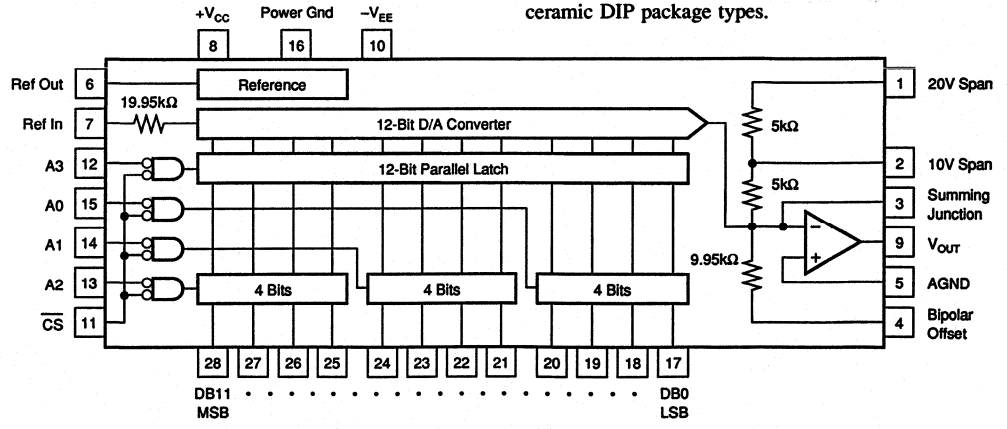
- ±1/2LSB MAX NONLINEARITY OVER TEMPERATURE
- MONOTONICITY GUARANTEED OVER TEMPERATURE
- MICROCOMPUTER INTERFACE: Double-Buffered Latch
- VOLTAGE OUTPUT: ±10V, ±5V, +10V With ±12V to ±15V Supplies
- LOW POWER DISSIPATION: 345mW typ
- PIN COMPATIBLE WITH AD667

DESCRIPTION

The DAC667 is a complete monolithic integrated circuit microprocessor-compatible 12-bit digital-to-analog converter. It includes a precision voltage reference, microcomputer interface logic, double-buffered latch, and a 12-bit D/A converter with a voltage output amplifier. Fast current switches and a laser-trimmed thin-film resistor network provide a highly accurate and fast D/A converter.

A double-buffered latch facilitates microcomputer interfacing to 4-, 8-, 12-, or 16-bit data buses. The input buffer latch holds the 12-bit data until it is transferred to an internal 12-bit D/A converter latch, giving precise timing control over an analog output change.

The DAC667 is specified to ±1/4LSB maximum linearity error (B and K grades) at +25°C and ±1/2LSB maximum over the temperature range. All grades are guaranteed monotonic over the specification temperature range. The DAC667 is available in two performance grades and in 28-pin, 0.6" wide plastic and ceramic DIP package types.



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Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

PDS-1091B

SPECIFICATIONS

ELECTRICAL

T_A = +25°C, ±12V. ±15V power supplies unless otherwise noted.

PARAMETER	DAC667JP MIN	DAC667JP TYP	DAC667JP MAX	DAC667KP MIN	DAC667KP TYP	DAC667KP MAX	UNITS
DIGITAL INPUTS							
Resolution			12			*	Bits
Logic Levels (TTL Compatible, T_{MIN} to T_{MAX})[1]							
V_{IH} (Logic 1)	+2		+5.5	*		*	V
V_{IL} (Logic 0)	0		+0.8	*		*	V
I_{IH} (V_{IH} = 5.5V)		3	10		*	*	µA
I_{IL} (V_{IL} = 0.8V)		1	5		*	*	µA
ACCURACY							
Linearity Error at +25°C		±1/4	±1/2		±1/8	±1/4	LSB
T_A = T_{MIN} to T_{MAX}		±1/2	±3/4		±1/4	±1/2	LSB
Differential Linearity Error at +25°C		±1/2	±3/4		±1/4	±1/2	LSB
T_A = T_{MIN} to T_{MAX}		Monotonicity Guaranteed			*		LSB
Gain Error[2]		±0.1	±0.2		*	*	% of FSR[3]
Unipolar Offset Error[2]		±1	±2		*	*	LSB
Bipolar Zero[2]		±0.05	±0.1		*	*	% of FSR
DRIFT							
Differential Linearity		±2			*		ppm of FSR/°C
Gain (Full Scale), T_A = +25°C to T_{MIN} or T_{MAX}		±5	±30		*	±15	ppm of FSR/°C
Unipolar Offset, T_A = +25°C to T_{MIN} or T_{MAX}		±1	±3			*	ppm of FSR/°C
Bipolar Zero, T_A = +25°C to T_{MIN} or T_{MAX}		±5	±10			*	ppm of FSR/°C
CONVERSION SPEED							
Settling Time to ±0.01% of FSR for FSR Change (2kΩ || 500pF Load, C_F = 0)							
With 10kΩ Feedback		3	4		*	*	µs
With 5kΩ Feedback		2	3		*	*	µs
For LSB Change		2			*		µs
Slew Rate	8			*			V/µs
ANALOG OUTPUT							
Ranges[4]		±2.5, ±5, ±10, +5, +10			*		V
Output Current	±5			*			mA
Output Impedance (DC)		0.05			*		Ω
Short Circuit Current			40			*	mA
REFERENCE OUTPUT	9.9	10	10.1	*	*	*	V
External Current	0.1	1		*	*		mA
POWER SUPPLY SENSITIVITY							
V_{CC} = +11.4 to +16.5VDC		5	10		*	*	ppm of FS/%
V_{EE} = −11.4 to −16.5VDC		5	10		*	*	ppm of FS/%
POWER SUPPLY REQUIREMENTS							
Rated Voltages		±12, ±15			*		V
Range[4]	±11.4		±16.5	*		*	V
Supply Current							
+11.4 to +16.5VDC		14	17		*	*	mA
−11.4 to −16.5VDC		9	12		*	*	mA
TEMPERATURE RANGE							
Specification	0		+70	*		*	°C
Operating	−40		+85	*		*	°C
Storage	−65		+125	*		*	°C

* Same as specification for DAC667JP.

ABSOLUTE MAXIMUM RATINGS

V_{CC} to Power Ground ..... 0V to +18V
V_{EE} to Power Ground ..... 0V to −18V
Digital Inputs (Pins 11–15, 17–28) to Power Ground ..... −1V to +7V
Ref In to Reference Ground ..... ±12V
Bipolar Offset to Reference Ground ..... ±12V
10V Span Resistor to Reference Ground ..... ±12V
20V Span Resistor to Reference Ground ..... ±24V
Ref Out, V_{OUT} (Pins 6, 9) ..... Indefinite Short to Power Ground, Momentary Short To V_{CC}
Power Dissipation 1000mW

TIMING SPECIFICATIONS

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
t_{DC}	Data Valid to End of $\overline{CS}$	50	–	–	ns
t_{AC}	Address Valid to End of $\overline{CS}$	100	–	–	ns
t_{CP}	$\overline{CS}$ Pulse Width	100	–	–	ns
t_{DH}	Data Hold Time	0	–	–	ns
t_{SETT}	Output Voltage Settling Time	–	2	4	µs

All models, T_A = +25°C, V_{CC} = +12V or +15V, V_{EE} = −12V or −15V.

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ELECTRICAL (CONT)

T_A = +25°C, ±12V. ±15V power supplies unless otherwise noted.

PARAMETER	DAC667AH MIN	DAC667AH TYP	DAC667AH MAX	DAC667BH MIN	DAC667BH TYP	DAC667BH MAX	UNITS
DIGITAL INPUT							
Resolution			12			*	Bits
Logic Levels (TTL Compatible, T_{MIN} to T_{MAX})[1]							
V_{IH} (Logic 1)	+2		+5.5	*		*	V
V_{IL} (Logic 0)	+0		+0.8	*		*	V
I_{IH} (V_{IH} = 5.5V)		3	10		*	*	µA
I_{IL} (V_{IL} = 0.8V)		1	5		*	*	µA
ACCURACY							
Linearity Error at +25°C		±1/4	±1/2		±1/8	±1/4	LSB
T_A = T_{MIN} to T_{MAX}		±1/2	±3/4		±1/4	±1/2	LSB
Differential Linearity Error at +25°C		±1/2	±3/4		±1/4	±1/2	LSB
T_A = T_{MIN} to T_{MAX}		Monotonicity Guaranteed			*		LSB
Gain Error[2]		±0.1	±0.2		*	*	% of FSR[3]
Unipolar Offset Error[2]		±1	±2		*	*	LSB
Bipolar Zero[2]		±0.05	±0.1		*	*	% of FSR
DRIFT							
Differential Linearity		±2			*		ppm of FSR/°C
Gain (Full Scale), T_A = +25°C to T_{MIN} or T_{MAX}		±5	±30		*	±15	ppm of FSR/°C
Unipolar Offset, T_A = +25°C to T_{MIN} or T_{MAX}		±1	±3			*	ppm of FSR/°C
Bipolar Zero, T_A = +25°C to T_{MIN} or T_{MAX}		±5	±10			*	ppm of FSR/°C
CONVERSION SPEED							
Settling Time to ±0.01% of FSR for FSR Change (2kΩ || 500pF Load)							
With 10kΩ Feedback		3	4		*	*	µs
With 5kΩ Feedback		2	3		*	*	µs
For LSB Change		2			*		µs
Slew Rate	8			*			V/µs
ANALOG OUTPUT							
Ranges[4]		±2.5, ±5, ±10, +5, +10			*		V
Output Current	±5			*			mA
Output Impedance (DC)		0.05			*		Ω
Short Circuit Current			40			*	mA
REFERENCE OUTPUT	9.9	10	10.1	*	*	*	V
External Current	0.1	1		*	*		mA
POWER SUPPLY SENSITIVITY							
V_{CC} = +11.4 to +16.5VDC		5	10		*	*	ppm of FS/%
V_{EE} = −11.4 to −16.5VDC		5	10		*	*	ppm of FS/%
POWER SUPPLY REQUIREMENTS							
Rated Voltages		±12, ±15			*		V
Range[4]	±11.4		±16.5	*		*	V
Supply Current							
+11.4 to +16.5VDC		14	17		*	*	mA
−11.4 to −16.5VDC		9	12		*	*	mA
TEMPERATURE RANGE							
Specification	−25		+85	*		*	°C
Operating	−40		+85	*		*	°C
Storage	−65		+150	*		*	°C

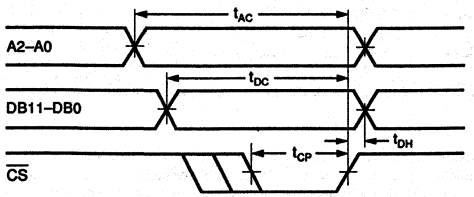
* Same as specification for DAC667AH.

NOTES: (1) The digital input specifications are 100% tested at +25°C and over the full temperature range. (2) Adjustable to zero. (3) FSR means full scale range and is 20V for ±10V range and 10V for the ±5V range. (4) ±10V full scale output can be achieved using ±11.4 supplies.

TIMING DIAGRAMS

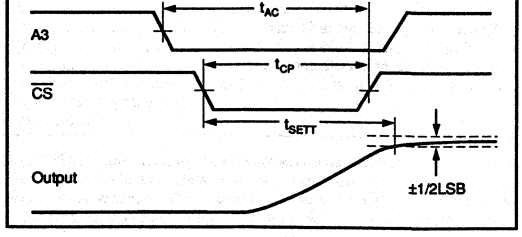
Write Cycle #1

Load first rank from Data Bus; A3 = 1.



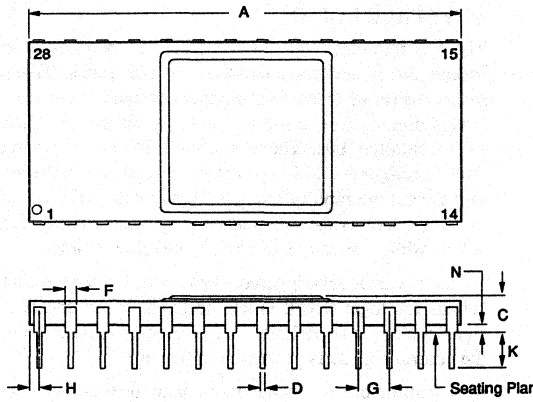
Write Cycle #2

Load second rank from first rank; A2, A1, A0 = 1.



MECHANICAL

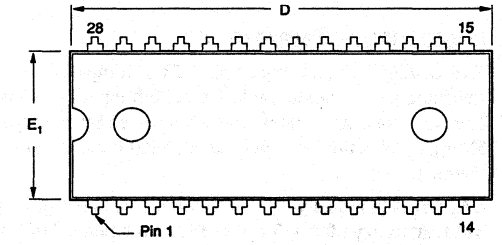
H Package — Ceramic DIP



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.386	1.414	35.20	35.92
C	.115	.175	2.92	4.45
D	.015	.021	0.38	0.53
F	.035	.060	0.89	1.52
G	.100 BASIC		2.54 BASIC	
H	.036	.064	0.91	1.63
J	.008	.012	0.20	0.30
K	.120	.240	3.05	6.10
L	.600 BASIC		15.24 BASIC	
M	—	10°	—	10°
N	.025	.060	0.64	1.52

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.

P Package — Plastic DIP

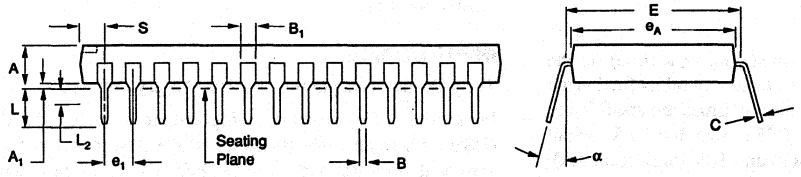


DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A(1)	.169	.200	4.29	5.08
A1 (1)	.015	.070	0.38	1.78
B	.015	.020	0.38	0.51
B1	.015	.055	0.38	1.40
C	.008	.012	0.20	0.30
D(1)	1.380	1.455	35.05	36.96
E	.600	.625	15.24	15.88
E1 (1)	.485	.550	12.32	13.97
e1	.100 BASIC		2.54 BASIC	
eA	.600 BASIC		15.24 BASIC	

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
L	.100	.200	2.54	5.08
L2	.000	.030	0.00	0.76
α	0°	15°	0°	15°
S(1)	.040	.080	1.02	2.03

(1) Not JEDEC Standard

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.



ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE (°C)	LINEARITY ERROR, MAX AT 25°C	GAIN TC, MAX (ppm/°C)
DAC667JP	Plastic DIP	0 to +70	±1/2LSB	±30
DAC667KP	Plastic DIP	0 to +70	±1/4LSB	±15
DAC667AH	Ceramic DIP	–25 to +85	±1/2LSB	±30
DAC667BH	Ceramic DIP	–25 to +85	±1/4LSB	±15

ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

DISCUSSION OF SPECIFICATIONS

LINEARITY ERROR

Linearity error is defined as the deviation of the analog output from a straight line drawn between the end points (digital inputs all ones and all zeros). DAC667 linearity error

is specified at ±1/4LSB max at +25°C for B and K grades, and ±1/2LSB max for A and J grades.

DIFFERENTIAL LINEARITY ERROR

Differential linearity error (DLE) is the deviation from a 1LSB output change from one adjacent state to the next. A DLE specification of 1/2LSB means that the output step size can range from 1/2LSB to 3/2LSB when the digital input code changes from one code word to the adjacent code word. If the DLE is more positive than –1LSB, the D/A is said to be monotonic.

MONOTONICITY

A D/A converter is monotonic if the output either increases or remains the same for increasing digital input values. All grades of the DAC667 are monotonic over their specification temperature range.

DRIFT

Gain drift is a measure of the change in the full scale range (FSR) output over the specification temperature range. Gain drift is expressed in parts per million per degree Celsius (ppm/°C).

Unipolar offset drift is measured with a data input of 000_{HEX}. The D/A is configured for unipolar output. Unipolar offset drift is expressed in parts per million of full scale range per degree Celsius (ppm of FSR/°C).

Bipolar zero drift is measured with a data input of 800_{HEX}. The D/A is configured for bipolar output. Bipolar zero drift is expressed in parts per million of full scale range per degree Celsius (ppm of FSR/°C).

SETTLING TIME

Settling time is the total time (including slew time) for the output to settle to within an error band around its final value after a change in input. Three settling times are specified to ±0.01% of full scale range (FSR): two for FSR output changes of 20V (10kΩ feedback) and 10V (5kΩ feedback), and one for a 1LSB change. The 1LSB change is measured at the major carry ($7FF_{HEX}$ to 800_{HEX}, and 800_{HEX} to $7FF_{HEX}$), the input transition at which worst-case settling time occurs.

OPERATION

DAC667 is a monolithic integrated-circuit 12-bit D/A converter. It is complete with 12-bit D/A switches and ladder network, voltage reference, output amplifier and microprocessor bus interface as shown in the front-page diagram.

INTERFACE LOGIC

The bus interface logic of the DAC667 consists of four independently addressable latches in two ranks. The first rank consists of three four-bit input latches which can be loaded directly from a 4-, 8-, 12- or 16-bit microprocessor/microcontroller bus. These latches hold data temporarily while a complete 12-bit word is assembled before loading it into the second rank of latches. This double buffered organization prevents the generation of spurious analog output values while the complete word is being assembled.

All latches are level-triggered. Data present when the control signals are logic 0 will enter the latch. When the control signals return to logic 1, the data is latched. A truth table for the control signals is presented in Table I.

It is permissible to enable more than one of the latches simultaneously. If a first rank latch is enabled coincident with the second rank latch, the data will reach the second rank correctly if the timing specifications on page 2 are met.

LOGIC INPUT COMPATIBILITY

The DAC667 digital inputs are TTL compatible (1.4V switching level) with a low leakage, high input impedance. Thus the inputs are suitable for being driven by any type of 5V logic. An equivalent circuit of a digital input is shown in Figure 1.

DAC667 data inputs will float to logic 1 and control inputs will float to logic 0 if left open. It is recommended that any unused inputs be connected to power common to improve noise immunity.

INPUT CODING

The DAC667 accepts positive-true binary input codes.

Input coding for unipolar analog output is straight binary (USB), where all zeros (000_{HEX}) on the data inputs gives a zero analog output and all ones (FFF_{HEX}) gives an analog output 1LSB below full scale.

Input coding for bipolar analog outputs is bipolar offset binary (BOB), where an input code of 000_{HEX} gives a minus full-scale output, an input of FFF_{HEX} gives an output 1LSB below positive full scale, and zero occurs for an input code of 800_{HEX}.

The DAC667 can be used with two's complement coding if a logic inverter is used ahead of the MSB input (DB11).

$\overline{CS}$	A3	A2	A1	A0	OPERATION
1	X	X	X	X	No Operation
X	1	1	1	1	No Operation
0	1	1	1	0	Enable Four LSBs of First Rank
0	1	1	0	1	Enable Four Middle Bits of First Rank
0	1	0	1	1	Enable Four MSBs of First Rank
0	0	1	1	1	Loads Second Rank from First Rank
0	0	0	0	0	All Latches Transparent

X = Don't care.

TABLE I. DAC667 Truth Table.

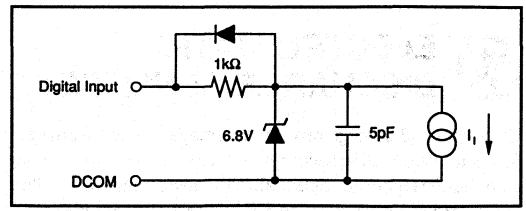


FIGURE 1. Equivalent Digital Input Circuit.

INTERNAL/EXTERNAL REFERENCE USE

DAC667 contains a +10V reference which is trimmed to typically ±0.2% and tested and guaranteed to ±1%. $V_{REF\ OUT}$ must be connected to $V_{REF\ IN}$ through a gain adjust resistor with a nominal value of 50Ω. A trim potentiometer with a nominal value of 100Ω can be used to provide adjustment to zero gain error. If an external 10.000V reference is used, it may be necessary to increase the trim range slightly.

The reference output may be used to drive external loads, sourcing up to 5mA. The load current should be constant, otherwise the gain (and bipolar offset, if connected) of the converter will vary.

It is possible to use references other than +10V. The recommended range of reference voltage is from +8V to +11V, which allows both 8.192V and 10.24V ranges to be used. The DAC667 is optimized for fixed-reference applications. If the reference voltage is expected to vary over a wide range, a CMOS multiplying D/A is a better choice.

GAIN AND OFFSET ADJUSTMENTS

Figures 2 and 3 illustrate the relationship of offset and gain adjustments to a unipolar- and a bipolar-connected DAC667. Offset should be adjusted first to avoid interaction of adjustments.

Offset Adjustment

For unipolar (USB) operation, apply the digital input code that should produce zero voltage output and adjust the offset potentiometer for zero output. For bipolar (BOB, BTC) operation, apply the digital input code that produces the maximum negative output voltage and adjust the offset potentiometer for minus full scale voltage. See Table II for calibration values and codes.

Gain Adjustment

For either unipolar or bipolar operation, apply the digital input that gives the maximum positive voltage output. Adjust the gain potentiometer for this positive full scale voltage. See Table II for calibration values.

DIGITAL INPUT	ANALOG OUTPUT				
	0 to +5V	0 to +10V	±2.5V	±5V	±10V
FFF_{HEX}	+4.9987V	+9.9976V	+2.4987V	+4.9976V	+9.9951V
800_{HEX}	+2.5000V	+5.0000V	0.0000V	0.0000V	0.0000V
$7FF_{HEX}$	+2.4987V	+4.9976V	−0.0013V	−0.0024V	−0.0049V
000_{HEX}	0.0000V	0.0000V	−2.5000V	−5.0000V	−10.0000V
1LSB	1.22mV	2.44mV	1.22mV	2.44mV	4.88mV

TABLE II. Calibration Values.

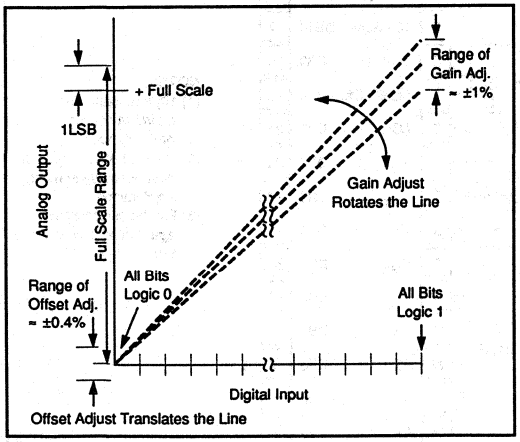


FIGURE 2. Relationship of Offset and Gain Adjustments for a Unipolar D/A Converter.

SETTLING TIME PERFORMANCE

The switches, reference and output amplifier of the DAC667 are designed for optimum settling time performance (Figure 4). Figure 4a shows the full scale range step response, V_{OUT} −10V to +10V to −10V, for data input 000_{HEX} to FFF_{HEX} to 000_{HEX}. Figure 4b shows the settling time response at plus full scale (+10V) for an output transition from −10V to +10V. Figure 4c shows the settling time response at minus full scale (−10V) for an output transition from +10V to −10V. Figure 4d shows the major carry glitch response for input code transitions $7FF_{HEX}$ to 800_{HEX} and for 800_{HEX} to $7FF_{HEX}$.

Unlike the Analog Devices AD667, the Burr-Brown DAC667 does not require an external capacitor (C_f = 20pF) across R_{SPAN} to eliminate overshoot. Using the 20pF with the Burr-Brown DAC667 increases the settling time about one microsecond. The DAC667 settling time is specified at 7µs maximum. The AD667 is specified at 4µs maximum.

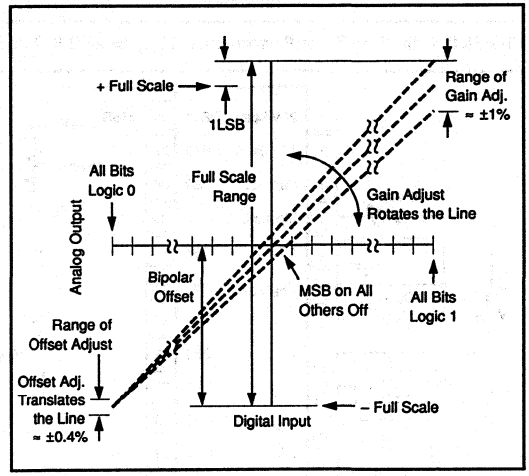


FIGURE 3. Relationship of Offset and Gain Adjustments for a Bipolar D/A Converter.

INSTALLATION

POWER SUPPLY CONNECTIONS

Note that the metal lid of the ceramic-packaged DAC667 is connected to $-V_{EE}$. Take care to avoid accidental short circuits in tightly spaced installations.

Power supply decoupling capacitors should be added as shown in Figure 5. Best settling performance occurs using a 1µF to 10µF tantalum capacitor at $-V_{EE}$. Applications with less critical settling time may be able to use 0.01µF at $-V_{EE}$ as well as at $+V_{CC}$. The capacitors should be located close to the DAC667 package.

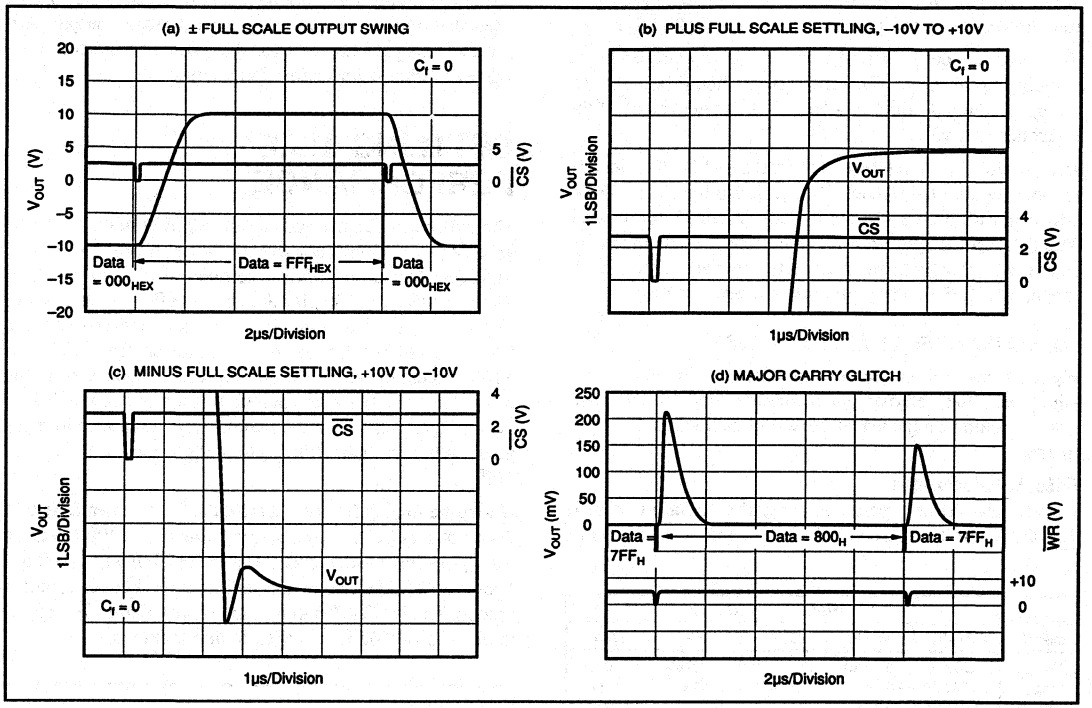


FIGURE 4. Settling Time Performance, Z_{LOAD} = 2kΩ II 500pF.

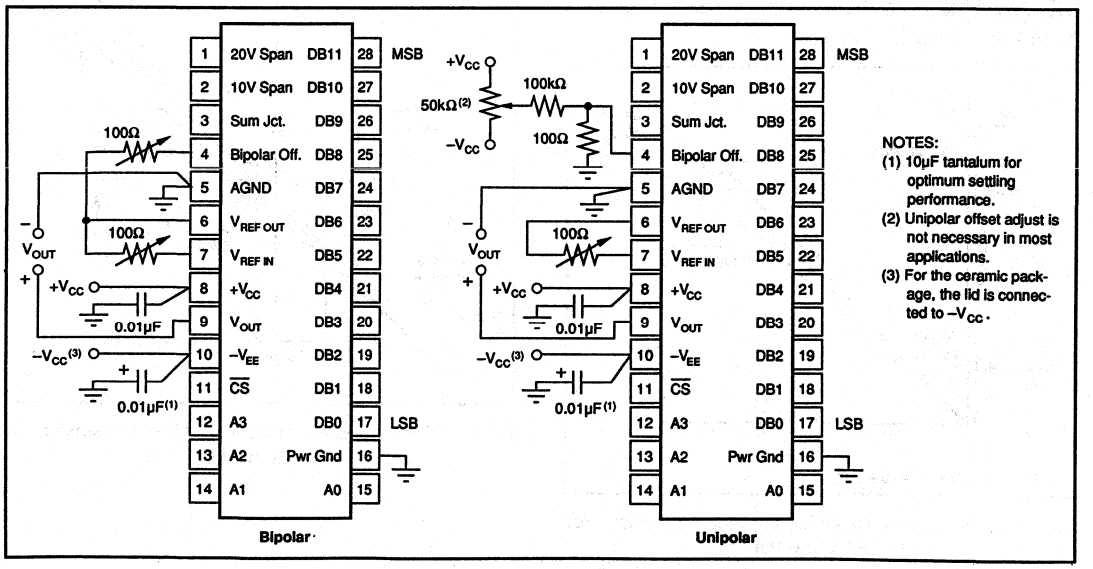


FIGURE 5. Power Supply, Gain and Offset Connections.

DAC667 features separate digital and analog power supply returns to permit optimum connections for low noise and high speed performance. It is recommended that both power ground (pin 16) and analog ground (AGND, pin 5) be connected directly to a ground plane under the package. If a ground plane is not used, connect the AGND and power ground pins together close to the package. Since the reference point for V_{OUT} and $V_{REF\ OUT}$ is the AGND pin, it is also important to connect the load directly to the AGND pin.

The change in current in the AGND pin due to an input data word change from 000_{HEX} to FFF_{HEX} is only 1mA.

OUTPUT VOLTAGE SWING AND RANGE CONNECTIONS

The DAC667 output amplifier can provide ±10V output swing while operating on ±11.4V supplies. The Analog Devices AD667 requires a minimum of ±12.5V to achieve an output swing of ±10V.

Internal scaling resistors provided in the DAC667 may be connected to produce bipolar output voltage ranges of ±10V, ±5V or ±2.5V or unipolar output voltage ranges of 0 to +5V or 0 to +10V. Refer to Figures 6, 7 and 8. Connections for various output ranges are shown in Table III.

The internal feedback resistors (5kΩ) and the bipolar offset resistor (9.95kΩ) are trimmed to an absolute tolerance of about ±10%.

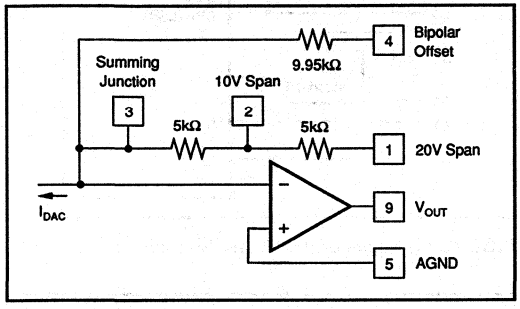


FIGURE 6. Output Amplifier Voltage Range Scaling Circuit.

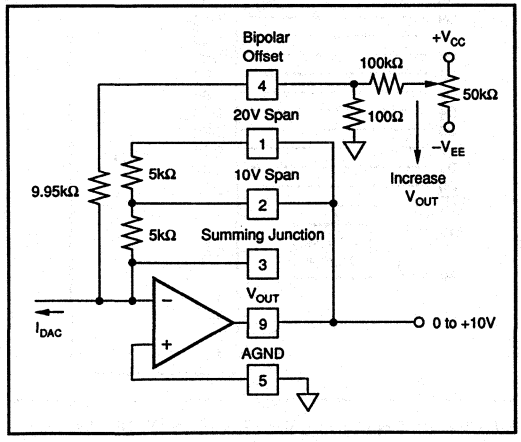


FIGURE 7. 0 to +10V Unipolar Voltage Output.

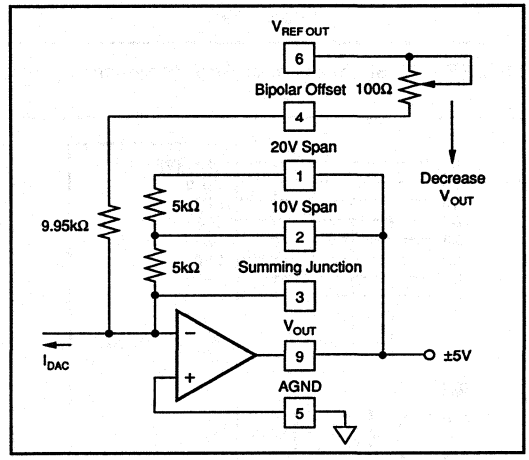


FIGURE 8. ±5V Bipolar Voltage Output.

MICROCOMPUTER BUS INTERFACING

8-BIT BUS INTERFACE

The DAC667 interfaces easily to 8-bit microprocessor systems of all types. The control logic makes possible the use of right- or left-justified data formats. Data formats for 8-bit buses are illustrated in Figure 9.

Whenever a 12-bit D/A is loaded from an 8-bit bus, two bytes are required. If the software program considers the data to be a 12-bit binary fraction (between 0 and 4095/4096), the data is left-justified, with the eight most significant bits in one byte and the remaining bits in the upper half of another byte. Right-justified data calls for the eight least significant bits to occupy one byte, with the four most significant bits residing in the lower half of another byte, simplifying integer arithmetic.

OUTPUT RANGE	DIGITAL INPUT CODES	CONNECT PIN 9 TO	CONNECT PIN 1 TO	CONNECT PIN 2 TO	CONNECT PIN 4 TO
±10V	Offset Binary	1	9	NC	6 (Through 50Ω fixed or 100Ω trim resistor.)
±5V	Offset Binary	1 and 2	2 and 9	1 and 9	6 (Through 50Ω fixed or 100Ω trim resistor.)
±2.5V	Offset Binary	2	3	9	6 (Through 50Ω fixed or 100Ω trim resistor.)
0 to +10V	Straight Binary	1 and 2	2 and 9	1 and 9	5 (Or optional trim. See Figure 7.)
0 to +5V	Straight Binary	2	3	9	5 (Or optional trim. See Figure 7.)

TABLE III. Output Voltage Range Connections.

Figure 10 shows an addressing scheme for use with a DAC-667 set up for left-justified data in an 8-bit system. The base address is decoded from the high-order address bits and the resultant active-low signal is applied to CS. The two LSBs of the address bus are connected as shown to the DAC667 address inputs. The latches now reside in two consecutive locations, with location X01 loading the four LSBs and location X10 loading the eight MSBs and updating the output.

Right-justified data can also be accommodated as shown in Figure 11. The DAC667 still occupies two adjacent locations in the processor's memory map. Location X01 loads the eight LSBs and location X10 loads the four MSBs and updates the output.

12- AND 16-BIT BUS INTERFACES

For operation with 12- and 16-bit buses, all four address lines (A0 through A3) are connected to logic 0, and the latch is enabled by $\overline{CS}$ asserted low. The DAC667 thus occupies a single memory location.

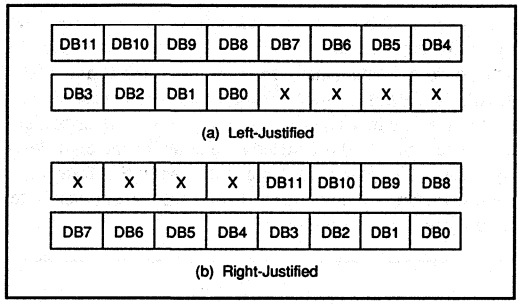


FIGURE 9. 12-Bit Data Formats for 8-Bit Systems.

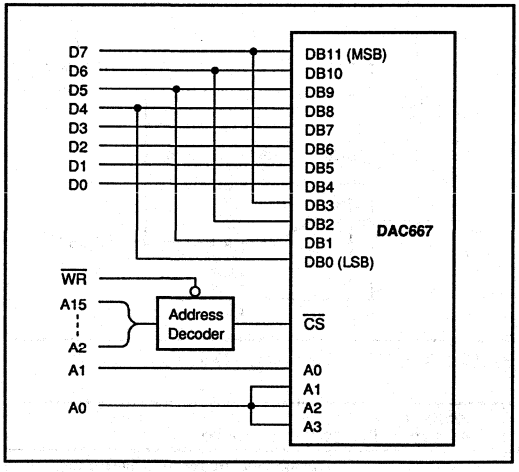


FIGURE 10. Left-Justified 8-Bit Bus Interface.

This configuration uses the first and second rank registers simultaneously. The $\overline{CS}$ input can be driven from an active-low decoded address. It should be noted that any data bus activity during the period when $\overline{CS}$ is low will cause activity at the DAC667 output. If data is not guaranteed stable during this period, the second rank register can be used to provide double buffering. See Figure 12.

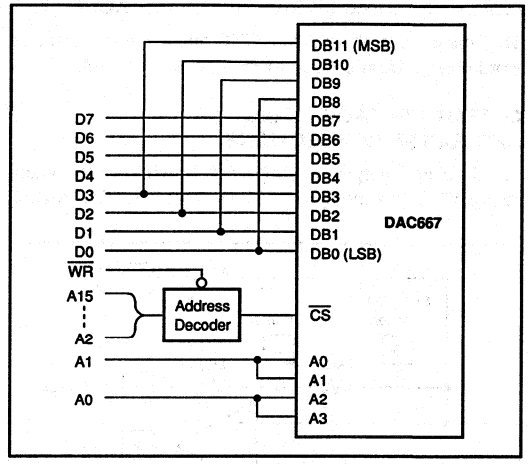


FIGURE 11. Right-Justified 8-Bit Bus Interface.

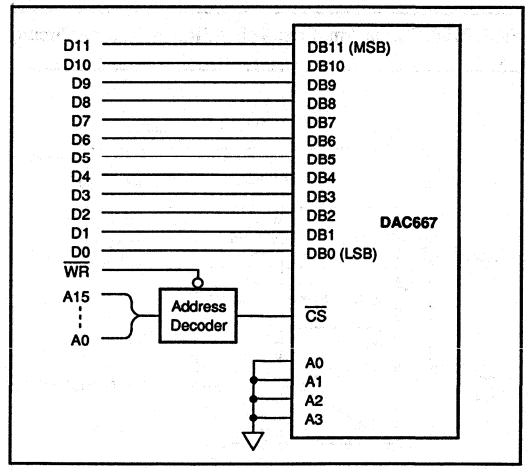


FIGURE 12. Connections for 12- and 16-Bit Bus Interface.

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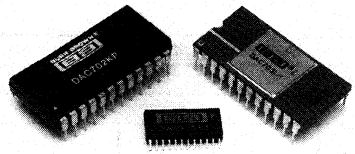


DAC700/702
DAC701/703

AVAILABLE IN DIE

Monolithic 16-Bit DIGITAL-TO-ANALOG CONVERTERS

FEATURES

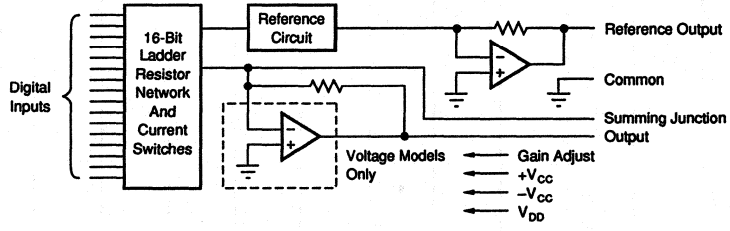
- MONOLITHIC CONSTRUCTION
- V_{OUT} AND I_{OUT} MODELS
- HIGH ACCURACY:
  Linearity Error ±0.0015% of FSR max
  Differential Linearity Error ±0.003% of FSR max
- MONOTONIC (at 15 bits) OVER FULL SPECIFICATION TEMPERATURE RANGE
- PIN-COMPATIBLE WITH DAC70, DAC71, DAC72
- LOW COST
- DUAL-IN-LINE PLASTIC AND HERMETIC CERAMIC AND SOIC
- /QM ENVIRONMENTAL SCREENING AVAILABLE
- BURN-IN PROGRAM AVAILABLE (-BI)

DESCRIPTION

This is another industry first from Burr-Brown—a complete 16-bit digital-to-analog converter that includes a precision buried-zener voltage reference and a low-noise, fast-settling output operational amplifier (voltage output models), all on one small monolithic chip. A combination of current-switch design techniques accomplishes not only 15-bit monotonicity over the entire specified temperature range, but also a maximum end-point linearity error of ±0.0015% of full-scale range. Total full-scale gain drift is limited to ±10ppm/°C maximum (LH and CH grades).

Digital inputs are complementary binary coded and are TTL-, LSTTL-, 54/74C- and 54/74HC-compatible over the entire temperature range. Outputs of 0 to +10V, ±10V, 0 to –2mA, and ±1mA are available.

These D/A converters are packaged in hermetic 24-pin ceramic side-brazed or molded plastic. The DIP-packaged parts are pin-compatible with the voltage and current output DAC71 and DAC72 model families. The DAC700 and DAC702 are also pin-compatible with the DAC70 model family. In addition, the DAC703 is offered in a 24-pin SOIC package for surface mount applications.



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Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL

At +25°C and rated power supplies unless otherwise noted.

MODEL	DAC702/703J, D			DAC700/701/702/703K			DAC700/701/702/703B, S			DAC700/701/702/703L, C			
PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
INPUT													
DIGITAL INPUT													
Resolution			16			•			•			•	Bits
Digital Inputs [1]													
V_{IH}	+2.4		+V_{CC}	•		•	•		•	•		•	V
V_{IL}	−1.0		+0.8	•		•	•		•	•		•	V
I_{IH}, V_I = +2.7V			+40			•			•			•	µA
I_{IL}, V_I = +0.4V		−0.35	−0.5		•	•		•	•		•	•	mA
TRANSFER CHARACTERISTICS													
ACCURACY[2]													
Linearity Error[4]		±0.0015	±0.006		•	±0.003		•	•		±0.00075	±0.0015	% of FSR[3]
Differential Linearity Error[4]		±0.003	±0.012		•	±0.006		•	•		±0.0015	±0.003	% of FSR
Differential Linearity Error at Bipolar Zero (DAC702/703)[4]					±0.003	±0.006		±0.0015	±0.003		•	•	% of FSR
Gain Error[5]		±0.07	±0.30		•	±0.15		±0.05	±0.10		•	•	%
Zero Error[5, 6]		±0.05	±0.10		•	•		•	•		•	•	% of FSR
Monotonicity Over Spec. Temp Range	13			14			•			15			Bits
DRIFT (over specification temperature range)													
Total Error Over Temperature Range (all models)[7]		±0.08			•	±0.15		±0.05	±0.10		•	•	% of FSR
Total Full Scale Drift:													
DAC700/701		±10			•	±30		±8.5	±18		±6	±13	ppm of FSR/°C
DAC702/703		±10			•	±25		±7	±15		•	•	ppm of FSR/°C
Gain Drift (all models)		±10	±30		•	±25		±7	±15		±5	±10	ppm/°C
Zero Drift:													
DAC700/701					±2.5	±5		±1.5	±3		•	•	ppm of FSR/°C
DAC702/703		±5	±15		•	±12		±4	±10		±2.5	±5	ppm of FSR/°C
Differential Linearity Over Temp.[4]			±0.012			+0.009, −0.006			•			+0.006, −0.003	% of FSR
Linearity Error Over Temp.[4]			±0.012			±0.006			•			±0.003	% of FSR
SETTLING TIME (to ±0.003% of FSR)[8]													
DAC701/703 (V_{OUT} Models)													
Full Scale Step, 2kΩ Load		4			•	8		•	•		•	•	µs
1LSB Step at Worst-Case Code[9]		2.5			•			•			•		µs
Slew Rate		10			•			•			•		V/µs
DAC700/702 (I_{OUT} Models)													
Full Scale Step (2mA),													
10 to 100Ω Load		350			•	1000		•	•		•	•	ns
1kΩ Load		1			•	3		•	•		•	•	µs
OUTPUT													
VOLTAGE OUTPUT MODELS													
DAC701 (CSB Code)					0 to +10			•					V
DAC703 (COB Code)		±10			•			•			•		V
Output Current	±5			•			•			•			mA
Output Impedance		0.15			•			•			•		Ω
Short Circuit to Common Duration		Indefinite			•			•			•		
CURRENT OUTPUT MODELS													
DAC700 (CSB Code)[10]					0 to −2			•			•		mA
Output Impedance[10]					4			•			•		kΩ
DAC702 (COB Code)[10]		±1			•			•			•		mA
Output Impedance[10]		2.45			•			•			•		kΩ
Compliance Voltage		±2.5			•			•			•		V

ELECTRICAL (CONT)

MODEL	DAC702/703J, D			DAC700/701/702/703K			DAC700/701/702/703B, S			DAC700/701/702/703L, C			
PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
REFERENCE VOLTAGE													
Voltage		+6.3		+6.0	+6.3	+6.6	+6.24	+6.3	+6.36	*	*	*	V
Source Current Available for External Loads		+2.5		+1.5	*		*	*		*	*		mA
Temperature Coefficient		±10			*	±25		*	±15		*	*	ppm/°C
Short Circuit to Common Duration		Indefinite			*			*			*		
POWER SUPPLY REQUIREMENTS													
Voltage: $+V_{CC}$	13.5	15	16.5	*	*	*	*	*	*	*	*	*	V
$-V_{CC}$	13.5	15	16.5	*	*	*	*	*	*	*	*	*	V
V_{DD}	+4.5	+5	+16.5	*	*	*	*	*	*	*	*	*	V
Current (No Load):													
DAC700/702													
(I_{OUT} Models)													
$+V_{CC}$		+10	+25		*	*		*	*		*	*	mA
$-V_{CC}$		−13	−25		*	*		*	*		*	*	mA
V_{DD}		+4	+8		*	*		*	*		*	*	mA
DAC701/703													
(V_{OUT} Models)													
$+V_{CC}$		+16	+30		*	*		*	*		*	*	mA
$-V_{CC}$		−18	−30		*	*		*	*		*	*	mA
V_{DD}		+4	+8		*	*		*	*		*	*	mA
Power Dissipation:													
(V_{DD} = +5.0V)(11)													
DAC700/702		365			*	790		*	630		*	*	mW
DAC701/703		530			*	940		*	780		*	*	mW
Power Supply Rejection:													
$+V_{CC}$		±0.0015	±0.006		*	*		*	±0.003		*	*	% of FSR/%V_{CC}
$-V_{CC}$		±0.0015	±0.006		*	*		*	±0.003		*	*	% of FSR/%V_{CC}
V_{DD}		±0.0001	±0.001		*	*		*	*		*	*	% of FSR/%V_{DD}
TEMPERATURE RANGE													
Specification:													
B, C Grades							−25		+85	*		*	°C
S Grades							−55		+125				°C
J, K, L Grades	0		+70	*		*				0		+70	°C
Storage: Ceramic				−60		+150	*		*	*		*	°C
Plastic, SOIC	−60		+100	*		*							°C

* Specification same as model to the left.

NOTES: (1) Digital inputs are TTL, LSTTL, 54/74C, 54/74HC, and 54/74HTC compatible over the operating voltage range of V_{DD} = +5V to +15V and over the specified temperature range. The input switching threshold remains at the TTL threshold of 1.4V over the supply range of V_{DD} = +5V to +15V. As logic "0" and logic "1" inputs vary over 0V to +0.8V and +2.4V to +10V respectively, the change in the D/A converter output voltage will not exceed ±0.0015% of FSR for the LH and CH grades, ±0.003% of FSR for the BH grade and ±0.006% of FSR for the KG grade. (2) DAC700 and DAC702 (current-output models) are specified and tested with an external output operational amplifier connected using the internal feedback resistor in all parameters except settling time. (3) FSR means full-scale range and is 20V for the ±10V range (DAC703), 10V for the 0 to +10V range (DAC701). FSR is 2mA for the ±1mA range (DAC702) and the 0 to +2mA range (DAC700). (4) ±0.0015% of full-scale range is equivalent to 1LSB in 15-bit resolution. ±0.003% of full-scale range is equivalent to 1LSB in 14-bit resolution. ±0.006% of full-scale range is equivalent to 1LSB in 13-bit resolution. (5) Adjustable to zero with external trim potentiometer. Adjusting the gain potentiometer rotates the transfer function around the zero point. (6) Error at input code $FFFF_H$ for DAC700 and DAC701, $7FFF_H$ for DAC702 and DAC703. (7) With gain and zero errors adjusted to zero at +25°C. (8) Maximum represents the 3σ limit. Not 100% tested for this parameter. (9) At the major carry, $7FFF_H$ to 8000_H and 8000_H to $7FFF_H$. (10) Tolerance on output impedance and output current is ±30%. (11) Power dissipation is an additional 40mW when V_{DD} is operated at +15V.

ABSOLUTE MAXIMUM RATINGS

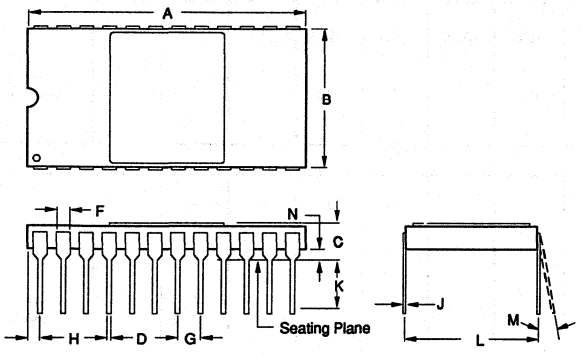
$+V_{CC}$ to Common ..... 0V, +18V
$-V_{CC}$ to Common ..... 0V, −18V
V_{DD} to Common ..... 0V, +18V
Digital Data Inputs to Common ..... −1V, +18V
Reference Out to Common ..... Indefinite Short to Common
External Voltage Applied to R_F (DAC700/702) ..... ±18V
External Voltage Applied to D/A Output (DAC701/703) ..... −5V to +5V
V_{OUT} (DAC701/703) ..... Indefinite Short to Common
Power Dissipation 1W
Storage Temperature ..... −60°C to +150°C
Lead Temperature (soldering, 10s) ..... 300°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

MECHANICAL

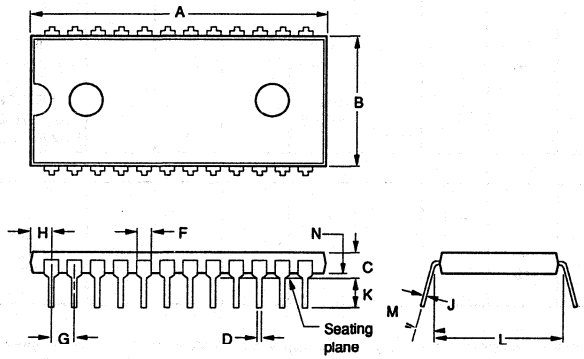
H Package—24-Pin Hermatic DIP



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.185	1.215	30.10	30.86
B	.600	.620	15.24	15.75
C	.125	.171	3.18	4.34
D	.015	.021	0.38	0.53
F	.035	.060	0.89	1.52
G	.100 BASIC		2.54 BASIC	
H	.030	.070	0.76	1.78
J	.008	.012	0.20	0.30
K	.120	.240	3.05	6.10
L	.600 BASIC		15.24 BASIC	
M	—	10°	—	10°
N	.025	.060	0.64	1.52

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

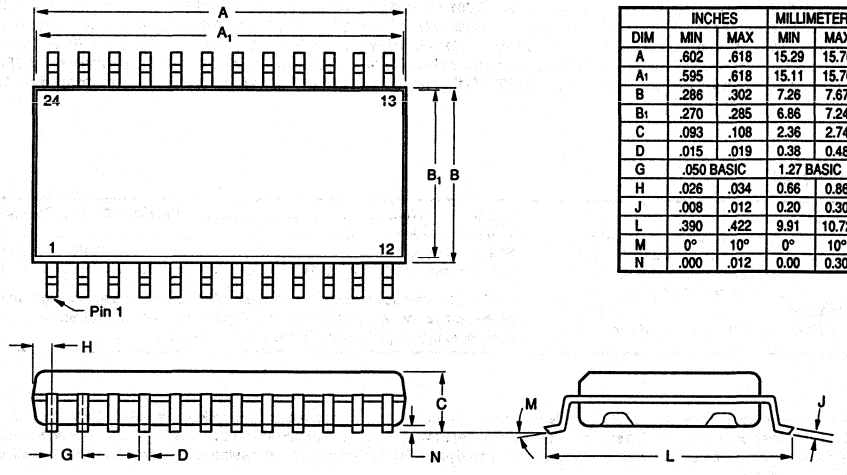
P Package—24-Pin Plastic DIP



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.233	1.283	31.32	32.59
B	.538	.575	13.67	14.61
C	.169	.224	4.29	5.70
D	.015	.023	0.38	0.58
F	.043	.062	1.09	1.57
G	.100 BASIC		2.54 BASIC	
H	.030	.090	0.76	2.29
J	.008	.015	0.20	0.38
K	.100	.132	2.54	3.35
L	.600 BASIC		15.24 BASIC	
M	0°	10°	0°	10°
N	.018	.022	0.46	0.56

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

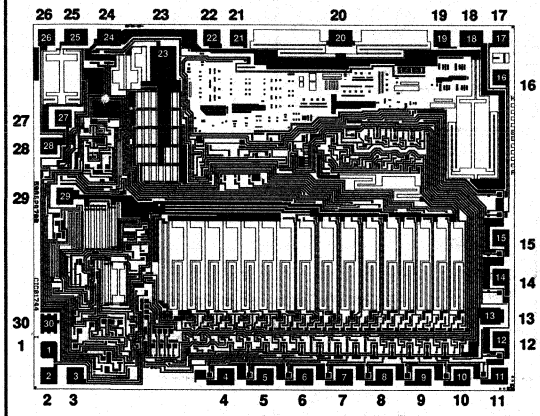
U Package (DAC703 Only) — 24-Pin SOIC



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.602	.618	15.29	15.70
A_1	.595	.618	15.11	15.70
B	.286	.302	7.26	7.67
B_1	.270	.285	6.86	7.24
C	.093	.108	2.36	2.74
D	.015	.019	0.38	0.48
G	.050 BASIC		1.27 BASIC	
H	.026	.034	0.66	0.86
J	.008	.012	0.20	0.30
L	.390	.422	9.91	10.72
M	0°	10°	0°	10°
N	.000	.012	0.00	0.30

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.

DICE INFORMATION



DAC702D DIE TOPOGRAPHY

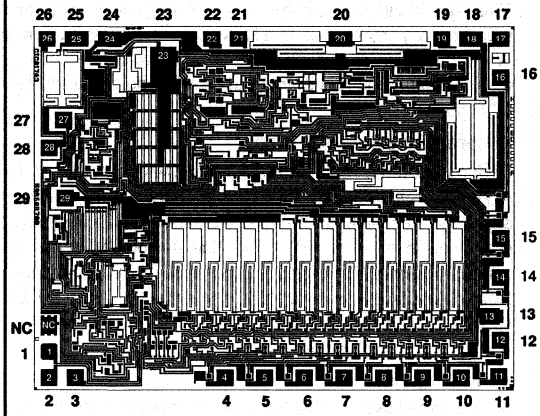
PAD	FUNCTION	PAD	FUNCTION
1	Bit 1 (MSB) Input	16	Bit 15 Input
2	Bit 2 Input	17	Bit 16 Input
3	Bit 3 Input	18	R_{FB} –10kΩ
4	Bit 4 Input	19	No Connection
5	Bit 5 Input	20	R_{FB} –10kΩ
6	Bit 6 Input	21	+5V Supply
7	Bit 7 Input	22	Digital Ground
8	Bit 8 Input	23	Analog Ground
9	Bit 9 Input	24	Current Output
10	Bit 10 Input	25	Bipolar Offset
11	Bit 11 Input	26	Gain Adjust
12	Bit 12 Input	27	+15V Supply
13	–15V Supply	28	Reference Output
14	Bit 13 Input	29	–15V Supply
15	Bit 14 Input	30	Zener Test Point
			Do Not Use

Substrate Bias: $-V_{CC}$

MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	153 x 120	3.89 x 3.05
Die Thickness	20 Mils	0.5
Min. Pad Size	4 x 4	0.1 x 0.1
Metalization	Aluminum	

See "DICE PRODUCTS" Section 17 in Data Book Supplement Volume 33c, or contact Burr-Brown for current information.



DAC703D DIE TOPOGRAPHY

PAD	FUNCTION	PAD	FUNCTION
1	Bit 1 (MSB) Input	16	Bit 15 Input
2	Bit 2 Input	17	Bit 16 Input
3	Bit 3 Input	18	R_{FB} –10kΩ
4	Bit 4 Input	19	Voltage Output
5	Bit 5 Input	20	R_{FB} –10kΩ
6	Bit 6 Input	21	+5V Supply
7	Bit 7 Input	22	Digital Ground
8	Bit 8 Input	23	Analog Ground
9	Bit 9 Input	24	Current Output
10	Bit 10 Input	25	Bipolar Offset
11	Bit 11 Input	26	Gain Adjust
12	Bit 12 Input	27	+15V Supply
13	–15V Supply	28	Reference Output
14	Bit 13 Input	29	–15V Supply
15	Bit 14 Input	30	Zener Test Point
			Do Not Use

Substrate Bias: $-V_{CC}$

MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	153 x 120	3.89 x 3.05
Die Thickness	20 Mils	0.5
Min. Pad Size	4 x 4	0.1 x 0.1
Metalization	Aluminum	

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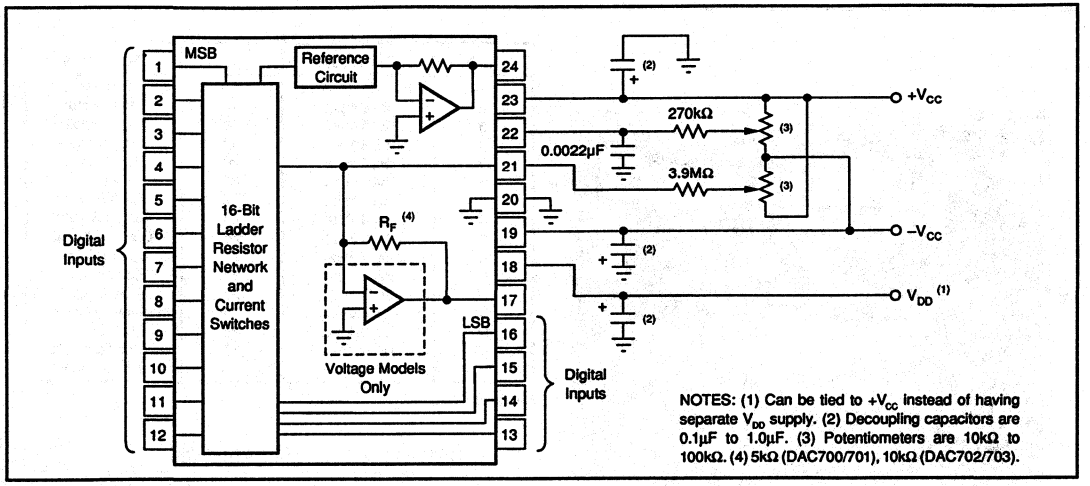
CONNECTION DIAGRAMS



PIN ASSIGNMENTS

PIN #	ALL PACKAGES	
	DAC700/702	DAC701/703
1	Bit 1 (MSB)	Bit 1 (MSB)
2	Bit 2	Bit 2
3	Bit 3	Bit 3
4	Bit 4	Bit 4
5	Bit 5	Bit 5
6	Bit 6	Bit 6
7	Bit 7	Bit 7
8	Bit 8	Bit 8
9	Bit 9	Bit 9
10	Bit 10	Bit 10
11	Bit 11	Bit 11
12	Bit 12	Bit 12
13	Bit 13	Bit 13
14	Bit 14	Bit 14
15	Bit 15	Bit 15
16	Bit 16 (LSB)	Bit 16 (LSB)
17	$R_{FEEDBACK}$	V_{OUT}
18	V_{DD}	V_{DD}
19	$-V_{CC}$	$-V_{CC}$
20	Common	Common
21	I_{OUT}	Summing Junction (Zero Adjust)
22	Gain Adjust	Gain Adjust
23	$+V_{CC}$	$+V_{CC}$
24	+6.3V Reference Output	+6.3V Reference Output

DIGITAL INPUT CODES	ANALOG OUTPUT		
	DAC700/701 Complementary Straight Binary (CSB)	DAC702/703 Complementary Offset Binary (COB)	DAC702/703 Complementary Two's Complement (CTC)*
0000_H	+ Full Scale	+ Full Scale	–1LSB
$7FFF_H$	+1/2 Full Scale	Bipolar Zero	– Full Scale
8000_H	+1/2 Full Scale –1LSB	–1LSB	+ Full Scale
$FFFF_H$	Zero	– Full Scale	Bipolar Zero

* Invert the MSB of the COB code with an external inverter to obtain CTC code.

TABLE I. Digital Input Codes.

DISCUSSION OF SPECIFICATIONS

DIGITAL INPUT CODES

The DAC700/701/702/703 accept complementary digital input codes in either binary format (CSB, unipolar or COB, bipolar). The COB models DAC702/703 may be connected by the user for either complementary offset binary (COB) or complementary two's complement (CTC) codes (see Table I).

ACCURACY

Linearity

This specification describes one of the most important measures of performance of a D/A converter. Linearity error is the deviation of the analog output from a straight line drawn through the end points (all bits ON point and all bits OFF point).

Differential Linearity Error

Differential linearity error (DLE) of a D/A converter is the deviation from an ideal 1LSB change in the output from one adjacent output state to the next. A differential linearity error specification of ±1/2LSB means that the output step sizes can be between 1/2LSB and 3/2LSB when the input changes from one adjacent input state to the next. A negative DLE specification of no more than –1LSB (–0.006% for 14-bit resolution) insures monotonicity.

Monotonicity

Monotonicity assures that the analog output will increase or remain the same for increasing input digital codes. The DAC700/701/702/703 are specified to be monotonic to 14 bits over the entire specification temperature range.

DRIFT

Gain Drift

Gain drift is a measure of the change in the full-scale range output over temperature expressed in parts per million per

ORDERING INFORMATION

MODEL	PACKAGE	OUTPUT CONFIGURATION	TEMPERATURE RANGE	LINEARITY ERROR, MAX AT +25°C (% of FSR)	GAIN DRIFT MAX (ppm/°C)
DAC702D,703D	25 Die/Pack	±1mA, ±10V	0°C to +70°C	±0.006	±30
DAC702JP, DAC703JP	Plastic DIP	±1mA, ±10V	0°C to +70°C	±0.006	±30
DAC702KP, DAC703KP	Plastic DIP	±1mA, ±10V	0°C to +70°C	±0.003	±25
DAC700KH, DAC701KH	Ceramic DIP	0 to –2mA, 0 to +10V	0°C to +70°C	±0.003	±25
DAC702KH, DAC703KH	Ceramic DIP	±1mA, ±10V	0°C to +70°C	±0.003	±25
DAC700BH, DAC701BH	Ceramic DIP	0 to –2mA, 0 to +10V	–25°C to +85°C	±0.003	±15
DAC702BH, DAC703BH	Ceramic DIP	±1mA, ±10V	–25°C to +85°C	±0.003	±15
DAC700BH/QM, DAC701BH/QM	Ceramic DIP	0 to –2mA, 0 to +10V	/QM Screening	±0.003	±15
DAC702BH/QM, DAC703BH/QM	Ceramic DIP	±1mA, ±10V	/QM Screening	±0.003	±15
DAC700LH, DAC701LH	Ceramic DIP	0 to –2mA, 0 to +10V	0°C to +70°C	±0.0015	±10
DAC700CH, DAC701CH	Ceramic DIP	0 to –2mA, 0 to +10V	–25°C to +85°C	±0.0015	±10
DAC700SH, DAC701SH	Ceramic DIP	0 to –2mA, 0 to +10V	–55°C to +125°C	±0.003	±15
DAC702LH, DAC703LH	Ceramic DIP	±1mA, ±10V	0°C to +70°C	±0.0015	±10
DAC702CH, DAC703CH	Ceramic DIP	±1mA, ±10V	–25°C to +85°C	±0.0015	±10
DAC702SH, DAC703SH	Ceramic DIP	±1mA, ±10V	–55°C to +125°C	±0.003	±15
DAC703JU	Plastic SOIC	±10V	0°C to +70°C	±0.006	
DAC703KU	Plastic SOIC	±10V	0°C to +70°C	±0.003	

BURN-IN SCREENING OPTION—See Text for Details.

MODEL	PACKAGE	OUTPUT CONFIGURATION	TEMPERATURE RANGE	LINEARITY ERROR, MAX AT +25°C (% of FSR)	BURN-IN TEMP. (160h)[1]
DAC702JP-BI	Plastic DIP	±1mA	0°C to +70°C	±0.006	85°C
DAC703JP-BI	Plastic DIP	±10V	0°C to +70°C	±0.006	85°C
DAC702KP-BI	Plastic DIP	±1mA	0°C to +70°C	±0.003	85°C
DAC703KP-BI	Plastic DIP	±10V	0°C to +70°C	±0.003	85°C
DAC700KH-BI	Ceramic DIP	0 to –2mA	0°C to +70°C	±0.003	85°C
DAC700LH-BI	Ceramic DIP	0 to –2mA	0°C to +70°C	±0.0015	85°C
DAC700BH-BI	Ceramic DIP	0 to –2mA	–25°C to +85°C	±0.003	85°C
DAC700CH-BI	Ceramic DIP	0 to –2mA	–25°C to +85°C	±0.0015	85°C
DAC700SH-BI	Ceramic DIP	0 to –2mA	–55°C to +125°C	±0.003	125°C
DAC701KH-BI	Ceramic DIP	0 to +10V	0°C to +70°C	±0.003	85°C
DAC701LH-BI	Ceramic DIP	0 to +10V	0°C to +70°C	±0.0015	85°C
DAC701BH-BI	Ceramic DIP	0 to +10V	–25°C to +85°C	±0.003	85°C
DAC701CH-BI	Ceramic DIP	0 to +10V	–25°C to +85°C	±0.0015	85°C
DAC701SH-BI	Ceramic DIP	0 to +10V	–55°C to +125°C	±0.003	125°C
DAC702KH-BI	Ceramic DIP	±1mA	0°C to +70°C	±0.003	85°C
DAC702LH-BI	Ceramic DIP	±1mA	0°C to +70°C	±0.0015	85°C
DAC702BH-BI	Ceramic DIP	±1mA	–25°C to +85°C	±0.003	85°C
DAC702CH-BI	Ceramic DIP	±1mA	–25°C to +85°C	±0.0015	85°C
DAC702SH-BI	Ceramic DIP	±1mA	–55°C to +125°C	±0.003	125°C
DAC703KH-BI	Ceramic DIP	±10V	0°C to +70°C	±0.003	85°C
DAC703LH-BI	Ceramic DIP	±10V	0°C to +70°C	±0.0015	85°C
DAC703BH-BI	Ceramic DIP	±10V	–25°C to +85°C	±0.003	85°C
DAC703CH-BI	Ceramic DIP	±10V	–25°C to +85°C	±0.0015	85°C
DAC703SH-BI	Ceramic DIP	±10V	–55°C to +125°C	±0.003	125°C

NOTE: (1) Or equivalent combination of time and temperature.

degree centigrade (ppm/°C). Gain drift is established by: (1) testing the end point differences for each D/A at t_{MIN}, +25°C and t_{MAX}; (2) calculating the gain error with respect to the +25°C value; and (3) dividing by the temperature change.

Zero Drift

Zero drift is a measure of the change in the output with $FFFF_H$ (DAC700 and DAC701) applied to the digital inputs over the specified temperature range. For the bipolar models, zero is measured at $7FFF_H$ (bipolar zero) applied to the digital inputs. This code corresponds to zero volts (DAC703) or zero milliamps (DAC702) at the analog output. The maximum change in offset at t_{MIN} or t_{MAX} is referenced to the zero error at +25°C and is divided by the temperature change. This drift is expressed in parts per million of full scale range per degree centigrade (ppm of FSR/°C).

SETTLING TIME

Settling time of the D/A is the total time required for the analog output to settle within an error band around its final value after a change in digital input. Refer to Figure 1 for typical values for this family of products.

Voltage Output

Settling times are specified to ±0.003% of FSR (±1/2LSB for 14 bits) for two input conditions: a full-scale range change of 20V (DAC703) or 10V (DAC701) and a 1LSB change at the "major carry," the point at which the worst-case settling

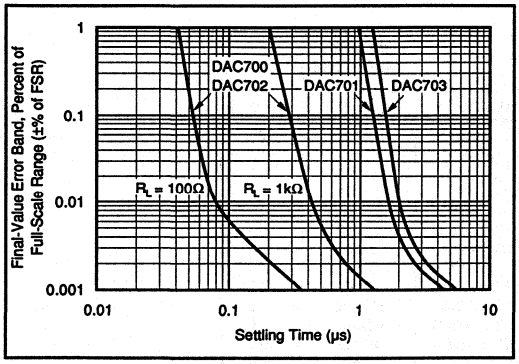


FIGURE 1. Final-Value Error Band vs Full-Scale Range Settling Time.

time occurs. (This is the worst-case point since all of the input bits change when going from one code to the next).

Current Output

Settling times are specified to ±0.003% of FSR for a full-scale range change for two output load conditions: one for 10Ω to 100Ω and one for 1000Ω. It is specified this way because the output RC time constant becomes the dominant factor in determining settling time for large resistive loads.

COMPLIANCE VOLTAGE

Compliance voltage applies only to current output models. It is the maximum voltage swing allowed on the output current pin while still being able to maintain specified accuracy.

POWER SUPPLY SENSITIVITY

Power supply sensitivity is a measure of the effect of a change in a power supply voltage on the D/A converter output. It is defined as a percent of FSR change in the output per percent of change in either the positive supply ($+V_{CC}$), negative supply ($-V_{CC}$) or logic supply (V_{DD}) about the nominal power supply voltages (see Figure 2).

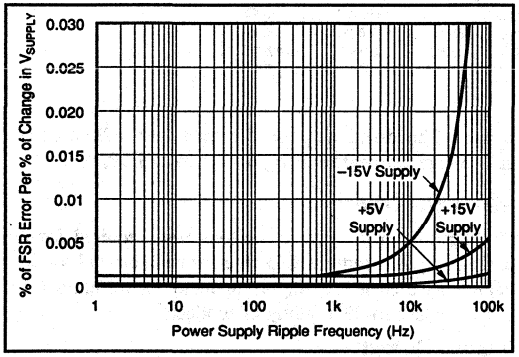


FIGURE 2. Power Supply Rejection vs Power Supply Ripple Frequency.

It is specified for DC or low frequency changes. The typical performance curve in Figure 2 shows the effect of high frequency changes in power supply voltages.

REFERENCE SUPPLY

All models have an internal low-noise +6.3V reference voltage derived from an on-chip buried zener diode. This reference voltage, available to the user, has a tolerance of ±5% (KH models) and ±1% (BH models). A minimum of 1.5mA is available for external loads. Since the output impedance of the reference output is typically 1W, the external load should remain constant.

If a varying load is to be driven by the reference supply, an external buffer amplifier is recommended to drive the load in order to isolate the bipolar offset (connected internally to the reference) from load variations.

BURN-IN SCREENING

Burn-in screening is an option available for selected models of the DAC700 family of products. Burn-in duration is 160 hours at the temperature shown below (or equivalent combination of time and temperature).

MODEL	TEMP. RANGE	BURN-IN SCREENING
DAC700BH-BI	–25°C to +85°C	160 hours at 85°C
DAC702SH-BI	–55°C to +125°C	160 hours at 125°

All units are tested after burn-in to ensure that grade specifications are met. To order burn-in add "-BI" to the base model number.

ENVIRONMENTAL SCREENING

/QM Screening

Burr-Brown /QM models are environmentally screened versions of our standard industrial products designed to provide enhanced reliability. The screening, tabulated below, is performed to selected methods of MIL-STD-883. Reference to these methods provides a convenient method of communicating the screening levels and basic procedures employed; it does not imply conformance to any other military standards or to any methods of MIL-STD-883 other than those specified below. Burr-Brown's detailed procedures may vary slightly, model-to-model, from those in MIL-STD-883.

Screening Flow for /QM Models

SCREEN	MIL-STD-883 METHOD	CONDITION	COMMENTS
Internal Visual	BBC Standard		QC4118
High Temperature Storage (Stabilization Bake)	1008	C	+150°C, 24h
Temperature Cycling	1010	C	–65°C to +150°C, 10 cycles
Burn-In	1015	B	–125°C, 160h
Constant Acceleration	2001	E	30,000G
Hermeticity Fine Leak Gross Leak	 1014 1014	 A1 or A2 C	 5×10^{-8} atm cc/s 60psig, 2h
External Visual	BBC Standard		QC5150

OPERATING INSTRUCTIONS

POWER SUPPLY CONNECTIONS

For optimum performance and noise rejection, power supply decoupling capacitors should be added as shown in the Connection Diagram. 1µF tantalum capacitors should be located close to the D/A converter.

EXTERNAL ZERO AND GAIN ADJUSTMENT

Zero and gain may be trimmed by installing external zero and gain potentiometers. Connect these potentiometers as shown in the Connection Diagram and adjust as described below. TCR of the potentiometers should be 100ppm/°C or less. The 3.9MΩ and 270kΩ resistors (±20% carbon or better) should be located close to the D/A converter to prevent noise pickup. If it is not convenient to use these high-value resistors, an equivalent "T" network, as shown in Figure 3, may be substituted in place of the 3.9MΩ part. A 0.001µF to 0.01µF ceramic capacitor should be connected from Gain Adjust to Common to prevent noise pickup. Refer to Figures 4 and 5 for the relationship of zero and gain adjustments to unipolar and bipolar D/A converters.

Zero Adjustment

For unipolar (CSB) configurations, apply the digital input code that produces zero voltage or zero current output and adjust the zero potentiometer for zero output.

For bipolar (COB, CTC) configurations, apply the digital input code that produces zero output voltage or current. See Table II for corresponding codes and the Connection Diagram for zero adjustment circuit connections. Zero calibration should be made before gain calibration.

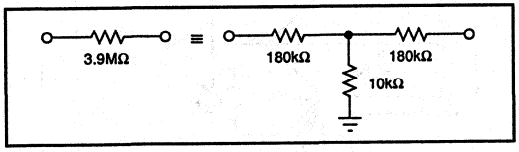


FIGURE 3. Equivalent Resistances.

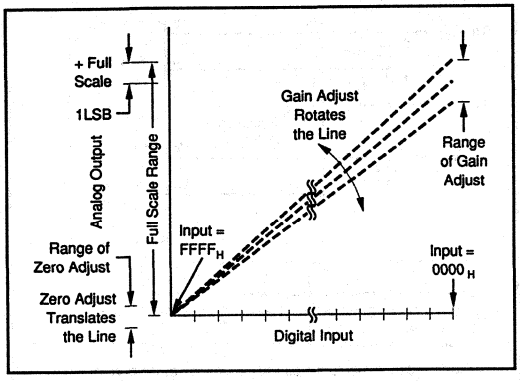


FIGURE 4. Relationship of Zero and Gain Adjustments for Unipolar D/A Converters, DAC700 and DAC701.

Gain Adjustment

Apply the digital input that gives the maximum positive output voltage. Adjust the gain potentiometer for this positive full scale voltage. See Table II for positive full scale voltages and the Connection Diagram for gain adjustment circuit connections.

INSTALLATION CONSIDERATIONS

This D/A converter family is laser-trimmed to 14-bit linearity. The design of the device makes the 16-bit resolution available. If 16-bit resolution is not required, bit 15 and bit 16 should be connected to V_{DD} through a single 1kΩ resistor.

Due to the extremely high resolution and linearity of the D/A converter, system design problems such as grounding and contact resistance become very important. For a 16-bit converter with a 10V full-scale range, 1LSB is 153µV. With a load current of 5mA, series wiring and connector resistance of only 30mΩ will cause the output to be in error by 1LSB. To understand what this means in terms of a system layout, the resistance of #23 wire is about 0.021Ω/ft. Neglecting contact resistance, less than 18 inches of wire will produce a 1LSB error in the analog output voltage!

In Figures 6, 7, and 8, lead and contact resistances are represented by R_1 through R_5. As long as the load resistance R_L is constant, R_2 simply introduces a gain error and can be removed during initial calibration. R_3 is part of R_L, if the output voltage is sensed at Common, and therefore introduces no error. If R_L is variable, then R_2 should be less than $R_{L\,MIN}/2^{16}$ to reduce voltage drops due to wiring to less than 1LSB. For example, if $R_{L\,MIN}$ is 5kΩ, then R_2 should be less than 0.08Ω. R_L should be located as close as possible to the D/A converter for optimum performance. The effect of R_4 is negligible.

In many applications it is impractical to sense the output voltage at the output pin. Sensing the output voltage at the system ground point is permissible with the DAC700 family

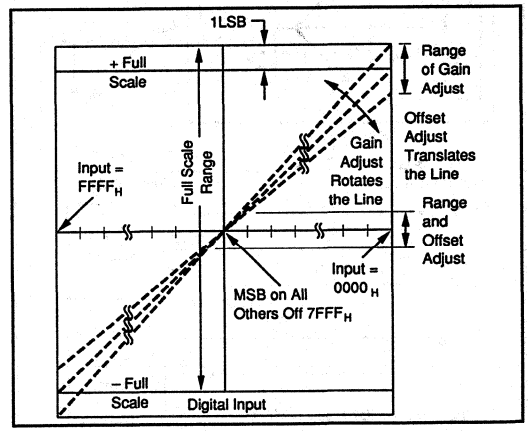


FIGURE 5. Relationship of Zero and Gain Adjustments for Bipolar D/A Converters, DAC702 and DAC703.

VOLTAGE OUTPUT MODELS							
		ANALOG OUTPUT					
		DAC701 UNIPOLAR			DAC703 BIPOLAR		
DIGITAL INPUT CODE		16-BIT	15-BIT	14-BIT	16-BIT	15-BIT	14-BIT
1LSB	(μV)	153	305	610	305	610	1224
0000_H	(V)	+9.99985	+9.99969	+9.99939	+9.99960	+9.99939	+9.99878
$FFFF_H$	(V)	0	0	0	−10.0000	−10.0000	−10.0000
ANALOG OUTPUT MODELS							
		ANALOG OUTPUT					
		DAC700 UNIPOLAR			DAC702 BIPOLAR		
DIGITAL INPUT CODE		16-BIT	15-BIT	14-BIT	16-BIT	15-BIT	14-BIT
1LSB	(μA)	0.031	0.061	0.122	0.031	0.061	0.122
0000_H	(mA)	−1.99997	−1.99994	−1.99988	−0.99997	−0.99994	−0.99988
$FFFF_H$	(mA)	0	0	0	+1.00000	+1.00000	+1.00000

TABLE II. Digital Input and Analog Output Relationships.

because the D/A converter is designed to have a constant return current of approximately 2mA flowing from Common. The variation in this current is under 20μA (with changing input codes), therefore R_4 can be as large as 3Ω without adversely affecting the linearity of the D/A converter. The voltage drop across R_4 (R_4 x 2mA) appears as a zero error and can be removed with the zero calibration adjustment. This alternate sensing point (the system ground point) is shown in Figures 6, 7, and 8.

Figures 7 and 8 show two methods of connecting the current output models (DAC700 or DAC702) with external precision output op amps. By sensing the output voltage at the load resistor (ie, by connecting R_F to the output of A_1 at R_L), the effect of R_1 and R_2 is greatly reduced. R_1 will cause a gain error but is independent of the value of R_L and can be eliminated by initial calibration adjustments. The effect of R_2 is negligible because it is inside the feedback loop of the output op amp and is therefore greatly reduced by the loop gain.

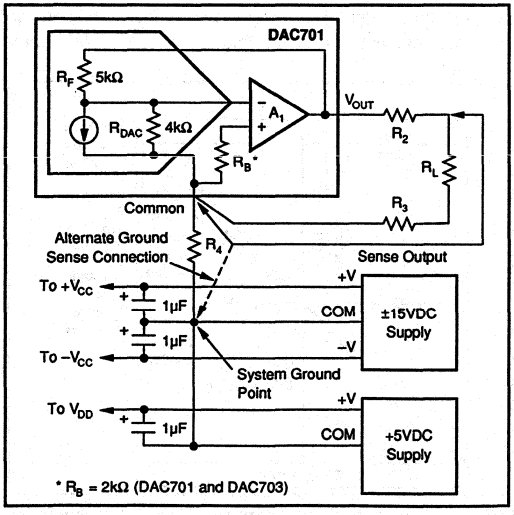
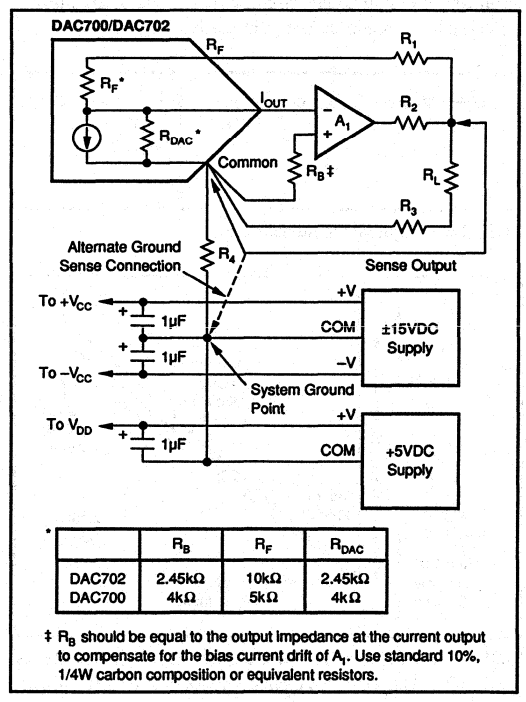


FIGURE 6. Output Circuit for Voltage Models.

If the output cannot be sensed at Common or the sytem ground point as mentioned above, the differential output circuit shown in Figure 8 is recommended. In this circuit the output voltage is sensed at the load common and not at the D/A converter common as in the previous circuits. The value of R_6 and R_7 must be adjusted for maximum common-mode rejection at R_L. Note that if R_3 is negligible, the circuit of Figure 8 can be reduced to the one shown in Figure 7. Again the effect of R_4 is negligible.

The D/A converter and the wiring to its connectors should be located to provide optimum isolation from sources of RFI and EMI. The key concept in elimination of RF radiation or



	R_B	R_F	R_{DAC}
DAC702	2.45kΩ	10kΩ	2.45kΩ
DAC700	4kΩ	5kΩ	4kΩ

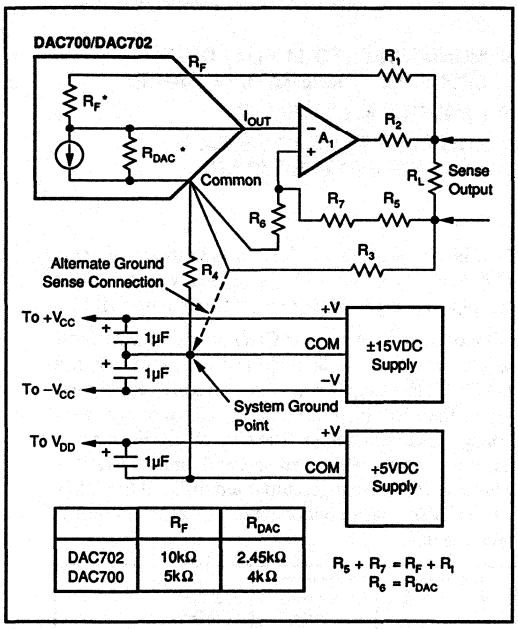
FIGURE 7. Preferred External Op Amp Configuration.

pickup is loop area; therefore, signal leads and their return conductors should be kept close together. This reduces the external magnetic field along with any radiation. Also, if a single lead and its return conductor are wired close together, they present a small flux-capture cross section for any external field. This reduces radiation pickup in the circuit.

APPLICATIONS

DRIVING AN EXTERNAL OP AMP WITH CURRENT OUTPUT D/AS

DAC700 and DAC702 are current output devices and will drive the summing junction of an op amp to produce an output voltage as shown in Figure 9. Use of the internal feedback resistor is required to obtain specified gain accuracy and low gain drift.



	R_F	R_{DAC}
DAC702	10kΩ	2.45kΩ
DAC700	5kΩ	4kΩ

FIGURE 8. Differential Sensing Output Op Amp Configuration.

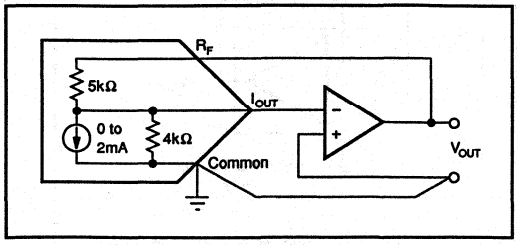


FIGURE 9. External Op Amp Using Internal Feedback Resistors.

DAC700 or DAC702 can be scaled for any desired voltage range with an external feedback resistor, but at the expense of increased drifts of up to ±50ppm/°C. The resistors in the DAC700 and DAC702 ratio track to ±1ppm/°C but their absolute TCR may be as high as ±50ppm/°C.

An alternative method of scaling the output voltage of the D/A converter and preserving the low gain drift is shown in Figure 10.

OUTPUTS LARGER THAN 20V RANGE

For output voltage ranges larger than ±10V, a high voltage op amp may be employed with an external feedback resistor. Use I_{OUT} values of ±1mA for bipolar voltage ranges and –2mA for unipolar voltage ranges (see Figure 11). Use protection diodes as shown when a high voltage op amp is used.

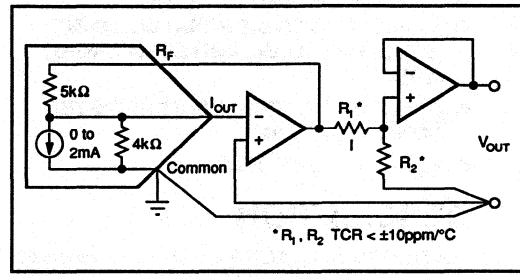


FIGURE 10. External Op Amp Using Internal and External Feedback Resistors to Maintain Low Gain Drift.

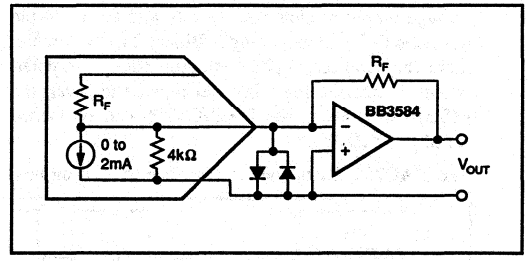


FIGURE 11. External Op Amp Using External Feedback Resistors.

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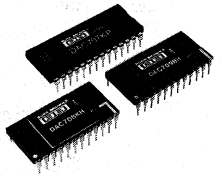


DAC707
DAC708/709

Microprocessor-Compatible 16-BIT DIGITAL-TO-ANALOG CONVERTERS

FEATURES

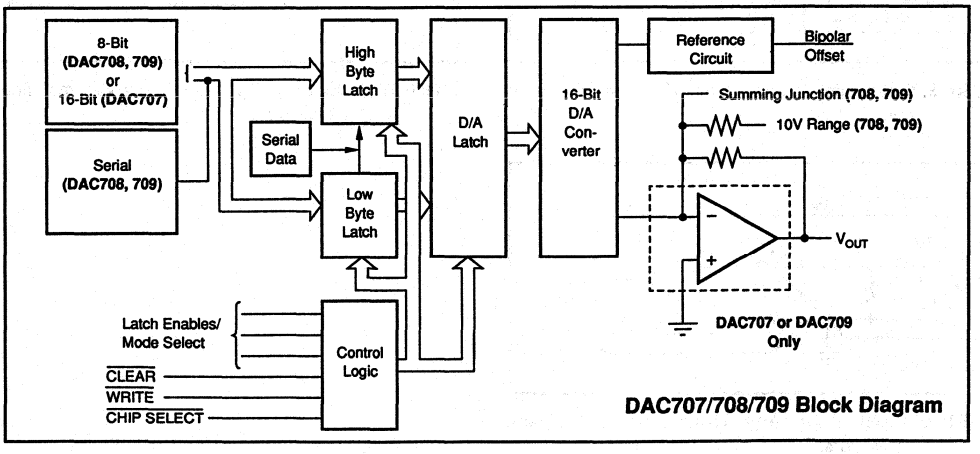
- TWO-CHIP CONSTRUCTION
- HIGH-SPEED 16-BIT PARALLEL, 8-BIT (BYTE) PARALLEL, AND SERIAL INPUT MODES
- DOUBLE-BUFFERED INPUT REGISTER CONFIGURATION
- V_{OUT} AND I_{OUT} MODELS
- HIGH ACCURACY: Linearity Error ±0.003% of FSR max Differential Linearity Error ±0.006% of FSR max
- MONOTONIC (TO 14 BITS) OVER SPECIFIED TEMPERATURE RANGE
- HERMETICALLY SEALED
- LOW COST PLASTIC VERSIONS AVAILABLE (DAC707JP/KP)

DESCRIPTION

The DAC708 and DAC709 are 16-bit converters designed to interface to an 8-bit microprocessor bus. 16-bit data is loaded in two successive 8-bit bytes into parallel 8-bit latches before being transferred into the D/A latch. The DAC708 and DAC709 are current and voltage output models respectively and are in 24-pin hermetic DIPs. Input coding is Binary Two's Complement (bipolar) or Unipolar Straight Binary (unipolar, when an external logic inverter is used to invert the MSB). In addition, the DAC708/709 can be loaded serially (MSB first).

The DAC707 is designed to interface to a 16-bit bus. Data is written into a 16-bit latch and subsequently the D/A latch. The DAC707 has bipolar voltage output and input coding is Binary Two's Complement (BTC).

All models have Write and Clear control lines as well as input latch enable lines. In addition, DAC708 and DAC709 have Chip Select control lines. In the bipolar mode, the Clear input sets the D/A latch to give zero voltage or current output. They are all 14-bit accurate and are complete with reference, and for the DAC707, and DAC709, a voltage output amplifier. All models are available with an optional burn-in, or environmental screening.



DAC707/708/709 Block Diagram

International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL

At T_A = +25°C, V_{CC} = ±15V, V_{DD} = +5V, and after a 10-minute warm-up unless otherwise noted.

MODEL	DAC707JP			DAC707/708/709KH, DAC707KP			DAC707/708/709BH, SH			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
INPUT										
DIGITAL INPUT										
Resolution			16			•			•	Bits
Bipolar Input Code (all models)		Binary Two's Complement			•			•		
Unipolar Input Code[1] (DAC708/709 only)					Unipolar Straight Binary			•		
Logic Levels[2]: V_{IH}	+2.0		+5.5	•		•	•		•	V
V_{IL}	–1.0		+0.8	•		•	•		•	V
I_{IH} (V_I = +2.7V)			1			•			•	µA
I_{IL} (V_I = +0.4V)			1			•			•	µA
TRANSFER CHARACTERISTICS										
ACCURACY[3]										
Linearity Error		±0.003	±0.006		±0.0015	±0.003		•	•	% of FSR[4]
Differential Linearity Error[5]		±0.0045	±0.012		±0.003	±0.006		•	•	% of FSR
at Bipolar Zero[5, 6]					±0.003	±0.006		±0.0015	±0.003	% of FSR
Gain Error[7]		±0.07	±0.30		•	±0.15		±0.05	±0.10	%
Zero Error[7]		±0.05	±0.1		•	•		•	•	% of FSR
Monotonicity Over Spec Temp Range	13			14			14			Bits
Power Supply Sensitivity: $+V_{CC}$, $-V_{CC}$		±0.0015	±0.006		•	•		•	±0.003	% of FSR/%V_{CC}
V_{DD}		±0.0001	±0.001		•	•		•	•	% of FSR/%V_{DD}
DRIFT (Over Spec Temp Range[3])										
Total Error Over Temp Range[8]		±0.08			•	±0.15		•	±0.10	% of FSR
Total Full Scale Drift		±10			•	±25		•	±15	ppm of FSR/°C
Gain Drift		±10	±30		•	±25		±7	±15	ppm/°C
Zero Drift: Unipolar (DAC708/709 only)					±2.5	±5		±1.5	±3	ppm of FSR/°C
Bipolar (all models)		±5	±15		•	±12		±4	±10	ppm of FSR/°C
Differential Linearity Over Temp[5]			±0.012			+0.009, –0.006			•	% of FSR
Linearity Error Over Temp[5]			±0.012			±0.006			•	% of FSR
SETTLING TIME (to ±0.003% of FSR)[9]										
Voltage Output Models										
Full Scale Step (2kΩ load)		4			•	8		•	8	µs
1LSB Step at Worst Case Code[10]		2.5			•	4		•	4	µs
Slew Rate		10			•			•		V/µs
Current Output Models										
Full Scale Step (2mA): 10 to 100Ω Load					350			•		ns
1kΩ Load					1			•		µs
OUTPUT										
VOLTAGE OUTPUT MODELS										
Output Voltage Range										
DAC709: Unipolar (USB Code)					0 to +10			•		V
Bipolar (BTC Code)					±5, ±10			•		V
DAC707 Bipolar (BTC Code)		±10			•			•		V
Output Current	±5			•			•			mA
Output Impedance		0.15			•			•		Ω
Short Circuit to Common Duration		Indefinite			•			•		
CURRENT OUTPUT MODELS										
Output Current Range (±30% typ)										
DAC708: Unipolar (USB Code)					0 to –2			•		mA
Bipolar (BTC Code)					±1			•		mA
Unipolar Output Impedance (±30% typ)					4.0			•		kΩ
Bipolar Output Impedance (±30% typ)					2.45			•		kΩ
Compliance Voltage					±2.5			•		V

ELECTRICAL (CONT)

At T_A = +25°C, V_{CC} = ±15V, V_{DD} = +5V, and after a 10-minute warm-up unless otherwise noted.

MODEL	DAC707JP			DAC707/708/709KH, DAC707KP			DAC707/708/709BH, SH			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
POWER SUPPLY REQUIREMENTS										
Voltage (all models): $+V_{CC}$	+13.5	+15	+16.5	*	*	*	*	*	*	V
$-V_{CC}$	−13.5	−15	−16.5	*	*	*	*	*	*	V
V_{DD}	+4.5	+5	+5.5	*	*	*	*	*	*	V
Current (No Load, +15V Supplies)										
Current Output Models: $+V_{CC}$					+10	+25		*	*	mA
$-V_{CC}$					−13	−25		*	*	mA
V_{DD}					+5	+10		*	*	mA
Voltage Output Models: $+V_{CC}$		+16	+30		*	*		*	*	mA
$-V_{CC}$		−18	−30		*	*		*	*	mA
V_{DD}		+5	+10		*	*		*	*	mA
Power Dissipation (±15V supplies)										
Current Output Models					370	800		*	*	mW
Voltage Output Models		535			*	950		*	*	mW
TEMPERATURE RANGE										
Specification: BH Grades							−25		+85	°C
JP, KP, KH Grades	0		+70	*		*				°C
SH Grades							−55		+125	°C
Storage: Ceramic				−65		+150	−65		+150	°C
Plastic	−60		+100	*		*				°C

*Specification same as for models in column to the left.

NOTES: (1) MSB must be inverted externally prior to DAC708/709 input. (2) Digital inputs are TTL, LSTTL, 54/74C, 54/74HC and 54/74HTC compatible over the specified temperature range. (3) DAC708 (current-output models) are specified and tested with an external output operational amplifier connected using the internal feedback resistor in all tests. (4) FSR means Full Scale Range. For example, for ±10V output, FSR = 20V. (5) ±0.0015% of Full Scale Range is equal to 1 LSB in 16-bit resolution, ±0.003% of Full Scale Range is equal to 1 LSB in 15-bit resolution. ±0.006% of Full Scale Range is equal to 1 LSB in 14-bit resolution. (6) Error at input code 0000_H. (For unipolar connection on DAC708/709, the MSB must be inverted externally prior to D/A input.) (7) Adjustable to zero with external trim potentiometer. Adjusting the gain potentiometer rotates the transfer function around the bipolar zero point. (8) With gain and zero errors adjusted to zero at +25°C. (9) Maximum represents the 3σ limit. Not 100% tested for this parameter. (10) The bipolar worst-case code change is $FFFF_H$ to 0000_H and 0000_H to $FFFF_H$. For unipolar (DAC708/709 only) it is $7FFF_H$ to 8000_H and 8000_H to $7FFF_H$.

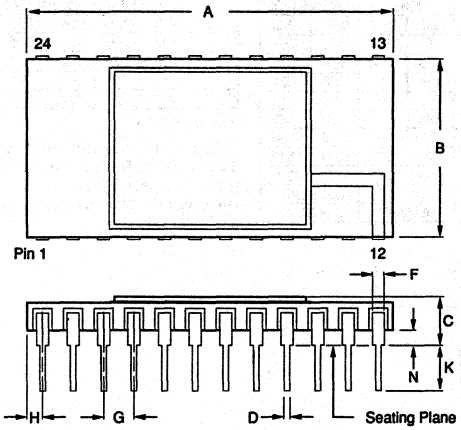
The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

ORDERING INFORMATION

MODEL	TEMPERATURE RANGE	INPUT CONFIG	OUTPUT CONFIG
DAC707JP	0°C to +70°C	16-bit port	±10V output
DAC707JP-BI	0°C to +70°C	16-bit port	±10V output
DAC707KP	0°C to +70°C	16-bit port	±10V output
DAC707KP-BI	0°C to +70°C	16-bit port	±10V output
DAC707KH	0°C to +70°C	16-bit port	±10V output
DAC707KH-BI	0°C to +70°C	16-bit port	±10V output
DAC707BH	–25°C to +85°C	16-bit port	±10V output
DAC707BH-BI	–25°C to +85°C	16-bit port	±10V output
DAC707BH/QM	–25°C to +85°C	16-bit port	±10V output
DAC707SH	–55°C to +125°C	16-bit port	±10V output
DAC707SH-BI	–55°C to +125°C	16-bit port	±10V output
DAC708KH	0°C to +70°C	8-bit port	±1mA output
DAC708KH-BI	0°C to +70°C	8-bit port	±1mA output
DAC708BH	–25°C to +85°C	8-bit port	±1mA output
DAC708BH-BI	–25°C to +85°C	8-bit port	±1mA output
DAC708BH/QM	–25°C to +85°C	8-bit port	±1mA output
DAC708SH	–55°C to +125°C	8-bit port	±1mA output
DAC708SH-BI	–55°C to +125°C	8-bit port	±1mA output
DAC709KH	0°C to +70°C	8-bit port	±10V output
DAC709KH-BI	0°C to +70°C	8-bit port	±10V output
DAC709BH	–25°C to +85°C	8-bit port	±10V output
DAC709BH-BI	–25°C to +85°C	8-bit port	±10V output
DAC709BH/QM	–25°C to +85°C	8-bit port	±10V output
DAC709SH	–55°C to +125°C	8-bit port	±10V output
DAC709SH-BI	–55°C to +125°C	8-bit port	±10V output

MECHANICAL

H Package — 24-Pin Hermatic DIP—DAC708/709H



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.190	1.210	30.23	30.73
B	.580	.600	14.73	15.24
C	.140	.185	3.56	4.70
D	.016	.020	0.41	0.51
F	.030	.050	0.76	1.27
G	.100 BASIC		2.54 BASIC	
H	.035	.065	0.89	1.65
J	.009	.012	0.23	0.30
K	.125	.180	3.18	4.57
L	.600 BASIC		15.24 BASIC	
N	.040	.060	1.02	1.52

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.

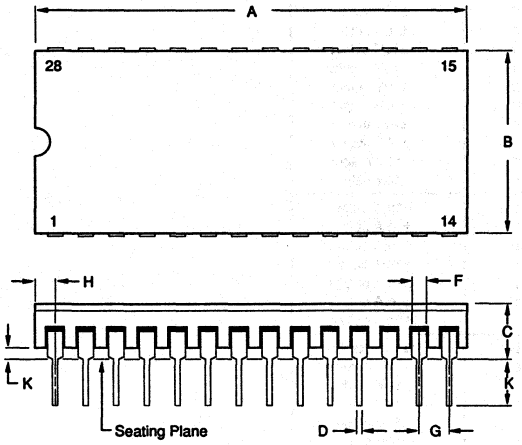
ABSOLUTE MAXIMUM RATINGS

V_{DD} to COMMON ..... 0V, +15V
$+V_{CC}$ to COMMON ..... 0V, +18V
$-V_{CC}$ to COMMON ..... 0V, –18V
Digital Data Inputs to COMMON ..... –0.5V, V_{DD} +0.5
DC Current any Input ..... ±10mA
Reference Out to COMMON ..... Indefinite Short to COMMON
V_{OUT} (DAC707, DAC709) ..... Indefinite Short to COMMON
External Voltage Applied to R_F (pin 13 or 14, DAC708) ..... ±18V
External Voltage Applied to D/A Output
(pin 1, DAC707; pin 14, DAC708) ..... ±5V
Power Dissipation 1000mW
Storage Temperature ..... –60°C to +150°C
Lead Temperature (soldering, 10s) ..... 300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

MECHANICAL

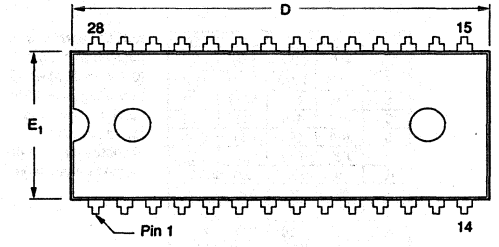
H Package — 28-Pin Hermetic DIP— DAC707-H



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.386	1.465	35.20	37.21
B	.610 BASIC		15.49 BASIC	
C	.160	.210	4.06	5.33
D	.015	.019	0.38	0.48
F	.045	.055	1.14	1.40
G	.100 BASIC		2.54 BASIC	
H	.035	.095	0.89	2.41
J	.008	.012	0.20	0.30
K	.125	.180	3.18	4.57
L	.600 BASIC		15.24 BASIC	
N	.020	.060	0.51	1.52

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.

P Package — 28-Pin Plastic DIP — DAC707JP/KP

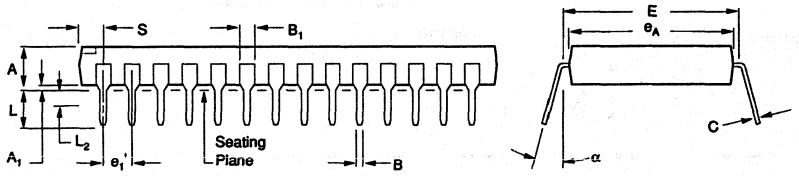


	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A(1)	.169	.200	4.29	5.08
A1(1)	.015	.070	0.38	1.78
B	.015	.020	0.38	0.51
B1	.015	.055	0.38	1.40
C	.008	.012	0.20	0.30
D(1)	1.380	1.455	35.05	36.96
E	.600	.625	15.24	15.88
E1(1)	.485	.550	12.32	13.97
e1	.100 BASIC		2.54 BASIC	
eA	.600 BASIC		15.24 BASIC	

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
L	.100	.200	2.54	5.08
L2	.000	.030	0.00	0.76
α	0°	15°	0°	15°
S(1)	.040	.080	1.02	2.03

(1) Not JEDEC Standard

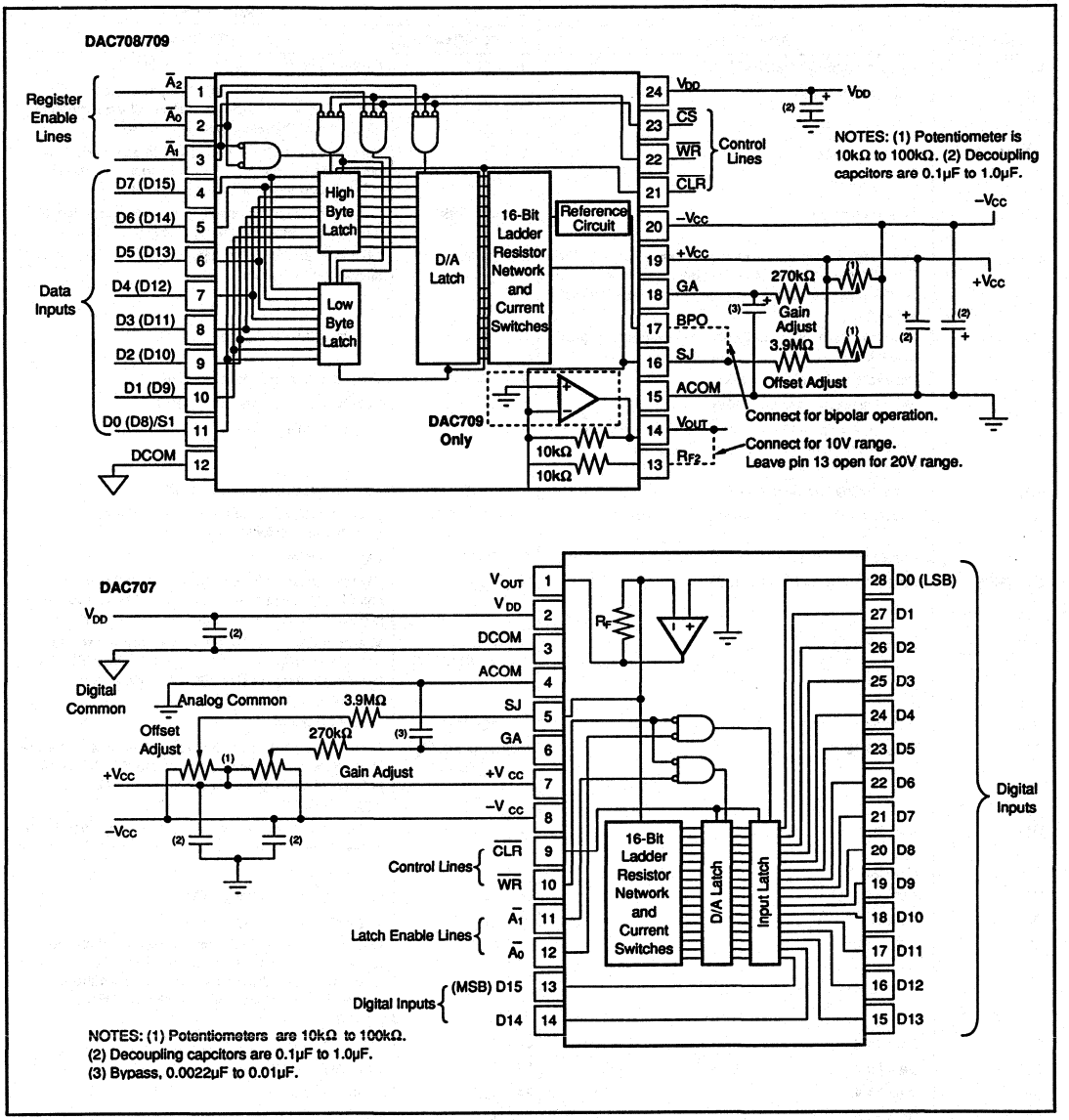
NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.



DESCRIPTION OF PIN FUNCTIONS

DAC707		Pin	DAC708/709	
DESIGNATOR	DESCRIPTION	#	DESIGNATOR	DESCRIPTION
V_{OUT}	Voltage output for DAC707 (±10V)	1	A_2	Latch enable for D/A latch (Active low)
V_{DD}	Logic supply (+5V)	2	A_0	Latch enable for "low byte" input (Active low). When both A_0 and A_1 are logic "0", the serial input mode is selected and the serial input is enabled.
DCOM	Digital common	3	A_1	Latch enable for "high byte" input (Active low). When both A_0 and A_1 are logic "0", the serial input mode is selected and the serial input is enabled.
ACOM	Analog common	4	D7 (D15)	Input for data bit 7 if enabling low byte (LB) latch or data bit 15 if enabling the high byte (HB) latch.
SJ	Summing junction of the internal output op amp for the DAC707. Offset adjust circuit is connected to the summing junction of the output amplifier. Refer to Block Diagram.	5	D6 (D14)	Input for data bit 6 if enabling LB latch or data bit 14 if enabling the HB latch.
GA	Gain adjust pin. Refer to Connection Diagram for gain adjust circuit.	6	D5 (D13)	Data bit 5 (LB) or data bit 13 (HB)
$+V_{CC}$	Positive supply voltage (+15V)	7	D4 (D12)	Data bit 4 (LB) or data bit 12 (HB)
$-V_{CC}$	Negative supply voltage (–15V)	8	D3 (D11)	Data bit 3 (LB) or data bit 11 (HB)
CLR	Clear line. Sets the input latch to zero and sets the D/A latch to the input code that gives bipolar zero on the D/A output (Active low)	9	D2 (D10)	Data bit 2 (LB) or data bit 10 (HB)
WR	Write control line (Active low)	10	D1 (D9)	Data bit 1 (LB) or data bit 9 (HB)
A_1	Enable for D/A converter latch (Active low)	11	D0 (D8)/SI	Data bit 0 (LB) or data bit 8 (HB). Serial input when serial mode is selected.
A_0	Enable for input latch (Active low)	12	DCOM	Digital common
D15 (MSB)	Data bit 15 (Most Significant Bit)	13	R_{F2}	Feedback resistor for internal or external operational amplifier. Connect to pin 14 when a 10V output range is desired. Leave open for a 20V output range.
D14	Data bit 14	14	V_{OUT} R_{F1} (DAC708)	Voltage output for DAC709 or feedback resistor for use with an external output op amp for the DAC708. Refer to Connection Diagram for connection of external op amp to DAC708.
D13	Data bit 13	15	ACOM	Analog common
D12	Data bit 12	16	SJ (DAC709) I_{OUT} (DAC708)	Summing junction of the internal output op amp for the DAC709, or the current output for the DAC708. Refer to Connection Diagram for connection of external op amp to DAC708.
D11	Data bit 11	17	BPO	Bipolar offset. Connect to pin 16 when operating in the bipolar mode. Leave open for unipolar mode.
D10	Data bit 10	18	GA	Gain adjust pin
D9	Data bit 9	19	$+V_{CC}$	Positive supply voltage (+15V)
D8	Data bit 8	20	$-V_{CC}$	Negative supply voltage (–15V)
D7	Data bit 7	21	CLR	Clear line. Sets the high and low byte input registers to zero and, for bipolar operation, sets the D/A register to the input code that gives bipolar zero on the D/A output. (In the unipolar mode, invert the MSB prior to the D/A.)
D6	Data bit 6	22	$\overline{WR}$	Write control line
D5	Data bit 5	23	$\overline{CS}$	Chip select control line
D4	Data bit 4	24	V_{DD}	Logic supply (+5V)
D3	Data bit 3	25	No pin	
D2	Data bit 2	26	No pin	(The DAC708 and DAC709 are in 24-pin packages)
D1	Data bit 1	27	No pin	
D0 (LSB)	Data bit 0 (Least Significant Bit)	28	No pin	

CONNECTION DIAGRAMS



DISCUSSION OF SPECIFICATIONS

DIGITAL INPUT CODES

For bipolar operation, the DAC707/708/709 accept positive-true binary two's complement input code. For unipolar operation (DAC708/709 only) the input code is positive-true straight-binary provided that the MSB input is inverted with an external inverter. See Table I.

Digital Input Codes	ANALOG OUTPUT	
	Unipolar Straight Binary[1] (DAC708/709 only; connected for Unipolar operation)	Binary Two's Complement (Bipolar operation; all models)
$7FFF_H$	+1/2 Full Scale –1LSB[2]	+Full Scale
0000_H	Zero	Zero
$FFFF_H$	+Full Scale	–1LSB
8000_H	+1/2 Full Scale	–Full Scale

NOTES: (1) MSB must be inverted externally. (2) Assumes MSB is inverted externally.

TABLE I. Digital Input Codes.

ACCURACY

Linearity

This specification describes one of the most important measures of performance of a D/A converter. Linearity error is the deviation of the analog output from a straight line drawn through the end points (–Full Scale point and +Full Scale point).

Differential Linearity Error

Differential Linearity Error (DLE) of a D/A converter is the deviation from and ideal 1LSB change in the output when the input changes from one adjacent code to the next. A differential linearity error specification of ±1/2LSB means that the output step size can be between 1/2LSB and 3/2LSB when the input changes between adjacent codes. A negative DLE specification of –1LSB maximum (–0.006% for 14-bit resolution) insures monotonicity.

Monotonicity

Monotonicity assures that the analog output will increase or remain the same for increasing input digital codes. The DAC707/708/709 are specified to be monotonic to 14 bits over the entire specification temperature range.

DRIFT

Gain Drift

Gain Drift is a measure of the change in the full-scale range output over temperature expressed in parts per million per degree centigrade (ppm/°C). Grain drift is established by: (1) testing the end point differences at t_{MIN}, +25°C and t_{MAX}; (2) calculating the gain error with respect to the +25°C value; and (3) dividing by the temperature change.

Zero Drift

Zero Drift is a measure of the change in the output with 0000_H applied to the D/A converter inputs over the specified temperature range. (For the DAC708/709 in unipolar mode, the MSB must be inverted). This code corresponds to zero volts (DAC707 and DAC709) or zero milliamps (DAC708) at the analog output. The maximum change in offset at t_{MIN} or t_{MAX} is referenced to the zero error at +25°C and is divided by the temperature change. This drift is expressed in FSR/°C.

SETTLING TIME

Settling time of the D/A is the total time required for the analog output to settle within an error band around its final value after a change in digital input. Refer to Figure 1 for typical values for this family of products.

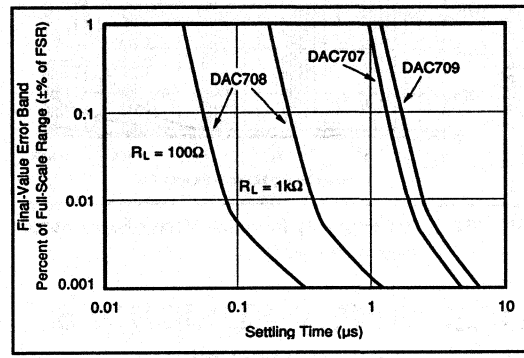


FIGURE 1. Final-Value Error Band Versus Full-Scale Range Settling Time.

Voltage Output

Settling times are specified to ±0.003% of FSR (±1/2LSB for 14 bits) for two input conditions: a full-scale range change of 20V (±10V) or 10V (±5V or 0 to 10V) and a 1LSB change at the "major carry", the point at which the worst-case settling time occurs. (This is the worst-case point since all of the input bits change when going from one code to the next.)

Current Output

Settling times are specified to ±0.003% of FSR for a full-scale range change for two output load conditions: one for 10Ω to 100Ω and one for 1000Ω. It is specified this way because the output RC time constant becomes the dominant factor in determining settling time for large resistive loads.

COMPLIANCE VOLTAGE

Compliance voltage applies only to current output models. It is the maximum voltage swing allowed on the output current pin while still being able to maintain specified accuracy.

POWER SUPPLY SENSITIVITY

Power supply sensitivity is a measure of the effect of a change in a power supply voltage on the D/A converter

output. It is defined as a percent of FSR change in the output per percent of change in either the positive supply ($+V_{CC}$), negative supply ($-V_{CC}$) or logic supply (V_{DD}) about the nominal power supply voltages (see Figure 2). It is specified for DC or low frequency changes. The typical performance curve in Figure 2 shows the effect of high frequency changes in power supply voltages.

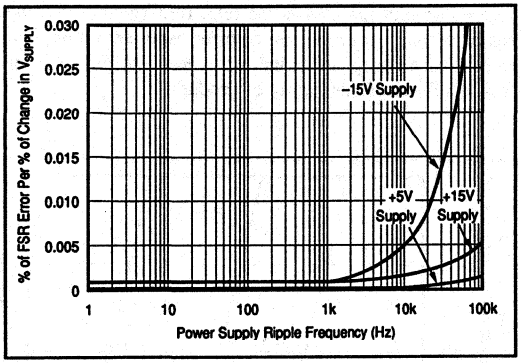


FIGURE 2. Power Supply Rejection Versus Power Supply Ripple Frequency.

OPERATING INSTRUCTIONS

POWER SUPPLY CONNECTIONS

For optimum performance and noise rejection, power supply decoupling capacitors should be added as shown in the Connection Diagram. 1µF tantalum capacitors should be located close to the D/A converter.

EXTERNAL ZERO AND GAIN ADJUSTMENT

Zero and gain may be trimmed by installing external zero and gain potentiometers. Connect these potentiometers as shown in the Connection Diagram and adjust as described below. TCR of the potentiometers should be 100ppm/°C or less. The 3.9MΩ and 270kΩ resistors (±20% carbon or better) should be located close to the D/A converter to prevent noise pickup. If it is not convenient to use these high-value resistors, an equivalent "T" network, as shown in Figure 3, may be substituted in place of the 3.9MΩ resistor. A 0.001µF to 0.01µF ceramic capacitor should be connected from GAIN ADJUST to ANALOG COMMON to prevent noise pickup. Refer to Figures 4 and 5 for the relationship of zero and gain adjustments to unipolar D/A converters.

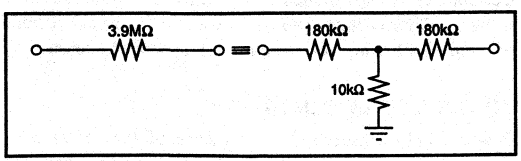


FIGURE 3. Equivalent Resistances.

Zero Adjustment

For unipolar (USB) configurations, apply the digital input code that produces zero voltage or zero current output and adjust the zero potentiometer for zero output.

For bipolar (BTC) configurations, apply the digital input code that produces zero output voltage or current. See Table II for corresponding codes and connection diagrams for zero adjustments circuit connections. Zero calibration should be made before gain calibration.

Gain Adjustment

Apply the digital input that gives the maximum positive output voltage. Adjust the gain potentiometer for this positive full-scale voltage. See Table II for positive full-scale voltages and the Connection Diagrams for gain adjustment circuit connections.

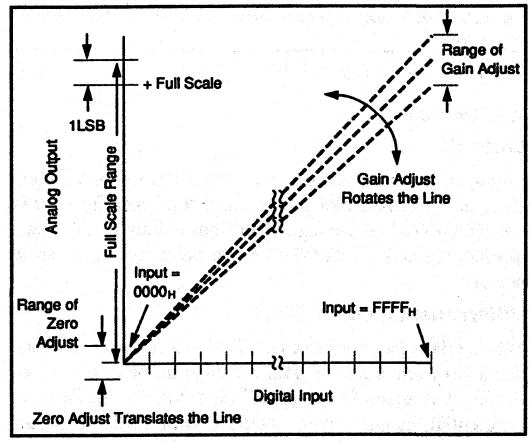


FIGURE 4. Relationship of Zero and Gain Adjustments for Unipolar D/A Converters, DAC708 and DAC709.

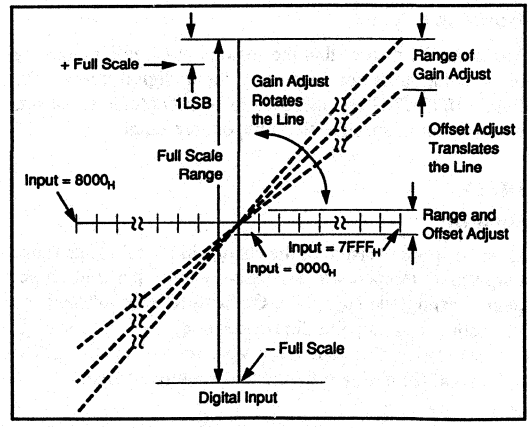


FIGURE 5. Relationship of Zero and Gain Adjustments for Bipolar D/A Converters, DAC707 and DAC708/709

VOLTAGE OUTPUT MODELS												
Digital Input Code	Analog Output Unipolar, 0 to +10V[1]			Units	Digital Input Code	Analog Output Bipolar, ±10V			Analog Output Bipolar, ±5V			Units
	16-Bit	15-Bit	14-Bit			16-Bit	15-Bit	14-Bit	16-Bit	15-Bit	14-Bit	
One LSB	153	305	610	µV	One LSB	305	610	1224	153	305	610	µV
$FFFF_H$	+9.99985	+9.99969	+9.99939	V	7FFFH	+9.99960	+9.99939	+9.99878	+4.99980	+4.99970	+4.99939	V
0000_H	0	0	0	V	8000H	–10.0000	–10.0000	–10.0000	–5.0000	–5.0000	–5.0000	V

CURRENT OUTPUT MODELS									
Digital Input Code	Analog Output Unipolar, 0 to –2mA[1]			Units	Digital Input Code	Analog Output Bipolar, ±1mA			Units
	16-Bit	15-Bit	14-Bit			16-Bit	15-Bit	14-Bit	
One LSB	0.031	0.061	0.122	µA	One LSB	0.031	0.061	0.122	µA
$FFFF_H$	–1.99997	–1.99994	–1.99988	mA	$7FFF_H$	–0.99997	–0.99994	–0.99988	mA
0000_H	0	0	0	mA	8000_H	+1.00000	+1.00000	+1.00000	mA

NOTE: (1) MSB assumed to be inverted externally.

TABLE II. Digital Input and Analog Output Voltage/Current Relationships.

INTERFACE LOGIC AND TIMING

DAC708/709

The signals CHIP SELECT ($\overline{CS}$), WRITE ($\overline{WR}$), register enables ($\overline{A}_0$, $\overline{A}_1$, and $\overline{A}_2$) and CLEAR ($\overline{CLR}$), provide the control functions for the microprocessor interface. They are all active in the "low" or logic "0" state. $\overline{CS}$ must be low to access any of the registers. $\overline{A}_0$ and $\overline{A}_1$ steer the input 8-bit data byte to the low- or high-byte input latch respectively. $\overline{A}_2$ gates the contents of the two input latches through to the D/A latch in parallel. The contents are then applied to the input of the D/A converter. When $\overline{WR}$ goes low, data is strobed into the latch or latches which have been enabled.

The serial input mode is activated when both $\overline{A}_0$ and $\overline{A}_1$ are logic "0" simultaneously. The D0 (D8)/SI input data line accepts the serial data MSB first. Each bit is clocked in by a $\overline{WR}$ pulse. Data is strobed through to the D/A latch by $\overline{A}_2$ going to logic "0" the same as in the parallel input mode.

Each of the latches can be made "transparent" by maintaining its enable signal at logic "0". However, as stated above, when both $\overline{A}_0$ and $\overline{A}_1$ are logic "0" at the same time, the serial mode is selected.

The $\overline{CLR}$ line resets both input latches to all zeros and sets the D/A latch to 0000_H. This is the binary code that gives a null, or zero, at the output of the D/A in the bipolar mode. In the unipolar mode, activating $\overline{CLR}$ will cause the output to go to one-half of full scale.

The maximum clock rate of the latches is 10MHz. The minimum time between write ($\overline{WR}$) pulses for successive enables is 20ns. In the serial input mode (DAC708 and DAC709), the maximum rate at which data can be clocked into the input shift register is 10MHz.

The timing of the control signals is given in Figure 6.

DAC707

The DAC707 interface timing is the same as that described above except instead of two 8-bit separately-enabled input latches, it has a single 16-bit input latch enabled by $\overline{A}_0$. The

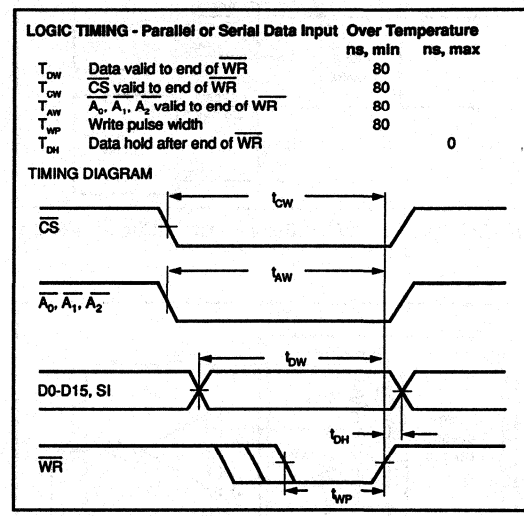


FIGURE 6. Logic Timing Diagram.

D/A latch is enabled by $\overline{A}_1$. Also, there is no serial-input mode and no CHIP SELECT ($\overline{CS}$) line.

INSTALLATION CONSIDERATIONS

Due to the extremely-high accuracy of the D/A converter, system design problems such as grounding and contact resistance become very important. For a 16-bit converter with a +10V full-scale range, 1LSB is 153µV. With a load current of 5mA, series wiring and connector resistance of only 30mΩ will cause the output to be in error by 1LSB. To understand what this means in terms of a system layout, the resistance of typical 1 ounce copper-clad printed circuit board material is approximately 1/2mΩ per square. In the example above, a 10 milliinch-wide conductor 60 milliinches long would cause a 1LSB error.

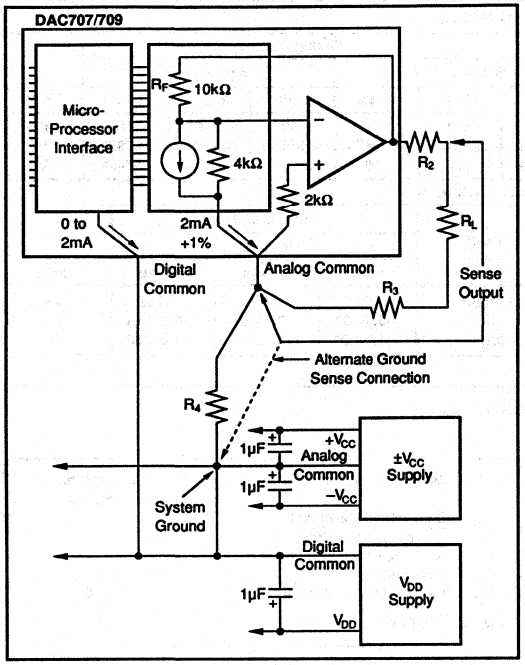


FIGURE 7. DAC707/709 Bipolar Output Circuit (Voltage Out).

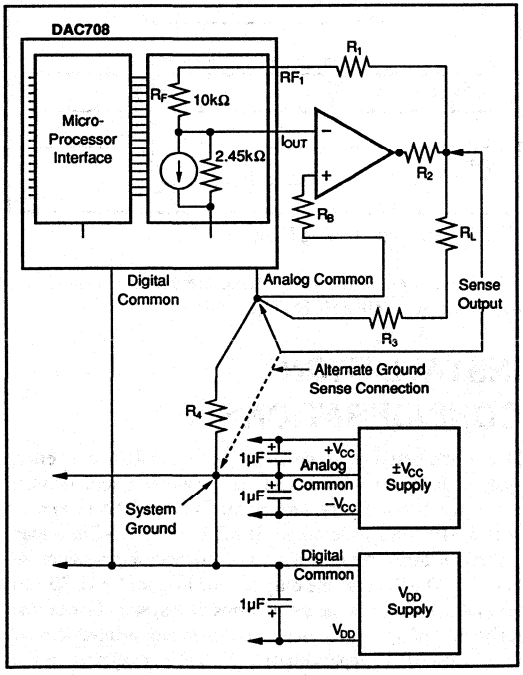


FIGURE 8. DAC708 Bipolar Output Circuit (with External Op Amp).

In Figures 7 and 8, lead and contact resistances are represented by R_1 through R_5. As long as the load resistance R_L is constant, R_2 simply introduces a gain error and can be removed with gain calibration. R_3 is part of R_L if the output voltage is sensed at ANALOG COMMON.

Figures 8 and 9 show two methods of connecting the current output model with an external precision output op amp. By sensing the output voltage at the load resistor (connecting R_F to the output of the amplifier at R_L) the effect of R_1 and R_2 is greatly reduced. R_1 will cause a gain error but is independent of the value of R_L and can be eliminated by initial calibration adjustments. The effect of R_2 is negligible because it is inside the feedback loop of the output op amp and is therefore greatly reduced by the loop gain.

In many applications it is impractical to sense the output voltage at ANALOG COMMON. Sensing the output voltage at the system ground point is permissible because these converters have separate analog and digital common lines and the analog return current is a near-constant 2mA and varies by only 10µA to 20µA over the entire input code range. R_4 can be as large as 3Ω without adversely affecting the linearity of the D/A converter. The voltage drop across R_4 is constant and appears as a zero error that can be nulled with the zero calibration adjustment.

Another approach senses the output at the load as shown in Figure 9. In this circuit the output voltage is sensed at the load common and not at the D/A converter common as in the previous circuits. The value of R_6 and R_7 must be adjusted for maximum common-mode rejection across R_L. The effect of R_4 is negligible as explained previously.

The D/A converter and the wiring to its connectors should be located to provide optimum isolation from sources of RFI and EMI. The key to elimination of RF radiation or pickup is small loop area. Signal leads and their return conductors should be kept close together such that they present a small flux-capture cross section for any external field.

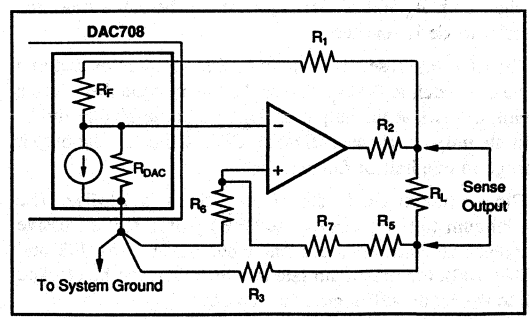


FIGURE 9. Alternate Connection for Ground Sensing at the Load (Current Output Models).

BURN-IN SCREENING

Burn-in screening is an option available for the entire DAC707 through DAC709 family of products. Burn-in duration is 160 hours at the temperature shown below (or equivalent combination of time and temperature).

Model	Temp. Range	Burn-In Screening
DAC709KH-BI	0°C to +70°C	160 hours at 85°C
DAC709BH-BI	–25°C to +85°C	160 hours at 85°C
DAC709SH-BI	–55°C to +125°C	160 hours at 125°C

All units are tested after burn-in to ensure that grade specifications are met. To order burn-in, add "–BI" to the base model.

ENVIRONMENTAL SCREENING

/QM Screening

All BH and SH models are available with Burr-Brown's /QM environmental screening for enhanced reliability. The screening, tabulated below, is performed to selected methods of MIL-STD-883. References to these methods provides a convenient method of communicating the screening levels and basic procedures employed; it does not imply conformance to any other military standards or to any methods of MIL-STD-883 other than those specified below. Burr-Brown's detailed procedures may vary slightly, model-to-model, from those in MIL-STD-883.

SCREENING FLOW FOR /QM MODELS

SCREEN	MIL-STD-883 METHOD	CONDITION	COMMENTS
Internal Visual	BBC Standard		QC4118
High Temperature Storage (Stabilization Bake)	1008	C	+150°C, 24hrs
Temperature Cycling	1010	C	–65 to +150°C, 10 cycles
Burn-in	1015	B	+125°C, 160hrs
Constant Acceleration	2001		
28-pin pkg.		B	10,000G
24-pin pkg.		E	30,000G
Hermeticity			
Fine Leak	1014	A1 or A2	
28-pin pkg.			2 x 10–7 atmcc/sec
24-pin pkg.			5 x 10–8 atmcc/sec
Gross Leak	1014	C	60psig, 2hr
External Visual	BBC Standard		QC5150

APPLICATIONS

LOADING THE DAC709 SERIALLY ACROSS AN ISOLATION BARRIER

A very useful application of the DAC709 is in achieving low-cost isolation that preserves high accuracy. Using the serial input feature of the input register pair, only three signal lines need to be isolated. The data is applied to pin 11 in a serial bit stream, MSB first. The $\overline{WR}$ input is used as a data strobe, clocking in each data bit. A RESET signal is provided for system startup and reset. These three signals are each optically isolated. Once the 16 bits of serial data have been strobed into the input register pair, the data is strobed through to the D/A register by the "carry" signal out of a 4-bit binary synchronous counter that has counted the 16 $\overline{WR}$ pulses used to clock in the data. The circuit diagram is given in Figure 10.

CONNECTING MULTIPLE DAC707s TO A 16-BIT MICROPROCESSOR BUS

Figure 11 illustrates the method of connecting multiple DAC707s to a 16-bit microprocessor bus. The circuit shown has two DAC707s and uses only one address line to select either the input register or the D/A register. An external address decoder selects the desired converter.

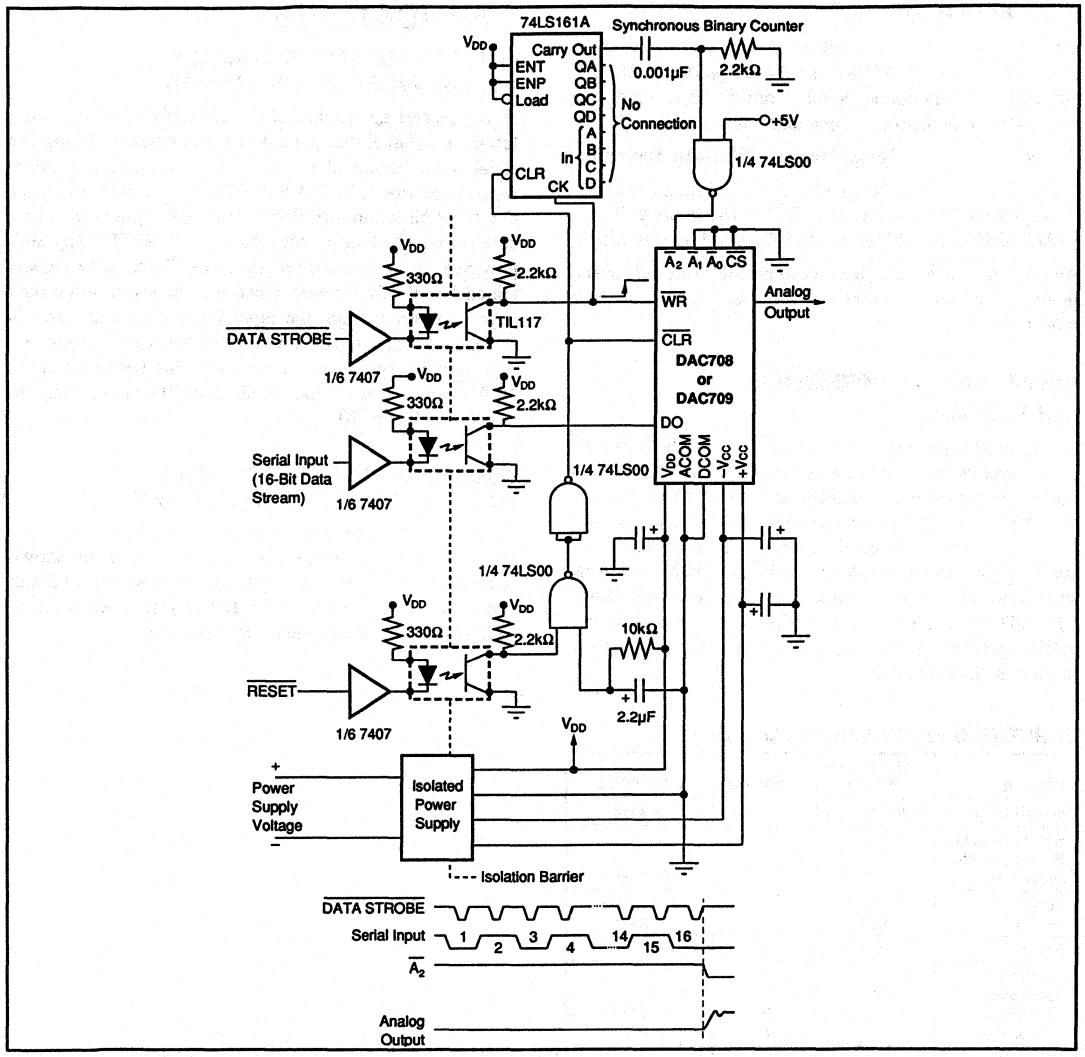


FIGURE 10. Serial Loading of Electrically Isolated DAC708/709.

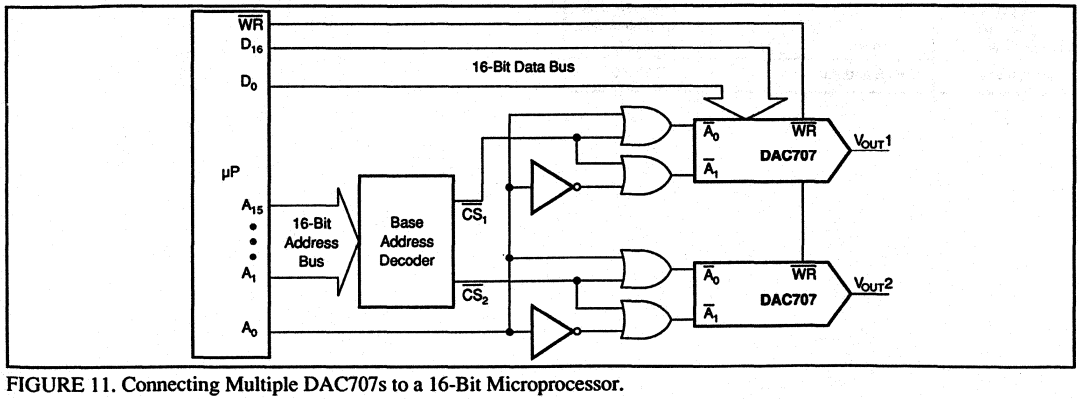


FIGURE 11. Connecting Multiple DAC707s to a 16-Bit Microprocessor.

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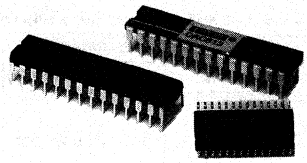


DAC813

Microprocessor-Compatible 12-BIT DIGITAL-TO-ANALOG CONVERTER

FEATURES

- ±1/2LSB NONLINEARITY OVER TEMPERATURE
- GUARANTEED MONOTONIC OVER TEMPERATURE
- LOW POWER: 270mW typ
- DIGITAL INTERFACE DOUBLE BUFFERED: 12 AND 8 + 4 BITS
- SPECIFIED AT ±12V AND ±15V POWER SUPPLIES
- RESET FUNCTION TO BIPOLAR ZERO
- 0.3" WIDE DIP AND SO PACKAGES

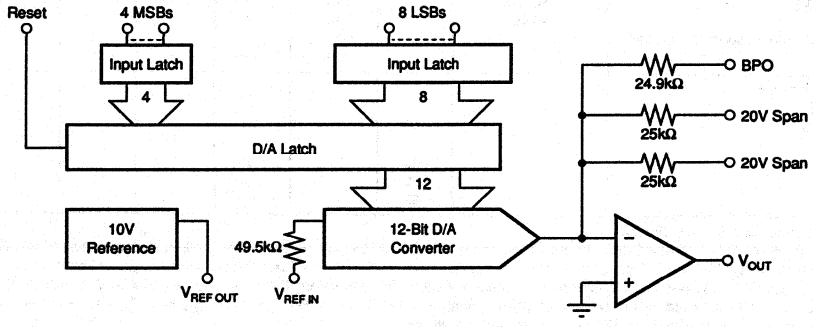
DESCRIPTION

The DAC813 is a complete monolithic 12-bit digital-to-analog converter with a flexible digital interface. It includes a precision +10V reference, interface control logic, double-buffered latch and a 12-bit D/A converter with voltage output operational amplifier. Fast current switches and laser-trimmed thin-film resistors provide a highly accurate, fast D/A converter.

Digital interfacing is facilitated by a double buffered latch. The input latch consists of one 8-bit byte and one 4-bit nibble to allow interfacing to 8-bit (right justified format) or 16-bit data buses. Input gating logic is designed so that the last nibble or byte to be loaded can be loaded simultaneously with the transfer of data to the D/A latch saving computer instructions.

A reset control allows the DAC813 D/A latch to asynchronously reset the D/A output to bipolar zero, a feature useful for power-up reset, recalibration, or for system re-initialization upon system failure.

The DAC813 is specified to ±1/2LSB maximum linearity error (J, A grades) and ±1/4LSB (K, B grades). It is packaged in a 28-pin 0.3" wide ceramic DIP (-40°C to +85°C specification temperature range), 28-pin 0.3" wide plastic DIP and 28-lead plastic SO (0°C to +70°C).



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Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL

T_A = +25°C, $\pm V_{CC}$ = ±12V or ±15V and load on V_{OUT} = 5kΩ || 500µF to common unless otherwise noted.

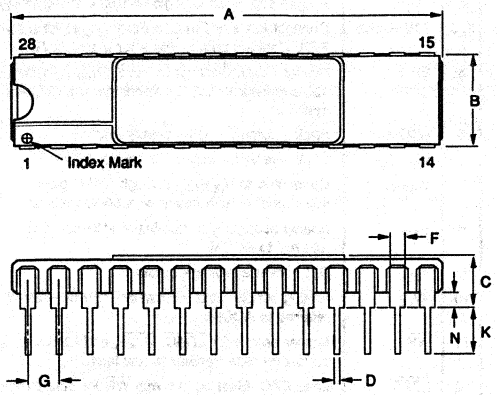
PARAMETER	CONDITIONS	DAC813AH, JP, JU, AU, D			DAC813BH, KP, KU			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
DIGITAL INPUTS								
Resolution				12			*	Bits
Codes[1]			USB, BOB			*		
Digital Inputs Over Temperature Range[2]								
V_{IH}		+2		+5.5	*		*	VDC
V_{IL}		0		+0.8	*		*	VDC
DATA Bits, $\overline{WR}$, $\overline{Reset}$, $\overline{LDAC}$, $\overline{LMSB}$, $\overline{LLSB}$				±10			*	µA
I_{IH}	V_{IN} = +2.7V			±10			*	µA
I_{IL}	V_{IN} = +0.4V							
ACCURACY								
Linearity Error			±1/4	±1/2		±1/8	±1/4	LSB
Differential Linearity Error			±1/2	±3/4		±1/4	±1/2	LSB
Gain Error[3]			±0.05	±0.2		*	*	%
Unipolar Offset Error[4]			±0.01	±0.02		*	*	% of FSR[6]
Bipolar Zero Error[5]			±0.02	±0.2		*	*	% of FSR
Monotonicity			Guaranteed			*		
Power Supply Sensitivity: $+V_{CC}$	20V Range		5	10		*	*	ppm of FSR/%
$-V_{CC}$			1	10		*	*	ppm of FSR/%
DRIFT	Over Specification							
Gain	Temperature Range		±5	±30		*	±15	ppm/°C
Unipolar Offset			±1	±3		*	±3	ppm of FSR/°C
Bipolar Zero			±3	±10		*	±5	ppm of FSR/°C
Linearity Error Over Temperature Range			±1/2	±3/4		±1/4	±1/2	LSB
Monotonicity Over Temperature Range			Guaranteed			*		
SETTLING TIME[7] (To Within ±0.01% of FSR of Final Value; 5kΩ || 500pF load)								
For Full Scale Range Change	20V Range		4.5	6		*	*	µs
	10V Range		3.3	5		*	*	µs
For 1LSB Change at Major Carry[8]			2			*		µs
Slew Rate			10			*		V/µs
ANALOG OUTPUT								
Voltage Range: Unipolar	$\pm V_{CC}$ > ±11.4V		0 to +10			*		V
Bipolar	$\pm V_{CC}$ > ±11.4V		±5, ±10			*		V
Output Current		±5			*			mA
Output Impedance	At DC		0.2			*		Ω
Short Circuit to Common Duration			Indefinite			*		mA
REFERENCE VOLTAGE								
Voltage		+9.95	+10	+10.05	*	*	*	V
Source Current Available for External Loads		5			*			mA
Impedance			2			*		Ω
Temperature Coefficient			±5	±25		*	*	ppm/°C
Short Circuit to Common Duration			Indefinite			*		mA
POWER SUPPLY REQUIREMENTS								
Voltage: $+V_{CC}$		+11.4	+15	+16.5	*	*	*	VDC
$-V_{CC}$		−11.4	−15	−16.5	*	*	*	VDC
Current: $+V_{CC}$ + V_L	No Load		13	15		*	*	mA
$-V_{CC}$	No Load		−5	−7		*	*	mA
Potential at DCOM with Respect to ACOM[9]		−3		+3	*		*	V
Power Dissipation			270	330		*	*	mW
TEMPERATURE RANGE								
Specification: J, K		0		+70	*		*	°C
A, B		−40		+85	*		*	°C
Operating: J. K		−40		+85	*		*	°C
A, B		−55		+125	*		*	°C
Storage: J, K		−60		+100	*		*	°C
A, B		−65		+150	*		*	°C

*Same as specification for DAC813AH, JP, JU.

NOTES: (1) USB = Unipolar Straight Binary; BOB = Bipolar Offset Binary. (2) TTL and 5V CMOS compatible. (3) Specified with 500Ω Pin 6 to 7. Adjustable to zero with external trim potentiometer. (4) Error at input code 000_{HEX} for unipolar mode, FSR = 10V. (5) Error at input code 800_{HEX} for bipolar range. Specified with 100Ω Pin 6 to 4 and with 500Ω pin 6 to 7. See page 9 for zero adjustment procedure. (6) FSR means Full Scale Range and is 20V for the ±10V range. (7) Maximum represents the 3σ limit. Not 100% tested for this parameter. (8) At the major carry, $7FF_{HEX}$ to 800_{HEX} and 800_{HEX} to $7FF_{HEX}$. (9) The maximum voltage at which ACOM and DCOM may be separated without affecting accuracy specifications.

MECHANICAL

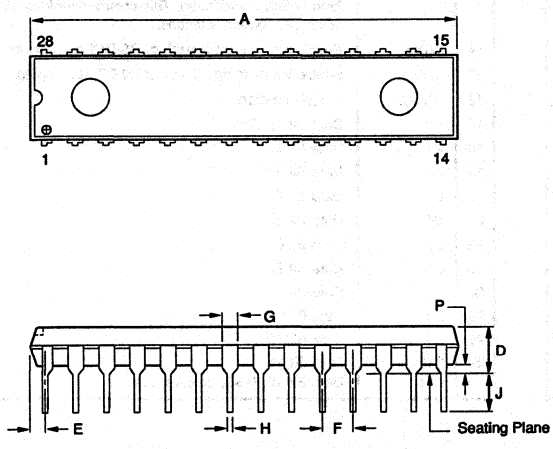
H Package — 0.3" 28-Pin Hermetic DIP



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.388	1.412	35.26	35.86
B	.300	.320	7.62	8.13
C	—	.160	—	4.06
D	.016	.020	0.41	0.51
F	.050 BASIC		1.27 BASIC	
G	.095	.105	2.41	2.67
J	.009	.012	0.23	0.30
K	.125	.180	3.18	4.57
L	.290	.310	7.37	7.87
N	.040	.060	1.02	1.52

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package. Metal lid connected to $-V_{CC}$.

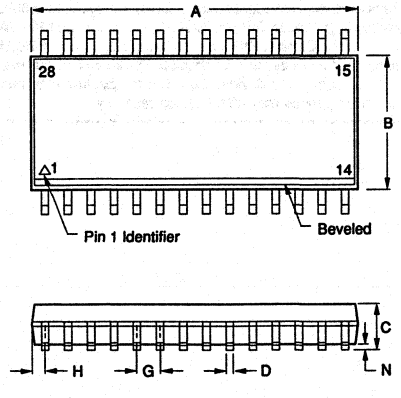
P Package — 0.3" 28-Pin Plastic DIP



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.255	1.355	31.88	34.42
B	.270	.290	6.86	7.37
D	.150	.170	3.81	4.32
E	.010	.080	0.25	2.03
F	.100 BASIC		2.54 BASIC	
G	.045	.055	1.14	1.40
H	.016	.020	0.41	0.51
J	.125	N/A	3.18	N/A
K	.300 BASIC		7.62 BASIC	
M	0°	15°	0°	15°
N	.008	.015	0.20	0.38
P	.020	.040	0.51	1.02

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.

U Package — 28-Pin Plastic SOIC



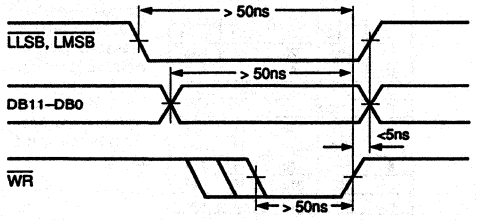
DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.700	.716	17.78	18.19
B	.286	.302	7.26	7.67
C	.093	.109	2.36	2.77
D	.016 BASIC		0.41 BASIC	
G	.050 BASIC		1.27 BASIC	
H	.022	.038	0.56	0.97
J	.008	.012	0.20	0.30
L	.398	.414	10.11	10.52
M	5° TYP		5° TYP	
N	.000	.012	0.00	0.30

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.

MINIMUM TIMING DIAGRAMS

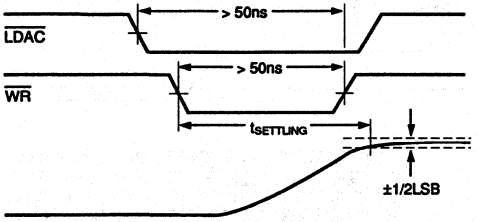
WRITE CYCLE #1

(Load first rank from Data Bus: $\overline{LDAC}$ = 1)



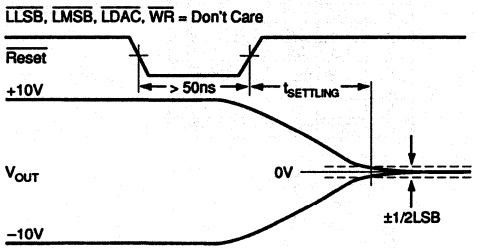
WRITE CYCLE #2

(Load second rank from first rank: $\overline{LLSB}$, $\overline{LMSB}$ = 1)



RESET COMMAND (Bipolar Mode)

$\overline{LLSB}$, $\overline{LMSB}$, $\overline{LDAC}$, $\overline{WR}$ = Don't Care



PIN DESCRIPTIONS

PIN	NAME	DESCRIPTION
1	$+V_L$	Positive supply pin for logic circuits. Connect to $+V_{CC}$.
2, 3	20V Range	Connect Pin 2 or Pin 3 to Pin 9 (V_{OUT}) for a 20V FSR. Connect both to Pin 9 for a 10V FSR.
4	BPO	Bipolar offset. Connect to Pin 6 ($V_{REF\ OUT}$) through 100Ω resistor or 200Ω potentiometer for bipolar operation.
5	ACOM	Analog common, $\pm V_{CC}$ supply return.
6	$V_{REF\ OUT}$	+10V reference output referred to ACOM.
7	$V_{REF\ IN}$	Connected to $V_{REF\ OUT}$ through a 1kΩ gain adjustment potentiometer or a 500Ω resistor.
8	$+V_{CC}$	Analog supply input, nominally +12V to +15V referred to ACOM.
9	V_{OUT}	D/A converter voltage output.
10	$-V_{CC}$	Analog supply input, nominally –12V or –15V referred to ACOM.
11	$\overline{WR}$	Master enable for $\overline{LDAC}$, $\overline{LLSB}$, and $\overline{LMSB}$. Must be low for data transfer to any latch.
12	$\overline{LDAC}$	Load DAC. Must be low with $\overline{WR}$ for data transfer to the D/A latch and simultaneous update of the D/A converter.
13	$\overline{Reset}$	When low, resets the D/A latch such that a Bipolar Zero output is produced. This control overrides all other data input operations.
14	$\overline{LMSB}$	Enable for 4-bit input latch of D8-D11 data inputs.
15	$\overline{LLSB}$	Enable for 8-bit input latch of D0-D7 data inputs.
16	DCOM	Digital common.
17	D0	Data Bit 1, LSB.
18	D1	Data Bit 2.
19	D2	Data Bit 3.
20	D3	Data Bit 4.
21	D4	Data Bit 5.
22	D5	Data Bit 6.
23	D6	Data Bit 7.
24	D7	Data Bit 8.
25	D8	Data Bit 9.
26	D9	Data Bit 10.
27	D10	Data Bit 11.
28	D11	Data Bit 12, MSB, positive true.

ABSOLUTE MAXIMUM RATINGS

$+V_{CC}$ to ACOM	0 to +18V
$-V_{CC}$ to ACOM	0 to –18V
$+V_{CC}$ to $-V_{CC}$	0 to +36V
DCOM with respect to ACOM	±4V
Digital Inputs (Pins 11–15, 17–28) to DCOM	–0.5V to $+V_{CC}$
External Voltage Applied to BPO Span Resistor	$\pm V_{CC}$
$V_{REF\ OUT}$	Indefinite Short to ACOM
V_{OUT}	Indefinite Short to ACOM

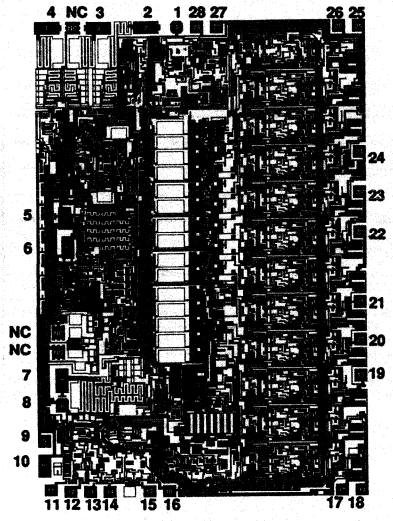
Power Dissipation	750mW
Lead Temperature (soldering, 10s)	+300°C
Max Junction Temperature	+165°C
Thermal Resistance, $\theta_{J\text{-}A}$: Plastic DIP and SOIC	130°C/W
Ceramic DIP	85°C/W

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE	LINEARITY ERROR, MAX AT +25°C	GAIN DRIFT (ppm/°C)
DAC813AU	Plastic SOIC	–40°C to +85°C	±1/2LSB	±30
DAC813JP	Plastic DIP	0°C to +70°C	±1/2LSB	±30
DAC813JU	Plastic SOIC	0°C to +70°C	±1/2LSB	±30
DAC813KP	Plastic DIP	0°C to +70°C	±1/4LSB	±15
DAC813KU	Plastic SOIC	0°C to +70°C	±1/4LSB	±15
DAC813AH	Ceramic DIP	–40°C to +85°C	±1/2LSB	±30
DAC813BH	Ceramic DIP	–40°C to +85°C	±1/4LSB	±15
DAC813D	25 Die/Pack	0°C to +70°C	±1/2LSB	±30

DICE INFORMATION



DAC813 DIE TOPOGRAPHY

PAD	FUNCTION	PAD	FUNCTION
1	$+V_L$	15	$\overline{LLSB}$
2	20V Range	16	DCOM
3	20V Range	17	DB0 (LSB)
4	BPO	18	DB1
5	ACOM	19	DB2
6	$V_{REF\ OUT}$	20	DB3
7	$V_{REF\ IN}$	21	DB4
8	$+V_{CC}$	22	DB5
9	V_{OUT}	23	DB6
10	$-V_{CC}$	24	DB7
11	$\overline{WR}$	25	DB8
12	$\overline{LDAC}$	26	DB9
13	$\overline{Reset}$	27	DB10
14	$\overline{LMSB}$		

Substrate Bias: $-V_{CC}$
NC: No Connection.

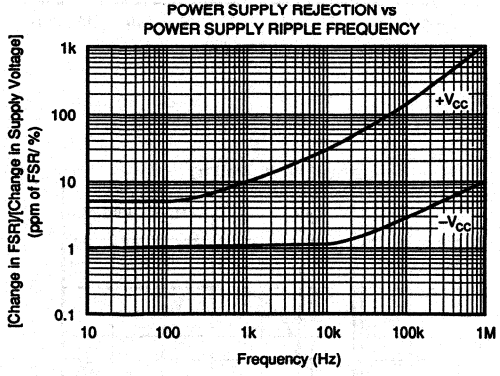
MECHANICAL INFORMATION

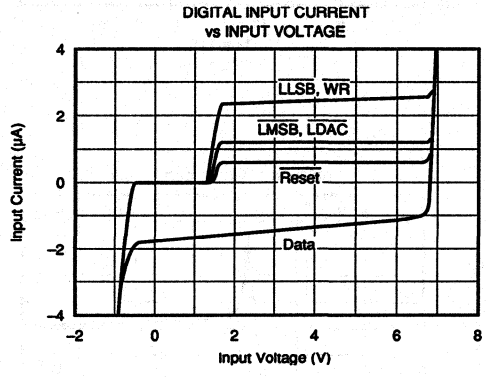
	MILS (0.001")	MILLIMETERS
Die Size	204 x 140 ±5	5.18 x 3.56 ±0.13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.10 x 0.10
Metalization	Aluminum	

See "DICE PRODUCTS" Section 17 in Data Book Supplement Volume 33c, or contact Burr-Brown for current information.

TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_{CC} = ±15V unless otherwise noted.





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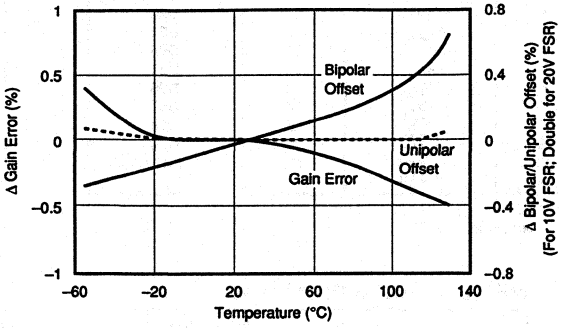
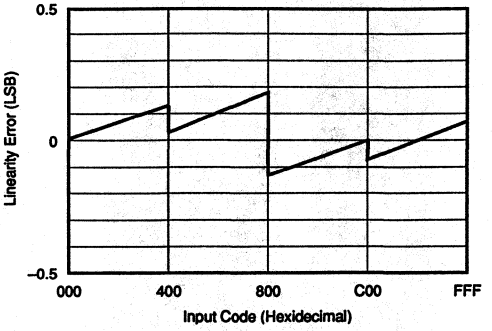
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_{CC} = ±15V unless otherwise noted.

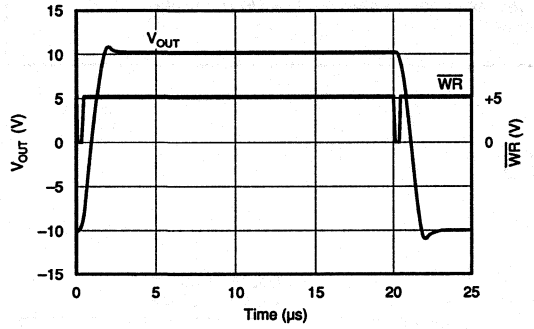
CHANGE OF GAIN AND OFFSET ERROR vs TEMPERATURE



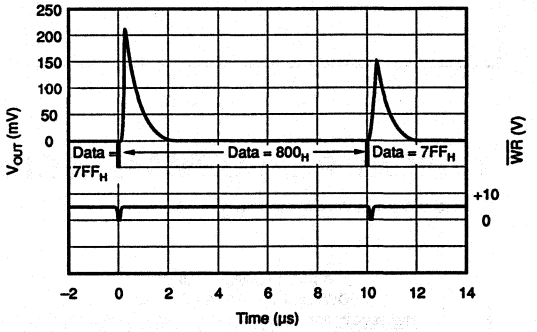
INTEGRAL LINEARITY ERROR



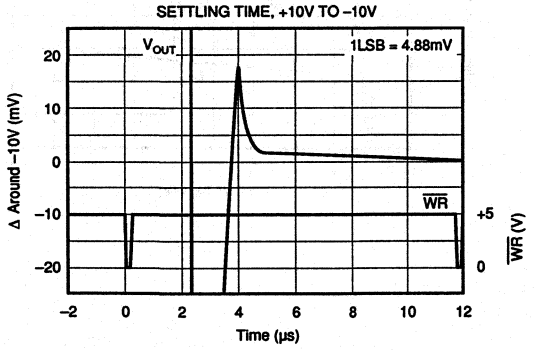
± FULL SCALE OUTPUT SWING



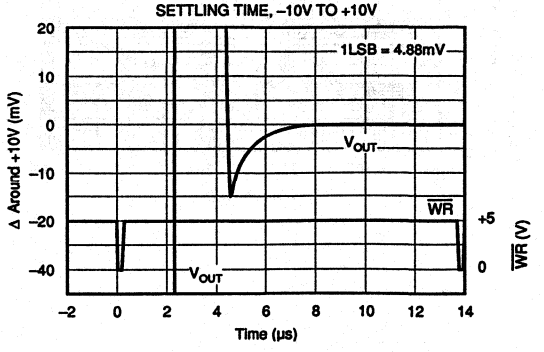
MAJOR CARRY GLITCH



SETTLING TIME, +10V TO −10V



SETTLING TIME, −10V TO +10V



ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

DISCUSSION OF SPECIFICATIONS

INPUT CODES

The DAC813 accepts positive-true binary input codes. DAC813 may be connected by the user for any one of the following codes: USB (Unipolar Straight Binary), BOB (Bipolar Offset Binary) or, using an external inverter on the MSB line, BTC (Binary Two's Complement). See Table I.

DIGITAL INPUT	ANALOG OUTPUT		
MSB to LSB	USB Unipolar Straight Binary	BOB Bipolar Offset Binary	BTC* Binary Two's Complement
FFF_{HEX}	+ Full Scale	+ Full Scale	Zero – 1LSB
800_{HEX}	+ 1/2 Full Scale	Zero	– Full Scale
$7FF_{HEX}$	+ 1/2 Full Scale – 1LSB	Zero – 1LSB	+ Full Scale
000_{HEX}	Zero	– Full Scale	Zero
* Invert MSB of BOB code with external inverter to obtain BTC code.			

TABLE I. Digital Input Codes.

LINEARITY ERROR

Linearity error as used in D/A converter specifications by Burr-Brown is the deviation of the analog output from a straight line drawn between the end points (inputs all "1s" and all "0s"). The DAC813 linearity error is specified at ±1/4LSB (max) at +25°C for B and K grades, and ±1/2LSB (max) for A and J grades.

DIFFERENTIAL LINEARITY ERROR

Differential linearity error (DLE) is the deviation from a 1LSB output change from one adjacent state to the next. A DLE specification of 1/2LSB means that the output step size can range from 1/2LSB to 3/2LSB when the input changes from one state to the next. Monotonicity requires that DLE be less than 1LSB over the temperature range of interest.

MONOTONICITY

A D/A converter is monotonic if the output either increases or remains the same for increasing digital inputs. All grades of DAC813 are monotonic over their specification temperature range.

DRIFT

Gain Drift is a measure of the change in the Full Scale Range (FSR) output over the specification temperature range. Gain Drift is expressed in parts per million per degree Celsius (ppm/°C).

Unipolar Offset Drift is measured with a data input of 000_{HEX}. The D/A is configured for unipolar output. Unipolar Offset Drift is expressed in parts per million of Full Scale Range per degree Celsius (ppm of FSR/°C).

Bipolar Zero Drift is measured with a data input of 800_{HEX}. The D/A is configured for bipolar output. Bipolar Zero Drift is expressed in parts per million of Full Scale Range per degree Celsius (ppm of FSR/°C).

SETTLING TIME

Settling Time is the total time (including slew time) for the output to settle within an error band around its final value after a change in input. Three settling times are specified to ±0.012% of Full Scale Range (FSR): two for maximum full scale range changes of 20V and 10V, and one for a 1LSB change. The 1LSB change is measured at the major carry ($7FF_{HEX}$ to 800_{HEX} and 800_{HEX} to $7FF_{HEX}$), the input transition at which worst-case settling time occurs.

REFERENCE SUPPLY

DAC813 contains an on-chip +10V reference. This voltage (pin 6) has a tolerance of ±50mV. $V_{REF\ OUT}$ must be connected to $V_{REF\ IN}$ through a gain adjust resistor with a nominal value of 500Ω. The connection can be made through an optional 1kΩ trim resistor to provide adjustment to zero gain error. The reference output may be used to drive external loads, sourcing at least 5mA. This current should be constant, otherwise the gain of the converter will vary.

POWER SUPPLY SENSITIVITY

Power supply sensitivity is a measure of the effect of a power supply change on the D/A converter output. It is defined as a ppm of FSR output change per percent of change in either $+V_{CC}$ or $-V_{CC}$ about the nominal voltages expressed in ppm of FSR/%. The first performance curve on page 5 shows typical power supply rejection versus power supply ripple frequency.

OPERATION

DAC813 is a complete single IC chip 12-bit D/A converter. The chip contains a 12-bit D/A converter, voltage reference, output amplifier, and microcomputer-compatible input logic as shown in Figure 1.

INTERFACE LOGIC

Input latches hold data temporarily while a complete 12-bit word is assembled before loading into the D/A latch. This double-buffered organization prevents the generation of spurious analog output values. Each latch is independently addressable.

All latches are level-triggered. Data present when the control signals are logic "0" will enter the latch. When any one of the control signals returns to logic "1", the data is latched. A truth table for the control signals is presented in Table II.

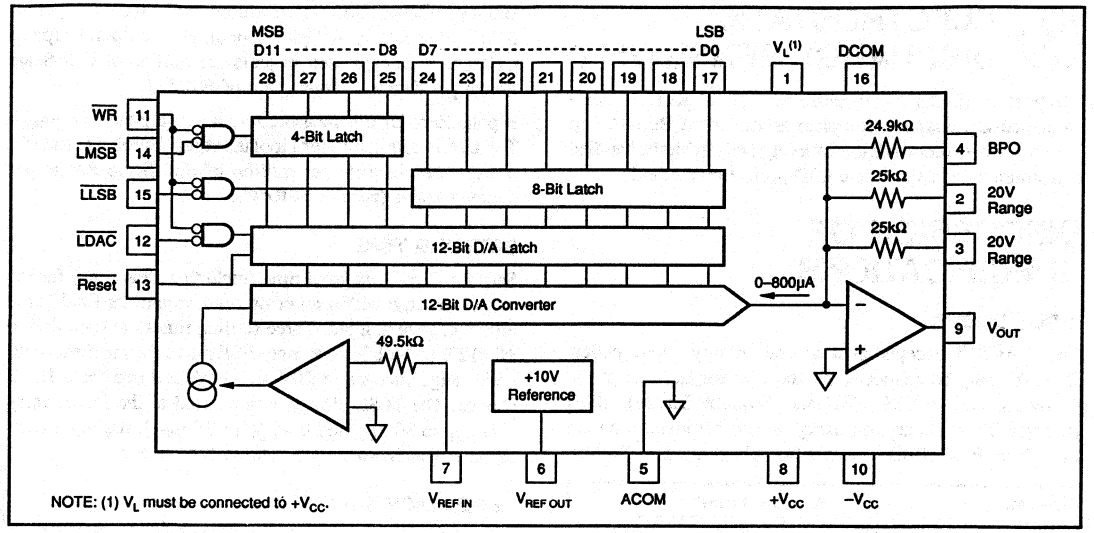


FIGURE 1. DAC813 Block Diagram.

WR	LLSB	LMSB	LDAC	RESET	OPERATION
1	X	X	X	1	No operation
X	X	X	X	0	D/A latch set to 800_{HEX}
0	1	0	1	1	Enables 4 MSBs input latch
0	0	1	1	1	Enables 8 LSBs input latch
0	1	1	0	1	Loads D/A latch from input latches
0	0	0	0	1	Makes all latches transparent
"X" = Don't Care					

TABLE II. DAC813 Interface Logic Truth Table.

LOGIC INPUT COMPATIBILITY

The DAC813 digital inputs are TTL, 5V CMOS compatible over the operating range of $+V_{CC}$. The input switching threshold remains at the TTL threshold over the supply range. An equivalent circuit of a digital input is shown in Figure 2.

The logic input current over temperature is low enough to permit driving the DAC813 directly from the outputs of 5V CMOS devices.

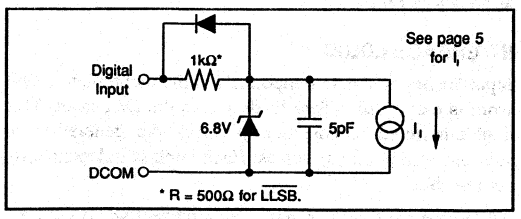


FIGURE 2. Equivalent Input Circuit for Digital Inputs.

RESET FUNCTION

When asserted low (<0.8V), $\overline{RESET}$ (Pin 13) forces the D/A latch to 800_{HEX} regardless of any other input logic condition. If the analog output is connected for bipolar operation (either ±10V or ±5V), the output will be reset to Bipolar Zero (0V). If the analog output is connected for unipolar operation (0 to +10V), the output will be reset to half-scale (+5V).

If $\overline{RESET}$ is not used, it should be connected to a voltage greater than +2V but not greater than +5.5V. If this voltage is not available $\overline{Reset}$ can be connected to $+V_{CC}$ through a 100kΩ to 1MΩ resistor to limit the input current.

GAIN AND OFFSET ADJUSTMENTS

Figures 3 and 4 illustrate the relationship of offset and gain adjustments to unipolar and bipolar D/A converter output.

OFFSET ADJUSTMENT

For unipolar (USB) configurations, apply the digital input code that should produce zero voltage output and adjust the offset potentiometer for zero output. For bipolar (BOB, BTC) configurations, apply the digital input code that should produce the maximum negative output voltage and adjust the offset potentiometer for minus full scale voltage. Example: If the full scale range is connected for 20V, the maximum negative output voltage is –10V. See Table III for corresponding codes.

GAIN ADJUSTMENT

For either unipolar or bipolar configurations, apply the digital input that should give the maximum positive voltage output. Adjust the gain potentiometer for this positive full scale voltage. See Table III for positive full scale voltages.

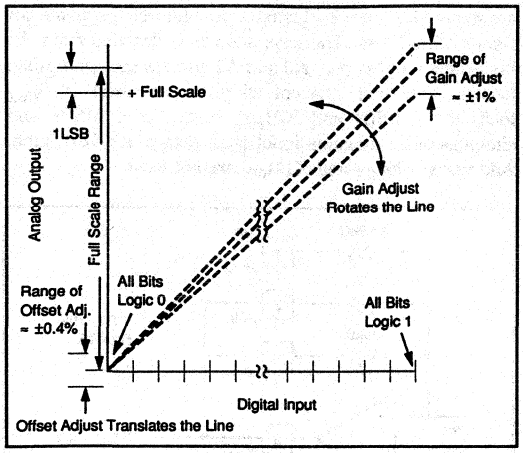


FIGURE 3. Relationship of Offset and Gain Adjustments for a Unipolar D/A Converter.

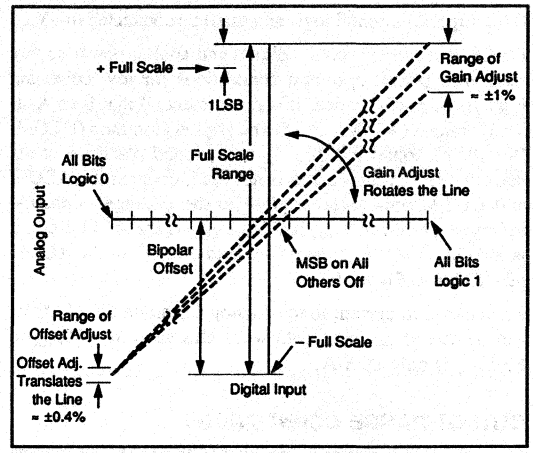


FIGURE 4. Relationship of Offset and Gain Adjustments for a Bipolar D/A Converter.

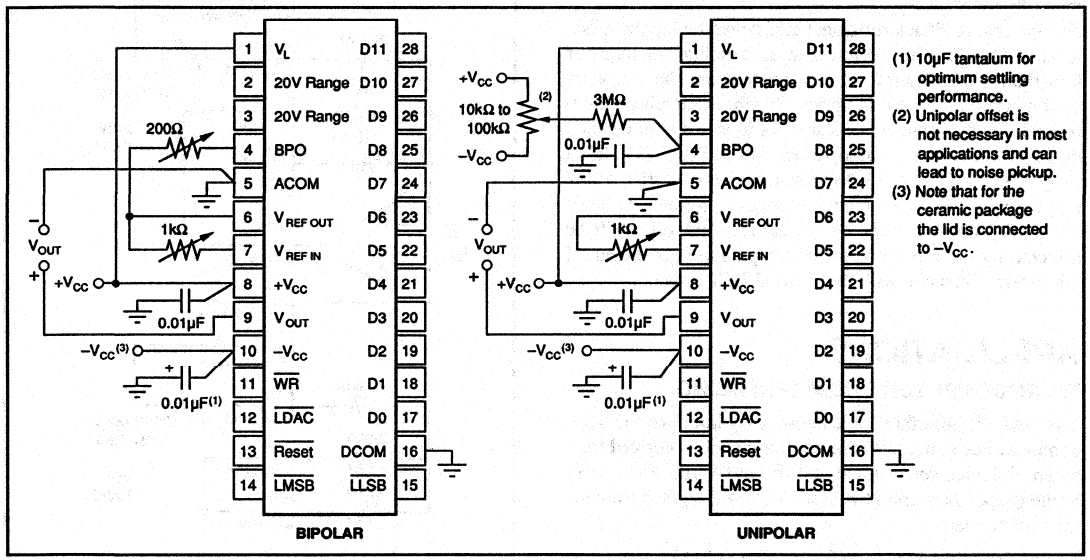


FIGURE 5. Power Supply, Gain, and Offset Connections.

DIGITAL INPUT	ANALOG OUTPUT		
MSB to LSB	0 to +10V	±5V	±10V
FFF_{HEX}	+9.9976V	+4.9976V	+9.9951V
800_{HEX}	+5.0000V	0.0000V	0.0000V
$7FF_{HEX}$	+4.9976V	–0.0024V	–0.0049V
000_{HEX}	0.0000V	–5.0000V	–10.0000V
1LSB	2.44mV	2.44mV	4.88mV

TABLE III. Digital Input/Analog Output.

INSTALLATION

POWER SUPPLY CONNECTIONS

Note that the lid of the ceramic packaged DAC813 is connected to $-V_{CC}$. Take care to avoid accidental short circuits in tightly spaced installations.

Power supply decoupling capacitors should be added as shown in Figure 5. Optimum settling performance occurs using a 1 to 10µF tantalum capacitor at $-V_{CC}$ and at least a 0.01µF ceramic capacitor at $+V_{CC}$. Applications with less critical settling time may be able to use 0.01µF at $-V_{CC}$ as well. The 0.01µF capacitors should be located close to the DAC813.

Pin 1 supplies internal logic and **must** be connected to $+V_{CC}$.

DAC813 features separate digital and analog power supply returns to permit optimum connections for low noise and high speed performance. It is recommended that both Analog Common (ACOM, Pin 5) and Digital Common (DCOM, Pin 10) be connected directly to a ground plane under the package. If a ground plane is not used, connect the ACOM and DCOM pins together close to the package. Since the reference point for V_{OUT} and $V_{REF\ OUT}$ is the ACOM pin, it is also important to connect the load directly to the ACOM pin. Refer to Figure 5.

The change in current in the Analog Common pin (ACOM, Pin 5) due to an input data word change from 000_{HEX} to FFF_{HEX} is only 800µA.

OUTPUT RANGE CONNECTIONS

Internal scaling resistors provided in the DAC813 may be connected to produce bipolar output voltage ranges of ±10V and ±5V or unipolar output voltage range of 0 to +10V. Refer to Figure 6.

The internal feedback resistors (25kΩ) and the bipolar offset resistor (24.9kΩ) are trimmed to an absolute tolerance of less than ±2%. Therefore, one can change the range by adding a series resistor in various feedback circuit configurations. For example, a 600Ω resistor in series with the 20V range terminal can be used to obtain a 20.48V (±10.24V) range (5mV LSB). A 7.98kΩ resistor in series with the 10V range connection (20V ranges in parallel) gives a 16.384V (±8.192V) bipolar range (4mV LSB). Gain drift will be affected by the mismatch of the temperature coefficient of the external resistor with the internal D/A resistors.

APPLICATIONS

MICROCOMPUTER BUS INTERFACING

The DAC813 interface logic allows easy interface to microcomputer bus structures. The control signal is derived from external device select logic and the I/O Write or Memory Write (depending upon the system design) signals from the microcomputer.

The latch enable lines $\overline{LMSB}$, $\overline{LLSB}$, and $\overline{LDAC}$ determine which of the latches are selected. It is permissible to enable two or more latches simultaneously, as shown in some of the following examples.

The double-buffered latch permits data to be loaded into the input latches of several DAC813s and later strobed into the D/A latch of all D/As, simultaneously updating all analog outputs. All the interface schemes shown below use a base address decoder. If blocks of memory are used, the base address decoder can be simplified or eliminated altogether.

8-BIT INTERFACE

The control logic of DAC813 permits interfacing to right-justified data formats, illustrated in Figure 7. When a 12-bit D/A converter is loaded from an 8-bit bus, two bytes of data are required. Figure 8 illustrates an addressing scheme for right-justified data. The base address is decoded from the high-order address bits. A0 and A1 address the appropriate latches. Note that adjacent addresses are used. $X10_{HEX}$ loads the 8 LSBs and $X01_{HEX}$ loads the 4 MSBs and simultaneously transfers input latch data to the D/A latch. Addresses $X00_{HEX}$ and $X11_{HEX}$ are not used.

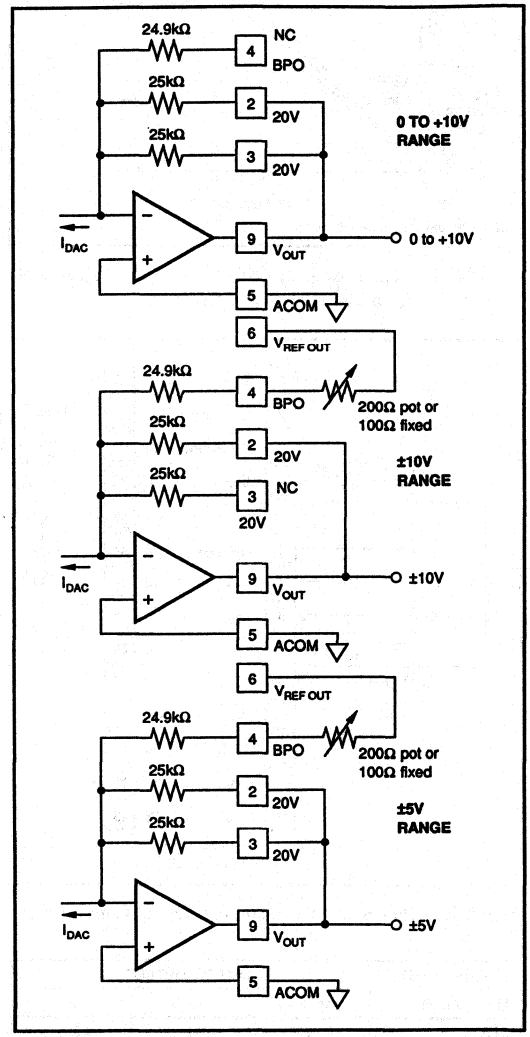


FIGURE 6. Output Amplifier Voltage Range Scaling Circuit.

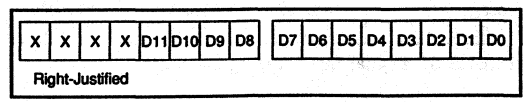


FIGURE 7. 12-Bit Data Format for 8-Bit Systems.

INTERFACING MULTIPLE DAC813s IN 8-BIT SYSTEMS

Many applications, such as automatic test systems, require that the outputs of several D/A converters be updated simultaneously. The interface shown in Figure 9 uses a 74LSB138 decoder to decode a set of eight adjacent addresses to load the input latches of four DAC813s. The example uses a right-justified data format.

A ninth address using A3 causes all DAC813s to be updated simultaneously. If a certain DAC813 is always loaded last (for instance, D/A #4), A3 is not needed, saving 8 address spaces for other uses. Incorporate A3 into the base address decoder, remove the inverter, connect the common $\overline{LDAC}$ line to $\overline{LLSB}$ of D/A #4, and connect D1 of the 74LS138 to +5V.

12- AND 16-BIT MICROCOMPUTER INTERFACE

For this application the input latch enable lines, $\overline{LMSB}$ and $\overline{LLSB}$, are tied low, causing the latches to be transparent. The D/A latch, and therefore DAC813, is selected by the address decoder and strobed by $\overline{WR}$.

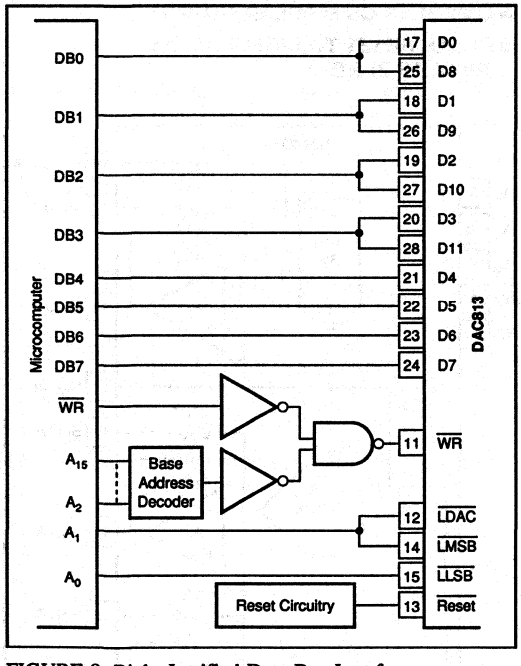
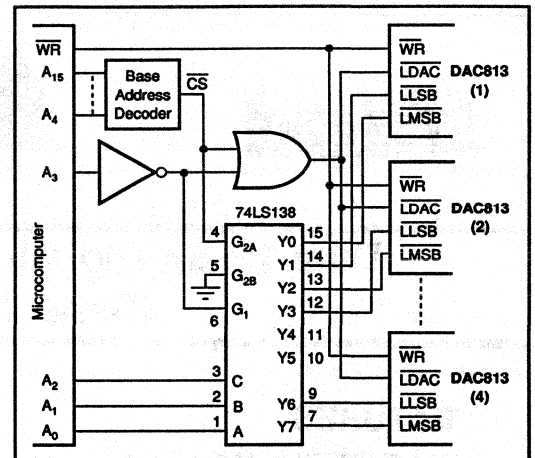


FIGURE 8. Right-Justified Data Bus Interface.



ADDRESS BUS A3	A2	A1	A0	OPERATION
0	0	0	0	Load 8 LSB – D/A #1
0	0	0	1	Load 4 MSB – D/A #1
0	0	1	0	Load 8 LSB – D/A #2
0	0	1	1	Load 4 MSB – D/A #2
0	1	0	0	Load 8 LSB – D/A #3
0	1	0	1	Load 4 MSB – D/A #3
0	1	1	0	Load 8 LSB – D/A #4
0	1	1	1	Load 4 MSB – D/A #4
1	X	X	X	Load D/A Latch—All D/A

FIGURE 9. Interfacing Multiple DAC813s to an 8-Bit Bus.

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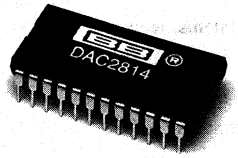


DAC2814

Dual 12-Bit Digital-to-Analog Converter (Serial Interface)

FEATURES

- COMPLETE DUAL DAC — INCLUDES INTERNAL REFERENCES AND OUTPUT AMPLIFIERS
- GUARANTEED SPECIFICATIONS OVER TEMPERATURE
- GUARANTEED MONOTONIC OVER TEMPERATURE
- HIGH-SPEED SERIAL INTERFACE (10MHz CLOCK)
- LOW POWER, 300mW (150mW/DAC)
- LOW GAIN DRIFT, 5ppm/°C
- LOW NONLINEARITY, ±1/2 LSB MAX
- UNIPOLAR OR BIPOLAR OUTPUT
- CLEAR/RESET TO UNIPOLAR OR BIPOLAR ZERO

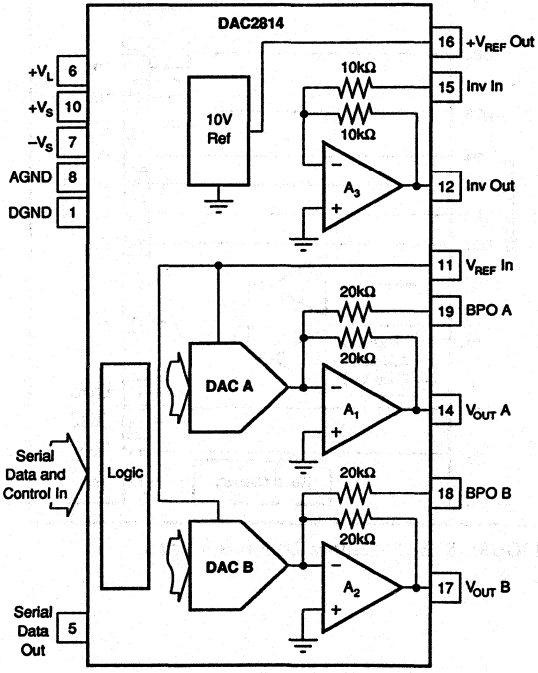
DESCRIPTION

The DAC2814 is one in a family of dual and quad 12-bit digital-to-analog converters. Serial, 8-bit, 12-bit interfaces are available. See back cover for details.

The DAC2814 is complete. It contains CMOS logic, switches, a high-performance buried-zener reference, and low-noise bipolar output amplifiers. No external components are required for either unipolar 0 to 10V, 0 to –10V, or bipolar ±10V output ranges.

The DAC2814 has a high-speed serial interface capable of being clocked at 10MHz. Serial data are clocked DAC B MSB first into a 24-bit shift register, then strobed into each DAC separately or simultaneously as required. The DAC has an asynchronous clear control for reset to unipolar or bipolar zero depending on the mode selected. This feature is useful for power-on reset or system calibration. The DAC2814 is packaged in a 24-pin plastic DIP rated for the –40°C to +85°C extended industrial temperature range.

High-stability laser-trimmed thin film resistors assure high reliability and true 12-bit integral and differential linearity over the full specified temperature range.



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Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

PDS-1103A

SPECIFICATIONS, Guaranteed over T_A = –40°C to +85°C unless otherwise specified.

ELECTRICAL

Specifications as shown for V_S = ±12V or ±15V, V_L = +5V, and R_L = 2kΩ unless otherwise noted.

PARAMETER	CONDITIONS	DAC2814AP MIN	DAC2814AP TYP	DAC2814AP MAX	DAC2814BP MIN	DAC2814BP TYP	DAC2814BP MAX	UNITS
DIGITAL INPUTS								
Resolution		12			•			Bits
V_{IH} (Input High Voltage)		+2		+5	•		•	V
V_{IL} (Input Low Voltage)		0		+0.8	•		•	V
I_{IN} (Input Current)	T_A = 25°C			±1			•	µA
	T_A = –40°C to +85°C			±10			•	µA
C_{IN} (Input Capacitance)			0.8			•		pF
DIGITAL OUTPUT								
Data Out V_{OL}	I_{SINK} = 1.6mA	0		+0.4	•		•	V
V_{OH}	I_{SOURCE} = 500µA	+2.4		+5	•		•	V
ACCURACY								
Integral, Relative Linearity[1]				±1			±1/2	LSB
Differential Nonlinearity[2]	T_A = 25°C			±1			•	LSB
	T_A = –40°C to +85°C		+1.5/–1				±1	LSB
Unipolar Offset Error	T_A = +25°C			±1			±0.5	mV
	T_A = –40°C TO +85°C			±3			•	mV
Bipolar Zero Error				±20			±10	mV
Gain Error Unipolar, Bipolar	With Internal or External 10.0V Ref			±0.2			±0.15	%
Power Supply Sensitivity[3]	V_S = ±11.4V to ±18V			30			•	ppmFSR/V
	V_L = +4.5V to +5.5V							
TEMPERATURE DRIFT								
Gain Drift Unipolar, Bipolar			±5	±30		•	±20	ppm/°C
Unipolar Offset Drift			±0.1	±5		•	•	ppmFSR/°C
Bipolar Zero Drift			±5	±15		•	±8	ppmFSR/°C
REFERENCE OUTPUT								
Output Voltage		+9.980	+10	+10.020	+9.985	•	+10.015	V
Reference Drift			±2	±30		•	±20	ppm/°C
Output Current	T_A = 25°C	+10/–5			•			mA
	T_A = –40°C to +85°C	+6.5/–5			•			mA
Max Load Capacitance (For Stability)			500			•		pF
Short Circuit Current			±20			•		mA
Load Regulation (ΔV_{OUT} vs ΔI_{LOAD})				40			•	ppm/mA
Supply Regulation (ΔV_{OUT} vs ΔV_S)				±5			•	ppm/V
INVERTER								
–10V Reference[4], Inverter Output		–10.020	–10	–9.980	–10.015	•	–9.985	V
–10V Reference Drift				±30			±20	ppm/°C
DC Output Impedance			0.1			•		Ω
Output Current		±7			•			mA
Max Load Capacitance (For Stability)			200			•		pF
Short Circuit Current			±30			•		mA
REFERENCE INPUT								
Reference Input Resistance		3.5	5		•	•		kΩ
Inverter Input Resistance		7	10		•	•		kΩ
BPO Input Resistance		14	20		•	•		kΩ
Reference Input Range				±10			•	V
ANALOG SIGNAL OUTPUTS								
Voltage Range		$–V_S$ + 1.4		$+V_S$ – 1.4	•		•	V
DC Output Impedance			0.1			•		Ω
Output Current		±5			•			mA
Max Load Capacitance (For Stability)	V_{OUT}		500			•		pF
Short Circuit Current			±30			•		mA
DYNAMIC PERFORMANCE[5]	C_L = 100pF							
Unipolar Mode Settling Time	To 1/2 LSB of Full Scale		2.5	10		•	•	µs
Bipolar Mode Settling Time	To 1/2 LSB of Full Scale		3.5	10		•	•	µs
Slew Rate			10			•		V/µs
Small-Signal Bandwidth			3			•		MHz
ANALOG GROUND CURRENT (Code Dependent)			±2			•		mA
DIGITAL CROSSTALK	Full Scale Transition C_L = 100pF		3			•		nV-s
D-TO-A GLITCH IMPULSE			30			•		nV-s

SPECIFICATIONS (CONT), Guaranteed over T_A = –40°C to +85°C unless otherwise specified.

ELECTRICAL

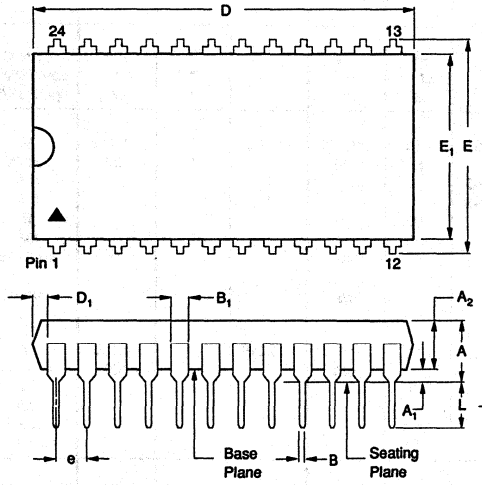
Specifications as shown for V_S = ±12V or ±15V, V_L = +5V, and R_L = 2kΩ unless otherwise noted.

PARAMETER	CONDITIONS	DAC2814AP			DAC2814BP			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
POWER SUPPLY								
$+V_S$ and $-V_S$		±11.4	±15	±18	•	•	•	V
$+V_L$		4.5	5	5.5	•	•	•	V
$+I_S$			+10	+13.5		•	•	mA
$-I_S$			–10	–13.5		•	•	mA
$+I_L$	Digital Inputs = 0V or $+V_L$		0.2	1		•	•	mA
$+I_L$	Digital Inputs = V_{IL} or V_{IH}			5			•	mA
Total Power, All DACs			300	410		•	•	mW
TEMPERATURE RANGE								
Specified		–40		+85	•		•	°C
Operating		–40		+85	•		•	°C
Thermal Resistance θ_{JA}			75			•		°C/W

NOTES: (1) End point linearity. (2) Guaranteed monotonic. (3) Change in bipolar full scale output. Includes voltage output DAC, voltage reference, and reference inverter. (4) Inverter output with inverter input connected to $+V_{REF}$. (5) Guaranteed but not tested.

MECHANICAL

P Package — 24-Pin Plastic, Double-Wide DIP



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.155	.250	3.94	6.35
A_1	.015	.070	.381	1.78
A_2	.140	.185	3.57	4.70
B	.014	.022	.356	.559
B_1	.040	.070	1.02	1.78
C	.008	.015	.20	.381
D	1.235	1.265	31.37	32.13
D_1	.040	.100	1.020	2.540
E	.600	.625	15.24	15.88
E_1	.525	.565	13.34	14.35

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
e	.100 BASIC		2.54 BASIC	
eA	.600 BASIC		15.24 BASIC	
eB	.600	.700	15.24	17.78
L	.115	.200	2.91	5.08

NOTES:
(1) Not JEDEC Standard.
(2) Controlling dimension: INCH.
(3) Dimensioning and tolerancing per ANSI Y14.5M-1982.
(4) Dimensions A, A_1 and L are measured with package seated in JEDEC Seating Plane Gauge GS-3.
(5) D and E_1 does not include mold flash. Mold flash shall not exceed .010 inches, 0.25mm.
(6) eB and eC are measured at the lead tips with the leads unconstrained. eC must be zero or greater.

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

ABSOLUTE MAXIMUM RATINGS

$+V_L$ to AGND	0V, +7V
$+V_L$ to DGND	0V, +7V
$+V_S$ to AGND	0V, +18V
$-V_S$ to AGND	0V, –18V
AGND to DGND	±0.3V
Any digital input to DGND	–0.3V, $+V_L$ +0.3V
Ref In to AGND	±25V
Ref In to DGND	±25V
Storage Temperature Range	–55°C to +125°C
Operating Temperature Range	–40°C to +85°C
Lead Temperature (soldering, 10s)	+300°C
Junction Temperature	+155°C
Output Short Circuit	Continuous to common or $\pm V_S$
Reference Short Circuit	Continuous to common or $+V_S$

ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

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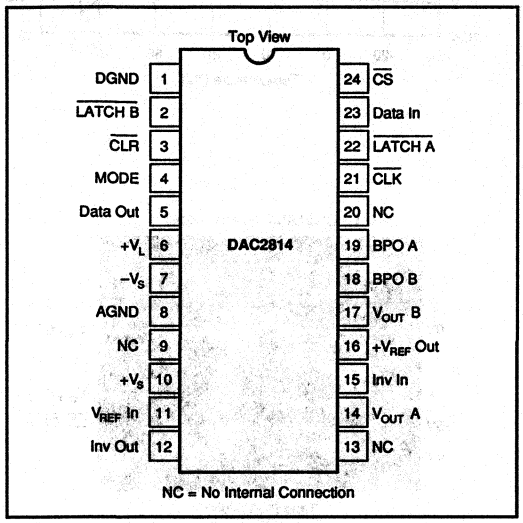
PIN DESIGNATIONS

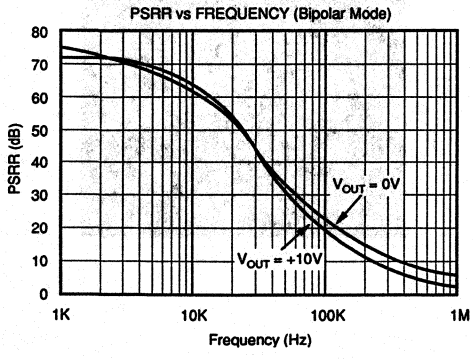
PIN	DESCRIPTOR	FUNCTION	PIN	DESCRIPTOR	FUNCTION
1	DGND	Digital common	24	$\overline{CS}$	Chip select enable, DAC A and DAC B
2	$\overline{LATCH\ B}$	Latch data update, logic input, DAC B	23	Data In	Serial data input
3	$\overline{CLR}$	Asychronous input reset to zero	22	$\overline{LATCH\ A}$	Latch data update, logic input, DAC A
4	MODE	Selection input for unipolar or bipolar reset to zero	21	$\overline{CLK}$	Clock input
5	Data Out	Serial data output	20	NC	No internal connection
6	$+V_L$	Positive logic power supply, +5V input	19	BPO A	Bipolar offset input, DAC A
7	$-V_S$	Negative analog power supply , –15V input	18	BPO B	Bipolar offset input, DAC B
8	AGND	Analog common	17	V_{OUT} B	Analog output voltage, DAC B
9	NC	No internal connection	16	$+V_{REF}$ Out	Reference voltage, +10V output
10	$+V_S$	Positive analog power supply, +15V input	15	Inv In	Inverter (A3) input
11	V_{REF} In	± Reference voltage input	14	V_{OUT} A	Analog output voltage, DAC A
12	Inv Out	Inverter (A3) output	13	NC	No internal connection

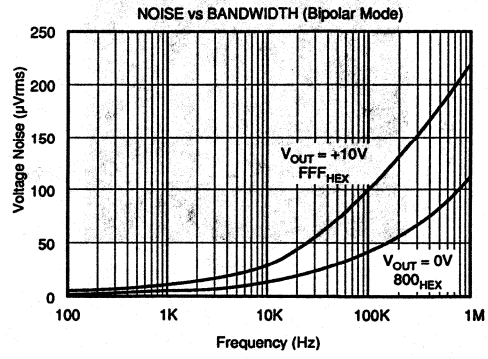
PIN CONFIGURATIONS



TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_S = ±12V or ±15V, V_L = +5V unless otherwise noted.

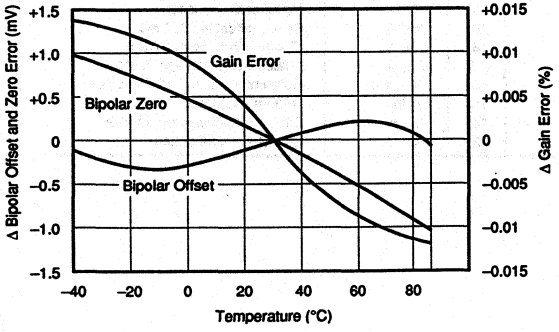




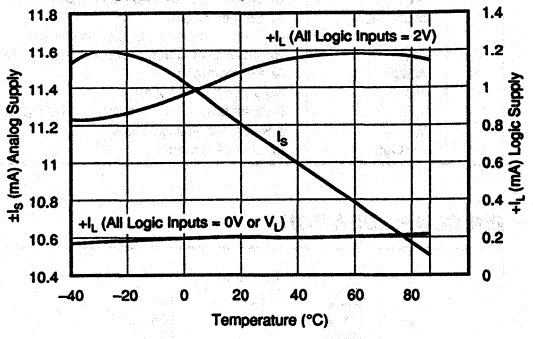
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_S = ±12V or ±15V, V_L = +5V unless otherwise noted.

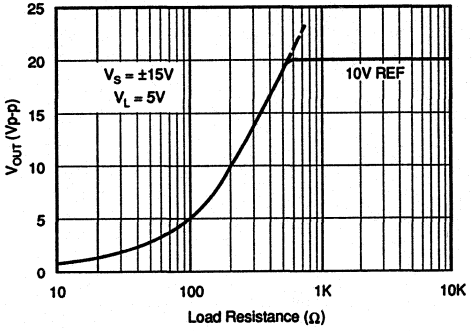
CHANGE OF GAIN, BIPOLAR OFFSET AND ZERO ERROR vs TEMPERATURE



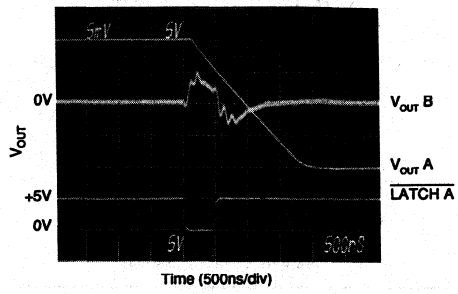
POWER SUPPLY CURRENT vs TEMPERATURE



OUTPUT VOLTAGE SWING vs RESISTOR LOAD

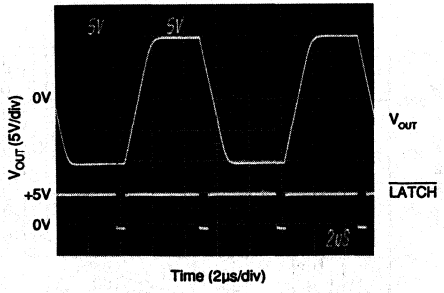


CROSSTALK (Bipolar Mode)

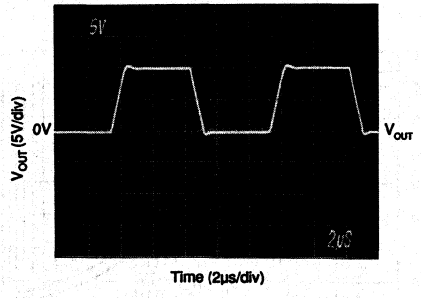


NOTE: Crosstalk is dominated by digital crosstalk/ feedthrough of the $\overline{\text{LATCH}}$ signal.

FULL-SCALE OUTPUT SWING BIPOLAR (20V Step)



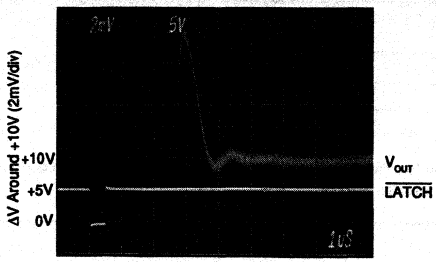
FULL-SCALE OUTPUT SWING UNIPOLAR (10V Step)



TYPICAL PERFORMANCE CURVES (CONT)

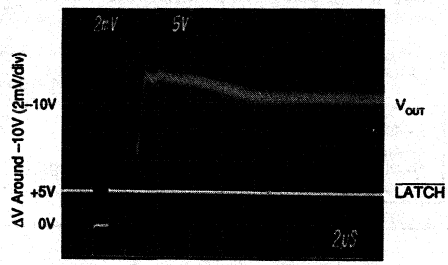
T_A = +25°C, V_S = ±12V or ±15V, V_L = +5V unless otherwise noted.

SETTLING TIME
BIPOLAR (–10V to +10V)



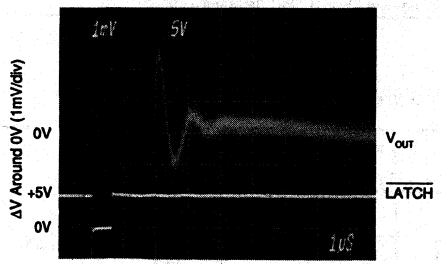
Time (1µs/div)

SETTLING TIME
BIPOLAR (+10V to –10V Step)



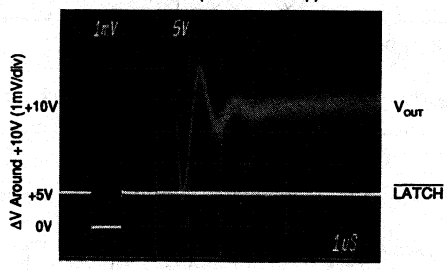
Time (2µs/div)

SETTLING TIME
UNIPOLAR (+10V to 0V STEP)



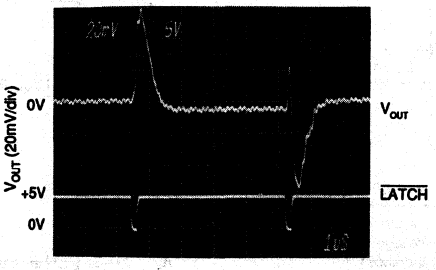
Time (1µs/div)

SETTLING TIME
UNIPOLAR (0V to +10V Step)



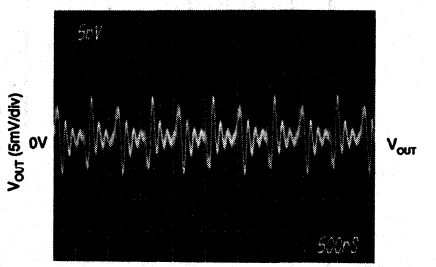
Time (1µs/div)

MAJOR CARRY GLITCH



Time (1µs/div)
NOTE: Data transition 800_{HEX} to $7FF_{HEX}$.

DIGITAL FEEDTHROUGH

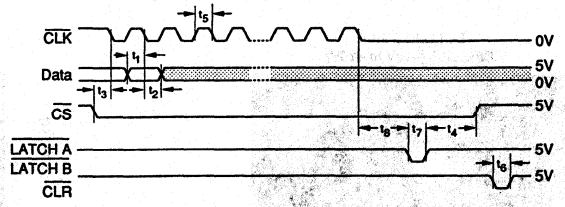


Time (500ns/div)
DAC output noise due to activity on digital inputs with latch disabled.

TIMING CHARACTERISTICS

V_L = +5V, T_A = –40°C to +85°C.

PARAMETER	MINIMUM
t_1—Data Setup Time	15ns
t_2—Data Hold time	15ns
t_3—Chip Select to $\overline{CLK}$, Latch, Data Setup Time	15ns
t_4—Chip Select to $\overline{CLK}$, Latch, Data Hold Time	40ns
t_5—$\overline{CLK}$ Pulse Width	40ns
t_6—Clear Pulse Width	40ns
t_7—Latch Pulse Width	40ns
t_8—$\overline{CLK}$ Edge to $\overline{LATCH\ A}$ or $\overline{LATCH\ B}$	15ns



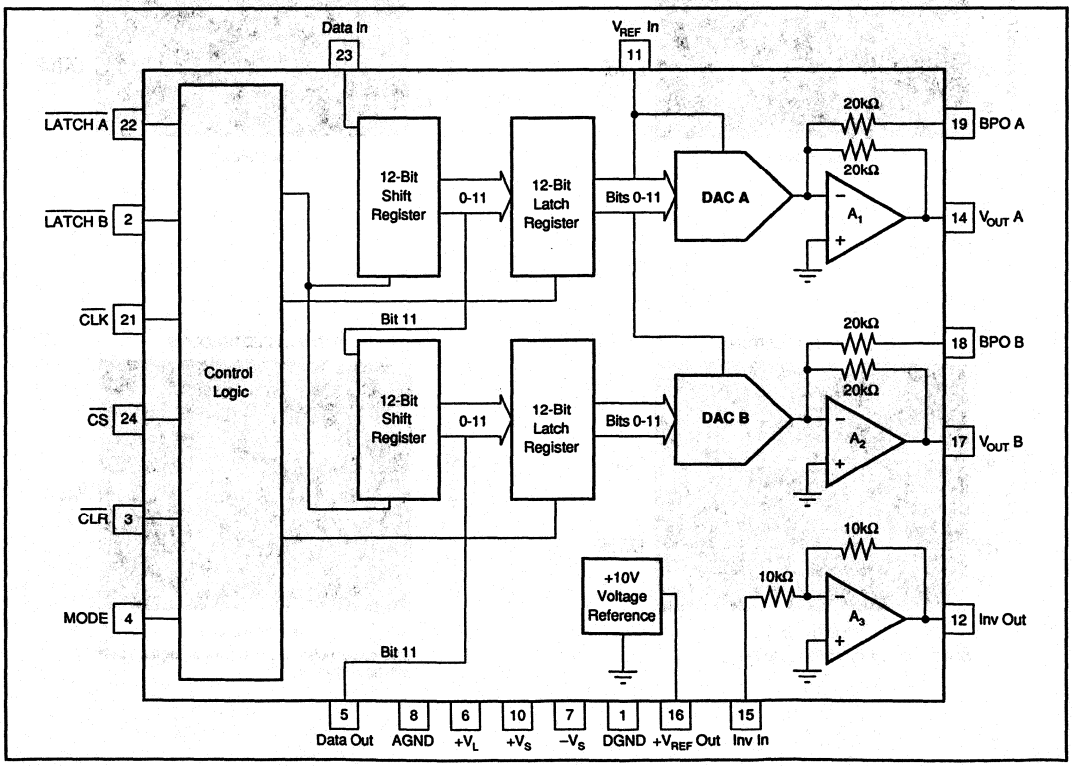
NOTES: (1) All input signal rise and fall times are measured from 10% to 90% of +5V. $t_R = t_F$ = 5ns.
(2) Timing measurement reference level is $\frac{V_{IH} + V_{IL}}{2}$.

INTERFACE LOGIC TRUTH TABLE

MODE	$\overline{CLR}$	$\overline{CLK}$	$\overline{CS}$	$\overline{LATCH\ A}$	$\overline{LATCH\ B}$	FUNCTION
X	1	↓	0	X	X	Data Clocked In
X	1	X	1	X	X	No Data Transfer
X	1	X	0	0	1	DAC A Register Updated
X	1	X	0	1	0	DAC B Register Updated
X	1	X	0	0	0	DAC A and DAC B Updated Together
0	0	X	X	X	X	All Registers Cleared
1	0	X	X	X	X	Shift Registers Cleared, DAC Registers = 800_{HEX}

NOTE: X = Don't care ↓ = Falling edge triggered.

FUNCTIONAL BLOCK DIAGRAM , DAC2814 — Dual, 12-bit DAC, Serial Port



DISCUSSION OF SPECIFICATIONS

INPUT CODES

All digital inputs of the DAC2814 are TTL and 5V CMOS compatible. Input codes for the DAC2814 are either USB (Unipolar Straight Binary) or BOB (Bipolar Offset Binary) depending on the mode of operation. See Figure 3 for ±10V bipolar connection. See Figures 4 and 5 for 0 to 10V and 0 to –10V unipolar connections.

UNIPOLAR AND BIPOLAR OUTPUTS FOR SELECTED INPUT

DIGITAL INPUT	UNIPOLAR (USB)	BIPOLAR (BOB)
FFF_{HEX}	+Full scale	+Full scale
800_{HEX}	+1/2 Full scale	Zero
$7FF_{HEX}$	+1/2 Full scale – 1 LSB	Zero – 1 LSB
000_{HEX}	Zero	–Full scale

INTEGRAL OR RELATIVE LINEARITY

This term, also know as end point linearity, describes the transfer function of analog output to digital input code. Integral linearity error is the deviation of the analog output versus code transfer function from a straight line drawn through the end points.

DIFFERENTIAL NONLINEARITY

Differential nonlinearity is the deviation from an ideal 1 LSB change in the output voltage when the input code changes by 1 LSB. A differential nonlinearity specification of ±1 LSB maximum guarantees monotonicity.

UNIPOLAR OFFSET ERROR

The output voltage for code 000_{HEX} when the DAC is in unipolar mode of operation.

BIPOLAR ZERO ERROR

The output voltage for code 800_{HEX} when the DAC is in the bipolar mode of operation.

GAIN ERROR

The deviation of the output voltage span ($V_{MAX} - V_{MIN}$) from the ideal span of 10V – 1 LSB (unipolar mode) or 20V – 1 LSB (bipolar mode). The gain error is specified with and without the internal +10V reference error included.

OUTPUT SETTLING TIME

The time required for the output voltage to settle within a percentage-of-full-scale error band for a full scale transition. Settling to ±0.012% (1/2 LSB) is specified for the DAC2814.

DIGITAL-TO-ANALOG GLITCH

Ideally, the DAC output would make a clean step change in response to an input code change. In reality glitches occur during the transition. See Typical Performance Curves.

DIGITAL CROSSTALK

Digital crosstalk is the glitch impulse measured at the output of one DAC due to a full scale transition on the other DAC—see Typical Performance Curves. It is dominated by digital coupling. Also, the integrated area of the glitch pulse is specified in nV–s. See table of electrical specifications.

DIGITAL FEEDTHROUGH

Digital feedthrough is the noise at a DAC output due to activity on the digital inputs—see Typical Performance Curves.

OPERATION

DACs can be updated simultaneously or independently as required. Data are transferred on falling clock edges into a 24-bit shift register. DAC B MSB is loaded first. Data are transferred to the DAC registers when the $\overline{\text{LATCH}}$ signals are brought low. The data are latched when the $\overline{\text{LATCH}}$ signals are brought high. Both $\overline{\text{LATCH}}$ signals may be tied together to allow simultaneous update of the DACs if required. The output of the DAC shift register is provided to allow cascading of several DACS on the same bit stream.

By using separate signals for $\overline{\text{LATCH A}}$ and $\overline{\text{LATCH B}}$, it is possible to update either one of the two DACs every 12 clock cycles.

CIRCUIT DESCRIPTION

Each of the two DACs in the DAC2814 consists of a CMOS logic section, a CMOS DAC cell, and an output amplifier. One buried-zener +10.0V reference and a reference inverter (for a –10.0V reference) are shared by both DACs.

Figure 1 is a simplified circuit for a DAC cell. An R, 2R ladder network is driven by a voltage reference at V_{REF}. Current from the ladder is switched either to I_{OUT} or AGND by 12 single-pole double-throw CMOS switches. This maintains constant current in each leg of the ladder regardless of digital input code. This makes the resistance at V_{REF} constant (it can be driven by either a voltage or current reference). The reference can be either positive or negative polarity with a range of up to ±10V.

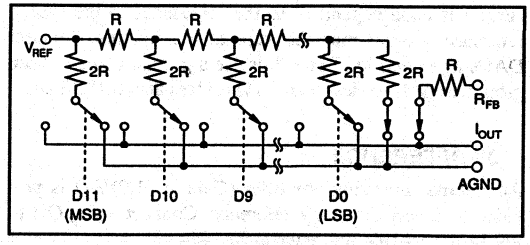


FIGURE 1. Simplified Circuit Diagram of DAC Cell.

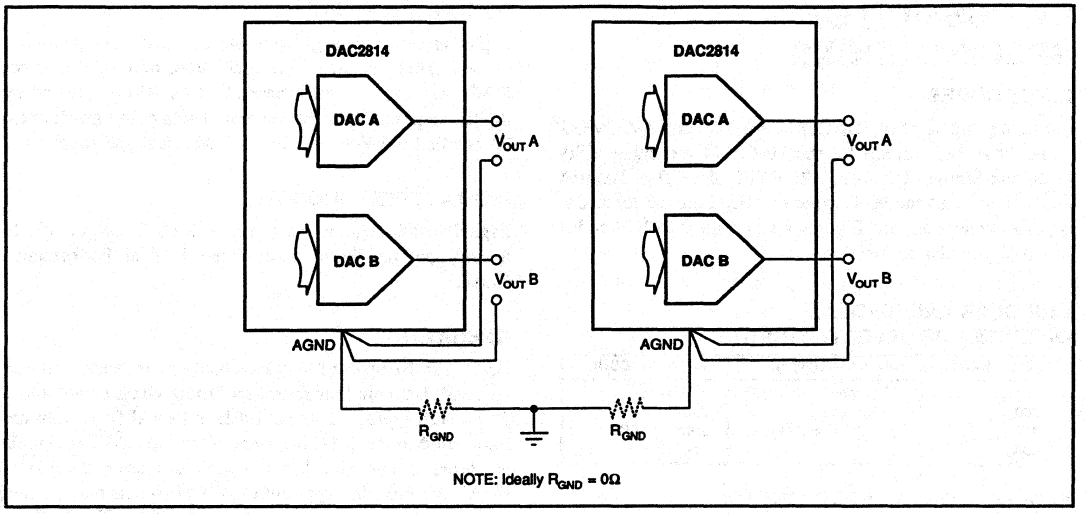


FIGURE 2. Recommended Ground Connections for Multiple DAC packages.

CMOS switches included in series with the ladder terminating resistor and the feedback resistor, R_{FB}, compensate for the temperature drift of the ladder switch ON resistance.

The output op amps are connected as transimpedance amplifiers to convert the DAC-cell output current into an output voltage. They have been specially designed and compensated for precision and fast settling in this application.

POWER SUPPLY CONNECTIONS

The DAC2814 is specified for operation with power supplies of V_L = +5V and V_S = either ±12V or ±15V. Even with the V_S supplies at ±11.4V the DACs can swing a full ±10V. Power supply decoupling capacitors (1µF tantalum) should be located close to the DAC power supply connections.

Separate digital and analog ground pins are provided to permit separate current returns. They should be connected together at one point. Proper layout of the two current returns will prevent digital logic switching currents from degrading the analog output signal. The analog ground current is code dependent so the impedance to the system reference ground must be kept to a minimum. Connect DACs as shown in Figure 2 or use a ground plane to keep ground impedance less than 0.1Ω for less than 0.1LSB error.

–10V REFERENCE

An internal inverting amplifier (Gain = –1.0V/V) is provided to invert the +10V reference. Connect $+V_{REF}$ Out to Inv In for a –10V reference at Inv Out.

OUTPUT RANGE CONNECTIONS

±10V Output Range

For a ±10V bipolar outputs connect the DAC2814 as shown in Figure 3. Connect the MODE to logic high (+5V) for reset to bipolar zero. With MODE connected low (GND) reset will be to –Full-Scale.

0 To +10V Output Range

For 0 to +10V unipolar outputs connect the DAC2814 as shown in Figure 4. Connect the MODE to logic low (GND) for reset to unipolar zero.

0 To –10V Output Range

For 0 to –10V unipolar outputs connect the DAC2814 as shown in Figure 5. Connect the MODE to logic low (GND) for reset to unipolar zero.

CONNECTION TO DIGITAL BUS

Cascaded Bus Connection

Multiple DAC2814s can be connected to the same $\overline{CLK}$ and DATA input lines in two ways. Since the output of the DAC shift register is available, any number of DAC2814s can be cascaded on the same input bit stream as shown in Figure 6. This arrangement allows all DACs in the system to be updated simultaneously and requires a minimum number of control signal inputs. However, up to 24N $\overline{CLK}$ cycles may be required to update any given DAC, where N = number of DAC2814s.

Parallel Bus Connection

Several DAC2814s can also have their DATA inputs connected in parallel as shown in Figure 7. This allows any DAC in the system to be updated in a maximum of 24 $\overline{CLK}$ cycles.

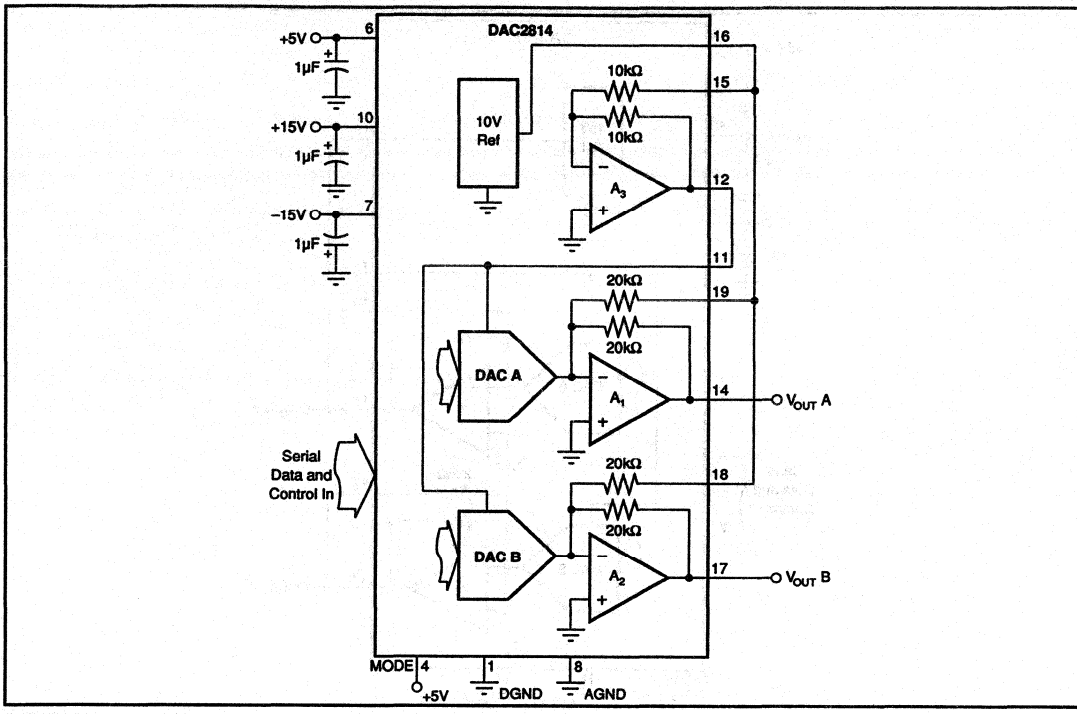


FIGURE 3. Analog Connections for ±10V DAC Output.

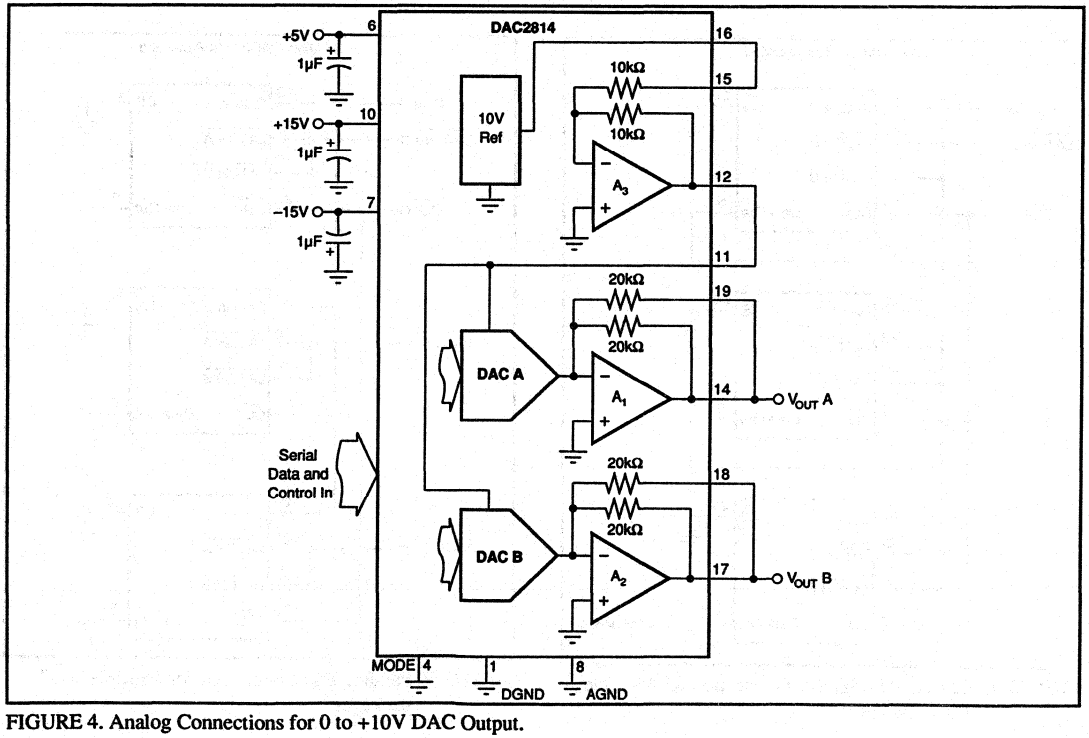


FIGURE 4. Analog Connections for 0 to +10V DAC Output.

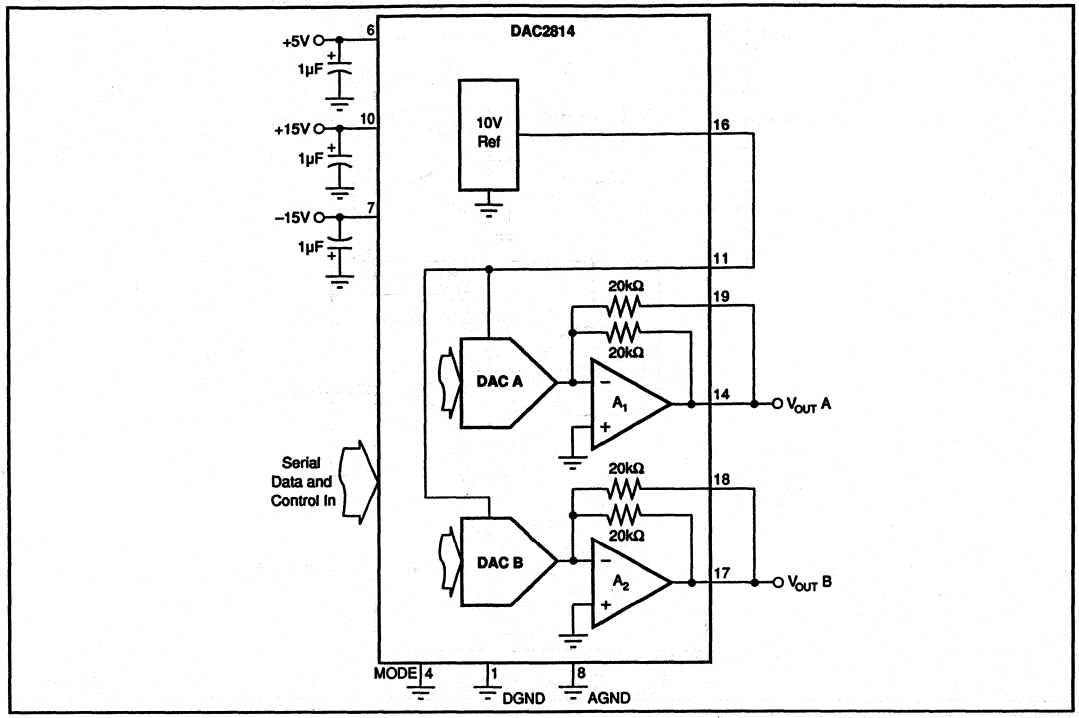


FIGURE 5. Analog Connections for 0 to –10V DAC Output.

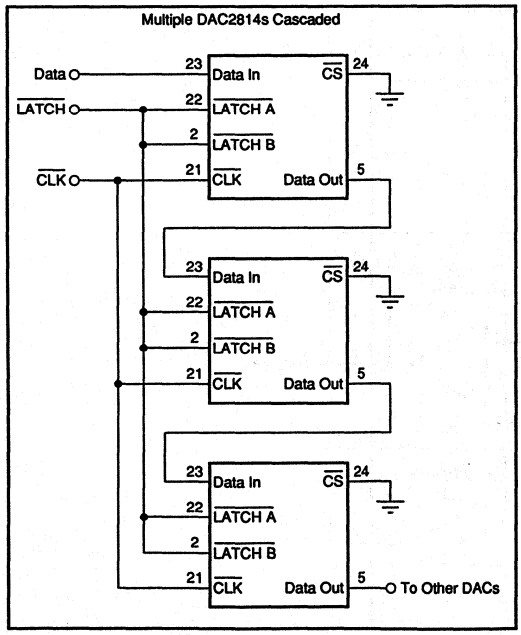


FIGURE 6. Cascaded Serial Bus Connection for Multiple DAC packages.

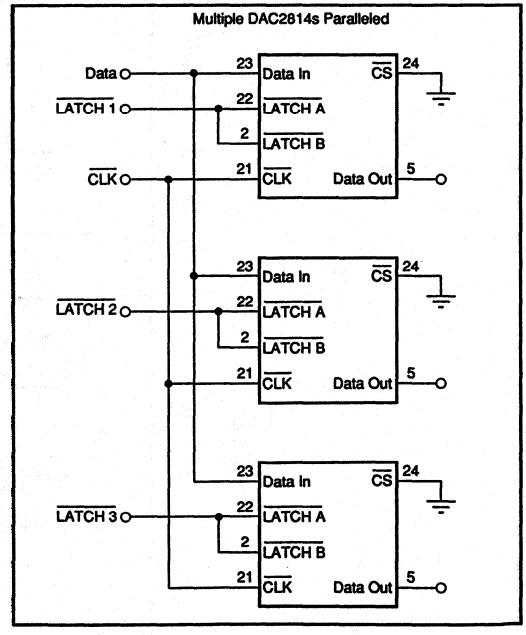
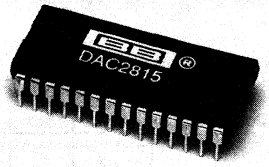


FIGURE 7. Parallel Bus Connection for Multiple DAC packages.

BURR-BROWN®



DAC2815

Dual 12-Bit Digital-to-Analog Converter (8-Bit Port Interface)

FEATURES

- COMPLETE DUAL DAC — INCLUDES INTERNAL REFERENCES AND OUTPUT AMPLIFIERS
- GUARANTEED SPECIFICATIONS OVER TEMPERATURE
- GUARANTEED MONOTONIC OVER TEMPERATURE
- HIGH-SPEED 8 + 4-BIT PARALLEL INTERFACE
- LOW POWER, 300mW (150mW/DAC)
- LOW GAIN DRIFT, 5ppm/°C
- LOW NONLINEARITY, ±1/2 LSB MAX
- UNIPOLAR OR BIPOLAR OUTPUT
- CLEAR/RESET TO UNIPOLAR OR BIPOLAR ZERO

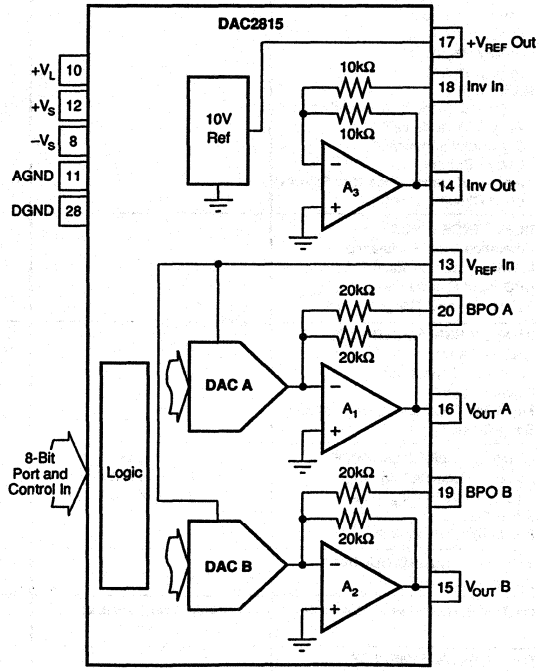
DESCRIPTION

The DAC2815 is one in a family of dual and quad 12-bit digital-to-analog converters (DACs). Serial, 8-bit, 12-bit interfaces are available. See back cover for details.

The DAC2815 is complete. It contains CMOS logic, switches, a high-performance buried-zener reference, and low-noise bipolar output amplifiers. No external components are required for either unipolar 0 to 10V, 0 to –10V, or bipolar ±10V output ranges.

The DAC2815 has a 2-byte (8 + 4) double-buffered interface. Data is first loaded (level transferred) into the input registers in two steps for each DAC. Then both DACs are updated simultaneously. The DAC has an asynchronous clear control for reset to unipolar or bipolar zero depending on the mode selected. This feature is useful for power-on reset or system calibration. The DAC2815 is packaged in a 28-pin plastic DIP rated for the –40°C to +85°C extended industrial temperature range.

High-stability laser-trimmed thin film resistors assure high reliability and true 12-bit integral and differential linearity over the full specified temperature range.



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Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS, Guaranteed over T_A = –40°C to +85°C unless otherwise specified.

ELECTRICAL

Specifications as shown for V_S = ±12V or ±15V, V_L = +5V, and R_L = 2kΩ unless otherwise noted.

PARAMETER	CONDITIONS	DAC2815AP			DAC2815BP			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
DIGITAL INPUTS								
Resolution		12			•			Bits
V_{IH} (Input High Voltage)		2		5	•		•	V
V_{IL} (Input Low Voltage)		0		0.8	•		•	V
I_{IN} (Input Current)	T_A = 25°C			±1			•	µA
	T_A = –40°C to +85°C			±10			•	µA
C_{IN} (Input Capacitance)			0.8			•		pF
ACCURACY								
Integral, Relative Linearity[1]				±1			±1/2	LSB
Differential Nonlinearity[2]	T_A = 25°C			±1			•	LSB
	T_A = –40°C to +85°C		+1.5/–1				±1	LSB
Unipolar Offset Error	T_A = +25°C			±1			±0.5	mV
	T_A = –40°C TO +85°C			±3			•	mV
Bipolar Zero Error				±20			±10	mV
Gain Error Unipolar, Bipolar	With Internal or External 10.0V Ref			±0.2			±0.15	%
Power Supply Sensitivity[3]	V_S = ±11.4V to ±18V, V_L = +4.5V to +5.5V			30			•	ppmFSR/V
TEMPERATURE DRIFT								
Gain Drift Unipolar, Bipolar			±5	±30		•	±20	ppm/°C
Unipolar Offset Drift			±0.1	±5		•	•	ppmFSR/°C
Bipolar Zero Drift			±5	±15		•	±8	ppmFSR/°C
REFERENCE OUTPUT								
Output Voltage		+9.980	+10	+10.020	+9.985	•	+10.015	V
Reference Drift			±2	±30		•	±20	ppm/°C
Output Current	T_A = 25°C	+10/–5			•			mA
	T_A = –40°C to +85°C	+6.5/–5			•			mA
Max Load Capacitance (For Stability)			500			•		pF
Short Circuit Current			±20			•		mA
Load Regulation (ΔV_{OUT} vs ΔI_{LOAD})				40			•	ppm/mA
Supply Regulation (ΔV_{OUT} vs ΔV_S)				±5			•	ppm/V
INVERTER								
–10V Reference[4], Inverter Output		–10.020	–10	–9.980	–10.015	•	–9.985	V
–10V Reference Drift				±30			±20	ppm/°C
DC Output Impedance			0.1			•		Ω
Output Current		±7			•			mA
Max Load Capacitance (For Stability)			200			•		pF
Short Circuit Current			±30			•		mA
REFERENCE INPUT								
Reference Input Resistance		3.5	5		•	•		kΩ
Inverter Input Resistance		7	10		•	•		kΩ
BPO Input Resistance		14	20		•	•		kΩ
Reference Input Range				±10			•	V
ANALOG SIGNAL OUTPUTS								
Voltage Range		$–V_S$ + 1.4		$+V_S$ – 1.4	•		•	V
DC Output Impedance			0.1			•		Ω
Output Current		±5			•			mA
Max Load Capacitance (For Stability)	V_{OUT}		500			•		pF
Short Circuit Current			±30			•		mA
DYNAMIC PERFORMANCE[5]	C_L = 100pF							
Unipolar Mode Settling Time	To 1/2 LSB of Full Scale		2.5	10		•	•	µs
Bipolar Mode Settling Time	To 1/2 LSB of Full Scale		3.5	10		•	•	µs
Slew Rate			10			•		V/µs
Small-Signal Bandwidth			3			•		MHz
ANALOG GROUND CURRENT (Code Dependent)			±2			•		mA
DIGITAL CROSSTALK	Full Scale Transition C_L = 100pF		3			•		nV-s
D-TO-A GLITCH IMPULSE			30			•		nV-s

SPECIFICATIONS (CONT), Guaranteed over T_A = –40°C to +85°C unless otherwise specified.

ELECTRICAL

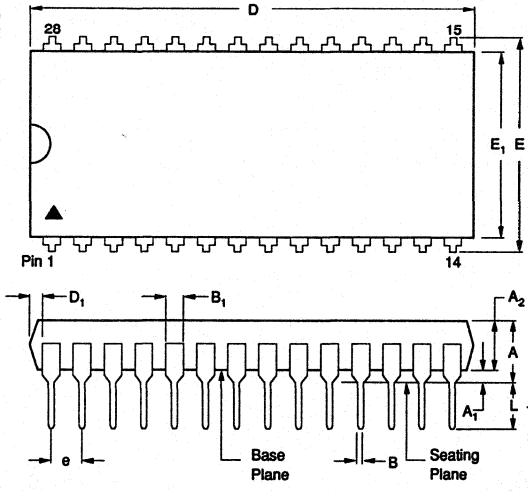
Specifications as shown for V_S = ±12V or ±15V, V_L = +5V, and R_L = 2kΩ unless otherwise noted.

PARAMETER	CONDITIONS	DAC2815AP			DAC2815BP			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
POWER SUPPLY								
$+V_S$ and $-V_S$		±11.4	±15	±18	*	*	*	V
$+V_L$		4.5	5	5.5	*	*	*	V
$+I_S$			+10	+13.5		*	*	mA
$-I_S$			–10	–13.5		*	*	mA
$+I_L$	Digital Inputs = 0V or $+V_L$		0.2	1		*	*	mA
$+I_L$	Digital Inputs = V_{IL} or V_{IH}			5			*	mA
Total Power, All DACs			300	410		*	*	mW
TEMPERATURE RANGE								
Specified		–40		+85	*		*	°C
Operating		–40		+85	*		*	°C
Thermal Resistance, θ_{JA}			75			*		°C/W

NOTES: (1) End point linearity. (2) Guaranteed monotonic. (3) Change in bipolar full scale output. Includes voltage output DAC, voltage reference, and reference inverter. (4) Inverter output with inverter input connected to $+V_{REF}$. (5) Guaranteed but not tested.

MECHANICAL

P Package — 28-Pin Plastic, Double-Wide DIP



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.155	.250	3.94	6.35
A1	.015	.070	.381	1.78
A2	.140	.185	3.57	4.70
B	.014	.022	.356	.559
B1	.040	.070	1.02	1.78
C	.008	.015	.20	.381
D	1.435	1.480	36.45	37.59
D1	.040	.100	1.020	2.540
E	.600	.625	15.24	15.88
E1	.525	.565	13.34	14.35

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
e	.100 BASIC		2.54 BASIC	
eA	.600 BASIC		15.24 BASIC	
eB	.600	.700	15.24	17.78
L	.115	.200	2.91	5.08

NOTES:
(1) Not JEDEC Standard.
(2) Controlling dimension: INCH.
(3) Dimensioning and tolerancing per ANSI Y14.5M-1982.
(4) Dimensions A, A_1 and L are measured with package seated in JEDEC Seating Plane Gauge GS-3.
(5) D and E_1 does not include mold flash. Mold flash shall not exceed .010 inches, 0.25mm.
(6) eB and eC are measured at the lead tips with the leads unconstrained. eC must be zero or greater.

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

ABSOLUTE MAXIMUM RATINGS

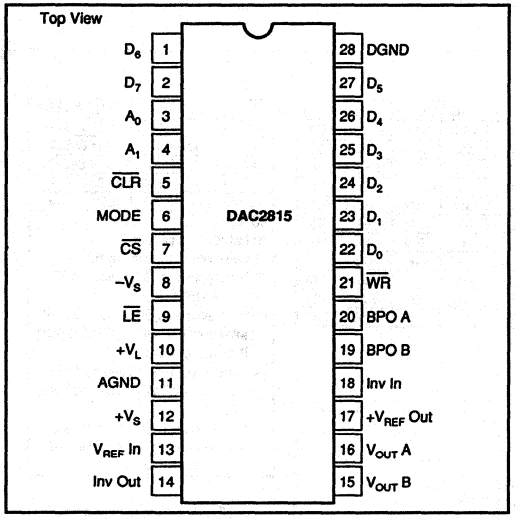
$+V_L$ to AGND	0V, +7V
$+V_L$ to DGND	0V, +7V
$+V_S$ to AGND	0V, +18V
$-V_S$ to AGND	0V, –18V
AGND to DGND	±0.3V
Any digital input to DGND	–0.3V, $+V_L$ +0.3V
Ref In to AGND	±25V
Ref In to DGND	±25V
Storage Temperature Range	–55°C to +125°C
Operating Temperature Range	–40°C to +85°C
Lead Temperature (soldering, 10s)	+300°C
Junction Temperature	+155°C
Output Short Circuit	Continuous to common or $\pm V_S$
Reference Short Circuit	Continuous to common or $+V_S$

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

PIN DESIGNATIONS

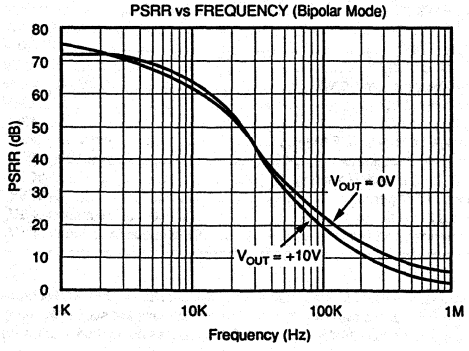
PIN	DESCRIPTOR	FUNCTION	PIN	DESCRIPTOR	FUNCTION
1	D_6	Data bit 6 input	28	DGND	Digital common
2	D_7	Data bit 7 input	27	D_5	Data bit 5 input
3	A_0	Address 0 input	26	D_4	Data bit 4 input
4	A_1	Address 1 input	25	D_3	Data bit 3 input
5	$\overline{CLR}$	Asychronous input reset to zero	24	D_2	Data bit 2 input
6	MODE	Selection input for unipolar or bipolar reset to zero	23	D_1	Data bit 1 input
7	$\overline{CS}$	Chip select enable, DAC A and DAC B	22	D_0	Data bit 0 input
8	$-V_S$	Negative analog power supply, –15V input	21	$\overline{WR}$	Write input, DAC A and DAC B
9	$\overline{LE}$	Latch data enable, DAC A and DAC B	20	BPO A	Bipolar offset input, DAC A
10	$+V_L$	Positive logic power supply, +5V input	19	BPO B	Bipolar offset input, DAC B
11	AGND	Analog common	18	Inv In	Inverter (A3) input
12	$+V_S$	Positive analog power supply, +15V input	17	$+V_{REF}$ Out	Reference voltage, +10V output
13	V_{REF} In	± Reference voltage input	16	V_{OUT} A	Analog output voltage, DAC A
14	Inv Out	Inverter (A_3) output	15	V_{OUT} B	Analog output voltage, DAC B

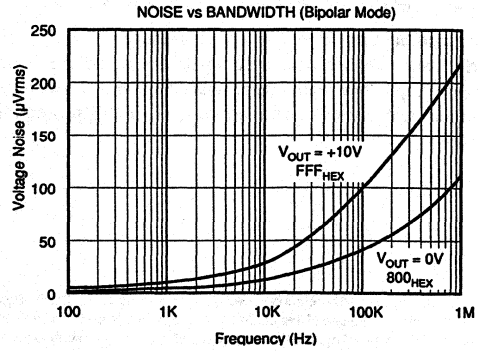
PIN CONFIGURATIONS



TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_S = ±12V or ±15V, V_L = +5V unless otherwise noted.

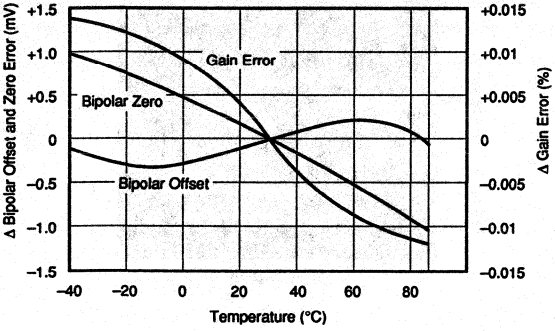




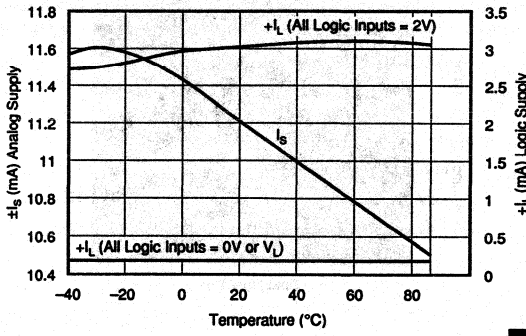
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_S = ±12V or ±15V, V_L = +5V unless otherwise noted.

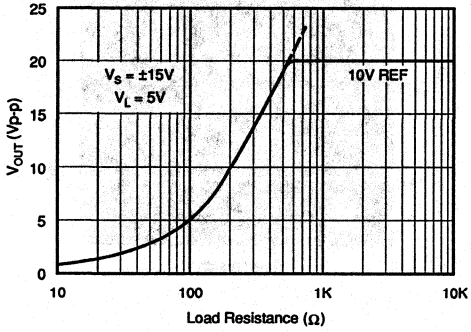
CHANGE OF GAIN, BIPOLAR OFFSET AND ZERO ERROR vs TEMPERATURE



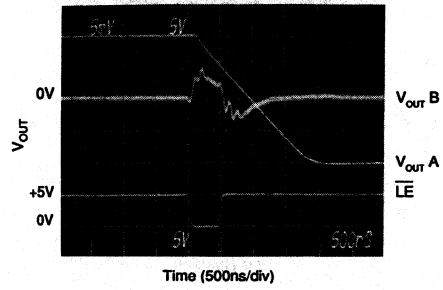
POWER SUPPLY CURRENT vs TEMPERATURE



OUTPUT VOLTAGE SWING vs RESISTOR LOAD



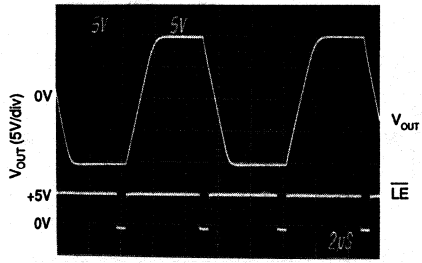
CROSSTALK (Bipolar Mode)



Time (500ns/div)

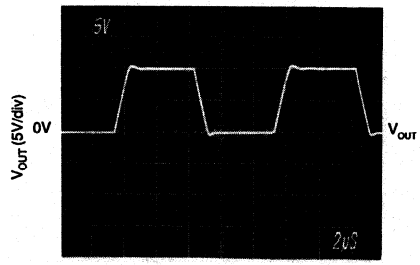
NOTE: Crosstalk is dominated by digital crosstalk/ feedthrough of the $\overline{LE}$ signal.

FULL-SCALE OUTPUT SWING BIPOLAR (20V Step)



Time (2µs/div)

FULL-SCALE OUTPUT SWING UNIPOLAR (10V Step)

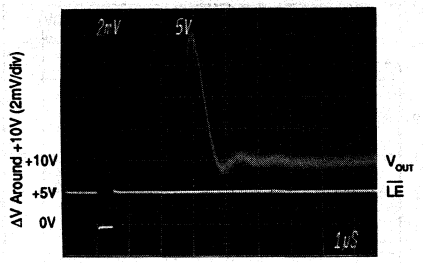


Time (2µs/div)

TYPICAL PERFORMANCE CURVES (CONT)

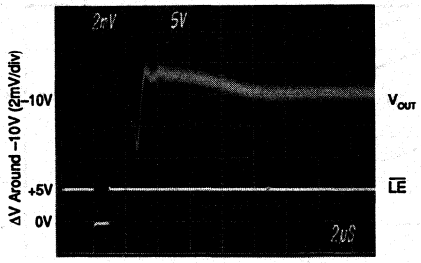
T_A = +25°C, V_S = ±12V or ±15V, V_L = +5V unless otherwise noted.

SETTLING TIME
BIPOLAR (–10V to +10V)



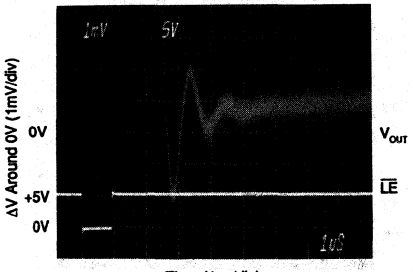
Time (1µs/div)

SETTLING TIME
BIPOLAR (+10V to –10V Step)



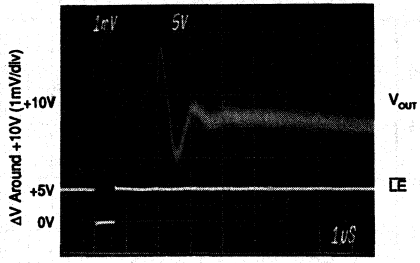
Time (2µs/div)

SETTLING TIME
UNIPOLAR (+10V to 0V STEP)



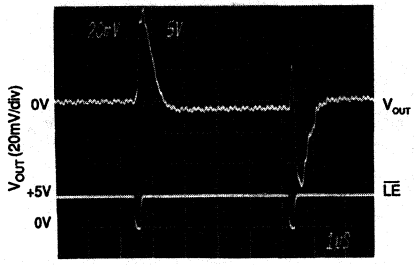
Time (1µs/div)

SETTLING TIME
UNIPOLAR (0V to +10V Step)



Time (1µs/div)

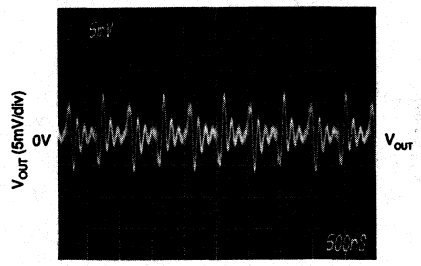
MAJOR CARRY GLITCH



Time (1µs/div)

NOTE: Data transition 800_{HEX} to $7FF_{HEX}$.

DIGITAL FEEDTHROUGH



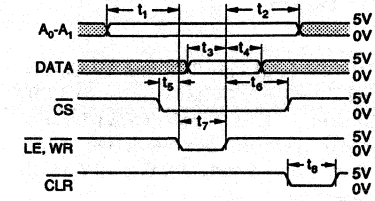
Time (500ns/div)

DAC output noise due to activity on digital inputs with latch disabled.

TIMING CHARACTERISTICS

$+V_L$ = +5V, T_A = −40°C to +85°C.

PARAMETER	MINIMUM
t_1—Address Valid to Write Setup Time	10ns
t_2—Address Valid to Write Hold Time	10ns
t_3—Data Setup Time	30ns
t_4—Data Hold Time	10ns
t_5—Chip Select to $\overline{LE}$ or Write Setup Time	0ns
t_6—Chip Select to $\overline{LE}$ or Write Hold Time	0ns
t_7—Write Pulse Width	40ns
t_8—Clear Pulse Width	40ns



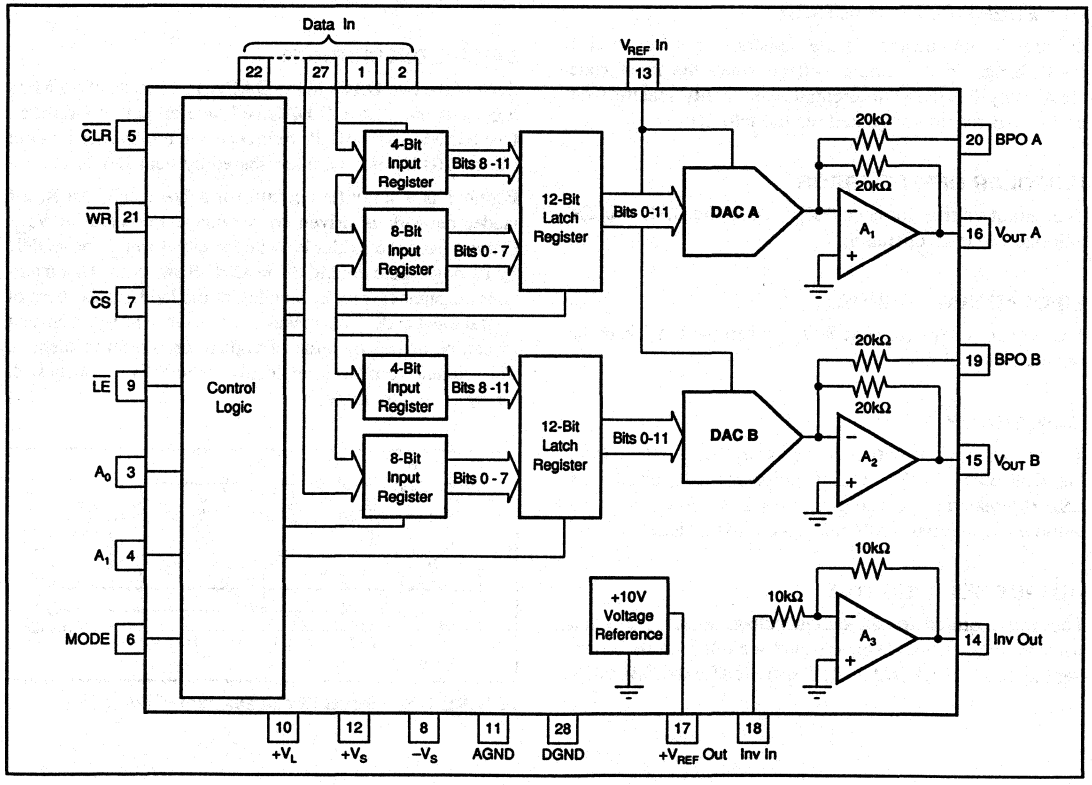
NOTES: (1) All input signal rise and fall times are measured from 10% to 90% of +5V. $t_R = t_F$ = 5ns.
(2) Timing measurement reference level is $\frac{V_{IH} + V_{IL}}{2}$.

INTERFACE LOGIC TRUTH TABLE

MODE	$\overline{CLR}$	$\overline{LE}$	$\overline{CS}$	$\overline{WR}$	A_1	A_0	FUNCTION
X	1	1	0	0	0	0	DAC A LS Input Register Loaded with D7-D0 (LSB)
X	1	1	0	0	0	1	DAC A MS Input Register Loaded with D3-(MSB)-D0
X	1	1	0	0	1	0	DAC B LS Input Register Loaded with D7-D0 (LSB)
X	1	1	0	0	1	1	DAC B MS Input Register Loaded with D3-(MSB)-D0
X	1	0	0	1	X	X	DAC A, DAC B Registers Updated Simultaneously from Input Registers
X	1	0	0	0	X	X	DAC A, DAC B Registers are Transparent
X	1	X	1	X	X	X	No Data Transfer
X	1	1	X	1	X	X	No Data Transfer
0	0	X	X	X	X	X	All Registers Cleared
1	0	X	X	X	X	X	Input Registers Cleared, DAC Registers = 800_{HEX}

NOTE: X = Don't care.

FUNCTIONAL BLOCK DIAGRAM, DAC2815 — Dual 12-bit DAC, 8-bit Port



DISCUSSION OF SPECIFICATIONS

INPUT CODES

All digital inputs of the DAC2815 are TTL and 5V CMOS compatible. Input codes for the DAC2815 are either USB (Unipolar Straight Binary) or BOB (Bipolar Offset Binary) depending on the mode of operation. See Figure 3 for ±10V bipolar connection. See Figures 4 and 5 for 0 to 10V and 0 to –10V unipolar connections.

UNIPOLAR AND BIPOLAR OUTPUTS FOR SELECTED INPUT

DIGITAL INPUT	UNIPOLAR (USB)	BIPOLAR (BOB)
FFF_{HEX}	+Full scale	+Full scale
800_{HEX}	+1/2 Full scale	Zero
$7FF_{HEX}$	+1/2 Full scale – 1 LSB	Zero – 1 LSB
000_{HEX}	Zero	–Full scale

INTEGRAL OR RELATIVE LINEARITY

This term, also known as end point linearity, describes the transfer function of analog output to digital input code. Integral linearity error is the deviation of the analog output versus code transfer function from a straight line drawn through the end points.

DIFFERENTIAL NONLINEARITY

Differential nonlinearity is the deviation from an ideal 1 LSB change in the output voltage when the input code changes by 1 LSB. A differential nonlinearity specification of ±1 LSB maximum guarantees monotonicity.

UNIPOLAR OFFSET ERROR

The output voltage for code 000_{HEX} when the DAC is in the unipolar mode of operation.

BIPOLAR ZERO ERROR

The output voltage for code 800_{HEX} when the DAC is in the bipolar mode of operation.

GAIN ERROR

The deviation of the output voltage span ($V_{MAX} - V_{MIN}$) from the ideal span of 10V – 1 LSB (unipolar mode) or 20V – 1 LSB (bipolar mode). The gain error is specified with and without the internal +10V reference error included.

OUTPUT SETTLING TIME

The time required for the output voltage to settle within a percentage-of-full-scale error band for a full scale transition. Settling to ±0.012% (1/2 LSB) is specified for the DAC2815.

DIGITAL-TO-ANALOG GLITCH

Ideally, the DAC output would make a clean step change in response to an input code change. In reality, glitches occur during the transition. See Typical Performance Curves.

DIGITAL CROSSTALK

Digital crosstalk is the glitch impulse measured at the output of one DAC due to a full scale transition on the other DAC—see Typical Performance Curves. It is dominated by digital coupling. Also, the integrated area of the glitch pulse is specified in nV–s. See table of electrical specifications.

DIGITAL FEEDTHROUGH

Digital feedthrough is the noise at a DAC output due to activity on the digital inputs—see Typical Performance Curves.

OPERATION

Depending on the address selected, the 4 MSBs or the 8 LSBs are written into the appropriate input register for each DAC when the $\overline{WR}$ signal is brought low. This data is latched in the input register when the $\overline{WR}$ goes high. Data are then transferred from the input registers to the DAC latch registers by bring $\overline{LE}$ low. The data are latched in the DAC latch registers when $\overline{LE}$ goes high. Both DACs are updated simultaneously.

CIRCUIT DESCRIPTION

Each of the two DACs in the DAC2815 consists of a CMOS logic section, a CMOS DAC cell, and an output amplifier. One buried-zener +10.0V reference and a reference inverter (for a –10.0V reference) are shared by both DACs.

Figure 1 is a simplified circuit for a DAC cell. An R, 2R ladder network is driven by a voltage reference at V_{REF}. Current from the ladder is switched either to I_{OUT} or AGND by 12 single-pole double-throw CMOS switches. This maintains constant current in each leg of the ladder regardless of digital input code. This makes the resistance at V_{REF} constant (it can be driven by either a voltage or current reference). The reference can be either positive or negative polarity with a range of up to ±10V.

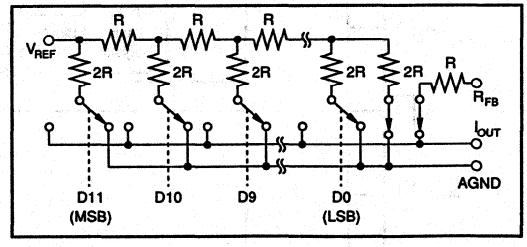


FIGURE 1. Simplified Circuit Diagram of DAC Cell.

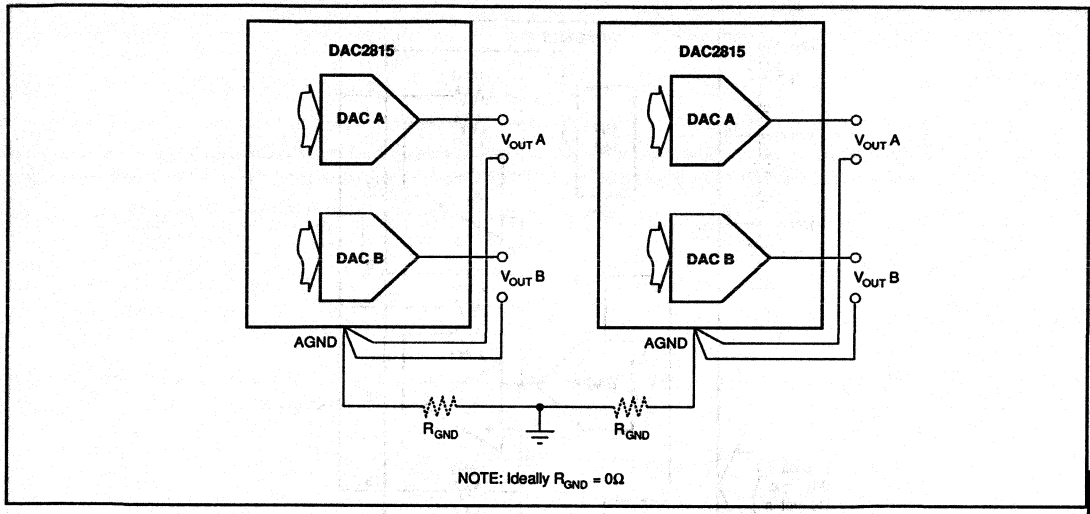


FIGURE 2. Recommended Ground Connections for Multiple DAC packages.

CMOS switches included in series with the ladder terminating resistor and the feedback resistor, R_{FB}, compensate for the temperature drift of the ladder switch ON resistance.

The output op amps are connected as transimpedance amplifiers to convert the DAC-cell output current into an output voltage. They have been specially designed and compensated for precision and fast settling in this application.

POWER SUPPLY CONNECTIONS

The DAC2815 is specified for operation with power supplies of V_L = +5V and V_S = either ±12V or ±15V. Even with the V_S supplies at ±11.4V the DACs can swing a full ±10V. Power supply decoupling capacitors (1µF tantalum) should be located close to the DAC power supply connections.

Separate digital and analog ground pins are provided to permit separate current returns. They should be connected together at one point. Proper layout of the two current returns will prevent digital logic switching currents from degrading the analog output signal. The analog ground current is code dependent so the impedance to the system reference ground must be kept to a minimum. Connect DACs as shown in Figure 2 or use a ground plane to keep ground impedance less than 0.1Ω for less than 0.1LSB error.

–10V REFERENCE

An internal inverting amplifier (Gain = –1.0V/V) is provided to invert the +10V reference. Connect $+V_{REF}$ Out to Inv In for a –10V reference at Inv Out.

OUTPUT RANGE CONNECTIONS

±10V Output Range

For a ±10V bipolar outputs connect the DAC2815 as shown in Figure 3. Connect the MODE to logic high (+5V) for reset to bipolar zero. With MODE connected low (GND) reset will be to –Full-Scale.

0 To +10V Output Range

For 0 to +10V unipolar outputs connect the DAC2815 as shown in Figure 4. Connect the MODE to logic low (GND) for reset to unipolar zero.

0 To –10V Output Range

For 0 to –10V unipolar outputs connect the DAC2815 as shown in Figure 5. Connect the MODE to logic low (GND) for reset to unipolar zero.

CONNECTION TO DIGITAL BUS

DAC2815s can easily be connected to a µprocessor bus. Decode your address lines to derive the control signals shown in Figure 6. Only one $\overline{\text{LATCH}}$ signal is required for a system where all DAC2815s are updated simultaneously. If you want to update DAC2815s independently, use separate $\overline{\text{LATCH}}$ signals. The $\overline{\text{LATCH}}$ and $\overline{\text{WRITE}}$ signals can be brought low simultaneously to update the DAC registers with the same processor instruction that writes the final 8-bit data word the DAC input registers.

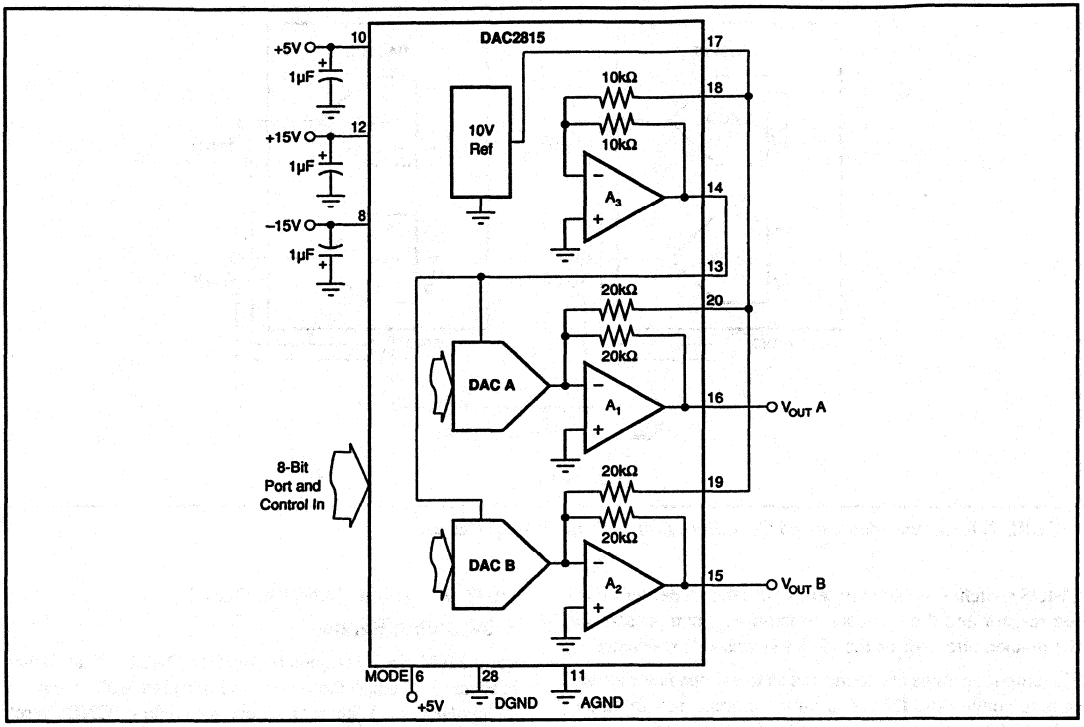


FIGURE 3. Analog Connections for ±10V DAC Output.

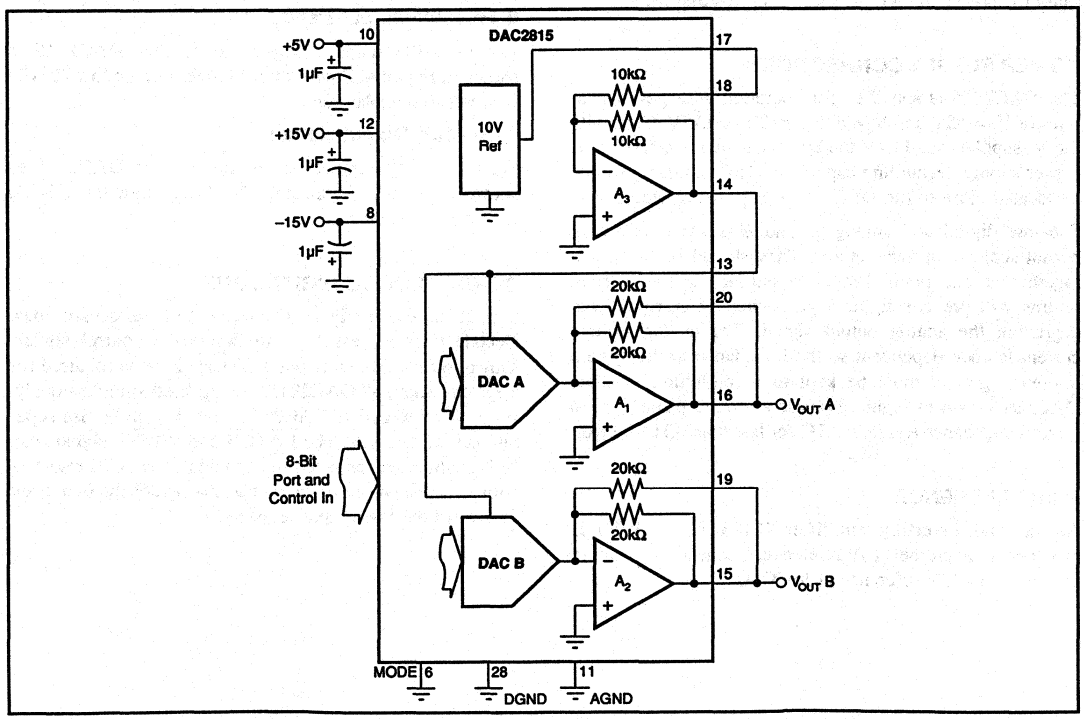


FIGURE 4. Analog Connections for 0 to +10V DAC Output.

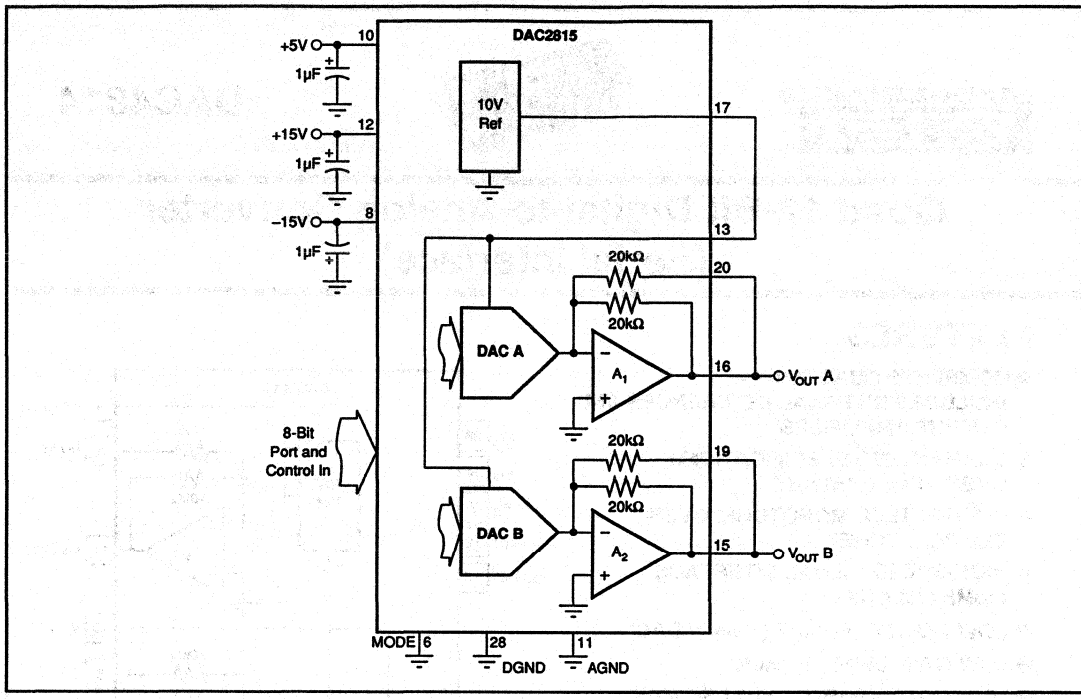


FIGURE 5. Analog Connections for 0 to –10V DAC Output.

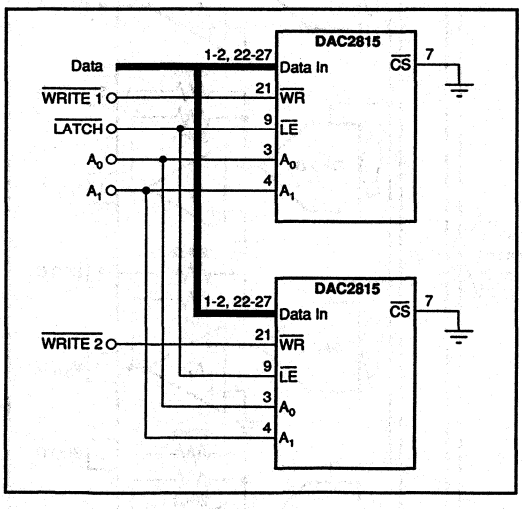


FIGURE 6. Logic Connection for Multiple DAC2815 Packages.

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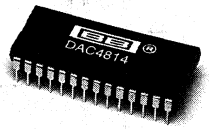


DAC4814

Quad 12-Bit Digital-to-Analog Converter (Serial Interface)

FEATURES

- COMPLETE QUAD DAC — INCLUDES INTERNAL REFERENCES AND OUTPUT AMPLIFIERS
- GUARANTEED SPECIFICATIONS OVER TEMPERATURE
- GUARANTEED MONOTONIC OVER TEMPERATURE
- HIGH-SPEED SERIAL INTERFACE (10MHz CLOCK)
- LOW POWER, 600mW (150mW/DAC)
- LOW GAIN DRIFT, 5ppm/°C
- LOW NONLINEARITY, ±1/2 LSB MAX
- UNIPOLAR OR BIPOLAR OUTPUT
- CLEAR/RESET TO UNIPOLAR OR BIPOLAR ZERO

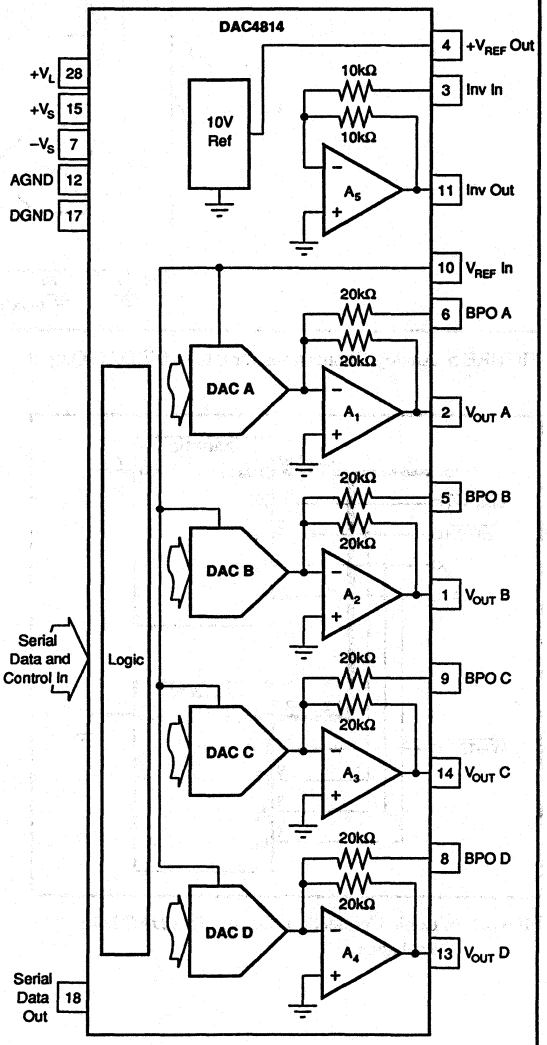
DESCRIPTION

The DAC4814 is one in a family of dual and quad 12-bit digital-to-analog converters. Serial, 8-bit, 12-bit interfaces are available. See back cover for details.

The DAC4814 is complete. It contains CMOS logic, switches, a high-performance buried-zener reference, and low-noise bipolar output amplifiers. No external components are required for either unipolar 0 to 10V, 0 to –10V, or bipolar ±10V output ranges.

The DAC4814 has a high-speed serial interface capable of being clocked at 10MHz. Serial data are clocked DAC D MSB first into a 48-bit shift register, then strobed into each DAC separately or simultaneously as required. The DAC has an asynchronous clear control for reset to unipolar or bipolar zero depending on the mode selected. This feature is useful for power-on reset or system calibration. The DAC4814 is packaged in a 28-pin plastic DIP rated for the –40°C to +85°C extended industrial temperature range.

High-stability laser-trimmed thin film resistors assure high reliability and true 12-bit integral and differential linearity over the full specified temperature range.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS, Guaranteed over T_A = –40°C to +85°C unless otherwise specified.

ELECTRICAL

Specifications as shown for V_S = ±12V or ±15V, V_L = +5V, and R_L = 2kΩ unless otherwise noted.

PARAMETER	CONDITIONS	DAC4814AP MIN	DAC4814AP TYP	DAC4814AP MAX	DAC4814BP MIN	DAC4814BP TYP	DAC4814BP MAX	UNITS
DIGITAL INPUTS								
Resolution		12			*			Bits
V_{IH} (Input High Voltage)		+2		+5	*		*	V
V_{IL} (Input Low Voltage)		0		+0.8	*		*	V
I_{IN} (Input Current)	T_A = 25°C			±1			*	µA
	T_A = –40°C to +85°C			±10			*	µA
C_{IN} (Input Capacitance)			0.8			*		pF
DIGITAL OUTPUT								
Data Out V_{OL}	I_{SINK} = 1.6mA	0		+0.4	*		*	V
V_{OH}	I_{SOURCE} = 500µA	+2.4		+5	*		*	V
ACCURACY								
Integral, Relative Linearity[1]				±1			±1/2	LSB
Differential Nonlinearity[2]	T_A = 25°C			±1			*	LSB
	T_A = –40°C to +85°C		+1.5/–1				±1	LSB
Unipolar Offset Error	T_A = +25°C			±1			±0.5	mV
	T_A = –40°C to +85°C			±3			*	mV
Bipolar Zero Error				±20			±10	mV
Gain Error Unipolar, Bipolar	With Internal or External 10.0V Ref			±0.2			±0.15	%
Power Supply Sensitivity[3]	V_S = ±11.4V to ±18V			30			*	ppmFSR/V
	V_L = +4.5V to +5.5V							
TEMPERATURE DRIFT								
Gain Drift Unipolar, Bipolar			±5	±30		*	±20	ppm/°C
Unipolar Offset Drift			±0.1	±5		*	*	ppmFSR/°C
Bipolar Zero Drift			±5	±15		*	±8	ppmFSR/°C
REFERENCE OUTPUT								
Output Voltage		+9.980	+10	+10.020	+9.985	*	+10.015	V
Reference Drift			±2	±30		*	±20	ppm/°C
Output Current	T_A = 25°C		+10/–5		*			mA
	T_A = –40°C to +85°C		+6.5/–5		*			mA
Max Load Capacitance (For Stability)			500			*		pF
Short Circuit Current			±20			*		mA
Load Regulation				40			*	ppm/mA
(ΔV_{OUT} vs ΔI_{LOAD})								
Supply Regulation				±5			*	ppm/V
(ΔV_{OUT} vs ΔV_S)								
INVERTER								
–10V Reference[4], Inverter Output		–10.020	–10	–9.980	–10.015	*	–9.985	V
–10V Reference Drift				±30			±20	ppm/°C
DC Output Impedance			0.1			*		Ω
Output Current		±7			*			mA
Max Load Capacitance (For Stability)			200			*		pF
Short Circuit Current			±30			*		mA
REFERENCE INPUT								
Reference Input Resistance		1.75	2.5		*	*		kΩ
Inverter Input Resistance		7	10		*	*		kΩ
BPO Input Resistance		14	20		*	*		kΩ
Reference Input Range				±10			*	V
ANALOG SIGNAL OUTPUTS								
Voltage Range		$–V_S$ + 1.4		$+V_S$ – 1.4	*		*	V
DC Output Impedance			0.1			*		Ω
Output Current		±5			*			mA
Max Load Capacitance (For Stability)	V_{OUT}		500			*		pF
Short Circuit Current			±30			*		mA
DYNAMIC PERFORMANCE[5]	C_L = 100pF							
Unipolar Mode Settling Time	To 1/2 LSB of Full Scale		2.5	10		*	*	µs
Bipolar Mode Settling Time	To 1/2 LSB of Full Scale		3.5	10		*	*	µs
Slew Rate			10			*		V/µs
Small-Signal Bandwidth			3			*		MHz
ANALOG GROUND CURRENT								
(Code Dependent)			±4			*		mA
DIGITAL CROSSTALK	Full Scale Transition		3			*		nV-s
	C_L = 100pF							
D-TO-A GLITCH IMPULSE			30			*		nV-s

SPECIFICATIONS (CONT), Guaranteed over T_A = –40°C to +85°C unless otherwise specified.

ELECTRICAL

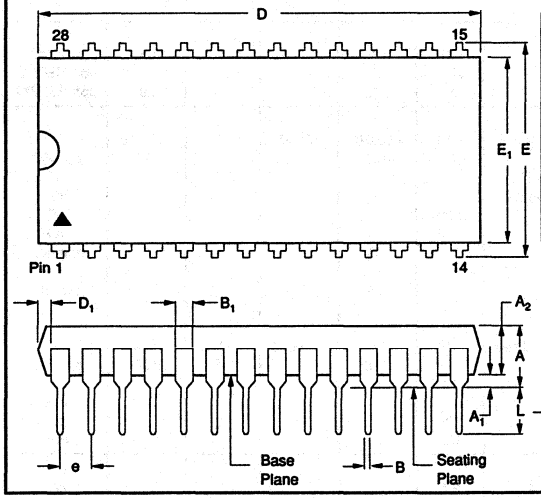
Specifications as shown for V_S = ±12V or ±15V, V_L = +5V, and R_L = 2kΩ unless otherwise noted.

PARAMETER	CONDITIONS	DAC4814AP			DAC4814BP			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
POWER SUPPLY								
$+V_S$ and $-V_S$		±11.4	±15	±18	*	*	*	V
$+V_L$		4.5	5	5.5	*	*	*	V
$+I_S$			+20	+24		*	*	mA
$-I_S$			–20	–25.5		*	*	mA
$+I_L$	Digital Inputs = 0V or $+V_L$		0.4	2		*	*	mA
$+I_L$	Digital Inputs = V_{IL} or V_{IH}			10			*	mA
Total Power, All DACs			600	753		*	*	mW
TEMPERATURE RANGE								
Specified		–40		+85	*		*	°C
Operating		–40		+85	*		*	°C
Thermal Resistance, θ_{JA}			75			*		°C/W

NOTES: (1) End point linearity. (2) Guaranteed monotonic. (3) Change in bipolar full scale output. Includes voltage output DAC, voltage reference, and reference inverter. (4) Inverter output with inverter input connected to $+V_{REF}$. (5) Guaranteed to but not tested.

MECHANICAL

P Package — 28-Pin Plastic, Double-Wide DIP



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.155	.250	3.94	6.35
A_1	.015	.070	.381	1.78
A_2	.140	.185	3.57	4.70
B	.014	.022	.356	.559
B_1	.040	.070	1.02	1.78
C	.008	.015	.20	.381
D	1.435	1.480	36.45	37.59
D_1	.040	.100	1.020	2.540
E	.600	.625	15.24	15.88
E_1	.525	.565	13.34	14.35

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
e	.100 BASIC		2.54 BASIC	
eA	.600 BASIC		15.24 BASIC	
eB	.600	.700	15.24	17.78
L	.115	.200	2.91	5.08

NOTES:
(1) Not JEDEC Standard.
(2) Controlling dimension: INCH.
(3) Dimensioning and tolerancing per ANSI Y14.5M-1982.
(4) Dimensions A, A_1 and L are measured with package seated in JEDEC Seating Plane Gauge GS-3.
(5) D and E_1 does not include mold flash. Mold flash shall not exceed .010 inches, 0.25mm.
(6) eB and eC are measured at the lead tips with the leads unconstrained. eC must be zero or greater.

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

ABSOLUTE MAXIMUM RATINGS

$+V_L$ to AGND	0V, +7V
$+V_L$ to DGND	0V, +7V
$+V_S$ to AGND	0V, +18V
$-V_S$ to AGND	0V,–18V
AGND to DGND	±0.3V
Any digital input to DGND	–0.3V, $+V_L$ +0.3V
Ref In to AGND	±25V
Ref In to DGND	±25V
Storage Temperature Range	–55°C to +125°C
Operating Temperature Range	–40°C to +85°C
Lead Temperature (soldering, 10s)	+300°C
Junction Temperature	+155°C
Output Short Circuit	Continuous to common or $\pm V_S$
Reference Short Circuit	Continuous to common or $+V_S$

ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

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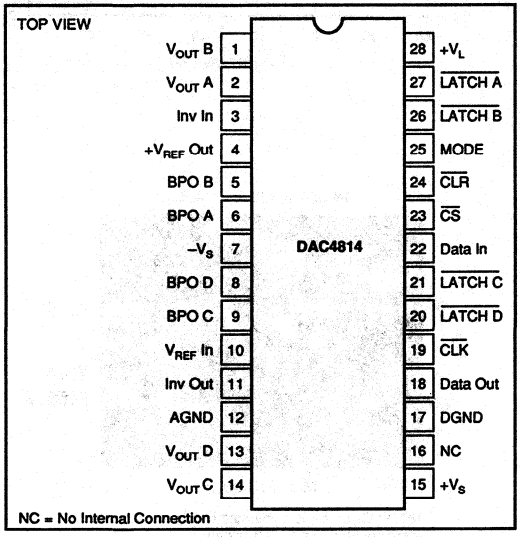
PIN DESIGNATIONS

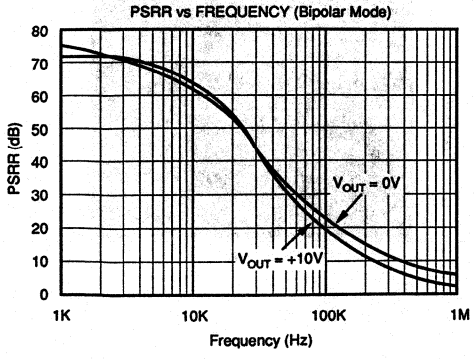
PIN	DESCRIPTOR	FUNCTION	PIN	DESCRIPTOR	FUNCTION
1	V_{OUT} B	Analog output voltage, DAC B	28	$+V_L$	Positive logic power supply, +5V input
2	V_{OUT} A	Analog output voltage, DAC A	27	$\overline{\text{LATCH A}}$	Latch data update, logic input, DAC A
3	Inv In	Inverter (A_2) input	26	$\overline{\text{LATCH B}}$	Latch data update, logic input, DAC B
4	$+V_{REF}$ Out	Positive reference voltage output (+10V output)	25	MODE	Selection input for unipolar or bipolar reset to zero
5	BPO B	Bipolar offset input, DAC B	24	$\overline{\text{CLR}}$	Asynchronous input reset to zero
6	BPO A	Bipolar offset input, DAC A	23	$\overline{\text{CS}}$	Chip select enable, DAC A, B, C, and D
7	$-V_S$	Negative analog power supply , –15V input	22	Data In	Serial data input
8	BPO D	Bipolar offset input, DAC D	21	$\overline{\text{LATCH C}}$	Latch data update, logic input, DAC C
9	BPO C	Bipolar offset input, DAC C	20	$\overline{\text{LATCH D}}$	Latch data update, logic input, DAC D
10	V_{REF} In	± Reference voltage input	19	$\overline{\text{CLK}}$	Clock input
11	Inv Out	Inverter (A_2) output	18	Data Out	Serial data output
12	AGND	Analog common	17	DGND	Digital common
13	V_{OUT} D	Analog output voltage, DAC D	16	NC	No internal connection
14	V_{OUT} C	Analog output voltage, DAC C	15	$+V_S$	Positive analog power supply, +15V input

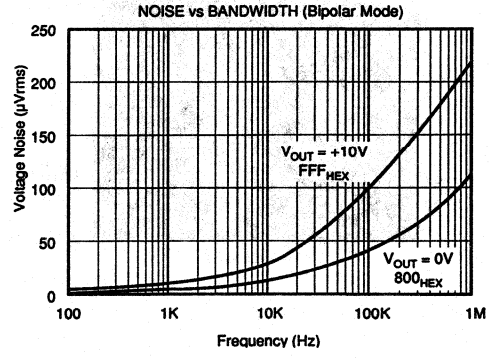
PIN CONFIGURATIONS



TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_S = ±12V or ±15V, V_L = +5V unless otherwise noted.

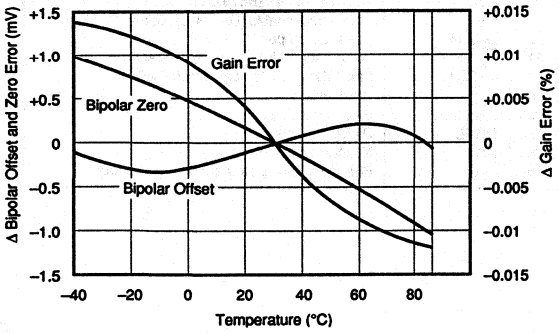




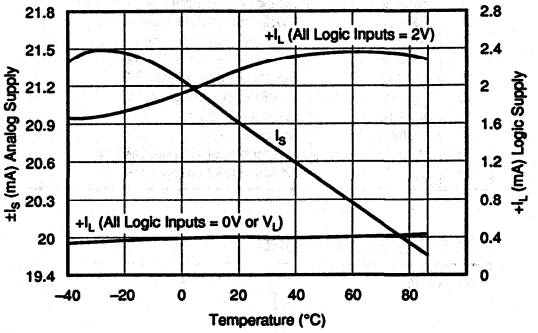
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_S = ±12V or ±15V, V_L = +5V unless otherwise noted.

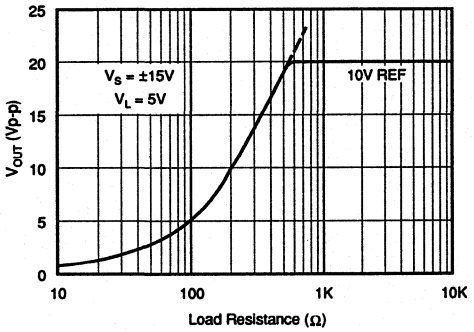
CHANGE OF GAIN, BIPOLAR OFFSET AND ZERO ERROR vs TEMPERATURE



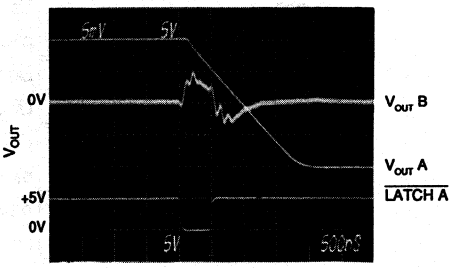
POWER SUPPLY CURRENT vs TEMPERATURE



OUTPUT VOLTAGE SWING vs RESISTOR LOAD



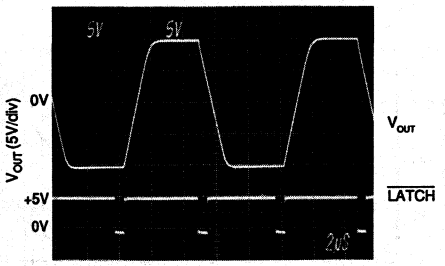
CROSSTALK (Bipolar Mode)



Time (500ns/div)

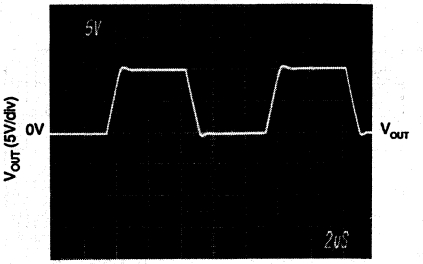
NOTE: Crosstalk is dominated by digital crosstalk/ feedthrough of the $\overline{\text{LATCH}}$ signal.

FULL-SCALE OUTPUT SWING BIPOLAR (20V Step)



Time (2µs/div)

FULL-SCALE OUTPUT SWING UNIPOLAR (10V Step)

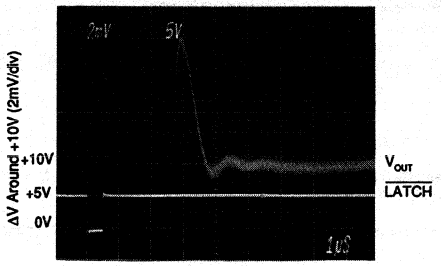


Time (2µs/div)

TYPICAL PERFORMANCE CURVES (CONT)

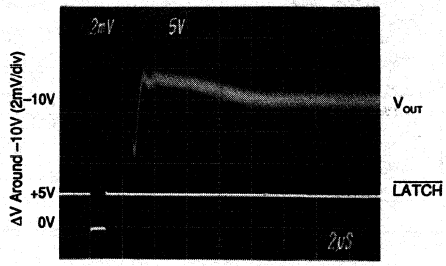
T_A = +25°C, V_S = ±12V or ±15V, V_L = +5V unless otherwise noted.

SETTLING TIME
BIPOLAR (–10V to +10V)



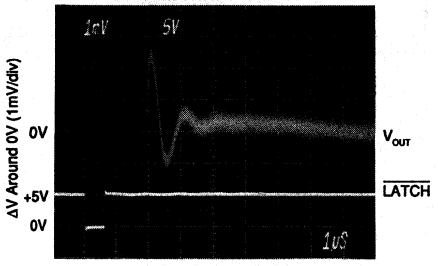
Time (1µs/div)

SETTLING TIME
BIPOLAR (+10V to –10V Step)



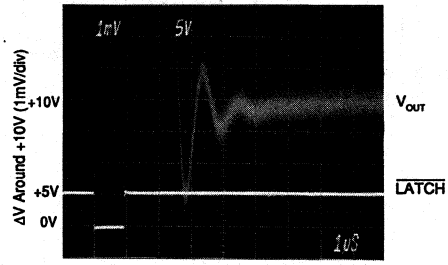
Time (2µs/div)

SETTLING TIME
UNIPOLAR (+10V to 0V STEP)



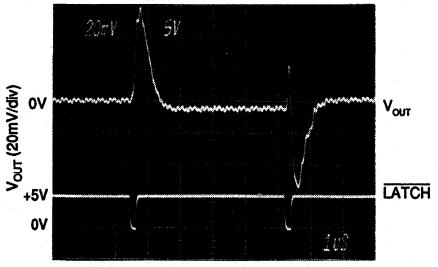
Time (1µs/div)

SETTLING TIME
UNIPOLAR (0V to +10V Step)



Time (1µs/div)

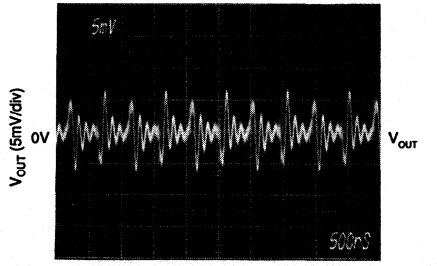
MAJOR CARRY GLITCH



Time (1µs/div)

NOTE: Data transition 800_{HEX} to $7FF_{HEX}$.

DIGITAL FEEDTHROUGH



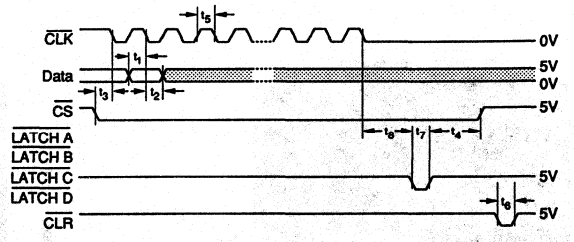
Time (500ns/div)

DAC output noise due to activity on digital inputs with latch disabled.

TIMING CHARACTERISTICS

V_S = ±15V, V_L = +5V, T_A = –40°C to +85°C.

PARAMETER	MINIMUM
t_1—Data Setup Time	15ns
t_2—Data Hold Time	15ns
t_3—Chip Select to $\overline{CLK}$, Latch, Data Setup Time	15ns
t_4—Chip Select to $\overline{CLK}$, Latch, Data Hold Time	40ns
t_5—$\overline{CLK}$ Pulse Width	40ns
t_6—Clear Pulse Width	40ns
t_7—Latch Pulse Width	40ns
t_8—$\overline{CLK}$ Edge to $\overline{LATCH\ A}$, $\overline{LATCH\ B}$, $\overline{LATCH\ C}$, or $\overline{LATCH\ D}$	15ns



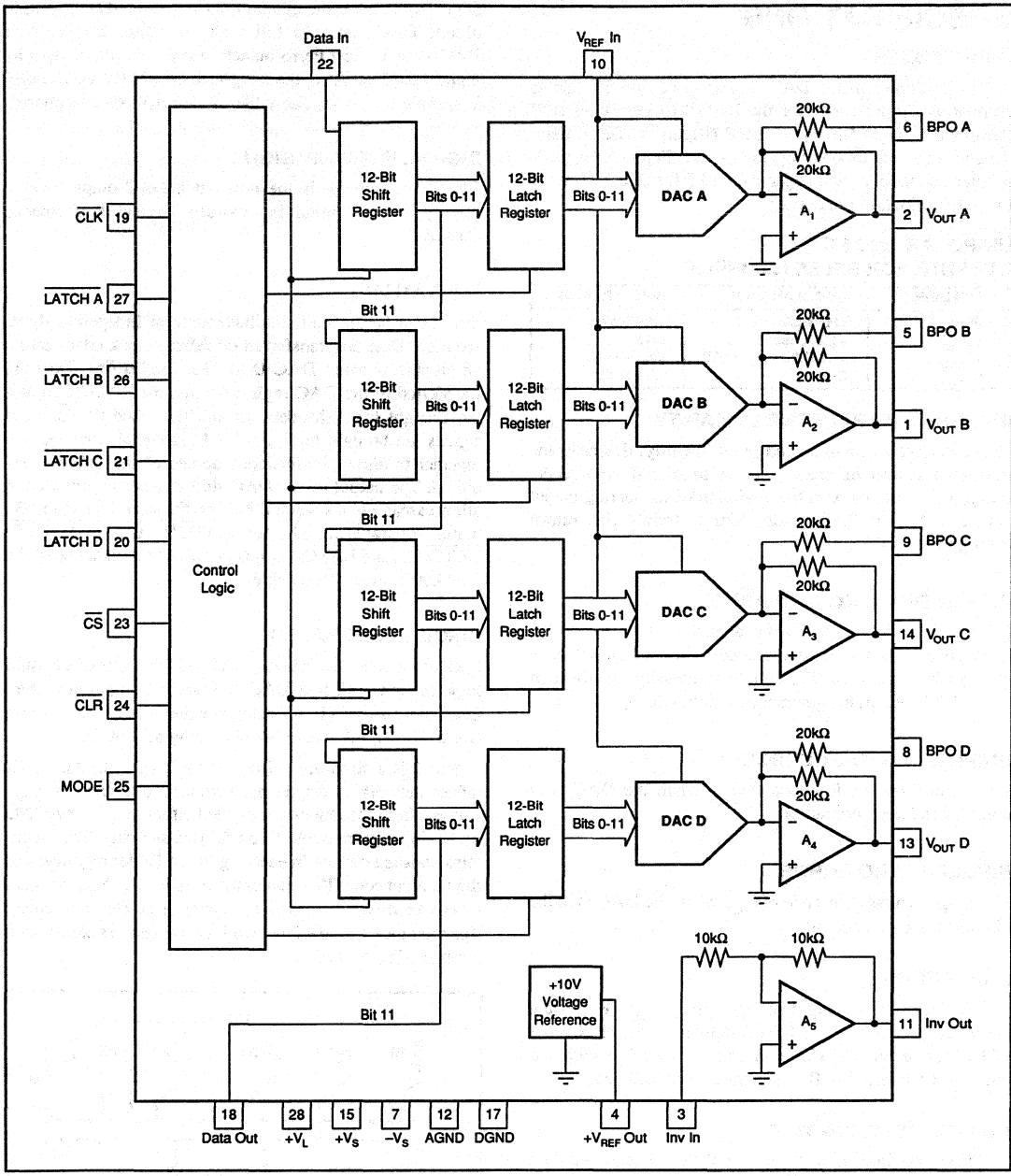
NOTES: (1) All input signal rise and fall times are measured from 10% to 90% of +5V. $t_R = t_F$ = 5ns.
(2) Timing measurement reference level is $\frac{V_{IH} + V_{IL}}{2}$.

INTERFACE LOGIC TRUTH TABLE

MODE	$\overline{CLR}$	$\overline{CLK}$	$\overline{CS}$	$\overline{LATCH\ A}$	$\overline{LATCH\ B}$	$\overline{LATCH\ C}$	$\overline{LATCH\ D}$	FUNCTION
X	1	↓	0	X	X	X	X	Data clocked in
X	1	X	1	X	X	X	X	No data transfer
X	1	X	0	0	1	1	1	DAC A register updated
X	1	X	0	1	0	1	1	DAC B register updated
X	1	X	0	1	1	0	1	DAC C register updated
X	1	X	0	1	1	1	0	DAC D register updated
X	1	X	0	0	0	0	0	All DAC registers updated simultaneously
0	0	X	X	X	X	X	X	All registers cleared
1	0	X	X	X	X	X	X	Shift registers cleared, DAC registers = 800_{HEX}

Note: X = Don't Care. ↓ = Falling edge triggered.

FUNCTIONAL BLOCK DIAGRAM, DAC4814 — Quad 12-bit DAC, Serial Port



DISCUSSION OF SPECIFICATIONS

INPUT CODES

All digital inputs of the DAC4814 are TTL and 5V CMOS compatible. Input codes for the DAC4814 are either USB (Unipolar Straight Binary) or BOB (Bipolar Offset Binary) depending on the mode of operation. See Figure 3 for ±10V bipolar connection. See Figures 4 and 5 for 0 to 10V and 0 to –10V unipolar connections.

UNIPOLAR AND BIPOLAR OUTPUTS FOR SELECTED INPUT

DIGITAL INPUT	UNIPOLAR (USB)	BIPOLAR (BOB)
FFF_{HEX}	+Full scale	+Full scale
800_{HEX}	+1/2 Full scale	Zero
$7FF_{HEX}$	+1/2 Full scale – 1 LSB	Zero – 1 LSB
000_{HEX}	Zero	–Full scale

INTEGRAL OR RELATIVE LINEARITY

This term, also known as end point linearity, describes the transfer function of analog output to digital input code. Integral linearity error is the deviation of the analog output versus code transfer function from a straight line drawn through the end points.

DIFFERENTIAL NONLINEARITY

Differential nonlinearity is the deviation from an ideal 1 LSB change in the output voltage when the input code changes by 1 LSB. A differential nonlinearity specification of ±1 LSB maximum guarantees monotonicity.

UNIPOLAR OFFSET ERROR

The output voltage for code 000_{HEX} when the DAC is in unipolar mode of operation.

BIPOLAR ZERO ERROR

The output voltage for code 800_{HEX} when the DAC is in the bipolar mode of operation.

GAIN ERROR

The deviation of the output voltage span ($V_{MAX} - V_{MIN}$) from the ideal span of 10V – 1 LSB (unipolar mode) or 20V – 1 LSB (bipolar mode). The gain error is specified with and without the internal +10V reference error included.

OUTPUT SETTLING TIME

The time required for the output voltage to settle within a percentage-of-full-scale error band for a full scale transition. Settling to ±0.012% (1/2 LSB) is specified for the DAC4814.

DIGITAL-TO-ANALOG GLITCH

Ideally, the DAC output would make a clean step change in response to an input code change. In reality, glitches occur during the transition. See Typical Performance Curves.

DIGITAL CROSSTALK

Digital crosstalk is the glitch impulse measured at the output of one DAC due to a full scale transition on the other DAC—see Typical Performance Curves. It is dominated by digital coupling. Also, the integrated area of the glitch pulse is specified in nV–s. See table of electrical specifications.

DIGITAL FEEDTHROUGH

Digital feedthrough is the noise at a DAC output due to activity on the digital inputs—see Typical Performance Curves.

OPERATION

DACs can be updated simultaneously or independently as required. Data are transferred on falling clock edges into a 48-bit shift register. DAC D MSB is loaded first. Data are transferred to the DAC registers when the $\overline{\text{LATCH}}$ signals are brought low. The data are latched when the $\overline{\text{LATCH}}$ signals are brought high. All $\overline{\text{LATCH}}$ signals may be tied together to allow simultaneous update of the DACs if required. The output of the DAC shift register is provided to allow cascading of several DACS on the same bit stream. By using separate signals for $\overline{\text{LATCH A}}$, $\overline{\text{LATCH B}}$, $\overline{\text{LATCH C}}$, and $\overline{\text{LATCH D}}$ it is possible to update one of the four DACs every 12 clock cycles.

CIRCUIT DESCRIPTION

Each of the four DACs in the DAC4814 consists of a CMOS logic section, a CMOS DAC cell, and an output amplifier. One buried-zener +10.0V reference and a reference inverter (for a –10.0V reference) are shared by all DACs.

Figure 1 is a simplified circuit for a DAC cell. An R, 2R ladder network is driven by a voltage reference at V_{REF}. Current from the ladder is switched either to I_{OUT} or AGND by 12 single-pole double-throw CMOS switches. This maintains constant current in each leg of the ladder regardless of digital input code. This makes the resistance at V_{REF} constant (it can be driven by either a voltage or current reference). The reference can be either positive or negative polarity with a range of up to ±10V.

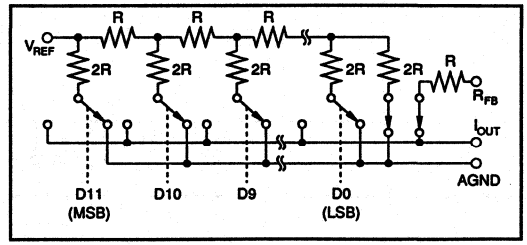


FIGURE 1. Simplified Circuit Diagram of DAC Cell.

CMOS switches included in series with the ladder terminating resistor and the feedback resistor, R_{FB}, compensate for the temperature drift of the ladder switch ON resistance.

The output op amps are connected as transimpedance amplifiers to convert the DAC-cell output current into an output voltage. They have been specially designed and compensated for precision and fast settling in this application.

POWER SUPPLY CONNECTIONS

The DAC4814 is specified for operation with power supplies of V_L = +5V and V_S = either ±12V or ±15V. Even with the V_S supplies at ±11.4V the DACs can swing a full ±10V. Power supply decoupling capacitors (1µF tantalum) should be located close to the DAC power supply connections.

Separate digital and analog ground pins are provided to permit separate current returns. They should be connected together at one point. Proper layout of the two current returns will prevent digital logic switching currents from degrading the analog output signal. The analog ground current is code dependent so the impedance to the system reference ground must be kept to a minimum. Connect DACs as shown in Figure 2 or use a ground plane to keep ground impedance less than 0.1Ω for less than 0.1LSB error.

–10V REFERENCE

An internal inverting amplifier (Gain = –1.0V/V) is provided to invert the +10V reference. Connect $+V_{REF}$ Out to Inv In for a –10V reference at Inv Out.

OUTPUT RANGE CONNECTIONS

±10V Output Range

For a ±10V bipolar output connect the DAC4814 as shown in Figure 3. Connect the MODE to logic high (+5V) for reset to bipolar zero. With MODE connected low (GND) reset will be to –Full-Scale.

0 To +10V Output Range

For 0 to +10V unipolar outputs connect the DAC4814 as shown in Figure 4. Connect the MODE to logic low (GND) for reset to unipolar zero.

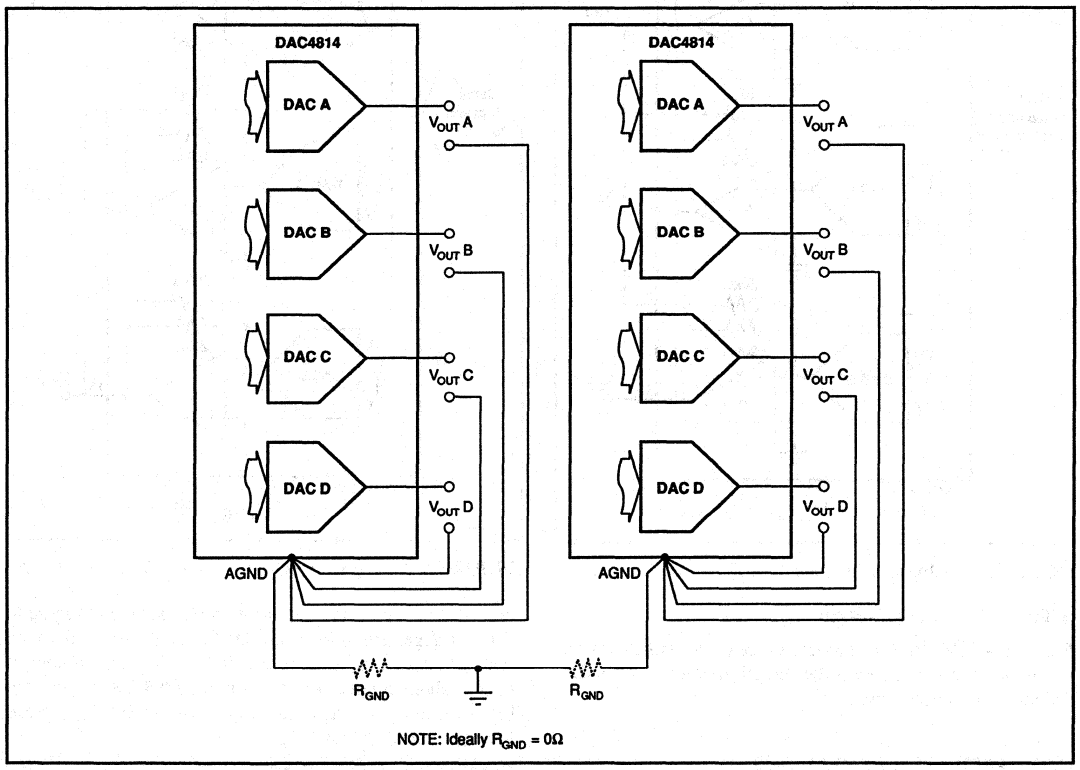


FIGURE 2. Recommended Ground Connections for Multiple DAC Packages.

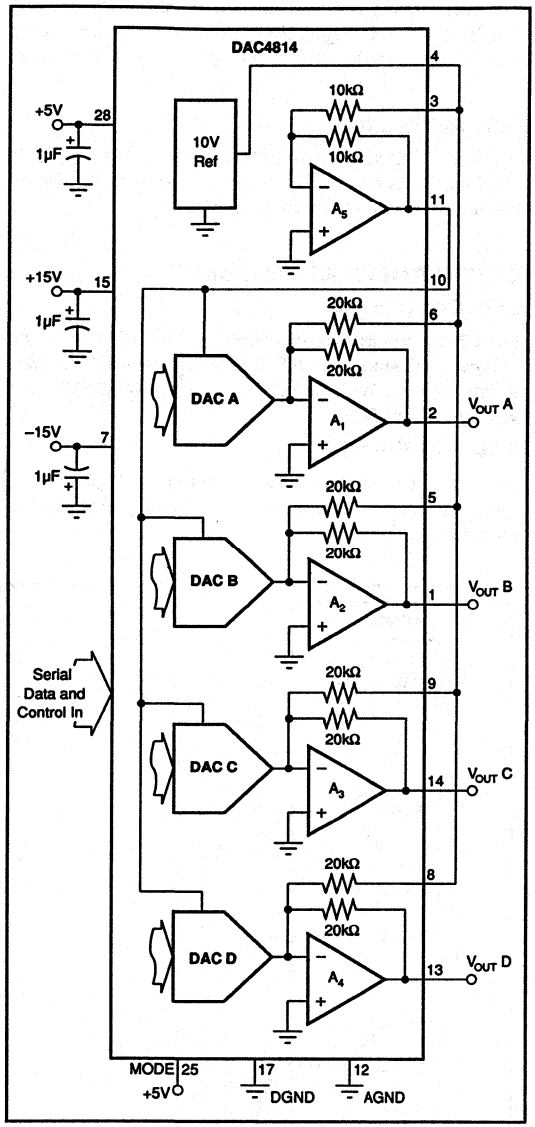


FIGURE 3. Analog Connections for ±10V DAC Output.

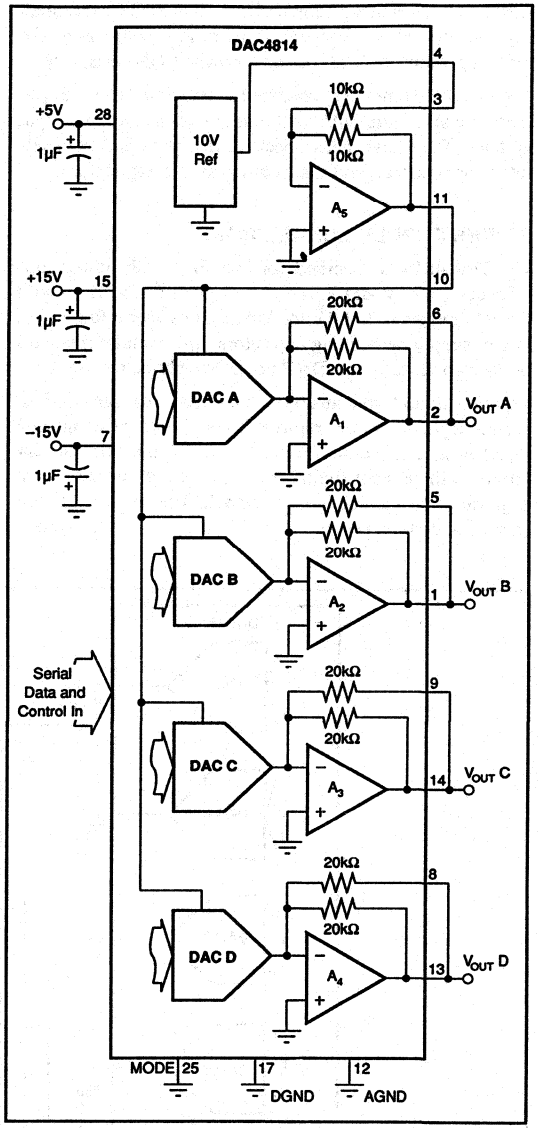


FIGURE 4. Analog Connections for 0 to +10V DAC Output.

0 To −10V Output Range

For 0 to −10V unipolar outputs connect the DAC4814 as shown in Figure 5. Connect the MODE to logic low (GND) for reset to unipolar zero.

CONNECTION TO DIGITAL BUS

Cascaded Bus Connection

Multiple DAC4814s can be connected to the same $\overline{CLK}$ and DATA input lines in two ways. Since the output of the DAC shift register is available, any number of DAC4814s can be cascaded on the same input bit stream as shown in Figure 6. This arrangement allows all DACs in the system to be updated simultaneously and requires a minimum number of control signal inputs. However, up to 48N $\overline{CLK}$ cycles may be required to update any given DAC, where N = number of DAC4814s.

Parallel Bus Connection

Several DAC4814s can also have their DATA inputs connected in parallel as shown in Figure 7. This allows any DAC in the system to be updated in a maximum of 48 $\overline{CLK}$ cycles.

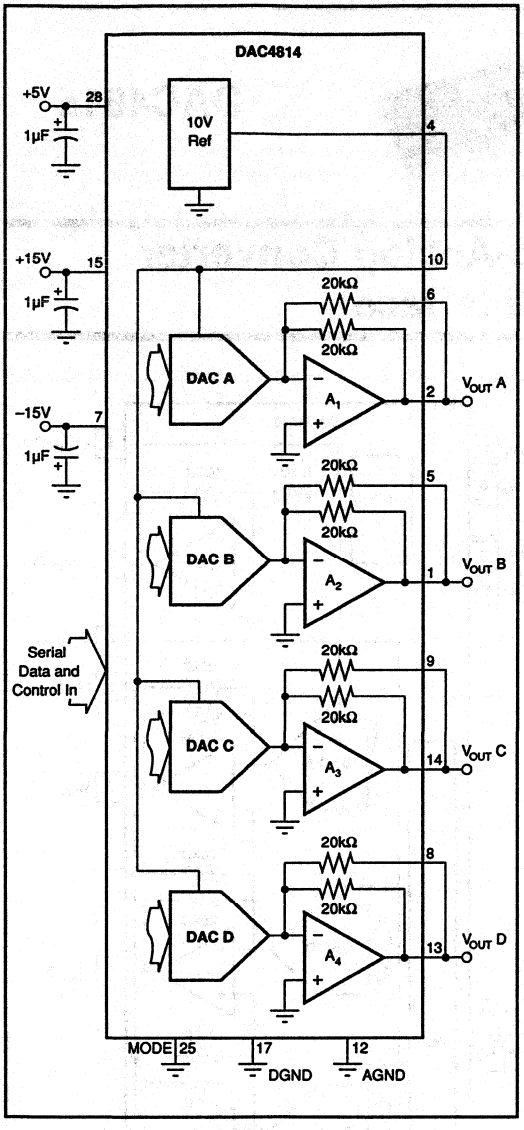


FIGURE 5. Analog Connections for 0 to –10V DAC Output.

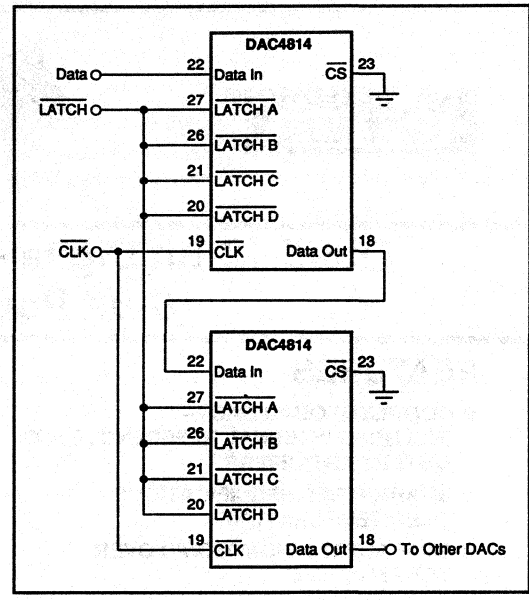


FIGURE 6. Cascaded Serial Bus Connection for Multiple DAC Packages.

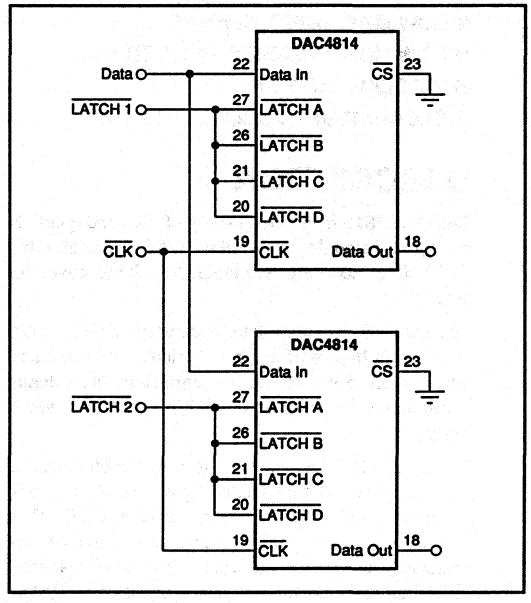


FIGURE 7. Parallel Bus Connection for Multiple DAC Packages.

For Immediate Assistance, Contact Your Local Salesperson

BURR-BROWN®

DAC4815

Quad 12-Bit Digital-to-Analog Converter (8-Bit Port Interface)

FEATURES

- COMPLETE QUAD DAC — INCLUDES INTERNAL REFERENCES AND OUTPUT AMPLIFIERS
- GUARANTEED SPECIFICATIONS OVER TEMPERATURE
- GUARANTEED MONOTONIC OVER TEMPERATURE
- HIGH-SPEED 8 + 4-BIT PARALLEL INTERFACE
- LOW POWER, 600mW (150mW/DAC)
- LOW GAIN DRIFT, 5ppm/°C
- LOW NONLINEARITY, ±1/2 LSB MAX
- BIPOLAR OUTPUT
- CLEAR/RESET TO BIPOLAR ZERO

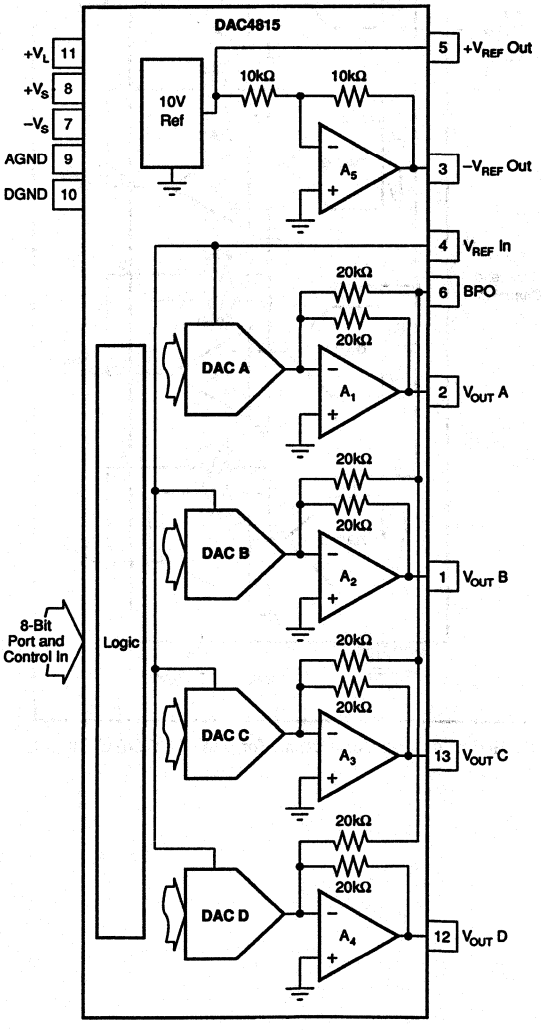
DESCRIPTION

The DAC4815 is one in a family of dual and quad 12-bit digital-to-analog converters (DACs). Serial, 8-bit, 12-bit interfaces are available. See back cover for details.

The DAC4815 is complete. It contains CMOS logic, switches, a high-performance buried-zener reference, and low-noise bipolar output amplifiers. No external components are required for bipolar ±10V output range.

The DAC4815 has a 2-byte (8 + 4) double-buffered interface. Data is first loaded (level transferred) into the input registers in two steps for each DAC. Then both DACs are updated simultaneously. The DAC has an asynchronous clear control for reset to bipolar zero. This feature is useful for power-on reset or system calibration. The DAC4815 is packaged in a 28-pin plastic DIP rated for the –40°C to +85°C extended industrial temperature range.

High-stability laser-trimmed thin film resistors assure high reliability and true 12-bit integral and differential linearity over the full specified temperature range.



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Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS, Guaranteed over T_A = –40°C to +85°C unless otherwise specified.

ELECTRICAL

Specifications as shown for V_S = ±12V or ±15V, V_L = +5V, and R_L = 2kΩ unless otherwise noted.

PARAMETER	CONDITIONS	DAC4815AP			DAC4815BP			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
DIGITAL INPUTS								
Resolution		12			•			Bits
V_{IH} (Input High Voltage)		2		5	•		•	V
V_{IL} (Input Low Voltage)		0		0.8	•		•	V
I_{IN} (Input Current)	T_A = 25°C			±1			•	µA
	T_A = –40°C to +85°C			±10			•	µA
C_{IN} (Input Capacitance)			0.8			•		pF
ACCURACY								
Integral, Relative Linearity[1]				±1			±1/2	LSB
Differential Nonlinearity[2]	T_A = 25°C			±1			•	LSB
	TA = –40°C to +85°C		±1.5/–1				±1	LSB
Bipolar Zero Error			±20			±10	mV	
Gain Error	With Internal or External 10.0V Ref			±0.2			±0.15	%
Power Supply Sensitivity[3]	V_S = ±11.4V to ±18V			30			•	ppmFSR/V
	V_L = +4.5V to +5.5V							
TEMPERATURE DRIFT								
Gain Drift			±5	±30		•	±20	ppm/°C
Bipolar Zero Drift			±5	±15		•	±8	ppmFSR/°C
REFERENCE OUTPUT								
Output Voltage		+9.980	+10	+10.020	+9.985	•	+10.015	V
Reference Drift			±2	±30		•	±20	ppm/°C
Output Current	T_A = 25°C	+10/–5			•			mA
	T_A = –40°C to +85°C	+5/–5			•			mA
Max Load Capacitance (For Stability)			500			•		pF
Short Circuit Current			±20			•		mA
Load Regulation				40			•	ppm/mA
(ΔV_{OUT} vs ΔI_{LOAD})								
Supply Regulation				±5			•	ppm/V
(ΔV_{OUT} vs ΔV_S)								
–REFERENCE OUTPUT, Inverter								
–10V Reference		–10.020	–10	–9.980	–10.015	•	–9.985	V
–10V Reference Drift				±30			±20	ppm/°C
DC Output Impedance			0.1			•		Ω
Output Current		±7			•			mA
Max Load Capacitance (For Stability)			200			•		pF
Short Circuit Current			30			•		mA
REFERENCE INPUT								
Reference Input Resistance		1.75	2.5		•	•		kΩ
Inverter Input Resistance		7	10		•	•		kΩ
BPO Input Resistance		3.5	5		•	•		kΩ
Reference Input Range				±10			•	V
ANALOG SIGNAL OUTPUTS								
Voltage Range		$–V_S$ + 1.4		$+V_S$ – 1.4	•		•	V
DC Output Impedance			0.1			•		Ω
Output Current		±5			•			mA
Max Load Capacitance (For Stability)	V_{OUT}		500			•		pF
Short Circuit Current			±30			•		mA
DYNAMIC PERFORMANCE[4]	C_L = 100pF							
Settling Time	To 1/2 LSB of Full Scale		3.5	10		•	•	µs
Slew Rate			10			•		V/µs
Small-Signal Bandwidth			3			•		MHz
ANALOG GROUND CURRENT								
(Code Dependent)			±4			•		mA
DIGITAL CROSSTALK	Full Scale Transition		3			•		nV-s
	C_L = 100pF							
D-TO-A GLITCH IMPULSE						•		nV-s
			30					
POWER SUPPLY								
$+V_S$ and $–V_S$		±11.4	±15	±18	•	•	•	V
$+V_L$		4.5	5	5.5	•	•	•	V
$+I_S$			+20	+24		•	•	mA
$–I_S$			–20	–25.5		•	•	mA
$+I_L$	Digital Inputs = 0V or $+V_L$		0.4	2		•	•	mA
$+I_L$	Digital Inputs = V_{IL} or V_{IH}			10			•	mA
Total Power, All DACs			600	753		•	•	mW

SPECIFICATIONS (CONT), Guaranteed over T_A = –40°C to +85°C unless otherwise specified.

ELECTRICAL

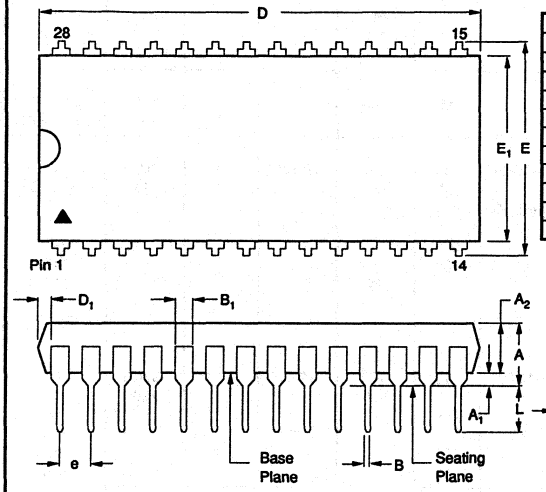
Specifications as shown for V_S = ±12V or ±15V, V_L = +5V, and R_L = 2kΩ unless otherwise noted.

PARAMETER	CONDITIONS	DAC4815AP			DAC4815BP			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
TEMPERATURE RANGE								
Specified		–40		+85	•		•	°C
Operating		–40		+85	•		•	°C
Thermal Resistance, θ_{JA}			75			•		°C/W

NOTES: (1) End point linearity. (2) Guaranteed monotonic. (3) Change in bipolar full scale output. Includes effect of voltage output DAC, voltage references. (4) Guaranteed but not tested.

MECHANICAL

P Package — 28-Pin Plastic, Double-Wide DIP



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.155	.250	3.94	6.35
A_1	.015	.070	.381	1.78
A_2	.140	.185	3.57	4.70
B	.014	.022	.356	.559
B_1	.040	.070	1.02	1.78
C	.008	.015	.20	.381
D	1.435	1.480	36.45	37.59
D_1	.040	.100	1.020	2.540
E	.600	.625	15.24	15.88
E_1	.525	.565	13.34	14.35

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
e	.100 BASIC		2.54 BASIC	
eA	.600 BASIC		15.24 BASIC	
eB	.600	.700	15.24	17.78
L	.115	.200	2.91	5.08

NOTES:
(1) Not JEDEC Standard.
(2) Controlling dimension: INCH.
(3) Dimensioning and tolerancing per ANSI Y14.5M-1982.
(4) Dimensions A, A_1 and L are measured with package seated in JEDEC Seating Plane Gauge GS-3.
(5) D and E_1 does not include mold flash. Mold flash shall not exceed .010 inches, 0.25mm.
(6) eB and eC are measured at the lead tips with the leads unconstrained. eC must be zero or greater.

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

ABSOLUTE MAXIMUM RATINGS

$+V_L$ to AGND	0V, +7V
$+V_L$ to DGND	0V, +7V
$+V_S$ to AGND	0V, +18V
$-V_S$ to AGND	0V, –18V
AGND to DGND	±0.3V
Any digital input to GND	–0.3V, $+V_L$ +0.3V
Ref In to AGND	±25V
Ref In to DGND	±25V
Storage Temperature Range	–55°C to +125°C
Operating Temperature Range	–40°C to +85°C
Lead Temperature (soldering, 10s)	+300°C
Junction Temperature	+155°C
Output Short Circuit	Continuous to common or $\pm V_S$
Reference Short Circuit	Continuous to common or $+V_S$

ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

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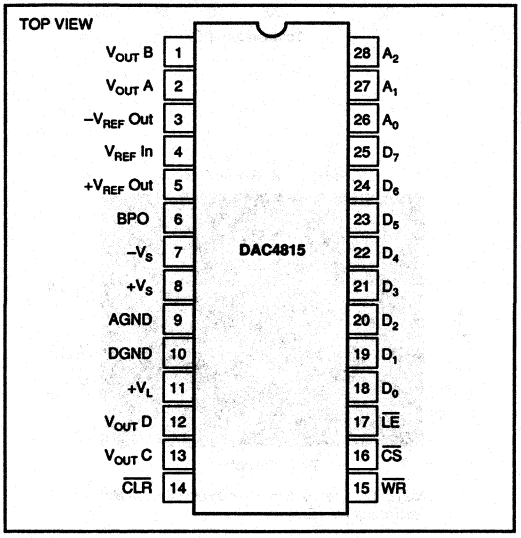
PIN DESIGNATIONS

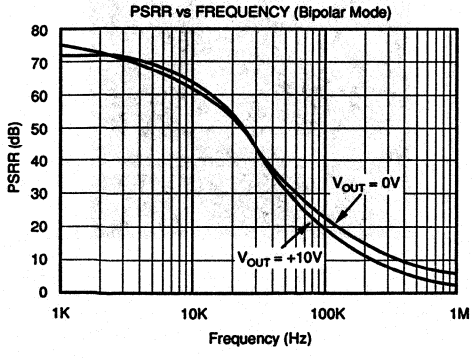
PIN	DESCRIPTOR	FUNCTION	PIN	DESCRIPTOR	FUNCTION
1	V_{OUT} B	Analog output voltage, DAC B	28	A_2	Address line 2 input
2	V_{OUT} A	Analog output voltage, DAC A	27	A_1	Address line 1 input
3	$-V_{REF}$ Out	Negative reference voltage output (–10V output)	26	A_0	Address line 0 input
4	V_{REF} In	± Reference voltage input	25	D_7	Data bit 7 input
5	$+V_{REF}$ Out	Positive reference voltage output (+10V output)	24	D_6	Data bit 6 input
6	BPO	Bipolar offset input, DAC A, B, C, and D	23	D_5	Data bit 5 input
7	$-V_S$	Negative analog power supply, –15V input	22	D_4	Data bit 4 input
8	$+V_S$	Positive analog power supply, +15V input	21	D_3	Data bit 3 input
9	AGND	Analog common	20	D_2	Data bit 2 input
10	DGND	Digital common	19	D_1	Data bit 1 input
11	$+V_L$	Positive logic power supply, +5V input	18	D_0	Data bit 0 input
12	V_{OUT} D	Analog output voltage, DAC D	17	$\overline{LE}$	Latch data enable, DAC A, B, C, and D
13	V_{OUT} C	Analog output voltage, DAC C	16	$\overline{CS}$	Chip select enable, DAC A, B, C, and D
14	$\overline{CLR}$	Asynchronous input reset to zero	15	$\overline{WR}$	Write input, DAC A, B, C, and D

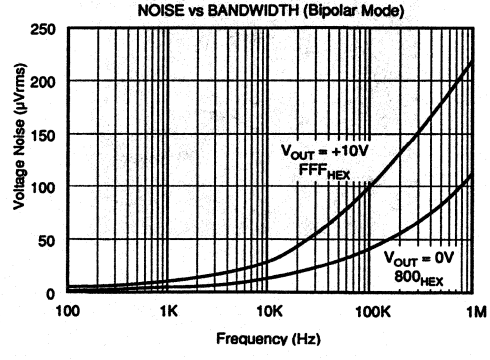
PIN CONFIGURATIONS



TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_S = ±12V or ±15V, V_L = +5V unless otherwise noted.

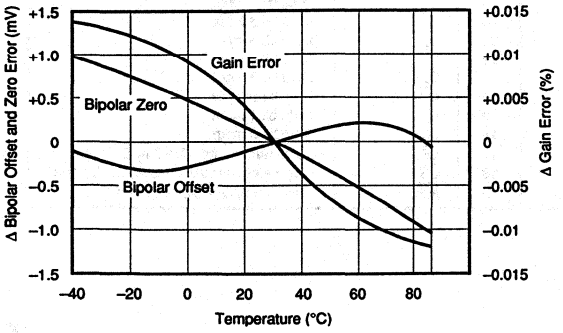




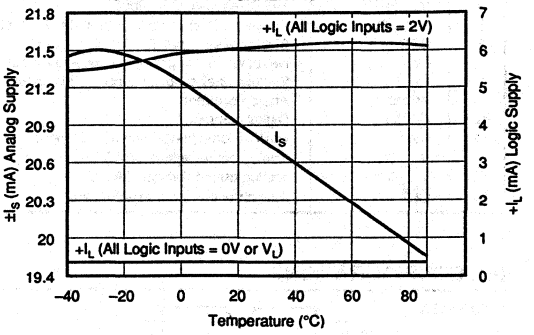
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_S = ±12V or ±15V, V_L = +5V unless otherwise noted.

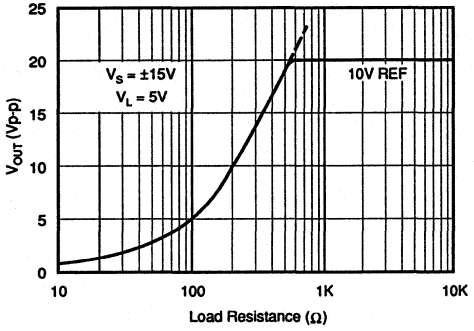
CHANGE OF GAIN, BIPOLAR OFFSET AND ZERO ERROR vs TEMPERATURE



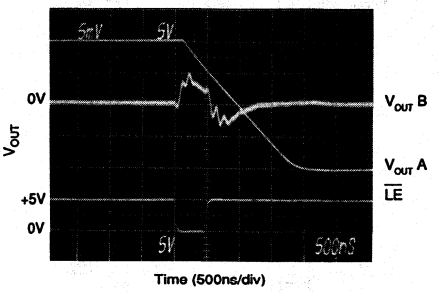
POWER SUPPLY CURRENT vs TEMPERATURE



OUTPUT VOLTAGE SWING vs RESISTOR LOAD

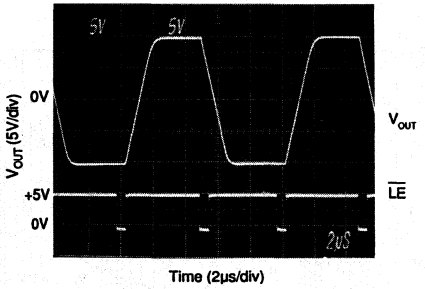


CROSSTALK (Bipolar Mode)

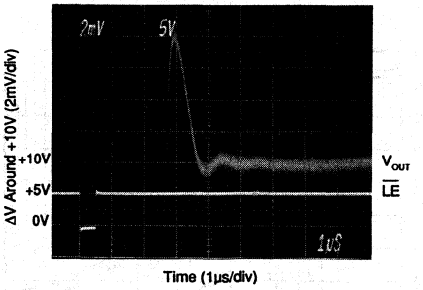


NOTE: Crosstalk is dominated by digital crosstalk/ feedthrough of $\overline{LE}$ signal.

FULL-SCALE OUTPUT SWING BIPOLAR (20V Step)



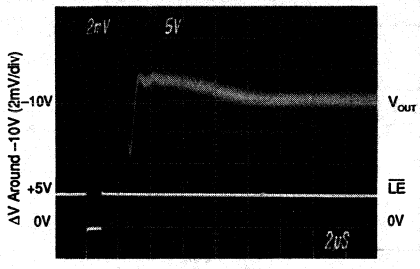
SETTLING TIME BIPOLAR (–10V to +10V)



TYPICAL PERFORMANCE CURVES (CONT)

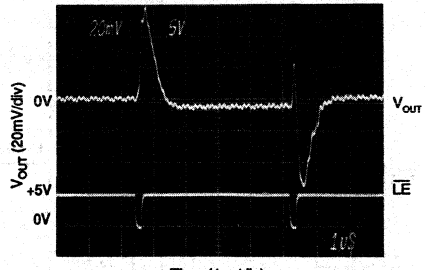
T_A = +25°C, V_S = ±12V or ±15V, V_L = +5V unless otherwise noted.

SETTLING TIME
BIPOLAR (+10V to –10V Step)



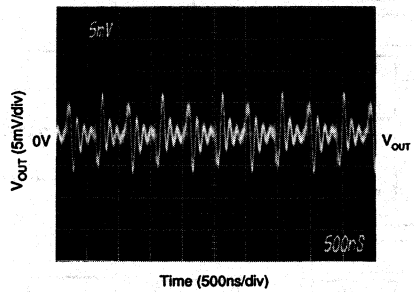
Time (2µs/div)

MAJOR CARRY GLITCH



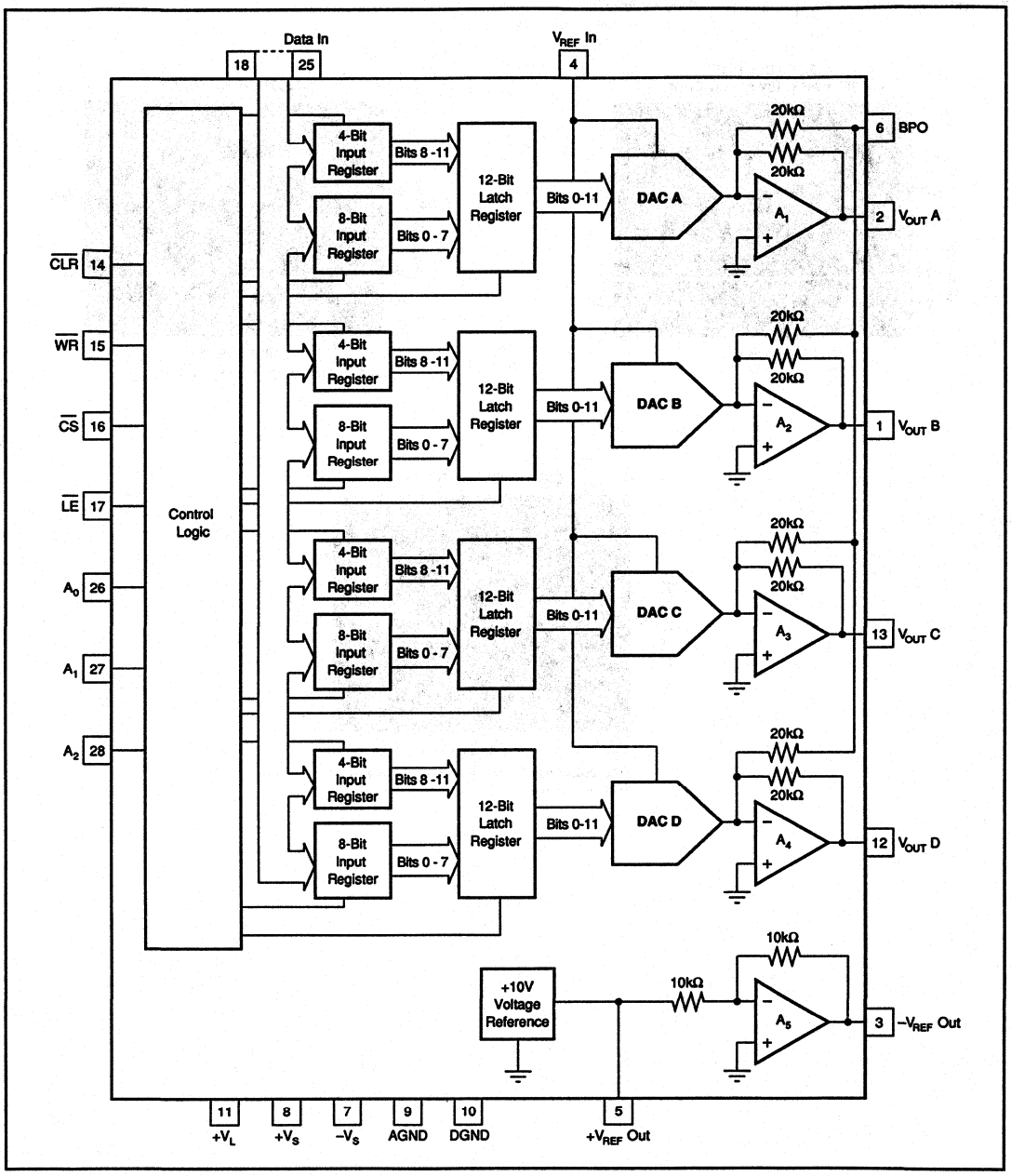
Time (1µs/div)
NOTE: Data transition 800_{HEX} to $7FF_{HEX}$.

DIGITAL FEEDTHROUGH



Time (500ns/div)
DAC output noise due to activity on digital inputs with latch disabled.

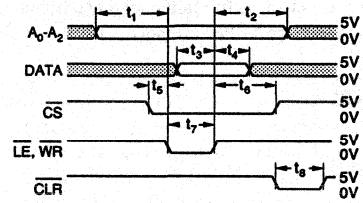
FUNCTIONAL BLOCK DIAGRAM, DAC4815 — Quad 12-bit DAC, 8-bit Port



TIMING CHARACTERISTICS

$+V_L$ = +5V, T_A = –40°C to +85°C.

PARAMETER	MINIMUM
t_1—Address Valid to Write Setup Time	20ns
t_2—Address Valid to Write Hold Time	10ns
t_3—Data Setup Time	30ns
t_4—Data Hold Time	10ns
t_5—Chip Select to $\overline{LE}$ or Write Setup Time	0ns
t_6—Chip Select to $\overline{LE}$ or Write Hold Time	0ns
t_7—Write Pulse Width	40ns
t_8—Clear Pulse Width	40ns



NOTES: (1) All input signal rise and fall times are measured from 10% to 90% of +5V. $t_R = t_F$ = 5ns.
(2) Timing measurement reference level is $\frac{V_{IH} + V_{IL}}{2}$.

INTERFACE LOGIC TRUTH TABLE

$\overline{CLR}$	$\overline{LE}$	$\overline{CS}$	$\overline{WR}$	A_2	A_1	A_0	FUNCTION
1	1	0	0	0	0	0	DAC A LS input register loaded with D7-D0(LSB)
1	1	0	0	0	0	1	DAC A MS input register loaded with D3(MSB)-D0
1	1	0	0	0	1	0	DAC B LS input register loaded with D7-D0(LSB)
1	1	0	0	0	1	1	DAC B MS input register loaded with D3(MSB)-D0
1	1	0	0	1	0	0	DAC C LS input register loaded with D7-D0(LSB)
1	1	0	0	1	0	1	DAC C MS input register loaded with D3(MSB)-D0
1	1	0	0	1	1	0	DAC D LS input register loaded with D7-D0(LSB)
1	1	0	0	1	1	1	DAC D MS input register loaded with D3(MSB)-D0
1	0	0	1	X	X	X	All DAC registers updated simultaneously from input registers
1	0	0	0	X	X	X	All DAC registers are transparent
1	X	1	X	X	X	X	No data transfer
1	1	X	1	X	X	X	No data transfer
0	X	X	X	X	X	X	Input registers cleared, DAC registers = 800_{HEX}

NOTE: X = Don't care.

DISCUSSION OF SPECIFICATIONS

INPUT CODES

All digital inputs of the DAC4815 are TTL and 5V CMOS compatible. Input codes for the DAC4815 are BOB (Bipolar Offset Binary). See Figure 3 for ±10V bipolar connection.

BIPOLAR OUTPUTS FOR SELECTED INPUT

DIGITAL INPUT	BIPOLAR (BOB)
FFF_{HEX}	+Full Scale
800_{HEX}	Zero
$7FF_{HEX}$	Zero – 1 LSB
000_{HEX}	–Full Scale

INTEGRAL OR RELATIVE LINEARITY

This term, also know as end point linearity, describes the transfer function of analog output to digital input code. Integral linearity error is the deviation of the analog output versus code transfer function from a straight line drawn through the end points.

DIFFERENTIAL NONLINEARITY

Differential nonlinearity is the deviation from an ideal 1 LSB change in the output voltage when the input code changes by 1 LSB. A differential nonlinearity specification of ±1 LSB maximum guarantees monotonicity.

BIPOLAR ZERO ERROR

The output voltage for code 800_{HEX}.

GAIN ERROR

The deviation of the output voltage span ($V_{MAX} - V_{MIN}$) from the ideal span of 20V – 1 LSB (bipolar mode). The gain error is specified with and without the internal +10V reference error included.

OUTPUT SETTLING TIME

The time required for the output voltage to settle within a percentage-of-full-scale error band for a full scale transition. Settling to ±0.012% (1/2 LSB) is specified for the DAC4815.

DIGITAL-TO-ANALOG GLITCH

Ideally, the DAC output would make a clean step change in response to an input code change. In reality, glitches occur during the transition. See Typical Performance Curves.

DIGITAL CROSSTALK

Digital crosstalk is the glitch impulse measured at the output of one DAC due to a full scale transition on the other DAC—see Typical Performance Curves. It is dominated by digital coupling. Also, the integrated area of the glitch pulse is specified in nV–s. See table of electrical specifications.

DIGITAL FEEDTHROUGH

Digital feedthrough is the noise at a DAC output due to activity on the digital inputs—see Typical Performance Curves.

OPERATION

Depending on the address selected, the 4 MSBs or the 8 LSBs are written into the appropriate input register for each DAC when the $\overline{WR}$ signal is brought low. The data are latched in the input register when the $\overline{WR}$ goes high. Data are then transferred from the input registers to the DAC latch registers by bringing $\overline{LE}$ low. The data are latched in the DAC latch registers when $\overline{LE}$ goes high. All DACs are updated simultaneously.

CIRCUIT DESCRIPTION

Each of the four DACs in the DAC4815 consists of a CMOS logic section, a CMOS DAC cell, and an output amplifier. One buried-zener +10.0V reference and a –10V reference are shared by all DACs.

Figure 1 is a simplified circuit for a DAC cell. An R, 2R ladder network is driven by a voltage reference at V_{REF}. Current from the ladder is switched either to I_{OUT} or AGND by 12 single-pole double-throw CMOS switches. This maintains constant current in each leg of the ladder regardless of digital input code. This makes the resistance at V_{REF} constant (it can be driven by either a voltage or current reference). The reference can be either positive or negative polarity with a range of up to ±10V.

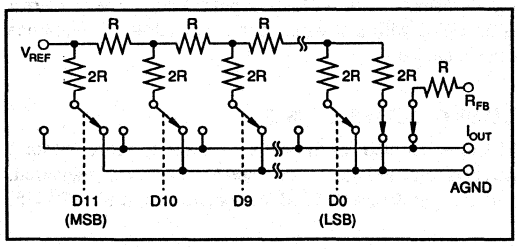


FIGURE 1. Simplified Circuit Diagram of DAC Cell.

CMOS switches included in series with the ladder terminating resistor and the feedback resistor, R_{FB}, compensate for the temperature drift of the ladder switch ON resistance.

The output op amps are connected as transimpedance amplifiers to convert the DAC-cell output current into an output voltage. They have been specially designed and compensated for precision and fast settling in this application.

POWER SUPPLY CONNECTIONS

The DAC4815 is specified for operation with power supplies of V_L = +5V and V_S = either ±12V or ±15V. Even with the V_S supplies at ±11.4V the DACs can swing a full ±10V. Power supply decoupling capacitors (1µF tantalum) should be located close to the DAC power supply connections.

Separate digital and analog ground pins are provided to permit separate current returns. They should be connected together at one point. Proper layout of the two current returns will prevent digital logic switching currents from degrading the analog output signal. The analog ground current is code dependent so the impedance to the system reference ground must be kept to a minimum. Connect DACs as shown in Figure 2 or use a ground plane to keep ground impedance less than 0.1Ω for less than 0.1LSB error.

±10V OUTPUT RANGE CONNECTION

For a ±10V bipolar output connect the DAC4815 as shown in Figure 3.

CONNECTION TO DIGITAL BUS

DAC4815s can easily be connected to a µprocessor bus. Decode your address lines to derive the control signals shown in Figure 4. Only one $\overline{LATCH}$ signal is required for a system where all DAC4815s are updated simultaneously. If your want to update DAC4815s independently, use separate $\overline{LATCH}$ signals. The $\overline{LATCH}$ and $\overline{WRITE}$ signals can be brought low simultaneously to update the DAC registers with the same processor instruction that writes the final 8-bit data word the DAC input registers.

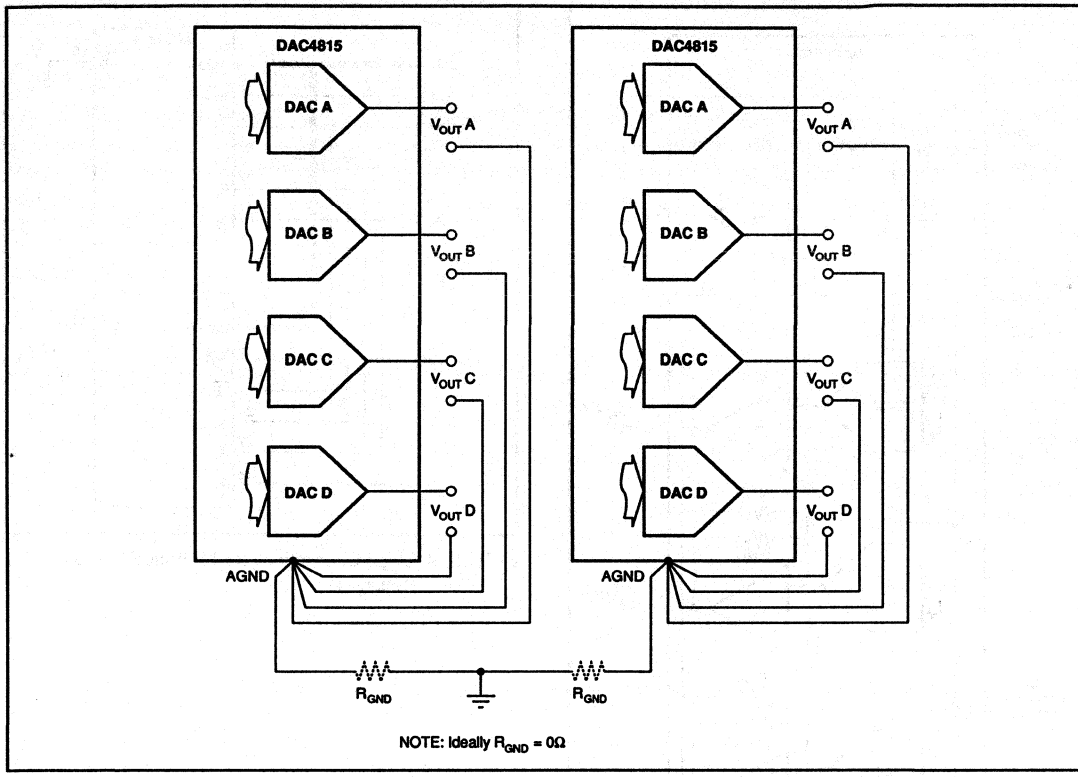


FIGURE 2. Recommended Ground Connections for Multiple DAC Packages.

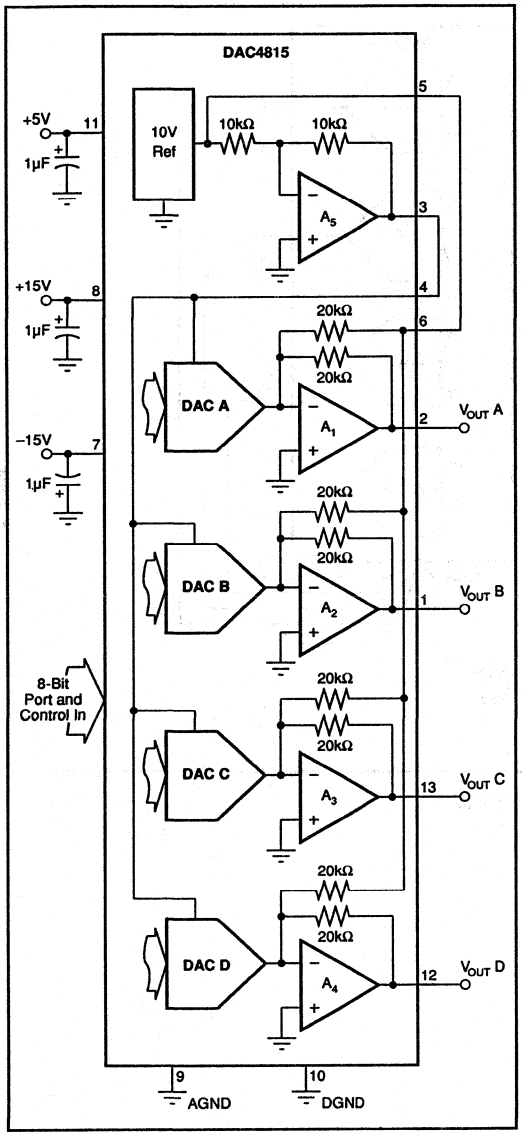


FIGURE 3. Analog Connections for ±10V DAC Output.

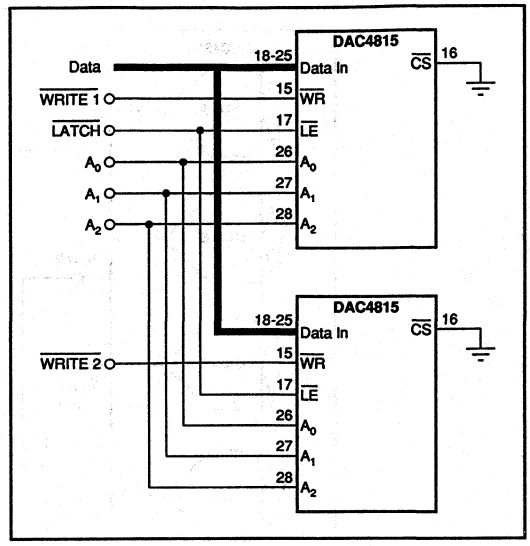


FIGURE 4. Logic Connections for Multiple DAC4815 Packages.

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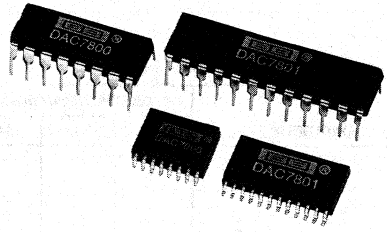


DAC7800
DAC7801
DAC7802

AVAILABLE IN DIE

Dual Monolithic CMOS 12-Bit Multiplying DIGITAL-TO-ANALOG CONVERTERS

FEATURES

- TWO D/As IN A 0.3" WIDE PACKAGE
- SINGLE +5V SUPPLY
- HIGH SPEED DIGITAL INTERFACE:
  Serial—DAC7800
  8 + 4-Bit Parallel—DAC7801
  12-Bit Parallel—DAC7802
- MONOTONIC OVER TEMPERATURE
- LOW CROSSTALK: –94dB min
- FULLY SPECIFIED OVER –40°C TO +85°C

APPLICATIONS

- PROCESS CONTROL OUTPUTS
- ATE PIN ELECTRONICS LEVEL SETTING
- PROGRAMMABLE FILTERS
- PROGRAMMABLE GAIN CIRCUITS
- AUTO-CALIBRATION CIRCUITS

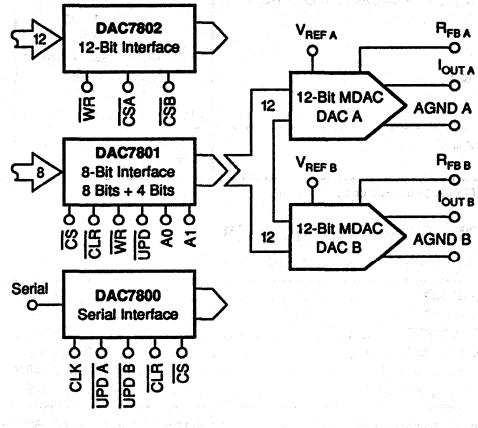
DESCRIPTION

The DAC7800, DAC7801 and DAC7802 are members of a new family of monolithic dual 12-bit CMOS multiplying digital-to-analog converters. The digital interface speed and the AC multiplying performance are achieved by using an advanced CMOS process optimized for data conversion circuits. High stability on-chip resistors provide true 12-bit integral and differential linearity over the wide industrial temperature range of –40°C to +85°C.

DAC7800 features a serial interface capable of clocking-in data at a rate of at least 10MHz. Serial data is clocked (edge triggered) MSB first into a 24-bit shift register and then latched into each D/A separately or simultaneously as required by the application. An asynchronous CLEAR control is provided for power-on reset or system calibration functions. It is packaged in a 16-pin 0.3" wide plastic DIP.

DAC7801 has a 2-byte (8 + 4) double-buffered interface. Data is first loaded (level transferred) into the input registers in two steps for each D/A. Then both D/As are updated simultaneously. DAC7801 features an asynchronous CLEAR control. DAC7801 is packaged in a 24-pin 0.3" wide plastic DIP.

DAC7802 has a single-buffered 12-bit data word interface. Parallel data is loaded (edge triggered) into the single D/A register for each D/A. DAC7802 is packaged in a 24-pin 0.3" wide plastic DIP.



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Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL

At V_{DD} = +5VDC, $V_{REF\,A}$ = $V_{REF\,B}$ = +10V, T_A = –40°C to +85°C unless otherwise noted.

PARAMETER	CONDITIONS	DAC7800/7801/7802KP, D			DAC7800/7801/7802LP			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
ACCURACY								
Resolution		12			*			Bits
Relative Accuracy				±1			±1/2	LSB
Differential Nonlinearity				±1			*	LSB
Gain Error	Measured Using $R_{FB\,A}$ and $R_{FB\,B}$. All Registers Loaded with All 1s.			±3			±1	LSB
Gain Temperature Coefficient(1)			2	5		*	*	ppm/°C
Output Leakage Current	T_A = +25°C		0.005	10		*	*	nA
	T_A = –40°C to +85°C		3	150		*	*	nA
REFERENCE INPUT								
Input Resistance		6	10	14	*	*	*	kΩ
Input Resistance Match			0.5	3		*	2	%
DIGITAL INPUTS								
V_{IH} (Input High Voltage)		2			*			V
V_{IL} (Input Low Voltage)				0.8			*	V
I_{IN} (Input Current)	T_A = +25°C			±1			*	µA
	T_A = –40°C to +85°C			±10			*	µA
C_{IN} (Input Capacitance)			0.8	10		*	*	pF
POWER SUPPLY								
V_{DD}		4.5		5.5	*		*	V
I_{DD}			0.2	2		*	*	mA
Power Supply Rejection	V_{DD} from 4.5V to 5.5V			0.002			*	%/%

* Same specification as for DAC7800/7801/7802KP.

AC PERFORMANCE

OUTPUT OP AMP IS OPA602.

At V_{DD} = +5VDC, $V_{REF\,A}$ = $V_{REF\,B}$ = +10V, T_A = +25°C unless otherwise noted. These specifications are fully characterized but not subject to test.

PARAMETER	CONDITIONS	DAC7800/7801/7802KP, D			DAC7800/7801/7802LP			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
OUTPUT CURRENT SETTLING TIME	To 0.01% of Full Scale R_L = 100Ω, C_L = 13pF		0.4	0.8		*	*	µs
DIGITAL-TO-ANALOG GLITCH IMPULSE	$V_{REF\,A}$ = $V_{REF\,B}$ = 0V R_L = 100Ω, C_L = 13pF		0.9			*		nV-s
AC FEEDTHROUGH	f_{VREF} = 10kHz		–75	–72		*	*	dB
OUTPUT CAPACITANCE	DAC Loaded with All 0s		30	50		*	*	pF
	DAC Loaded with All 1s		70	100		*	*	pF
CHANNEL-TO-CHANNEL ISOLATION								
$V_{REF\,A}$ to $I_{OUT\,B}$	$f_{VREF\,A}$ = 10kHz $V_{REF\,B}$ = 0V, Both DACs Loaded with 1s	–90	–94			*	*	dB
$V_{REF\,B}$ to $I_{OUT\,A}$	$f_{VREF\,B}$ = 10kHz $V_{REF\,A}$ = 0V, Both DACs Loaded with 1s	–90	–101			*	*	dB
DIGITAL CROSSTALK	Full Scale Transition R_L = 100Ω, C_L = 13pF		0.9			*		nV-s

NOTE: (1) Guaranteed but not tested.

ABSOLUTE MAXIMUM RATINGS

At T_A = +25°C unless otherwise noted.

V_{DD} to AGND	0V, +7V
V_{DD} to DGND	0V, +7V
AGND to DGND	–0.3, V_{DD}
Digital Input to DGND	–0.3, V_{DD} + 0.3
$V_{REF\,A}$, $V_{REF\,B}$ to AGND	±25V
$V_{REF\,A}$, $V_{REF\,B}$ to DGND	±25V
$I_{OUT\,A}$, $I_{OUT\,B}$ to AGND	–0.3, V_{DD}
Storage Temperature Range	–55°C to +125°C
Operating Temperature Range	–40°C to +85°C
Lead Temperature (soldering, 10s)	+300°C
Junction Temperature	+175°C

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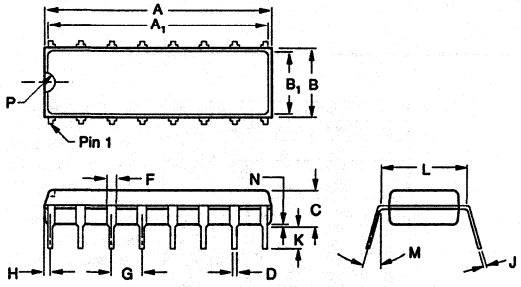
ORDERING INFORMATION

MODEL	RELATIVE ACCURACY	GAIN ERROR	PACKAGE
DAC7800KP	±1LSB	±3LSB	16-Pin DIP
DAC7800KU			16-Lead SO
DAC7800LP	±1/2LSB	±1LSB	16-Pin DIP
DAC7800LU			16-Lead SO
DAC7800D	±1LSB	±3LSB	100 Die/Pack
DAC7801KP	±1LSB	±3LSB	24-Pin DIP
DAC7801KU			24-Lead SO
DAC7801LP	±1/2LSB	±1LSB	24-Pin DIP
DAC7801LU			24-Lead SO
DAC7801D	±1LSB	±3LSB	100 Die/Pack
DAC7802KP	±1LSB	±3LSB	24-Pin DIP
DAC7802KU			24-Lead SO
DAC7802LP	±1/2LSB	±1LSB	24-Pin DIP
DAC7802LU			24-Lead SO
DAC7802D	±1LSB	±3LSB	100 Die/Pack

MECHANICAL — DAC7800KP/LP

P Package — 16-Pin Plastic DIP

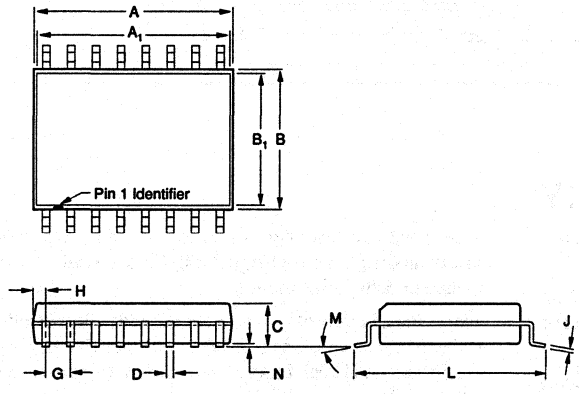


DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.740	.800	18.80	20.32
A1	.725	.785	18.42	19.94
B	.230	.290	5.85	7.38
B1	.200	.250	5.09	6.36
C	.120	.200	3.05	5.09
D	.015	.023	0.38	0.59
F	.030	.070	0.76	1.78
G	.100 BASIC		2.54 BASIC	
H	0.20	.050	0.51	1.27
J	.008	.015	0.20	0.38
K	.070	.150	1.78	3.82
L	.300 BASIC		7.63 BASIC	
M	0°	15°	0°	15°
N	.010	.030	0.25	0.76
P	.025	.050	0.64	1.27

NOTE: Leads in true position within 0.010" (0.25mm) R at MMC at seating plane.

MECHANICAL — DAC7800KU/LU

U Package — 16-Pin SOIC

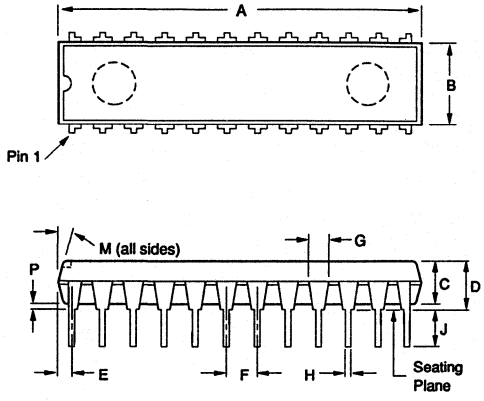


DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.400	.416	10.16	10.57
A1	.388	.412	9.86	10.46
B	.286	.302	7.26	7.67
B1	.268	.286	6.81	7.26
C	.093	.109	2.36	2.77
D	.015	.020	0.38	0.51
G	.050 BASIC		1.27 BASIC	
H	.022	.038	0.56	0.97
J	.008	.012	0.20	0.30
L	.391	.421	9.93	10.69
M	5° TYP		5° TYP	
N	.000	.012	0.00	0.30

NOTE: Leads in true position within 0.010" (0.25mm) R at MMC at seating plane.

MECHANICAL — DAC7801KP/LP, DAC7802KP/LP

P Package — 24-Pin Single Wide Plastic DIP



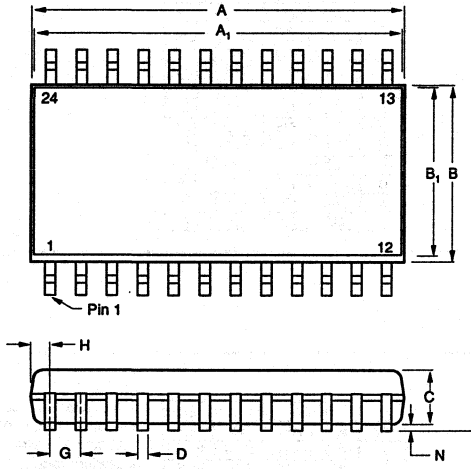
DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.125	1.255	28.58	31.88
B	.250	.290	6.35	7.37
C	—	—	—	—
D	.150	.170	3.81	4.32
E	.010	.080	0.25	2.03
F	.100 BASIC		2.54 BASIC	
G	.050	.070	1.27	1.78

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
H	.016	.020	0.41	0.51
J	.125	N/A	3.18	N/A
K	.300 BASIC		7.62 BASIC	
L	—	—	—	—
M	0°	15°	0°	15°
N	.008	.015	0.20	0.38
P	.010	.030	0.25	0.76

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.

MECHANICAL — DAC7801KU/LU, DAC7802KU/LU

U Package — 24-Pin SOIC



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.602	.618	15.29	15.70
A_1	.595	.618	15.11	15.70
B	.286	.302	7.26	7.67
B_1	.270	.285	6.86	7.24
C	.093	.108	2.36	2.74
D	.015	.019	0.38	0.48
G	.050 BASIC		1.27 BASIC	
H	.026	.034	0.66	0.86
J	.008	.012	0.20	0.30
L	.390	.422	9.91	10.72
M	0°	10°	0°	10°
N	.000	.012	0.00	0.30

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.

ELECTROSTATIC DISCHARGE SENSITIVITY

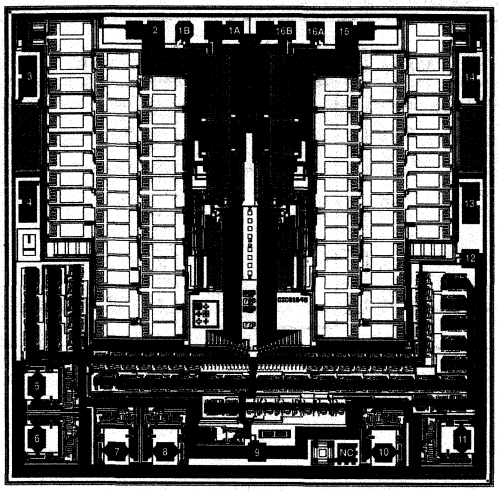
Electrostatic discharge can cause damage ranging from performance degradation to complete device failure.

Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

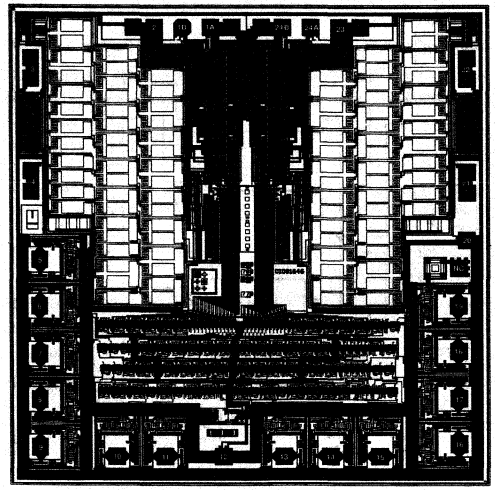
Digital Inputs: All digital inputs of the DAC780X family incorporate on-chip ESD protection circuitry. This protection is designed and has been tested to withstand five 2500V positive and negative discharges (100pF in series with 1500Ω) applied to each digital input.

Analog Pins: Each analog pin has been tested to Burr-Brown's analog ESD test consisting of five 1000V positive and negative discharges (100pF in series with 1500Ω) applied to each pin. AGND, I_{OUT}, and R_{FB} show some sensitivity. Failure to observe ESD handling procedures could result in catastrophic device failure.

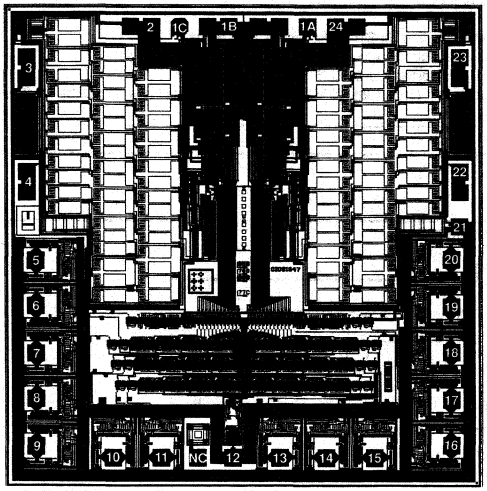
DICE INFORMATION



DAC7800 DIE TOPOGRAPHY



DAC7801 DIE TOPOGRAPHY



DAC7802 DIE TOPOGRAPHY

MECHANICAL INFORMATION

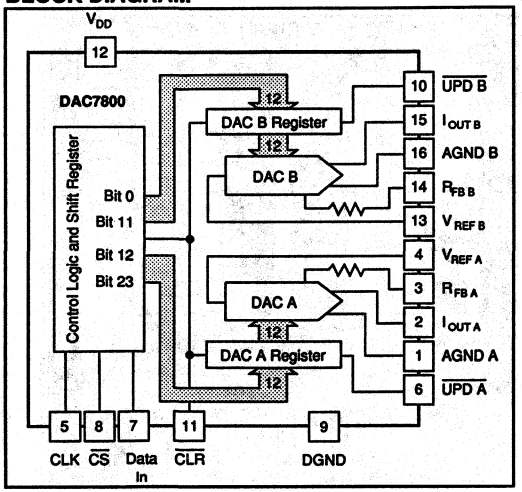
	MILS (0.001")	MILLIMETERS
Die Size	131 x 121 ±5	3.33 x 3.07 ±0.13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.10 x 0.10
Metalization	Aluminum	

Substrate Bias: $+V_{DD}$

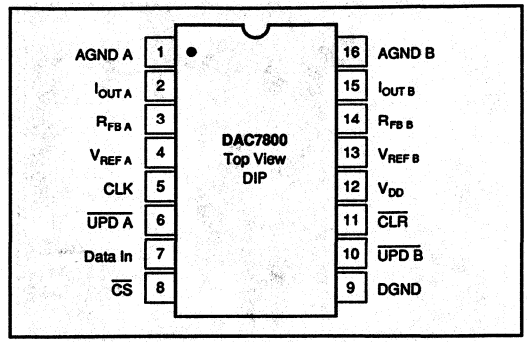
See "DICE PRODUCTS" Section 17 in Data Book Supplement Volume 33c, or contact Burr-Brown for current information.

DAC7800

BLOCK DIAGRAM



PIN CONFIGURATION

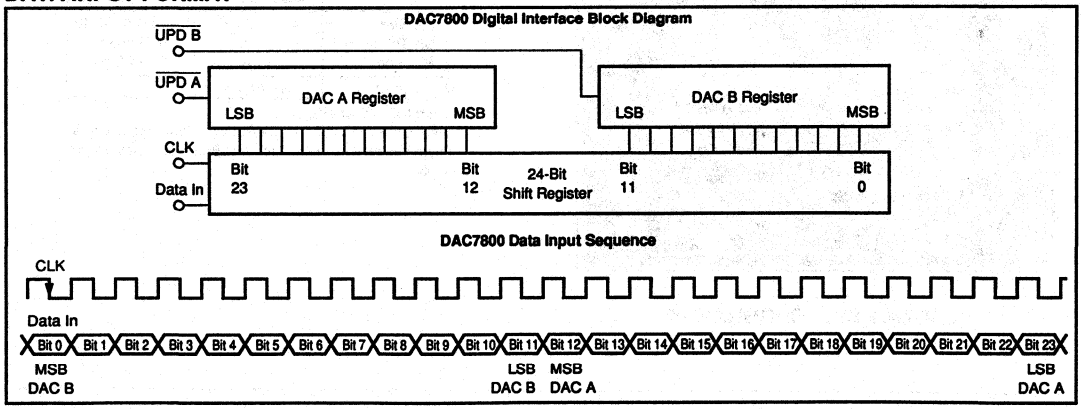


LOGIC TRUTH TABLE

CLK	$\overline{\text{UPD A}}$	$\overline{\text{UPD B}}$	$\overline{\text{CS}}$	$\overline{\text{CLR}}$	FUNCTION
X	X	X	X	0	All register contents set to 0's (asynchronous).
X	X	X	1	X	No data transfer.
↓	X	X	0	1	Input data is clocked into input register (location Bit 23) and previous data shifts.
X	0	1	0	1	Input register bits 23 (LSB)—12 (MSB) are loaded into DAC A.
X	1	0	0	1	Input register bits 11 (LSB)—0 (MSB) are loaded into DAC B.
X	0	0	0	1	Input register bits 23 (LSB)—12 (MSB) are loaded into DAC A, and input register bits 11 (LSB)—0 (MSB) are loaded into DAC B.

X = Don't care. ↓ means falling edge triggered.

DATA INPUT FORMAT

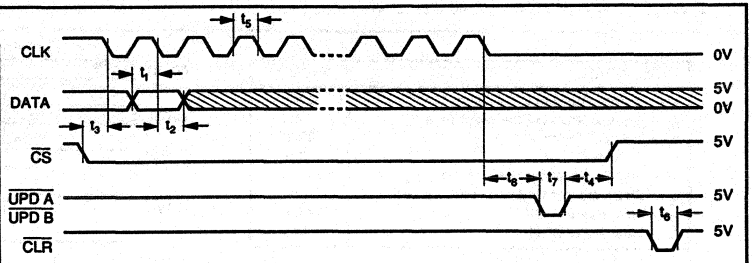


DAC7800 (CONT)

TIMING CHARACTERISTICS

V_{DD} = +5V, $V_{REF\,A}$ = $V_{REF\,B}$ = +10V, T_A = –40°C to +85°C.

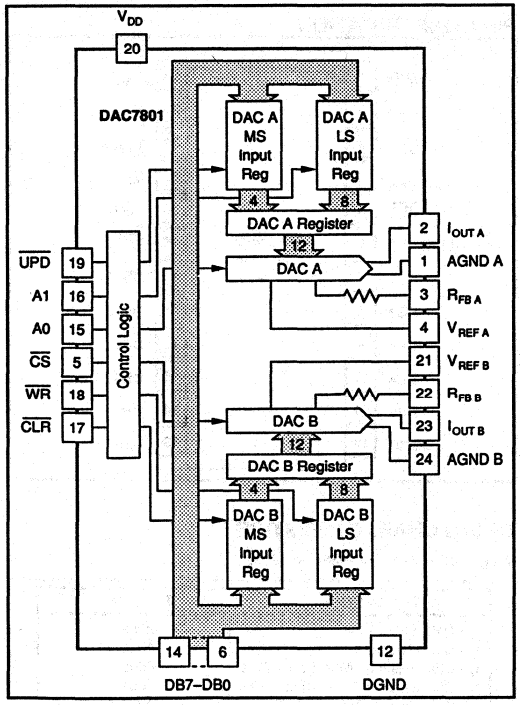
PARAMETER	MINIMUM
t_1 — Data Setup Time	15ns
t_2 — Data Hold Time	15ns
t_3 — Chip Select to CLK, Update, Data Setup Time	15ns
t_4 — Chip Select to CLK, Update, Data Hold Time	40ns
t_5 — CLK Pulse Width	40ns
t_6 — Clear Pulse Width	40ns
t_7 — Update Pulse Width	40ns
t_8 — CLK Edge to $\overline{UPD\,A}$ or $\overline{UPD\,B}$	15ns



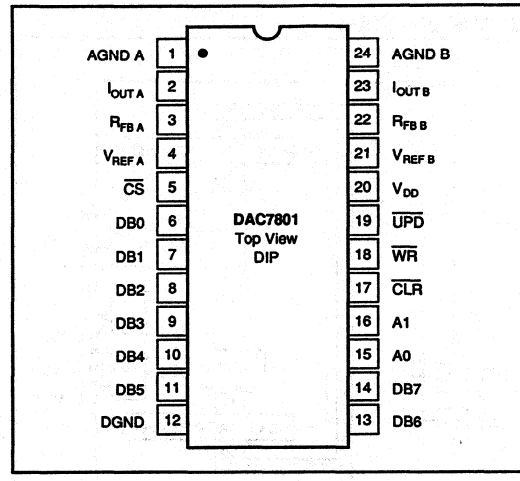
NOTES: (1) All input signal rise and fall times are measured from 10% to 90% of +5V. $t_R = t_F$ = 5ns. (2) Timing measurement reference level is $\frac{V_{IH} + V_{IL}}{2}$.

DAC7801

BLOCK DIAGRAM



PIN CONFIGURATION



LOGIC TRUTH TABLE

CLR	UPD	CS	WR	A1	A0	FUNCTION
1	1	1	X	X	X	No Data Transfer
1	1	X	1	X	X	No Data Transfer
0	X	X	X	X	X	All Registers Cleared
1	1	0	0	0	0	DAC A LS Input Register Loaded with DB7–DB0 (LSB)
1	1	0	0	0	1	DAC A MS Input Register Loaded with DB3 (MSB)–DB0
1	1	0	0	1	0	DAC B LS Input Register Loaded with DB7–DB0 (LSB)
1	1	0	0	1	1	DAC B MS Input Register Loaded with DB3 (MSB)–DB0
1	0	1	0	X	X	DAC A, DAC B Registers Updated Simultaneously from Input Registers
1	0	0	0	X	X	DAC A, DAC B Registers are Transparent

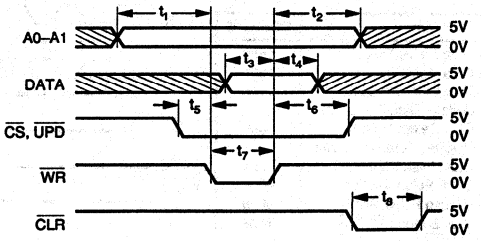
X = Don't care.

DAC7801 (CONT)

TIMING CHARACTERISTICS

V_{DD} = +5V, $V_{REF\,A}$ = $V_{REF\,B}$ = +10V, T_A = –40°C to +85°C.

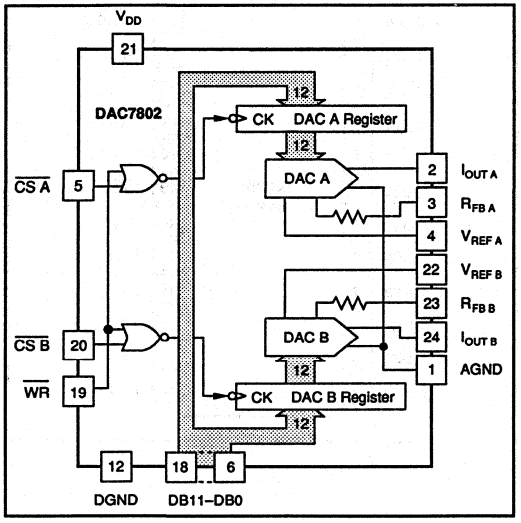
PARAMETER	MINIMUM
t_1 — Address Valid to Write Setup Time	10ns
t_2 — Address Valid to Write Hold Time	10ns
t_3 — Data Setup Time	30ns
t_4 — Data Hold Time	10ns
t_5 — Chip Select or Update to Write Setup Time	0ns
t_6 — Chip Select or Update to Write Hold Time	0ns
t_7 — Write Pulse Width	40ns
t_8 — Clear Pulse Width	40ns



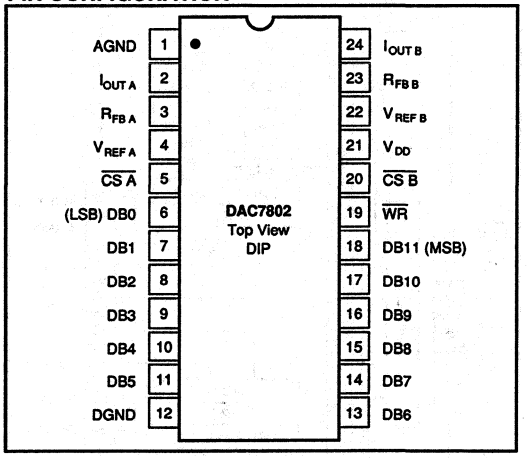
NOTES: (1) All input signal rise and fall times are measured from 10% to 90% of +5V. $t_R = t_F$ = 5ns. (2) Timing measurement reference level is $\frac{V_{IH} + V_{IL}}{2}$.

DAC7802

BLOCK DIAGRAM



PIN CONFIGURATION



LOGIC TRUTH TABLE

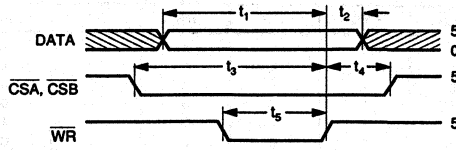
$\overline{CSA}$	$\overline{CSB}$	$\overline{WR}$	FUNCTION
X	X	1	No Data Transfer
1	1	X	No Data Transfer
↓	↓	0	A Rising Edge on $\overline{CSA}$ or $\overline{CSB}$ Loads Data to the Respective DAC
0	1	↓	DAC A Register Loaded from Data Bus
1	0	↓	DAC B Register Loaded from Data Bus
0	0	↓	DAC A and DAC B Registers Loaded from Data Bus

X = Don't care. ↓ means rising edge triggered.

TIMING CHARACTERISTICS

At V_{DD} = +5V, and T_A = –40°C to +85°C.

PARAMETER	MINIMUM
t_1 - Data Setup Time	20ns
t_2 - Data Hold Time	15ns
t_3 - Chip Select to Write Setup Time	30ns
t_4 - Chip Select to Write Hold Time	0ns
t_5 - Write Pulse Width	30ns

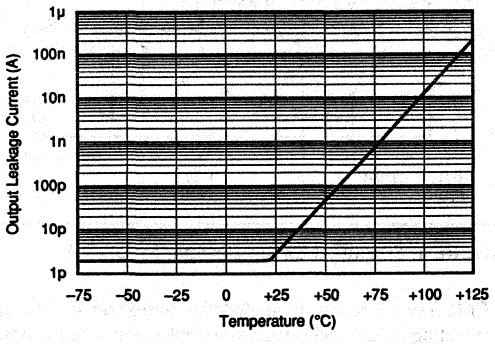


NOTES: (1) All input signal rise and fall times are measured from 10% to 90% of +5V. $t_R = t_F$ = 5ns. (2) Timing measurement reference level is $\frac{V_{IH} + V_{IL}}{2}$.

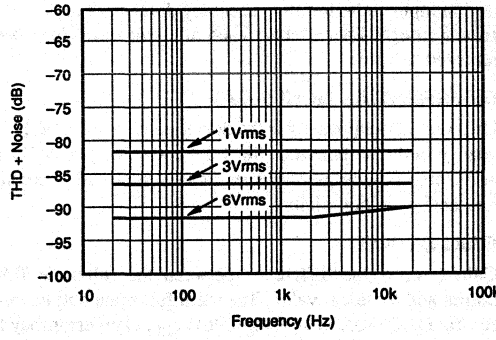
TYPICAL PERFORMANCE CURVES

OUTPUT OP AMP IS OPA602.
T_A = +25°C, V_{DD} = +5V.

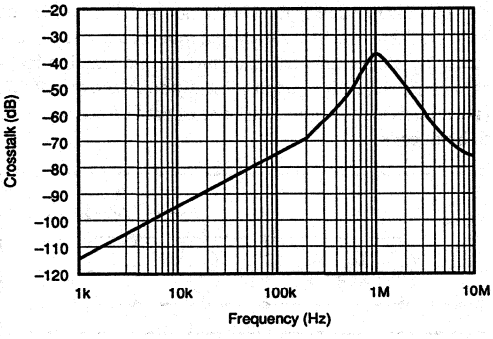
OUTPUT LEAKAGE CURRENT vs TEMPERATURE



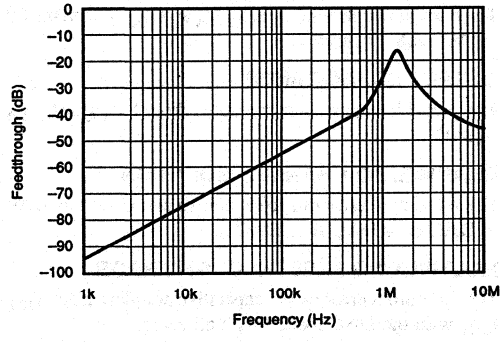
THD + NOISE vs FREQUENCY



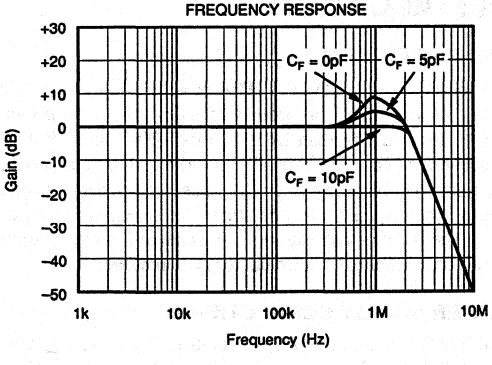
CHANNEL-TO-CHANNEL ISOLATION vs FREQUENCY



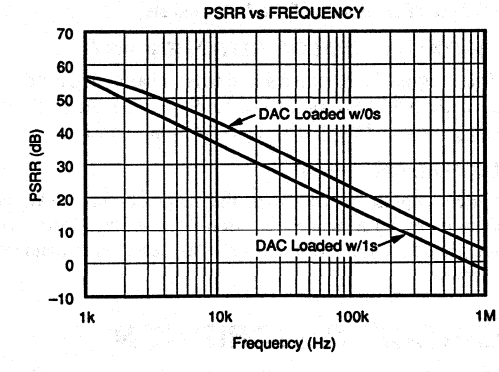
FEEDTHROUGH vs FREQUENCY



FREQUENCY RESPONSE



PSRR vs FREQUENCY



DISCUSSION OF SPECIFICATIONS

RELATIVE ACCURACY

This term, also known as end point linearity or integral linearity, describes the transfer function of analog output to digital input code. Relative accuracy describes the deviation from a straight line, after zero and full scale errors have been adjusted to zero.

DIFFERENTIAL NONLINEARITY

Differential nonlinearity is the deviation from an ideal 1LSB change in the output when the input code changes by 1LSB. A differential nonlinearity specification of 1LSB maximum guarantees monotonicity.

GAIN ERROR

Gain error is the difference between the full-scale DAC output and the ideal value. The ideal full scale output value for the DAC780X is $-(4095/4096)V_{REF}$. Gain error may be adjusted to zero using external trims as shown in Figures 5 and 7.

OUTPUT LEAKAGE CURRENT

The current which appears at $I_{OUT\,A}$ and $I_{OUT\,B}$ with the DAC loaded with all zeros.

OUTPUT CAPACITANCE

The parasitic capacitance measured from $I_{OUT\,A}$ or $I_{OUT\,B}$ to AGND.

CHANNEL-TO-CHANNEL ISOLATION

The AC output error due to capacitive coupling from DAC A to DAC B or DAC B to DAC A.

MULTIPLYING FEEDTHROUGH ERROR

The AC output error due to capacitive coupling from V_{REF} to I_{OUT} with the DAC loaded with all zeros.

OUTPUT CURRENT SETTLING TIME

The time required for the output current to settle to within ±0.01% of final value for a full scale step.

DIGITAL-TO-ANALOG GLITCH ENERGY

The integrated area of the glitch pulse measured in nanovolt-seconds. The key contributor to digital-to-analog glitch is charge injected by digital logic switching transients.

DIGITAL CROSSTALK

Glitch impulse measured at the output of one DAC but caused by a full scale transition on the other DAC. The integrated area of the glitch pulse is measured in nanovolt-seconds.

CIRCUIT DESCRIPTION

Figure 1 shows a simplified schematic of one half of a DAC780X. The current from the $V_{REF\,A}$ pin is switched between $I_{OUT\,A}$ and AGND by 12 single-pole double-throw CMOS switches. This maintains a constant current in each leg of the ladder regardless of the input code. The input resistance at V_{REF} is therefore constant and can be driven by either a voltage or current, AC or DC, positive or negative polarity, and have a voltage range up to ±20V.

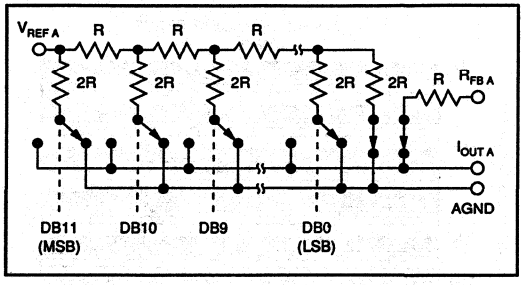


FIGURE 1. Simplified Circuit Diagram for DAC A.

A CMOS switch transistor, included in series with the ladder terminating resistor and in series with the feedback resistor, $R_{FB\,A}$, compensates for the temperature drift of the ON resistance of the ladder switches.

Figure 2 shows an equivalent circuit for DAC A. C_{OUT} is the output capacitance due to the N-channel switches and varies from about 30pF to 70pF with digital input code. The current source I_{LKG} is the combination of surface and junction leakages to the substrate. I_{LKG} approximately doubles every 10°C. R_O is the equivalent output resistance of the D/A and it varies with input code.

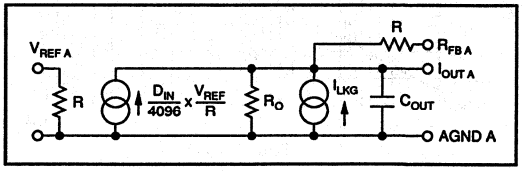


FIGURE 2. Equivalent Circuit for DAC A.

INSTALLATION

ESD PROTECTION

All digital inputs of the DAC780X incorporate on-chip ESD protection circuitry. This protection is designed to withstand 2.5kV (using the Human Body Model, 100pF and 1500Ω). However, industry standard ESD protection methods should be used when handling or storing these components. When not in use, devices should be stored in conductive foam or rails. The foam or rails should be discharged to the destination socket potential before devices are removed.

POWER SUPPLY CONNECTIONS

The DAC780X are designed to operate on $V_{DD} = +5V \pm 10\%$. For optimum performance and noise rejection, power supply decoupling capacitors C_D should be added as shown in the application circuits. These capacitors (1µF tantalum recommended) should be located close to the D/A. AGND and

DGND should be connected together at one point only, preferably at the power supply ground point. Separate returns minimize current flow in low-level signal paths if properly connected. Output op amp analog common (+ input) should be connected as near to the AGND pins of the DAC780X as possible.

WIRING PRECAUTIONS

To minimize AC feedthrough when designing a PC board, care should be taken to minimize capacitive coupling between the V_{REF} lines and the I_{OUT} lines. Similarly, capacitive coupling between DACs may compromise the channel-to-channel isolation. Coupling from any of the digital control or data lines might degrade the glitch and digital crosstalk performance. Solder the DAC780X directly into the PC board without a socket. Sockets add parasitic capacitance (which can degrade AC performance).

AMPLIFIER OFFSET VOLTAGE

The output amplifier used with the DAC780X should have low input offset voltage to preserve the transfer function linearity. The voltage output of the amplifier has an error component which is the offset voltage of the op amp multiplied by the "noise gain" of the circuit. This "noise gain" is equal to $(R_F/R_O + 1)$ where R_O is the output impedance of the D/A I_{OUT} terminal and R_F is the feedback network impedance. The non-linearity occurs due to the output impedance varying with code. If the 0 code case is excluded (where R_O = infinity), the R_O will vary from R to 3R providing a "noise gain" variation between 4/3 and 2. In addition, the variation of R_O is non-linear with code, and the largest steps in R_O occur at major code transitions where the worst differential non-linearity is also likely to be experienced. The non-linearity seen at the amplifier output is $2V_{OS} - 4V_{OS}/3 = 2V_{OS}/3$. Thus, to maintain good non-linearity the op amp offset should be much less than 1/2LSB.

UNIPOLAR CONFIGURATION

Figure 3 shows DAC780X in a typical unipolar (two-quadrant) multiplying configuration. The analog output values versus digital input code are listed in Table II. The operational amplifiers used in this circuit can be single amplifiers such as the OPA602, or a dual amplifier such as the OPA2107. C1 and C2 provide phase compensation to minimize settling time and overshoot when using a high speed operational amplifier.

If an application requires the D/A to have zero gain error, the circuit shown in Figure 4 may be used. Resistors R2 and R4 induce a positive gain error greater than worst-case initial negative gain error. Trim resistors R1 and R3 provide a variable negative gain error and have sufficient trim range to correct for the worst-case initial positive gain error plus the error produced by R2 and R4.

BIPOLAR CONFIGURATION

Figure 5 shows the DAC780X in a typical bipolar (four-quadrant) multiplying configuration. The analog output values versus digital input code are listed in Table III.

DATA INPUT	ANALOG OUTPUT
MSB ↓ ↓ LSB	
1111 1111 1111	$-V_{REF}$ (4095/4096)
1000 0000 0000	$-V_{REF}$ (2048/4096) = $-1/2V_{REF}$
0000 0000 0001	$-V_{REF}$ (1/4096)
0000 0000 0000	0 Volts

TABLE II. Unipolar Output Code.

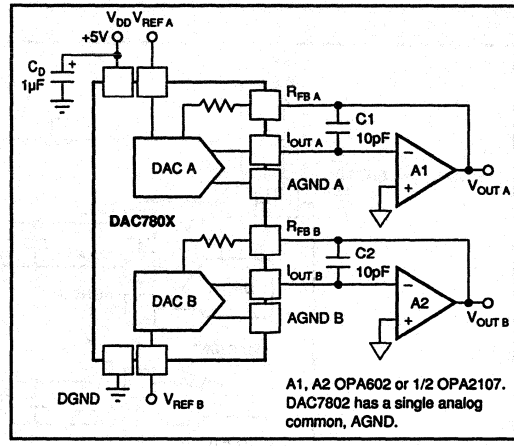


FIGURE 3. Unipolar Configuration.

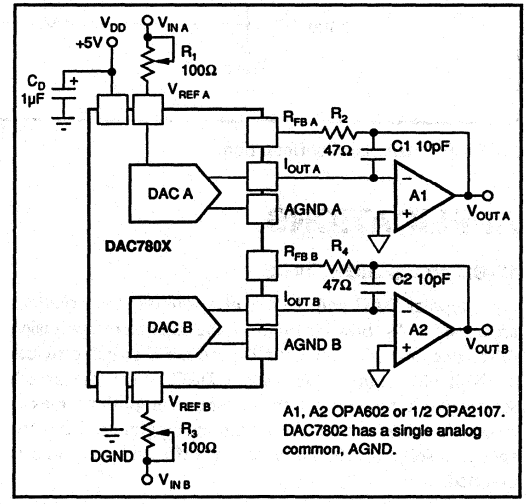


FIGURE 4. Unipolar Configuration with Gain Trim.

The operational amplifiers used in this circuit can be single amplifiers such as the OPA602, a dual amplifier such as the OPA2107, or a quad amplifier like the OPA404. C1 and C2 provide phase compensation to minimize settling time and overshoot when using a high speed operational amplifier. The bipolar offset resistors R5–R7 and R8–R10 should be ratio-matched to 0.01% to ensure the specified gain error performance.

If an application requires the D/A to have zero gain error, the circuit shown in Figure 6 may be used. Resistors R2 and R4 induce a positive gain error greater than worst-case initial negative gain error. Trim resistors R1 and R3 provide a variable negative gain error and have sufficient trim range to correct for the worst-case initial positive gain error plus the error produced by R2 and R4.

DATA INPUT	ANALOG OUTPUT
MSB ↓ ↓ LSB	
1111 1111 1111	$+V_{REF}$ (2047/2048)
1000 0000 0001	$+V_{REF}$ (1/2048)
1000 0000 0000	0 Volts
0111 1111 1111	$-V_{REF}$ (1/2048)
0000 0000 0000	$-V_{REF}$ (2048/2048)

TABLE III. Bipolar Output Code.

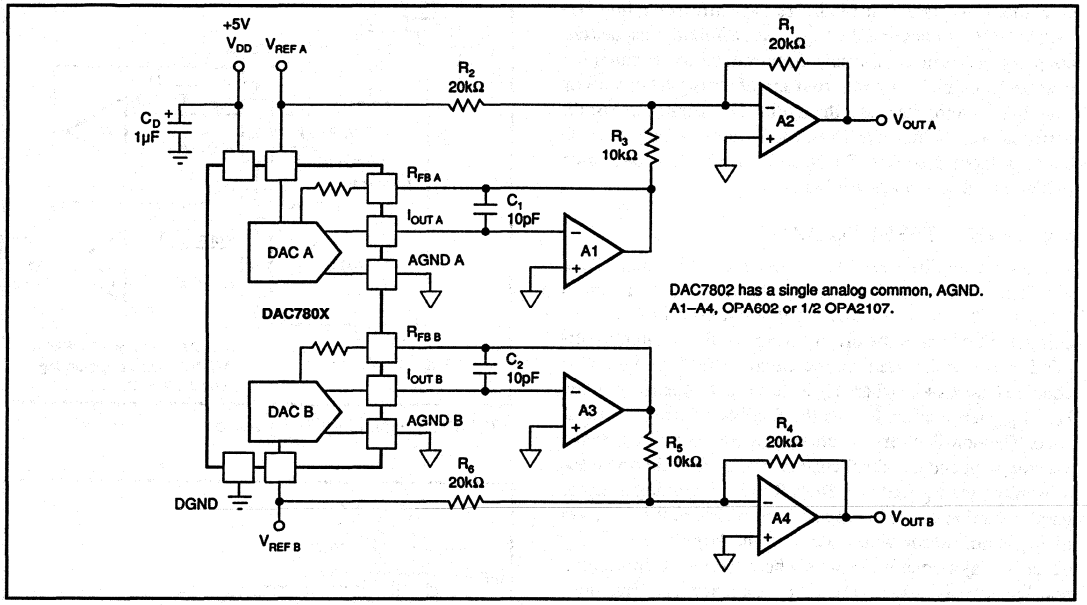


FIGURE 5. Bipolar Configuration.

APPLICATIONS

12-BIT PLUS SIGN DACS

For a bipolar DAC with 13 bits of resolution, two solutions are possible. As shown in Figure 7, the addition of a precision difference amplifier and a high speed JFET switch provides a 12-bit plus sign voltage-output DAC. When the switch selects the op amp output, the difference amplifier serves as a non-inverting output buffer. If the analog ground side of the switch is selected, the output of the difference amplifier is inverted.

Another option, shown in Figure 8, also produces a 12-bit plus sign output without the additional switch and digital control line.

DIGITALLY PROGRAMMABLE ACTIVE FILTER

DAC780X are shown in Figure 9 in a digitally programmable active filter application. The design is based on the state-variable filter, Burr-Brown UAF42, an active filter topology that offers stable and repeatable filter characteristics.

DAC1 and DAC2 can be updated in parallel with a single word to set the center frequency of the filter. DAC 4, which makes use of the uncommitted op amp in UAF42, sets the Q of the filter. DAC3 sets the gain of the filter transfer function without changing the Q of the filter. The reverse is also true.

The center frequency is determined by $f_C = 1/2\pi RC$ where R is the ladder resistance of the D/A (typical value, 10kΩ) and C the internal capacitor value (1000pF) of the UAF42. External capacitors can be added to lower the center frequency of the filter. But the highest center frequency for this circuit will be about 16kHz because the effective series resistance of the D/A cannot be less than 10kΩ.

Note that the ladder resistance of the D/A may vary from device to device. Thus, for best tracking, DAC2 and DAC3 should be in the same package. Some calibration may be necessary from one filter to another.

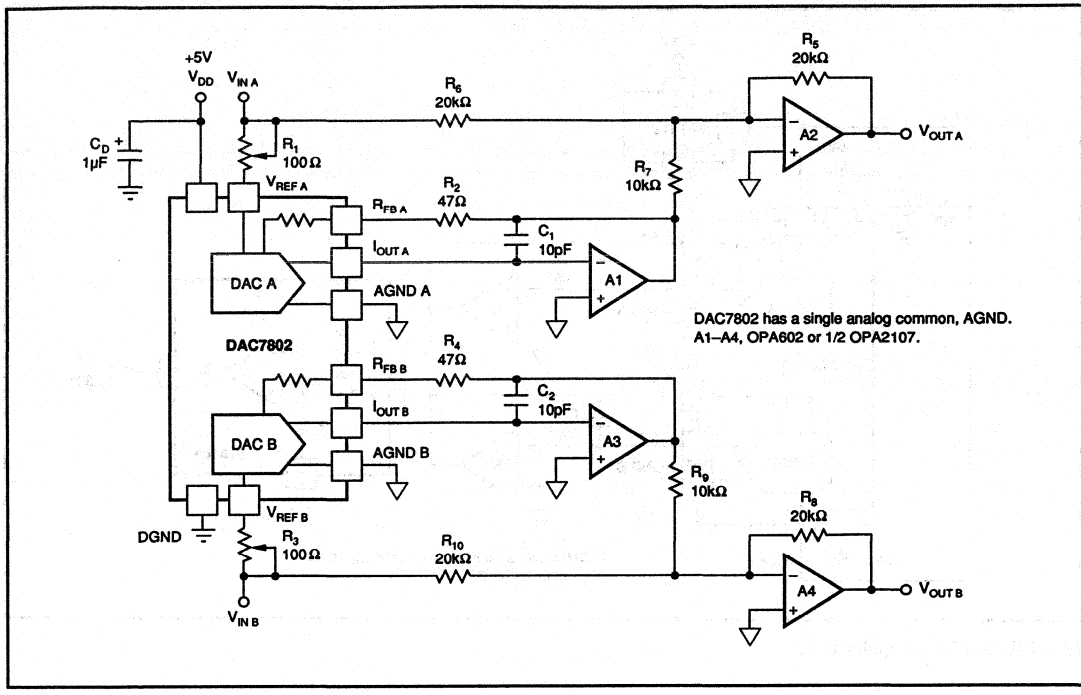


FIGURE 6. Bipolar Configuration with Gain Trim.

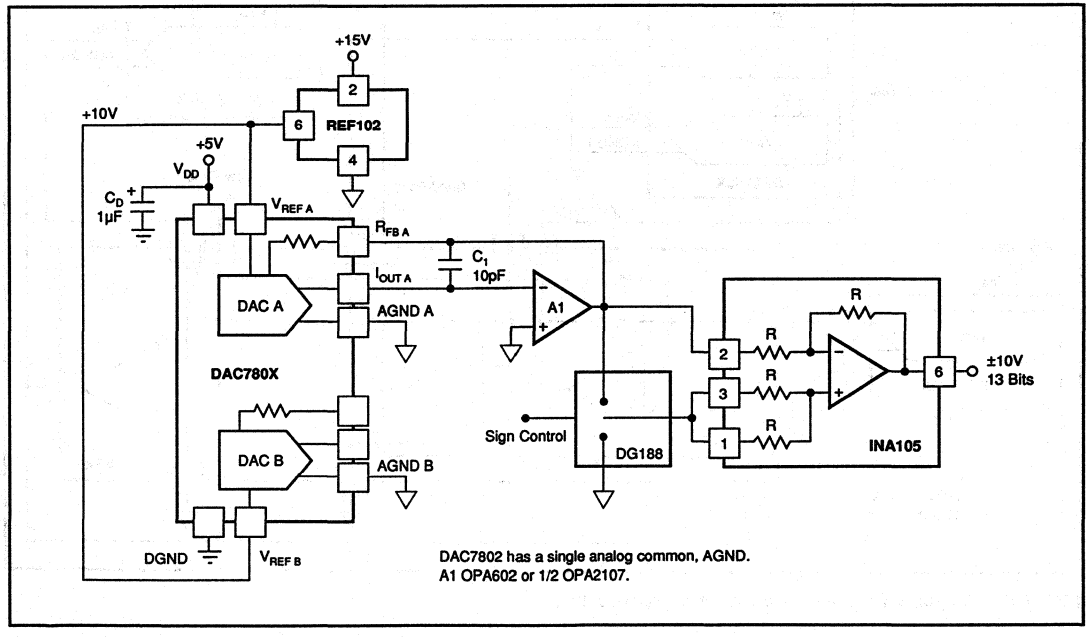


FIGURE 7. 12-Bit Plus Sign DAC.

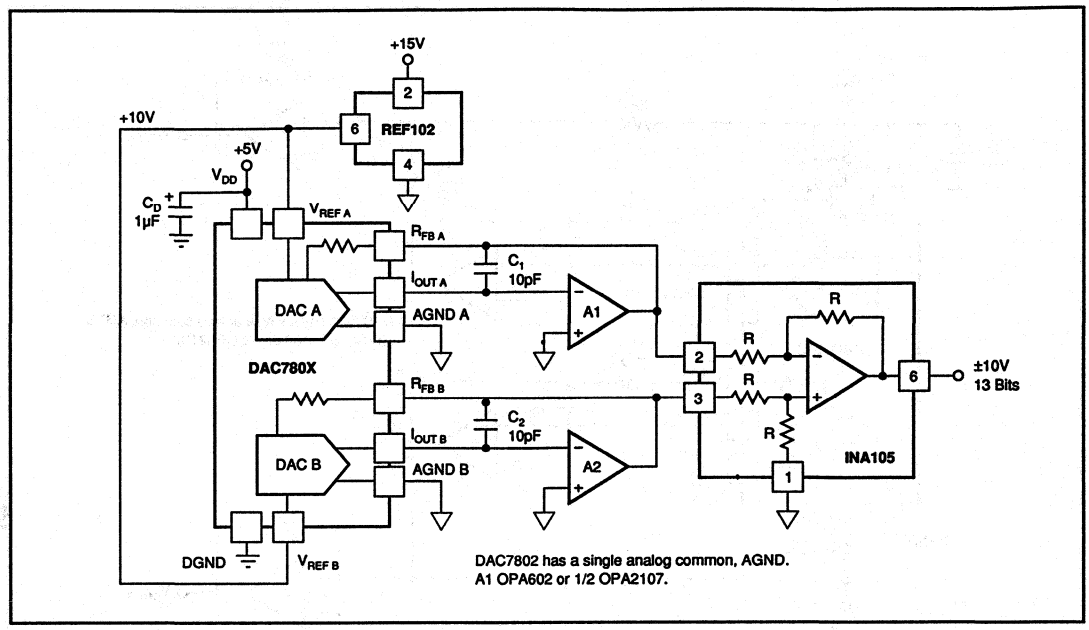


FIGURE 8. 13-Bit Bipolar DAC.

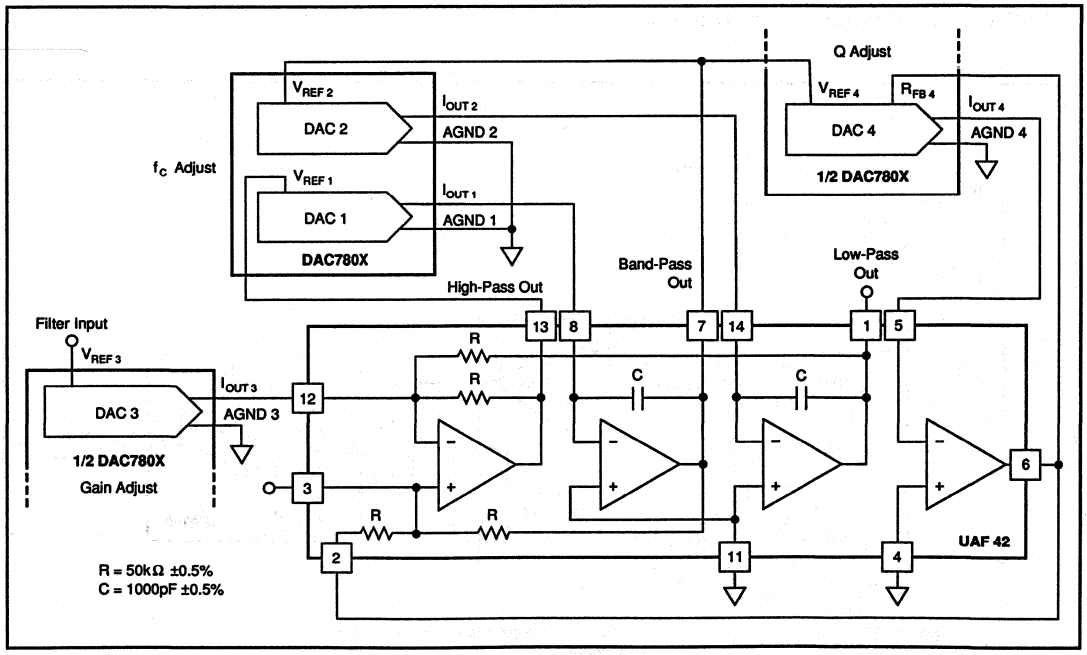


FIGURE 9. Digitally Programmable Universal Active Filter.

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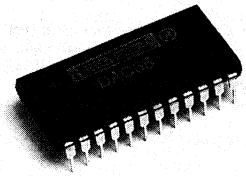


DAC65

AVAILABLE IN DIE

12-Bit High Speed DIGITAL-TO-ANALOG CONVERTER

FEATURES

- FAST SETTLING: 35ns
- INTEGRAL LINEARITY ERROR: ±0.25LSB
- DIFFERENTIAL LINEARITY ERROR: ±0.25LSB
- HIGH SPECTRAL PURITY: –70dBc, f_c = 1MHz
- INTERNAL REFERENCE
- 24-PIN PLASTIC DIP PACKAGE

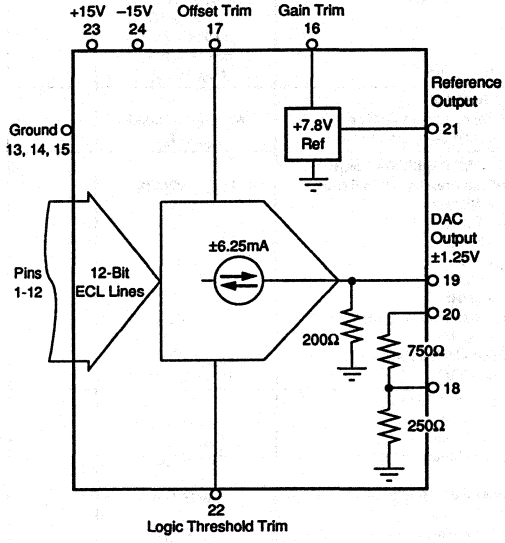
APPLICATIONS

- DIRECT DIGITAL FREQUENCY SYNTHESIZERS
- FAST ATE SYSTEMS
- ARBITRARY WAVEFORM GENERATORS
- HIGH-RESOLUTION VIDEO GRAPHICS
- DIGITAL-TO-ANALOG RECONSTRUCTION
- SPREAD SPECTRUM LOCAL OSCILLATOR

DESCRIPTION

The DAC65 is a fast-settling monolithic 12-bit digital-to-analog converter. OFF-chip bypass capacitors are included in the package for higher performance and user convenience. Excellent linearity and accuracy are achieved with laser-trimmed thin film nichrome resistors. The DAC features bipolar output voltage or current and internal voltage reference. The internal precision resistor network can be used with an external op amp to give an output greater than ±1.25V.

Low harmonic distortion and spurious products together with a low quantizing noise floor make the DAC65 an excellent choice for direct digital frequency synthesizer applications. High accuracy and low gain drift allow its use in precision high-speed test equipment designs. Low-noise ECL logic is used to preserve clean analog output spectral performance.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL

T_A = +25°C, $\pm V_{CC}$ = ±15V, and 5-minute warm-up in a normal convection environment unless otherwise noted.

PARAMETER	CONDITIONS	DAC65JP			DAC65KP			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
DIGITAL INPUTS								
Logic	12 Parallel Input Lines			ECL Compatible				
Resolution			12			*		Bits
ECL Logic Input Levels[1]: V_{IL}	Logic "0"	–0.81	–0.9	–0.98	*	*	*	V
I_{IL}		0.5	1.2	2	*	*	*	mA
V_{IH}	Logic "1"	–1.95	–1.79	–1.63	*	*	*	V
I_{IH}		0.5	1.2	2	*	*	*	mA
Logic Threshold: Voltage		–1.2	–1.3	–1.4	*	*	*	V
Current		1.5	2.3	3.2	*	*	*	mA
ANALOG OUTPUT								
Bipolar Output Current[2]	R_L = 0Ω		±6.25			*		mA
Bipolar Output Voltage[2]	R_L = ∞		±1.25			*		V
Output Resistance			200			*		Ω
Output Capacitance			3			*		pF
Internal Resistors: R_1	Pin 18 to Pin 20		750			*		Ω
R_2	Pin 18 to Pin 15		250			*		Ω
Ratio Accuracy	R_1/R_2		±0.05	±0.25		*	*	%
Absolute Accuracy	R_1, R_2		±0.25	±0.5		*	*	%
Output Noise	Static, All Bits On, BW = 10MHz		10			*		µVrms
TRANSFER CHARACTERISTICS								
Integral Linearity Error	V_O = ±1.25V		±0.25	±0.75		*	±0.5	LSB
			±0.006	±0.018		*	±0.012	% of FSR[3]
Differential Linearity Error	V_O = ±1.25V		±0.25	±0.75		*	±0.55	LSB
			±0.006	±0.018		*	±0.012	% of FSR
Bipolar Gain Error[4]	V_O = ±1.25V		±0.1	±0.25		*	*	%FSR
Trim Range	R_{TRIM} = 10kΩ		±5			*		mV
Bipolar Offset Error[4]	V_O = ±1.25V		±0.1	±0.15		*	*	%FSR
Trim Range	R_{TRIM} = 10kΩ		±3			*		mV
Monotonic	12 Bit		Guaranteed			Guaranteed		
Power Supply Rejection	Δ $\pm V_{CC}$ = ±14V to ±16V		±0.0012	±0.1		*	*	%FSR/%V_{CC}
SETTLING TIME								
Voltage Output:	R_L = 200Ω (Internal)							
1LSB Change	Settling to ±0.024% FSR		30	40		*	35	ns
Full Scale Change	Settling to ±1% FSR		17			*		ns
	±0.1% FSR		23			*		ns
	±0.024% FSR		30			*		ns
	±0.012% FSR		35			*		ns
Glitch Energy[5]	Major Carry		250			*		LSB-ns
REFERENCE								
Reference Output Voltage	No External Load	+7	+7.8	+8.6	*	*	*	V
Reference Temperature Drift	T_{MIN} to T_{MAX}		±40			*		ppm/°C
DYNAMIC PERFORMANCE[6]								
Spurious Free Dynamic Range	f_{CLOCK} = 20MHz							
f_C = 100kHz			–73			*		dBc
f_C = 1MHz			–70			*		dBc
f_C = 5MHz			–66			*		dBc
f_C = 100kHz	f_{CLOCK} = 35MHz		–71			*		dBc
f_C = 1MHz			–68			*		dBc
f_C = 5MHz			–61			*		dBc
Total Harmonic Distortion (THD)	f_{CLOCK} = 20MHz							
f_C = 1MHz			–68			*		dBc
Signal-to-Noise Ratio (SNR)	f_{CLOCK} = 20MHz							
f_C = 1MHz	BW = 10MHz		–70			*		dBc
Temperature DRIFT								
Bipolar Gain	T_{MIN} to T_{MAX}		±20	±40		*	*	ppm FSR/°C
Bipolar Offset	T_{MIN} to T_{MAX}		±10	±15		*	*	ppm FSR/°C
Integral Linearity Error	T_{MIN} to T_{MAX}		±0.5	±1		*	±0.75	LSB
			±0.012	±0.024		*	±0.018	% of FSR
Differential Linearity Error	T_{MIN} to T_{MAX}		±0.8	±1		*	±0.75	LSB
			±0.019	±0.024		*	±0.018	% of FSR
Ratio Accuracy, Internal R_1 and R_2	T_{MIN} to T_{MAX}		±20			*		ppm/°C
POWER SUPPLIES								
Rated Voltage	$\pm V_{CC}$		±15			*		V
Derated Performance	$\pm V_{CC}$	±13		±16	*		*	V
Current Quiescent: $+I_{CC}$	V_O = + Full Scale		+24	+30		*	*	mA
$-I_{CC}$	V_O = + Full Scale		–54	–65		*	*	mA
Power Dissipation	V_O = + Full Scale		1.2	1.43		*	*	W

SPECIFICATIONS (CONT)

ELECTRICAL

T_A = +25°C, $\pm V_{CC}$ = ±15V, and 5-minute warm-up in a normal convection environment unless otherwise noted.

PARAMETER	CONDITIONS	DAC65JP			DAC65KP			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
TEMPERATURE RANGE								
Specification	Ambient Temperature	0		+70	*		*	°C
Operating	Ambient Temperature	–40		+85	*		*	°C
θ_{JA} (7)			40			*		°C/W

* Same specification as for DAC65JP.

NOTES: (1) Logic input voltages and currents are dependent on the logic threshold voltage. The logic input values given in each column are correct for the logic threshold voltage given in that column. (2) The DAC65 is internally trimmed for ±1.25V output. The accuracy of ±6.25mA is about ±30% and its drift is about the same as the voltage output. (3) FSR is Full Scale Range, which is ±1.25V or 2.5V total. (4) Offset error is measured with all bits off (positive full scale = +1.25V) and is calculated as a percent of FSR = 2.5V. (5) Refer to Output Glitch section. (6) Measured in direct digital synthesizer (see Figure 9, application section). (7) Thermal resistance depends on many factors, such as whether or not DAC65 is mounted directly to a ground plane, how it is placed on the PC board, or if forced air cooling is used. (8) Specifications were characterized at +25°C and over temperature with an air flow of 8 cu ft/min.

ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE
DAC65JP	24-Pin Plastic DIP	0°C to +70°C
DAC65KP	24-Pin Plastic DIP	0°C to +70°C

ABSOLUTE MAXIMUM RATINGS

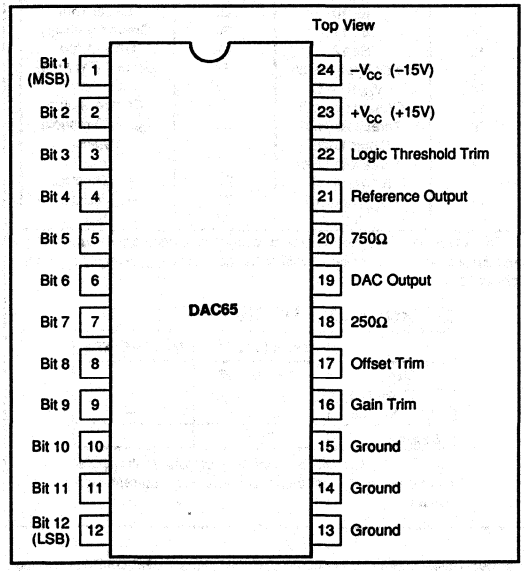
$\pm V_{CC}$	±18V
Logic Input	0V to –5.2V
Case Temperature	–40°C to +85°C
Junction Temperature	+150°C
Storage Temperature	–55°C to +125°C
Lead Temperature (soldering, 10s)	+300°C

Stresses above these ratings may permanently damage the device.

ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that this integrated circuit be handled and stored using appropriate ESD protection methods.

PIN CONFIGURATION

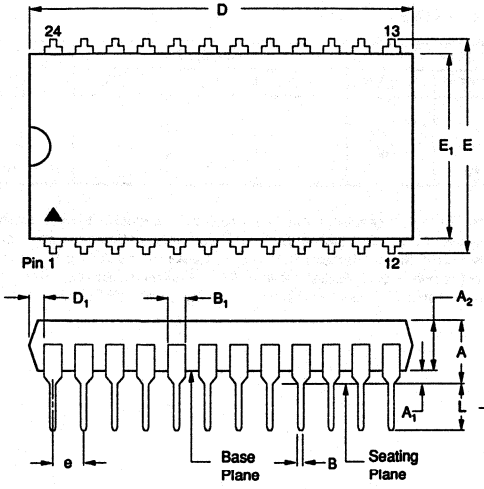


PIN DEFINITIONS

PIN NO	DESIGNATION	DESCRIPTION
1-12	ECL Data Input	12 parallel input data lines, ECL compatible.
13,14,15	Grounds	
16	Gain Trim	Input for externally adjusting gain error.
17	Offset Trim	Input for externally adjusting offset error.
18	250Ω	Internal resistor ratio matched to an internal 750Ω resistor for amplifying DAC output voltage with an external op amp.
19	DAC Output	DAC output voltage of ±1.25V or output current of ±6.25mA.
20	750Ω	Internal resistor ratio matched to an internal 250Ω resistor for amplifying DAC output voltage with an external op amp.
21	Reference Out	Reference output voltage of +7.8V.
22	Logic Threshold Trim	Input voltage for adjusting logic threshold.
23	$+V_{CC}$	Plus power supply, +15V.
24	$-V_{CC}$	Minus power supply, –15V.

MECHANICAL

P Package — 24-Pin Plastic, Double-Wide DIP



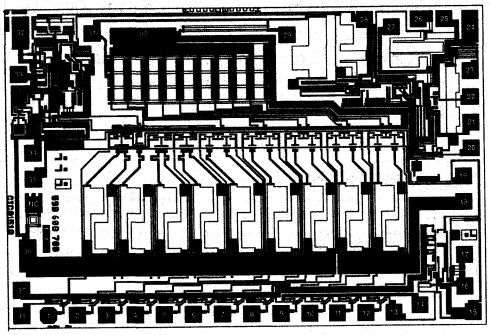
DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.155	.250	3.94	6.35
A_1	.015	.070	.381	1.78
A_2	.140	.185	3.57	4.70
B	.014	.022	.356	.559
B_1	.040	.070	1.02	1.78
C	.008	.015	.20	.381
D	1.235	1.265	31.37	32.13
D_1	.040	.100	1.020	2.540
E	.600	.625	15.24	15.88
E_1	.525	.565	13.34	14.35

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
e	.100 BASIC		2.54 BASIC	
eA	.600 BASIC		15.24 BASIC	
eB	.600	.700	15.24	17.78
L	.115	.200	2.91	5.08

NOTES:
(1) Not JEDEC Standard.
(2) Controlling dimension: INCH.
(3) Dimensioning and tolerancing per ANSI Y14.5M-1982.
(4) Dimensions A, A_1 and L are measured with package seated in JEDEC Seating Plane Gauge GS-3.
(5) D and E_1 does not include mold flash. Mold flash shall not exceed .010 inches, 0.25mm.
(6) eB and eC are measured at the lead tips with the leads unconstrained. eC must be zero or greater.

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

DICE INFORMATION



DAC65 DIE TOPOGRAPHY

PAD	FUNCTION	PAD	FUNCTION
1	Bit 1	20	Reference Filter
2	Bit 2	21	NC
3	Bit 3	22	NC
4	Bit 4	23	Gain Trim
5	Bit 5	24	Ground (Reference)
6	Bit 6	25	Ground (Power)
7	Bit 7	26	Reference Out
8	Bit 8	27	NC
9	Bit 9	28	$+V_{CC}$
10	Bit 10	29	Offset Trim
11	Bit 11	30	Ground (Analog)
12	Bit 12	31	DAC Output
13	Logic Bypass Cap	32	Ground (Op Amp)
14	$-V_{CC}$ (Logic)	33	Op Amp Compensation
15	Ground (Digital)		
16	Threshold Trim (Logic Low)	34	I_{SWITCH} Threshold Bypass
17	Threshold Trim (Logic High)	35	NC
		36	$-V_{CC}$ (Analog)
18	$-V_{CC}$ (Analog)	37	$-V_{CC}$ (Logic)
19	NC	38	NC

NC: Do not connect. Ground: All ground connections should be returned to a ground plane. VCC: All supplies should be bypassed using good high frequency techniques.

MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	150 x 103 ±5	—
Die Thickness	20 ±3	—
Min. Pad Size	5 x 5	—
Backing	Gold	

See "DICE PRODUCTS" Section 17 in Data Book Supplement Volume 33c, or contact Burr-Brown for current information.

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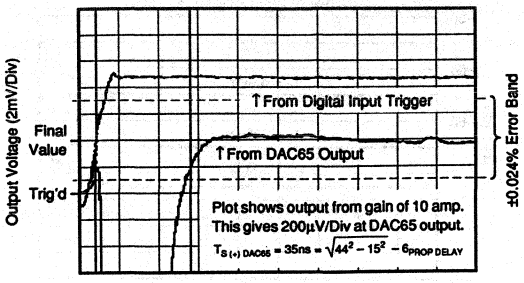
TYPICAL PERFORMANCE CURVES

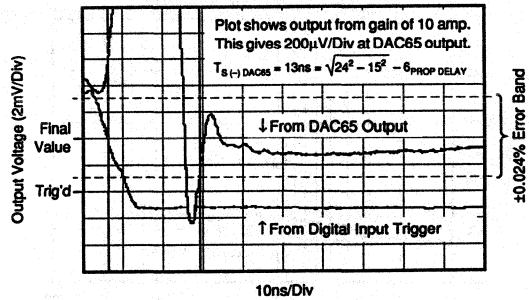
$\pm V_{CC}$ = ±15V, 5-minute warmup, and T_A = +25°C, unless otherwise noted.

POSITIVE FULL SCALE SETTLING TIME
(SEE SETTLING TIME SECTION CIRCUIT)



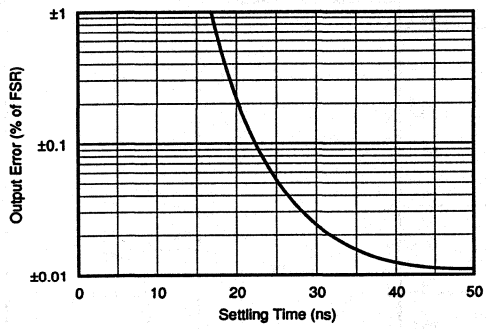
* Includes 15ns settling time from gain of 10 amplifier.

NEGATIVE FULL SCALE SETTLING TIME
(SEE SETTLING TIME SECTION CIRCUIT)

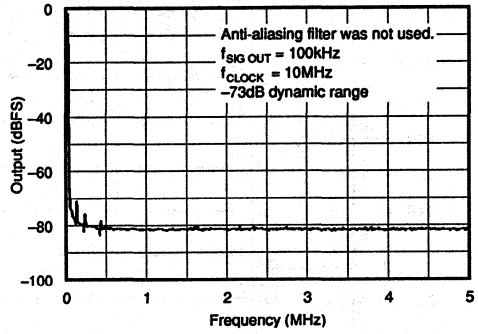


* Includes 15ns settling time from gain of 10 amplifier.

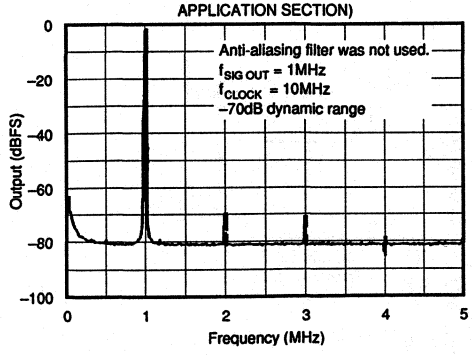
ACCURACY vs SETTLING TIME



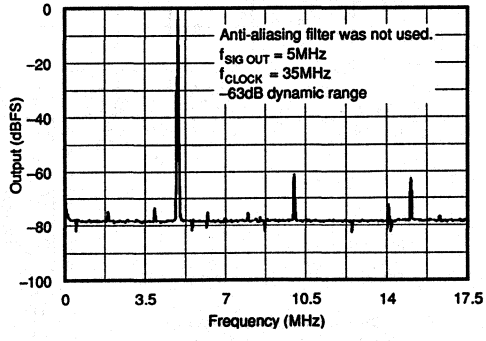
100kHz SPECTRAL PURITY
DIRECT DIGITAL FREQUENCY SYNTHESIZER CIRCUIT
(SEE DIRECT DIGITAL SYNTHESIZER
APPLICATION SECTION)



1MHz SPECTRAL PURITY
DIRECT DIGITAL FREQUENCY SYNTHESIZER CIRCUIT
(SEE DIRECT DIGITAL SYNTHESIZER
APPLICATION SECTION)



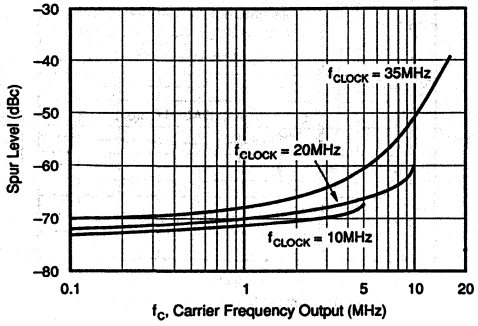
5MHz SPECTRAL PURITY
DIRECT DIGITAL FREQUENCY SYNTHESIZER CIRCUIT
(SEE DIRECT DIGITAL SYNTHESIZER
APPLICATION SECTION)



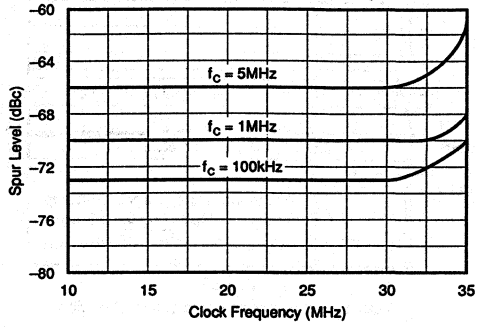
TYPICAL PERFORMANCE CURVES (CONT)

$\pm V_{CC}$ = ±15V, 5-minute warmup, and T_A = +25°C, unless otherwise noted.

SPURIOUS-FREE DYNAMIC RANGE vs CARRIER OUTPUT DIRECT DIGITAL SYNTHESIZER CIRCUIT WITH OUTPUT DEGLITCHER



SPURIOUS-FREE DYNAMIC RANGE vs CLOCK FREQUENCY DIRECT DIGITAL SYNTHESIZER CIRCUIT WITH OUTPUT DEGLITCHER (SEE APPLICATION SECTION)



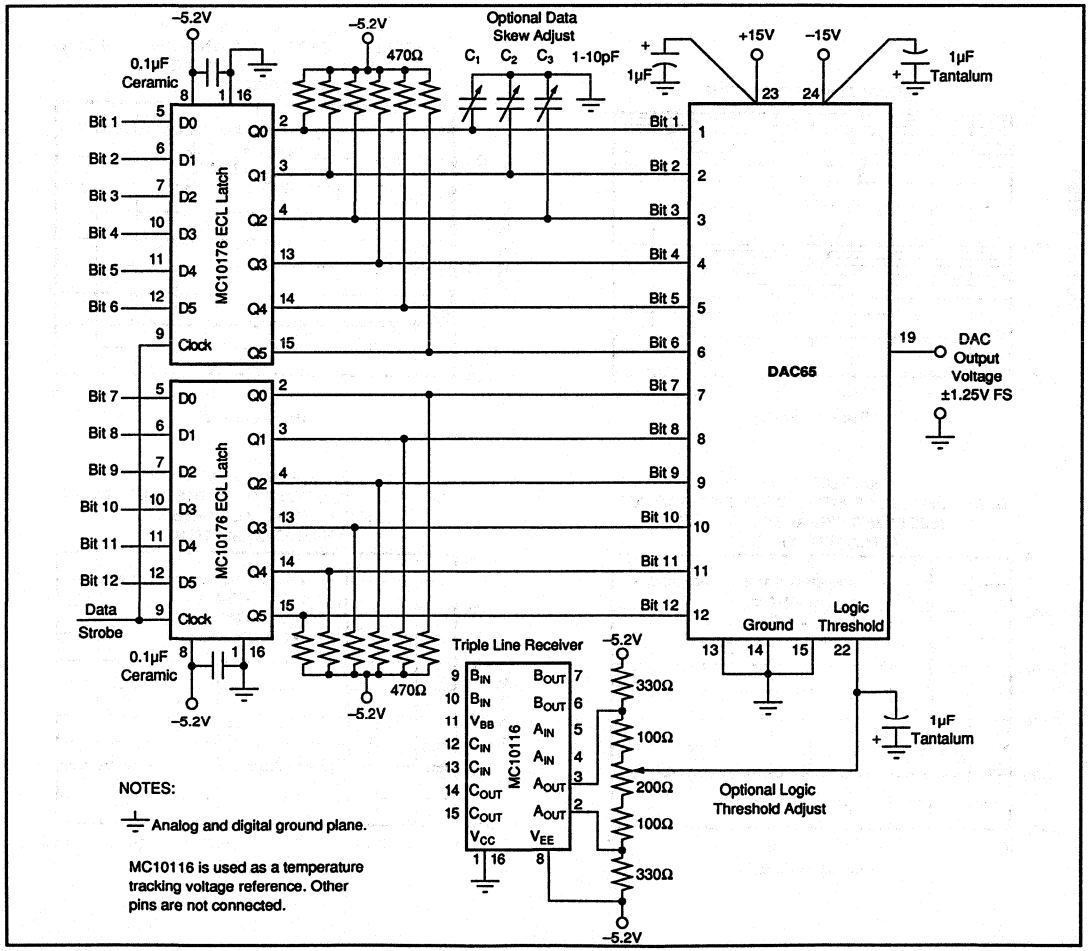


FIGURE 1. DAC65 Basic Connection Diagram Including Interface Latches and Glitch Adjust Circuitry.

THEORY OF OPERATION

The DAC65 is a laser-trimmed high-speed monolithic circuit. Internal capacitors are used to reduce the amount of external filtering required.

The DAC65 is comprised of 12 high-speed current switches which steer a reference current, of approximately ±6.25mA, into a 200Ω R-2R resistor ladder network. An accurate ±1.25V output voltage is produced at pin 19 by laser-trimming the reference voltage and ladder.

The reference voltage and output current have low drift. Integral linearity is trimmed to 14 bits.

INSTALLATION AND OPERATING INSTRUCTIONS

Figure 1 shows the basic connection for the DAC65.

Input ECL buffer latches shown are required and can also be used to adjust data skew to reduce output glitch energy (see output glitch section). In addition, logic threshold can be adjusted to optimize glitch and noise immunity (see logic threshold section). One ground plane is recommended for analog and digital signal returns as shown (see grounding section).

OPTIONAL OFFSET AND GAIN ADJUSTMENT

The offset and gain errors can be optionally adjusted to zero by using potentiometers shown in Figure 2. These points can be driven by low speed DACs to servo these errors to zero. If desired the trim pins maybe left unconnected.

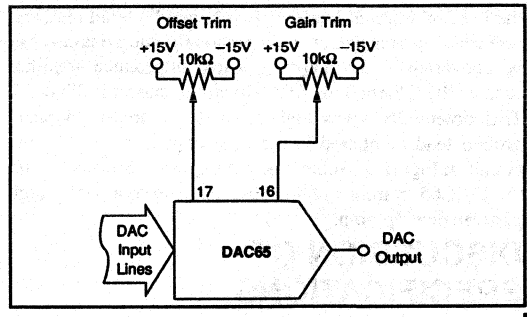


FIGURE 2. Optional External Offset and Gain Adjust.

LOGIC CODING TABLE, BOB, Bipolar Offset Binary

ECL Logic Coding	ECL Logic Voltage	V_{OUT} Bipolar	I_{OUT} Bipolar
000000000000	More Pos than −0.9V	−1.25V	−6.25mA
011111111111		0V	0mA
111111111111	More Neg than −1.79V	+1.25V	+6.25mA

ECL Logic Threshold is −1.3V.

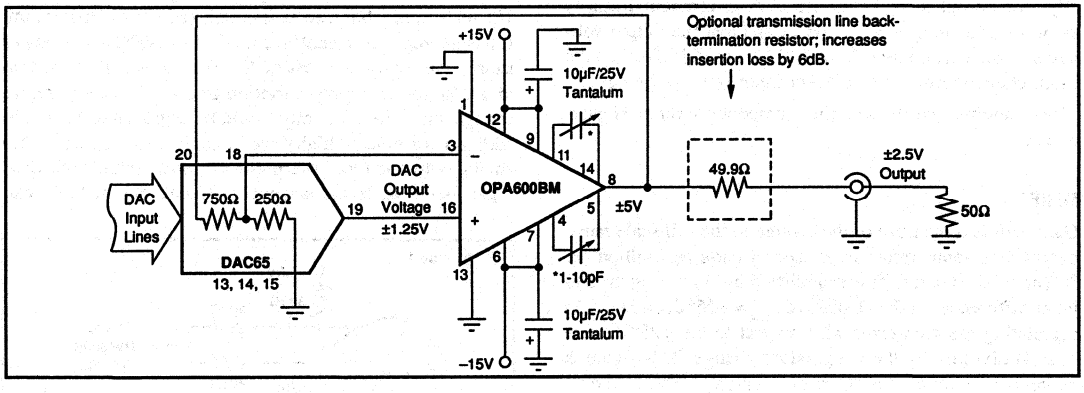


FIGURE 3. Optional Use of DAC65 Internal Resistors with External Amplifier/Cable Driver.

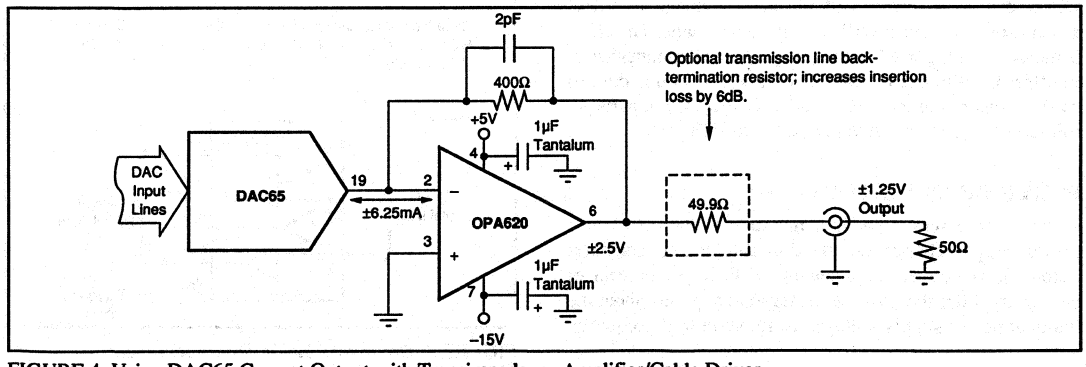


FIGURE 4. Using DAC65 Current Output with Transimpedance Amplifier/Cable Driver.

OPTIONAL EXTERNAL AMPLIFICATION

The ±1.25V at the output of the DAC65 can be accurately amplified by using the two thin film internal resistors with an external op amp shown in Figure 3. These resistors have been ratio-trimmed to high precision and are very stable over temperature. Also, since they will temperature-track the DAC65 internal ladder network, good overall temperature stability is achievable. Alternatively, the ±6.25mA can be converted to a voltage by a transimpedance amplifier such as the OPA600, or OPA620 circuit shown in Figure 4. This potentially gives higher speed due to the "virtual" ground load compared to the high impedance load of the circuit in Figure 3. Achieving settling times consistent with the DAC65 current output requires an exceptionally high performance op amp.

DISCUSSION OF SPECIFICATIONS

ACCURACY

Linearity of a digital-to-analog converter is one of the true measures of its performance. The linearity error of the DAC65 is specified over its entire temperature range. The analog output will not vary by more than ±1/2LSB from a best fit straight line over the specified temperature range.

Differential linearity error of a digital-to-analog converter is the deviation from an ideal 1LSB voltage change from one adjacent output state to the next. A differential linearity error specification of ±1/2LSB means that the output voltage step sizes can range from 1/2LSB to 3/2LSB when the input changes from one adjacent input state to the next.

Monotonicity over the specified temperature range is guaranteed.

DRIFT

Gain drift is a measure of the change in the full scale range output over temperature expressed in parts per million per °C (ppm/°C). Gain drift is established by: 1) testing the end point difference for the DAC65 at t_{MIN} = +25°C, and t_{MAX}; 2) calculating the gain error with respect to the +25°C value and; 3) dividing by the temperature change. This figure is expressed in ppm FSR/°C and is given in the electrical specifications (includes drift of internal reference).

Offset drift is a measure of the actual change in output around zero over the specified temperature range. The offset is measured at t_{MIN} = +25°C, and t_{MAX}. The maximum change in offset is referenced to the offset at +25°C and is divided by the temperature range. This drift is expressed in parts per million of full scale range per °C (ppm FSR/°C).

POWER SUPPLY SENSITIVITY

Power supply sensitivity is a measure of the effect of a power supply change on the digital-to-analog converter output. It is defined as a percent of FSR per percent of change in either the positive or negative supplies about the nominal power supply voltage. To improve high frequency noise rejection, each supply lead should be bypassed to ground as close to the unit as possible with a 1µF CS-type tantalum capacitor.

GROUNDING

Care must be exercised when grounding the DAC65 (pins 13, 14, and 15). In order to preserve the stated linearity and accuracy specifications, it is necessary to use the ground pins as the analog ground reference point. Any voltage drop that develops between any of these three pins and the actual ground reference point will degrade the performance of the DAC65. To achieve fast settling performance, it is recommended that pins 13, 14, and 15 be returned directly to a heavy copper ground plane. The analog ground should be located as close to the DAC65 as possible.

DIGITAL INTERFACE, LOGIC THRESHOLD, AND NOISE IMMUNITY

The DAC65 is compatible with conventional ECL logic families such as ECL 10k and 100k. Each DAC65 digital input is connected to the base of one side of a differential amplifier. The logic 0 input voltage is –1.79V with an input current of 1.2mA. The logic 1 input voltage is –0.9V with an input current of 1.2mA.

The logic threshold function of the DAC65 can be used to deal with noise in the ECL input-driving circuitry. The ECL 10k logic family has a noise immunity of 125mV maximum. It has a temperature coefficient of –1.4mV/°C and a power supply sensitivity of 16mV/%ΔV. With a realistic condition of a 5% power supply variation and a 25°C temperature change, the noise immunity would be degraded to 10mV. In addition, a precision high-speed digital-to-analog converter analog output is more susceptible to noise than is the ECL logic. Noise at levels acceptable to the digital logic can

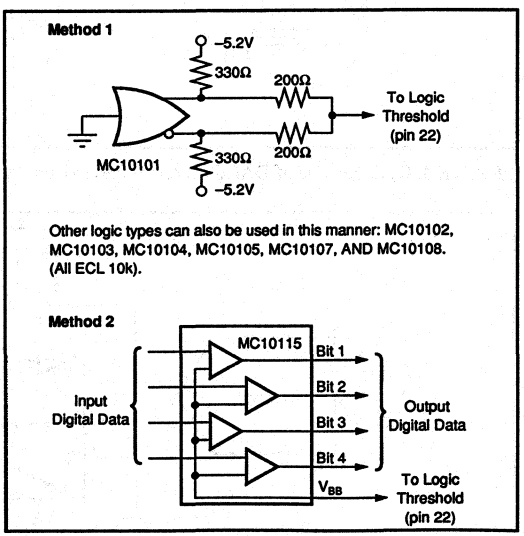


FIGURE 5. Driving the Logic Threshold Input.

couple through the D/A, resulting in an unacceptably noisy analog output. Low spurious output requires a clean digital input.

By making use of the logic threshold input feature, the threshold voltage of the DAC65 can be dynamically adjusted as the temperature and power supplies vary to give maximum noise immunity at the analog output over a wide range of conditions.

The MC10115 line receiver (or similar logic function) can be used to drive the DAC65 logic threshold, pin 22 (driven by the V_{BB} output of the ECL gate as shown in Figure 1). Refer to an ECL 10k data book for more detail. Figure 5 shows alternate methods for generating a logic threshold voltage.

SETTLING TIME

Settling time for the DAC65 is the total time required for the output to settle within an error band around its final value after a digital input change. This includes the digital delay of the internal switches.

The settling time of the DAC65 is determined by digitizing the output waveform produced by toggling the inputs between 011111111111 and 100000000000 continuously and verifying that the output settles to within ±1/2LSB in the specified time. The testing technique used is described in detail in Burr-Brown Application Note AN-115. Figure 6 shows a settling time circuit. The output amplifier, set to a gain of 10, is used to more easily observe the fast settling signal. Its gain, settling time, and propagation delay must be removed to arrive at the DAC65 performance.

Typical settling time curves of the DAC65 versus output error is shown in the Typical Performance Curves section. These curves are for digital code changes around the major carry. Typical output response characteristics of the DAC65 are also shown in the Typical Performance Curves section. Notice that these curves display the output of the gain of 10 amplifier from Figure 6. The unamplified DAC65 output is actually ten times smaller and is more difficult to observe due to noise.

In order to achieve minimum settling time, it is necessary to observe the following good high-frequency construction techniques:

1. The power supplies, including the logic threshold input (pin 22), should be bypassed by 1µF CS-type tantalum capacitors connected directly to the pins.
2. Use a heavy 2 ounce ground plane to connect common ground points.
3. Remove the ground plane beneath signal lines where it would add capacitance.
4. Separate analog and digital signal leads to avoid coupling of the digital signal into the analog paths.
5. Bring the source of the digital driving signal as close to the inputs of the DAC65 as possible. If the digital inputs are not clean, it will be necessary to reshape them using a latch or line drivers. Figure 1 shows how to interface the DAC65 to input latches. It is recommended that the logic power line be bypassed near the digital logic circuitry to achieve clean logic signals.
6. If possible, the DAC65 should be soldered directly into the printed circuit board although low profile sockets are acceptable.

OUTPUT GLITCH

"Glitch" is defined as the difference in the waveforms at the output of the DAC when data skew is present and when it is not. The measurement of glitch is accomplished by measuring the area between these two waveforms.

An output glitch of less than 250LSBns is achievable with the DAC65 because it employs ECL circuitry and current switches that have virtually identical delay times for input signals, making either positive or negative logic transitions. A glitch results when the digital data changes from one code to the next and the bits do not all switch at the same time. The delay time between the earliest and latest switching bits is called skew time. Typically during the skew time of the digital data, which includes the DAC switching, the digital code is undefined and the DAC output can go to any voltage between the full scale extremes. The glitch creates noisy output spurs and harmonics which can be troublesome in

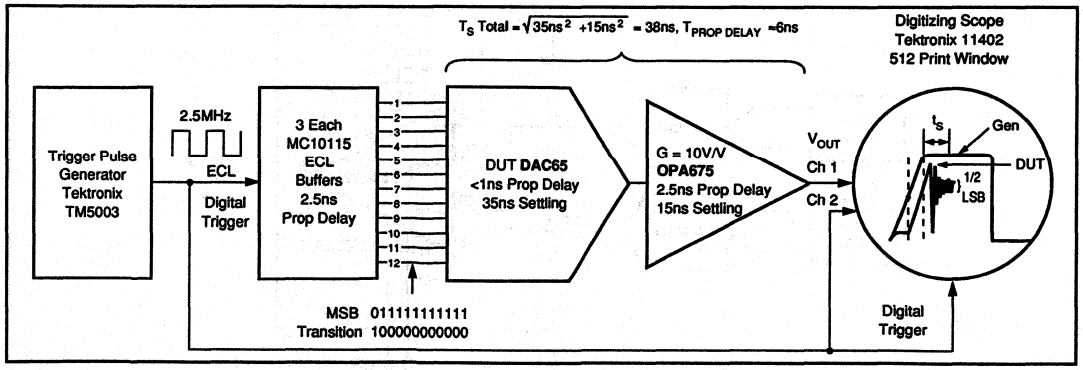


FIGURE 6. High Speed DAC65 Settling Time Test Circuit.

applications such as precision displays and complex waveform generation. Figure 7 is a photograph of a scope trace of the DAC output with a glitch occurring at the major carry transition.

The DAC65 design has been optimized for low glitch energy. However, a further reduction in the output glitch can be achieved by adjusting the skew of the higher order bits of the driving circuitry and by adjusting the logic threshold. This can be done by connecting a variable capacitor from the data lines to ground on each of the first three significant bits, as shown in Figure 1. More than three lines may be adjusted if desired. It will be necessary to create a driving digital code pattern that causes a major carry transition around these bits. It is convenient to use a digital ramp from a counter for this purpose. Initially set the logic threshold exactly half-way between logic 1 and a logic 0. This will be about –1.3V. Then examine the major carry transition associated with bit 3 and adjust the capacitor for minimum glitch. Make the same adjustment to bit 1. If done in this order, interactions will be minimized. Finally, fine tune the response by adjusting the logic threshold voltage (pin 22) for minimum glitch. It may be necessary to repeat this procedure once or twice for complete optimization.

Another approach is to apply a sinewave of amplitude that just toggles bit 3 with bits 32 and 1 at zero. Observe the spectrum on an analog spectrum analyzer and adjust C_3 for minimum amplitude of frequency spurs. Successively increase the sinewave amplitude and stop at each bit (bit 2 and bit 1) to adjust C_2 and C_1 for minimum spurs. This method assures lowest distortion by minimizing spurs caused by DAC output glitch.

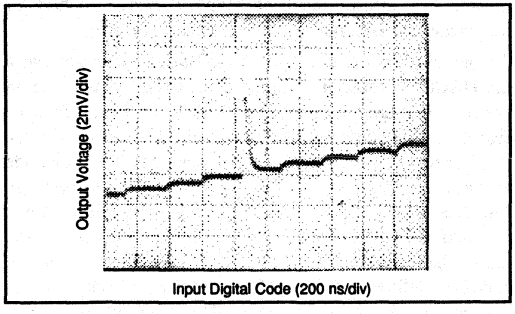


FIGURE 7. Typical Glitch Response at Major Carry Transition.

APPLICATIONS INFORMATION

The DAC65 can be used to reconstruct an analog signal at the output of a digital arbitrary waveform generator. It can be used without an external output amplifier or can be used with a 50Ω coaxial cable driver amplifier such as the OPA620, OPA621, or OPA600. ECL buffers can be used in addition to latches on the digital input to reduce high frequency noise on the ECL inputs from leaking through to the analog output.

TWO CHANNEL SWITCHED OUTPUT

Higher speed can be obtained from a direct digital frequency synthesizer by using two DAC65s in the circuit shown in Figure 8. DACs are ping-ponged and each DAC samples every other data point. While one DAC is settling on one sample, the other is being applied to the OPA675 (a switched input op amp used as a high speed buffered multiplexer). This circuit can be used to produce higher bandwidth signals or can be used as an output deglitcher when timed properly. Trimming or matching the two DACs may be required.

DIRECT DIGITAL SYNTHESIZER

The DAC65 can be used to construct a high quality direct digital synthesizer (DDS). Figures 9 and 10 show a Stanford Telecom STEL-1173 numerical controlled oscillator (NCO) with internal sinewave weighed ROM. DAC deglitching is done with a SHC600 sample/hold in Figure 9. Five potentiometers are used for skew timing adjust at the input in Figure 10. Test results shown in the Typical Performance Curves were generated by circuits shown in Figure 9. Output deglitching and data skew adjust can be used together for somewhat lower spur levels.

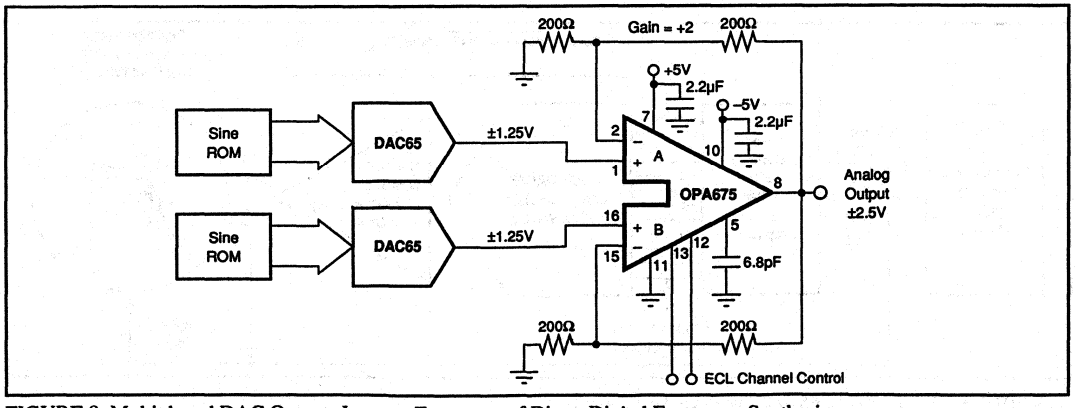


FIGURE 8. Multiplexed DAC Outputs Increase Frequency of Direct Digital Frequency Synthesizer.

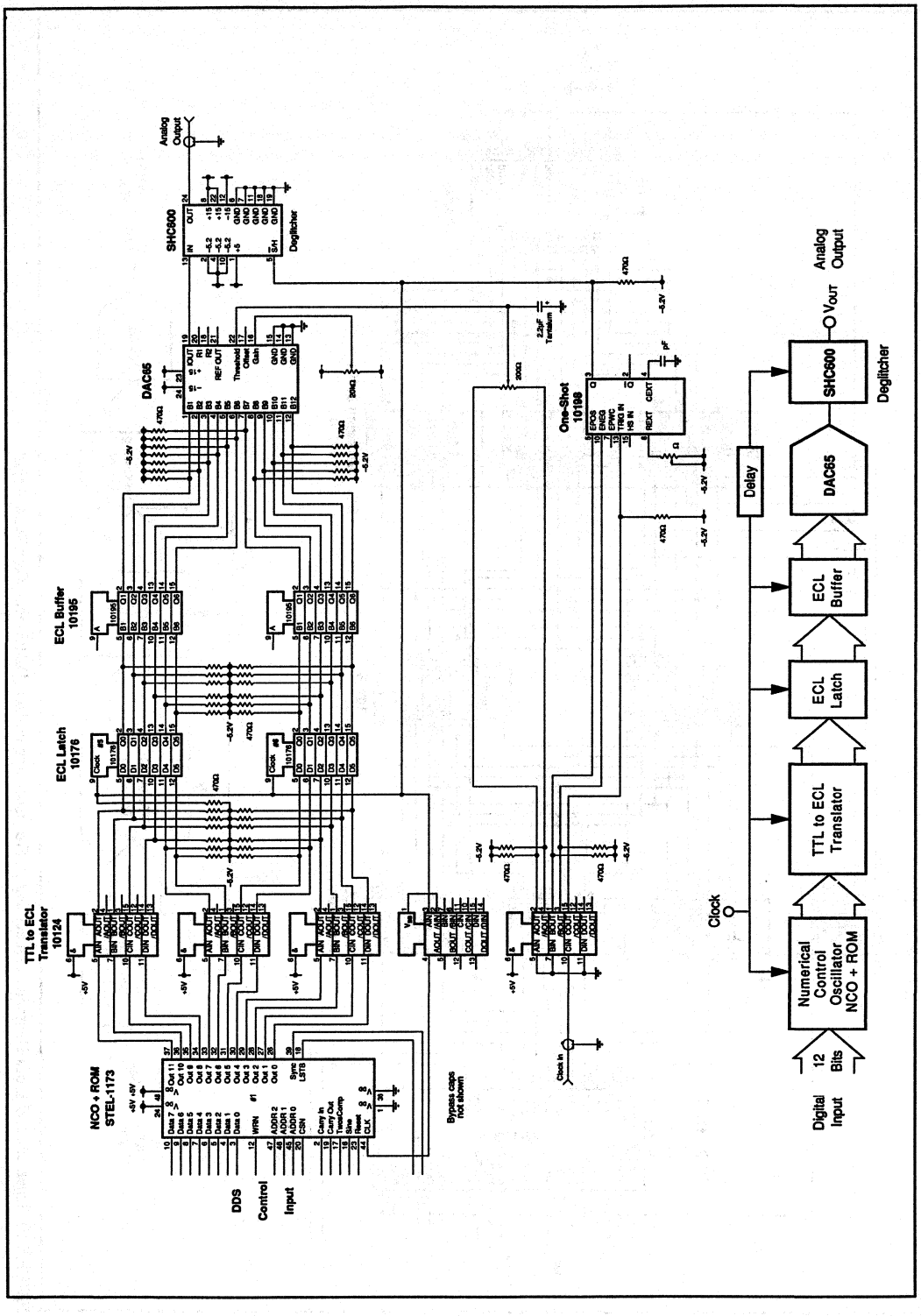


FIGURE 9. Schematic and Block Diagram of Direct Digital Frequency Synthesizer (DDFS) with Deglitched Output.

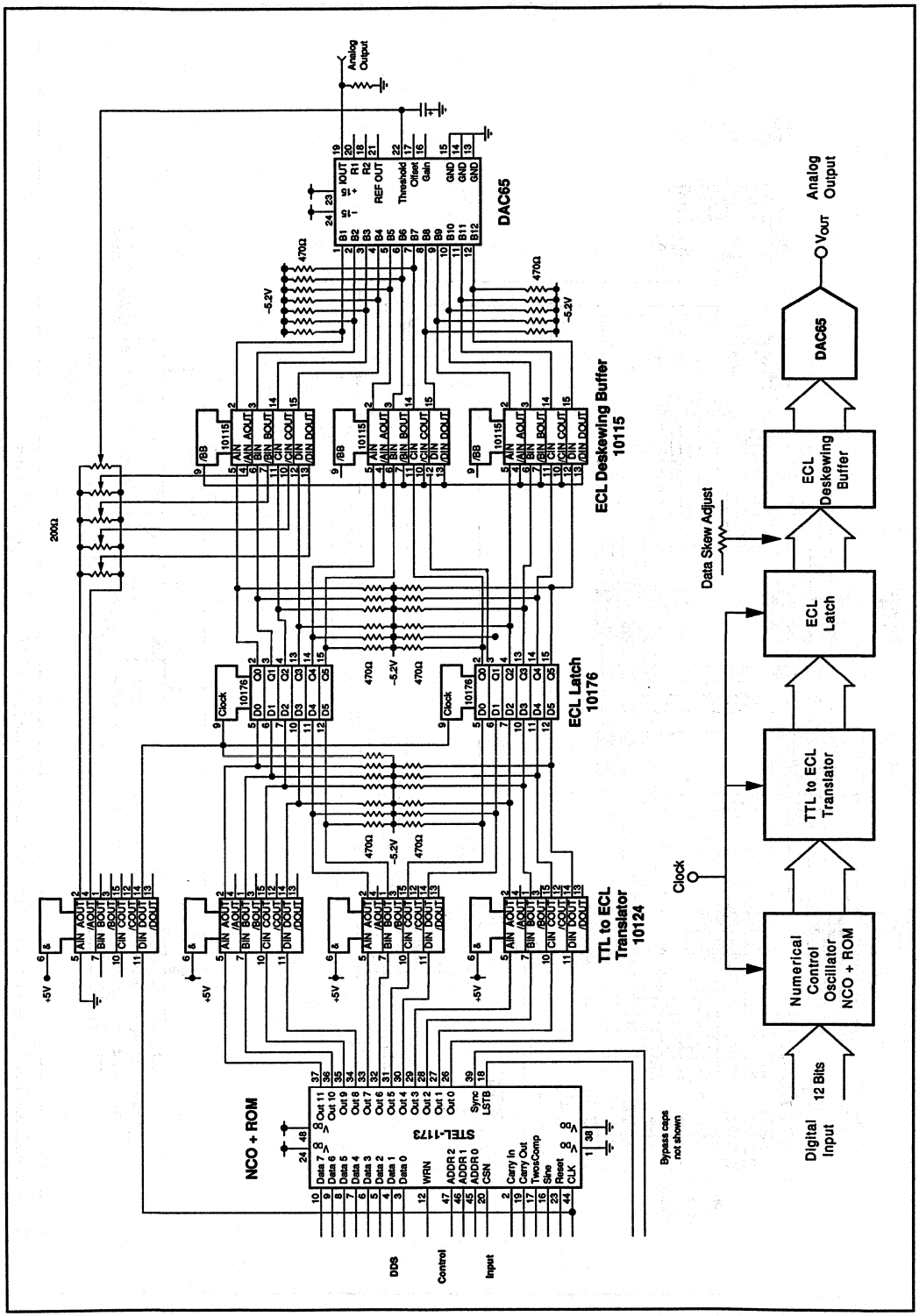


FIGURE 10. Schematic and Block Diagram of Direct Digital Frequency Synthesizer (DDFS) with Data Skew Adjust.

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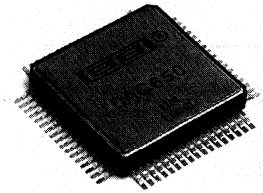


DAC650

ADVANCE INFORMATION
SUBJECT TO CHANGE

12-Bit 500MHz DIGITAL-TO-ANALOG CONVERTER

FEATURES

- 12-BIT RESOLUTION
- 500MHz UPDATE RATE
- LOW GLITCH — 20pVS
- FAST SETTLING: <5ns
- INTERNAL LATCH AND REFERENCE
- LASER TRIMMED ACCURACY
- SURFACE MOUNT PACKAGE

APPLICATIONS

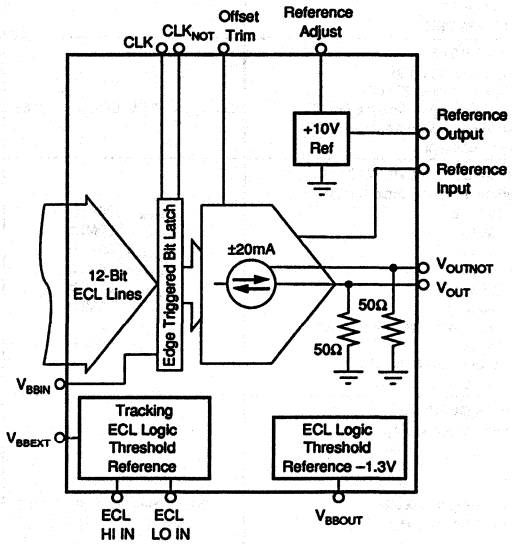
- DIRECT DIGITAL SYNTHESIS
- ARBITRARY WAVEFORM GENERATION
- HIGH RESOLUTION GRAPHICS
- COMMUNICATIONS LOCAL OSCILLATORS
  - Spread Spectrum
  - Base Stations
  - Digitally Tuned Receivers

DESCRIPTION

The DAC650 is a high performance 12-bit digital to analog converter for high frequency waveform generation. It is complete with an internal low drift reference and data latch. The internal segmentation and latching provide for minimal output glitch energy.

The ECL compatibility provides for low digital noise at high update rates. The 50Ω output resistance and low output capacitance simplify transmission line design and filtering at the output. Complementary outputs are offered for increased performance while driving transformers or differential amplifiers.

The DAC650 combines precision thin film and bipolar technology with high speed gallium arsenide to create a high performance, cost effective solution for modern waveform synthesis systems.



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Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL

At 25°C and rated supplies, unless otherwise noted.

PARAMETER	CONDITIONS	DAC650JL MIN	DAC650JL TYP	DAC650JL MAX	UNITS
DIGITAL INPUTS					
Logic	12 Parallel Input Lines	ECL			
Resolution				12	Bits
ECL Logic Input Levels[1]: V_{IL}	Logic "0"	–1.475	–1.8	–2	V
I_{IL}			1.0	10	µA
V_{IH}	Logic "1"	–1.115	–0.8	–0.6	V
I_{IH}			1.0	10	µA
Logic Threshold: Voltage		–1.2	–1.3	–1.4	V
DIGITAL TIMING					
Input Data Rate		DC		500	MHz
CLK Pulse Width High or Low		1			ns
Set-up Time			2.7		ns
Hold Time (Referred to CLK)			–700		ps
Propagation Delay			1.5		ns
ANALOG OUTPUT					
Bipolar Output Current	R_L = 0Ω		±20		mA
Bipolar Output Voltage	R_L = ∞		±1.0V		V
Output Resistance	V_{OUT}, V_{OUTNOT} to Ground		50		Ω
Output Capacitance			5		pF
Output Impedance Drift			50		ppm/°C
Absolute Accuracy			±0.25		%
TRANSFER CHARACTERISTICS					
Integral Linearity Error	Best Fit Straight Line		±0.024	±0.048	%FSR
Differential Linearity Error			±0.024	±0.048	%FSR
Bipolar Gain Error			±0.5	±1.0	%FSR
Bipolar Offset Error			±0.5	±1.0	%FSR
TIME DOMAIN PERFORMANCE					
Glitch Energy	Major Carry		20		pV-s
Output Rise/Fall Time			500		ps
Settling Time [2]					
±0.024% FSR	1 LSB Change		1		ns
±1% FSR	Full Scale Change		<5ns		ns
±0.1% FSR			TBD		ns
±0.024% FSR			TBD		ns
REFERENCES					
V_{BB} Input Range (Pin 1)		–1.4	–1.3	–1.2	V
$V_{BB\ INT}$ Reference (Pin 68)		–1.4	–1.3	–1.2	V
$V_{BB\ EXT}$ Tracking Reference (Pin 67)	$ECL_{HI\ IN}$ = –0.8V, $ECL_{LO\ IN}$ = –1.8V	–1.4	–1.3	–1.2	V
Internal Reference Voltage (Ref Out)			10	10.05	V
Ref In Resistance			4950		Ω
DYNAMIC PERFORMANCE [4]					
Spurious Free Dynamic Range					
f_O = 100kHz	f_{CLOCK} = 100MHz		70		dBFS[3]
f_O = 1MHz	f_{CLOCK} = 100MHz		68		dBFS
f_O = 25MHz	f_{CLOCK} = 100MHz		58		dBFS
f_O = 1MHz	f_{CLOCK} = 500MHz		TBD		dBFS
f_O = 25MHz	f_{CLOCK} = 500MHz		TBD		dBFS
f_O = 100MHz	f_{CLOCK} = 500MHz		TBD		dBFS
Total Harmonic Distortion (THD)					
f_O = 1MHz	f_{CLOCK} = 100MHz		–67		dBFS
Signal-to-Noise Ratio (SNR)					
f_O = 1MHz			TBD		dB
POWER SUPPLIES					
Supply Voltages: $+V_{CC}$	Operating, T_{MIN} to T_{MAX}	+13.5	+15	+16.5	V
$-V_{CC}$		–13.5	–15	–16.5	V
$+V_{DD1}$		+4.5	+5	+5.5	V
$-V_{DD2}$		–4.5	–5.2	–5.5	V
Power Supply Rejection	+25°C, All Supplies ±10% Change		0.05	0.08	%/%
Supply Currents: $+I_{CC}$	Operating, T_{MIN} to T_{MAX}		10	13	mA
$-I_{CC}$			–47	–50mA	mA
$+I_{DD1}$			53	57	mA
$-I_{DD2}$			–191	–245	mA
Power Consumption	Operating		2.0	2.6	W

SPECIFICATIONS (CONT)

ELECTRICAL

At 25°C and rated supplies, unless otherwise noted.

PARAMETER	CONDITIONS	DAC650JL MIN	DAC650JL TYP	DAC650JL MAX	UNITS
TEMPERATURE RANGE					
Specification: DAC650JL	Ambient	0		+70	°C
θ_{CA}			27		°C/W

NOTES: (1) V_{BBIN} (Pin1) connected to V_{BBINT} (Pin 68). (2) Settling time is influenced by load due to fast edge speeds. Use good transmission line techniques for best results. (3) dBFS is "dB referred to full scale."

ORDERING INFORMATION

MODEL	DESCRIPTION	TEMPERATURE RANGE (AMBIENT)
DAC650JL	68-Pin Ceramic, Gullwing Leads	0°C to +70°C

ABSOLUTE MAXIMUM RATINGS

$\pm V_{CC}$	±18V
Logic Input	+0.5V to –5.5V
Case Temperature	–40°C to +125°C
Junction Temperature	+150°C
Storage Temperature	–55°C to +125°C
Lead Temperature (soldering, 10s)	+300°C

Stresses above these ratings may permanently damage the device.

ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that this integrated circuit be handled and stored using appropriate ESD protection methods.

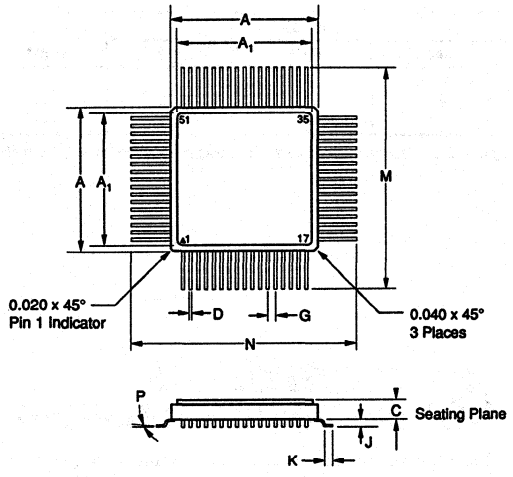
PIN DEFINITIONS

PIN NO	DESIGNATION	DESCRIPTION	PIN NO	DESIGNATION	DESCRIPTION
1	V_{BB}	Sets Logic Threshold for Bits 1-12	35	AGND	Ground for Analog Output Current
2	Bit 1	MSB	36	AGND	
3	Bit 2		37	AGND	
4	Bit 3		38	AGND	
5	Bit 4		39	V_{OUTNOT}	Complementary Output Voltage
6	Bit 5		40	V_{OUTNOT}	
7	Bit 6		41	V_{OUTNOT}	
8	Bit 7		42	AGND	
9	Bit 8		43	AGND	
10	Bit 9		44	AGND	
11	Bit 10		45	V_{OUT}	Output Voltage
12	Bit 11		46	V_{OUT}	
13	Bit 12	LSB	47	V_{OUT}	
14	V_{EE}	Logic Power (–5.2V Nominal)	48	AGND	
15	V_{EE}		49	AGND	
16	CLK	Clock	50	AGND	
17	CLK_{NOT}	Not Clock	51	AGND	
18	NC	No Connection	52	–15V	–15V Supply
19	V_{EE}		53	–15V	
20	V_{EE}		54	PWR GND	Ground for Analog Supplies
21	V_{EE}		55	+5V	+5V Supply
22	V_{EE}		56	+5V	+5V Supply
23	V_{EE}		57	V_{OS} ADJ	Offset Adjust
24	V_{EE}		58	PWR GND	Ground for Analog Supplies
25	V_{EE}		59	Ref_{ADJ}	Reference Out Adjust
26	V_{EE}		60	Ref_{OUT}	Reference Out (+10V, Buffered)
27	DGND	Ground for Logic	61	Ref_{IN}	Reference In (4.995kΩ)
28	DGND		62	+15V	+15V Supply
29	DGND		63	PWR GND	Ground for Analog Supplies
30	DGND		64	–5.2V Analog	Analog Power (–5.2V Nominal)(1)
31	DGND		65	ECL LO_{IN}	External ECL LOW input (optional)
32	DGND		66	ECL HI_{IN}	External ECL HI input (optional)
33	DGND		67	V_{BBEXT}	The buffered mean of LO_{EXT} and HI_{EXT}
34	DGND		68	V_{BBINT}	Internally generated –1.3V reference

NOTE: (1) Both the –5.2V Logic and –5.2V analog pins should be powered from a common supply.

MECHANICAL

?? Package — 68-Lead with Gull Wings



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.940	.960	23.88	24.38
A_1	.865	.875	21.97	22.23
C	.200 REF		4.81 REF	
D	.013	.025	0.33	0.64
G	.050 BASIC		1.27 BASIC	
J	.045	.055	1.14	1.40
K	.045 REF		1.14 REF	
M	1.200	1.220	30.48	30.99
N	1.200	1.220	30.48	30.99
P	0°	6°	0°	6°

NOTE: Formed leads shall be planar with respect to one another within 0.004 max at seating plane.

TECHNOLOGY OVERVIEW

The DAC650 uses a new design approach to achieve very fast settling time and high resolution. A unique mixed-technology design uses only two active chips: one gallium arsenide and the other silicon.

The GaAs MESFET die is used for those circuits which determine speed. This includes the latches, data decoders, and current switches. A silicon die with thin film is used for those circuits which determine accuracy, such as the precision references and current sources. The separate precision R-2R resistor ladders are laser trimmed to further increase the accuracy of the DAC650. A block diagram of the DAC650 is shown in Figure 1.

THEORY OF OPERATION

The DAC650 employs a familiar architecture where input bits switch on the appropriate current sources. Bits 1-3 are decoded into 7 segments before the first set of latches. A similar delay is given for the 9 least significant bits to minimize data skew. The edge triggered master-slave latches are driven by an internal clock buffer. This buffer placement has matched the clock lines to each of the 32 latches, thus minimizing output glitch energy.

There are 7 current sources for bits 1 to 3. Current sources for bits 4-8 are scaled down in binary fashion. These current sources are switched directly to the output of the R-2R ladder. Bits 9-12 are fed to the laser trimmed R-2R ladder for proper scaledown. The segmentation further minimizes output glitch which can cause spectral degradation.

The output current sees 50Ω of output impedance from the equivalent resistance of a R-2R ladder (100Ω) in parallel with 100Ω (Figure 1). With all of the current sources off, the output voltage is at +1V. With all current sources on (–40mA), the output voltage is at –1V. There is also a complementary V_{OUTNOT} output that allows for a differential output signals. The full scale complementary outputs (V_{OUT} and V_{OUTNOT}) can be simply modeled as ±20mA in parallel with 50Ω. This gives an output swing of 1Vp-p with an external 50Ω load.

REFERENCE/GAIN ADJUSTMENT

A precision +10V reference is included in the DAC650. A 50Ω resistor should be connected between REF_{IN} and REF_{OUT} for the specified unadjusted gain. Alternatively, an external reference may be used. However, the internal reference has been laser trimmed to minimize offset and gain drift. Multiple DACs may be run from one master reference by connecting a 50Ω resistor from each REF_{IN} to the master REF_{OUT}. A 100Ω potentiometer may be used in place of the 50Ω resistor in order to provide a ±1% gain adjustment range (Figure 2).

A wider adjustment range of ±20% may be achieved by connecting a 10kΩ potentiometer from REF_{OUT} to ground, with the wiper connected to the REF_{ADJ} pin. Adjusting the output to more than 40mA full scale may degrade high frequency performance and reliability due to higher current densities and operating temperature. Alternatively, lower full scale currents will affect operation because there is less current available to charge internal and external capacitances.

It should be noted that the gain adjust techniques mentioned above affect the current output and thus the voltage output from the DAC650. The voltage output will also be affected by an external load acting in parallel with the 50Ω output impedance.

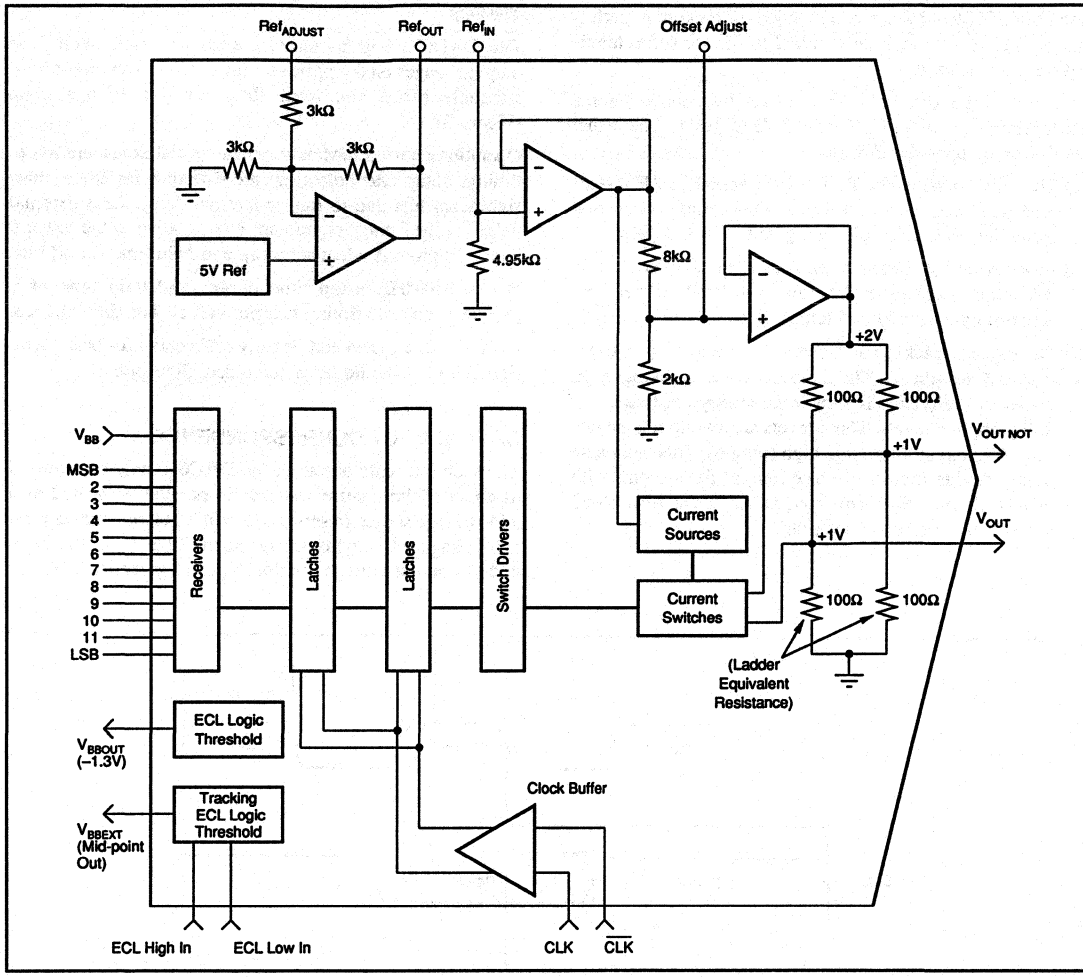


Figure 1. Functional Block Diagram of the DAC650.

OFFSET ADJUST

The offset may be adjusted by connecting a potentiometer between the +5V supply and ground with the wiper connected to the offset adjust pin. The voltage on this pin with no connection is about 2V, with an equivalent impedance of 1.6kΩ. A 10kΩ potentiometer will give the necessary adjustment range. The full scale range of the DAC output may be offset so it is not symmetrical around zero, but the full scale range must also be adjusted so that the output swing does not exceed ±1V. Connecting the offset adjust pin to ground gives a unipolar output of 0 to –2V (with no load) or 0 to –1V (with a 50Ω load). This also reduces the current requirements for the +5V supply by 20mA.

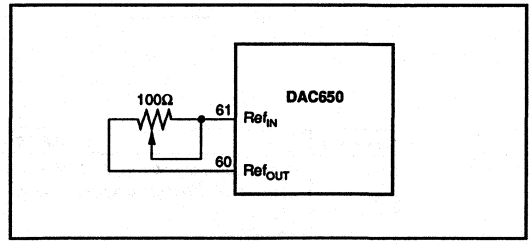


Figure 2. Using a Potentiometer for ±1% Gain Adjust.

DIGITAL INPUTS/LOGIC THRESHOLDS

The input logic levels and clock levels are ECL compatible. The data inputs are single ended ECL and the clock input is differential.

The internal impedance of the data and clock inputs is a high impedance (FET gate), and is clamped to the digital supply and ground to protect against ESD damage. ESD precautions should still be used when handling the DAC650.

At frequencies greater than 100MHz, transmission line techniques are recommended for data and clock inputs. A termi-

nation of 50Ω to –2V is recommended for maximum performance. For lower clock rates, 470Ω to –5V or series termination may be used.

The input data threshold level is set by connecting the appropriate voltage (–1.2V to –1.4V) to pin 1. The actual level may be provided 3 ways:

(1) The user connects the DAC650's internal –1.3V threshold reference directly to pin 1. This simple connection provides excellent noise margins for ECL levels.

(2) An external V_{BB} system reference is applied to pin 1. This technique may allow data threshold levels to track the system over supply and temperature variations.

(3) The internal tracking ECL threshold reference (pin 67) is applied to pin 1. The output of the tracking ECL threshold reference is simply the average of two externally applied levels. These levels are a system logic low (pin 65) and system logic high (pin 66). This technique may provide increased noise margin for systems with levels slightly different from ECL. Leave pins 65-67 open if this option is not used.

TIMING

The DAC650 has an internal edge triggered latch. The output changes on the positive edge of CLK. Data must have adequate setup and hold time for proper operation (Figure 3).

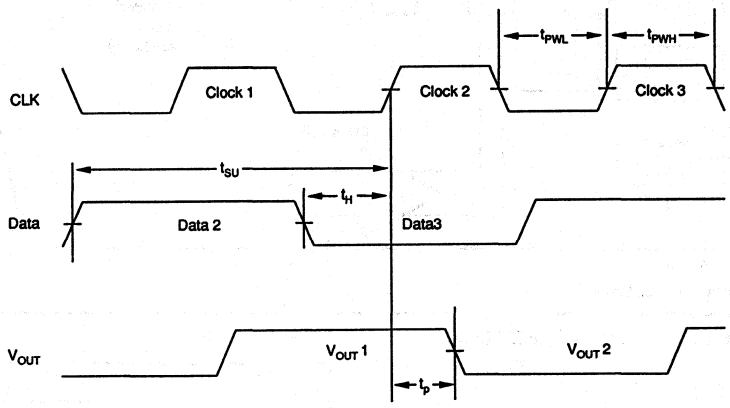
Operation above 250MHz requires special consideration to timing. Setup and hold time are different for the 3 most significant bits due to longer internal delay. Less external delay for the 3 most significant bits (relative to the lower 9 bits) will provide adequate setup and hold time for all bits.

Below 250MHz, setup time of 4ns and hold time of 0 provides adequate timing margin with all bits time aligned.

CLK and CLK_{NOT} should be truly differential for best operation, i.e. they should have coincident 50% points.

DATA IN/VOUT CORRESPONDENCE

The each full scale output of the DAC650 may be modeled as either ±20mA current source in parallel with 50Ω or a ±1V voltage source in series with 50Ω. The nominal current and voltage bit weights are given in Table I and the input code vs output voltage relationships are given in Table II.



SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_P	Propagation delay. 50% of CLK to 50% of V_{OUT}.		1.5		ns
t_{SU}	Setup time DATA must remain stable before CLK (50% of CLK to 50% of Data).				
	Bits 1-3		2.7		ns
	Bits 4-12		1		ns
t_H	Hold time DATA must remain stable after CLK (50% of DATA to 50% of CLK).				
	Bits 1-3		–1		ns
	Bits 4-12		–300		ps
t_{PWL}	CLK pulse width low (50% to 50%).		1		ns
t_{PWH}	CLK pulse width high (50% to 50%).		1		ns

Figure 3. Timing Diagram for the DAC650.

Transmission line techniques at the output are also recommended to minimize ringing and glitching. Ideally, both of the outputs should see the same termination, including any delay between the DAC650 and the load.

Since the outputs V_{OUT} and V_{OUTNOT} are equal in magnitude but opposite in sign, they are ideal for driving RF transformers (Figures 4, 5, 6.) The primary may be connected between the two outputs. The secondary may be floating or referenced to ground. This results in a 2X signal power and some cancellation of clock feedthrough, glitching, and distortion.

If only one output is used, the unused output should be terminated identically. If the terminations cannot be identical and the unused output must be unterminated, the termination for the used output should be as close as possible to the DAC650.

LAYOUT AND POWER SUPPLIES

A multilayer PC board with a solid ground and power planes is recommended. An example of a typical circuit configuration and layout is given in Figures 7 and 8. The DAC650 has multiple ground pins to minimize pin impedances. All of the ground pins (analog and digital both) should be connected directly to the analog ground plane at the DAC650.

Wide busses for the power paths are recommended as good general practice. There are several internal power supply bypass capacitors, but external bypassing is still recommended. A 10µF ceramic capacitor in parallel with a 0.01µF chip capacitor will be sufficient in most applications.

Pin 64, Analog V_{EE}, should be connected to the same supply as the digital V_{EE} pins (–5.2V).

BIT	VOLTAGE (No External Load)	CURRENT
1	1V	20mA
2	.5V	10mA
3	0.25V	5mA
4	0.125V	2.5mA
5	62.5mV	1.25mA
6	31.25mV	625µA
7	15.625mV	312.5µA
8	7.8125mV	156.25µA
9	3.9063mV	78.125µA
10	1.9531mV	39.06µA
11	976µV	19.53µA
12 (LSB)	488µV	9.76µA

Table I. Nominal Bit Weight Values.

INPUT BITS 1 2 3 4 5 6 7 8 9 10 11 12	V_{OUT}	NV_{OUT}
0 0 0 0 0 0 0 0 0 0 0 0	+1.000	–1 + 488µV
0 0 0 0 0 0 0 0 0 0 0 1	+1 – 488µV	–1 + 976µV
0 0 0 0 0 0 0 0 0 0 1 0	+1 – 976µV	–1 + 1.464mV
•		
•		
•		
•		
0 1 0 0 0 0 0 0 0 0 0 0	0.50	–0.50 + 488µV
1 0 0 0 0 0 0 0 0 0 0 0	0.000	+488µV
1 1 1 1 1 1 1 1 1 1 1 1	–1 + 488µV	+1.000

Table II. Input Code vs Output Voltage Relationships.

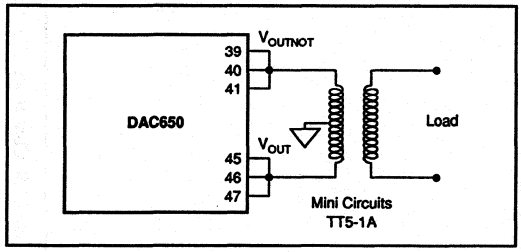


Figure 4. Using an RF Transformer at the Output of the DAC650. Filtering the Outputs Before the Transformer Improves the Performance in Some Applications.

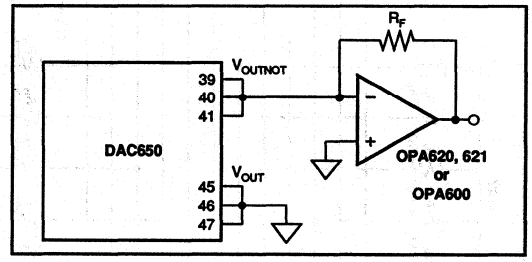


Figure 5. A High Speed Single Ended Amplifier at the Output. The Gain is $-R_F/50\Omega$.

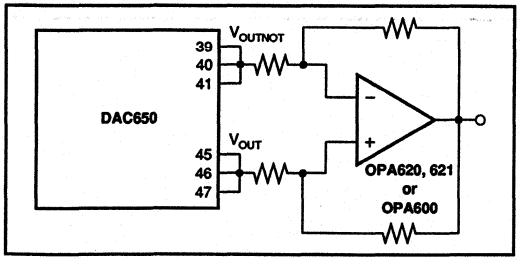


Figure 6. A High Speed Differential Amplifier at the Output.

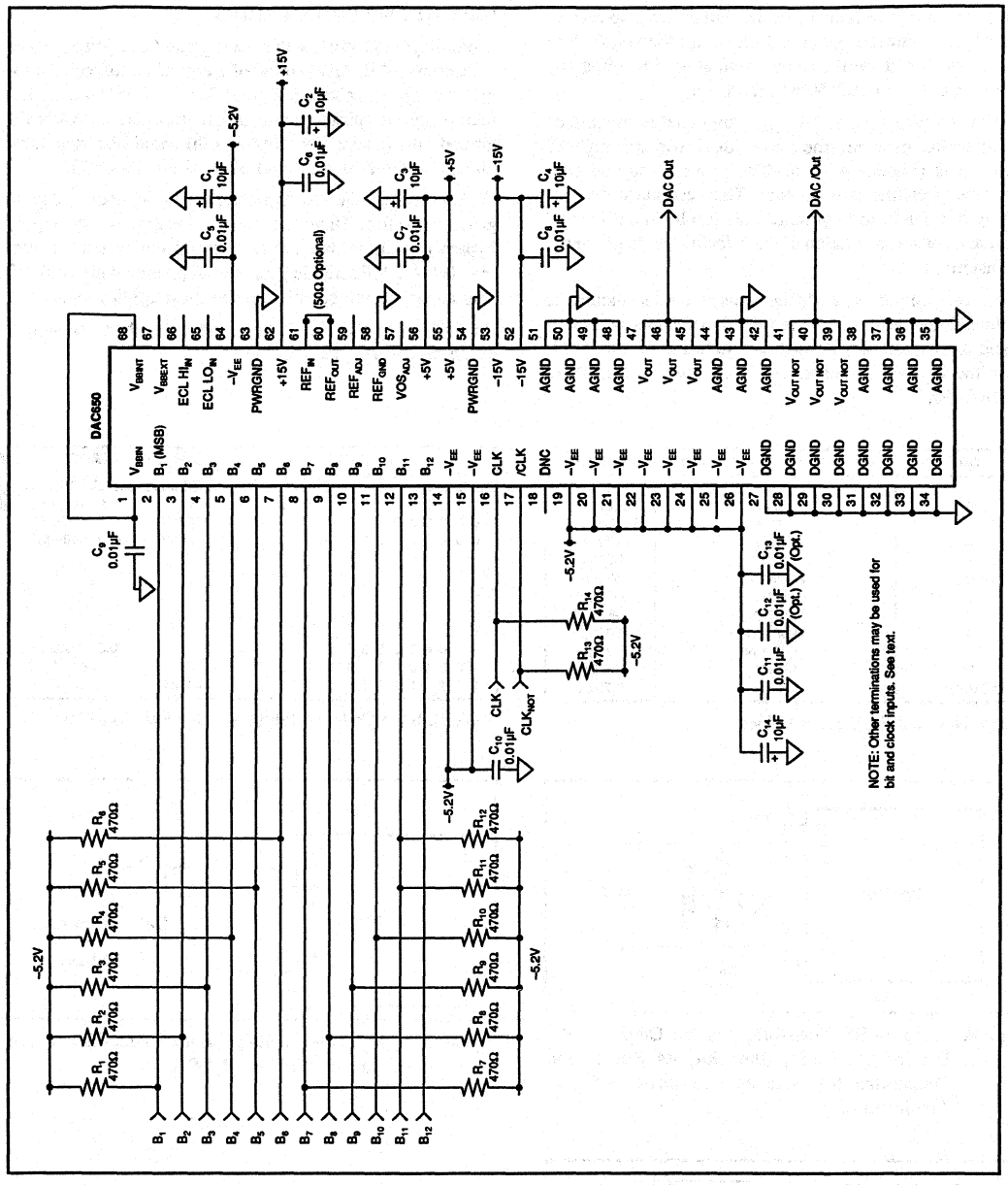
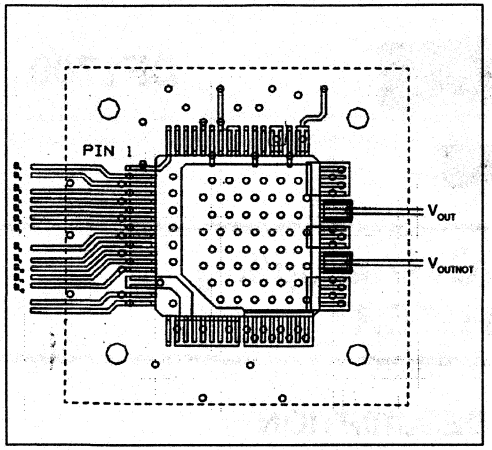
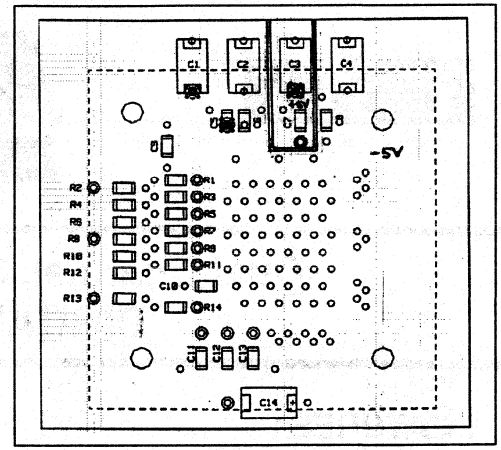


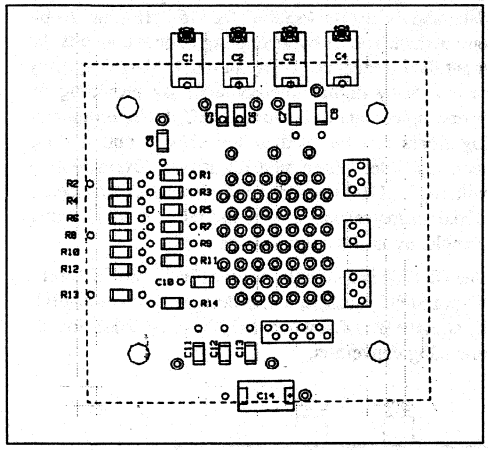
FIGURE 7. Typical DAC650 Connection Diagram.



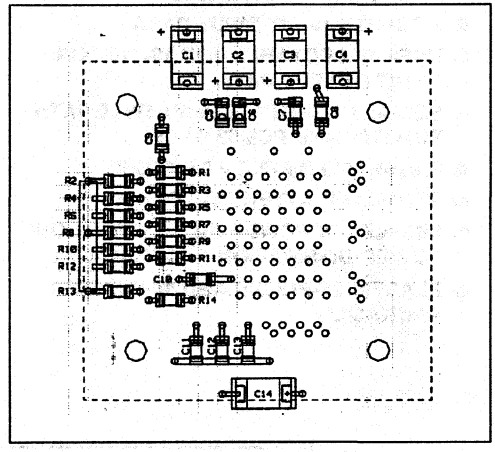
PC Board , Signal Layer (Layer 1, Top Layer, Top View).



–5V and +5V Planes (Layer 2).



Ground Plane, (Layer 3).



Solder Side (Layer 4, Bottom Layer, Top View).

FIGURE 8. Suggested PC Board Layout. (Not to scale.)

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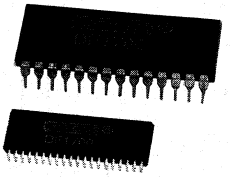


DF1700

Dual Channel, 8x Oversampling DIGITAL FILTER

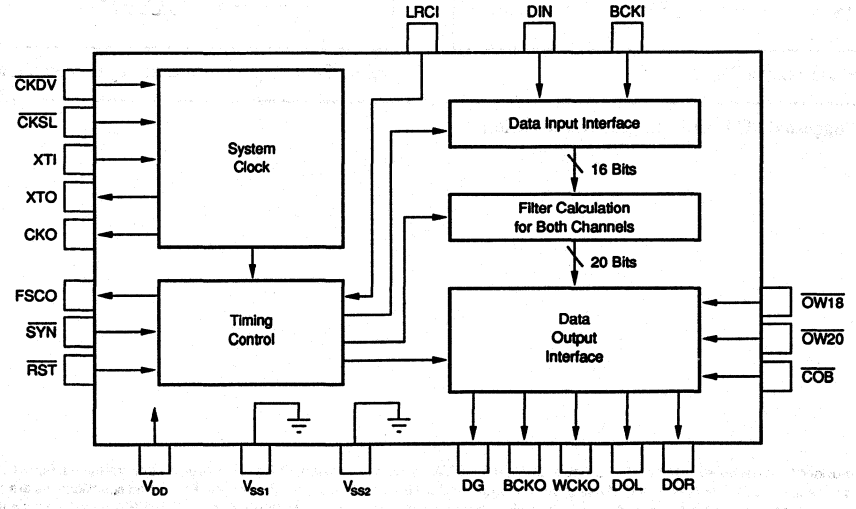
FEATURES

- DUAL CHANNEL DIGITAL INTERPOLATION FILTERS
- ACCEPTS 16-BIT INPUT DATA
- USER-SELECTABLE FOR 16-, 18-, OR 20-BIT OUTPUT DATA
- SERIAL OUTPUT IS COMPATIBLE WITH PCM1700 AND PCM63 DACs
- PASSBAND RIPPLE < 0.00005dB
- STOPBAND ATTENUATION > 110dB
- SINGLE +5V POWER SUPPLY FOR LOW POWER DISSIPATION OF 250mW Max
- PLASTIC 28-PIN DIP AND 40-PIN SOIC PACKAGES

DESCRIPTION

The DF1700 is a high performance, 8x oversampling CMOS digital filter. This filter accepts 16-bit input data and is user-selectable for 16-, 18-, or 20-bit output data. The 8x oversampling feature converts the input data frequency (fs) to an output data frequency of 8 x fs by digital interpolation. By providing 8x oversampled data to an audio DAC, lower order analog filters can be used at the DAC's output, thus reducing filter phase non-linearities. Oversampling with the DF1700 simultaneously improves the fidelity of the analog reconstruction and reduces analog filter complexity at the output of the DAC.

The DF1700 is available in a plastic 28-pin DIP and a 40-pin SOIC package, and is designed for compatibility with the Burr-Brown PCM1700 and PCM63 digital-to-analog converters.

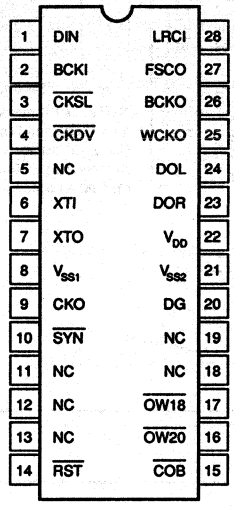


International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

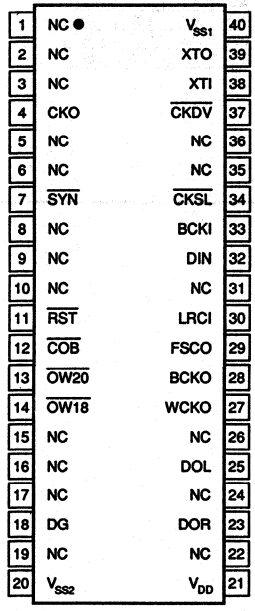
PDS-1093

PIN CONFIGURATION

P Package—28-Pin Plastic DIP (Top View)



U Package—40-Pin Plastic SOIC (Top View)



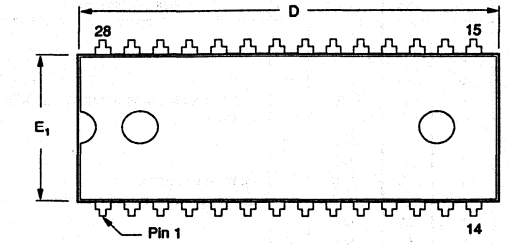
PIN DESCRIPTION

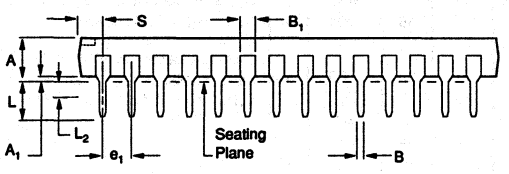
PIN NUMBER SOIC	PIN NUMBER DIP	NAME	I/O[1]	DESCRIPTION
1	–	NC	–	
2	–	NC	–	
3	–	NC	–	
4	9	CKO	O	Clock output (same frequency as XTI input clock).
5	–	NC	–	
6	–	NC	–	
7	10	SYN	I	H: Free-running mode; L: Forced synchronizing mode.
8	11	NC	–	
9	12	NC	–	
10	13	NC	–	
11	14	RST	I	H: Normal operation; L: System reset.
12	15	COB	I	Select output data format— H: Two's complement; L: Complemented offset binary (COB).
13	16	OW20	I	Select number of output data bits.[2]
14	17	OW18	I	Select number of output data bits.[2]
15	–	NC	–	
16	18	NC	–	
17	19	NC	–	
18	20	DG	O	Deglitch control clock.
19	–	NC	–	
20	21	V_{SS2}	–	Ground 2.
21	22	V_{DD}	–	Supply voltage (+5V).
22	–	NC	–	
23	23	DOR	O	Rch serial data output (8fs rate).
24	–	NC	–	
25	24	DOL	O	Lch serial data output (8fs rate).
26	–	NC	–	
27	25	WCKO	O	Output timing control (word clock).
28	26	BCKO	O	Output timing control for serial data (bit clock).
29	27	FSCO	O	Internal timing clock (fs rate)
30	28	LRCI	I	Multiplex clock for Lch/Rch input data (fs rate)—H: Lch; L: Rch.
31	–	NC	–	
32	1	DIN	I	Serial data input.
33	2	BCKI	I	Timing clock for serial input data.
34	3	CKSL	I	Select system clock.[2]
35	–	NC	–	
36	5	NC	–	
37	4	CKDV	I	Select system clock.[2]
38	6	XTI	I	Input for oscillator or external clock (system clock).
39	7	XTO	O	Output for oscillator; not connected when using external clock.
40	8	V_{SS1}	–	Ground 1.

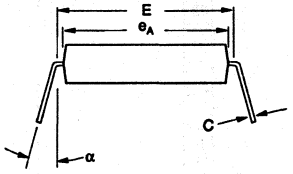
NOTES: (1) I = Input terminal; O = Output terminal. (2) Refer to the Functional Description section for details.

MECHANICAL

P Package — 28-Pin Plastic DIP







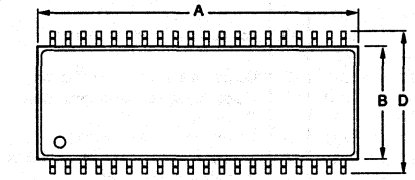
DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A(1)	.169	.200	4.29	5.08
A1(1)	.015	.070	0.38	1.78
B	.015	.020	0.38	0.51
B1	.015	.055	0.38	1.40
C	.008	.012	0.20	0.30
D(1)	1.380	1.455	35.05	36.96
E	.600	.625	15.24	15.88
E1(1)	.485	.550	12.32	13.97
e1	.100 BASIC		2.54 BASIC	
eA	.600 BASIC		15.24 BASIC	

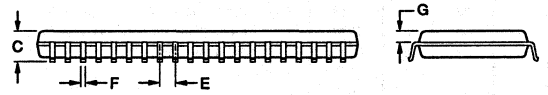
DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
L	.100	.200	2.54	5.08
L2	.000	.030	0.00	0.76
α	0°	15°	0°	15°
S(1)	.040	.080	1.02	2.03

(1) Not JEDEC Standard

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.

U Package — 40-Pin Plastic SOIC





DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.036	1.059	26.30	26.90
B	.362	.378	9.20	9.60
C	.099	.107	2.50	2.70
D	.453	.476	11.50	12.10
E	.042	.058	1.07	1.47
F	.012	.020	0.30	0.50
G	.043	.051	1.10	1.30

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

DC SPECIFICATIONS

ELECTRICAL

DIGITAL CHARACTERISTICS: V_{DD} = 4.75V to 5.25V, V_{SS} = 0V, T_A = –20°C to +70°C unless otherwise specified.

PARAMETER	PIN	SYMBOL	CONDITION	DF1700P/U MIN	DF1700P/U TYP	DF1700P/U MAX	UNITS
INPUT							
Logic Family					CMOS		
Logic Voltages	XTI	V_{IL1}				$0.3V_{DD}$	V
	XTI	V_{IH1}		$0.7V_{DD}$			V
	(1)	V_{IL2}				0.5	V
	(1)	V_{IH2}		2.4			V
Input Leakage Current	XTI	I_{LH}	$V_{IN} = V_{DD}$		10	20	µA
	XTI	I_{LL}	$V_{IN} = 0V$		10	20	µA
	(1)	I_{LH}	$V_{IN} = V_{DD}$			1	µA
Input Current	(1)	I_{IL}	$V_{IN} = 0V$		10	20	µA
OUTPUT							
Logic Family					CMOS		
Logic Voltages	(2)	V_{OL}	I_{OL} = 1.6mA			0.4	V
	(2)	V_{OH}	I_{OH} = –0.4mA	2.5			V
POWER SUPPLY REQUIREMENTS							
Supply Voltages		V_{DD}		4.75	5	5.25	V
Supply Current		I_{DD}	V_{DD} = 5V, F_{SYS} (3)			45	mA
Power Dissipation		P_D	Nominal V_{DD}			250	mW
TEMPERATURE RANGE (Ambient, T_A)							
Specification				–20		70	°C
Operating				–20		70	°C

NOTES: (1) Refers to pins LRCI, DIN, BCKI, $\overline{CKSL}$, $\overline{CKDV}$, $\overline{SYN}$, $\overline{RST}$, $\overline{COB}$, $\overline{OW20}$, and $\overline{OW16}$. (2) Refers to pins CKO, DG, DOL, DOR, WCKO, BCKO, and FSCO. (3) F_{SYS} is the frequency of the internal system clock. $F_{SYS} = F_{XTI}$ with $\overline{CKDV}$ = H and $F_{SYS} = F_{XTI}/2$ with $\overline{CKDV}$ = L.

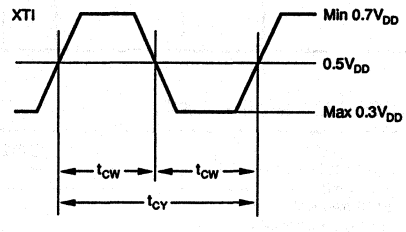
AC SPECIFICATIONS

ELECTRICAL

V_{DD} = 4.75V to 5.25V, V_{SS} = 0V, T_A = –20°C to 70°C unless otherwise specified.

PARAMETER	SYMB	CONDITION $\overline{CKSL}$	CONDITION $\overline{CKDV}$	CONDITION x fs(1)	DF1700P/U MIN	DF1700P/U TYP	DF1700P/U MAX	UNITS
XTI TERMINAL								
CRYSTAL OSCILLATOR								
Oscillating Frequency	f_{MAX}	H	H	192	1		13	MHz
	f_{MAX}	H	L	384	2		26	MHz
	f_{MAX}	L	H	256	1		13	MHz
	f_{MAX}	L	L	512	2		26	MHz
EXTERNAL CLOCK								
Clock Pulse Width	t_{CW}	H	H	192	35		500	ns
	t_{CW}	H	L	384	15		250	ns
	t_{CW}	L	H	256	35		500	ns
	t_{CW}	L	L	512	15		250	ns
Clock Period	t_{CY}	H	H	192	76		1000	ns
	t_{CY}	H	L	384	38		500	ns
	t_{CY}	L	H	256	76		1000	ns
	t_{CY}	L	L	512	38		500	ns

Timing Waveform



NOTES: (1) fs = sampling frequency.

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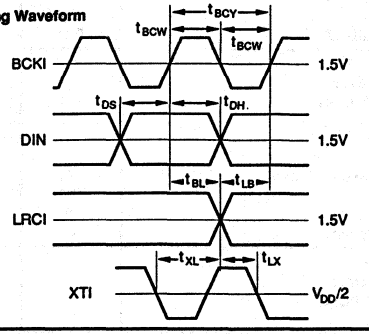
AC SPECIFICATIONS (CONT)

ELECTRICAL

V_{DD} = 4.75V to 5.25V, V_{SS} = 0V, T_A = –20°C to 70°C unless otherwise specified.

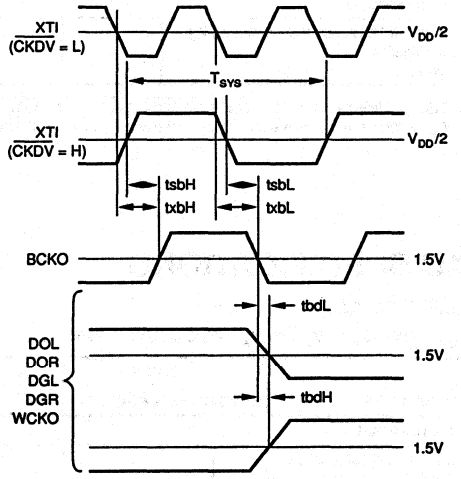
PARAMETER	SYMBOL	DF1700P/U MIN	TYP	MAX	UNITS
INPUT TIMING (BCKI, DIN, LRCI, XTI)					
BCKI, Pulse Width	t_{BCW}	100			ns
BCKI, Cycle Time	t_{BCY}	200			ns
DIN, Setup Time	t_{DS}	75			ns
DIN, Hold Time	t_{DH}	75			ns
Rising Edge of Last BCKI To Edge of LRCI	t_{BL}	75			ns
Edge of LRCI To Rising Edge of First BCKI	t_{LB}	75			ns
Falling Edge of XTI To Rising Edge of LRCI	t_{XL}	20			ns
Rising Edge of LRCI To Falling Edge of XTI	t_{LX}	0			ns

Timing Waveform



PARAMETER	SYMBOL	CONDITION	DF1700P/U MIN	TYP	MAX	UNITS
OUTPUT TIMING						
BCKO Delay Time from XTI	txbH	$\overline{CKDV}$ = L	35		120	ns
	txbL	$\overline{CKDV}$ = L	35		120	ns
	txbH	$\overline{CKDV}$ = H	35		120	ns
	txbL	$\overline{CKDV}$ = H	35		120	ns
Output Delay	tbdL	C_L = 15pF	–10	0	10	ns
	tbdH	C_L = 15pF	–10	0	10	ns

Timing Waveform



ORDERING INFORMATION

DF1700 ( )

Basic Model Number

Package Code
- P: 28-pin Plastic DIP
- U: 40-pin Plastic SOIC

ABSOLUTE MAXIMUM RATINGS

$+V_{DD}$	–0.3V to 7.0V
Input Voltage	–0.3 to V_{DD} +0.3V
Soldering Temperature	255°C
Soldering Time	10s
Storage Temperature	–40°C to +125°C

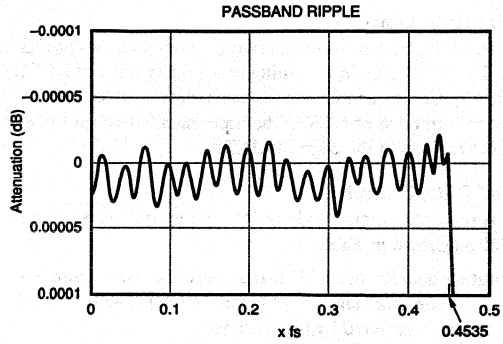
Stresses above these ratings may permanently damage the device.

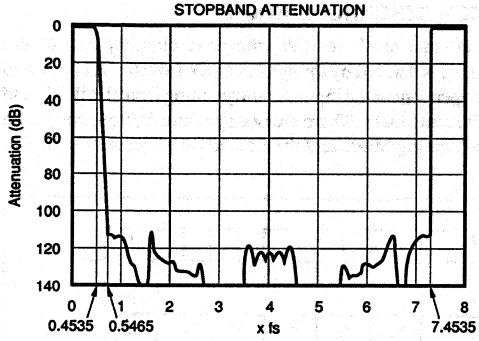
ELECTROSTATIC DISCHARGE SENSITIVITY

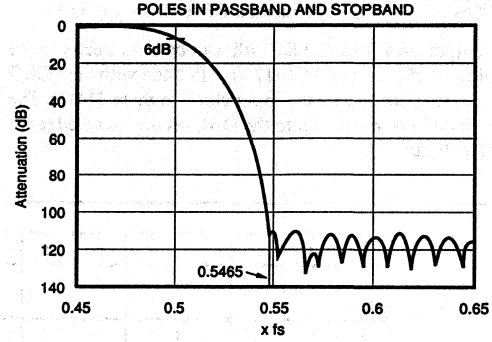
Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

THEORETICAL FILTER CHARACTERISTICS

PARAMETER	CHARACTERISTICS
Passband	0 ~ 0.4535fs
Stopband	0.5465fs ~ 7.4535fs
Passband Ripple	Within ±0.00005dB
Stopband Attenuation	More than 110dB
Group Delay Time	Constant







THEORY OF OPERATION

The DF1700 has dual filters. Each filter consists of three cascaded, 2x oversampling finite impulse response (FIR) filters as shown in Figure 1. The output of the first, 153-tap filter is again 2x oversampled by the second, 29-tap filter. This 4x oversampled data is again 2x oversampled by a third, 17-tap filter. This oversampling technique further separates the desired analog signal and the sampling frequency. This is desirable because a low-pass filter is required at the output of a DAC to remove all unwanted frequency components caused by the sampling frequency. With the analog signal frequency further separated from the sampling frequency, a lower order analog filter with much better phase characteristics can be used at the output of the DAC without worrying about fold-over noise.

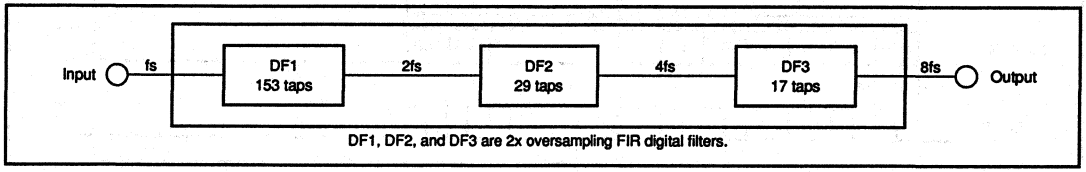


FIGURE 1. Block Diagram of Channel Filter.

FUNCTIONAL DESCRIPTION

SYSTEM CLOCK

The internal system clock of the DF1700 is generated by either a crystal oscillator connected across pins XTI and XTO driving the internal clock generator, or an external clock applied at pin XTI. Four different XTI clock frequencies can be obtained with the control of pins CKDV and CKSL. This will provide the correct clock period of the internal system clock as indicated in Table I. For XTI clock frequencies of 384fs and 512fs, the clock is divided by two for internal use. The system clock signal of the same frequency as pin XTI is available at pin CKO.

DATA

Serial Data Input

The 16-bit input data format is two's complement and MSB first. The serial data input timing is the rising edge of BCKI (Figure 2). Consequently the input serial data must be changed at the falling edge of BCKI. The input data is latched to the internal register at the edge of LRCI.

Serial Data Output

The serial data output mode is selected by pins $\overline{OW18}$ and $\overline{OW20}$ as shown in Table II.

The output data format is MSB first and either two's complement or complementary offset binary (COB). The format of output data is selected by the $\overline{COB}$ pin:

$\overline{COB}$ = H Two's complement
$\overline{COB}$ = L Complemented Offset Binary (COB)

The output data from the DF1700 can be fed directly to the data inputs of either the PCM1700 or PCM63 with the BCKO clock output serving as the input clock to these DACs. The data bits will be clocked into the DAC on the rising edges of BCKO (Figure 3).

CONDITION		XTI CLOCK (F_{XI})	CLOCK PERIOD OF INTERNAL SYSTEM CLOCK
$\overline{CKDV}$	$\overline{CKSL}$		
H	H	192fs	$1/F_{XI}$
H	L	256fs	$1/F_{XI}$
L	H	384fs	$2/F_{XI}$
L	L	512fs	$2/F_{XI}$

NOTE: fs = sampling frequency.

TABLE I. System Clock Frequency Selection.

$\overline{OW18}$	$\overline{OW20}$	NO. OF OUTPUT DATA BITS
H	H	16
L	H	18
H	L	20

TABLE II. Programming the Number of Output Data Bits.

CLOCK SYNCHRONIZATION

The internal clock for the arithmetic circuitry and output interface is derived by the system clock from the XTI pin, and is independent of the input circuitry timing from the BCKI and LRCI input clocks. There are two synchronization modes: the Free-Running Mode and the Forced Synchronization Mode.

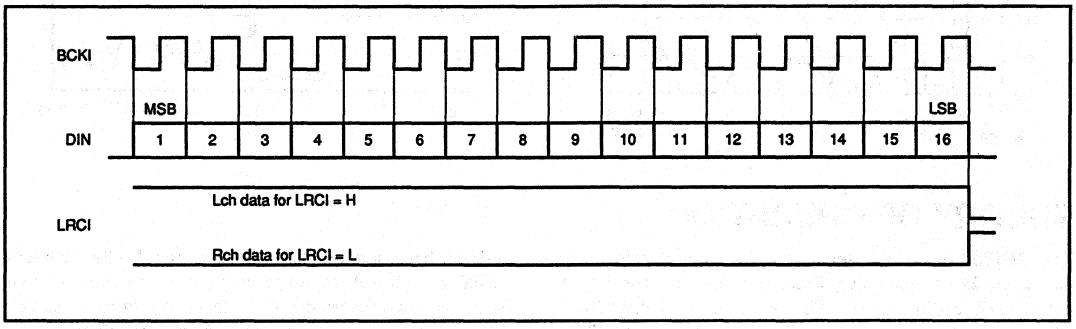


FIGURE 2. Input Timing Waveforms for Clocking Data into the DF1700.

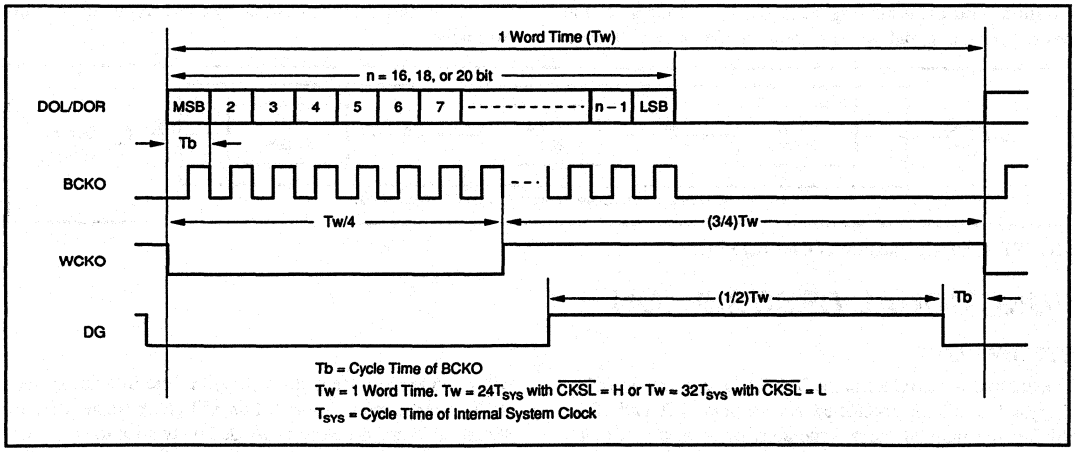


FIGURE 3. Output Data Timing Waveforms.

Free-Running Mode ($\overline{SYN}$ = H)

No adjustment of the internal clock takes place for phase differences between the internal clock and the LRCI clock of up to ±3/8 of the input data sample period (1/fs). Hence, internal timing is not affected even if jitter is present on the LRCI clock input, and no jitter or timing glitches appear on the data output. If the clock phase differences exceed the ±3/8fs limit, or if the RESET function is executed, the internal clock is synchronized to the rising edge of LRCI.

Forced Synchronization Mode ($\overline{SYN}$ = L)

In this mode the internal clock is resynchronized at each rising edge of LRCI. Note that device misoperation may occur if jitter in the LRCI input shortens the LRCI period below the required system clock period. Furthermore, if the LRCI period is too long, internal arithmetic operations will function correctly, but output timing is adversely affected.

The internal timing clock derived from the system clock is available at the FSCO pin.

SYSTEM RESET

The RESET function is useful for synchronizing the internal arithmetic circuitry and output section clock with the LRCI external input clock when operating in the free-running mode ($\overline{SYN}$ = H). It is not necessary to reset in the forced synchronization mode. Reset is also not required if the output timing needs not be synchronized with LRCI. Figure 4 shows the connection to reset the DF1700 on power-up.

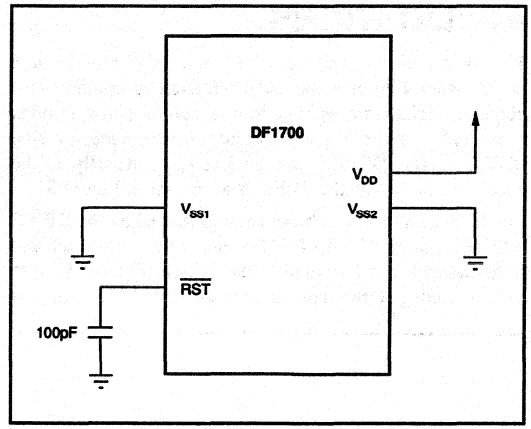
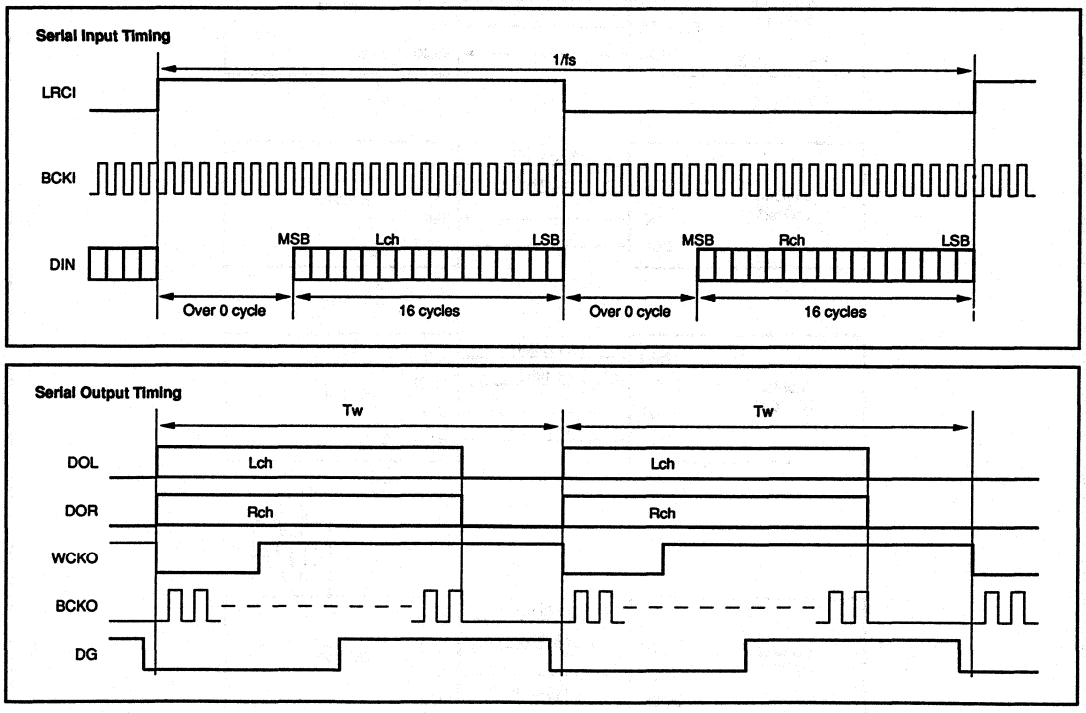


FIGURE 4. System Reset Circuit.

TIMING DIAGRAMS



APPLICATIONS

The most common application for the DF1700 is in high performance digital audio playback such as compact disc players. Digital information from a compact disc is often formatted using a digital interface format receiver chip (DIFRC). The DF1700 can be interfaced directly to the output of many popular DIFRCs as shown in Figure 5.

The fs data stream which has been formatted by the DIFRC is 8x oversampled by the DF1700 and separated into left and right channel data for input to the PCM1700 DAC (Figure 6). The analog stereo outputs from the PCM1700 each pass through a three pole Generalized Immittance Converter (GIC) low-pass filter which has extremely low distortion and negligible phase shift. An evaluation board, the DEM1143, is available from Burr-Brown for the PCM1700/DF1700. This board has the features mentioned above as well as an AES/EBU interface and breadboard area for user experimentation. Figure 7 shows a similar circuit diagram with the DF1700 providing 8x oversampled data to a pair of PCM63 DACs.

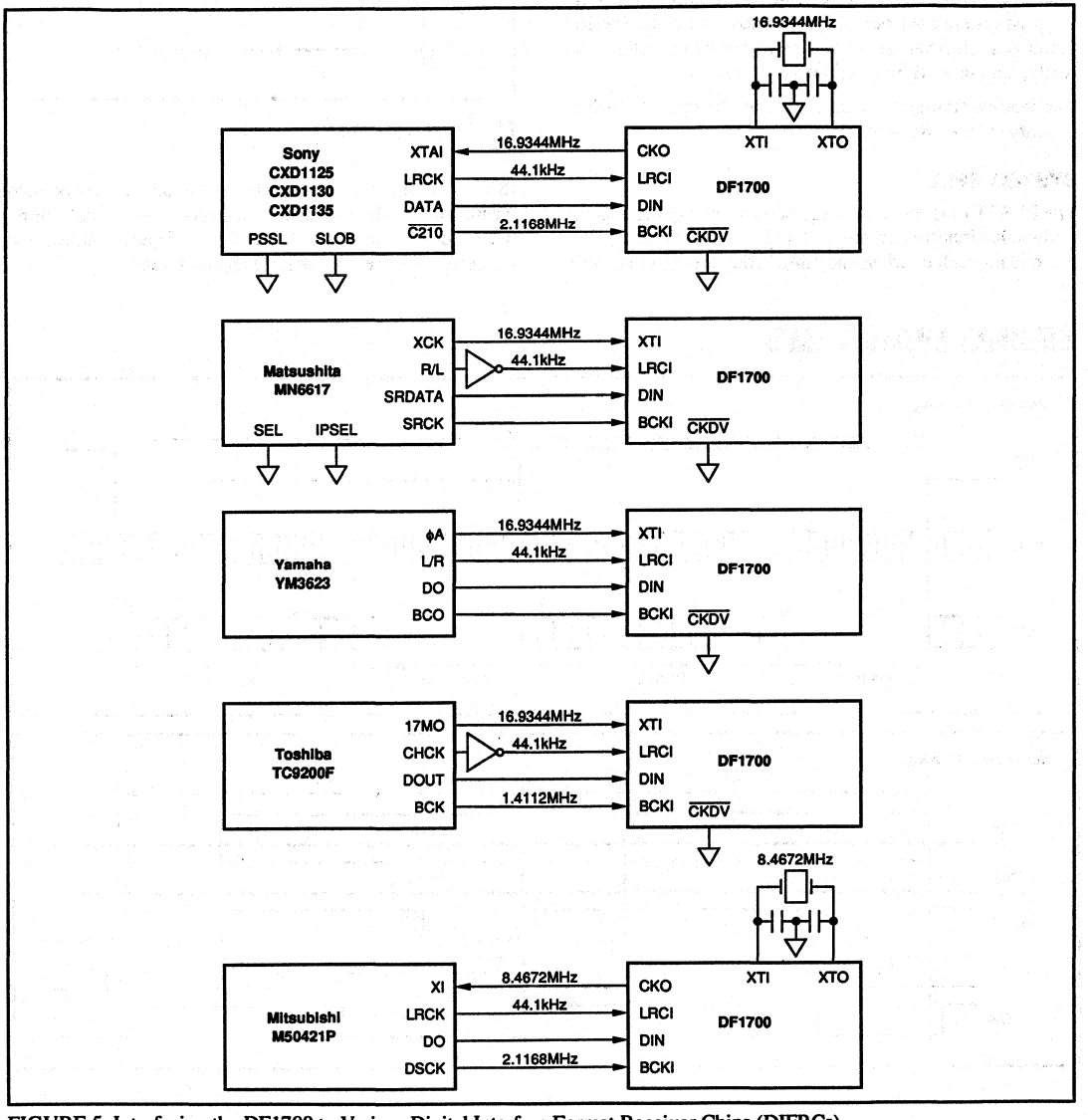


FIGURE 5. Interfacing the DF1700 to Various Digital Interface Format Receiver Chips (DIFRCs).

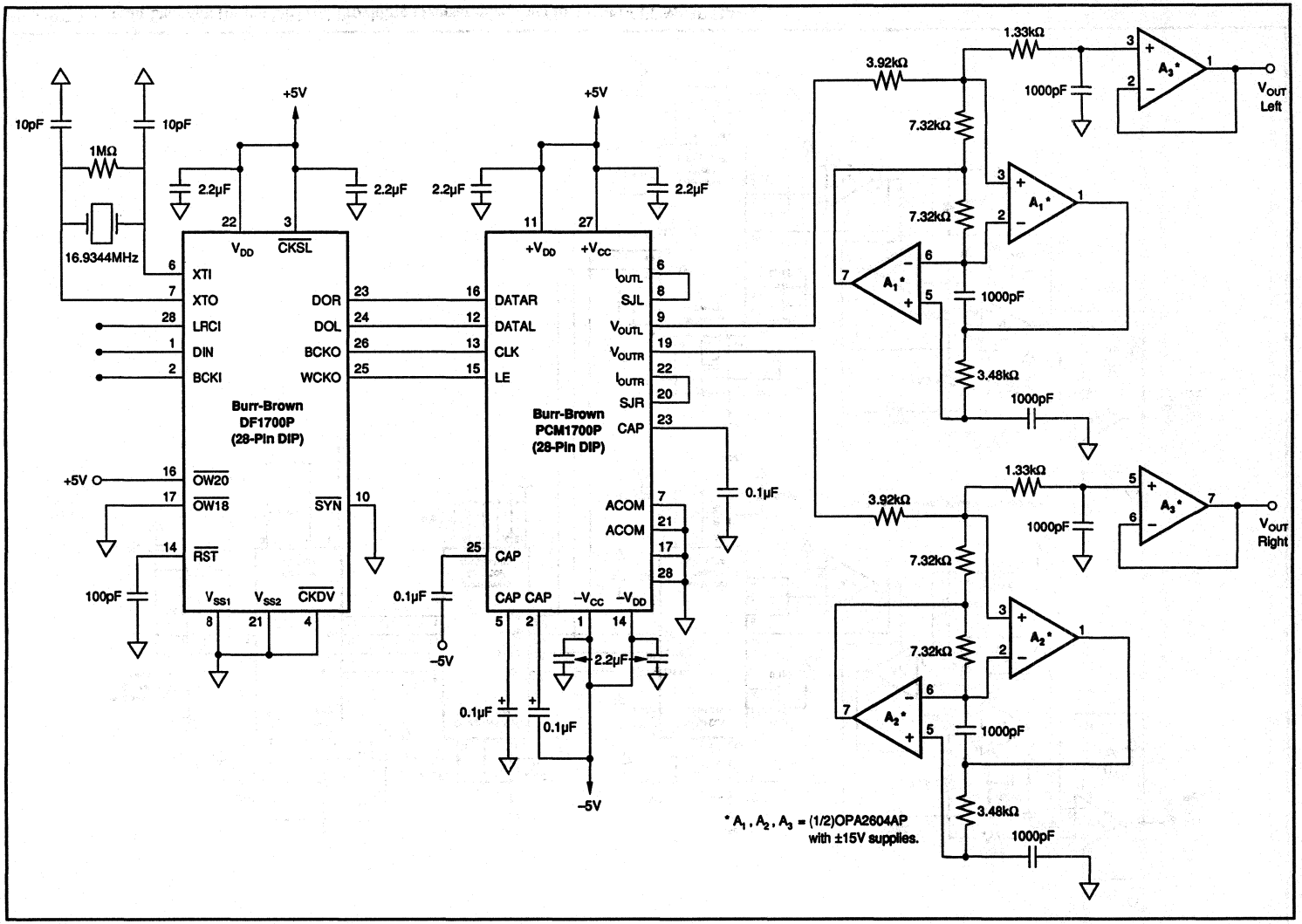


FIGURE 6. Circuit Diagram for the DF1700 Providing Oversampled Data to the PCM1700P Dual-Channel DAC.

Or, Call Customer Service at 1-800-548-6132 (USA Only)

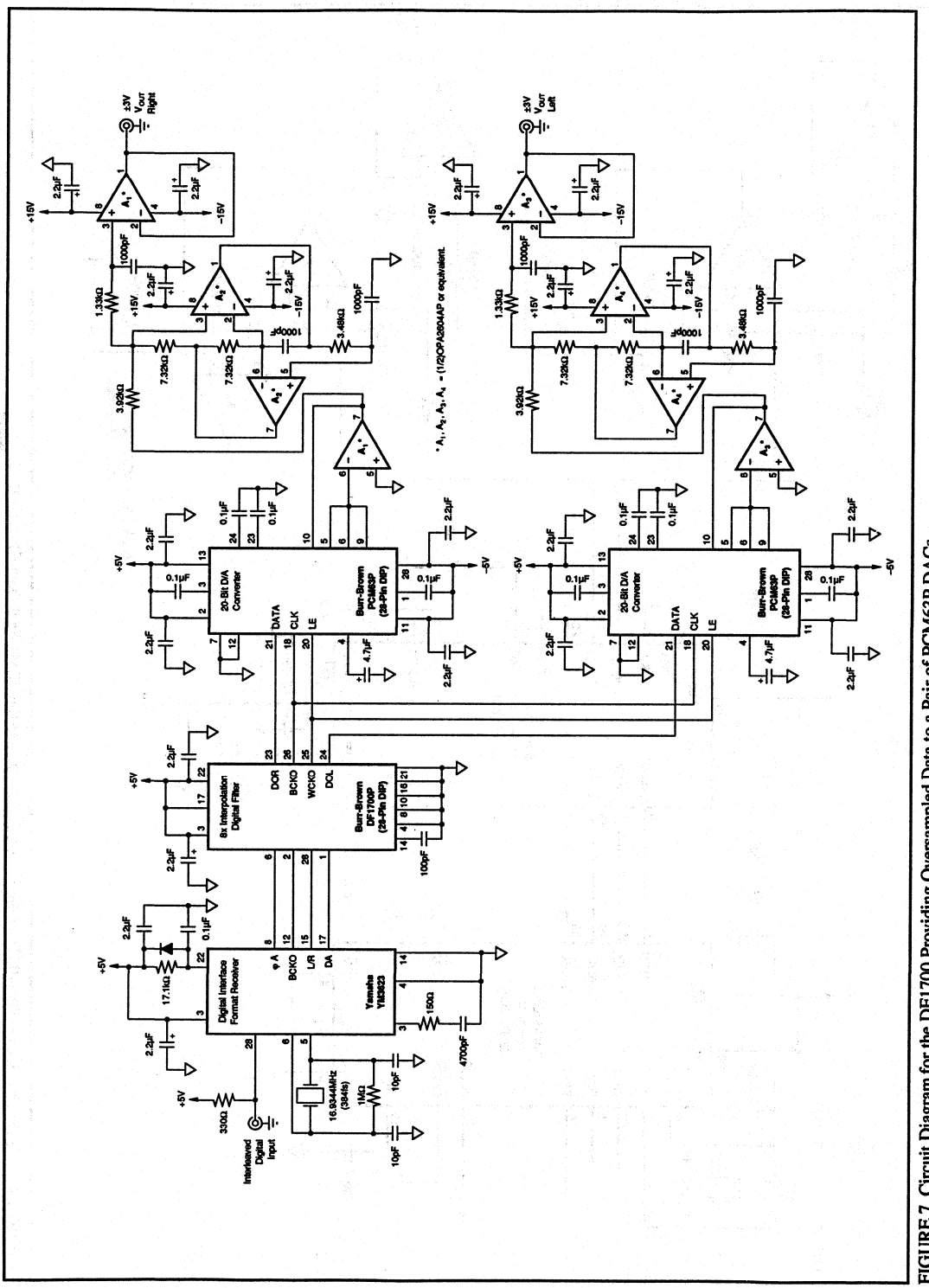


FIGURE 7. Circuit Diagram for the DF1700 Providing Oversampled Data to a Pair of PCM63P DACs.

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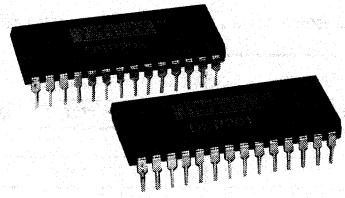


DSP201
DSP202

DSP-Compatible Single/Dual DIGITAL-TO-ANALOG CONVERTERS

FEATURES

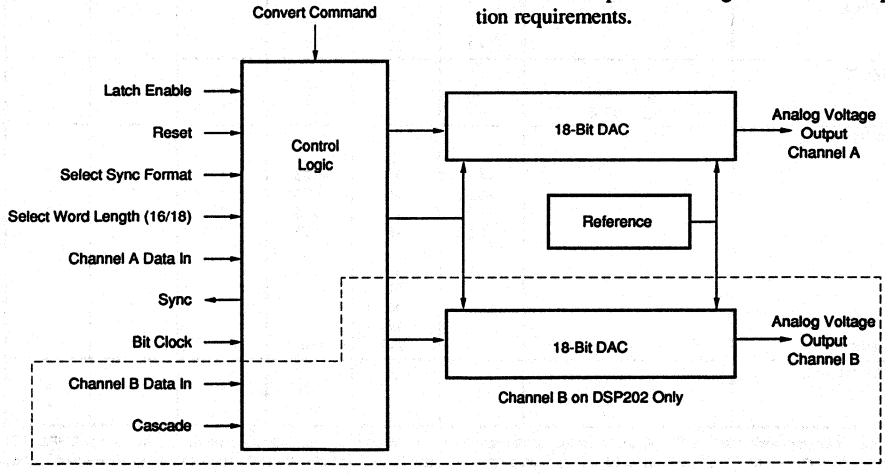
- ZERO-CHIP INTERFACE TO DSP ICs: AD, AT&T, MOTOROLA, TI
- SINGLE CHANNEL: DSP201
- DUAL CHANNEL: DSP202
  Two Serial Inputs or Cascade from Single 32-Bit Word
- UPDATE RATE TO 500kHz
- DYNAMIC SPECIFICATIONS:
  Signal/(Noise + Distortion) = 90dB;
  THD = –92dB
- USER SELECTABLE 16-BIT OR 18-BIT DATA WORDS

DESCRIPTION

The DSP201 and DSP202 are high performance digital-to-analog converters designed for simplicity of use with modern digital signal processing ICs. Both are complete with all interface logic for use directly with DSP ICs, and provide analog output voltages updated at up to 500kHz.

The DSP201 offers a single complete voltage output channel, accepting either 16 bits or 18 bits of input data, and can be driven by 16-bit, 24-bit, or 32-bit serial ports. The DSP202 offers two complete voltage output channels, with either two separate input ports, or a mode to drive both output channels from a single 32-bit word.

Both the DSP201 and DSP202 are packaged in standard, low-cost 28-pin plastic DIP packages. Each is offered in two performance grades to match application requirements.



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Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL

T_A = 0°C to 70°C, Output Update Frequency, f_S = 400kHz, $V_A+ = V_D+ = +5V$, $V_A- = V_D- = -5V$, unless otherwise specified.

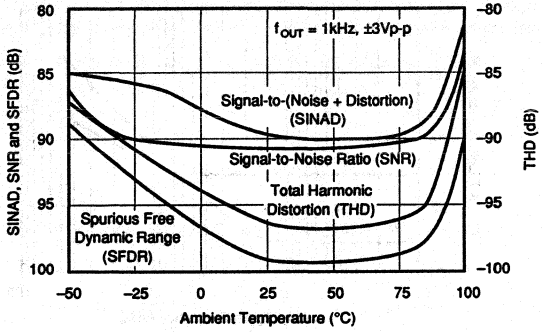
PARAMETER	CONDITIONS	DSP201JP DSP202JP			DSP201KP DSP202KP			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
RESOLUTION				18			•	Bits
DYNAMIC RANGE			108			•		dB
ANALOG OUTPUT								
Voltage Range	R_L = 375Ω		±3		•			V
Impedance			0.1			•		Ω
Current	R_L = 375Ω		±8			•		mA
Slew Rate	R_L = 1.5kΩ, C_L = 100pF		15			•		V/µs
Settling Time to 0.006% for Full-Scale Step	R_L = 1.5kΩ, C_L = 100pF		2.5			•		µs
THROUGHPUT SPEED (1)								
Update Rate	CASC = LOW on DSP202	500			•			kHz
DSP202 in Cascade Mode	CASC = HIGH	300						kHz
AC ACCURACY (2, 3)								
Signal to (Noise + Distortion) Ratio	f_{OUT} = 1kHz	82	86		88	90		dB(4)
	f_{OUT} = 1kHz (–60dB)		30			32		dB
	f_{OUT} = 10kHz	80	86		86	90		dB
Total Harmonic Distortion	f_{OUT} = 1kHz		–90	–85		–92	–88	dB
Channel Separation on DSP202	f_{OUT} = 1kHz to 100kHz		105			•		dB
DC ACCURACY								
Integral Nonlinearity Error			±0.006			±0.004		%
Differential Nonlinearity Error			±0.006			±0.004		%
Bipolar Zero Error (5)			±10			•		mV
Bipolar Zero Error Drift			20			•		ppm FSR/°C
Bipolar Zero Mismatch (5)	DSP202 Channels		5			•		mV
Gain Error			1	3		•	•	%
Gain Error Drift			100			•		ppm/°C
Gain Error Mismatch	DSP202 Channels		1	3		•	•	%
Digital Feedthrough	ENABLE = HIGH		–105			•		dB
Power Supply Sensitivity	$-5.1 < V_A-, V_D- < -4.9$		–60			•		dB
	$+4.9 < V_A+, V_D+ < +5.1$		–60			•		dB
DIGITAL INPUTS								
Format			Serial; MSB first; 16/18-bit and Cascaded					
Coding			Binary Twos Complement					
Logic Levels								
V_{IL}	I_L = ±10µA	0		+0.8	•		•	V
V_{IH}	I_{IH} = ±10µA	+2.4		+5	•		•	V
Data Transfer Clock								
Frequency				12	•		•	MHz
Duty Cycle		40	50	60	•	•	•	%
DIGITAL OUTPUTS								
V_{OL}	I_{OL} = 4mA	0		+0.4	•		•	V
V_{OH}	I_{OH} = 4mA	+2.4		+5	•		•	V
POWER SUPPLIES								
Rated Voltage								
V_A+		+4.75	+5	+5.25	•	•	•	V
V_A-		–5.25	–5	–4.75	•	•	•	V
V_D+		+4.75	+5	+5.25	•	•	•	V
V_D-		–5.25	–5	–4.75	•	•	•	V
Current								
I_A+			18			•		mA
I_A-			17			•		mA
I_D+			13			•		mA
I_D-			25			•		mA
Power Consumption			365	450		•	•	mW
TEMPERATURE RANGE								
Specification		0		+70	•		•	°C
Storage		–40		+125	•		•	°C

NOTES: (1) The data transfer clock must be at least 24 times the update rate for the standard mode, and 40 times the update rate in the DSP202 Cascade Mode. (2) All dynamic specifications are based on 2048-point FFTs. (3) Data for the 1kHz test is bandlimited to 0 to 20kHz. Data for the 10kHz test is bandlimited to 0 to 40kHz. (4) All specifications in dB are referred to a full-scale output, ±3Vp-p. (5) Adjustable to zero with external potentiometer.

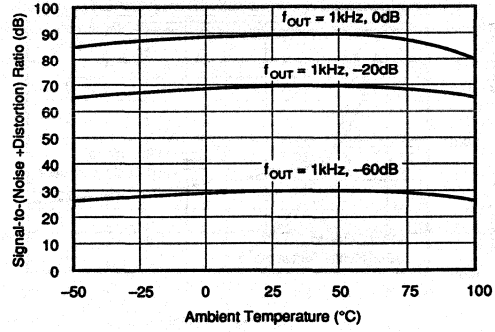
TYPICAL PERFORMANCE CURVES

T_A = +25°C; Update Frequency, f_S = 400kHz; $V_A+ = V_D+ = +5V$; $V_A- = V_D- = 5V$; SWL = HIGH; CASC = LOW; Output Bandwidth Limited to 20kHz; unless otherwise noted.

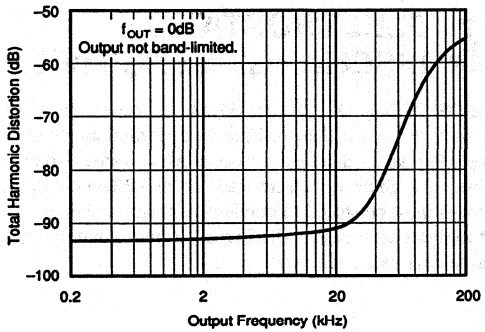
DYNAMIC PERFORMANCE vs TEMPERATURE



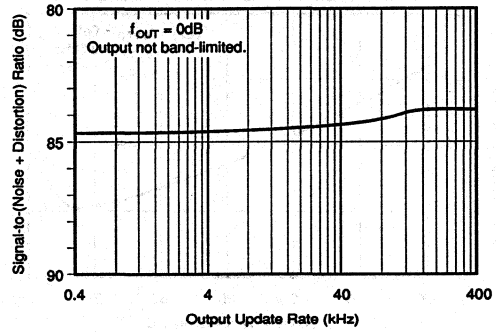
SIGNAL-TO-(NOISE + DISTORTION) RATIO vs TEMPERATURE AND AMPLITUDE



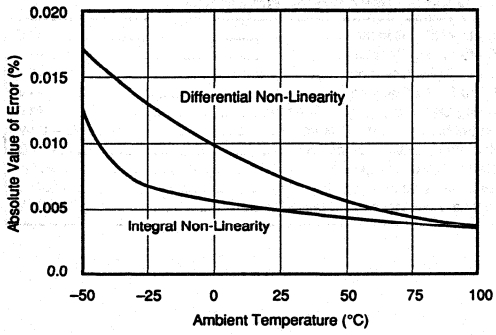
TOTAL HARMONIC DISTORTION vs OUTPUT FREQUENCY



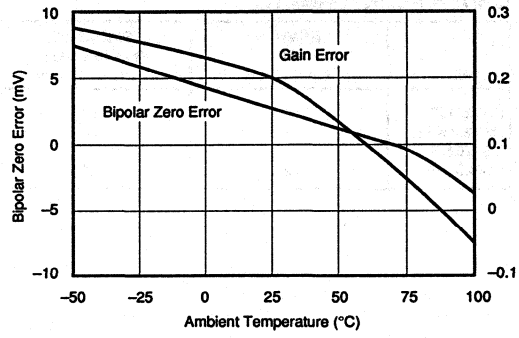
SIGNAL-TO-(NOISE + DISTORTION) vs OUTPUT UPDATE RATE



INTEGRAL AND DIFFERENTIAL LINEARITY ERROR vs TEMPERATURE (For Worst-Case Codes.)



BIPOLAR ZERO ERROR AND GAIN ERROR vs TEMPERATURE



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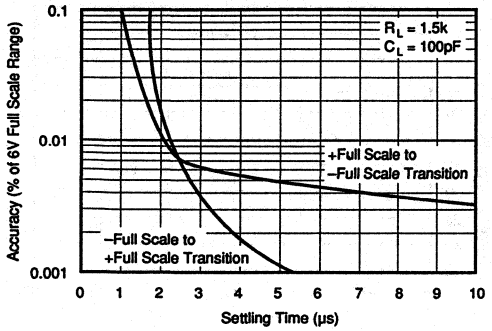
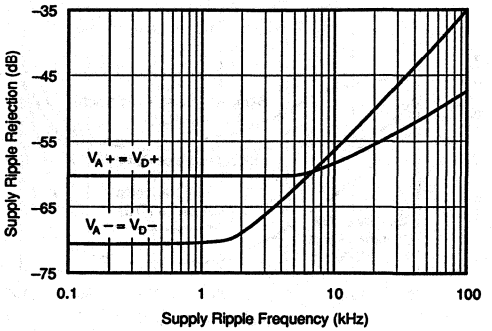
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C; Update Frequency, f_S = 400kHz; $V_A+ = V_D+ = +5V$; $V_A- = V_D- = 5V$; SWL = HIGH; CASC = LOW; Output Bandwidth Limited to 20kHz; unless otherwise noted.

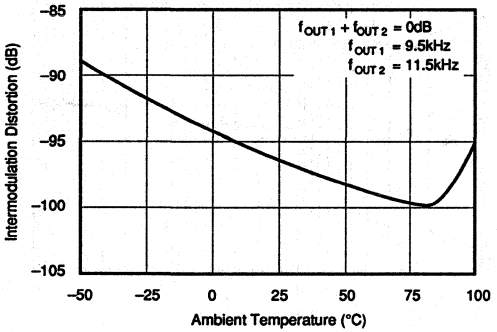
OUTPUT VOLTAGE SETTLING TIME



POWER SUPPLY REJECTION vs SUPPLY RIPPLE FREQUENCY



INTERMODULATION DISTORTION vs TEMPERATURE



ELECTROSTATIC DISCHARGE SENSITIVITY

The DSP201 and DSP202 are ESD (electrostatic discharge) sensitive devices, and normal standard precautions should be taken. Permanent damage may occur on unconnected devices subject to high energy electrostatic fields. When not in use, devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

ORDERING INFORMATION

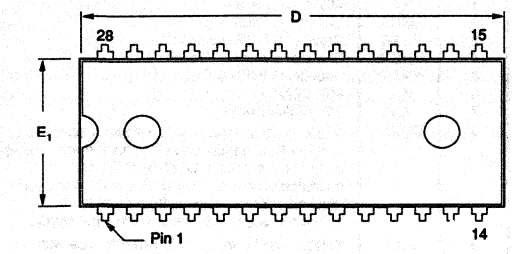
MODEL	NUMBER OF CHANNELS	SIGNAL-TO-(NOISE + DIST.) RATIO, dB min
DSP201JP	1	82
DSP201KP	1	88
DSP202JP	2	82
DSP202KP	2	88

ABSOLUTE MAXIMUM RATINGS

V_A+ to Analog Common	+7V
V_A- to Analog Common	–7V
V_D+ to Digital Common	+7V
V_D- to Digital Common	–7V
Analog Common to Digital Common	±1V
Control Inputs to Digital Common	–0.5 to V_D + 0.5V
Maximum Junction Temperature	150°C
Internal Power Dissipation	825mW
Lead Temperature (soldering, 10s)	+300°C
Thermal Resistance, θ_{JA}: Plastic DIP	50°C/W

MECHANICAL

P Package — 28-Pin Plastic DIP

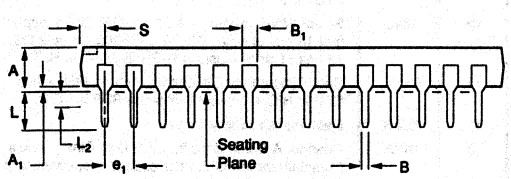


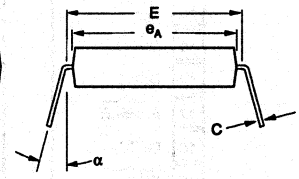
DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A (1)	.169	.200	4.29	5.08
A1 (1)	.015	.070	0.38	1.78
B	.015	.020	0.38	0.51
B1	.015	.055	0.38	1.40
C	.008	.012	0.20	0.30
D (1)	1.380	1.455	35.05	36.96
E	.600	.625	15.24	15.88
E1 (1)	.485	.550	12.32	13.97
e1	.100 BASIC		2.54 BASIC	
eA	.600 BASIC		15.24 BASIC	

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
L	.100	.200	2.54	5.08
L2	.000	.030	0.00	0.76
α	0°	15°	0°	15°
Q1	.020	.070	0.51	1.78
S1	.040	.080	1.02	2.03

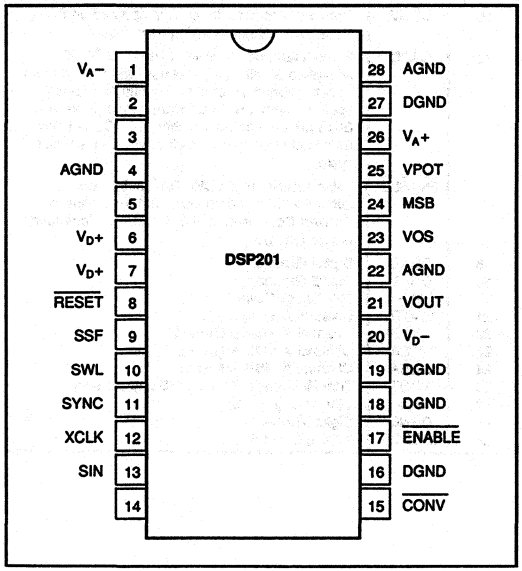
(1) Not JEDEC Standard.

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.





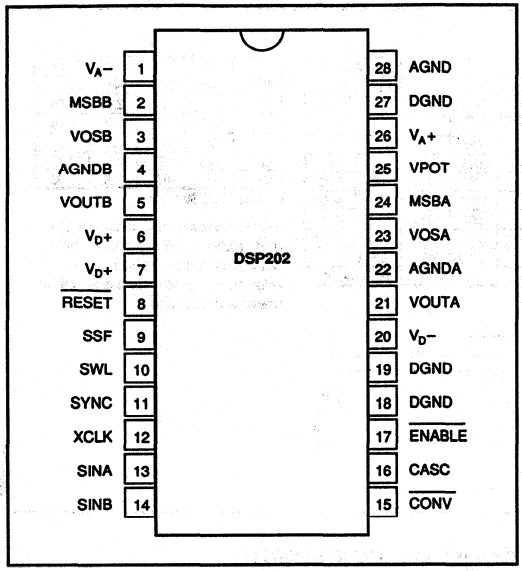
DSP201 PIN CONFIGURATION



DSP201 PIN ASSIGNMENTS

PIN #	NAME	DESCRIPTION
1	V_A-	–5V Analog Power.
2		No Internal Connection.
3		No Internal Connection.
4	AGND	Analog Ground.
5		No Internal Connection.
6	V_D+	+5V Digital Power.
7	V_D+	+5V Digital Power.
8	$\overline{RESET}$	Reset. If LOW, DAC output will be 0V after two convert commands, and will remain there as long as the Reset input is LOW. If HIGH, normal operation proceeds. Two convert commands are required after Reset goes from LOW to HIGH before the output will relate to the input word.
9	SSF	Select Sync Format In. Tie HIGH for use with Motorola and TI DSP ICs. Tie LOW for use with AT&T DSP ICs.
10	SWL	Select Word Length In. If HIGH, DSP201 accepts first 16 bits of data. If LOW, DSP201 accepts first 18 bits of data.
11	SYNC	Data Synchronization Output. Active HIGH when SSF is HIGH, active LOW when SSF is LOW.
12	XCLK	Data Transfer Clock Input.
13	SIN	Serial Data In. MSB first, Binary Two's Complement format.
14		No Internal Connection.
15	CONV	Convert Command In. DAC is updated on falling edge, and initiates clocking new data in.
16	DGND	Digital Ground.
17	$\overline{ENABLE}$	Latch Enable In. If LOW, DAC output will be latched with new data word on falling edge of Convert Command. If HIGH, Convert Commands will be ignored.
18	DGND	Digital Ground.
19	DGND	Digital Ground.
20	V_D-	–5V Digital Power.
21	VOUT	Voltage Out.
22	AGND	Analog Ground.
23	VOS	VOS Adjust In.
24	MSB	MSB Adjust In.
25	VPOT	Trim Reference Out for MSB adjustment.
26	V_A+	+5V Analog Power.
27	DGND	Digital Ground.
28	AGND	Analog Ground.

DSP202 PIN CONFIGURATION



DSP202 PIN ASSIGNMENTS

PIN #	NAME	DESCRIPTION
1	V_A-	–5V Analog Power.
2	MSBB	Channel B MSB Adjust In.
3	VOSB	Channel B VOS Adjust In.
4	AGNDB	Channel B Analog Ground.
5	VOUTB	Channel B Voltage Out.
6	V_D+	+5V Digital Power.
7	V_D+	+5V Digital Power.
8	$\overline{\text{RESET}}$	Reset. If LOW, DAC output will be 0V after two Convert Commands, and will remain there as long as the Reset input is LOW. If HIGH, normal operation proceeds. Two Convert Commands are required after Reset goes from LOW to HIGH before the output will relate to the input word.
9	SSF	Select Sync Format In. Tie HIGH for use with Motorola and TI DSP ICs. Tie LOW for use with AT&T DSP ICs.
10	SWL	Select Word Length In. If HIGH, DSP202 accepts first 16 bits of data. If LOW, DSP202 accepts first 18 bits of data. Must be HIGH if CASC is HIGH.
11	SYNC	Data Synchronization Output. Active HIGH when SSF is HIGH, active LOW when SSF is LOW.
12	XCLK	Data Transfer Clock Input.
13	SINA	Channel A Serial Data In. MSB first, Binary Two's Complement format. In Cascade Mode, connect to SINB and to DSP IC output.
14	SINB	Channel B Serial Data In. MSB first, Binary Two's Complement format. In Cascade Mode, connect to SINA and to DSP IC output.
15	CONV	Convert Command In. DAC is updated on falling edge, and initiates clocking new data in.
16	CASC	Select Cascade Mode In. If HIGH, DSP202 accepts a 32-bit word, and uses the first 16 bits to update channel A, and the second 16 bits to update channel B. In Cascade Mode, SINA and SINB are connected together. If CASC is LOW, data is strobed into both channels on each clock cycle.
17	$\overline{\text{ENABLE}}$	Latch Enable In. If LOW, DAC output will be latched with new data word on falling edge of Convert Command. If HIGH, Convert Commands will be ignored.
18	DGND	Digital Ground.
19	DGND	Digital Ground.
20	V_D-	–5V Digital Power.
21	VOUTA	Channel A Voltage Out.
22	AGNDA	Channel A Analog Ground.
23	VOSA	Channel A VOS Adjust In.
24	MSBA	Channel A MSB Adjust In.
25	VPOT	Trim Reference Out for MSB adjustments.
26	V_A+	+5V Analog Power.
27	DGND	Digital Ground.
28	AGND	Analog Ground.

THEORY OF OPERATION

The DSP201 and DSP202 are basic voltage output digital-to-analog converters with complete logic interface circuitry for ease of use with standard digital signal processing ICs. Data words are transmitted from the DSP IC on its serial port, leaving the DSP IC parallel ports free for digital communication.

The DSP201 and DSP202 are pipelined internally. When the user gives a convert command at time t, two actions are initiated. First, the data stored in the internal shift registers following the previous convert command (at t – 1) is used to update the output D/A converters immediately. Second, the DSP201 or DSP202 transmits a synchronization pulse to the DSP IC and starts clocking new data into the shift register using the system Bit Clock. This data is then used to update the D/As when the t + 1 convert command is received.

Both the DSP201 and DSP202 are 18-bit D/As internally. On-chip logic can be programmed to use 18-bits of data to update the D/A outputs, or can be programmed to update the D/A based on 16-bit data words. Additionally, the logic in the DSP202 can accept a 32-bit data word (the Cascade Mode), and update both D/A channels simultaneously with 16 bits each. All of these modes can be hard-wired or logic-controlled externally, so that no extra overhead on the part of the DSP IC is required.

In the 16-bit modes, the DSP201 and DSP202 will append zeros to the 16-bits transferred to each of the internal D/As, which are full 18-bit converters. The 18-bit word-length mode can be used with DSP ICs programmed for either 24-bit or 32-bit output words, in which case the DSP201 or DSP202 will clock in the first 18-bits of data after the synchronization pulse, and ignore additional information on the serial line. When programmed to accept 16-bit words, the DSP201 and DSP202 can be used with DSP ICs programmed to output 16-, 24-, or 32-bit words, and will ignore additional information after the first 16 bits on the serial line.

The DSP201 and DSP202 are complete voltage output D/A converters, with on-chip references and output amplifiers to drive ±3V into 375Ω loads. State-of-the-art bipolar technologies are used in the D/A section to maximize the output update rate, to maximize dynamic performance, and to eliminate glitch problems. Advanced plastic packaging methods makes this performance attainable economically.

BASIC OPERATION

DATA FORMAT AND OUTPUT LEVELS

The DSP201 and DSP202 accept serial data, MSB first, in standard Binary Two's Complement format. The length of the data words can be selected as shown below, and the D/A output level generated by a specific input code is shown in Table I.

As with all standard D/As, the output ranges from negative full scale (–3V) to 1 LSB below positive full scale (+3V – 1LSB). The bipolar output amplifiers are designed to drive 375Ω loads at full speed and accuracy.

UPDATING THE OUTPUT

With $\overline{\text{ENABLE}}$ (pin 17) LOW, the falling edge of a Convert Command arriving on CONV (pin 15) will immediately update the D/A outputs with the data stored in the internal shift registers following the previous Convert Command. The Convert Command can be asynchronous to any other signals or clocks without reducing accuracy, although system accuracy is often enhanced by synchronizing digital signals.

For a full-scale change in the input code, the output will typically settle to within ±0.006% of its final level within 2.5µs. The slew rate of the output amplifier is typically 15V/µs, for a full power bandwidth close to 800kHz. All of the specifications and typical performance curves are achieved with a full 400kHz update rate, unless otherwise specified. The DSP201 and DSP202 are guaranteed operational to a full 500kHz update rate, which exceeds the maximum Bit Clock rate for most standard DSP ICs.

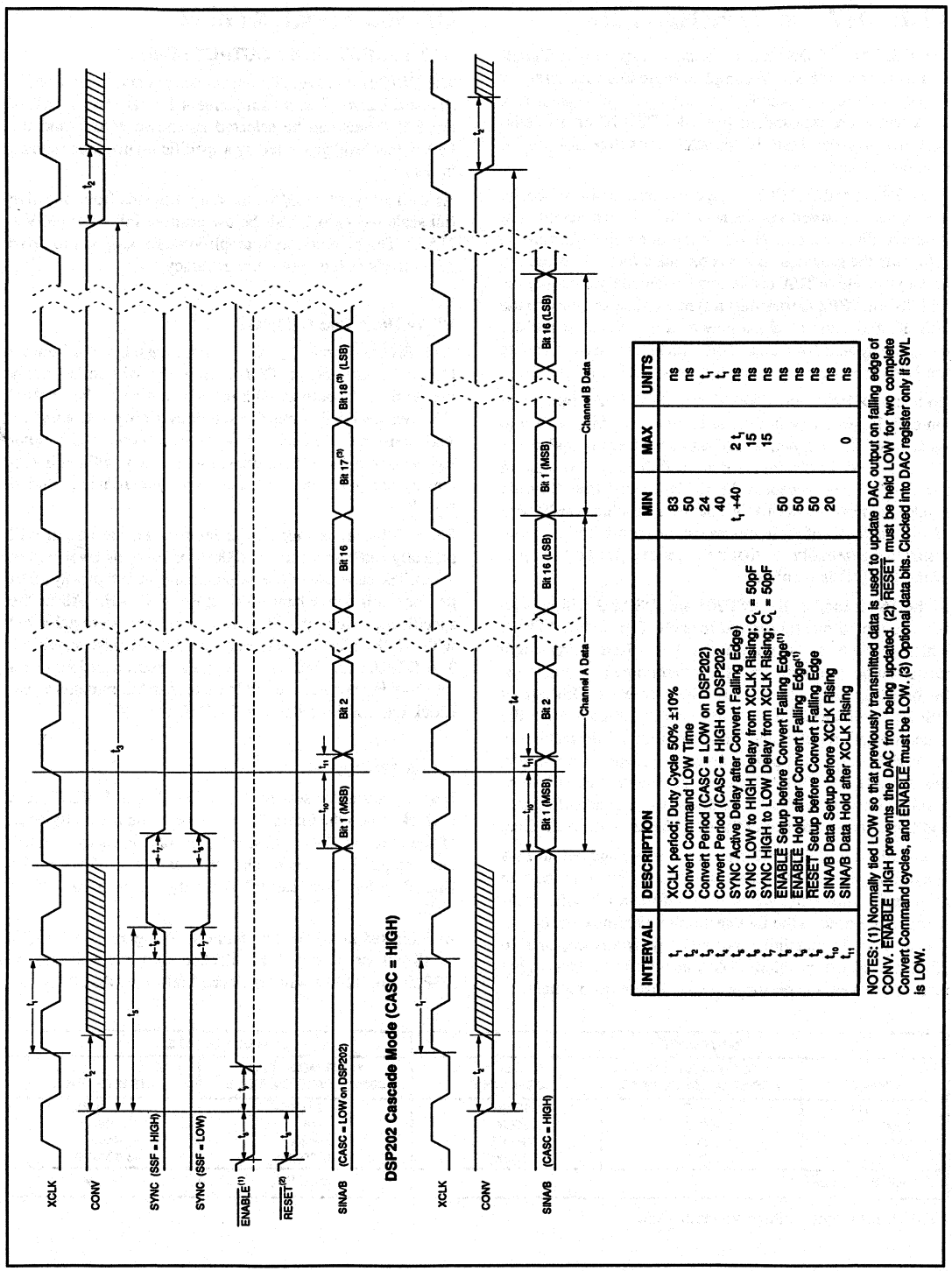
DATA TRANSFER

Data is transmitted serially to the DSP201 or DSP202, and is clocked into the internal shift registers on the rising edge of the external Data Transfer Clock or Bit Clock (XCLK input on pin 12.) This clock can be as fast as 12MHz. The Data Transfer Clock can tolerate duty cycles from 40% to 60%.

As indicated in the timing diagrams in Figure 1, either 16- or 18-bits of data will be clocked into the DSP201 or DSP202, or 32-bits will be clocked into the DSP202 in the

INPUT CODE			OUTPUT VOLTAGE	
BINARY	16-BIT MODE AND DSP202 CASCADE MODE	HEX 18-BIT MODE	16-BIT MODE AND DSP202 CASCADE MODE	18-BIT MODE
0111...1111	7FFF	1FFFF	+2.999908V	2.999977V
0000...0000	0000	00000	0V	0V
1111...1111	FFFF	3FFFF	–92µV	–23µV
1000...0000	8000	20000	–3.000000V	–3.000000V
Theoretical LSB Size			91.6µV	22.9µV

TABLE I. Output Voltage vs Input Code.



INTERVAL	DESCRIPTION	MIN	MAX	UNITS
t_1	XCLK period; Duty Cycle 50% ±10%	83		ns
t_2	Convert Command LOW Time	50		ns
t_3	Convert Period (CASC = LOW on DSP202)	24		t_1
t_4	Convert Period (CASC = HIGH on DSP202	40		t_1
t_5	SYNC Active Delay after Convert Falling Edge)	t_1 +40	2 t_1	ns
t_6	SYNC LOW to HIGH Delay from XCLK Rising; C_L = 50pF		15	ns
t_7	SYNC HIGH to LOW Delay from XCLK Rising; C_L = 50pF		15	ns
t_8	ENABLE Setup before Convert Falling Edge(1)	50		ns
t_9	ENABLE Hold after Convert Falling Edge(1)	50		ns
t_{10}	RESET Setup before Convert Falling Edge	50		ns
t_{11}	SINA/B Data Setup before XCLK Rising	20		ns
	SINA/B Data Hold after XCLK Rising		0	ns

NOTES: (1) Normally tied LOW so that previously transmitted data is used to update DAC output on falling edge of CONV. ENABLE HIGH prevents the DAC from being updated. (2) RESET must be held LOW for two complete Convert Command cycles, and ENABLE must be LOW. (3) Optional data bits. Clocked into DAC register only if SWL is LOW.

FIGURE 1. DSP201 and DSP202 Timing.

Cascade Mode, but internal digital overhead requires additional Data Transfer Clock cycles before a new Convert Command can be sent. The minimum time between Convert Commands is 24 times the Data Transfer Clock period for either the DSP201 or the DSP202 in standard modes, and 40 times the Data Transfer clock period for the DSP202 in the Cascade Mode. There is no maximum time between Convert Commands.

These additional clock cycles are used to set up the internal shift registers and logic, and are included in the specifications for maximum update rate. This means a 12MHz Bit Clock can achieve the maximum specified update rate of 500kHz.

DATA SYNCHRONIZATION

The DSP201 and DSP202 have internal logic to generate a synchronization pulse (SYNC on pin 11) to signal the host processor to transmit data. The synchronization pulse is sent when a Convert Command is received, and the SYNC output changes on the rising edge of XCLK. Timing is shown in Figure 1.

The synchronization pulse can be programmed to be either active High or active Low, depending on the logic level input on SSF (Select Sync Format on pin 9.) If SSF is LOW, SYNC will be normally HIGH, and will transmit a LOW pulse after a Convert Command is received. If SSF is HIGH, SYNC will be normally LOW, and will transmit a HIGH pulse after a Convert Command is received. The SYNC pulse will be as wide as one clock cycle on the Data Transfer Clock input on XCLK (pin 12.)

SELECTING WORD LENGTH

If the Select Word Length input (SWL, pin 10) is HIGH, the DSP201 or DSP202 will accept 16 bits of data after a Convert Command, with the timing shown in Figure 1. After these 16 bits, additional data on SIN (DSP201 pin 13) or SINA and SINB (DSP202 pins 13 and 14) will be ignored. Transparent to the user, the internal shift register will append two zeroes to the 16-bit data words before updating the D/As on the next Convert Command.

If SWL is LOW, the DSP201 or DSP202 will clock 18 bits of data into the internal shift register after a Convert Command, with the timing shown in Figure 1. Subsequent data on SIN (DSP201 pin 13) or SINA and SINB (DSP202 pins 13 and 14) will be ignored.

In the 16-bit mode, an increment of 1 LSB will change the D/A output by approximately 91.6μV (the 6V full scale range divided by 2^{16}), while an LSB in the 18-bit mode will change the output approximately 22.9μV ($6V/2^{18}$).

The DSP201 and DSP202 analog performance is tested in production using the 16-bit mode (with SWL HIGH), and the typical performance curves were generated using the 16-bit mode. Verification is made during final test that the 18-bit mode functions, but the extra resolution of these last two bits is not used when testing the analog performance.

DSP202 CASCADE MODE

If CASC on the DSP202 (pin 16) is HIGH, the Cascade Mode is implemented. In this mode, SINA (pin 13) and SINB (pin 14) are strapped together and connected to the serial output port of an appropriate DSP IC or other data word source. A Convert Command initiates the transfer of a 32-bit word to the DSP202.

In the Cascade Mode, care must be taken to make sure SWL (pin 10) is HIGH.

LATCH ENABLE

If $\overline{\text{ENABLE}}$ (pin 17) is LOW, the D/A outputs will be latched with new data on the falling edge of the Convert Command. Taking $\overline{\text{ENABLE}}$ HIGH causes the DSP201 or DSP202 to ignore Convert Commands. With $\overline{\text{ENABLE}}$ HIGH when a Convert Command arrives at time t, data latched in the internal shift register after the Convert Command at t – 1 is not latched to the D/As, but a new synchronization pulse is still generated and the data in the shift register is overwritten. This feature allows multiple DSP201s or DSP202s to share a single DSP IC and still be independently updated.

RESET

Taking $\overline{\text{RESET}}$ (pin 8) LOW will cause the D/As to output 0V after two Convert Commands are received. The two Convert Commands clear out the internal shift registers, and data input on the serial input lines will be ignored while $\overline{\text{RESET}}$ is low. This facilitates designing an analog output system that goes into a known, benign state either at power-up, after fault conditions or during a calibration cycle. $\overline{\text{ENABLE}}$ (pin 17) must be LOW when resetting the DSP201 or DSP202 outputs to 0V.

After $\overline{\text{RESET}}$ is taken HIGH, two Convert Commands are required before the output will relate to the input data. Also, $\overline{\text{ENABLE}}$ must be LOW for the data to be latched to the D/As. The first Convert Command again latches the outputs at 0V, and the second Convert Command drives the output to the level determined by the data clocked in after the first Convert Command.

A $\overline{\text{RESET}}$ command after power up is not required for proper operation of the DSP201 or DSP202.

LAYOUT CONSIDERATIONS

Because of the high resolution, linearity and speed of the DSP201 and DSP202, system design problems such as ground path resistance, contact resistance and power supply quality become very important.

GROUNDS

To achieve the maximum performance from the DSP201 or DSP202, care should be taken to minimize the effect of current flows in the system grounds that may corrupt the output voltages generated by the D/As. Pin 22 on the DSP201 and pins 4 and 22 on the DSP202 are the most

critical internal grounds, and care should be taken especially at these points to make them as close as possible to the same potential as the system analog ground. The design of the DSP201 and DSP202 insures that these pins will have minimal current flowing through them.

Internally, power currents are directed to the digital grounds (pins 18, 19, and 27) for internal digital currents, which are primarily switching currents, and to the analog grounds (pin 28, plus pin 4 on the DSP201) for analog currents, which are primarily from the internal current switches and the output amplifier. Pin 16 on the DSP201 is used internally as a logic level, and injects essentially no current into the ground.

Wherever possible, it is strongly recommended that separate analog and digital ground planes be used. With an LSB level of 92µV in 16-bit modes, and one quarter of that in 18-bit modes, the currents switched in a typical DSP system (processor, memory, etc.) can easily corrupt the output accuracy of the D/A's unless great care is taken to analyze and design for current flows.

POWER SUPPLY DECOUPLING

All of the supplies should be decoupled to the appropriate grounds using tantalum capacitors in parallel with ceramic capacitors, as shown in Figures 2 and 3. For optimum performance of any high resolution D/A, all of the supplies need to be as clean as possible. If separate digital and analog supplies are available in a system, care should be taken to insure that the difference between the analog and the digital supplies is not more than 0.5V for more than a few hundred milliseconds, as may occur at power-on.

Separate –5V analog and digital supplies are not needed. These pins are kept separate internally to minimize coupling. Drive pin 20 from the –5V analog supply, and make sure that the decoupling shown in Figure 2 or 3 are placed as close as possible to the D/As.

CALIBRATION AND ADJUSTMENT OPTIONAL EXTERNAL OFFSET AND MSB TRIMS

All of the specifications for the DSP201 and DSP202, plus the typical performance curves, are based on the performance of these D/As without external trims. In most applications, external trims are not required.

If external trims are not used, pins 23, 24, and 25 on the DSP201 should be left open, as should pins 2, 3, 23, 24 and 25 on the DSP202. These pins should not be decoupled with capacitors or tied to any specific potential, or the noise on the D/A outputs may increase.

ADJUSTING OFFSET

Where required by specific applications, offsets can be trimmed using the circuits in Figure 2 (DSP201) or Figure 3 (DSP202.) As with all standard D/As, offset on the DSP201 and DSP202 means the difference of the output from the ideal negative full scale value. The DSP201 and DSP202 use a current switching D/A architecture, and the current from this is internally amplified to produce a ±3V output range. Negative full scale output thus results from having all of the internal current switches turned off. Offset on the DSP201 and DSP202 should not be confused with the delta from 0V with an input code of 0000...0000 (0000 hex for 16-bit Modes, 00000 hex for 18-bit Modes). This is often described as bipolar zero error, and includes the effects of both offset and gain error.

To trim the offsets, first latch the D/As with 1000...0000 (8000 hex or 20000 hex). Then adjust the offset adjustment pots to produce an output of –3.000000V.

ADJUSTING THE MSB WEIGHT

The MSB adjustment circuitry shown in Figure 2 for the DSP201 and in Figure 4 for the DSP202 basically change the weight of the MSB by adding to or subtracting from the current controlled by the internal MSB switch.

Depending on the application, the MSB adjustments can be made in one of three different ways to optimize the system performance using the DSP201 or DSP202. For dynamic performance, the MSB can be adjusted to minimize distortion of either a full-scale or low level sine-wave output. For applications stressing differential linearity, the 0000...0000 (0000 hex or 00000 hex) to 1000...0000 (FFFF hex or 3FFFF hex) transition can be trimmed to change the output of the D/As precisely 1 LSB (92µV in the 16-bit Mode or 23µV in the 18-bit Mode.)

To adjust for minimum distortion of full-scale sinewaves, strobe the inputs to the DSP201 or DSP202 with codes representing ideal full scale sine waves, then trim the MSB adjustment circuit to minimize distortion, as measured by either a distortion analyzer or by digitizing the output with an appropriate A/D and running FFT analyses.

In many audio applications, it is more appropriate to adjust for minimum distortion with low level sinewave outputs. This minimizes zero-crossover error, which can be a concern in high-end audio systems. To do this, strobe the inputs to the DSP201 or DSP202 with codes representing ideal low-level sine waves (–60dB from full scale works well), and then trim the MSB adjustment circuit to minimize distortion, again using a distortion analyzer or FFT analyses to check the results of the trims.

The MSB adjustment circuits can also be used to trim the D/A outputs directly for the transition from 0000...0000 (0000 hex or 00000 hex) to 1111...1111 (FFFF hex or 3FFFF hex), eliminating differential linearity error at the major carry. Ideally, this transition of the digital input code should cause the D/A outputs to change 92µV in the 16-bit Mode or 23µV in the 18-bit Mode. A simple way to make this adjustment is to continually load alternately the codes 1111...1111 (FFFF hex or 3FFFF hex) and 0000...0000 (0000 hex or 00000 hex) into the DSP201 or DSP202. An amplifier with sufficient gain can then drive an oscilloscope input, and the transition output step can be adjusted.

An alternative for calibrating on a bench is to tie SIN (DSP201 pin 13) or SINA and SINB (DSP202 pins 13 and 14) HIGH, and provide a Bit Clock and periodic Convert Commands. This loads 1111...1111 ($FFFF_{HEX}$ or $3FFFF_{HEX}$), driving the output to 1LSB below 0V. Then periodically bring RESET (pin 8) LOW for at least two Convert Commands, which is the equivalent of loading all 0s, so the output is 0V. Now the output can be adjusted for an ideal transition step.

ADJUSTING BIPOLAR ZERO ERROR

If it is important in a specific application to adjust bipolar zero error, the user should first adjust the MSB trim circuits, and then use the offset adjust circuits to adjust the outputs to 0V with input codes of all 0s (0000...0000; 0000 hex or 00000 hex.) In this case, it is not possible to also trim offset at –Full Scale, as described above.

GAIN ERROR

Gain error on the DSP201 or DSP202 cannot be directly adjusted. If required in a specific application, gain can be trimmed out at the system level by adjusting the gain used in an output amplifier stage, such as would be used in any active output filter. In this case, the bipolar zero error should be adjusted first as discussed above. Then, the gain on the output amplifier should be adjusted to minimize the deviation from ideal for –Full Scale (1000...000; 8000 hex or 20000 hex) and +Full Scale (0111...1111; 7FFF hex or 1FFFF hex.)

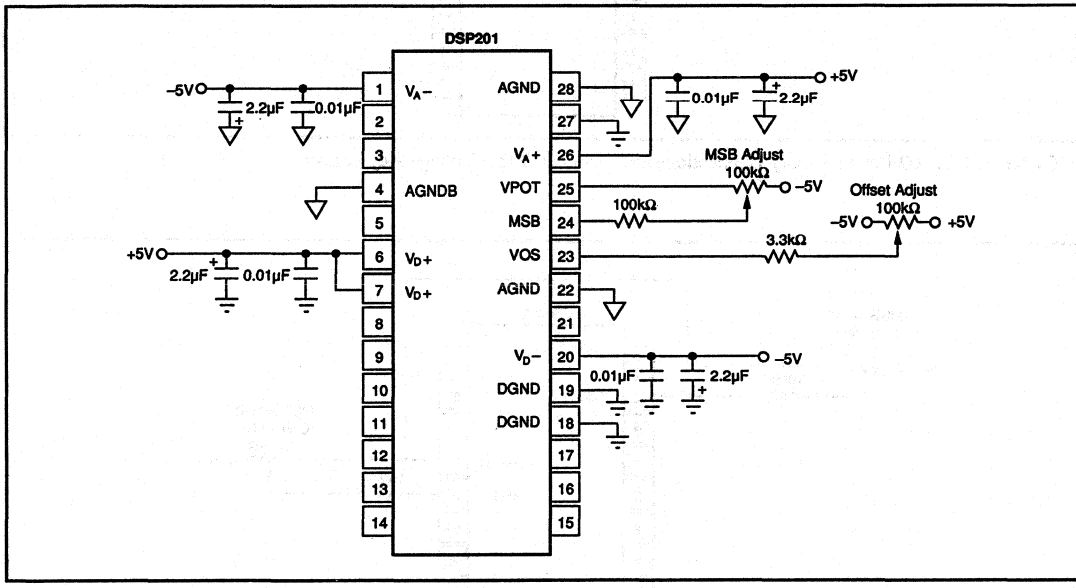


FIGURE 2. DSP201 Power Supply Connections and Optional Adjust Circuits.

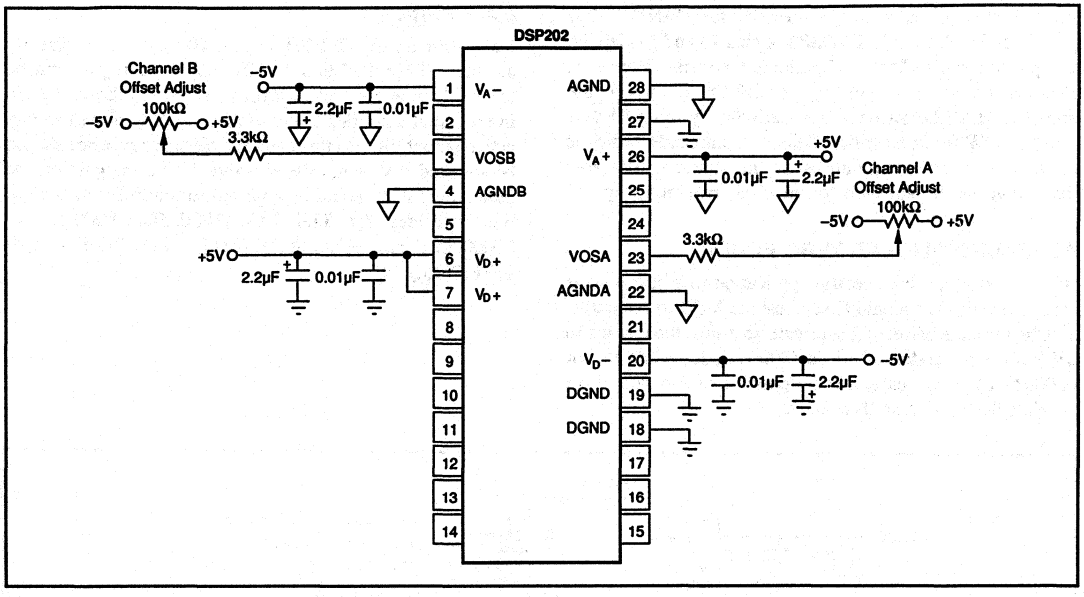


FIGURE 3. DSP202 Power Supply Connections and Optional Offset Voltage Adjustment.

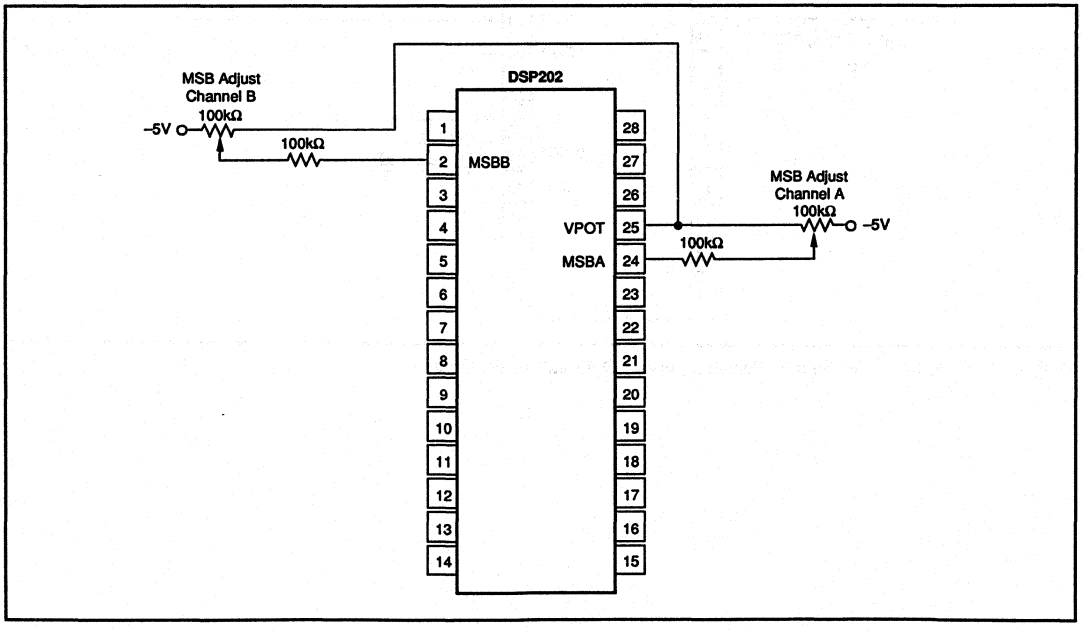


FIGURE 4. DSP202 Optional MSB Adjust Circuit.

APPLICATIONS

USING PARALLEL PORTS WITH THE DSP201 OR DSP202

Figure 5 shows a circuit for converting parallel outputs into the serial data stream required by the DSP201, and meets the requirements for timing signals. Doubling this circuit allows the DSP202 to be driven from a 32-bit parallel port. In most applications, this circuit can be easily incorporated into gate arrays or other programmed logic circuits already used in the system, since the extra gate count is not high.

DEGLITCHING

Particularly in high resolution D/A converters, changing input codes may cause glitching on the output that excessively corrupts the dynamic purity of an output signal. The DSP201 and DSP202 are designed to minimize output glitching, and all of the performance specifications and typical performance curves are based on tests with no extra deglitching circuitry. In particular, the guaranteed Signal-to-(Noise + Distortion) performance would be impossible to attain with any significant glitching.

COMPLETE ANALOG INPUT/OUTPUT SYSTEM

The DSP201 or DSP202 can be paired with the Burr-Brown DSP101 or DSP102 analog-to-digital converter to provide both analog input and analog output for a complete digital signal processing system. The DSP101 and DSP102 are respectively single and dual channel 200kHz sampling A/Ds with easy to use interfacing logic that complement the DSP201 and DSP202. Figure 6 shows a single channel analog input and output system based on a DSP201 and a DSP101, and the minimal connections required to interface to a DSP IC. A pair of channels can be implemented using a single DSP202 and a single DSP102, either with two separate DSP ICs, with a single DSP IC with dual serial input and output channels, or a single DSP IC capable of 32-bit words in the Cascade Mode.

For maximum flexibility in system design, the DSP201 or DSP202 D/As can be updated at a different rate than the conversion rate used on the DSP101 or DSP102 A/Ds, and either or both of these rates can be asynchronous to the clocks used with the DSP IC.

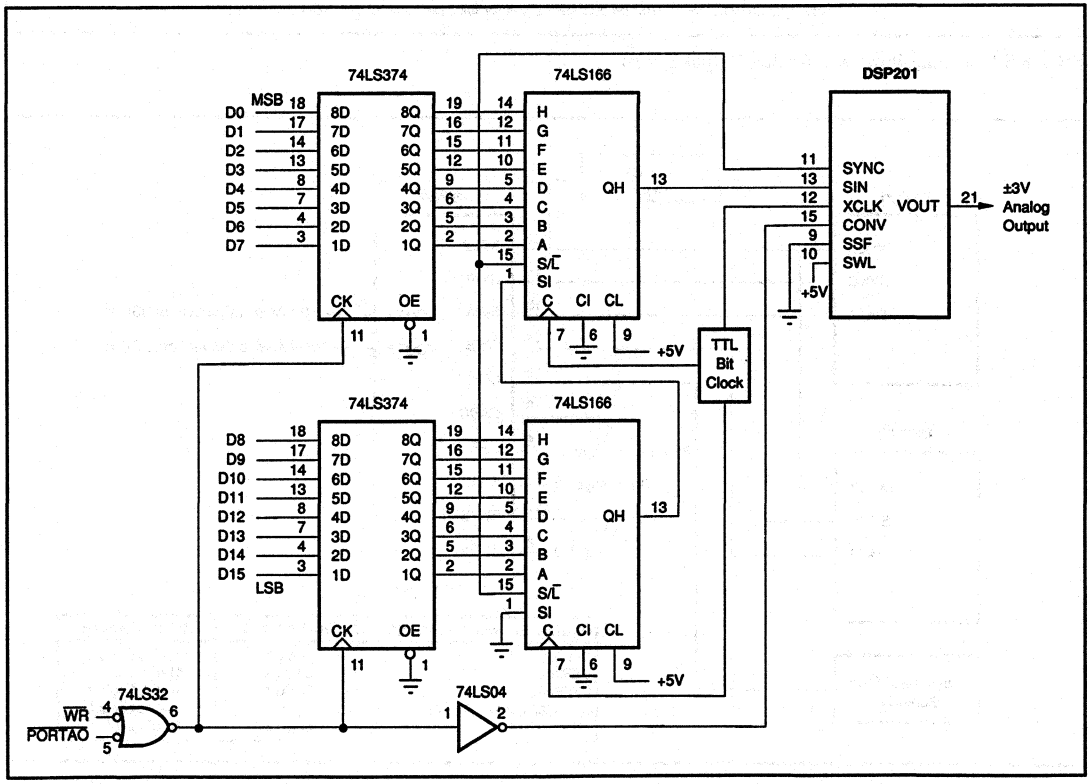
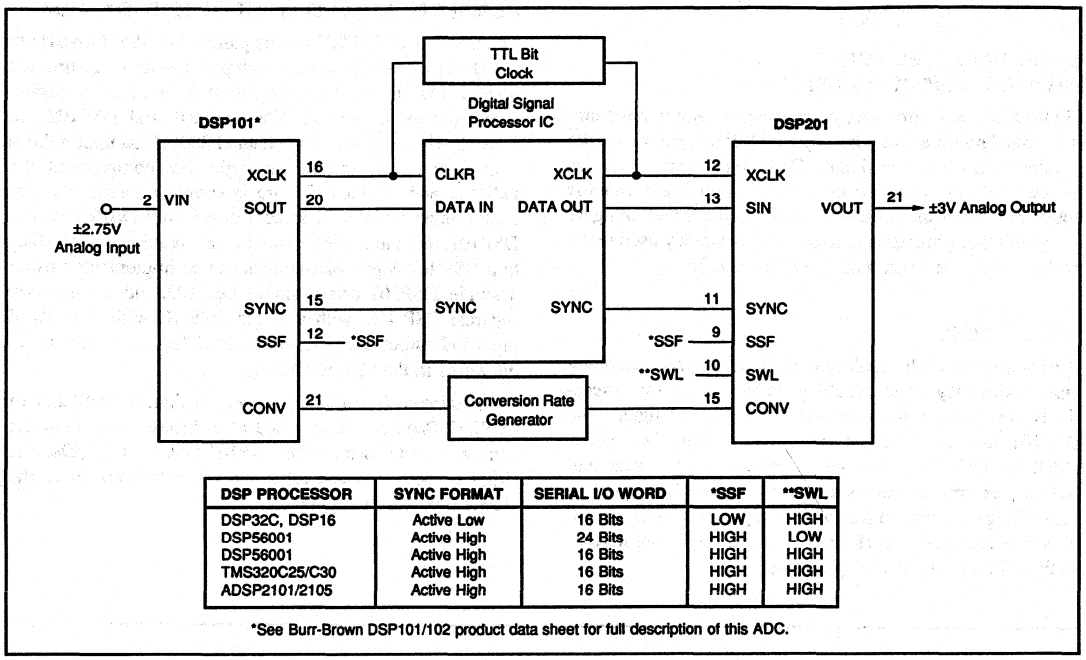


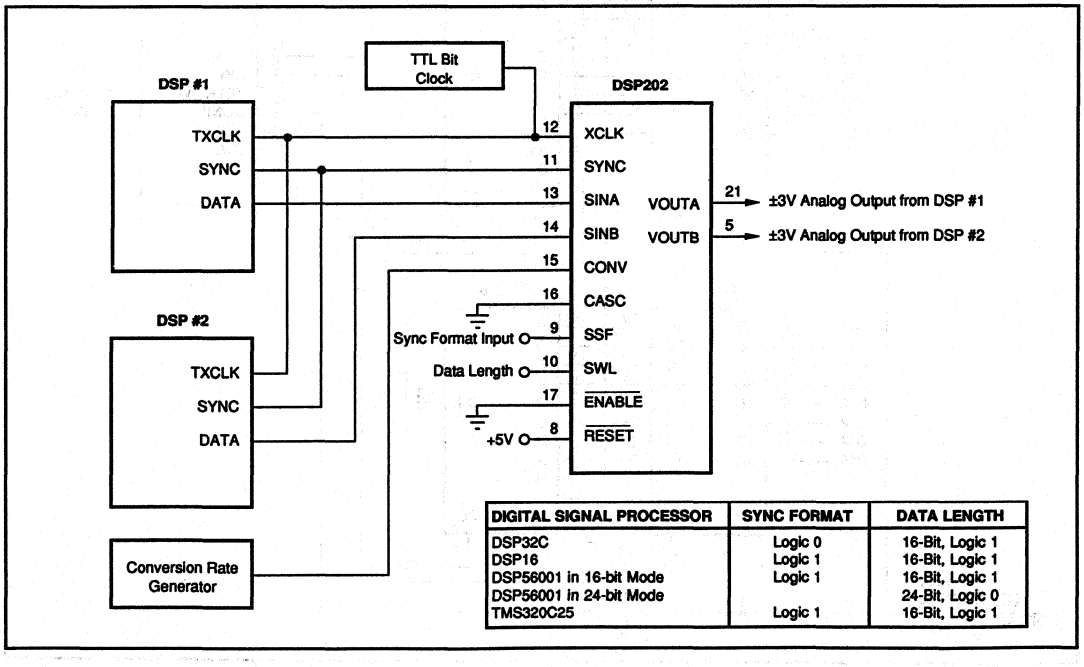
FIGURE 5. Driving the DSP201 from a 16-Bit Parallel Port.



DSP PROCESSOR	SYNC FORMAT	SERIAL I/O WORD	*SSF	**SWL
DSP32C, DSP16	Active Low	16 Bits	LOW	HIGH
DSP56001	Active High	24 Bits	HIGH	LOW
DSP56001	Active High	16 Bits	HIGH	HIGH
TMS320C25/C30	Active High	16 Bits	HIGH	HIGH
ADSP2101/2105	Active High	16 Bits	HIGH	HIGH

*See Burr-Brown DSP101/102 product data sheet for full description of this ADC.

FIGURE 6. Analog Input and Analog Output System.



DIGITAL SIGNAL PROCESSOR	SYNC FORMAT	DATA LENGTH
DSP32C	Logic 0	16-Bit, Logic 1
DSP16	Logic 1	16-Bit, Logic 1
DSP56001 in 16-bit Mode	Logic 1	16-Bit, Logic 1
DSP56001 in 24-bit Mode		24-Bit, Logic 0
TMS320C25	Logic 1	16-Bit, Logic 1

FIGURE 7. DSP202 with Dual DSP ICs.

USING DSP201 AND DSP202 WITH TEXAS INSTRUMENTS DSP ICS

Figures 6 thru 12 show various ways to use the DSP201 and DSP202 with DSP ICs from the Texas Instruments TMS320Cxx series. For simplicity, all of these circuits are based on using the TMS320Cxx in the mode where SSF (Select Synch Format, pin 9) is tied HIGH, so that there is an active High synchronization pulse generated by the DSP201 or DSP202 after receiving a Convert Command. The synchronization pulse can be changed to active Low simply by making SSF LOW, where appropriate, without changing basic operation of the D/As. The timing for either synchronization mode is shown in Figure 1.

In all cases, the DSP201 and DSP202 expect to receive the data with the MSB first, and the TMS320Cxx needs to be programmed for this.

Figure 6 shows a circuit for using the TMS320C25 to generate a complete analog input and analog output system using the DSP201 plus the Burr-Brown DSP101 A/D.

Figure 7 shows how to use two TMS320C25 chips to drive the two channels of the DSP202.

The TMS320C30 has dual serial I/O ports, which can be used to drive the dual inputs on the DSP202, as shown in Figure 8. This circuit can maximize the update rate for the channels. Since the TMS320C30 can also output 32-bit words, both channels of the DSP202 can be updated from a single serial output port on the TMS320C30, using the cascade mode as shown in Figure 9.

Figures 10 and 11 show complete two-channel analog input and analog output systems consisting of three basic chips, the TMS320C30 plus a DSP202 dual D/A and a Burr-Brown DSP102 dual A/D. Figure 10 makes use of the dual serial I/O ports on the TMS320C30, and is shown with the DSP202 in the 16-bit Mode, which maximizes the possible throughput rate on the system. Figure 11 makes use of the 32-bit word length mode in the TMS320C30 and the Cascade Mode on both the DSP202 and the DSP102 to provide two full analog I/O channels over a single serial I/O port on the TMS320C30. Thus, up to four complete, separate analog I/O channels could be operated using a single TMS320C30, by making use of the second serial port.

Figure 12 shows how to use a TMS320C25 to update the analog output of the DSP201.

USING DSP201 AND DSP202 WITH MOTOROLA DSP ICS

Figure 13 shows how to use the DSP201 with a Motorola DSP56001. Using the DSP202 requires using two DSP56001s, as indicated in Figure 7.

The DSP56001 needs to be programmed for transmission of the MSB bit first with SYNC in the Bit Mode. If the DSP56001 is programmed for 16-bit data words, SWL (pin 10) on the DSP201 or DSP202 needs to be tied HIGH to select the 16-bit Mode. In the DSP56001 24-bit mode, the DSP201 or DSP202 can be programmed to accept data lengths of 16-bits (with SWL HIGH) or 18-bits (with SWL LOW), and will ignore the trailing bits on the serial line.

For use with the Motorola DSP56001, SSF (pin 9) on the DSP201 or DSP202 needs to be tied HIGH. This will cause the DSP201 or DSP202 to transmit an appropriate active High synchronization pulse on SYNC (pin 11) after a Convert Command is received by the DSP201 or DSP202. Timing is shown in Figure 1.

Even though the DSP201 or DSP202 require a minimum of 24 Bit Clock pulses between convert commands, the maximum update rate for the D/As using a 5MHz Bit Clock will still be over 200kHz (5MHz / 24 = 208.3kHz.)

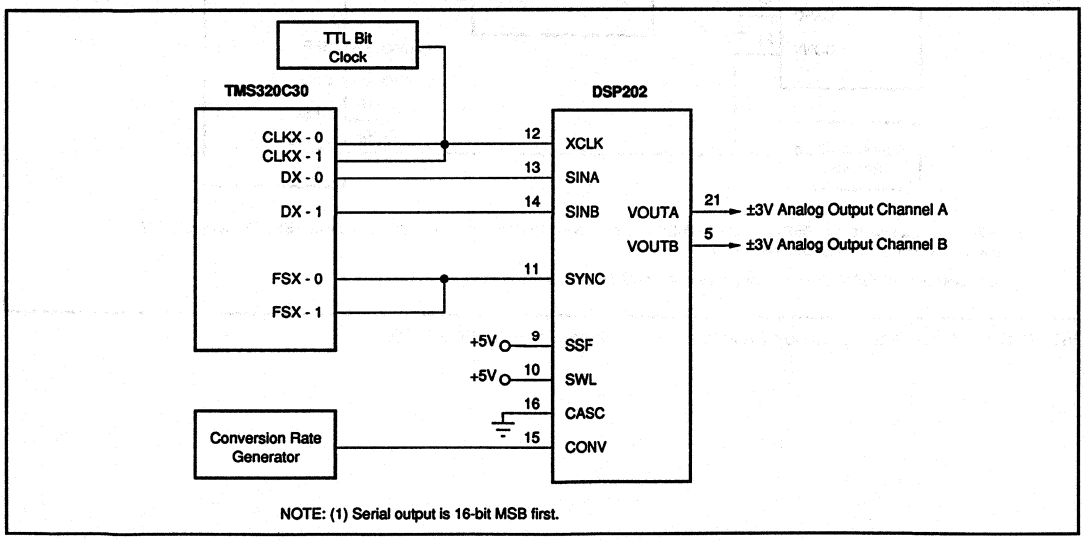


FIGURE 8. Using DSP202 with TMS320C30's Dual SIO.

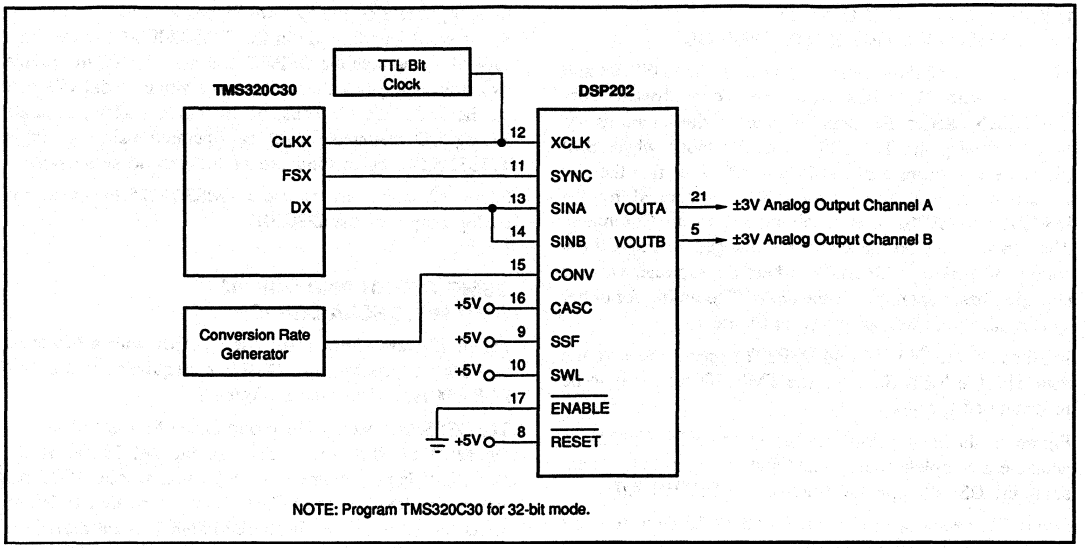


FIGURE 9. Using DSP202 with TMS320C30 in Cascade Mode.

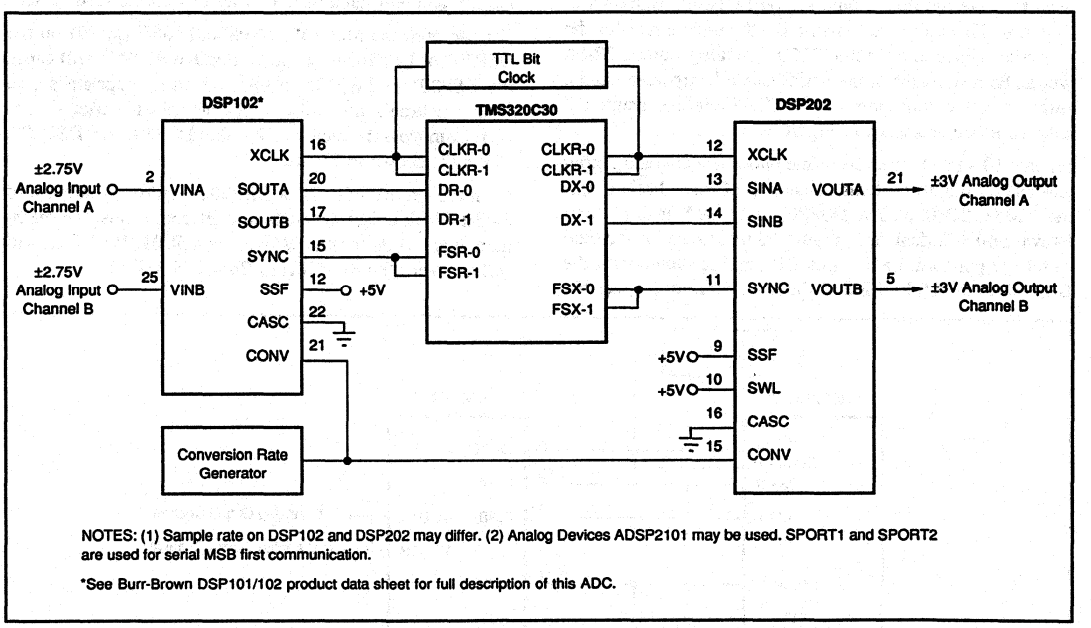


FIGURE 10. Two-Channel Analog Input and Output System with TMS320C30.

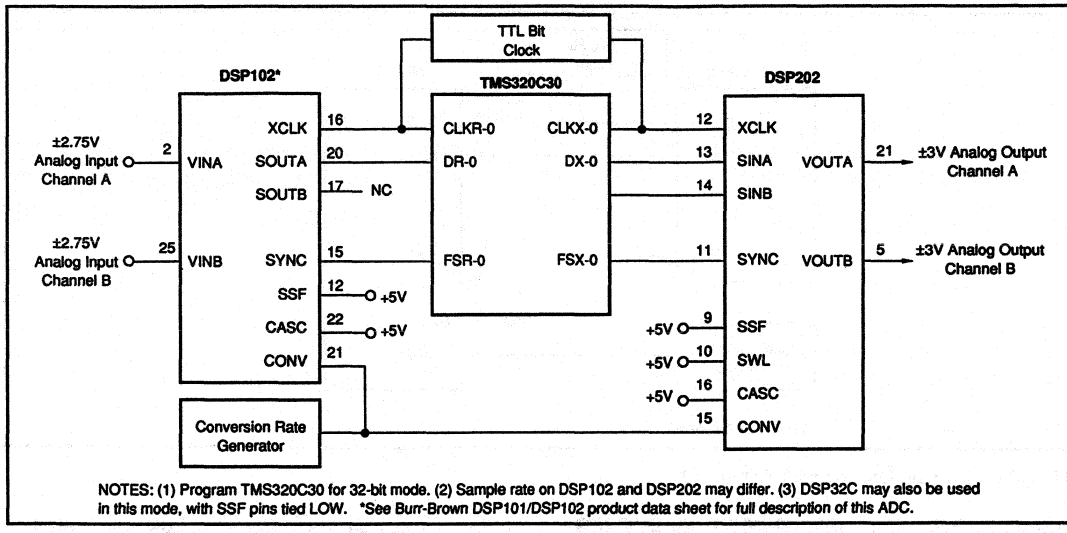


FIGURE 11. Two-Channel Analog Input and Output System with TMS320C30 in Cascade Mode.

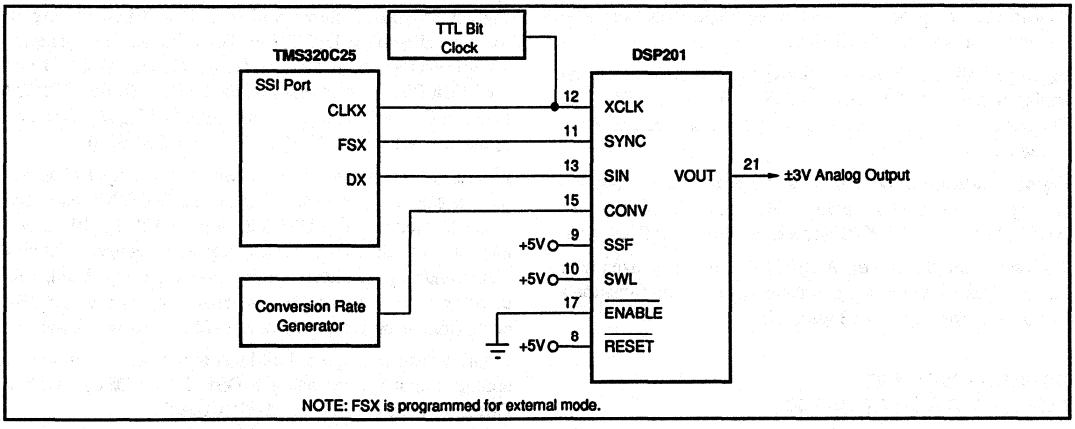


FIGURE 12. Using DSP201 with TMS320C25.

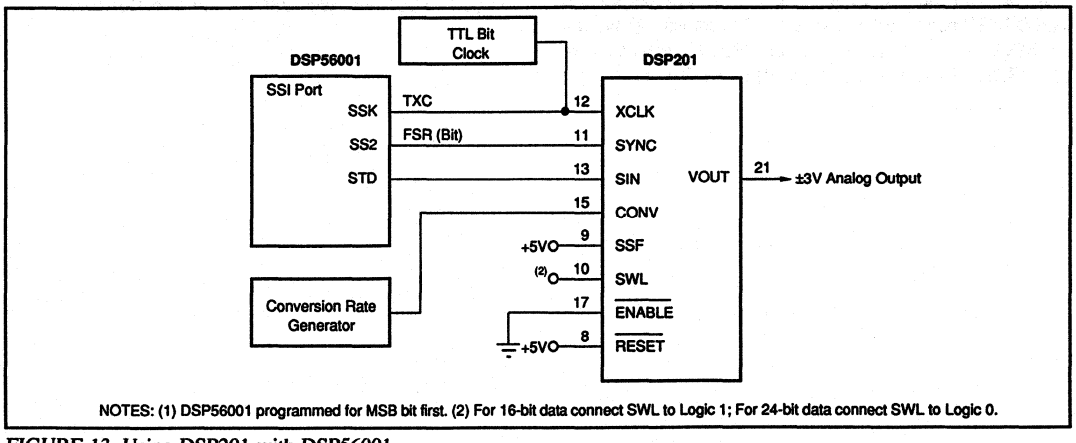


FIGURE 13. Using DSP201 with DSP56001.

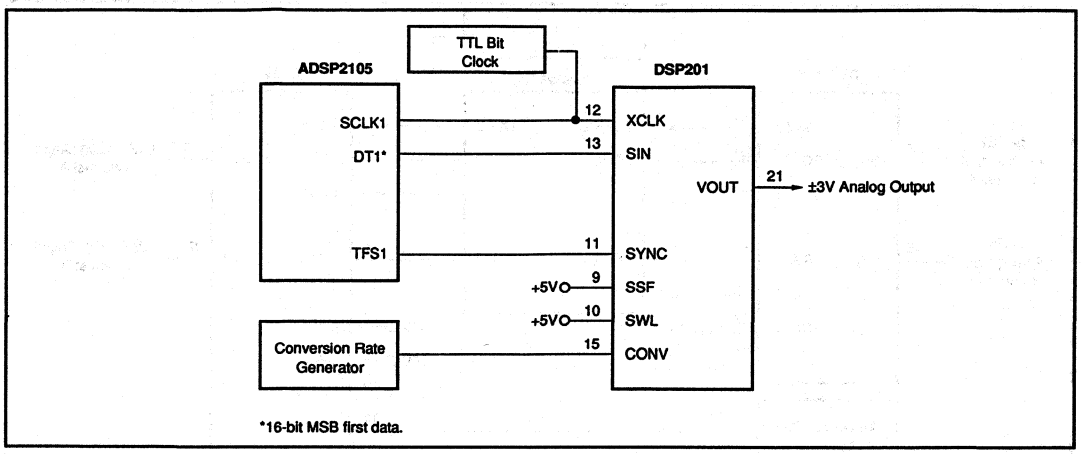


FIGURE 14. Using DSP201 with ADSP-2105.

USING DSP201 AND DSP202 WITH ADI DSP ICS

When using the DSP201 or DSP202 with the ADSP2101 or ADSP2105, the processors need to be programmed to transmit the data with the MSB first.

Figure 14 shows the connections required to generate an analog output channel using an ADSP2105 with the DSP201. The same basic circuit can also be used to connect a DSP201 to the ADSP2101.

Figure 6 indicates how to build a complete analog input and analog output system using either the ADSP2101 or ADSP2105 with a DSP201 and a Burr-Brown DSP101 A/D.

The two serial ports on the ADSP2101 can also be used with the DSP202 to make two complete analog output channels as noted in footnote 2 of Figure 10.

USING DSP201 AND DSP202 WITH AT&T DSP ICS

Figures 15, 16 and 17 show how to use the DSP201 and DSP202 with the DSP16 and DSP32C in different modes. The DSP IC needs to be programmed to transmit data with the MSB first, and the DSP201 or DSP202 needs to have SSF (Select Sync Format on pin 9) tied LOW so that the D/As will output an appropriate active Low synchronization pulse after a Convert Command is received.

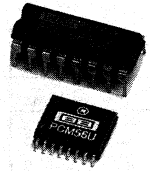
Figures 15 and 17 show the DSP32C and DSP16 respectively used with the DSP201 in the 16-bit Mode to generate a single analog output channel. With a 12MHz Bit Clock and the 24 Bit Clock cycles required by the DSP201 and DSP202 between Convert Commands, the output of Figure 15 can be updated at a full 500kHz (12MHz/24 = 500kHz.)

Figure 16 shows how to drive two analog output channels from a single 32-bit serial port on the DSP32C, using the Cascade Mode on the DSP202. With a 12MHz Bit Clock and the 40 Bit Clock cycles required between Convert Commands by the DSP for internal logic overhead, this circuit can update two separate analog outputs at 300kHz each from a single serial port (12MHz/40 = 300kHz.)

Figure 6 indicates how to build a complete analog input and analog output system using a DSP32C or DSP16 with a DSP201 and a Burr-Brown DSP101 A/D.

Figure 7 shows a two channel analog output system using a single DSP202 with two DSP32Cs or two DSP16s.

BURR-BROWN®



PCM56P
PCM56U

DESIGNED FOR AUDIO

Serial Input 16-Bit Monolithic DIGITAL-TO-ANALOG CONVERTER

FEATURES

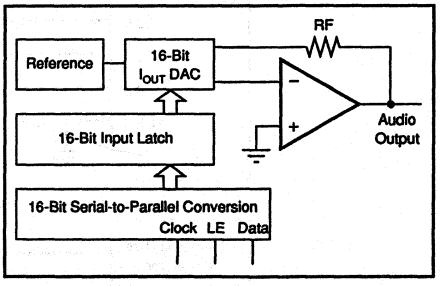
- SERIAL INPUT
- LOW COST
- NO EXTERNAL COMPONENTS REQUIRED
- 16-BIT RESOLUTION
- 15-BIT MONOTONICITY, TYP
- 0.001% OF FSR TYP DIFFERENTIAL LINEARITY ERROR
- 0.0025% MAX THD: FS Input, K Grade, 16 Bits
- 0.02% MAX THD: –20dB Input, K Grade, 16 Bits
- 1.5µs SETTLING TIME, TYP: Voltage Out
- 96dB DYNAMIC RANGE
- ±3V OR ±1mA AUDIO OUTPUT
- EIAJ STC-007-COMPATIBLE
- OPERATES ON ±5V TO ±12V SUPPLIES
- PINOUT ALLOWS I_{OUT} OPTION
- PLASTIC DIP OR SOIC PACKAGE

DESCRIPTION

The PCM56 is a state-of-the-art, fully monotonic, digital-to-analog converter that is designed and specified for digital audio applications. This device employs ultra-stable nichrome (NiCr) thin-film resistors to provide monotonicity, low distortion, and low differential linearity error (especially around bipolar zero) over long periods of time and over the full operating temperature.

This converter is completely self-contained with a stable, low noise, internal zener voltage reference; high speed current switches; a resistor ladder network; and a fast settling, low noise output operational amplifier all on a single monolithic chip. The converters are operated using two power supplies that can range from ±5V to ±12V. Power dissipation with ±5V supplies is typically less than 200mW. Also included is a provision for external adjustment of the MSB error (differential linearity error at bipolar zero) to further improve total harmonic distortion (THD) specifications if desired. Few external components are necessary for operation, and all critical specifications are 100% tested. This helps assure the user of high system reliability and outstanding overall system performance.

The PCM56 is packaged in a high-quality 16-pin molded plastic DIP package or SOIC and has passed operating life tests under simultaneous high-pressure, high-temperature, and high-humidity conditions.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 66-6491 • FAX: (602) 889-1510

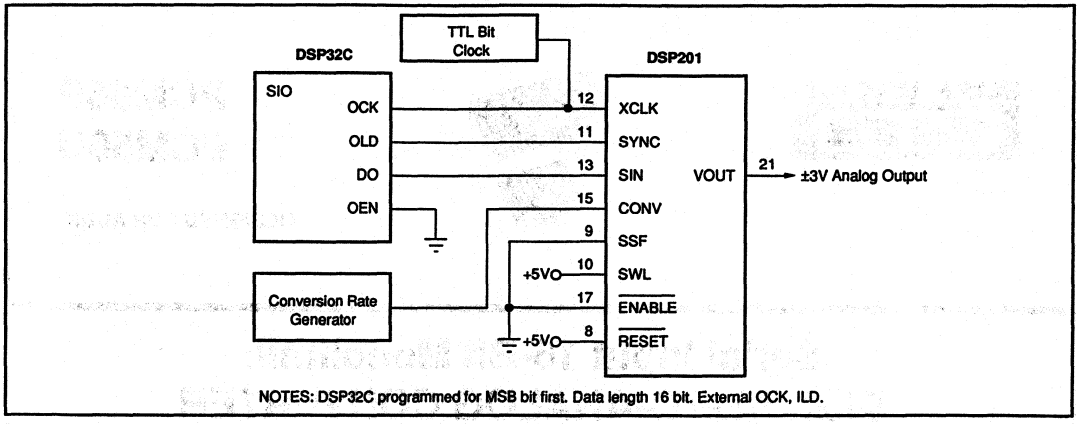


FIGURE 15. Using DSP201 with DSP32C with 16-Bit Data Words.

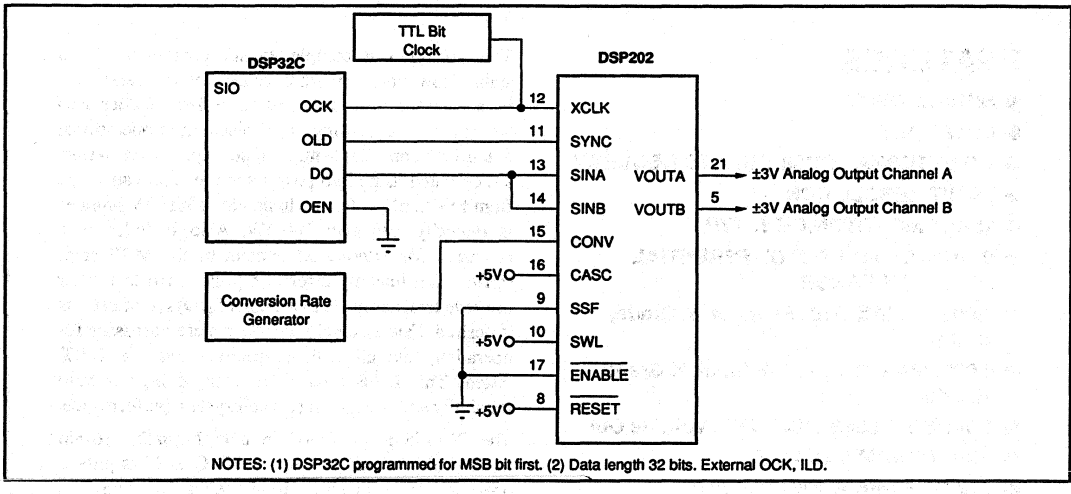


FIGURE 16. Using DSP202 with DSP32C in Cascade Mode.

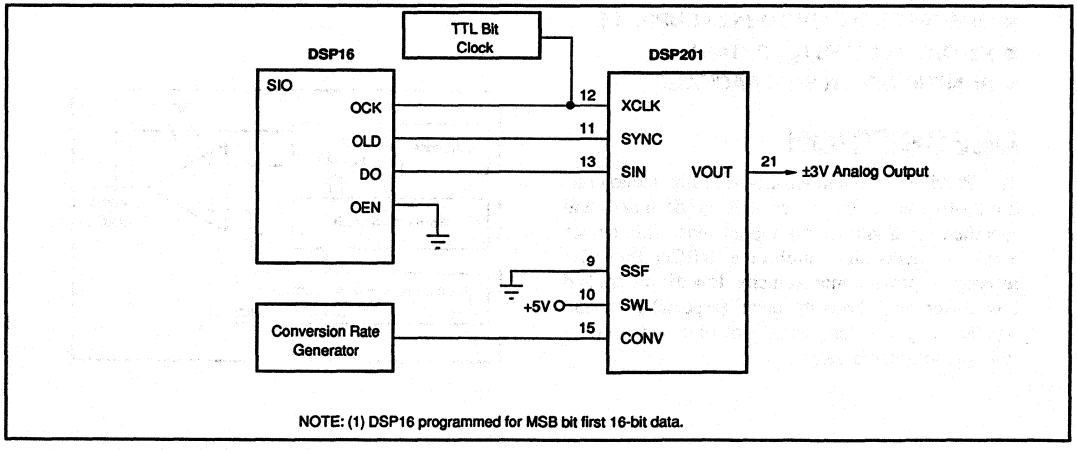


FIGURE 17. Using DSP201 with DSP16.

SPECIFICATIONS

ELECTRICAL

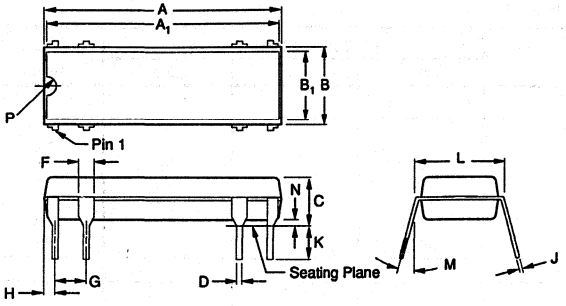
Typical at +25°C, and nominal power supply voltages ±5V unless otherwise noted.

PARAMETER	PCM56U, PCM56P/-J/-K MIN	TYP	MAX	UNITS
INPUT				
DIGITAL INPUT				
Resolution		16		Bits
Digital Inputs[1]: V_{IH}	+2.4		$+V_L$	V
V_{IL}	0		+0.8	V
I_{IH}, V_{IN} = +2.7V			+1.0	µA
I_{IL}, V_{IN} = +0.4V			–50	µA
Input Clock Frequency	10.0			MHz
TRANSFER CHARACTERISTICS				
ACCURACY				
Gain Error		±2.0		%
Bipolar Zero Error		±30		mV
Differential Linearity Error		±0.001		% of FSR[2]
Noise (rms, 20Hz to 20kHz) at Bipolar Zero (V_{OUT} models)		6		µV
TOTAL HARMONIC DISTORTION				
V_O = ±FS at f = 991Hz: PCM56P-K		0.002	0.0025	%
PCM56P-J		0.002	0.004	%
PCM56P, PCM56U		0.002	0.008	%
PCM56P-L		0.002	0.010	%
V_O = –20dB at f = 991Hz: PCM56P-K		0.018	0.020	%
PCM56P-J		0.018	0.040	%
PCM56P, PCM56U		0.018	0.040	%
PCM56P-L		0.018	0.10	%
V_O = –60dB at f = 991Hz: PCM56P-K		1.8	2.0	%
PCM56P-J		1.8	4.0	%
PCM56P, PCM56U		1.8	4.0	%
PCM56P-L		1.8	10.0	%
MONOTONICITY		15		Bits
DRIFT (0°C to +70°C)				
Total Drift[3]		±25		ppm of FSR/°C
Bipolar Zero Drift		±4		ppm of FSR/°C
SETTLING TIME (to ±0.006% of FSR)				
Voltage Output: 6V Step		1.5		µs
1LSB		1.0		µs
Slew Rate		12		V/µs
Current Output, 1mA Step: 10Ω to 100Ω Load		350		ns
1kΩ Load[4]		350		ns
WARM-UP TIME	1			Min
OUTPUT				
Voltage Output Configuration: Bipolar Range		±3.0		V
Output Current	±8.0			mA
Output Impedance		0.10		Ω
Short Circuit Duration		Indefinite to Common		
Current Output Configuration:				
Bipolar Range (±30%)		±1.0		mA
Output Impedance (±30%)		1.2		kΩ
POWER SUPPLY REQUIREMENTS[5]				
Voltage: $+V_S$ and $+V_L$	+4.75	+5.00	+13.2	V
$–V_S$ and $–V_L$	–4.75	–5.00	–13.2	V
Supply Drain (No Load): +V ($+V_S$ and $+V_L$ = +5V)		+10.00	+17.0	mA
–V ($–V_S$ and $–V_L$ = –5V)		–25.0	–35.0	mA
+V ($+V_S$ and $+V_L$ = +12V)		+12.0		mA
–V ($–V_S$ and $–V_L$ = –12V)		–27.0		mA
Power Dissipation: V_S and V_L = ±5V		175	260	mW
V_S and V_L = ±12V		468		mW
TEMPERATURE RANGE				
Specification	0		+70	°C
Operation	–25		+70	°C
Storage	–60		+100	°C

NOTES: (1) Logic input levels are TTL/CMOS-compatible. (2) FSR means full-scale range and is equivalent to 6V (±3V) for PCM56 in the V_{OUT} mode. (3) This is the combined drift error due to gain, offset, and linearity over temperature. (4) Measured with an active clamp to provide a low impedance for approximately 200ns. (5) All specifications assume $+V_S$ connected to $+V_L$ and $–V_S$ connected to $–V_L$. If supplies are connected separately, $–V_L$ must not be more negative than $–V_S$ supply voltage to assure proper operation. No similar restriction applies to the value of $+V_L$ with respect to $+V_S$.

MECHANICAL

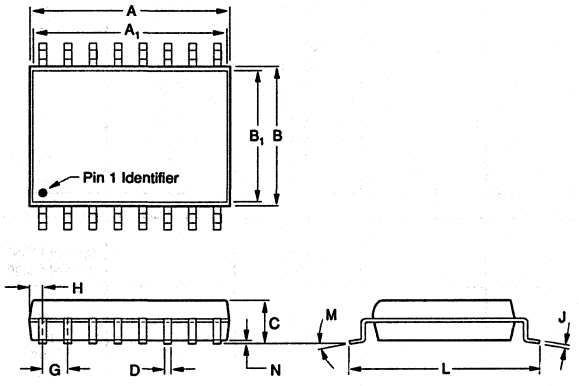
P Package — Single Wide 16-Pin Plastic DIP



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	.740	.800	18.80	20.32
A1	.725	.785	18.42	19.94
B	.230	.290	5.85	7.38
B1	.200	.250	5.09	6.36
C	.120	.200	3.05	5.09
D	.015	.023	0.38	0.59
F	.030	.070	0.76	1.78
G	.100 BASIC		2.54 BASIC	
H	.020	.050	0.51	1.27
J	.008	.015	0.20	0.38
K	.070	.150	1.78	3.82
L	.300 BASIC		7.63 BASIC	
M	0°	15°	0°	15°
N	.010	.030	0.25	0.76
P	.025	.050	0.64	1.27

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

U Package — 16-Pin SOIC



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	.400	.416	10.16	10.57
A1	.388	.412	9.86	10.46
B	.286	.302	7.26	7.67
B1	.268	.286	6.81	7.26
C	.093	.109	2.36	2.77
D	.015	.020	0.38	0.51
G	.050 BASIC		1.27 BASIC	
H	.022	.038	0.56	0.97
J	.008	.012	0.20	0.30
L	.391	.421	9.93	10.69
M	5° TYP		5° TYP	
N	.000	.012	0.00	0.30

NOTE: Leads in true position within 0.010" (0.25mm) R at MMC at seating plane.

ORDERING INFORMATION

MODEL	THD AT FS (%)
PCM56U	0.008 Max
PCM56P	0.008 Max
PCM56P-J	0.004
PCM56P-K	0.0025
PCM56P-L	0.01

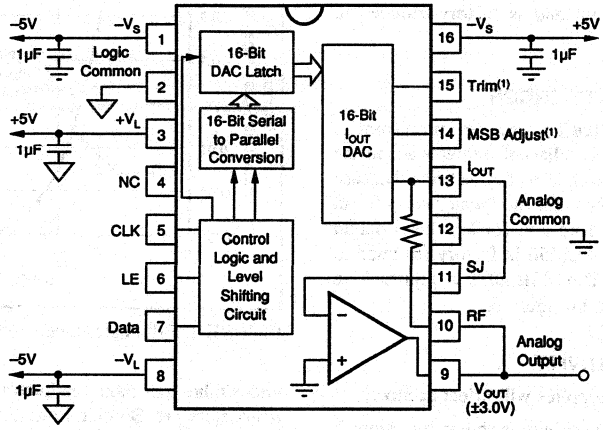
ABSOLUTE MAXIMUM RATINGS

DC Supply Voltages	±16VDC
Input Logic Voltage	–1V to $+V_S$/$+V_L$
Power Dissipation	850mW
Operating Temperature	–25°C to +70°C
Storage Temperature	–60°C to +100°C
Lead Temperature (soldering, 10s)	+300°C

PIN ASSIGNMENTS

PIN	DESCRIPTION	MNEMONIC
P1	Analog Negative Supply	$-V_S$
P2	Logic Common	LOG COM
P3	Logic Positive Supply	$+V_L$
P4	No Connection	NC
P5	Clock Input	CLK
P6	Latch Enable Input	LE
P7	Serial Data Input	DATA
P8	Logic Negative Supply	$-V_L$
P9	Voltage Output	V_{OUT}
P10	Feedback Resistor	RF
P11	Summing Junction	SJ
P12	Analog Common	ANA COM
P13	Current Output	I_{OUT}
P14	MSB Adjustment Terminal	MSB ADJ
P15	MSB Trim-pot Terminal	TRIM
P16	Analog Positive Supply	$+V_S$

CONNECTION DIAGRAM



NOTE: (1) MSB error (Bipolar Zero differential linearity error) can be adjusted to zero using the external circuit shown in Figure 6.

DISCUSSION OF SPECIFICATIONS

The PCM56 is specified to provide critical performance criteria for a wide variety of applications. The most critical specifications for D/A converter in audio applications are Total Harmonic Distortion, Differential Linearity Error, Bipolar Zero Error, parameter shifts with time and temperature, and settling time effects on accuracy.

The PCM56 is factory-trimmed and tested for all critical key specifications.

The accuracy of a D/A converter is described by the transfer function shown in Figure 1. Digital input to analog output relationship is shown in Table I. The errors in the D/A converter are combinations of analog errors due to the linear circuitry, matching and tracking properties of the ladder and scaling networks, power supply rejection, and reference errors. In summary, these errors consist of initial errors including Gain, Offset, Linearity, Differential Linearity, and Power Supply Sensitivity. Gain drift over temperature rotates the line (Figure 1) about the bipolar zero point and Offset drift shifts the line left or right over the operating temperature range. Most of the Offset and Gain drift with temperature or time is due to the drift of the internal reference zener diode. The converter is designed so that these drifts are in opposite directions. This way the Bipolar Zero voltage is virtually unaffected by variations in the reference voltage.

DIGITAL INPUT CODES

The PCM56 accepts serial input data (MSB first) in the Binary Two's Complement (BTC) form. Refer to Table I for input/output relationships.

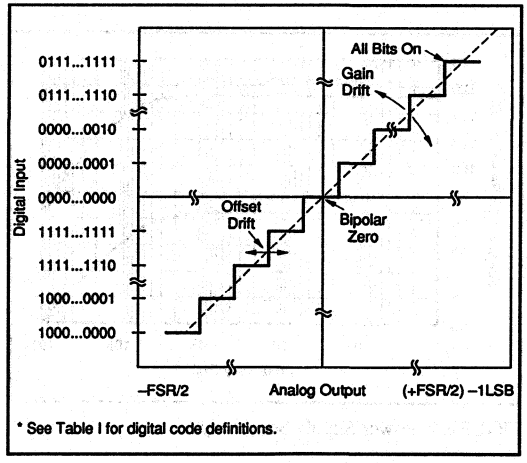


FIGURE 1. Input vs Output for an Ideal Bipolar D/A Converter.

DIGITAL INPUT	ANALOG OUTPUT		
Binary Two's Complement (BTC)	DAC Output	Voltage (V), V_{OUT} Mode	Current (mA), I_{OUT} Mode
7FFF Hex	+ Full Scale	+2.999908	–0.999970
8000 Hex	– Full Scale	–3.000000	+1.000000
0000 Hex	Bipolar Zero	0.000000	0.000000
FFFF Hex	Zero –1LSB	–0.000092	+0.030500µA

TABLE I. Digital Input to Analog Output Relationship.

BIPOLAR ZERO ERROR

Initial Bipolar Zero Error (Bit 1 "on" and all other bits "off") is the deviation from 0V out and is factory-trimmed to typically ±30mV at +25°C.

DIFFERENTIAL LINEARITY ERROR

Differential Linearity Error (DLE) is the deviation from an ideal 1LSB change from one adjacent output state to the next. DLE is important in audio applications because excessive DLE at Bipolar Zero (at the "major carry") can result in audible crossover distortion for low level output signals. Initial DLE on the PCM56 is factory trimmed to typically ±0.001% of FSR. The MSB DLE is adjustable to zero using the circuit shown in Figure 6.

POWER SUPPLY SENSITIVITY

Changes in the DC power supplies will affect accuracy.

The PCM56 power supply sensitivity is shown by Figure 2. Normally, regulated power supplies with 1% or less ripple are recommended for use with the DAC. See also Power Supply Connections paragraph in the Installation and Operating Instructions section.

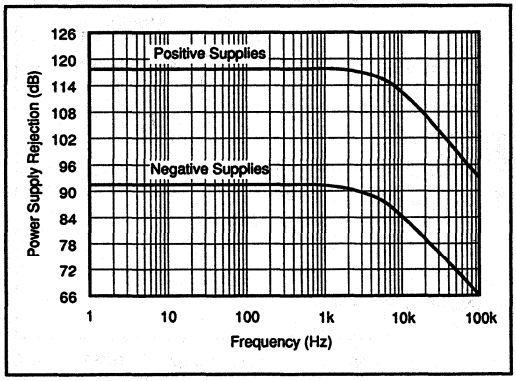


FIGURE 2. Power Supply Sensitivity.

SETTLING TIME

Settling time is the total time (including slew time) required for the output to settle within an error band around its final value after a change in input (see Figure 3).

Settling times are specified to ±0.006% of FSR: one for a large output voltage change of 6V and one for a 1LSB change. The 1LSB change is measured at the major carry (0000 hex to ffff hex), the point at which the worst-case settling time occurs.

STABILITY WITH TIME AND TEMPERATURE

The parameters of a D/A converter designed for audio applications should be stable over a relatively wide temperature range and over long periods of time to avoid

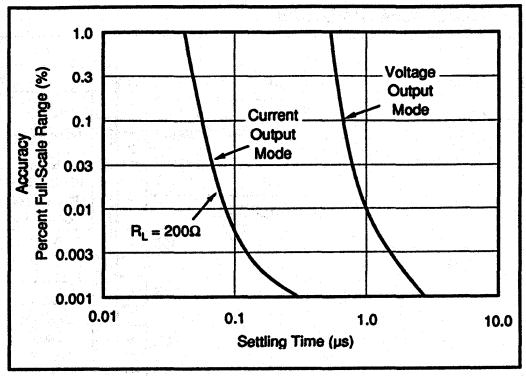


FIGURE 3. Full Scale Range Settling Time vs Accuracy.

undesirable periodic readjustment. The most important parameters are Bipolar Zero Error, Differential Linearity Error, and Total Harmonic Distortion. Most of the Offset and Gain drift with temperature or time is due to the drift of the internal reference zener diode. The PCM56 is designed so that these drifts are in opposite directions so that the Bipolar Zero voltage is virtually unaffected by variations in the reference voltage. Both DLE and THD are dependent upon the matching and tracking of resistor ratios and upon V_{BE} and h_{FE} of the current-source transistors. The PCM56 was designed so that any absolute shift in these components has virtually no effect on DLE or THD. The resistors are made of identical links of ultra-stable nichrome thin-film. The current density in these resistors is very low to further enhance their stability.

DYNAMIC RANGE

The Dynamic Range is a measure of the ratio of the smallest signals the converter can produce to the full-scale range and is usually expressed in decibels (dB). The theoretical dynamic range of a converter is approximately 6 X n, or about 96dB of a 16-bit converter. The actual, or useful, dynamic range is limited by noise and linearity errors and is therefore somewhat less than the theoretical limit. However, this does point out that a resolution of at least 16 bits is required to obtain a 90dB minimum dynamic range, regardless of the accuracy of the converter. Another specification that is useful for audio applications is Total Harmonic Distortion.

TOTAL HARMONIC DISTORTION

THD is useful in audio applications and is a measure of the magnitude and distribution of the Linearity Error, Differential Linearity Error, and Noise, as well as Quantization Error. To be useful, THD should be specified for both high level and low level input signals. This error is unadjustable and is the most meaningful indicator of D/A converter accuracy for audio applications.

The THD is defined as the ratio of the square root of the sum of the squares of the values of the harmonics to the value of

the fundamental input frequency and is expressed in percent or dB. The rms value of the PCM56 error referred to the input can be shown to be:

$$\epsilon_{rms} = \sqrt{1/n \sum_{i=1}^{n} \left[E_L(i) + E_Q(i)\right]^2} \quad (1)$$

where n is the number of samples in one cycle of any given sine wave, $E_L(i)$ is the linearity error of the PCM56 at each sampling point, and $E_Q(i)$ is the quantization error at each sampling point. The THD can then be expressed as:

$$THD = \epsilon_{rms} / E_{rms} = \frac{\sqrt{1/n \sum_{i=1}^{n} \left[E_L(i) + E_Q(i)\right]^2}}{E_{rms}} \times 100\% \quad (2)$$

where E_{rms} is the rms signal-voltage level.

This expression indicates that, in general, there is a correlation between the THD and the square root of the sum of the squares of the linearity errors at each digital word of interest. However, this expression does not mean that the worst-case linearity error of the D/A is directly correlated to the THD.

For the PCM56 the test period was chosen to be 22.7µs (44.1kHz), which is compatible with the EIAJ STC-007 specification for PCM audio. The test frequency is 991Hz and the amplitude of the input signal is 0dB, –20dB, and –60dB down from full scale.

Figure 4 shows the typical THD as a function of output voltage.

Figure 5 shows typical THD as a function of frequency.

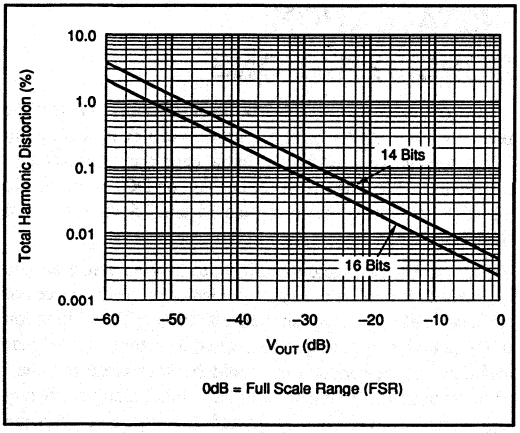


FIGURE 4. Total Harmonic Distortion (THD) vs V_{OUT}.

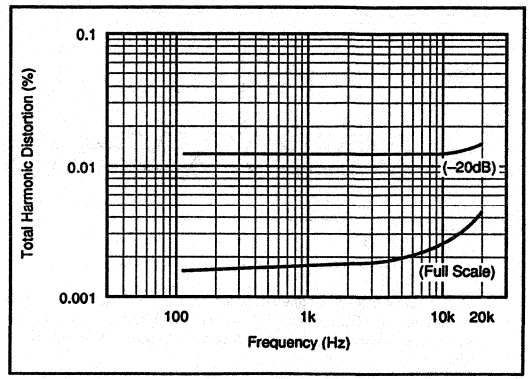


FIGURE 5. Total Harmonic Distortion (THD) vs Frequency.

INSTALLATION AND OPERATING INSTRUCTIONS

POWER SUPPLY CONNECTIONS

For optimum performance and noise rejection, power supply decoupling capacitors should be added as shown in the Connection Diagram. These capacitors (1µF tantalum or electrolytic recommended) should be located close to the converter.

MSB ERROR ADJUSTMENT PROCEDURE (OPTIONAL)

The MSB error of the PCM56 can be adjusted to make the differential linearity error (DLE) at BPZ essentially zero. This is important when the signal output levels are very low, because zero crossing noise (DLE at BPZ) becomes very significant when compared to the small code changes occurring in the LSB portion of the converter.

Differential linearity error at bipolar zero and THD are guaranteed to meet data sheet specifications without any external adjustment. However, a provision has been made for an optional adjustment of the MSB linearity point which makes it possible to eliminate DLE error at BPZ. Two procedures are given to allow either static or dynamic adjustment. The dynamic procedure is preferred because of the difficulty associated with the static method (accurately measuring 16-bit LSB steps).

To statically adjust DLE at BPZ, refer to the circuit shown in Figure 6, or the PCM56 connection diagram.

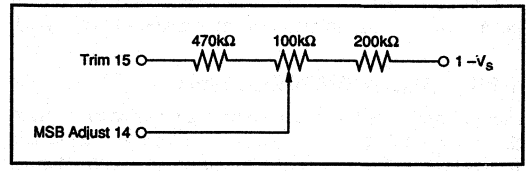
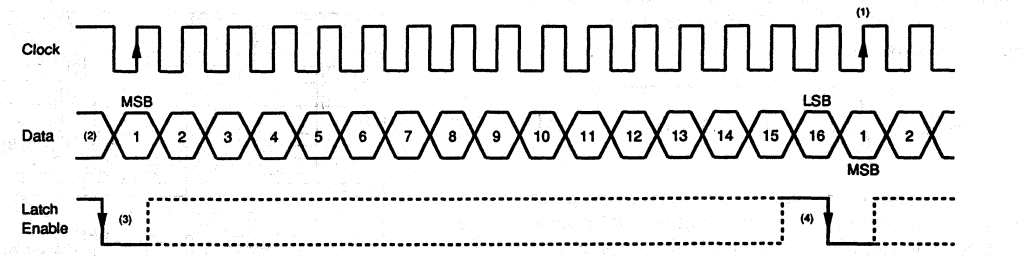


FIGURE 6. MSB Adjustment Circuit.



NOTES: (1) If clock is stopped between input of 16-bit data words, latch enable (LE) must remain low until after the first clock of the next 16-bit data word stream. (2) Data format is binary two's complement (BTC). Individual data bits are clocked in on the corresponding positive clock edge. (3) Latch enable (LE) must remain low at least one clock cycle after going negative. (4) Latch enable (LE) must be high for at least one clock cycle before going negative.

FIGURE 7. Input Timing Diagram.

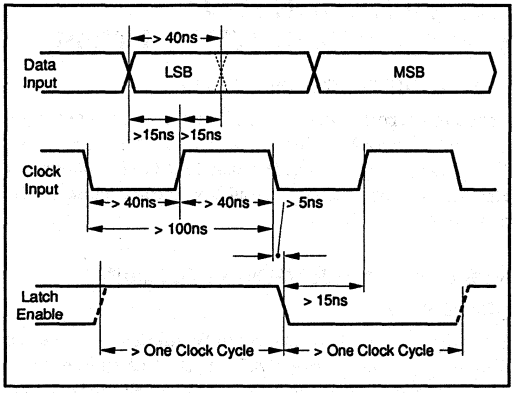


FIGURE 8. Input Timing Relationships.

After allowing ample warm-up time (5-10 minutes) to assure stable operation of the PCM56, select input code FFFF hexadecimal (all bits on except the MSB). Measure the audio output voltage using a 6-1/2 digit voltmeter and record it. Change the digital input code to 0000 hexadecimal (all bits off except the MSB). Adjust the 100kΩ potentiometer to make the audio output read 92μV more than the voltage reading of the previous code (a 1LSB step = 92μV).

A much simpler method is to dynamically adjust the DLE at BPZ. Again, refer to Figure 6 for circuitry and component values. Assuming the device has been installed in a digital audio application circuit, send the appropriate digital input to produce a –80dB level sinusoidal output. While measuring the THD of the audio circuit output, adjust the 100kΩ potentiometer until a minimum level of distortion is observed.

INPUT TIMING CONSIDERATIONS

Figure 7 and 8 refer to the input timing required to interface the inputs of PCM56 to a serial input data stream. Serial data is accepted in Binary Two's Complement (BTC) with the MSB being loaded first. Data is clocked in on positive going clock (CLK) edges and is latched into the DAC input register on negative going latch enable (LE) edges.

The latch enable input must be high for at least one clock cycle before going low, and then must be held low for at least one clock cycle. The last 16 data bits clocked into the serial input register are the ones that are transferred to the DAC input register when latch enable goes low. In other words, when more than 16 clock cycles occur between a latch enable, only the data present during the last 16 clocks will be transferred to the DAC input register.

One requirement for clocking in all 16 bits is the necessity for a "17th" clock pulse. This automatically occurs when the clock is continuous (last bit shifts in on the first bit of the next data word). If the clock is stopped between input of 16-bit data words, the latch enable (LE) must remain low until after the first clock of the next 16-bit data word stream. This ensures that the latch is properly set up.

Figure 7 refers to the general input format required for the PCM56. Figure 8 shows the specific relationships between the various signals and their timing constraints.

INSTALLATION CONSIDERATIONS

If the optional external MSB error circuitry is used, a potentiometer with adequate resolution and a TCR of 100ppm/°C or less is required. Also, extra care must be taken to insure that no leakage path (either AC or DC) exists to pin 14. If the circuit is not used, pins 14 and 15 should be left open.

The PCM converter and the wiring to its connectors should be located to provide the optimum isolation from sources of RFI and EMI. The important consideration in the elimination of RF radiation or pickup is loop area; therefore, signal leads and their return conductors should be kept close together. This reduces the external magnetic field along with any radiation. Also, if a signal lead and its return conductor are wired close together, they represent a small flux-capture cross section for any external field. This reduces radiation pickup in the circuit.

APPLICATIONS

Figures 9 and 10 show a circuit and timing diagram for a single PCM56 used to obtain both left- and right-channel output in a typical digital audio system. The audio output of the PCM56 is alternately time-shared between the left and right channels. The design is greatly simplified because the PCM56 is a complete D/A converter requiring no external reference or output op amp.

A sample/hold (S/H) amplifier, or "deglitcher" is required at the output of the D/A for both the left and right channel, as shown in Figure 9. The S/H amplifier for the left channel is composed of A_1, SW_1, and associated circuitry. A_1 is used as an integrator to hold the analog voltage in C_1. Since the source and drain of the FET switch operate at a virtual ground when "C" and "B" are connected in the sample mode, there is no increase in distortion caused by the modulation effect of R_{ON} by the audio signal.

Figure 10 shows the deglitcher controls for both left and right channels which are produced by timing control logic. A delay of 1.5µs ($t\omega$) is provided to allow the output of the PCM56 to settle within a small error band around its final value before connecting it to the channel output. Due to the fast settling time of the PCM56 it is possible to minimize the delay between the left- and right-channel outputs when using a single D/A converter for both channels. This is important because the right- and left-channel data are recorded in-phase and the use of the slower D/A converter would result in significant phase error at higher frequencies.

The obvious solution to the phase shift problem in a two-channel system would be to use two D/A converters (one per channel) and time the outputs to change simultaneously. Figure 11 shows a block diagram of the final test circuitry used for PCM56. It should be noted that no deglitching circuitry is required on the DAC output to meet specified THD performance. This means that when one PCM56 is used per channel, the need for all the sample/hold and controls circuitry associated with a single DAC (two-channel) design is effectively eliminated. The PCM56 is tested to meet its THD specifications without the need for output deglitching.

A low-pass filter is required after the PCM56 to remove all unwanted frequency components caused by the sampling frequency as well as those resulting from the discrete nature of the D/A output. This filter must have a flat frequency response over the entire audio band (0-20kHz) and a very high attenuation above 20kHz.

Most previous digital audio circuits used a higher order (9-13 pole) analog filter. However, the phase response of an analog filter with these amplitude characteristics is nonlinear and can disturb the pulse-shaped characteristic transients contained in music.

SECOND GENERATION SYSTEMS

One method of avoiding the problems associated with a higher order analog filter would be to use digital filter oversampling techniques. Oversampling by a factor of two would move the sampling frequency (88.2kHz) out to a point where only a simple low-order phase-linear analog filter is required after the deglitcher output to remove unwanted intermodulation products. In a digital compact

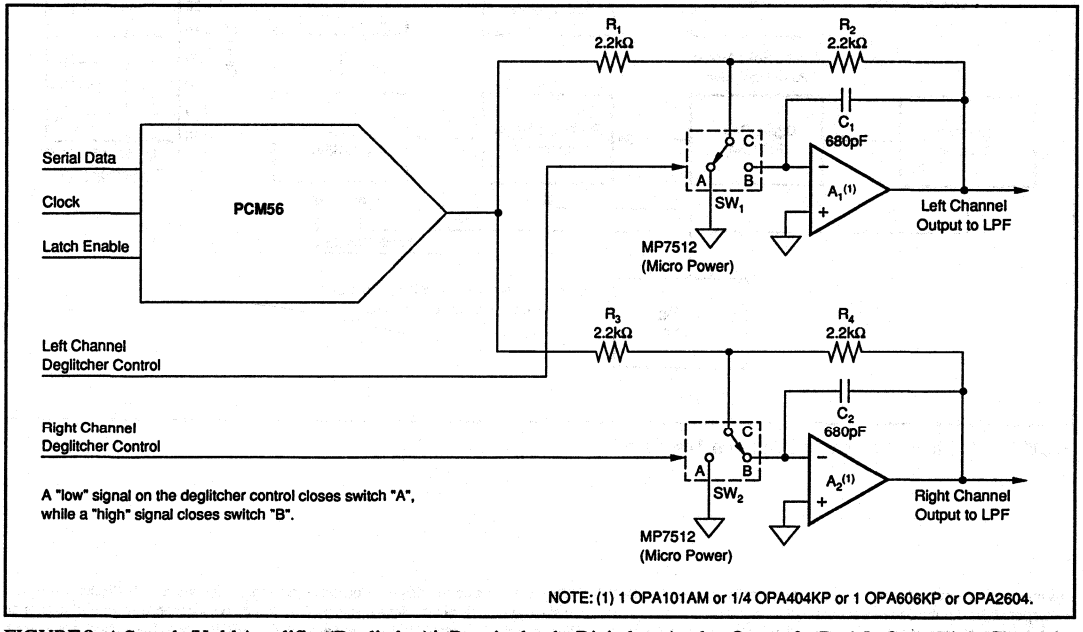


FIGURE 9. A Sample/Hold Amplifier (Deglitcher) is Required at the Digital-to-Analog Output for Both Left and Right Channels.

disc application, various VLSI chips perform the functions of error detection/correction, digital filtering, and formatting of the digital information to provide the clock, latch enable, and serial input to the PCM56. These VLSI chips are available from several sources (Sony, Yamaha, Signetics, etc.) and are specifically optimized for digital audio applications.

Oversampled circuitry requires a very fast D/A converter since the sampling frequency is multiplied by a factor of two or more (for each output channel). A single PCM56 can provide two-channel oversampling at a 4X rate (176.4kHz/channel) and still remain well within the settling time requirements for maintaining specified THD performance. This would reduce the complexities of the analog filter even further from that used in 2X oversampling circuitry.

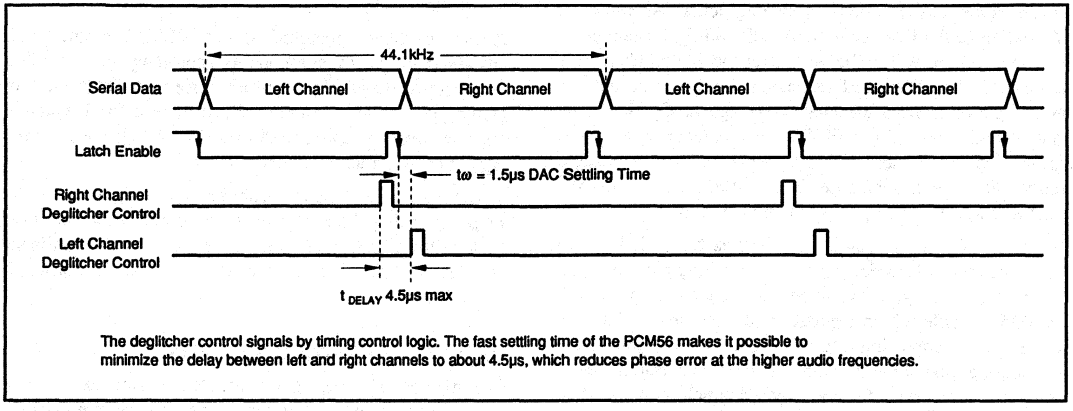


FIGURE 10. Timing Diagram for the Deglitcher Control Signals.

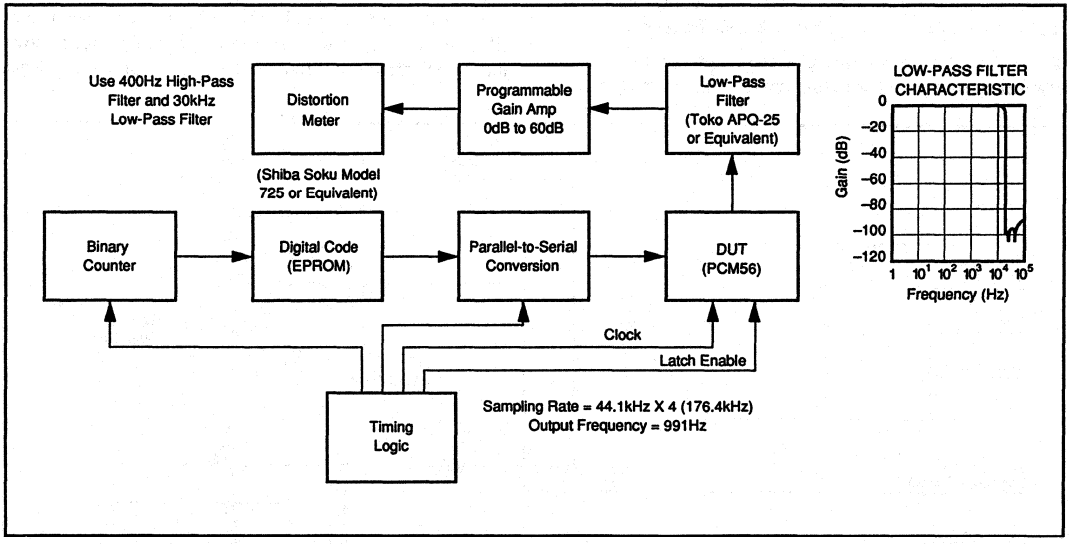


FIGURE 11. Block Diagram of Distortion Test Circuit.

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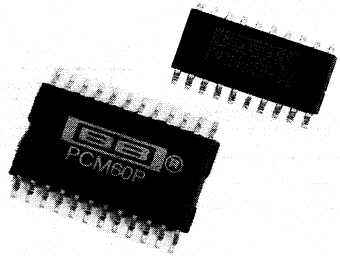


PCM60P
PCM66P

16-Bit CMOS Monolithic Audio DIGITAL-TO-ANALOG CONVERTER

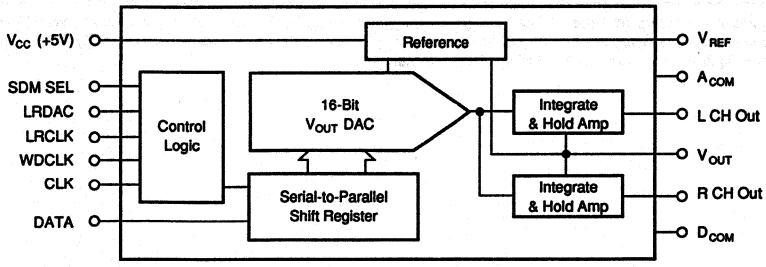
FEATURES

- LOW COST 16-BIT 2-CHANNEL CMOS MONOLITHIC D/A CONVERTER
- SINGLE SUPPLY +5V OPERATION
- 50mW POWER DISSIPATION
- GLITCH-FREE VOLTAGE OUTPUTS
- LOW DISTORTION: –86dB max THD + N
- COMPLETE WITH REFERENCE
- SERIAL INPUT FORMAT
- SINGLE OR DUAL DAC MODE OPERATION
- PLASTIC 20-PIN SOIC PACKAGE (PCM66P)
- PLASTIC 24-PIN SOIC PACKAGE (PCM60P)

DESCRIPTION

The PCM60P/66P is a low cost, dual output 16-bit CMOS digital-to-analog converter. The PCM60P/66P features true glitch-free voltage outputs and requires only a single +5V supply. The PCM60P/66P doesn't require an external reference. Total power dissipation is less than 50mW max. Low maximum Total Harmonic Distortion + Noise (–86dB max; PCM60P-J, PCM66P-J) is 100% tested. Either one or two channel output modes are fully user selectable.

The PCM60P/66P comes in a space-saving 24-pin plastic SOIC package. PCM60P/66P accepts a serial data input format and is compatible with other Burr-Brown PCM products such as the industry standard PCM56P.



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Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL

All specifications at 25°C, and $+V_{CC}$ = +5V unless otherwise noted.

PARAMETER	CONDITIONS	PCM60P/66P AND PCM60P-J/66P-J MIN	TYP	MAX	UNITS
RESOLUTION				16	Bits
DYNAMIC RANGE			96		dB
INPUT					
DIGITAL INPUT			TTL Compatible CMOS		
Logic Family					
Logic Level: V_{IH}	I_{IH} = +40µA max	+2.4		+5.25	V
V_{IL}	I_{IL} = –40µA max	0		0.8	V
Data Format			Serial BTC[1]		
Input Clock Frequency		8.5			MHz
DYNAMIC CHARACTERISTICS					
TOTAL HARMONIC DISTORTION + N[2]					
PCM60P/66P: f = 991Hz (0dB)[3]	f_S = 176.4kHz[4]		–88	–82	dB
f = 991Hz (–20dB)	f_S = 176.4kHz		–68		dB
f = 991Hz (–60dB)	f_S = 176.4kHz		–28		dB
PCM60P-J/66P-J: f = 991Hz (0dB)	f_S = 176.4kHz		–92	–86	dB
f = 991Hz (–20dB)	f_S = 176.4kHz		–68		dB
f = 99lHz (–60db)	f_S = 176.4kHz		–28		dB
CHANNEL SEPARATION		+80	+85		dB
TRANSFER CHARACTERISTICS					
ACCURACY					
Gain Error	V_{OUT} = 2.6		±2	±10	%
Gain Mismatch	Channel to Channel		±1		%
Bipolar Zero Error[5]			±30		mV
Gain Drift	0°C to 70°C		100		ppm/°C
Warm-up Time		1			minute
IDLE CHANNEL SNR[6]	20-20kHz with A-weighted filter		±90		dB
OUTPUT					
ANALOG OUTPUT					
Output Range			2.6		Vp-p
Output Impedance			2		Ω
Short Circuit Duration	To Be Determined				
Settling Time	Suffieicnt to Meet 176.4kHz THD + N Specs				
Glitch Energy	Meets All THD + N Specs Without External Output Deglitching				
POWER SUPPLY REQUIREMENTS					
$+V_{CC}$ Supply Voltage		+4.75	+5	+5.25	V
Supply Current			+9.5		mA
Power Dissipation	V_{CC} = +5V			50	mW
TEMPERATURE RANGE					
Specification		0		+70	°C
Operating		–30		+70	°C
Storage		–60		+100	°C

NOTES: (1) Binary Two's Complement coding. (2) Ratio of (Distortion$_{RMS}$ + Noise$_{RMS}$) / Signal$_{RMS}$. (3) D/A converter output frequency/signal level (on both left and right channels). (4) D/A converter sample frequency (4 x 44.1kHz; 4 times oversampling per channel). (5) Offset error at bipolar zero. (6) Ratio of output at BPZ (Bipolar Zero) to the full scale range using 20kHz low pass filter in addition to an A-weighted filter.

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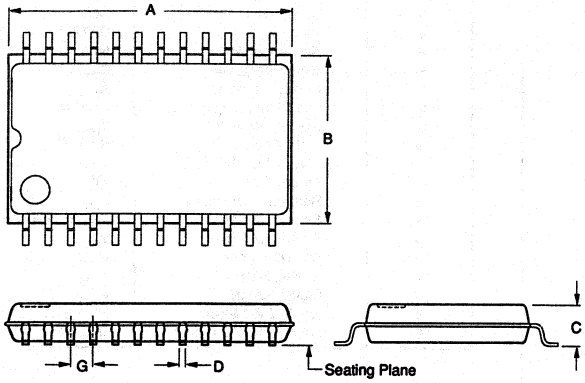
MECHANICAL

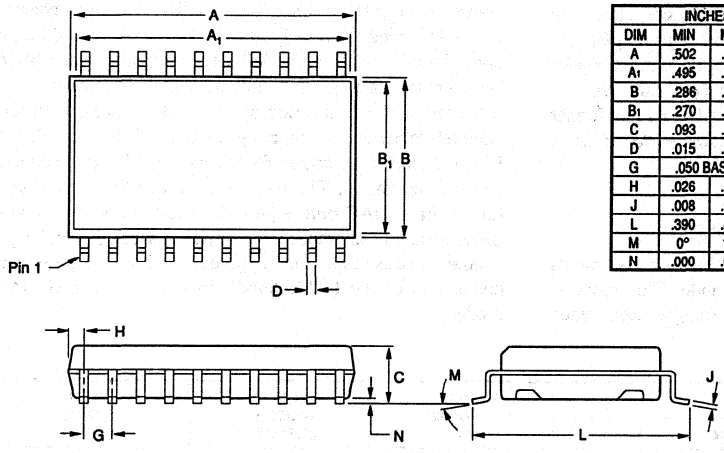
P Package — 24-Pin SOIC
PCM60P



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.614	.630	15.60	16.00
A1	.610	TYP	15.5	TYP
B	.328	.346	8.33	8.80
B1	.331	TYP	8.4	TYP
C	—	.098	—	2.50
D	.012	.020	0.30	0.50
G	.046	.054	1.17	1.37
H	.075	.115	1.91	2.92
J	.0039	.010	0.1	0.26
L	.453	.476	11.5	12.1
M	0°	TYP	0°	TYP
N	.0039		0.10	

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

P Package — 20-Pin Plastic SOIC
PCM66P



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.502	.518	12.75	13.16
A1	.495	.518	12.57	13.16
B	.286	.302	7.26	7.67
B1	.270	.285	6.86	7.24
C	.093	.108	2.36	2.74
D	.015	.019	0.38	0.48
G	.050 BASIC		1.27 BASIC	
H	.026	.034	0.66	0.86
J	.008	.012	0.20	0.30
L	.390	.422	9.91	10.72
M	0°	10°	0°	10°
N	.000	.012	0.00	0.30

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

ABSOLUTE MAXIMUM RATINGS

DC Supply Voltage	±10V
Input Voltage Range	–3V to +5.25V
Power Dissipation	50mW
Operating Temperature	–30°C to +70°C
Storage Temperature	–60°C to +100°C
Lead Temperature (soldering, 10s)	+300°C

ORDERING INFORMATION

PCM60P/PCM66P -X

Basic Model Number
P: Plastic
Performance Grade Code

PCM60P PIN ASSIGNMENTS

PIN	DESCRIPTION	MNEMONIC
1	Left/Right Clock	LRCLK
2	Word Clock	WDCLK
3	Clock Input	CLK
4	Data Input	DATA
5	No Connection	NC
6	No Connection	NC
7	Digital Common	D_{COM}
8	Analog Common	A_{COM}
9	No Connection	NC
10	Left Channel V_{OUT}	L CH Out
11	Output Common	V_{COM}
12	Right Channel V_{out}	R CH Out
13	$+V_{CC}$ Analog Supply	$+V_{CC}$
14	$+V_{CC}$ Analog Supply	$+V_{CC}$
15	Reference Decouple	C_{REF}
16	No Connection	NC
17	V_{REF} Sense	V_{REF} SENSE
18	Voltage Reference	V_{REF}
19	$+V_{CC}$ Analog Supply	$+V_{CC}$
20	$+V_{CC}$ Analog Supply	$+V_{CC}$
21	$+V_{CC}$ Digital Supply	$+V_{CC}$
22	No Connection	NC
23	Single DAC Mode	SDM SEL
24	Left/Right DAC Select	LRDAC

PCM66P PIN ASSIGNMENTS

PIN	DESCRIPTION	MNEMONIC
1	Left/Right Clock	LRCLK
2	Word Clock	WDCLK
3	Clock Input	CLK
4	Data Input	DATA
5	No Connection	NC
6	Digital Common	D_{COM}
7	Analog Common	A_{COM}
8	Left Channel V_{OUT}	L CH Out
9	Output Common	V_{COM}
10	Right Channel V_{OUT}	R CH Out
11	Analog Supply	$+V_{CC}$
12	Analog Supply	$+V_{CC}$
13	Reference Decouple	C_{REF}
14	Reference Sense	V_{REF} SENSE
15	Reference Output	V_{REF}
16	Analog Supply	$+V_{CC}$
17	Analog Supply	$+V_{CC}$
18	Digital Supply	$+V_{CC}$
19	Single DAC Mode	SDM SEL
20	Left/Right DAC Select	LRDAC

THEORY OF OPERATION

The PCM60P/66P is a dual output, 16-bit CMOS digital-to-analog audio converter. The PCM60P/66P, complete with internal reference, has two glitch-free voltage outputs and requires only a single +5V power supply. Output modes using either one or two channels per DAC are user selectable. The PCM60P/66P accepts a serial data input format that is compatible with other Burr-Brown PCM products such as the industry standard PCM56P.

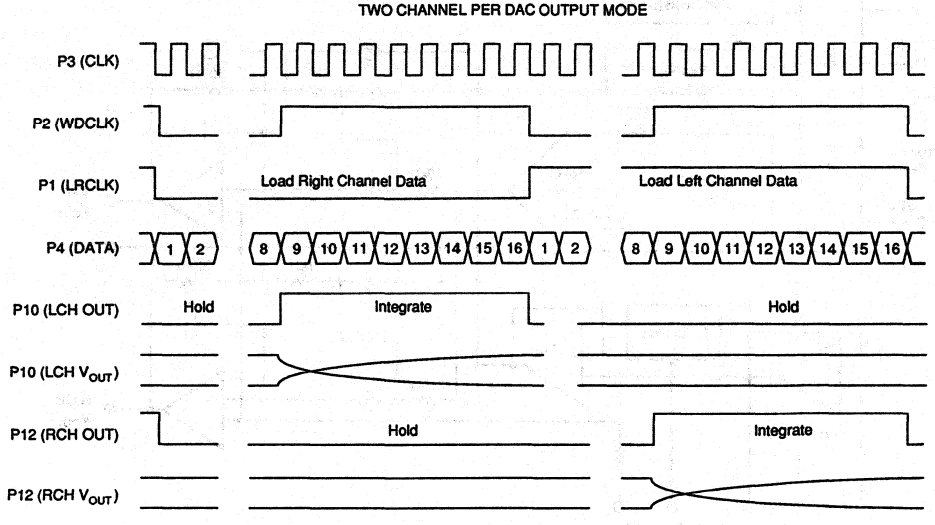
ONE DAC TWO-CHANNEL OPERATION

Normally, the PCM60P/66P is operated with a continuous clock input in a two-channel output mode. This mode is selected when SDM SEL is held low (single DAC mode select). Refer to the truth table shown by Table I for exact control logic relationships. Data for left and right channel output is loaded alternately into the PCM60P/66P while the control logic switches the left and right output amplifiers between the appropriate integrate and hold modes. Data word latching is controlled by WDCLK (word clock) and channel selection is made by LRCLK (left/right clock). Figure 1 shows the timing for the single DAC two-channel mode of operation. The block diagram in Figure 2 shows how a single DAC output provides switched output to both integrate and hold amplifiers. Output between left and right channels in this mode is not in phase. See Figure 3 for proper connection of the PCM60P/66P in the two-channel DAC mode.

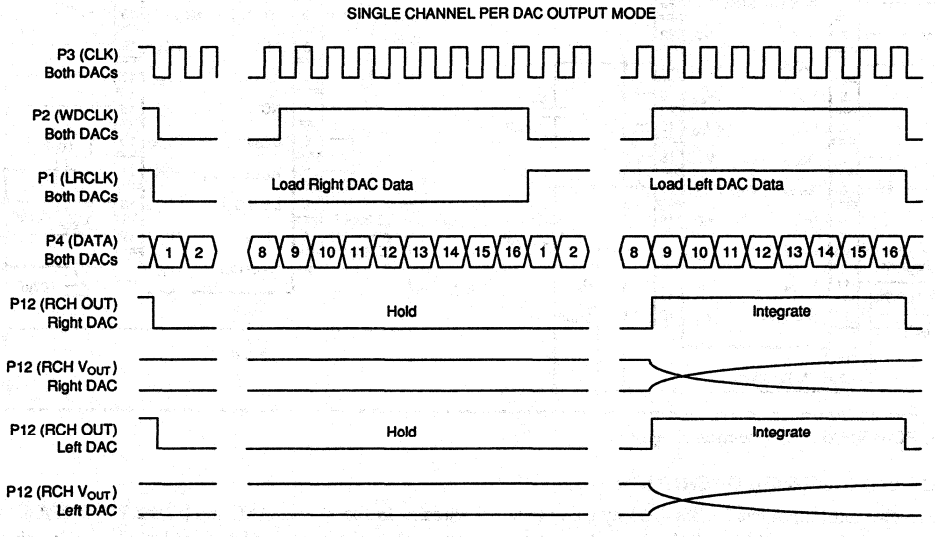
PIN FUNCTIONS				SERIAL DATA WORD INPUT	LEFT CHANNEL OUTPUT	RIGHT CHANNEL OUTPUT
SDM SEL	LRDAC	LRCLCK	WDCLK			
0	X	0	0	Right	Hold	Hold
0	X	0	1	Right	Integrate	Hold
0	X	1	0	Left	Hold	Hold
0	X	1	1	Left	Hold	Integrate
1	0	0	0	Inhibited	V_{COM}	Hold
1	0	0	1	Inhibited	V_{COM}	Hold
1	0	1	0	Left	V_{COM}	Integrate
1	0	1	1	Left	V_{COM}	Integrate
1	1	0	0	Right	V_{COM}	Hold
1	1	0	1	Right	V_{COM}	Hold
1	1	1	0	Inhibited	V_{COM}	Integrate
1	1	1	1	Inhibited	V_{COM}	Integrate

NOTE: Positive edge of CLK (P3) latches LRCLK (P1), WDCLK (P2), and DATA (P4).

TABLE I. PCM60P/66P Logic Truth Table.



NOTES: Single DAC Mode Select = 0; L/R DAC Select = X; WDCLK = 50% duty cycle; Serial Data is read in MSB first with BTC coding (MSB = Bit 1).



NOTES: Single DAC Mode Select = 1; L/R DAC Select = 0 (Left DAC) or 1 (Right DAC).

FIGURE 1. PCM60P/66P Timing Diagram.

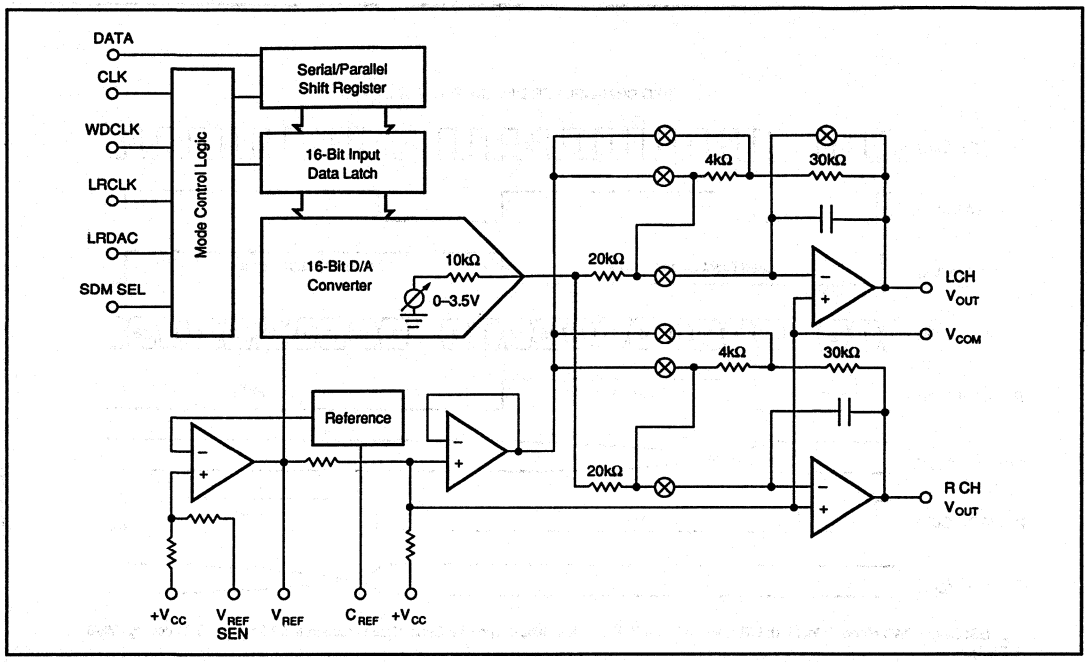


FIGURE 2. PCM60P/66P Block Diagram.

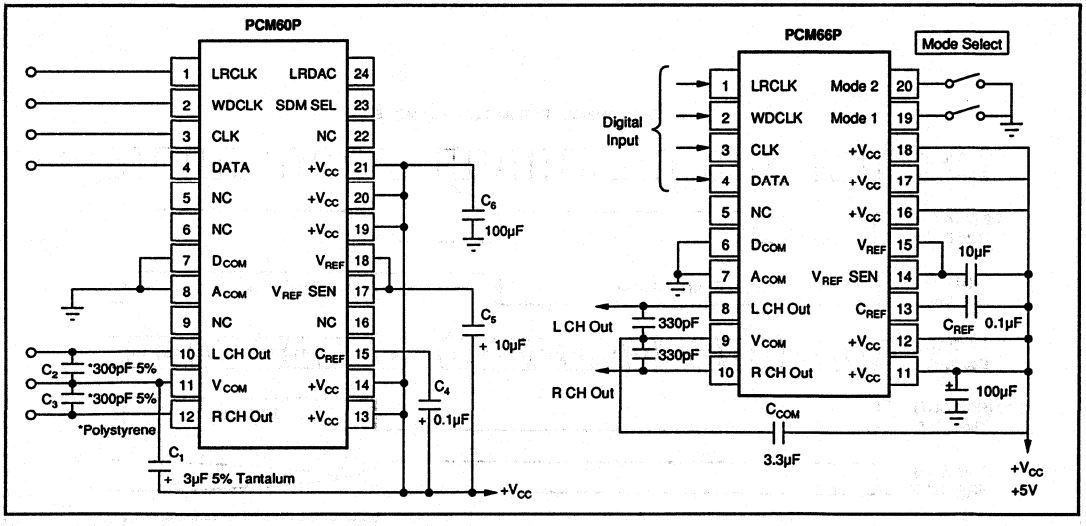


FIGURE 3. PCM60P/66P Connection Diagram.

TWO DAC TWO-CHANNEL OPERATION

In phase, two-channel output can be obtained by using two PCM60P/66Ps and choosing the single DAC mode (setting SDM SEL high). With the use of a high or low input level on LRDAC (P left/right DAC select), each DAC can have its right channel output dedicated to either left or right data input with no additional input signals being required to latch the appropriate data from an alternating L/R data word input stream. In the single DAC mode, the PCM60P/66P's left channel output is disabled and held at $+V_{COM}$. In this mode both DACs share common inputs for DATA, CLK, WDCLK, and LRCLK. Otherwise circuit connection is the same as the two-channel DAC mode, with the exception of LRDAC whose level selects whether the single DAC will output dedicated left or right channel data.

INTEGRATE AND HOLD OUTPUT AMPLIFIERS

The PCM60P/66P incorporates integrate and hold amplifiers on each output channel. This allows a single, very fast DAC to feed both amplifiers and reduce circuit complexity. It also serves to block the output glitch from the DAC to the individual channel outputs and effectively makes the PCM60P/66P outputs "glitch-free." The PCM60P/66P is a single +5V supply device with a voltage output swing of 2.8Vp-p. The outputs swing asymmetrically around V_{COM} ($+V_{CC} - 2.33V$). See Table II for exact input/output relationships. Since true CMOS amplifiers are used on the PCM60P/66P, the load resistance on the outputs should not be less than 100kΩ and the capacitive loads should not exceed 100pF. For maximum low-distortion performance, output buffer amplifiers should be considered.

DIGITAL INPUT	ANALOG OUTPUT	
Binary Two's Complement (Hex)	DAC Output (V)	Voltage (V) V_{OUT} Mode
7FFF	+FS	+3.5629443
0000	BPZ	+2.1629871
8000	–FS	+0.7630299
2E5B	V_{COM}	+2.6700000

TABLE II. PCM60P/66P Input/Output Relationships.

DISCUSSION OF SPECIFICATIONS

TOTAL HARMONIC DISTORTION + NOISE

The key specification for the PCM60P/66P is total harmonic distortion plus noise. Digital data words are read into the PCM60P/66P at four times the standard audio sampling frequency of 44.1kHz or 176.4kHz for each channel, such that a sine wave output of 991Hz is realized. For production testing, the output of the DAC goes to a programmable gain amplifier to provide gain at lower signal output test levels and then through a 20kHz low pass filter before being fed into an analog type distortion analyzer. Figure 4 shows a block diagram of the production THD + N test setup.

In terms of signal measurement, THD + N is the ratio of $Distortion_{RMS} + Noise_{RMS}/Signal_{RMS}$ expressed in dB. For the PCM60P/66P, THD + N is 100% tested at three different output levels using the test setup shown in Figure 4. It is significant to note that this circuit does not include any output deglitching circuitry. This means the PCM60P/66P meets even its –60dB THD + N specification without use of external deglitchers.

ABSOLUTE LINEARITY

Even though absolute integral and differential linearity specs are not given for the PCM60P/66P, the extremely low THD + N performance is typically indicative of 14-bit to 15-bit integral linearity in the DAC depending on the grade specified. The relationship between THD + N and linearity, however, is not such that an absolute linearity specification for every individual output code can be guaranteed.

IDLE CHANNEL SNR

Another appropriate spec for a digital audio converter is idle channel signal-to-noise ratio (idle channel SNR). This is the ratio of the noise on either DAC output at bipolar zero in relation to the full scale range of the DAC. The output of the DAC is band limited from 20Hz to 20kHz and an A-weighted filter is applied to make this measurement.

OFFSET, GAIN, AND TEMPERATURE DRIFT

The PCM60P/66P is specified for other important parameters such as channel separation and gain mismatch between output channels. And although the PCM60P/66P is primarily meant for use in dynamic applications, typical specs are also given for more traditional DC parameters such as gain error, bipolar zero offset error, and temperature gain drift.

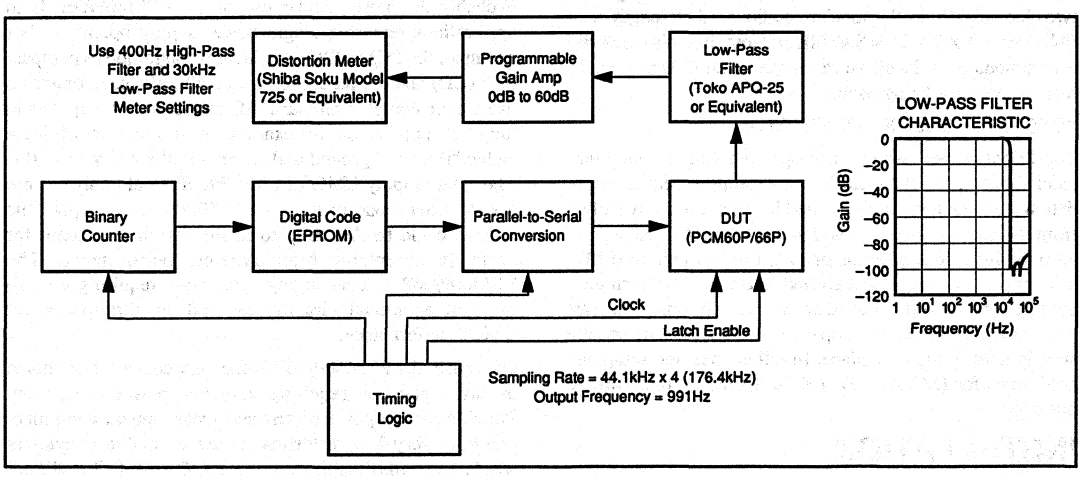


FIGURE 4. THD + N Test Setup Diagram.

TIMING CONSIDERATIONS

The data format of the PCM60P/66P is binary two's complement (BTC) with the most significant bit (MSB) being first in the serial input bit stream. Table II describes the exact input data to voltage output coding relationship. Any number of bits can precede the 16 bits to be loaded, as only the last 16 will be transferred to the parallel DAC register on the first positive edge of CLK (clock input) after WDCLK (word clock) has gone low. All inputs to the PCM60P/66P are TTL level compatible.

WDCLK DUTY CYCLE

WDCLK is the input signal that controls when data is loaded and how long each output is in the integrate mode. It is therefore recommended that a 50% (high) duty cycle be maintained on WDCLK. This will ensure that each output will have enough time to reach its final output value, and that the output level of each channel will be within the gain mismatch specification. Refer to Figure 1 for exact timing relationships of WDCLK to CLK and LRCLK and the outputs of the PCM60P/66P. The WDCLK can be high longer than 50%, as long as setup and hold times shown in Figure 5 are observed and the time high is roughly equivalent for both left and right channels.

SETUP AND HOLD TIMES

The individual serial data bit shifts, the serial to parallel data transfer, and left/right control are triggered on positive CLK edges. The setup time required for DATA, WDCLK, and LRCLK to be latched by the next positive going CLK is 15ns minimum. A minimum hold time of 15ns is also required after the positive going CLK edge for each data bit to be shifted into the serial input register. Refer to Figure 5 for the timing relationship of these signals.

MAXIMUM CLOCK RATE

The 100% tested maximum clock rate of 8.47MHz for the PCM60P/66P is derived by multiplying the standard audio sample rate of 44.1kHz times eight (4X oversampling times two channels) times the standard audio word bit length of 24 (44.1kHz X 4 X 2 X 24 = 8.47MHz). Note that this clock rate accommodates a 24-bit word length, even though only 16 bits are actually being used.

"STOPPED-CLOCK" OPERATION

The PCM60P/66P is normally operated with a continuous clock input signal. If the clock is to be stopped between input data words, the last 16 bits shifted in are not actually shifted from the serial register to the latched parallel DAC register until the first clock after the one used to input bit 16 (LSB). This means the data is not shifted into the DHC latch until the start of the next 16-bit data word input, unless at least one additional clock accompanies the 16 used to serially shift in data in the first place. In either case, the setup and hold times for DATA, WDCLK, and LRCLK must still be observed.

INSTALLATION

The PCM60P/66P only requires a single +5V supply. The +5V supply, however, is used in deriving the internal reference. It is therefore very important that this supply be as "clean" as possible to reduce coupling of supply noise to the outputs. If a good analog supply is available at greater than +5V, a zener diode can be used to obtain a stable +5V supply. A 100µF decoupling capacitor as shown in Figure 3 should be used regardless of how good the +5V supply is to maximize power supply rejection. All grounds should be connected to the analog ground plane as close to the PCM60P/66P as possible.

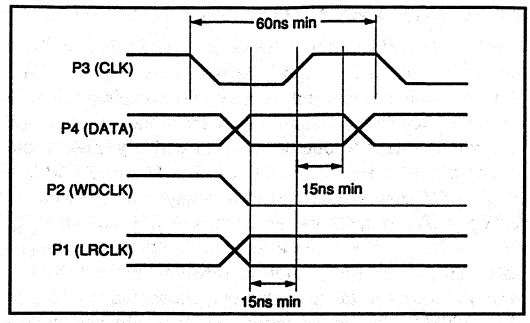


FIGURE 5. PCM60P/66P Setup and Hold Timing Diagram.

FILTER CAPACITOR REQUIREMENTS

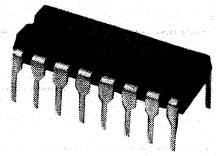
As shown in Figure 3, C_{REF} and V_{REF} SENSE should have decoupling capacitors of 0.1µF (C_4) and 10µF (C_5) to $+V_{CC}$ respectively with no special tolerance being required. To maximize channel separation between left and right channels, 5% 300pF capacitors (C_2 and C_3) between V_{COM} and left and right channel outputs are required in addition to a 5% 3µF capacitor (C_1) between V_{COM} and +5V. The ratio of 10k to 1 is the important factor here for proper circuit operation. Placement of all capacitors should be as close to the appropriate pins of the PCM60P/66P as possible to reduce noise pickup from surrounding circuitry.

APPLICATIONS

Probably the most popular use of the PCM60P/66P is in applications requiring single power supply operation. For example, the PCM60P/66P is ideal for automotive compact disk (CD) and digital audio tape (DAT) playback units. To use a more complex bipolar DAC requiring ±5V supplies in the +12V application, for example, would require driving a stable "floating" ground and regulating the +12V to +10V. The single supply CMOS PCM60P/66P would only require a +5V zener diode to regulate its 50mW max supply. The outputs could be AC coupled to the rest of the circuit for perfectly acceptable high dynamic performance. The PCM60P/66P is ideal in any application requiring a minimum of additional circuitry as well as ultra-low-power CMOS performance.

Of course, the PCM60P/66P is the D/A converter of choice in any application requiring very low power dissipation. Portable battery powered test and measurement equipment requiring very low distortion digital to analog converters would be an ideal application for the CMOS PCM60P/66P with its 50mW max power dissipation.

BURR-BROWN®



PCM61P

See Also PCM1700P
Dual 18-Bit D/A Converter
Pg. 9.2.227

Serial Input 18-Bit Monolithic Audio DIGITAL-TO-ANALOG CONVERTER

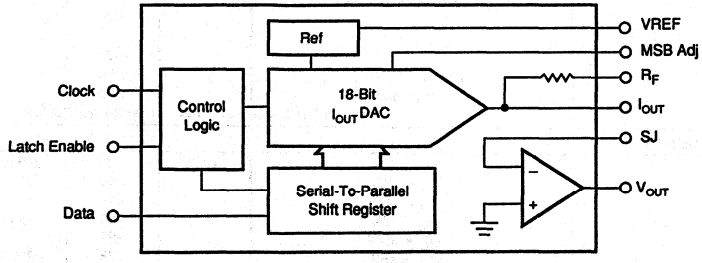
FEATURES

- 18-BIT MONOLITHIC AUDIO D/A CONVERTER
- LOW MAX THD + N: –92dB Without External Adjust
- 100% PIN COMPATIBLE WITH INDUSTRY STD 16-BIT PCM56P
- GLITCH FREE OUTPUT OF ±3V OR ±1mA
- CAPABLE OF 8X OVERSAMPLING RATE IN V_{OUT} MODE
- COMPLETE WITH INTERNAL REFERENCE AND OUTPUT OP AMP
- RELIABLE PLASTIC 16-PIN DIP PACKAGE

DESCRIPTION

The PCM61P is an 18-bit totally pin compatible performance replacement for the popular 16-bit PCM56P. With the addition of two extra bits, lower max THD + N (–92dB; PCM61P-K) can be achieved in audio applications already using the PCM56P. The PCM61P is complete with internal reference and output op amp and requires no external parts to function as an 18-bit DAC. The PCM61P is capable of an 8-times oversampling rate (single channel) and meets all of its specifications without an external output deglitcher.

The PCM61P comes in a small, reliable 16-pin plastic DIP package that has passed operating life tests under simultaneous high temperature, high humidity and high pressure testing.



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Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (602) 746-7270

SPECIFICATIONS

ELECTRICAL

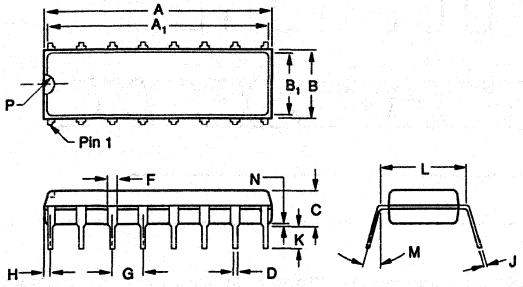
All specifications at 25°C, and $+V_{CC}$ = +5V unless otherwise noted.

PARAMETER	CONDITIONS	PCM61P/P-J/P-K MIN	TYP	MAX	UNITS
RESOLUTION				18	Bits
DYNAMIC RANGE			108		dB
INPUT					
DIGITAL INPUT					
Logic Family			TTL/CMOS Compatible		
Logic Level: V_{IH}		+2		$+V_{CC}$	V
V_{IL}		0		+0.8	V
I_{IH}	V_{IH} = +2.7V			+1	µA
I_{IL}	V_{IL} = +0.4V			–50	µA
Data Format		Serial BTC[1]			
Input Clock Frequency				16.9	MHz
DYNAMIC CHARACTERISTICS					
Total Harmonic Distortion + N[2]	Without MSB Adjustments				
PCM61P					
f = 991Hz (0dB)[3]	f_S = 176.4kHz[4]		–88	–82	dB
f = 991Hz (–20dB)	f_S = 176.4kHz		–74	–68	dB
f = 991Hz (–60dB)	f_S = 176.4kHz		–34	–28	dB
PCM61P-J					
f = 991Hz (0dB)	f_S = 176.4kHz		–94	–88	dB
f = 991Hz (–20dB)	f_S = 176.4kHz		–76	–74	dB
f = 991Hz (–60dB)	f_S = 176.4kHz		–36	–34	dB
PCM61P-K					
f = 991Hz (0dB)	f_S = 176.4kHz		–98	–92	dB
f = 991Hz (–20dB)	f_S = 176.4kHz		–80	–74	dB
f = 991Hz (–60dB)	f_S = 176.4kHz		–40	–34	dB
IDLE CHANNEL SNR	20Hz to 20kHz at BPZ[5]		112		dB
TRANSFER CHARACTERISTICS					
ACCURACY					
Gain Error			±2		%
Bipolar Zero Error			±30		mV
Differential Linearity Error			±0.001		%
Total Drift[6]	0°C to 70°C		±25		ppm of FSR/°C
Bipolar Zero Drift	0°C to 70°C		±4		ppm of FSR/°C
Warm-up Time		1			Minute
MONOTONICITY			16		Bits
ANALOG OUTPUT					
Voltage: Output Range			±3		V
Output Current		±8			mA
Output Impedance			0.1		Ω
Current: Output Range	±30%		±1		mA
Output Impedance	±30%		1.2		kΩ
SETTLING TIME	To ±0.006% of FSR				
Voltage: 6V Step			1.5		µs
1 LSB			1.0		µs
Slew Rate			12		V/µs
Current: 1mA Step	10Ω to 100Ω Load		250		ns
1mA Step	1kΩ Load		350		ns
Glitch Energy	Meets all THD + N specs without external deglitching				
POWER SUPPLY REQUIREMENTS[7]					
$\pm V_{CC}$ Supply Voltage		±4.75	±5	±13.2	V
Supply Current: $+I_{CC}$	$+V_{CC}$ = +5V		+10	+17	mA
$+I_{CC}$	$+V_{CC}$ = +12V		+12		mA
$-I_{CC}$	$-V_{CC}$ = –5V		–25	–35	mA
$-I_{CC}$	$-V_{CC}$ = –12V		–27		mA
Power Dissipation	$\pm V_{CC}$ = ±5V		175	260	mW
	$\pm V_{CC}$ = ±12V		475		mW
TEMPERATURE RANGE					
Specification		0		+70	°C
Operating		–30		+70	°C
Storage		–60		+100	°C

NOTES: (1) Binary Two's Complement coding. (2) Ratio of (Distortion$_{RMS}$ + Noise$_{RMS}$)/Signal$_{RMS}$. (3) D/A converter output frequency/signal level. (4) D/A converter sample frequency (4 x 44.1kHz; 4 times oversampling). (5) Bipolar zero, using A-weighted filter. (6) This is the combined drift error due to gain, offset, and linearity over temperature. (7) All positive and all negative supply pins must be tied together respectively.

MECHANICAL

P Package — 16-Pin Plastic DIP



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.740	.800	18.80	20.32
A1	.725	.785	18.42	19.94
B	.230	.290	5.85	7.38
B1	.200	.250	5.09	6.36
C	.120	.200	3.05	5.09
D	.015	.023	0.38	0.59
F	.030	.070	0.76	1.78
G	.100 BASIC		2.54 BASIC	
H	0.20	.050	0.51	1.27
J	.008	.015	0.20	0.38
K	.070	.150	1.78	3.82
L	.300 BASIC		7.63 BASIC	
M	0°	15°	0°	15°
N	.010	.030	0.25	0.76
P	.025	.050	0.64	1.27

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

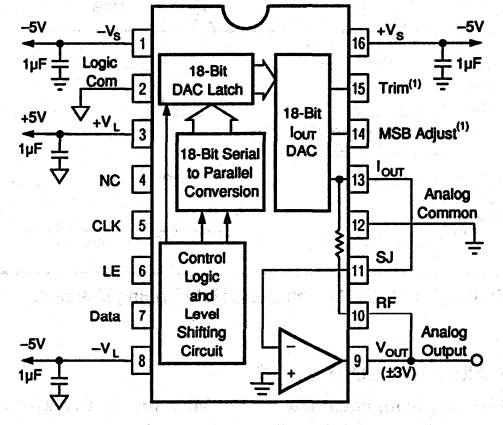
PIN ASSIGNMENTS

1	$-V_S$	Analog Negative Supply
2	LOG COM	Logic Common
3	$+V_L$	Logic Positive Supply
4	NC	No Connection
5	CLK	Clock Input
6	LE	Latch Enable Input
7	DATA	Serial Data Input
8	$-V_L$	Logic Negative Supply
9	V_{OUT}	Voltage Output
10	RF	Feedback Resistance
11	SJ	Summing Junction
12	ANA COM	Analog Common
13	I_{OUT}	Current Output
14	MSB ADJ	MSB Adjustment Terminal
15	TRIM	MSB Trim-pot Terminal
16	$+V_S$	Analog Positive Supply

ABSOLUTE MAXIMUM RATINGS

DC Supply Voltages	±16VDC
Input Logic Voltage	−1V to V_S/$+V_L$
Power Dissipation	850mW
Operating Temperature Range	−25°C to +70°C
Storage Temperature Range	−60°C to +100°C
Lead Temperature (soldering, 10s)	+300°C

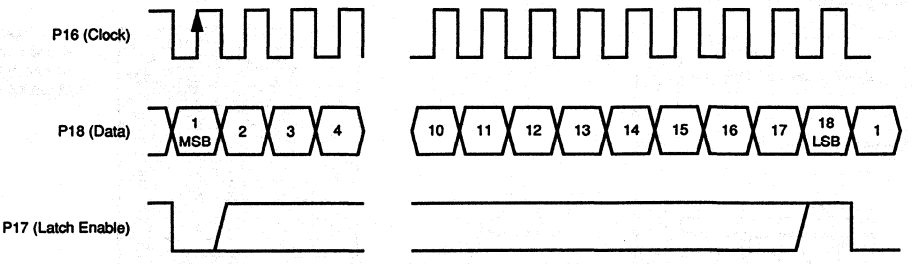
CONNECTION DIAGRAM



NOTE: (1) MSB error (Bipolar Zero differential linearity error) can be adjusted to zero using the external circuit shown in Figure 4.

DIGITAL INPUT	ANALOG OUTPUT		
Binary Two's Complement (BTC)	DAC Output	Voltage (V) V_{OUT} Mode	Current (mA) I_{OUT} Mode
1FFFF Hex	+FS	−0.99999237	+2.99997711
00000 Hex	BPZ	0.00000000	0.00000000
3FFFF Hex	BPZ − 1LSB	+0.00000763	−0.00002289
20000 Hex	−FS	+1.00000000	−3.00000000

TABLE I. PCM61P Input/Output Relationships.



NOTES: (1) If clock is stopped between input of 18-bit data words, latch enable (LE) must remain low until after the first clock of the next 18-bit data word stream. (2) Data format is binary two's complement (BTC). Individual data bits are clocked in on the corresponding positive clock edge. (3) Latch enable (LE) must remain low at least one clock cycle after going negative. (4) Latch enable (LE) must be high for at least one clock cycle before going negative.

FIGURE 2. PCM61P Timing Diagram.

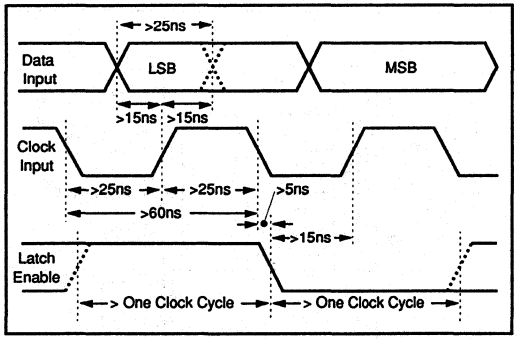


FIGURE 3. PCM61P Setup and Hold Timing Diagram.

MAXIMUM CLOCK RATE

The maximum clock rate of 16.9MHz for the PCM61P is derived by multiplying the standard audio sample rate of 44.1kHz times sixteen (16X oversampling) times the standard audio word bit length of 24 (44.1kHz x 16 x 24 = 16.9MHz). Note that this clock rate accommodates a 24-bit word length, even though only 18 bits are actually being used.

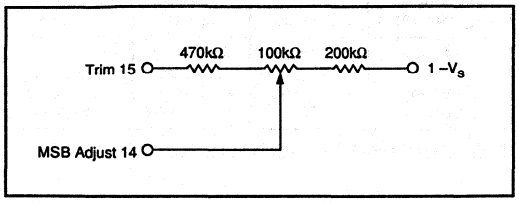


FIGURE 4. MSB Adjust Circuit.

MSB ERROR ADJUSTMENT PROCEDURE (OPTIONAL)

The MSB error of the PCM61P can be adjusted to make the differential linearity error (DLE) at BPZ essentially zero. This is important when the signal output levels are very low, because zero crossing noise (DLE at BPZ) becomes very significant when compared to the small code changes occurring in the LSB portion of the converter.

To statically adjust DLE at BPZ, refer to the circuit shown in Figure 4 or the PCM61P connection diagram.

Differential linearity error at bipolar zero and THD are guaranteed to meet data sheet specifications without any external adjustment. However, a provision has been made for an optional adjustment of the MSB linearity point, which makes it possible to eliminate DLE error at BPZ. Two procedures are given to allow either static or dynamic adjustment. The dynamic procedure is preferred because of the difficulty associated with the static method (accurately measuring 16-bit LSB steps).

After allowing ample warm-up time (5-10 minutes) to assure stable operation of the PCM61P, select input code 3FFFF hexadecimal (all bits on except the MSB). Measure the output voltage using a 6-1/2 digit voltmeter and record it. Change the digital input code to 00000 hexadecimal (all bits off except the MSB). Adjust the 100kΩ potentiometer to make the output read 22.9μV more than the voltage reading of the previous code (a 1LSB step = 22.9μV). A much simpler method is to dynamically adjust the DLE at BPZ. Assuming the device has been installed in a digital audio application circuit, send the appropriate digital input to produce a –60dB level sinusoidal output, then adjust the 100kΩ potentiometer until a minimum level of distortion is observed.

BURR-BROWN®

PCM63P

Colinear™ 20-Bit Monolithic Audio DIGITAL-TO-ANALOG CONVERTER

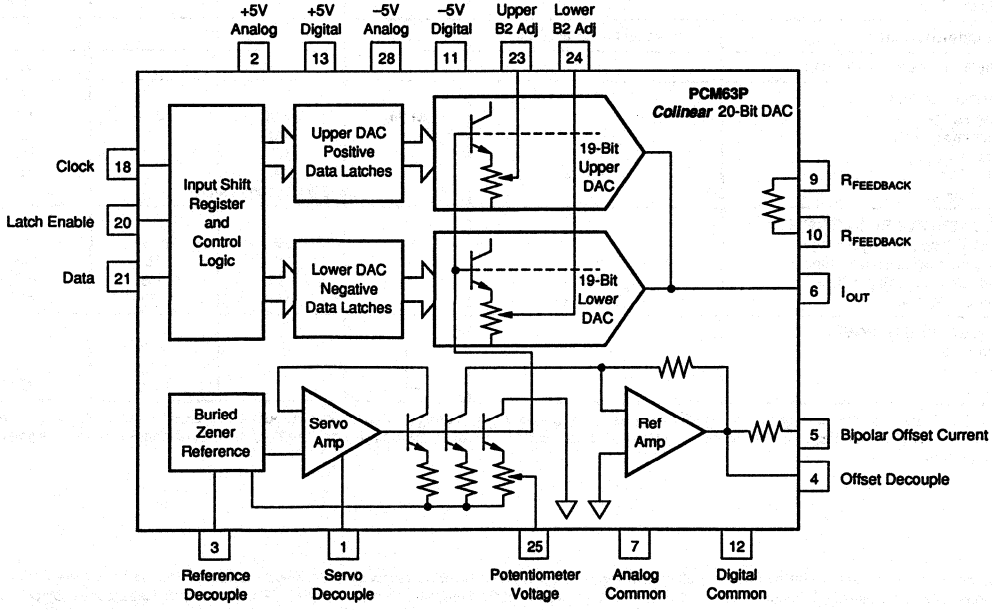
FEATURES

- ***COLINEAR* 20-BIT AUDIO DAC**
- **NEAR-IDEAL LOW LEVEL OPERATION**
- **GLITCH-FREE OUTPUT**
- **ULTRA LOW –96dB max THD + N (Without External Adjustment)**
- **116dB SNR min (A-Weight Method)**
- **INDUSTRY STD SERIAL INPUT FORMAT**
- **FAST (200ns) CURRENT OUTPUT (±2mA; ±2% max)**
- **CAPABLE OF 16x OVERSAMPLING**
- **COMPLETE WITH REFERENCE**

DESCRIPTION

The PCM63P is a precision 20-bit digital-to-analog converter with ultra-low distortion (–96dB max with a full scale output; PCM63P-K). Incorporated into the PCM63P is a unique ***Colinear*** dual-DAC per channel architecture that eliminates unwanted glitches and other nonlinearities around bipolar zero. The PCM63P also features a very low noise (116dB max SNR; A-weighted method) and fast settling current output (200ns typ, 2mA step) which is capable of 16-times oversampling rates.

Applications include very low distortion frequency synthesis and high-end consumer and professional digital audio applications.



Colinear™, Burr-Brown Corp.

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Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL

All specifications at 25°C and $\pm V_A$ and $\pm V_D$ = ±5V, unless otherwise noted.

PARAMETER	CONDITIONS	PCM63P, PCM63P-J, PCM63P-K MIN	TYP	MAX	UNITS
RESOLUTION		20			Bits
DYNAMIC RANGE, THD + N at –60dB Referred to Full Scale					
PCM63P		96	100		dB
PCM63P-J		100	104		dB
PCM63P-K		104	108		dB
DIGITAL INPUT					
Logic Family			TTL/CMOS Compatible		
Logic Level: V_{IH}		+2		$+V_D$	V
V_{IL}		0		0.8	V
I_{IH}	V_{IH} = +2.7V			+1	µA
I_{IL}	V_{IL} = +0.4V			–50	µA
Data Format			Serial, MSB First, BTC[1]		
Input Clock Frequency			30	25	MHz
TOTAL HARMONIC DISTORTION + N[2], Without Adjustments					
PCM63P					
f = 991Hz (0dB)[3]	f_S = 352.8kHz[4]		–92	–88	dB
f = 991Hz (–20dB)	f_S = 352.8kHz		–80	–74	dB
f = 991Hz (–60dB)	f_S = 352.8kHz		–40	–36	dB
PCM63P-J					
f = 991Hz (0dB)	f_S = 352.8kHz		–96	–92	dB
f = 991Hz (–20dB)	f_S = 352.8kHz		–82	–76	dB
f = 991Hz (–60dB)	f_S = 352.8kHz		–44	–40	dB
PCM63P-K					
f = 991Hz (0dB)	f_S = 352.8kHz		–100	–96	dB
f = 991Hz (–20dB)	f_S = 352.8kHz		–88	–82	dB
f = 991Hz (–60dB)	f_S = 352.8kHz		–48	–44	dB
ACCURACY					
Level Linearity	at –90dB Signal Level		±0.3	±1	dB
Gain Error			±1	±2	%
Bipolar Zero Error[5]			±10		mV
Gain Drift	0°C to 70°C		25		ppm/°C
Bipolar Zero Drift	0°C to 70°C		4		ppm of FSR/°C
Warm-up Time		1			Minute
IDLE CHANNEL SNR[6]	20Hz to 20kHz at BPZ[7]	+116	+120		dB
POWER SUPPLY REJECTION			+86		dB
ANALOG OUTPUT					
Output Range		±1.96	±2.00	±2.04	mA
Output Impedance			670		Ω
Internal $R_{FEEDBACK}$			1.5		kΩ
Settling Time	2mA Step		200		ns
Glitch Energy			No Glitch Around Zero		
POWER SUPPLY REQUIREMENTS					
$\pm V_A$, $\pm V_D$ Supply Voltage Range		±4.50	±5	±5.50	V
$+I_A$, $+I_D$ Combined Supply Current	$+V_A$, $+V_D$ = +5V		10	15	mA
$-I_A$, $-I_D$ Combined Supply Current	$-V_A$, $-V_D$ = –5V		–35	–45	mA
Power Dissipation	$\pm V_A$, $\pm V_D$ = ±5V		225	300	mW
TEMPERATURE RANGE					
Specification		0		+70	°C
Operating		–40		+85	°C
Storage		–60		+100	°C

NOTES: (1) Binary Two's Complement coding. (2) Ratio of ($Distortion_{RMS}$ + $Noise_{RMS}$) / $Signal_{RMS}$. (3) D/A converter output frequency (signal level). (4) D/A converter sample frequency (8 x 44.1kHz; 8x oversampling). (5) Offset error at bipolar zero. (6) Measured using an OPA27 and 1.5kΩ feedback and an A-weighted filter. (7) Bipolar Zero.

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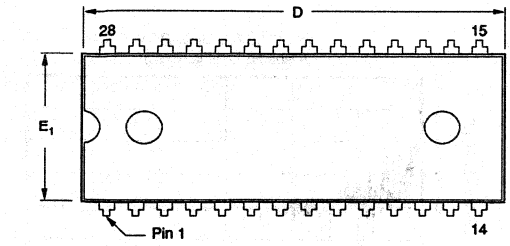
MECHANICAL

P Package — 28-Pin Plastic DIP

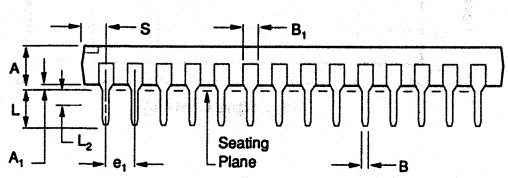


DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A(1)	.169	.200	4.29	5.08
A1 (1)	.015	.070	0.38	1.78
B	.015	.020	0.38	0.51
B1	.015	.055	0.38	1.40
C	.008	.012	0.20	0.30
D(1)	1.380	1.455	35.05	36.96
E	.600	.625	15.24	15.88
E1 (1)	.485	.550	12.32	13.97
e1	.100 BASIC		2.54 BASIC	
eA	.600 BASIC		15.24 BASIC	

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
L	.100	.200	2.54	5.08
L2	.000	.030	0.00	0.76
α	0°	15°	0°	15°
Q1	.020	.070	0.51	1.78
S1	.040	.080	1.02	2.03

(1) Not JEDEC Standard

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.



PIN ASSIGNMENTS

PIN	DESCRIPTION	MNEMONIC
P1	Servo Amp Decoupling Capacitor	CAP
P2	+5V Analog Supply Voltage	$+V_A$
P3	Reference Decoupling Capacitor	CAP
P4	Offset Decoupling Capacitor	CAP
P5	Bipolar Offset Current Output (+2mA)	BPO
P6	DAC Current Output (0 to –4mA)	I_{OUT}
P7	Analog Common Connection	ACOM
P8	No Connection	NC
P9	Feedback Resistor Connection (1.5kΩ)	RF_1
P10	Feedback Resistor Connection (1.5kΩ)	RF_2
P11	–5V Digital Supply Voltage	$-V_D$
P12	Digital Common Connection	DCOM
P13	+5V Digital Voltage Supply	$+V_D$
P14	No Connection	NC
P15	No Connection	NC
P16	No Connection	NC
P17	No Connection	NC
P18	DAC Data Clock Input	CLK
P19	No Connection	NC
P20	DAC Data Latch Enable	LE
P21	DAC Data Input	DATA
P22	No Connection	NC
P23	Optional Upper DAC Bit-2 Adjust (–4.29V)*	UB2 Adj
P24	Optional Lower DAC Bit-2 Adjust (–4.29V)*	LB2 Adj
P25	Bit Adjust Reference Voltage Tap (–3.52V)*	V_{POT}
P26	No Connection	NC
P27	No Connection	NC
P28	–5V Analog Supply Voltage	$-V_A$

*Nominal voltages at these nodes assuming $\pm V_A$; $\pm V_D$ = ±5V.

ABSOLUTE MAXIMUM RATINGS

$+V_A$, $+V_D$ to ACOM/DCOM	0V to +8V
$-V_A$, $-V_D$ to ACOM/DCOM	0V to –8V
$-V_A$, $-V_D$ to $+V_A$, $+V_D$	0V to +16V
ACOM to DCOM	±0.5V
Digital Inputs (pins 18, 20, 21) to DCOM	–1V to $+V_D$
Power Dissipation	500mW
Lead Temperature, (soldering, 10s)	+300°C
Max Junction Temperature	165°C
Thermal Resistance, θ_{JA}	70°C/W

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

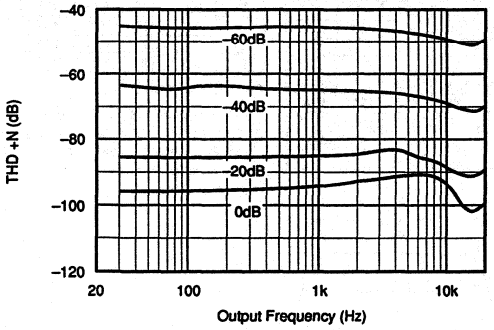
ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE	MAX THD + N, AT 0dB
PCM63P	Plastic DIP	0°C to +70°C	–88dB
PCM63P-J	Plastic DIP	0°C to +70°C	–92dB
PCM63P-K	Plastic DIP	0°C to +70°C	–96dB

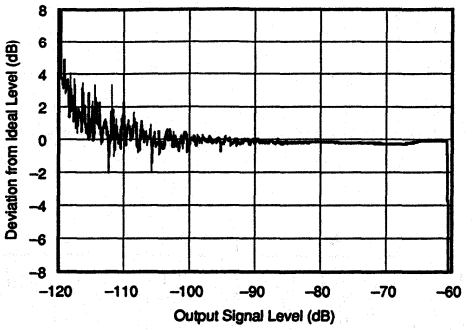
TYPICAL PERFORMANCE CURVES

All specifications at 25°C and $\pm V_A$ and $\pm V_D$ = ±5.0V, unless otherwise noted.

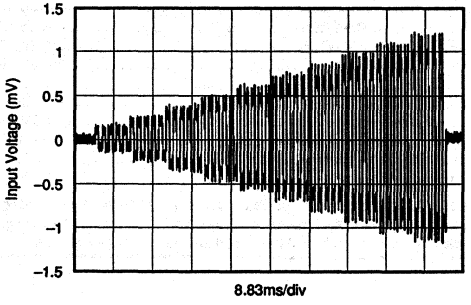
THD + N vs FREQUENCY



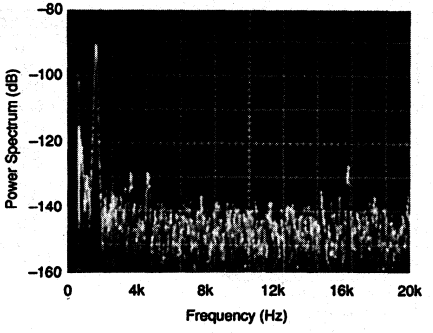
16-BIT LEVEL LINEARITY
(Dithered Fade to Noise)



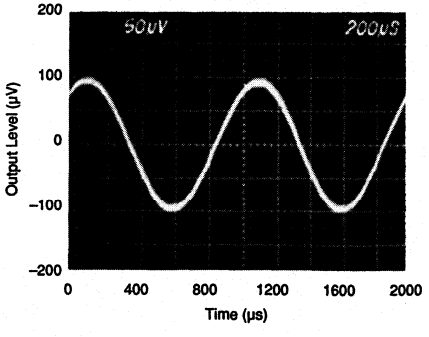
16-BIT MONOTONICITY



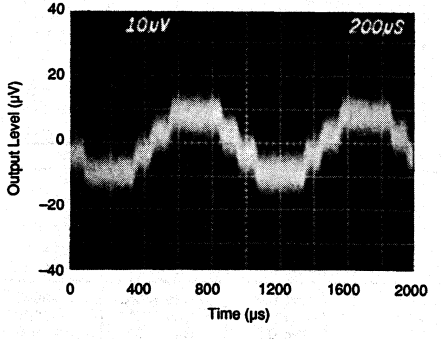
-90dB SIGNAL SPECTRUM
(100Hz Bandwidth)



-90dB SIGNAL
(10Hz to 20kHz Bandwidth)



-110dB SIGNAL
(10Hz to 20kHz Bandwidth)



THEORY OF OPERATION

DUAL-DAC *COLINEAR* ARCHITECTURE

Digital audio systems have traditionally used laser-trimmed, current-source DACs in order to achieve sufficient accuracy. However even the best of these suffer from potential low-level nonlinearity due to errors at the major carry bipolar zero transition. More recently, DACs employing a different architecture which utilizes noise shaping techniques and very high oversampling frequencies, have been introduced ("Bitstream", "MASH", or 1-bit DACs). These DACs overcome the low level linearity problem, but only at the expense of signal-to-noise performance, and often to the detriment of channel separation and intermodulation distortion if the succeeding circuitry is not carefully designed.

The PCM63 is a new solution to the problem. It combines all the advantages of a conventional DAC (excellent full scale performance, high signal-to-noise ratio and ease of use) with superior low-level performance. Two DACs are combined in a complementary arrangement to produce an extremely linear output. The two DACs share a common reference and a common R-2R ladder to ensure perfect tracking under all conditions. By interleaving the individual bits of each DAC and employing precise laser trimming of resistors, the highly accurate match required between DACs is achieved.

This new, complementary linear or dual-DAC ***Colinear*** approach, which steps away from zero with small steps in both directions, avoids any glitching or "large" linearity errors and provides an absolute current output. The low level performance of the PCM63P is such that real 20-bit resolution can be realized, especially around the critical bipolar zero point.

Table I shows the conversion made by the internal logic of the PCM63P from binary two's complement (BTC). Also, the resulting internal codes to the upper and lower DACs (see front page block diagram) are listed. Notice that only the LSB portions of either internal DAC are changing around bipolar zero. This accounts for the superlative performance of the PCM63P in this area of operation.

DISCUSSION OF SPECIFICATIONS

DYNAMIC SPECIFICATIONS

Total Harmonic Distortion + Noise

The key specification for the PCM63P is total harmonic distortion plus noise (THD + N). Digital data words are read into the PCM63P at eight times the standard compact disk audio sampling frequency of 44.1kHz (352.8kHz) so that a sine wave output of 991Hz is realized. For production testing, the output of the DAC goes to an I to V converter, then to a programmable gain amplifier to provide gain at lower signal output test levels, and then through a 40kHz low pass filter before being fed into an analog type distortion analyzer. Figure 1 shows a block diagram of the production THD + N test setup.

For the audio bandwidth, THD + N of the PCM63P is essentially flat for all frequencies. The typical performance curve, "THD + N vs Frequency", shows four different output signal levels: 0dB, –20dB, –40dB, and –60dB. The test signals are derived from a special compact test disk (the CBS CD-1). It is interesting to note that the –20dB signal falls only about 10dB below the full scale signal instead of the expected 20dB. This is primarily due to the superior low-level signal performance of the dual-DAC ***Colinear*** architecture of the PCM63P.

In terms of signal measurement, THD + N is the ratio of $Distortion_{RMS} + Noise_{RMS} / Signal_{RMS}$ expressed in dB. For the PCM63P, THD + N is 100% tested at all three specified output levels using the test setup shown in Figure 1. It is significant to note that this test setup does not include any output deglitching circuitry. All specifications are achieved without the use of external deglitchers.

Dynamic Range

Dynamic range in audio converters is specified as the measure of THD + N at an effective output signal level of –60dB referred to 0dB. Resolution is commonly used as a theoretical measure of dynamic range, but it does not take into account the effects of distortion and noise at low signal levels. The

ANALOG OUTPUT	INPUT CODE (20-bit Binary Two's Complement)	LOWER DAC CODE (19-bit Straight Binary)	UPPER DAC CODE (19-bit Straight Binary)
+Full Scale	011...111	111...111 + 1LSB*	111...111
+Full Scale – 1LSB	011...110	111...111 + 1LSB*	111...110
Bipolar Zero + 2LSB	000...010	111...111 + 1LSB*	000...010
Bipolar Zero + 1LSB	000...001	111...111 + 1LSB*	000...001
Bipolar Zero	000...000	111...111 + 1LSB*	000...000
Bipolar Zero – 1LSB	111...111	111...111	000...000
Bipolar Zero – 2LSB	111...110	111...110	000...000
–Full Scale + 1LSB	100...001	000...001	000...000
–Full Scale	100...000	000...000	000...000

*The extra weight of 1LSB is added at this point to make the transfer function symmetrical around bipolar zero.

TABLE I. Binary Two's Complement to ***Colinear*** Conversion Chart.

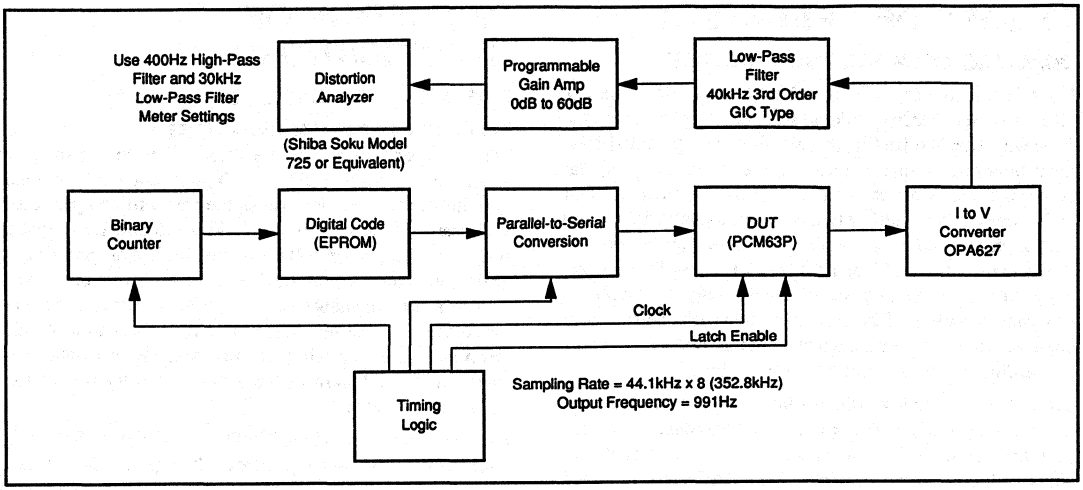


FIGURE 1. Production THD + N Test Setup.

Colinear architecture of the PCM63P, with its ideal performance around bipolar zero, provides a more usable dynamic range, even using the strict audio definition, than any previously available D/A converter.

Level Linearity

Deviation from ideal versus actual signal level is sometimes called "level linearity" in digital audio converter testing. See the "–90dB Signal Spectrum" plot in the Typical Performance Curves section for the power spectrum of a PCM63P at a –90dB output level. (The "–90dB Signal" plot shows the actual –90dB output of the DAC). The deviation from ideal for PCM63P at this signal level is typically less than ±0.3dB. For the "–110dB Signal" plot in the Typical Performance Curves section, true 20-bit digital code is used to generate a –110dB output signal. This type of performance is possible only with the low-noise, near-theoretical performance around bipolar zero of the PCM63P's ***Colinear*** DAC circuitry.

A commonly tested digital audio parameter is the amount of deviation from ideal of a 1kHz signal when its amplitude is decreased from –60dB to –120dB. A digitally dithered input signal is applied to reach effective output levels of –120dB using only the available 16-bit code from a special compact disk test input. See the "16-Bit Level Linearity" plot in the Typical Performance Curves section for the results of a PCM63P tested using this 16-bit dithered fade-to-noise signal. Note the very small deviation from ideal as the signal goes from –60dB to –100dB.

DC SPECIFICATIONS

Idle Channel SNR

Another appropriate specification for a digital audio converter is idle channel signal-to-noise ratio (idle channel SNR). This is the ratio of the noise on the DAC output at bipolar zero in relation to the full scale range of the DAC. To make this measurement, the digital input is continuously fed the code for bipolar zero while the output of the DAC is band-limited from 20Hz to 20kHz and an A-weighted filter is applied. The idle channel SNR for the PCM63P is typically greater than 120dB, making it ideal for low-noise applications.

Monotonicity

Because of the unique dual-DAC ***Colinear*** architecture of the PCM63P, increasing values of digital input will always result in increasing values of DAC output as the signal moves away from bipolar zero in one-LSB steps (in either direction). The "16-Bit Monotonicity" plot in the Typical Performance Curves section was generated using 16-bit digital code from a test compact disk. The test starts with 10 periods of bipolar zero. Next are 10 periods of alternating 1LSBs above and below zero, and then 10 periods of alternating 2LSBs above and below zero, and so on until 10LSBs above and below zero are reached. The signal pattern then begins again at bipolar zero.

With PCM63P, the low-noise steps are clearly defined and increase in near-perfect proportion. This performance is achieved without any external adjustments. By contrast, sigma-delta ("Bitstream", "MASH", or 1-bit DAC) architectures are too noisy to even see the first 3 or 4 bits change (at 16 bits), other than by a change in the noise level.

Absolute Linearity

Even though absolute integral and differential linearity specs are not given for the PCM63P, the extremely low THD + N performance is typically indicative of 16-bit to 17-bit integral linearity in the DAC, depending on the grade specified. The relationship between THD + N and linearity, however, is not such that an absolute linearity specification for every individual output code can be guaranteed.

Offset, Gain, And Temperature Drift

Although the PCM63P is primarily meant for use in dynamic applications, specifications are also given for more traditional DC parameters such as gain error, bipolar zero offset error, and temperature gain and offset drift.

DIGITAL INPUT

Timing Considerations

The PCM63P accepts TTL compatible logic input levels. Noise immunity is enhanced by the use of differential current mode logic input architectures on all input signal lines. The data format of the PCM63P is binary two's complement (BTC) with the most significant bit (MSB) being first in the serial input bit stream. Table II describes the exact relationship of input data to voltage output coding. Any number of bits can precede the 20 bits to be loaded, since only the last 20 will be transferred to the parallel DAC register after LE (P20, Latch Enable) has gone low.

All DAC serial input data (P21, DATA) bit transfers are triggered on positive clock (P18, CLK) edges. The serial-to-parallel data transfer to the DAC occurs on the falling edge of Latch Enable (P20, LE). The change in the output of the DAC coincides with the falling edge of Latch Enable (P20, LE). Refer to Figure 2 for graphical relationships of these signals.

Maximum Clock Rate

A typical clock rate of 16.9MHz for the PCM63P is derived by multiplying the standard audio sample rate of 44.1kHz by sixteen times (16x oversampling) the standard audio word bit length of 24 bits (44.1kHz x 16 x 24 = 16.9MHz). Note that this clock rate accommodates a 24-bit word length, even though only 20 bits are actually being used. The maximum clock rate of 25MHz is guaranteed, but is not 100% final tested. The setup and hold timing relationships are shown in Figure 3.

"Stopped Clock" Operation

The PCM63P is normally operated with a continuous clock input signal. If the clock is to be stopped between input data words, the last 20 bits shifted in are not actually shifted from the serial register to the latched parallel DAC register until Latch Enable (LE, P20) goes low. Latch Enable must remain low until after the first clock cycle of the next data word to insure proper DAC operation. In any case, the setup and hold times for Data and LE must be observed as shown in Figure 3.

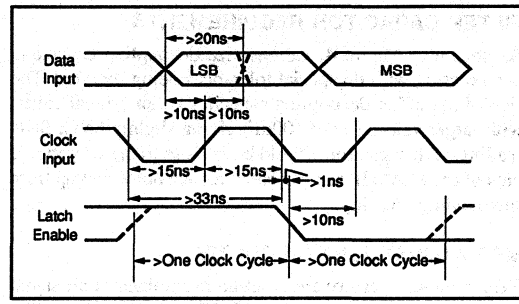
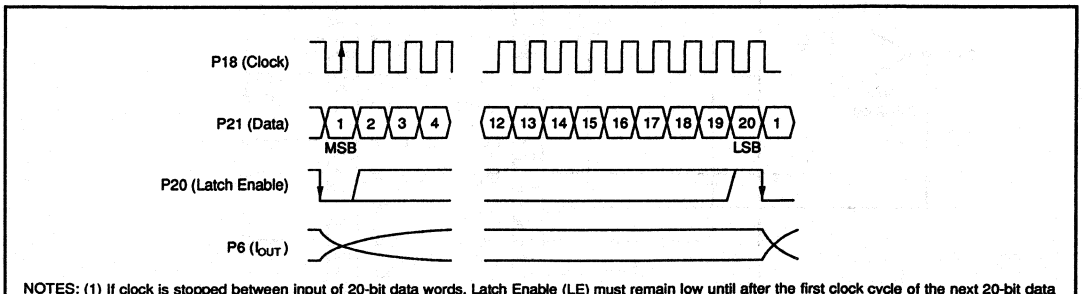


FIGURE 3. Setup and Hold Timing Diagram.

DIGITAL INPUT	ANALOG OUTPUT	CURRENT OUTPUT	VOLTAGE OUTPUT (With External Op Amp)
1,048,576LSBs	Full Scale Range	4.00000000mA	6.00000000V
1LSB	NA	3.81469727nA	5.72204590µV
$7FFFF_{HEX}$	+Full Scale	–1.99999619mA	+2.99999428V
00000_{HEX}	Bipolar Zero	0.00000000mA	0.00000000V
$FFFFF_{HEX}$	Bipolar Zero – 1LSB	+0.00000381mA	–0.00000572V
80000_{HEX}	–Full Scale	+2.00000000mA	–3.00000000V

TABLE II. Digital Input/Output Relationships.



NOTES: (1) If clock is stopped between input of 20-bit data words, Latch Enable (LE) must remain low until after the first clock cycle of the next 20-bit data word stream. (2) Data format is binary two's complement (BTC). Individual data bits are clocked in on the corresponding positive clock edge. (3) Latch Enable (LE) must remain low at least one clock cycle after going negative. (4) Latch Enable (LE) must be high for at least one clock cycle before going negative. (5) I_{OUT} changes on negative going edge of Latch Enable (LE).

FIGURE 2. Timing Diagram.

INSTALLATION

POWER SUPPLIES

Refer to Figure 4 for proper connection of the PCM63P in the voltage-out mode using the internal feedback resistor. The feedback resistor connections (P9 and P10) should be left open if not used. The PCM63P only requires a ±5V supply. Both positive supplies should be tied together at a single point. Similarly, both negative supplies should be connected together. No real advantage is gained by using separate analog and digital supplies. It is more important that both these supplies be as "clean" as possible to reduce coupling of supply noise to the output. Power supply decoupling capacitors should be used at each supply pin to maximize power supply rejection, as shown in Figure 4, regardless of how good the supplies are. Both commons should be connected to an analog ground plane as close to the PCM63P as possible.

FILTER CAPACITOR REQUIREMENTS

As shown in Figure 4, various size decoupling capacitors can be used, with no special tolerances being required. The size of the offset decoupling capacitor is not critical either, with larger values (up to 100µF) giving slightly better SNR readings. All capacitors should be as close to the appropriate pins of the PCM63P as possible to reduce noise pickup from surrounding circuitry.

MSB ADJUSTMENT CIRCUITRY

Near optimum performance can be maintained at all signal levels without using the optional MSB adjust circuitry of the PCM63P shown in Figure 5. Adjustability is provided for those cases where slightly better full-scale THD + N is desired. Use of the MSB adjustments will only affect larger dynamic signals (between 0dB and –6dB). This improvement comes from bettering the gain match between the upper and lower DACs at these signal levels. The change is realized by small adjustments in the bit-2 weights of each DAC. Great care should be taken, however, as improper adjustment will easily result in degraded performance.

In theory, the adjustments would seem very simple to perform, but in practice they are actually quite complex. The first step in the theoretical procedure would involve making each bit-2 weight ideal in relation to its code minus one value (adjusting each potentiometer for zero differential nonlinearity error at the bit-2 major carries). This would be the starting point of each 100kΩ potentiometer for the next adjustment. Then, each potentiometer would be adjusted equally, in opposite directions, to achieve the lowest full-scale THD + N possible (reversing the direction of rotation

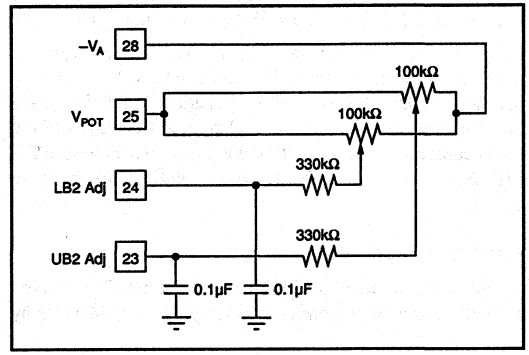


FIGURE 5. Optional Bit-2 Adjustment Circuitry.

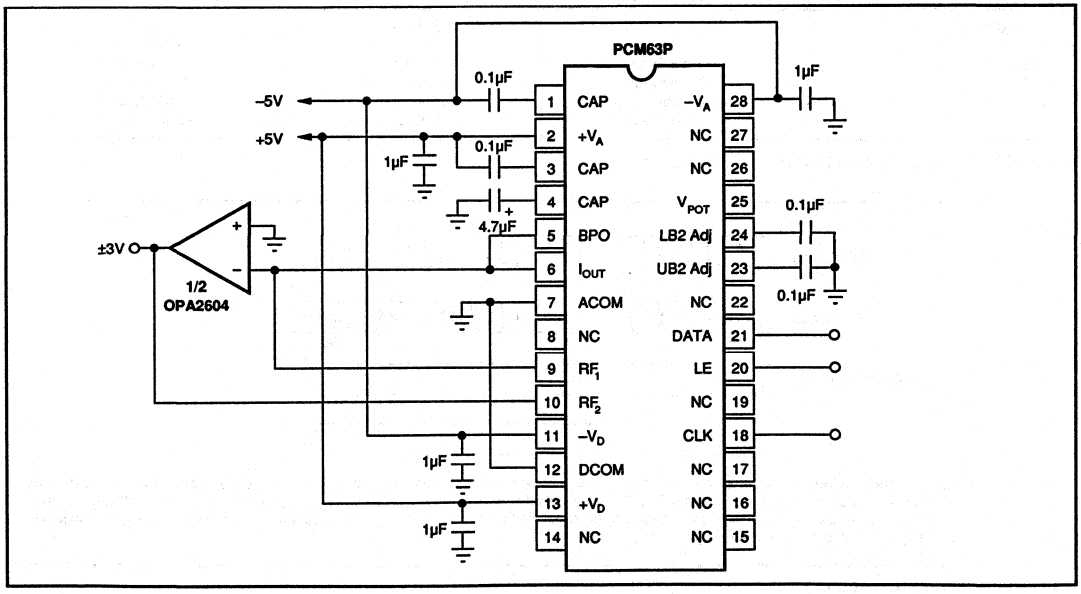


FIGURE 4. Connection Diagram.

for both if no immediate improvement were noted). This procedure would require the generation of the digital bit-2 major carry code to the input of the PCM63P and a DVM or oscilloscope capable of reading the output voltage for a one LSB step (5.72μV) in addition to a distortion analyzer.

A more practical approach would be to forego the minor correction for the bit-2 major carry adjustment and only adjust for upper and lower DAC gain matching. The problem is that just by connecting the MSB circuitry to the PCM63P, the odds are that the upper and lower bit-2 weights would be greatly changed from their unadjusted states and thereby adversely affect the desired gain adjustment. Just centering the 100kΩ potentiometers would not necessarily provide the correct starting point. To guarantee that each 100kΩ potentiometer would be set to the correct starting or null point (no current into or out of the MSB adjust pins), the voltage drop across each corresponding 330kΩ resistor would have to measure 0V. A voltage drop of ±1.25mV across either 330kΩ resistor would correspond to a ±1LSB change in the null point from its unadjusted state (1LSB in current or 3.81nA x 330kΩ = 1.26mV). Once these starting points for each potentiometer had been set, each potentiometer would then be adjusted equally, in opposite directions, to achieve the lowest full-scale THD + N possible. If no immediate improvement were noted, the direction of rotation for both potentiometers would be reversed. One direction of potentiometer counter-rotations would only make the gain mismatch and resulting THD + N worse, while the opposite would gradually improve and then worsen the THD + N after passing through a no mismatch point. The determination of the correct starting direction would be arbitrary. This procedure still requires a good DVM in addition to a distortion analyzer.

Each user will have to determine if a small improvement in full-scale THD + N for their application is worth the expense of performing a proper MSB adjustment.

APPLICATIONS

The most common application for the PCM63P is in high-performance and professional digital audio playback, such as in CD and DAT players. The circuit in Figure 6 shows the PCM63P in a typical combination with a digital interface format receiver chip (Yamaha YM3623), an 8X interpolating digital filter (Burr-Brown DF1700P), and two third-order low-pass anti-imaging filters (implemented using Burr-Brown OPA2604APs).

Using an 8X digital filter increases the number of samples to the DAC by a factor of 8, thereby reducing the need for a higher order reconstruction or anti-imaging analog filter on the DAC output. An analog filter can now be constructed using a simple phase-linear GIC (generalized immittance converter) architecture. Excellent sonic performance is achieved using a digital filter in the design, while reducing overall circuit complexity at the same time.

Because of its superior low-level performance, the PCM63P is also ideally suited for other high-performance applications such as direct digital synthesis (DDS).

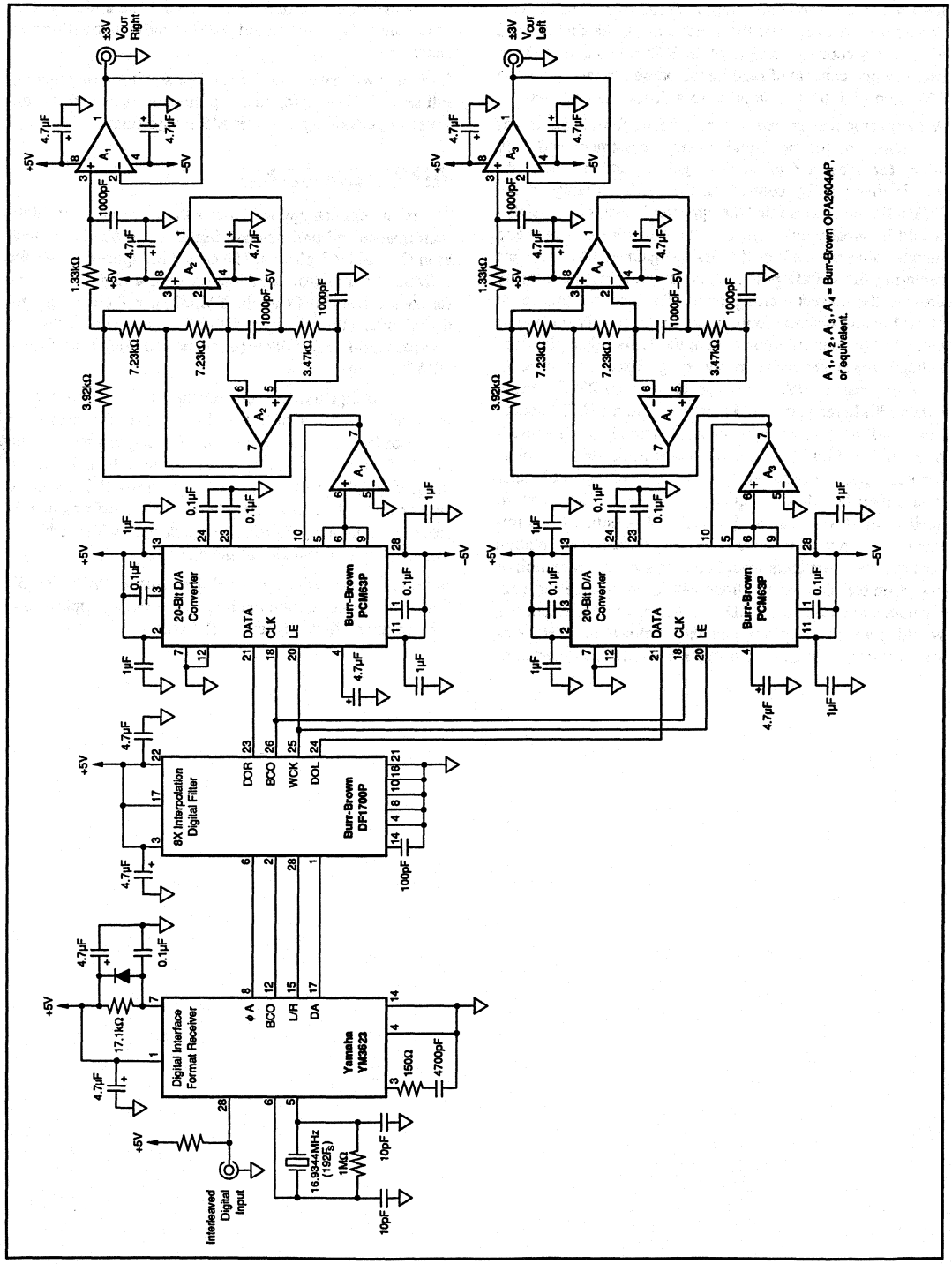
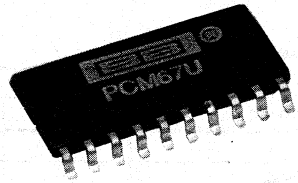


FIGURE 6. Stereo Audio Application.

BURR-BROWN®



PCM67

Dual 18-Bit Monolithic Audio DIGITAL-TO-ANALOG CONVERTER

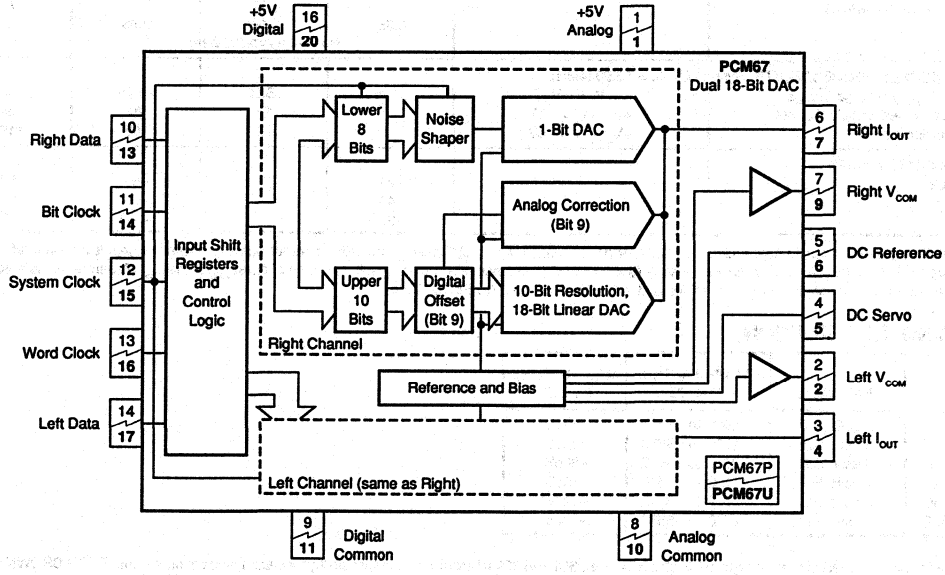
FEATURES

- DUAL 18-BIT BiCMOS AUDIO DAC
- EXCELLENT LOW LEVEL THD + N (–40dB max at –60dBFSR, J GRADE)
- SINGLE SUPPLY +5V OPERATION
- LOW POWER: 75mW TYPICAL
- OPERATING RANGE –25°C TO +85°C
- AVAILABLE IN SPACE SAVING 16-PIN DIP OR 20-PIN SOIC
- CAPABLE OF 16X OVERSAMPLING
- COMPLETE WITH REFERENCE
- LOW COST

DESCRIPTION

The PCM67 is a low cost, dual output 18-bit BiCMOS digital-to-analog converter utilizing a novel architecture to achieve excellent low level performance. By combining a conventional thin-film R-2R ladder DAC, a digital offset technique with analog correction, and an advanced one-bit DAC, the PCM67 achieves high resolution and low zero-crossing distortion.

The PCM67 can be used in a wide variety of consumer audio applications. Its low cost, small size, low power dissipation, and single +5V operation make it ideal for portable digital audio, while its additional wide operating temperature range make it ideal for automotive digital audio and similar applications.



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Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL

All specifications at +25°C and $+V_A$, $+V_D$ = +5V unless otherwise noted

PARAMETER	CONDITIONS	PCM67P/U MIN	PCM67P/U TYP	PCM67P/U MAX	UNITS
RESOLUTION			18		Bits
DYNAMIC RANGE, THD + N at –60dB Referred to Full Scale			108		dB
DIGITAL INPUT					
Logic Family			TTL/CMOS Compatible		
Logic Level: V_{IH}	I_{IH} = ±5µA	+2		$+V_D$	V
V_{IL}	I_{IL} = ±5µA	0		0.8	V
Data Format			Serial, MSB First, BTC[1]		
Input System Clock Frequency			16.9344	20	MHz
TOTAL HARMONIC DISTORTION + N[2,3,4]					
PCM67P, PCM67U					
f = 991Hz (0dB)	f_S = 352.8kHz		–86	–82	dB
f = 991Hz (–20dB)	f_S = 352.8kHz		–68	–64	dB
f = 991Hz (–60dB)	f_S = 352.8kHz		–40	–34	dB
PCM67P-J, PCM67U-J					
f = 991Hz (0dB)	f_S = 352.8kHz		–91	–88	dB
f = 991Hz (–20dB)	f_S = 352.8kHz		–72	–68	dB
f = 991Hz (–60dB)	f_S = 352.8kHz		–46	–40	dB
PCM67P-K, PCM67U-K					
f = 991Hz (0dB)	f_S = 352.8kHz		–95	–92	dB
f = 991Hz (–20dB)	f_S = 352.8kHz		–74	–70	dB
f = 991Hz (–60dB)	f_S = 352.8kHz		–46	–40	dB
CHANNEL SEPARATION			106		dB
ACCURACY					
Level Linearity	at –90dB Signal Level		±1		dB
Gain Error			±3	±10	%
Gain Mismatch, Channel to Channel			±1	±5	%
Gain Drift	0°C to 70°C		95		ppm/°C
Warm-up Time			1		Minute
IDLE CHANNEL SNR[5]	20Hz to 40kHz at BPZ[6]		110		dB
ANALOG OUTPUT					
Output Range (±3%)			1.2		mA
Output Impedance (±30%)			600		Ω
V_{COM}		3.35	3.50	3.65	V
Glitch Energy			No Glitch Around Zero		
POWER SUPPLY REQUIREMENTS, System Clock = 16.9344MHz					
$+V_A$, $+V_D$ Supply Voltage Range	$+V_A$ = $+V_D$	+4.75	+5.00	+5.25	V
$+I_A$, $+I_D$ Combined Supply Current	$+V_A$, $+V_D$ = +5V		15	20	mA
Power Dissipation	$+V_A$, $+V_D$ = +5V		75	105	mW
TEMPERATURE RANGE					
Specification		–25		+85	°C
Operating		–40		+85	°C
Storage		–55		+100	°C

NOTES: (1) Binary Two's Complement coding. (2) Ratio of (Distortion$_{RMS}$+Noise$_{RMS}$)/Signal$_{RMS}$. (3) D/A converter output frequency/signal level (both left and right channels are "on"). (4) D/A converter sample frequency (8 x 44.1kHz; 8X oversampling per channel). (5) Ratio of Noise$_{RMS}$/Signal$_{RMS}$. Measured using a 40kHz 3rd order GIC (Generalized Immittance Converter) filter and an A-weighted filter. (6) Bipolar Zero.

ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE	MAX THD + N, AT 0dB
PCM67P	Plastic DIP	–25°C to +85°C	–82dB
PCM67U	Plastic SOIC	–25°C to +85°C	–82dB
PCM67P-J	Plastic DIP	–25°C to +85°C	–88dB
PCM67U-J	Plastic SOIC	–25°C to +85°C	–88dB
PCM67P-K	Plastic DIP	–25°C to +85°C	–92dB
PCM67U-K	Plastic SOIC	–25°C to +85°C	–92dB

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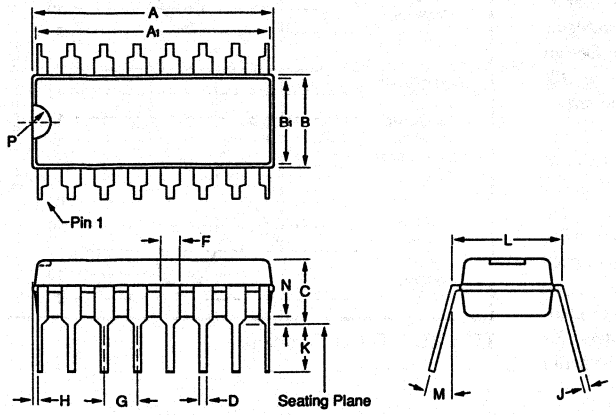
MECHANICAL

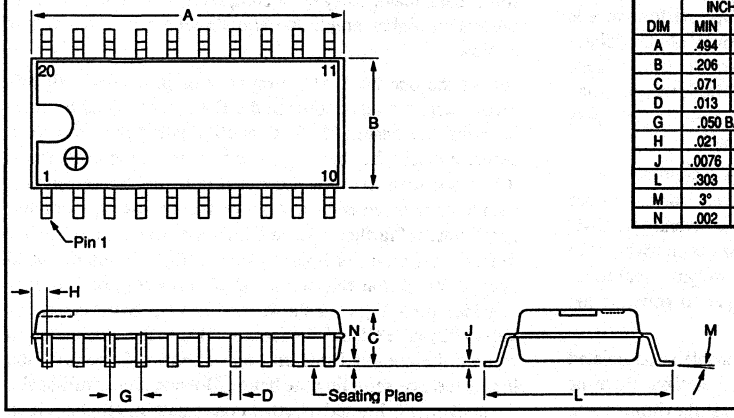
P Package — 16-Pin Plastic DIP



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.740	.800	18.80	20.32
A_1	.725	.785	18.42	19.94
B	.230	.290	5.85	7.38
B_1	.200	.250	5.09	6.36
C	.120	.200	3.05	5.09
D	.015	.023	0.38	0.59
F	.030	.070	0.76	1.78
G	.100 BASIC		2.54 BASIC	
H	.020	.050	0.51	1.27
J	.008	.015	0.20	0.38
K	.070	.150	1.78	3.82
L	.300 BASIC		7.63 BASIC	
M	0°	15°	0°	15°
N	.010	.030	0.25	0.76
P	.025	.050	0.64	1.27

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

U Package — 20-Pin Plastic SOIC



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.494	.498	12.55	12.65
B	.206	.210	5.23	5.33
C	.071	.077	1.80	1.96
D	.013	.017	0.33	0.43
G	.050 BASIC		1.27 BASIC	
H	.021	.025	0.53	0.64
J	.0076	.0082	0.19	0.21
L	.303	.311	7.70	7.90
M	3°	5°	3°	5°
N	.002	.006	0.05	0.15

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

PIN ASSIGNMENTS

PCM67P	PCM67U	DESCRIPTION	MNEMONIC
1	1	+5V Analog Supply Voltage	$+V_A$
2	2	Left Voltage Common	LV_{COM}
	3	No Connection	NC
3	4	Left Current Output (0 to 1.2mA)	LI_{OUT}
4	5	Servo Decoupling Capacitor	SRVCAP
5	6	Reference Decoupling Capacitor	REFCAP
6	7	Right Current Output (0 to 1.2mA)	RI_{OUT}
	8	No Connection	NC
7	9	Rigth Voltage Common	RV_{COM}
8	10	Analog Common	ACOM
9	11	Digital Common	DCOM
	12	Reserved for Future Use	RSRVD
10	13	Right Data Input	RDATA
11	14	Bit Clock	BTCK
12	15	System Clock	SYSCK
13	16	Word Clock	WDCK
14	17	Left Data Input	LDATA
	18	Reserved for Future Use	RSRVD
15	19	Reserved for Future Use	RSRVD
16	20	+5V Digital Supply Voltage	$+V_D$

ABSOLUTE MAXIMUM RATINGS

$+V_A$, $+V_D$ to ACOM, DCOM	0V to +6.5V
ACOM to DCOM	±0.5V
Digital Inputs to DCOM	–0.3V to $+V_D$ + 0.3V
Power Dissipation	300mW
Lead Temperature, (soldering, 10s)	+300°C
Max Junction Temperature	165°C
Thermal Resistance, θ_{JA}	70°C/W

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

THEORY OF OPERATION

Digital converters in audio systems have traditionally utilized a laser-trimmed, current-source DAC architecture. Unfortunately, this type of technology suffers from the problems inherent in switching widely varying current levels. Design improvements have helped, but DACs of this type still exhibit low-level nonlinearity due to errors at the major carry.

Recently, DACs employing a different architecture have been introduced. Most of these DACs utilize a one-bit DAC with "noise shaping" techniques and very high oversampling rate to achieve the digital-to-analog conversion. Basically, the trade-off is from very accurate but slow current sources to one rapidly sampled current source whose average output in the audio frequency range is equal to the current desired. Noise shaping ensures that the "undesirable" frequencies associated with the one-bit DAC output lie outside the audio range.

These "Bitstream", "MASH", or one-bit DACs overcome the low level linearity problems of conventional DACs since there can be no major carry error. However, this architecture exhibits problems of it own: signal-to-noise performance is usually worse than a similar conventional DAC, "dither noise" may be needed in order to get rid of unwanted tones, a separate high-speed clock may be required, the part may show sensitivity to clock jitter, and a high-order low-pass filter is necessary to filter the DAC output.

The PCM67 is a cross between these two architectures. It includes both a conventional laser-trimmed, current-source DAC and an advanced one-bit DAC. The conventional DAC is a 10-bit DAC where each bit weight has been trimmed to 18-bit linearity. The one-bit DAC has a weight equal to bit 10 and employs a first-order noise shaper to generate the "bitstream."

This approach does not eliminate all the problems associated with the two architectures but rather minimizes them as much as possible. The conventional DAC still exhibits some major carry error which would normally reduce low-level linearity. However, to reduce this error even further, the PCM67 utilizes an offset technique whereby bit 9 is subtracted from the digital input code whenever it is positive (see Figure 1 and Table I). When this is done, an offset current equal to the weight of bit 9 is switched in to compensate.

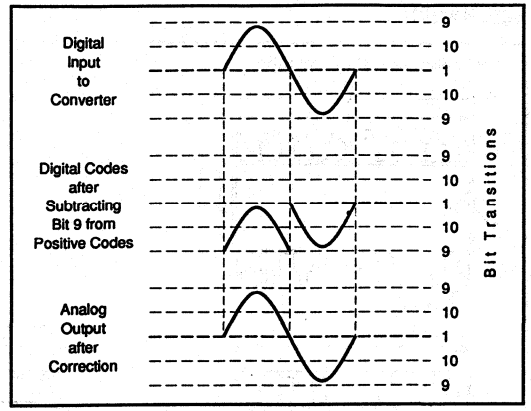


FIGURE 1. Offset Technique.

This offset comes from a one-bit DAC which has also been trimmed to 18-bit linearity. While this technique doesn't remove the major carry error completely, the "glitch" is only present in higher amplitude signals where it is much less audible.

As for the one-bit DAC, a number of problems with this architecture are also reduced: the DAC is designed to operate from the system clock, thus eliminating the need for a separate clock; the lower quantizing level of the DAC make it less sensitive to clock jitter; and output filtering requirements are reduced because "out-of-band noise" has smaller amplitude, is "farther out," and increases much more slowly due to the first-order noise shaper. Still, it is important to keep in mind that the one-bit DAC imposes some design considerations. Figure 2 shows the THD + N of the converter versus "System Clock" frequency. This is the clock used to operate the one-bit DAC and noise shaper. Generally, the higher the oversampling the better. However, near full-scale, the converter is limited by other constraints and higher clock frequencies (past $96f_s$) tend to slightly worsen its performance. At low levels, performance improves almost linearly with increasing clock frequency. The one-bit DAC was designed to operate between $96f_s$ (4X oversampling) and $384f_s$ (16X oversampling). But, it can be operated at $48f_s$ (2X oversampling) with slightly reduced performance.

ANALOG OUTPUT	INPUT CODE (18-Bit Binary Two's Complement)	10-BIT DAC CODE (10-Bit Binary Two's Complement)	OFFSET CORRECTION
+Full Scale	01 1111 1111 1111 1111	01 1111 1101	Yes
+Full Scale – 1LSB	01 1111 1111 1111 1110	01 1111 1101	Yes
Bipolar Zero + 512 LSBs	00 0000 0010 0000 0000	00 0000 0000	Yes
Bipolar Zero + 511 LSBs	00 0000 0001 1111 1111	11 1111 1111	Yes
Bipolar Zero + 1LSB	00 0000 0000 0000 0001	11 1111 1110	Yes
Bipolar Zero	00 0000 0000 0000 0000	11 1111 1110	Yes
Bipolar Zero – 1LSB	11 1111 1111 1111 1111	11 1111 1111	No
–Full Scale + 1LSB	10 0000 0000 0000 0001	10 0000 0000	No
–Full Scale	10 0000 0000 0000 0000	10 0000 0000	No

TABLE I. Digital Inputs and PCM67's Resulting Internal State.

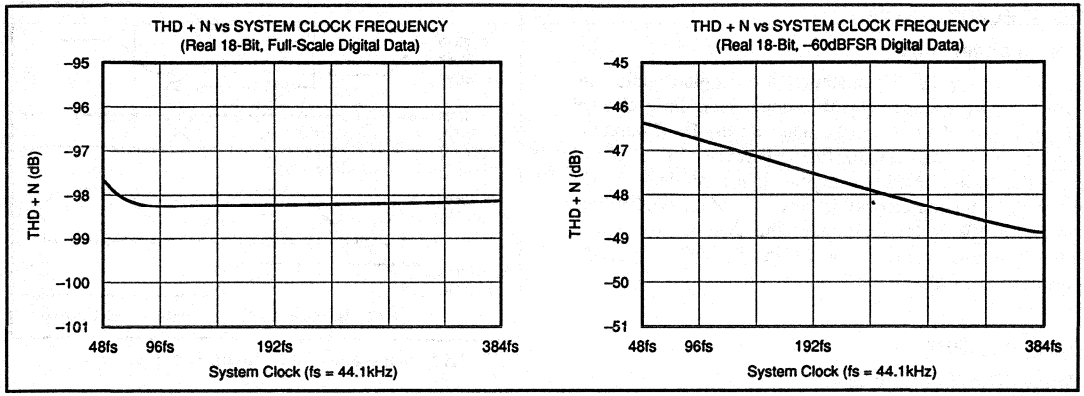


FIGURE 2. THD + N versus System Clock Frequency.

DISCUSSION OF SPECIFICATIONS

DYNAMIC SPECIFICATIONS

Total Harmonic Distortion + Noise

A key specification for audio DACs is usually total harmonic distortion plus noise (THD + N). For the PCM67, THD + N is tested in production as shown in Figure 3. Digital data words are read into the PCM67 at eight times the standard compact disk audio sampling frequency of 44.1kHz (352.8kHz) so that a sine wave output of 991Hz is realized. The output of the DAC goes to an I to V converter, then to a programmable gain amplifier to provide gain at lower signal output test levels, and then through a 40kHz low pass filter before being fed into an analog type distortion analyzer.

Dynamic Range

Dynamic range in audio converters is specified as the measure of THD + N at an effective output signal level of –60dB referred to 0dB. Resolution is commonly used as a theoretical measure of dynamic range, but it does not take into account the effects of distortion and noise at low signal levels. The PCM67, with its improved performance around bipolar zero, provides greater than 108dB of dynamic range.

Level Linearity

Deviation from ideal versus actual signal level is sometimes called "level linearity" in digital audio converter testing. The deviation from ideal for PCM67 at –90dB output signal is typically less than ±1dB.

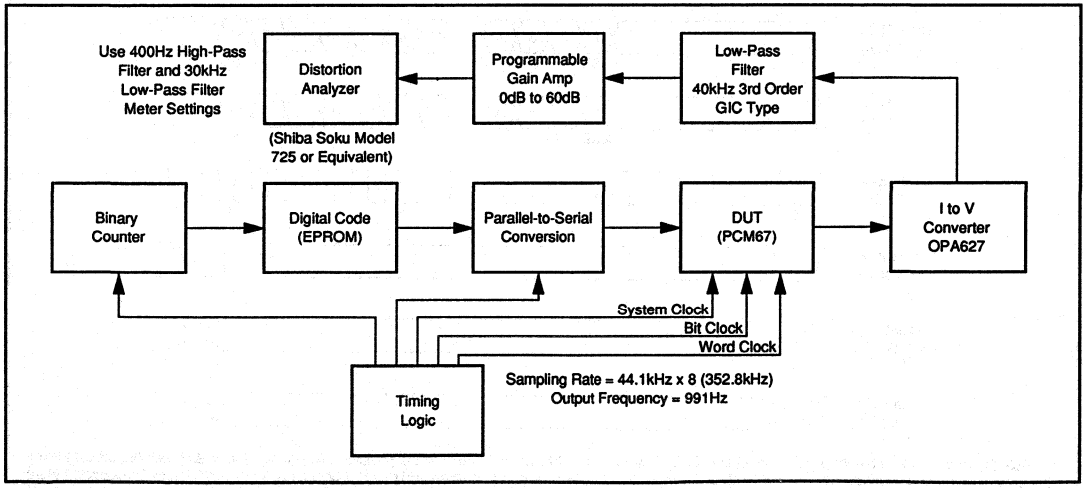


FIGURE 3. Production THD + N Test Setup.

DC SPECIFICATIONS

Idle Channel SNR

Another appropriate specification for a digital audio converter is idle channel signal-to-noise ratio (idle channel SNR). This is the ratio of the noise on the DAC output at bipolar zero in relation to the full scale range of the DAC. To make this measurement, the digital input is continuously fed the code for bipolar zero while the output of the DAC passed through a 40kHz low-pass filter and then an A-weighted filter. The idle-channel SNR for the PCM67 is typically greater than 110dB.

DIGITAL INPUT

Timing Considerations

The PCM67 accepts TTL compatible logic input levels. The data format of the PCM67 is binary two's complement (BTC) with the most significant bit (MSB) being first in the serial input bit stream. Table II describes the exact relationship of input data to current output coding. Six Bit Clock cycles must precede the 18 bits to be loaded.

All DAC serial input data bit transfers are triggered on positive Bit Clock (BTCK) edges. The serial-to-parallel data transfer to the DAC occurs on the falling edge of Word Clock (WDCK). The change in the output of the DAC coincides with the falling edge of Word Clock (WDCK). Refer to Figure 4 for graphical relationships of these signals. The setup and hold timing relationships for these and other signals are shown in Figure 5.

DIGITAL INPUT	ANALOG OUTPUT	CURRENT OUTPUT
262,144LSBs	Full Scale Range	1.200000mA
1LSB	NA	4.5776362nA
$1FFFF_{HEX}$	+Full Scale	1.199995mA
00000_{HEX}	Bipolar Zero	0.600000mA
$3FFFF_{HEX}$	Bipolar Zero – 1LSB	0.599995mA
20000_{HEX}	–Full Scale	0.000000mA

TABLE II. Digital Input/Analog Output Relationships.

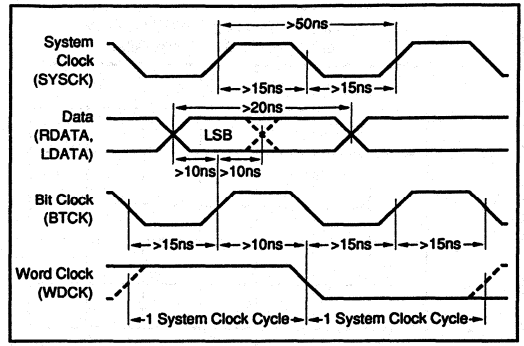
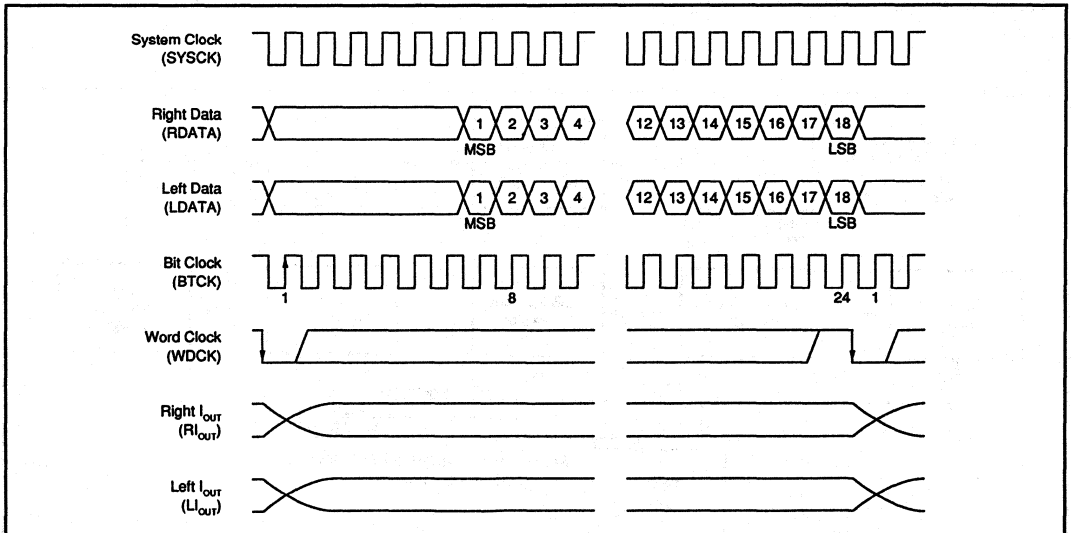


FIGURE 5. Setup and Hold Timing Diagram.

The PCM67 requires that the System Clock (SYSCK) be a multiple of 24 times the Word Clock (WDCK) in order for the one-bit DAC and noise shaper to function properly. There is no constraint on the phase relationship between System Clock (SYSCK) and Bit Clock (BTCK).

Maximum Clock Rate

A typical clock rate of 16.9344MHz for the PCM67 is derived by multiplying the standard audio sample rate of 44.1kHz by sixteen times (16X oversampling) and then by



NOTES: (1) Data format is binary two's complement (BTC). Individual data bits are clocked in on the positive-going clock edge of Bit Clock (BTCK). (2) Word Clock (WDCK) must remain low at least one System Clock (SYSCK) cycle after going negative and must be high for at least one System Clock cycle before going negative. (3) Right I_{OUT} (RI_{OUT}) and Left I_{OUT} (LI_{OUT}) change on the negative-going edge of Word Clock. (4) System Clock must be a multiple of 24 of the Word Clock frequency. (5) There is no constraint on the phase relationship between System Clock and Bit Clock.

FIGURE 4. Timing Diagram.

the standard audio word bit length of 24 bits (44.1kHz x 16 x 24 = 16.9344MHz). Note that this clock rate accommodates a 24-bit word length, even though only 18 bits are actually being used. The maximum clock rate of 20MHz is guaranteed, but is not 100% final tested.

INSTALLATION

POWER SUPPLIES

Refer to Figure 6 for proper connection of the PCM67. The PCM67 requires only a +5V supply. Both analog and digital supplies should be tied together at a single point, and no real advantage is gained by using separate supplies. It is more important that both these supplies be as "clean" as possible to reduce coupling of supply noise to the output. A power supply decoupling capacitor should be used near the analog supply pin to maximize power supply rejection, as shown in Figure 6, regardless of how good the supplies are. Both commons should be connected to an analog ground plane as close to the PCM67 as possible.

FILTER CAPACITOR REQUIREMENTS

As shown in Figure 6, various size decoupling capacitors can be used, with no special tolerances being required. All capacitors should be as close to the appropriate pins of the PCM67 as possible to reduce noise pickup from surrounding circuitry.

RESERVED PINS

Burr-Brown is currently investigating different modes of operation for future PCM67 type products (left/right data on one data pin, etc.) and has reserved some pins on the PCM67 for future use. On the PCM67P (16-pin DIP), one "reserved" (RSRVD) pin has been included. The PCM67U (20-pin SOIC) includes three reserved (RSRVD) pins. These pins should be considered as digital input pins and tied to +5V. If you require a different mode of operation than that currently offered by the PCM67, please contact your local Burr-Brown Sales Representative or Burr-Brown directly (at the number given on the front of this product data sheet) for more information.

APPLICATIONS

The most common application for the PCM67 is in consumer digital audio playback, such as in CD and DAT players. The circuit in Figure 6 shows the PCM67 in a typical configuration with a digital interface format receiver chip (Yamaha YM3623), an 8X interpolating digital filter (Burr-Brown DF1700P), and two third-order low-pass anti-imaging filters (implemented using Burr-Brown OPA2604APs).

The 8X digital filter increases the number of samples to the DAC by a factor of 8 while providing the necessary clock and data inputs. A simple linear-phase GIC (generalized immittance converter) low-pass filter is used for anti-imaging and also serves to filter out the "shaped-noise" of the one-bit DAC.

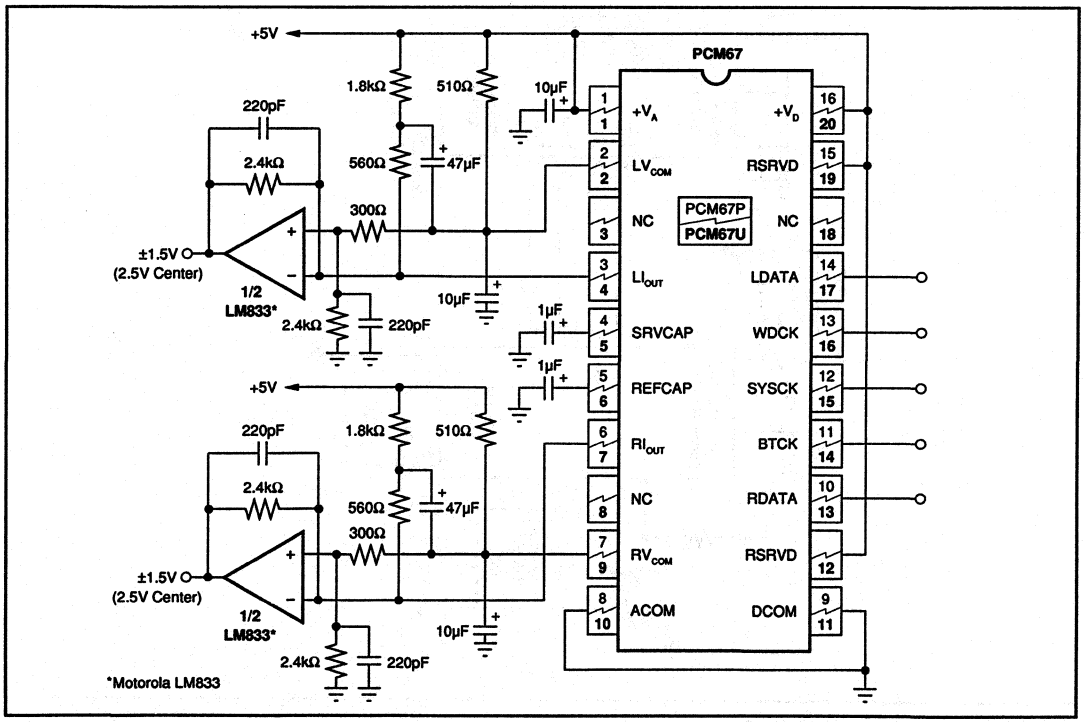


FIGURE 6. Connection Diagram.

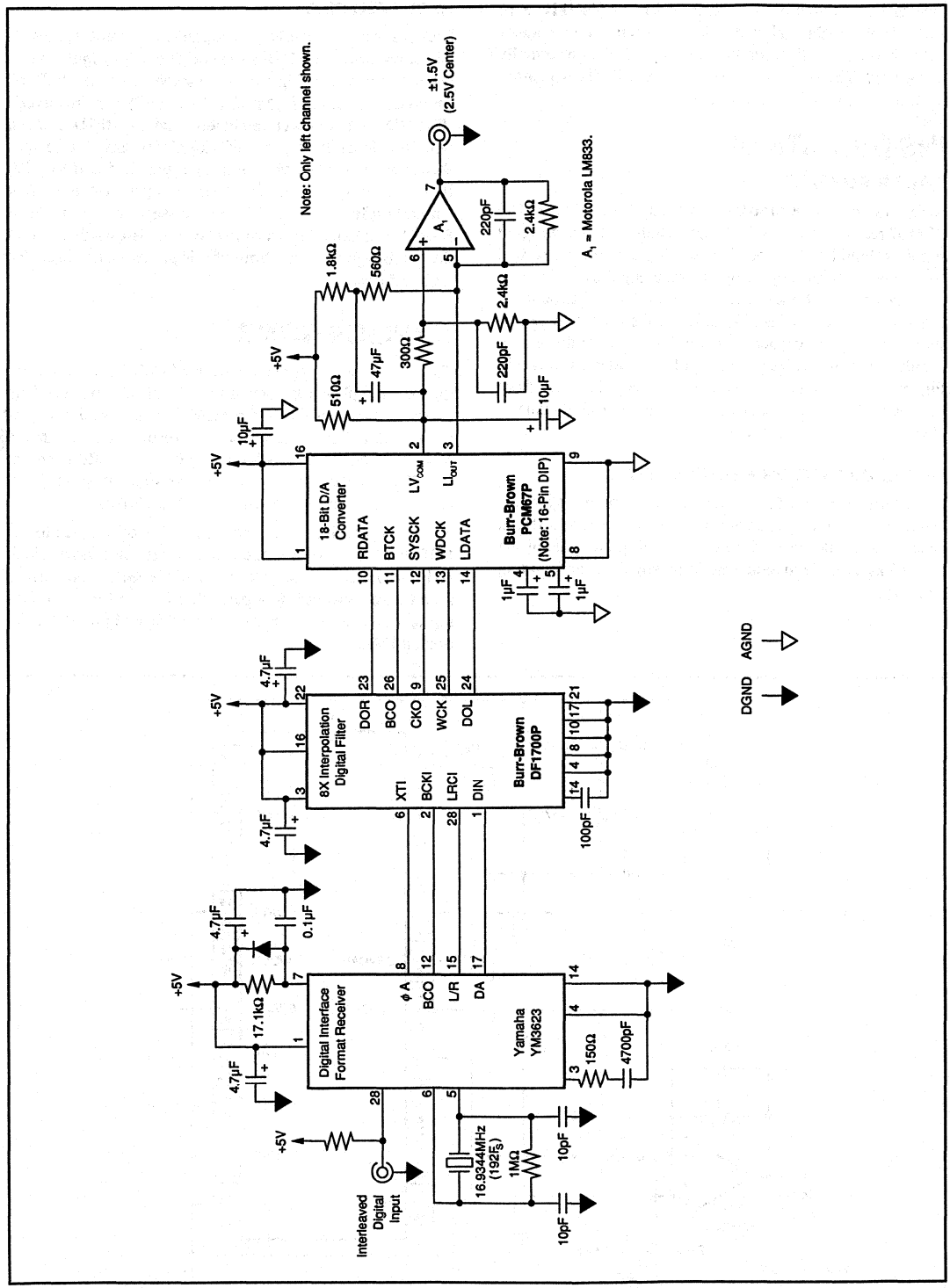


FIGURE 7. Stereo Audio Application.

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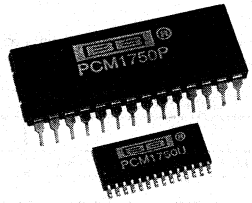


PCM1750P
PCM1750U

Dual CMOS 18-Bit Monolithic Audio ANALOG-TO-DIGITAL CONVERTER

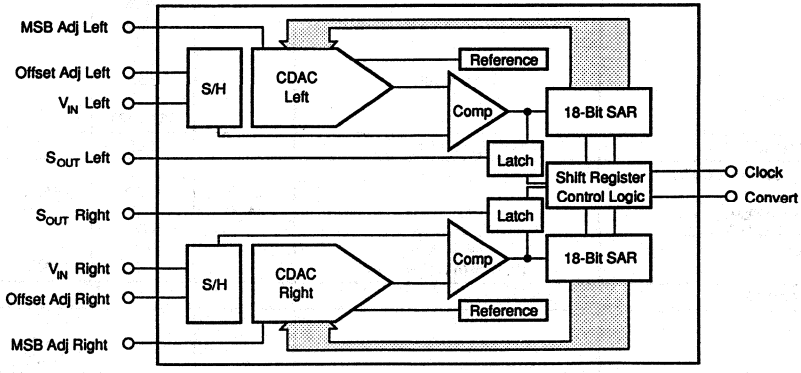
FEATURES

- DUAL18-BIT LOW-POWER CMOS AUDIO A/D CONVERTER
- FAST 4.5µs MIN CONVERSION TIME INCLUDING S/H
- VERY LOW MAX THD+N: –88dB Without External Adjust
- COMPLETE WITH INTERNAL REFERENCE AND DUAL S/H FUNCTION
- TWO CO-PHASE SAMPLED, ±2.75V AUDIO INPUTS
- CAPABLE OF 4X PER CHANNEL OVERSAMPLING RATE
- RUNS ON ±5V SUPPLIES AND DISSIPATES 300mW MAX
- COMPACT 28-PIN PLASTIC DIP OR SOIC

DESCRIPTION

The PCM1750 is a low cost, dual 18-bit CMOS analog-to-digital converter optimized for dynamic signal applications. The PCM1750 features true co-phased inputs with an internal sample/hold function for each channel. The PCM1750 also comes complete with an internal reference. Total power dissipation is less than 300mW max using ±5V voltage supplies. Low maximum Total Harmonic Distortion + Noise (–88dB max) is 100% tested. The very fast PCM1750 is capable of 4X audio bandwidth oversampling rates on both input channels simultaneously, providing greater freedom to designers in selecting input anti-aliasing filters.

PCM1750 outputs serial data in a format that is compatible with many digital filter chips and comes packaged in a space saving 28-pin plastic DIP or SOIC.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL

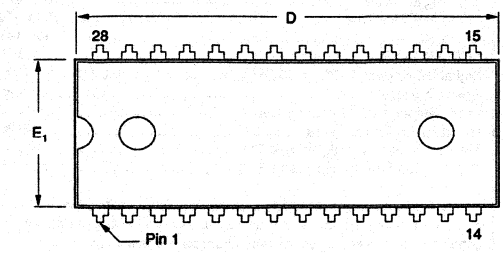
At 25°C, and $\pm V_A = \pm 5.0V$; $+V_D = +5.0V$, unless otherwise noted. Where relevant, specifications apply to both left and right input/output channels.

PARAMETER	CONDITIONS	PCM1750P/U MIN	PCM1750P/U TYP	PCM1750P/U MAX	UNITS
RESOLUTION		18			Bits
DYNAMIC RANGE	THD + N at –60dB Referred to Full Scale	+88	+90		dB
ANALOG INPUT					
Input Range			±2.75		V
Input Capacitance			20		pF
Aperture Delay			10		ns
Aperture Uncertainty (Jitter)			50		ps_{rms}
Full Power Input Bandwidth			500		kHz
DIGITAL INPUT/OUTPUT					
Logic Family			CMOS Compatible		
Logic Level: V_{IH}	$I_{IH} = \pm 5\mu A$	+3.5		$+V_D + 0.3$	V
V_{IL}	$I_{IL} = \pm 5\mu A$	–0.3		+1.5	V
V_{OH}	$I_{SOURCE} = 1.0mA$	+2.7	+4.7		V
V_{OL}	$I_{SINK} = 3.2mA$		+0.2	+0.4	V
Output Data Format			Serial, MSB First, BTC[1]		
Convert Command			Positive Edge		
Convert Command Pulse Width			81		ns
Conversion Time	Throughput Including Sample/Hold[2]	4.5	5.2	20.8	µs
DYNAMIC CHARACTERISTICS (20Hz to 24kHz; 4X data decimated to 1X)					
Signal-to-Noise Ratio[3]	fs = 192kHz[4]; f_{IN} = 1kHz (0dB)[5]	+88	+90		dB[6]
Total Harmonic Distortion + N[7]	Without External Adjustments				
f_{IN} = 1kHz (0dB)	fs = 192kHz		–90	–88	dB
f_{IN} = 1kHz (–20dB)	fs = 192kHz		–70	–68	dB
f_{IN} = 1kHz (–60dB)	fs = 192kHz		–30	–28	dB
Channel Separation	fs = 192kHz; f_{IN} = 1kHz (0dB) and 0V	+96	+108		dB
ACCURACY					
Gain Error			±2	±5	%
Gain Mismatch	Channel to Channel		±0.5	±2.0	%
BPZ (Bipolar Zero) Error[8]			±2		mV
BPZ Error Mismatch	Channel to Channel		±3		mV
BPZ Differential Linearity Error[9]			±0.002		% of FSR[10]
Linearity Error			±0.003		% of FSR
Warm-up Time			1		ms
DRIFT (With Internal Reference)					
Gain	0°C to 70°C		±50		ppm/°C
Bipolar Zero	0°C to 70°C		±10		ppm of FSR/°C
DRIFT (Exclusive of Internal Reference)					
Gain	0°C to 70°C		±10		ppm/°C
Bipolar Zero	0°C to 70°C		±3		ppm of FSR/°C
REFERENCE					
V_{REF} Output (Pins 19, 24):					
Voltage			+2.75		V
Current			±100		µA
Impedance			0.2		Ω
Accuracy			±25		mV
Drift	0°C to 70°C		±50		ppm/°C
V_{REF} Input (Pins 18, P25):					
Impedance[11]			363 || 120		Ω || pF
POWER SUPPLY REJECTION	% of V_{IN} / % of V_{SUPPLY}[12]		0.03		% / %
POWER SUPPLY REQUIREMENTS					
$\pm V_A$ Supply Voltage Range		±4.75	±5.00	±5.25	V
$+V_D$ Supply Voltage Range		+4.75	+5.00	+5.25	V
$+I_A$; $+I_D$ Combined Supply Current	$+V_A$; $+V_D$ = +5.0V		+28		mA
$-I_A$ Supply Current	$-V_A$ = –5.0V		–13		mA
Power Dissipation	$\pm V_A = \pm 5.0V$; $+V_D$ = +5.0V		210	300	mW
TEMPERATURE RANGE					
Specification		0		+70	°C
Operating		–40		+85	°C
Storage		–60		+100	°C

NOTES: (1) Binary Two's Complement coding. (2) The PCM1750 is tested and guaranteed at 5.2µs, however it will operate at 4.5µs. The dynamic performance is not guaranteed or tested at this conversion rate. (3) Ratio of $Signal_{RMS}$ / ($Distortion_{RMS}$ + $Noise_{RMS}$). (4) A/D converter sample frequency (4 x 48kHz; 4X oversampling per channel). (5) A/D converter input frequency (signal level). (6) Referred to input signal level. (7) Ratio of ($Distortion_{RMS}$ + $Noise_{RMS}$) / $Signal_{RMS}$. (8) Externally adjustable to zero error. (9) Differential non-linearity error at bipolar major carry input code. Externally adjustable to zero error. (10) Full scale range (5.50V). (11) Refer to equivalent circuit in Figure 1. (12) Worst case operating condition. Refer to typical performance curves.

MECHANICAL

P Package — 28-Pin Plastic DIP

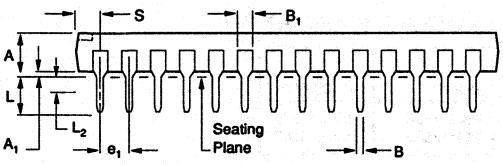


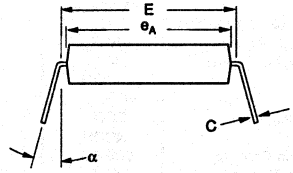
DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A(1)	.169	.200	4.29	5.08
A1(1)	.015	.070	0.38	1.78
B	.015	.020	0.38	0.51
B1	.015	.055	0.38	1.40
C	.008	.012	0.20	0.30
D(1)	1.380	1.455	35.05	36.96
E	.600	.625	15.24	15.88
E1(1)	.485	.550	12.32	13.97
e1	.100 BASIC		2.54 BASIC	
eA	.600 BASIC		15.24 BASIC	

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
L	.100	.200	2.54	5.08
L2	.000	.030	0.00	0.76
α	0°	15°	0°	15°
S(1)	.040	.080	1.02	2.03

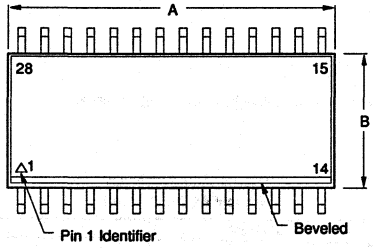
(1) Not JEDEC Standard

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.



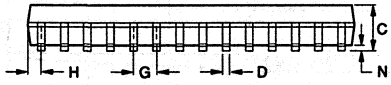


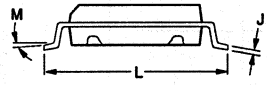
U Package — 28-Pin Plastic SOIC



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.700	.716	17.78	18.19
B	.286	.302	7.26	7.67
C	.093	.109	2.36	2.77
D	.016 BASIC		0.41 BASIC	
G	.050 BASIC		1.27 BASIC	
H	.022	.038	0.56	0.97
J	.008	.012	0.20	0.30
L	.398	.414	10.11	10.52
M	5° TYP		5° TYP	
N	.000	.012	0.00	0.30

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.





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PIN ASSIGNMENTS

PIN	DESCRIPTION	MNEMONIC
1	–5V Analog Supply Voltage	$-V_A$
2	+5V Analog Supply Voltage	$+V_A$
3	Serial Output (Left Channel)	SOUTL
4	External Clock Input	CLK
5	+5V Analog Supply Voltage	$+V_A$
6	+5V Digital Voltage Supply	$+V_D$
7	+5V Digital Voltage Supply	$+V_D$
8	Digital Common Connection	DCOM
9	Analog Common Connection	ACOM
10	Digital Common Connection	DCOM
11	Convert Command Input	CONVERT
12	Serial Output (Right Channel)	SOUTR
13	+5V Analog Supply Voltage	$+V_A$
14	–5V Analog Supply Voltage	$-V_A$
15	Offset Adjust (Right Channel)	OFF_{ADJR}
16	MSB Adjust (Right Channel)	MSB_{ADJR}
17	Analog Voltage Input (Right Channel; ±2.75V)	V_{INR}
18	Reference Voltage Input (Right Channel)	$VREF_{INR}$
19	Reference Voltage Output (Right Channel)	$VREF_{OUTR}$
20	Analog Common Connection	ACOM
21	Reference Voltage Decouple	$VREF_{CAP}$
22	Reference Common Connection	RCOM
23	Analog Common Connection	ACOM
24	Reference Voltage Output (Left Channel)	$VREF_{OUTL}$
25	Reference Voltage Input (Left Channel)	$VREF_{INL}$
26	Analog Voltage Input (Left Channel; ±2.75V)	V_{INL}
27	MSB Adjust (Left Channel)	MSB_{ADJL}
28	Offset Adjust (Left Channel)	OFF_{ADJL}

ABSOLUTE MAXIMUM RATINGS

Analog Input Voltage (V_{IN})	$-V_A$ –0.3V to $+V_A$ + 0.3V
$+V_A$; $+V_D$ to ACOM/DCOM	0 to +7V
$-V_A$ to ACOM/DCOM	0 to –7V
$-V_A$ to $+V_A$; $+V_D$	0 to +14V
ACOM to DCOM	±1V
Digital Inputs (pins 4, 11) to DCOM	–0.3V to $+V_D$ + 0.3V
Power Dissipation	400mW
Lead Temperature, (soldering 10s)	+300°C
Max Junction Temperature	165°C
Thermal Resistance, θ_{JA}: Plastic DIP	80°C/W
Thermal Resistance, θ_{JA}: Plastic SOIC	100°C/W

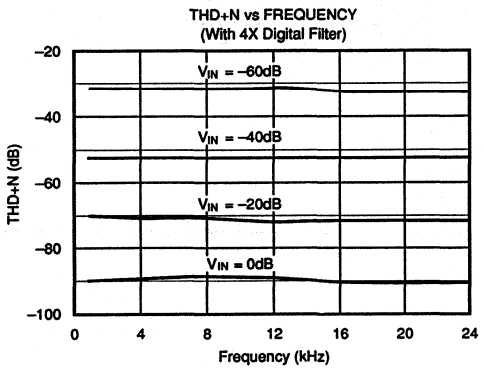
NOTE: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

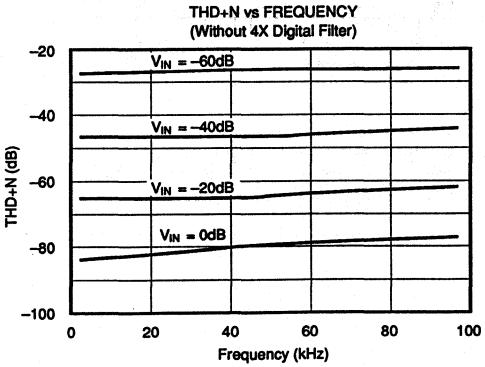
ORDERING INFORMATION

MODEL	PACKAGE
PCM1750P	Plastic DIP
PCM1750U	Plastic SOIC

TYPICAL PERFORMANCE CURVES

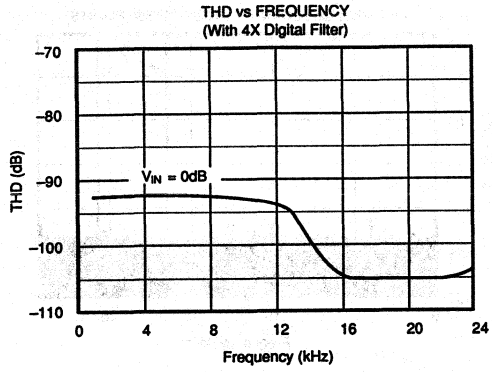
At 25°C, and $\pm V_A = \pm 5.0V$; $+V_D = +5V$, unless otherwise noted. Where relevant, specifications apply to both left and right input output channels.

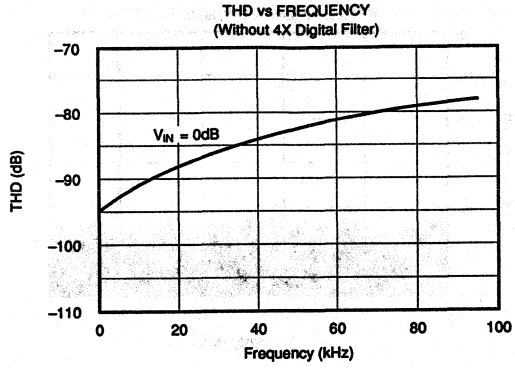


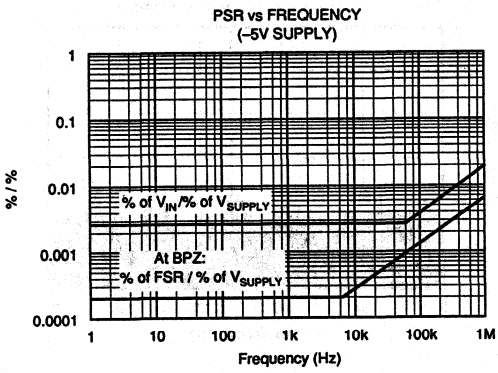


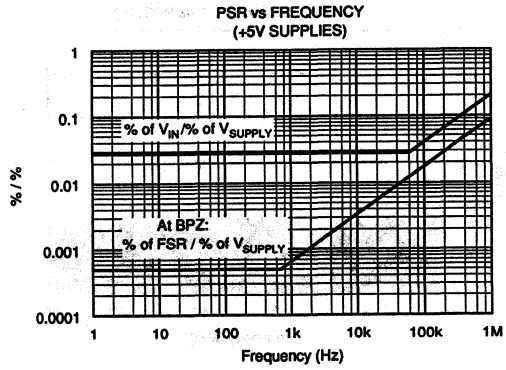
TYPICAL PERFORMANCE CURVES (CONT)

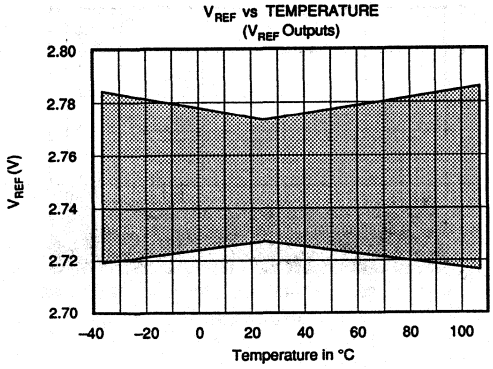
At 25°C, and $\pm V_A = \pm 5.0V$; $+V_D = +5.0V$, unless otherwise noted. Where relevant, specifications apply to both left and right input-output channels.

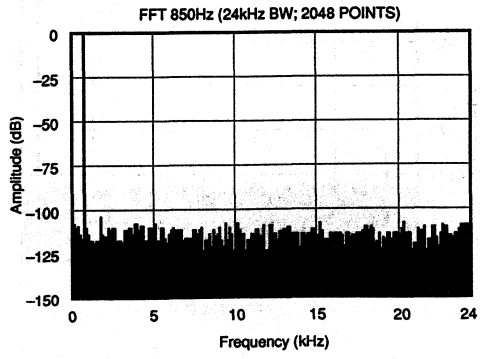






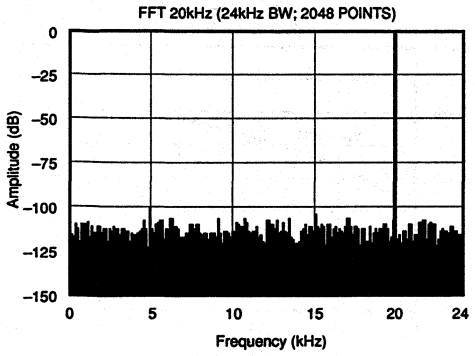


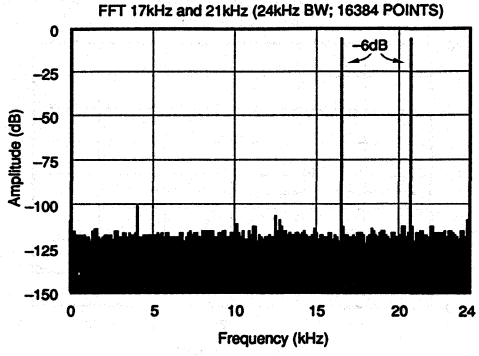


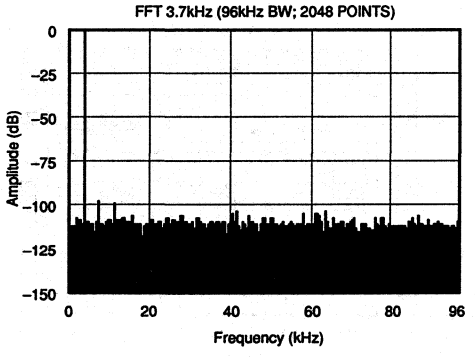


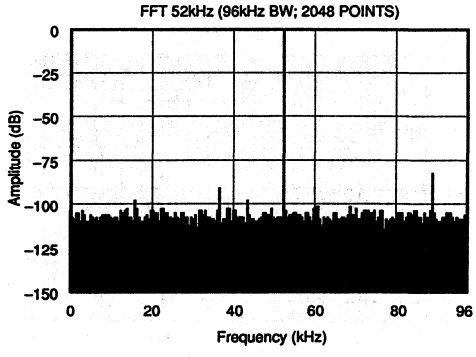
TYPICAL PERFORMANCE CURVES (CONT)

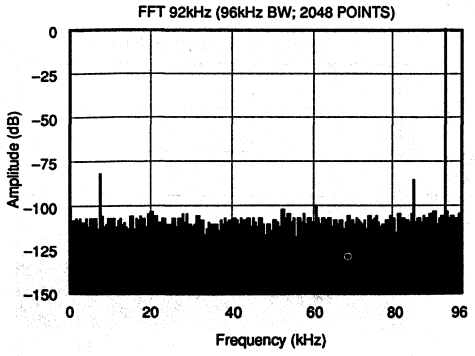
At 25°C, and $\pm V_A$; $+V_D = \pm 5V$, unless otherwise noted. Where relevant, specifications apply to both left and right input-output channels.

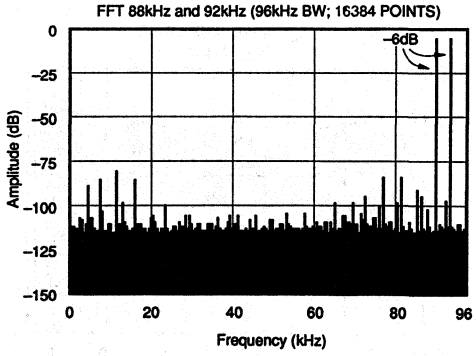












THEORY OF OPERATION

OVERVIEW

The PCM1750 is a dual 18-bit successive approximation CMOS analog-to-digital converter with serial data outputs designed especially for digital audio and similar applications. The single-chip converter is fabricated on a 3µ P-well CMOS process which includes poly-poly capacitors, laser-trimmable nichrome resistors, and two layers of interconnect metal. The dual converter employs a switched capacitor architecture which provides separate, simultaneous S/H (sample/hold) functions for each input channel. The separate S/H for each channel results in a desired feature called co-phase sampling which means that both S/H circuits are switched at the same time into the HOLD mode to capture their respective input signals simultaneously. This eliminates phasing errors produced by alternative architecture ADCs which do not sample the two input channels at the same time.

Switched binary-weighted poly-poly capacitors are used in CDAC (capacitive digital-to-analog converter) configurations to form the successive approximation converter sections

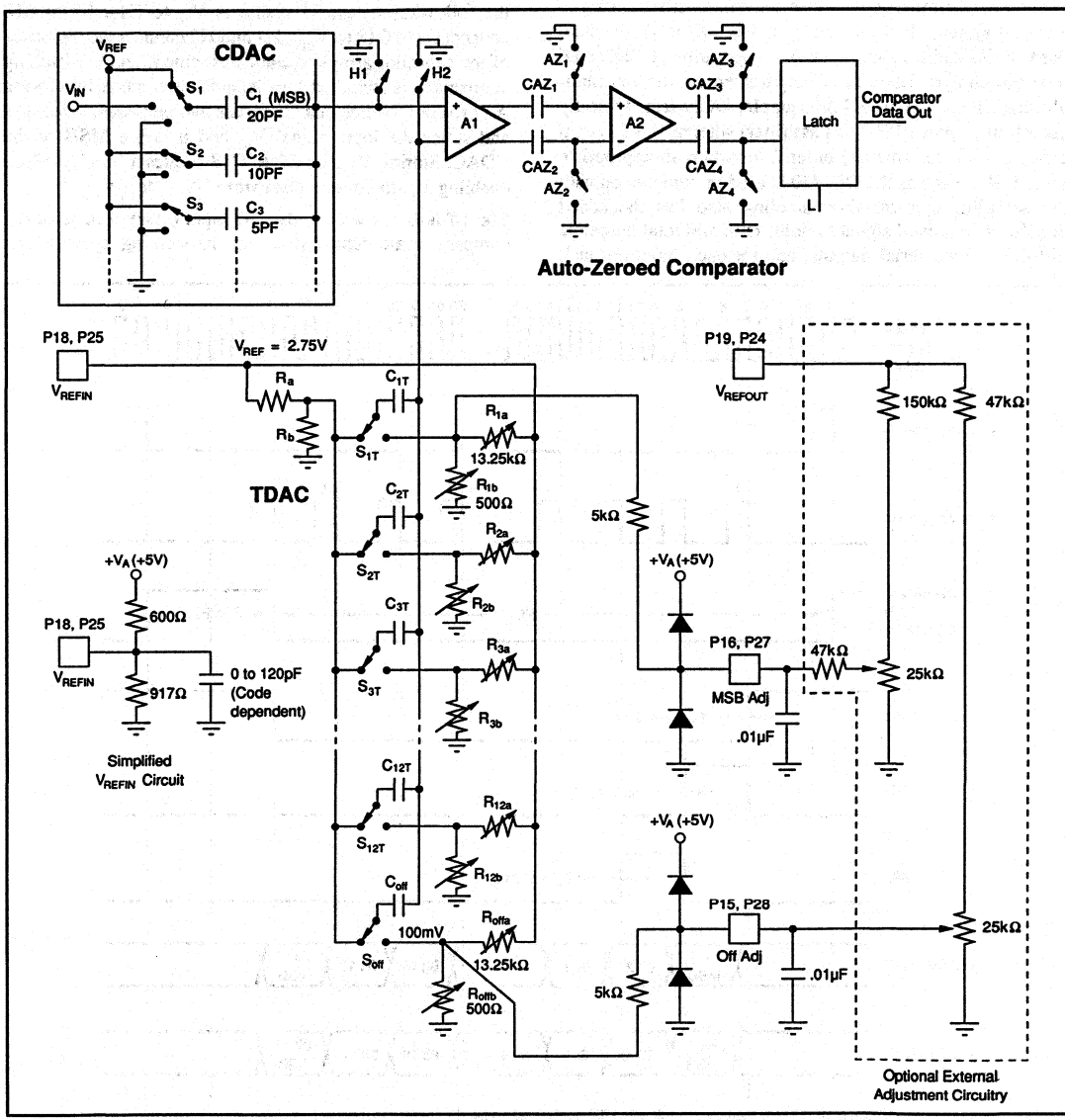


FIGURE 1. PCM1750 Simplified Circuit Diagram.

of the PCM1750. Two other switched-capacitor TDACs (trim-DACs, which employ laser-trimmed nichrome resistors) are also used to provide small correction voltages to the latching comparators. These small correction voltages compensate for ratio matching errors of the binary-weighted capacitors in the CDAC. The comparators contain autozeroed preamplifier stages ahead of the latching amplifier stage to produce a one bit, serial data stream that controls the successive approximation algorithm for each channel of the PCM1750.

To simplify user application, the PCM1750 includes an internal band-gap reference with fast settling buffer amplifiers to drive the CDACs. The dual converters operate synchronously (to minimize digital noise conversion errors) using an external system clock (normally at 1X, 2X or 4X the standard 48kHz audio sampling rate). By operating at a 2X or 4X over sampling rate the roll-off requirement for the input anti-aliasing filters is relaxed. For example, 1X systems typically use a 9 to 11 pole LPF (low pass filter) whereas a 4X system can use a 6th (or smaller) order filter when an appropriate digital filter such as the DF1750 is used in conjunction with the sampling system. Oversampling also has the added benefit of improved signal to noise ratio and total harmonic distortion. Two serial outputs, one for each input channel, provide binary-two's-complement coded output to an optional external digital decimation filter when over sampling operation is desired. The use of the optional companion digital filter, the DF1750, is described later in the installation and application sections of this product data sheet. A separate product data sheet is also available for the Burr-Brown DF1750 giving all the specifications and performance diagrams associated with this digital filter.

SAMPLE (TRACKING) MODE

After each conversion, the dual ADC returns to the SAMPLE mode in order to track the input signals. The switches shown in the simplified circuit diagram of Figure 1 will then be in the following states: S1 connects V_{IN} to C1 ; S2 to S18 connect C2 to C18 to V_{REF}; H1 and H2 connect the top plates of the capacitor arrays to analog common; and the latching comparator is switched into its auto-zero mode by closing AZ1 to AZ4. Notice that C1 serves two purposes: it samples and stores the input signal V_{IN} and it is the MSB of the CDAC. Storing V_{REF} on C2 to C18 creates a bipolar offset, enabling V_{IN} to cover a span from $-V_{REF}$ to $+V_{REF}$.

The 1/f noise as well as the DC input offset voltage of the comparator are removed by an autozeroing cycle which

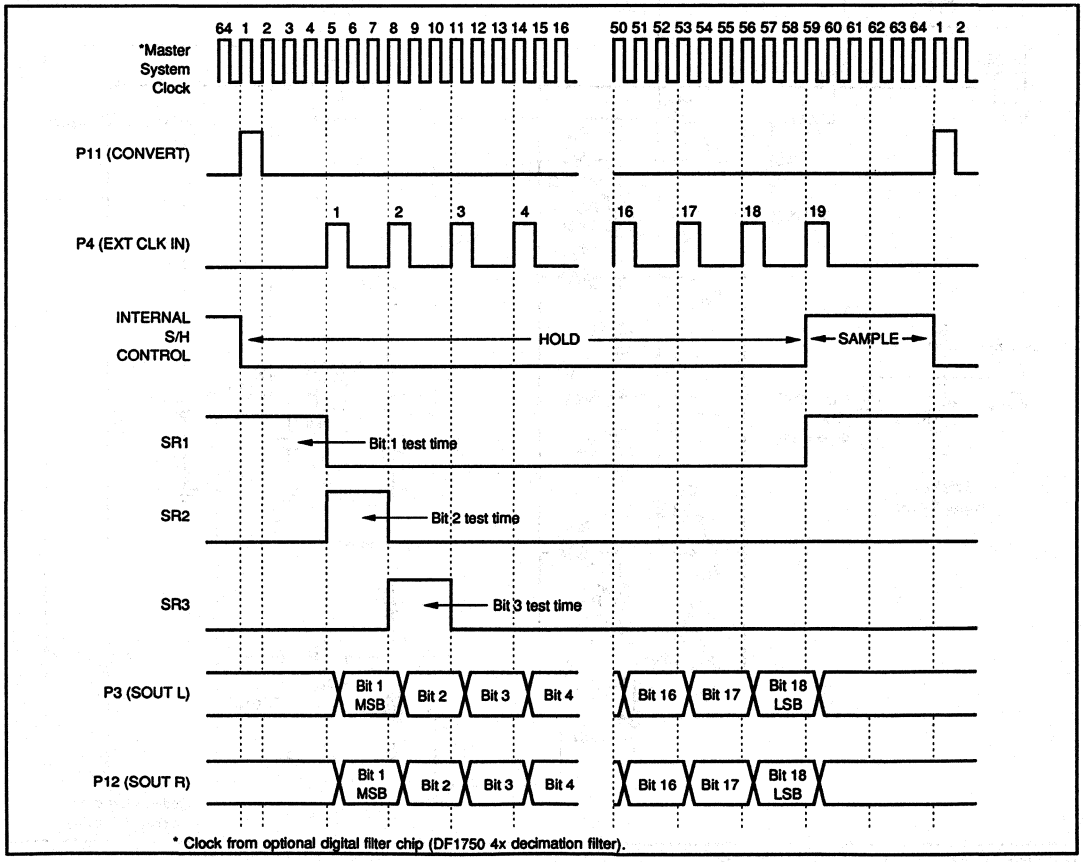


FIGURE 2. PCM1750 Input/Output Timing Diagram.

occurs during the SAMPLE period (see the timing diagram shown in Figure 2). These errors are stored on the AC coupling capacitors (CAZ1 to CAZ4, shown in Figure 1) between the gain stages. During the SAMPLE period the inputs to gain stages A1 and A2 and the latch are grounded by switches H1, H2, and AZ1 to AZ4. Capacitors CAZ1 and CAZ2 track the amplified offset voltage of gain stage A1 and capacitors CAZ3 and CAZ4 do the same for A2. At the beginning of a conversion cycle, the autozeroing switches open and the instantaneous amplified value of both the DC offset voltage and the low-frequency flicker noise is stored on the coupling capacitors to produce zero comparator offset during a conversion cycle.

SUCCESSIVE APPROXIMATION CONVERSION PROCESS

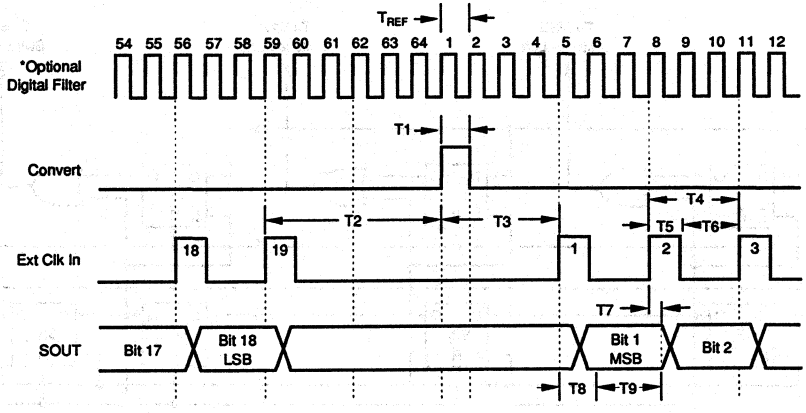
The timing diagram in Figure 2 illustrates the successive approximation routine of the PCM1750. Control signals CONVERT and CLK are derived from a master system clock which comes from a $256f_s$ (256 X the base sampling frequency of 48kHz) clock used by the optional digital filter. There are 64 clocks shown in the timing diagram because the PCM1750 is shown operating at 4 times the standard 48kHz sample rate (192kHz).

Several events occur on the rising edge of the CONVERT command. Switches AZ1 to AZ4, H1 and H2 open and switch S1 reconnects the MSB capacitor, C1, from V_{IN} to analog common (see Figure 1). This terminates the comparator auto-zero cycle and simultaneously switches (co-phase sampling) both converters from tracking their respective input signals into the HOLD mode, thus capturing the instantaneous value of V_{IN} (with a small delay specified as the aperture time).

At the start of a conversion cycle when S1 is switched to analog common, the sampled input signal V_{IN} will appear at the comparator input as $-V_{IN}/2$ due to the 2-to-1 capacitive divider action of C1 = C2 + C3 + ... C18. In a somewhat similar manner, V_{REF} is transferred to the comparator input as $-V_{REF}/2$ to create a bipolar offset.

The 19-bit shift register, shown in Figure 4, controls testing of the bits of the dual ADCs beginning with bit-1 (MSB) and proceeding one bit at a time to bit-18 (LSB), leaving ON those bits that don't cause the cumulative value of the CDAC to exceed the original input value and leaving OFF those bits that do. Since the bits of both channels are tested together, only one shift register is required to control both ranks of 18 data latches.

For example, the testing of bit-2 proceeds in the following manner. The positive pulse from the second shift register element SR2, (see Figure 2 and 4) is applied to the bit-2 data latch and NOR gate. The NOR gate in turn drives S2 and switches bit-2 at the beginning of the bit-2 test interval. Note that the bit interval must be long enough to allow both the comparator input to settle and the comparator to respond. On



PARAMETER	DESCRIPTION	MIN	NOMINAL	MAX	UNITS
T1 (1 x TREF)	Convert Command High	24	33	55	% of T4
T2 (6 x TREF)	S/H Acquisition Time	420	486		ns
T3 (4 x TREF)	Convert to Clock time	281	326	1302	ns
T4 (3 x TREF)	Master Clock Input	211	244	977	ns
T5 (1 x TREF)	Clock High	24	33	55	% of T4
T6 (2 x TREF)	Clock Low	45	67	76	% of T4
T7	Data Hold Time	10			ns
T8	Data Setup Time			100	ns
T9	Data Valid Time	120	154	1212	ns
TCONV (64 x TREF)	Conversion Throughput Time	4.5	5.2	20.8	µs
TREF (Sample Rate /64)	Ext Digital Filter Clock	70	81	326	ns

Note: The nominal timing shown in this diagram is all done automatically by the DF1750 digital filter. Only the optional digital filter clock is required when the DF1750 is used.

FIGURE 3. PCM1750 Setup and Hold Timing Diagram.

the next rising edge of CLKIN, at the end of the test interval, the comparator latch is strobed, providing a feedback logic level which tells the second data latch if bit-2 should be kept or rejected. This logic level is stored in the data latch and is passed on to switch S2 via the NOR gate on the falling edge of the pulse from SR2. This decision to keep or reject bit-2 moves the comparator input closer to a null condition, namely, zero potential. This sequential process continues for bit-3 through bit-18 and nulls the comparator inputs to within a value limited by the total system noise and the resolution/speed of the comparator.

Notice from the timing diagram in Figure 2 that the successive approximation algorithm operates synchronously with an external clock to minimize digitally-coupled switching noise from corrupting either the sample-to-hold operation or the critical comparator bit decisions. The two serial output data streams are derived synchronously from the respective latched comparator outputs and are available after a delay of one CLKIN cycle as illustrated in Figure 2. The serial output driver cells are TTL and CMOS compatible.

DIFFERENTIAL LINEARITY CALIBRATION

To understand the calibration of the PCM1750 it is necessary to discuss some of the characteristics of poly-poly capacitors. Poly capacitors are known to have equal or better stability and matching properties when compared to other precision components such as thin film resistors. On a well controlled process, ratio matching is typically 0.1% — a very respectable number for an untrimmed component. Even more impressive is their ratio tracking versus temperature of approximately 0.1ppm/°C.

Achieving DLE (differential linearity error) of less than 1/2 LSB at the 16-bit level requires ratio matching of the more significant bits to about 0.001%. Since the untrimmed ratio matching of poly capacitors is about two orders of magnitude larger than this requirement, a one-time factory calibration of the upper bits is required as described in the next section. Next, consider the effect of temperature due to the ratio tracking of 0.1ppm/°C. Over a 50°C span, DLE will change less than 1LSB at 18-bits; therefore, recalibration at temperature extremes is not necessary. Because of this excellent stability versus temperature (and versus time, also), the one-time factory calibration to correct initial DLE is more than satisfactory in meeting the accuracy requirements of the PCM1750.

TDAC OPERATION

Operation of the TDAC (trim DAC), which is laser trimmed at the wafer level, is described using bit-1 as an example. Switch S1T (see Figure 1) operates between two voltage levels—a reference level set by voltage divider Ra, Rb and a laser trimmable level set by R1a, R1b. The differences of these two levels is coupled by capacitor C1T to the minus input of the comparator to generate a correction voltage for

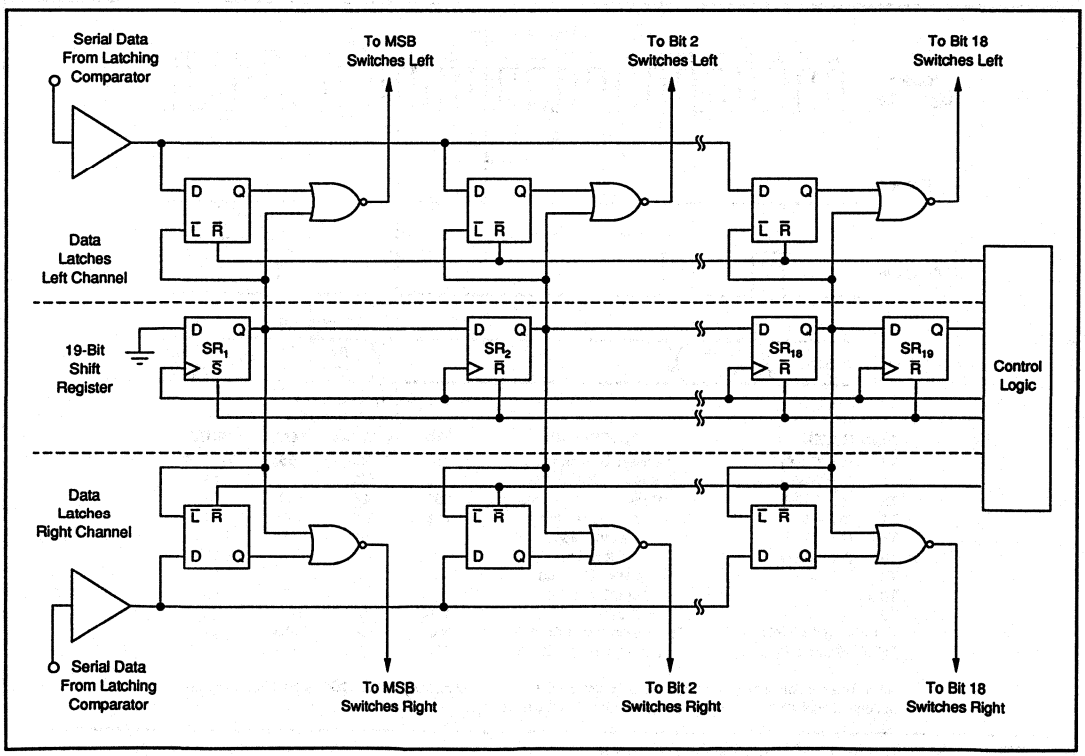


FIGURE 4. PCM1750 Successive Approximation Logic Diagram.

bit-1. The switches of the CDAC and the switches of the TDAC operate concurrently with each other, that is, when a decision is made to keep or reject bit-1, the same decision is made for the correction voltage for bit-1. Even though the ratio stability of the nichrome resistors used in the TDAC may not be as good as the poly capacitors, it is inconsequential because the correction voltage of each bit has a limited range of adjustment.

The DLE at the major carry (a code change from 111...111 to 000...000; in binary two's complement coding) is typically ±1/2 LSB at the 16-bit level, which is sufficient to provide 90dB SNR and –30dB low level distortion (–60dB input). For applications requiring less DLE at the major carry, a pin is provided for each channel to make an external MSB adjustment.

DISCUSSION OF SPECIFICATIONS

RESOLUTION AND DYNAMIC RANGE

The theoretical resolution of the PCM1750 is 18-bits. The maximum possible number of output codes or counts at 18-bits is 262,144 or 108dB (calculated by raising 2 to the 18th power). The relative accuracy of any A/D converter, however, is more a function of it's absolute linearity and signal-to-noise ratio than how many bits of resolution it has. These more pertinent specifications are described later in this section.

Dynamic range, as it is usually defined for digital audio converters, is the measure of THD + N at an effective input signal level of –60dB referred to 0dB. For the PCM1750 this value is typically 90dB and a minimum of 88dB (for audio bandwidth = 20Hz to 24kHz, THD + N at –60db = –30 db typ, –28dB max; f_{IN} = 1kHz and f_S = 192kHz). Resolution is also commonly used as a theoretical measure of dynamic range, but it does not take into account the effects of distortion and noise at low signal levels.

ANALOG INPUT RANGE

The analog input range for the PCM1750 is a bipolar ±2.75V (nominal). Table I gives the precise input/output and voltage/code relationships for the PCM1750. Figure 5 shows these same relationships in a graphical format. It should be noted that the computed voltage input levels represent center values (the midpoint between code transitions). Output coding is in binary two's complement.

DIGITAL OUTPUT	ANALOG INPUT	VOLTAGE INPUT
262144 LSBs	Full Scale Range	5.50000000V
1 LSB	Minimum Step Size	20.98083496µV
$1FFFF_{HEX}$	+Full Scale	+2.74997902V
00000_{HEX}	Bipolar Zero	0.00000000V
$3FFFF_{HEX}$	Bipolar Zero –1LSB	–0.00002098V
20000_{HEX}	–Full Scale	–2.75000000V

TABLE I. Analog Input to Digital Output Relationships.

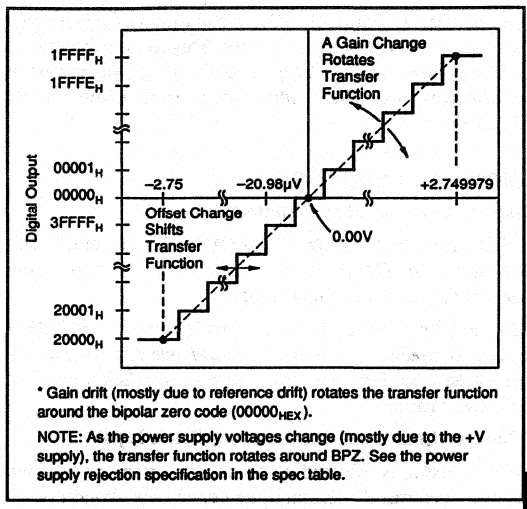


FIGURE 5. Analog Input to Digital Output Diagram.

From Figure 5, the effects of offset and gain errors can be visualized. These errors can change value in response to changes in temperature and/or supply voltage. In addition, gain error (or the full scale range, FSR) changes in direct proportion to the $VREF_{IN}$ voltage value.

SAMPLE AND HOLD PARAMETERS

Aperture Delay and Uncertainty

Aperture delay is the time required to switch from the SAMPLE to HOLD mode. This time is typically 10ns for the PCM1750 and it is constant. Aperture uncertainty (jitter) is the amount of uncertainty associated with the aperture delay. Aperture uncertainty affects the overall accuracy of the converter and is greatest at the maximum input frequency of the converter. The formula for determining the maximum input frequency (f_{MAX}) for a given error contribution due to aperture uncertainty is: $f_{MAX} = (2 \times \pi \times t_{jitter} \times 2^N)^{-1}$ where t_{jitter} is the RMS aperture uncertainty and 2^N is the desired SNR (signal-to-noise ratio) expressed in total number of quantization levels. A 15-bit SNR, therefore, would be expressed as 2^{15} or 32768. Using the typical PCM1750 aperture jitter of $50ps_{rms}$ and an SNR at the 15-bit level, $f_{MAX} = (2 \times \pi \times 50ps \times 32768)^{-1}$ or 97.1kHz. This matches very closely with the rated dynamic accuracy of the PCM1750 where THD + N = –88dB max. This means the typical aperture jitter of PCM1750 only becomes a factor when input signals to it exceed 97kHz and/or an SNR greater than 15-bits is desired.

Input Bandwidth

The full power bandwidth of the PCM1750 is that input frequency above which significant distortion is observed (THD+N > 10-bits or –60dB for a full scale input signal). In the data sheet, this number is specified as typically being 500kHz. In wideband operation (when no digital filter is used) the additional full power bandwidth of the PCM1750

can be used to purposely alias a band-limited signal down into the baseband of the converter. This technique is called undersampling and can be used to directly down-convert an intermediate frequency riding on a much higher carrier frequency.

DIGITAL I/O AND TIMING

Input/Output Logic Compatibility

Digital logic on the PCM1750 is CMOS compatible. Digital outputs on the PCM1750 are capable of driving a minimum of two standard TTL input loads.

Digital output coding is in binary two's complement. Table I gives the precise input/output voltage/code relationships for the PCM1750. Figure 5 shows these same relationships in a graphical format.

Convert Command and External Clock Input

A conversion is initiated on its positive going edge of the convert command. Although the convert command can return low at any time (prior to 50ns before the rising edge of the 19th clock), a typical convert command pulse width of 81ns (as called out in Figure 3) is specified for a 192kHz sample rate (f_S). The reason for a pulse width spec is to reduce problems associated with digital logic feedthrough noise. The return of convert command to a logic low level in the specified time interferes least with the successive approximation process. Also, it should be noted that putting fast logic edges (<5ns) on convert command (P11) and the external clock input (P4) may cause logic feedthrough to the analog stages in the converter and will result in added distortion during the sampling and conversion process. Using the optional DF1750 digital filter provides adequately slow transitions to maintain full specification performance. If necessary, an external RC, on the convert command line may be used to slow fast logic edges.

As with the convert command, the external clock input is positive edge triggered and is not duty-cycle dependent other than to improve digital feedthrough noise immunity. A 50% duty cycle clock can be used instead of 33% if desired. Refer to Figure 3 for recommended timing relationships. Regardless of what clock duty cycle is used, all operations relating to valid data clocking should be synchronized to the rising edge of the clock input.

Although there is a maximum conversion time called out in the specification table, the PCM1750 can have a considerably longer conversion cycle. Droop of the internal capacitors will ulitmately determine what the true maximum conversion time can be. The min/typ/max times shown in Figure 3 are based on minimum sample rate of 48 kHz, a typical of 192kHz, and a maximum of 222kHz. All specifications are tested at 192kHz. The minimum sample rate assumption is based on clock periods that increase as time between convert commands increases. Any sample rate down to near DC can be utilized by observing maximum clock cycle requirements and spacing convert commands to achieve lower sample rates. This means that the time interval T2 shown in Figure 3 does not have a maximum value.

Clock Lockout

Any number of clocks can be given to the PCM1750 beyond the 19 required for normal operation. If a continuous clock is used, all clocks beyond the 19th are gated off by the PCM1750's internal logic until the next positive going edge of the convert command. The converter also goes into the sample (track) mode starting on the positive edge of the 19th clock until the next positive edge of the convert command, regardless of how many additional clocks are offered. The ideal operation of the converter stops the clock input after the 19th during this critical signal acquisition time. This is the timing shown in Figure 3. The critical timing aspect that must be observed if a clock input other than the recommended is used, is that ample time following the positive edge of convert command proceed the next rising clock edge. If this time is shortened, the most important bit-1 (MSB) decision, which is finalized on the first clock edge after convert command, will be adversely affected. In other words, the clock input cannot have a rising edge during the time interval T3 shown in Figure 3.

SIGNAL-TO-NOISE RATIO

Another specification for A/D converters is signal-to-noise ratio (SNR). For this measurement, a full-scale 1kHz signal is applied and the sampling rate of the PCM1750 is set at 192kHz. An FFT is performed on the digital output and the noise power in the non-harmonic audio-bandwidth frequency bins (20Hz to 24kHz) is summed and expressed in relation to the full-scale input signal.

One advantage of using the PCM1750 in this oversampled mode with the optional DF1750 digital decimation filter is that the converter noise is spread over the full 0Hz to 96kHz passband and then suppressed by the digital filter stopband attenuation (from 24kHz to 96kHz). This effectively increases the SNR of the PCM1750 by 6dB when it is used as an audio bandwidth converter. The other advantage is that the need for a higher-order anti-aliasing input filtering is greatly reduced.

THD + N

The key specification for the PCM1750 is total harmonic distortion plus noise (THD + N). In terms of signal measurement, THD + N is the ratio of $Distortion_{RMS}$ + $Noise_{RMS}$ / $Signal_{RMS}$ expressed in dB. For the PCM1750, THD + N is 100% tested at all three specified input levels using the production test setup shown in Figure 6. For this measurement, as with the SNR test, a full-scale 1kHz signal is applied and the sampling rate of the PCM1750 is set at 192kHz (which is 4X the standard digital audio sample rate of 48kHz). An FFT is performed on the digital output and the total power in all audio-bandwidth frequency bins (20Hz to 24kHz) is summed and expressed in relation to the full-scale input signal.

For the audio band, the THD+N of the PCM1750 is essentially flat for all frequencies and input signal levels. In the *Typical Performance Curves* THD + N versus Frequency plots are shown at four different input signal levels (with and without a 4X decimation filter): 0dB, –20dB, –40dB, and –60dB.

CHANNEL SEPARATION

To test channel separation a 1kHz signal sampled at 192kHz is placed on one input of the PCM1750 while the other input is held at 0V. An FFT is performed on the idle (0V) channel and the result checked to insure that the 1kHz tone is suppressed by a minimum of 96dB.

GAIN AND OFFSET ERRORS

Initial gain and bipolar offset errors are laser trimmed at the wafer level and 100% final tested to insure compliance with the electrical specifications. Bipolar offset errors can be further reduced to zero by using the optional offset adjustment circuitry shown in the connection diagram (Figure 7). Gain errors can be adjusted by varying V_{REF} to either channel of the converter. This is accomplished by either using an adjustable external reference or by placing buffer amplifiers with adjustable gain between $VREF_{OUT}$ and $VREF_{IN}$ as shown in Figure 8a.

INTEGRAL AND DIFFERENTIAL LINEARITY

DC Linearity Testing

The absolute linearity of the PCM1750 is on the order of 15-bits or more as can be seen from the THD versus Frequency plots in the *Typical Performance Curves*. Not every code in the converter must be 15-bit linear to achieve the specified THD + N performance, but a very high percentage will be that linear. The same observation also applies to differential linearity errors in the PCM1750. Because the PCM1750 is not 100% tested for DC linearity specifications, no minimum or maximum specifications are given for integral or differential linearity errors.

No Missing Codes Operation

A no missing codes specification is not given for the PCM1750 for the same reasons as given above. The PCM1750, however, typically has fewer than 16 codes (less than 0.01%) missing at a 14-bit resolution level. A 100% no missing codes specification cannot be maintained above the 12-bit level, although this has very little impact on overall dynamic performance (THD + N). The few missing codes that do occur at higher resolution levels are at the bit-2 and lower major carry transitions of the converter. There are typically no missing codes (at 14-bits) around the critical bipolar zero operation zone (±1/8 of full scale range around bipolar zero or 0V). The critical bipolar differential linearity error can be reduced from its initial value to zero using the optional MSB adjustment circuitry shown in the connection diagram (Figure 7).

REFERENCE

The gain drift of the PCM1750 is primarily due to the drift associated with the reference. Better drift performance can be achieved using an external reference like the ones explained in the applications section (Figures 8b, 8c). The *Typical Performance Curves* plot of V_{REF} Output versus Temperature shows the full range of operation including initial error and typical gain drift. Pertinent performance data are found in the electrical specification table.

Reference Bypass

Both P18 and P25 ($VREF_{IN}$) should be bypassed with a 10µF to 47µF tantalum capacitor. If there are important system reasons for using the PCM1750 reference externally, the outputs of P19 and P24 must be appropriately buffered, and bypassed (see Figure 8).

POWER SUPPLY REJECTION

Because of the architecture of the PCM1750, power supply rejection varies with input signal size. The spec table value is expressed in the relative terms of percent of V_{IN} per

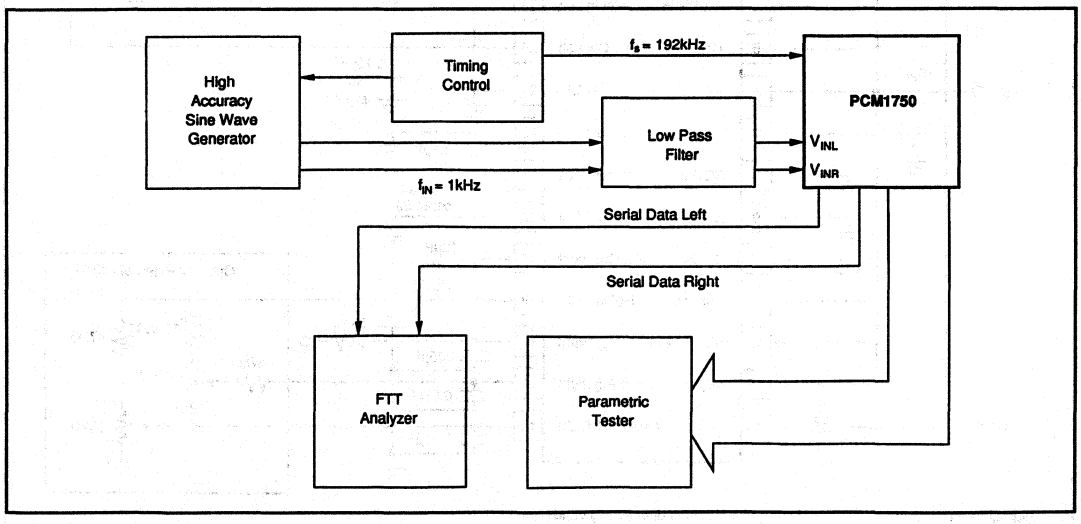


FIGURE 6. PCM1750 Production Test Setup.

percent change of the supply voltage. The PSR versus Frequency plot in the *Typical Performance Curves* show PSR expressed versus an increase in power supply ripple frequency.

PERFORMANCE OVER TEMPERATURE

Specification Temperatures

All critical specifications are tested at 25°C. The drift specification temperature range is from 0°C to +70°C. The PCM1750 will operate over the wider temperature range of –40°C to +85°C.

Gain and Offset Drift

Although the PCM1750 is primarily meant for use in dynamic applications, specifications are also given for more traditional DC drift parameters such as temperature gain and offset drift. The primary cause of drift in the PCM1750 is the bandgap reference. Much lower gain drift can be realized if necessary by using any circuit similar to the external reference circuits shown in Figure 8. Also, refer to the *Typical Performance Curves* of V_{REF} Output versus Temperture.

Dynamic Performance

Dynamic performance is predominated by the absolute linearity of the PCM1750. Because of the excellent ratio tracking versus temperature of poly-poly capacitors, there is virtually no change in dynamic performance of the converter over temperature (primarily THD + N). The dynamic specifications over temperature cannot be guaranteed, however, as they are not 100% tested.

INSTALLATION

ANTI-ALIASING FILTER

To prevent unwanted input signals from being aliased into the passband of the converter, it is necessary to suppress all out of band signals above 1/2 the sampling frequency of the ADC by using a low-pass filter. The requirement for an anti-aliasing filter, however, can be reduced by using oversampling techniques. By raising the sample rate of the converter by a factor of 2 or even 4, the roll off of the anti-aliasing filter can be reduced. In Figure 9, a 6th order, linear-phase, anti-aliasing filter is implemented using low-cost dual audio op amps. This filter will suppress frequencies above 96kHz by 80dB. For many applications a 4th or 2nd order anti-aliasing filter will be adequate when using the PCM1750 in the 4X oversampling mode.

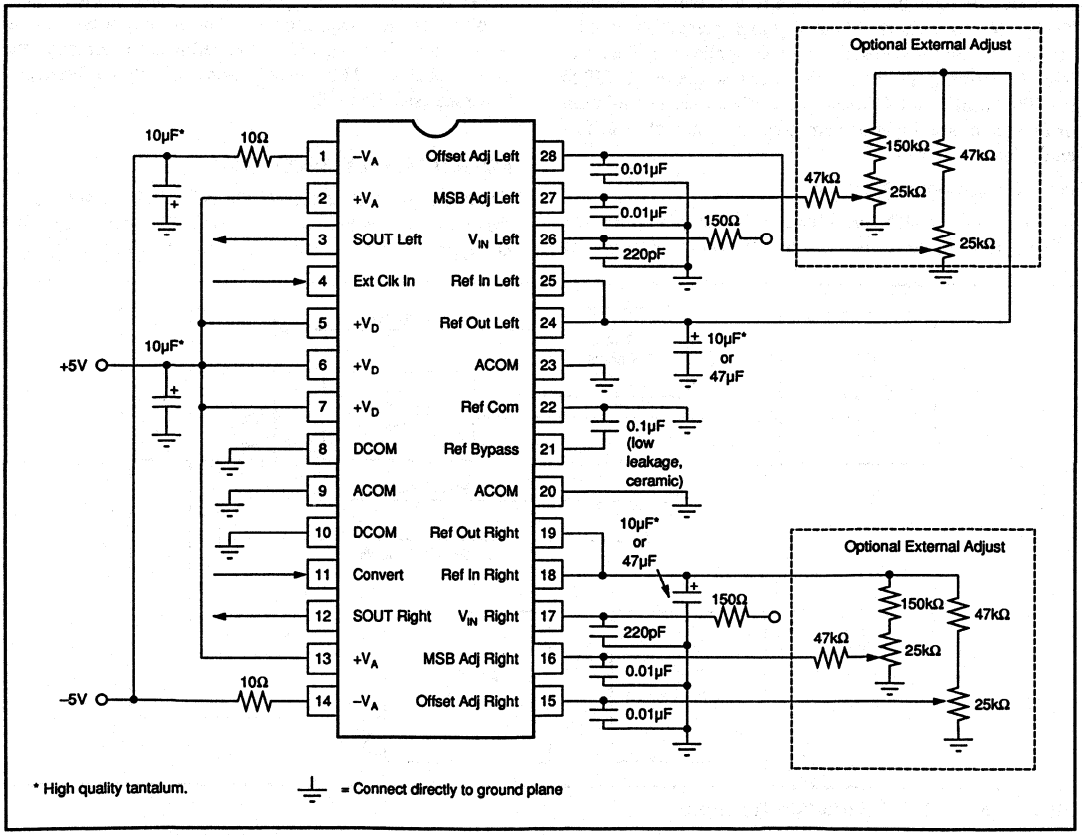


FIGURE 7. PCM1750 Connection Diagram.

INPUT SIGNAL CONDITIONING

RC Input Circuit

Note the 150Ω resistors and 220pF capacitors on each analog input as shown in the connection diagram (Figure 7). This input circuit configuration is required to achieve optimum SNR performance of the PCM1750. Various other component values will yield satisfactory results, but the resistor should never exceed 200Ω.

Buffer Amplifier

To avoid introducing distortion, the PCM1750 input must be driven by a low active impedance source (op amps such as the NE5532, Burr-Brown OPA2604, or equivalent are ideal).

EXTERNAL ADJUSTMENTS

The simplified circuit diagram (see Figure 1) shows one of two complete channels on the PCM1750. The input switched capacitors, trim DAC and comparator are detailed. The trim DAC switches are activated whenever the corresponding bit is chosen during the successive approximation routine. The first 12 bits of the ADC have corresponding trim DAC circuits. The R1a to R12a and R1b to R12b resistors can be laser trimmed at the wafer level if necessary to correct for any nonlinearities. The nominal voltage for the internally generated V_{REF} is 2.75V and it is a relatively low impedance, buffered voltage output. It should be noted that just the act of connecting the optional adjustment circuits will affect the MSB DLEs and bipolar offsets since it is unlikely that the initial potentiometer settings (even if centered) would match the factory trimmed null potentials. If connected, the potentiometers must be properly adjusted.

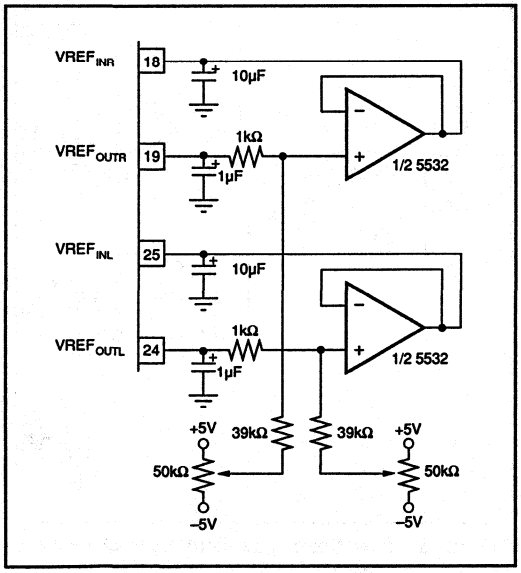


FIGURE 8a. Circuit for External Gain Adjustment Using the Internal Reference.

MSB Adjust

The MSB adjust pin connects to the center of the R1a/R1b resistive divider for bit-1. After laser trimming this point is nominally 100mV. All the MSB and offset adjust pins should be connected to ground using a 0.01µF capacitor, especially if traces to the potentiometers are long. If the adjust pins are not used, they should still be bypassed to ground.

Since there are internal 5kΩ resistors and clamp diodes to both ground and +5V on the MSB and offset adjust pins, there are obvious limits to their range of adjustment. With a nominal internal voltage on these points of +100mV, there will be a greater limitation in making negative adjustments than positive. A negative voltage at either adjustment pin, however, is acceptable up to one diode drop (–0.6V) below ground.

The preferred method of MSB DLE adjustment is to input a small level signal and adjust for minimum THD + N.

Offset Adjust

The offset adjust switch (S_{OFF}) position is controlled by whether the ADC is in the sample or hold mode. Switching from sample to hold effectively allows any charge offsets associated with the sampling process to be eliminated. Grounding the input to the converter as far ahead of the A/D as possible (in front of the anti-aliasing filter for example) and then adjusting the bipolar zero error will remove the offsets associated with the entire sampling system.

LAYOUT CONSIDERATIONS

Power Requirements

Noise on the power supply lines can degrade converter performance, especially noise and spikes from a switching power supply. Appropriate supplies or filters must be used. Although the PCM1750 positive supplies have separate digital and analog +5V, for most applications the +5V digital supply pins should be connected to the +5V analog supply. If they aren't connected together, a potential latchup condition can occur when the power supplies are not turned on at the same time. If one supply pin is powered and the other is not, the PCM1750 may latch up and draw excessive current. In normal operation, this is not a problem because both $+V_A$ and $+V_D$ should be connected together. However, during evaluation, incoming inspection, repair, etc., where the potential of a "hot" socket exists, care should be taken to power the PCM1750 only after it has been socketed.

All supplies should be bypassed as shown in Figure 7. The bypass capacitors should placed as close to their respective supply pins as possible. Additional .01µF capacitors may be placed in parallel with the larger value capacitors to increase high-frequency rejection, but generally they are not required when high quality tantalums are used. The 0.1µF capacitor between P21 and P22 should be a low leakage type (such as ceramic) and must be put as close to these pins as possible to reduce noise pickup.

The PCM1750 is sensitive to supply voltages outside the absolute maximum ratings shown in the specification tables. Do not exceed –8V on the negative supplies at any time or irreversible damage may occur. Note the 10Ω resistors in series with each –5V supply line (shown in Figure–7) to help protect the part from severe damage if the supplies are over-ranged momentarily.

Grounding Requirements

Because of the high resolution and linearity of the PCM1750, system design problems such as ground path resistance and contact resistance become very important.

The ACOM and DCOM pins are separated internally on the PCM1750. To eliminate unwanted ground loops, all commons (both analog and digital) should be connected to the same low-impedance ground plane. This should be an analog ground plane separate from other high-frequency digital ground planes on the same board. If the analog and digital commons of the PCM1750 are connected to different ground planes, care should be taken to keep them within 0.6V of each other to insure proper operation of the converter.

A ground plane is usually the best solution for preserving dynamic performance and reducing noise coupling into sensitive converter circuits. Where any compromises must be made, the common return of the analog input signals should be referenced to the ACOM pins. This will prevent voltage drops in the power supply returns from appearing in series with the input signal.

Coupling between analog input and digital lines should be minimized by careful layout. For instance, if the lines must cross, they should do so at right angles. Parallel analog and digital lines should be separated from each other by a pattern connected to common.

If external MSB and offset adjust potentiometers are used, the potentiometers and related resistors should be located as close to the PCM1750 as possible.

Minimizing "Glitches"

Coupling of external transients into an analog-to-digital converter can cause errors which are difficult to debug. Care should be taken to avoid glitches during critical times in the sampling and conversion process. Since the PCM1750 has an internal sample/hold function, the signal that switches it into the HOLD state (CONVERT going HIGH) is critical, as it would be on any sample/hold amplifier. The CONVERT rising edge should have minimal ringing, especially during the 20ns after it rises.

APPLICATIONS

USING A DIGITAL FILTER

A 4X decimation filter is available for the PCM1750 called the DF1750. It is available in a 28-pin DIP or a 40-pin SOIC package. The use of this filter greatly eases the implementation of the PCM1750 in audio band applications.

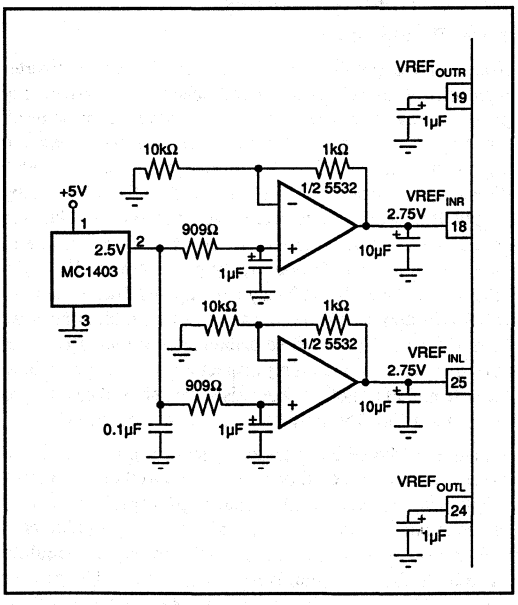


FIGURE 8b. External Reference Circuit Using Standard 2.5V Reference.

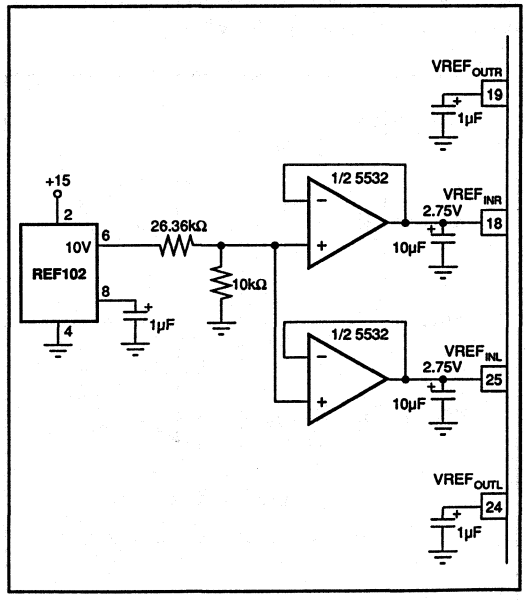


FIGURE 8c. Low Noise, Low Drift External Reference Circuit.

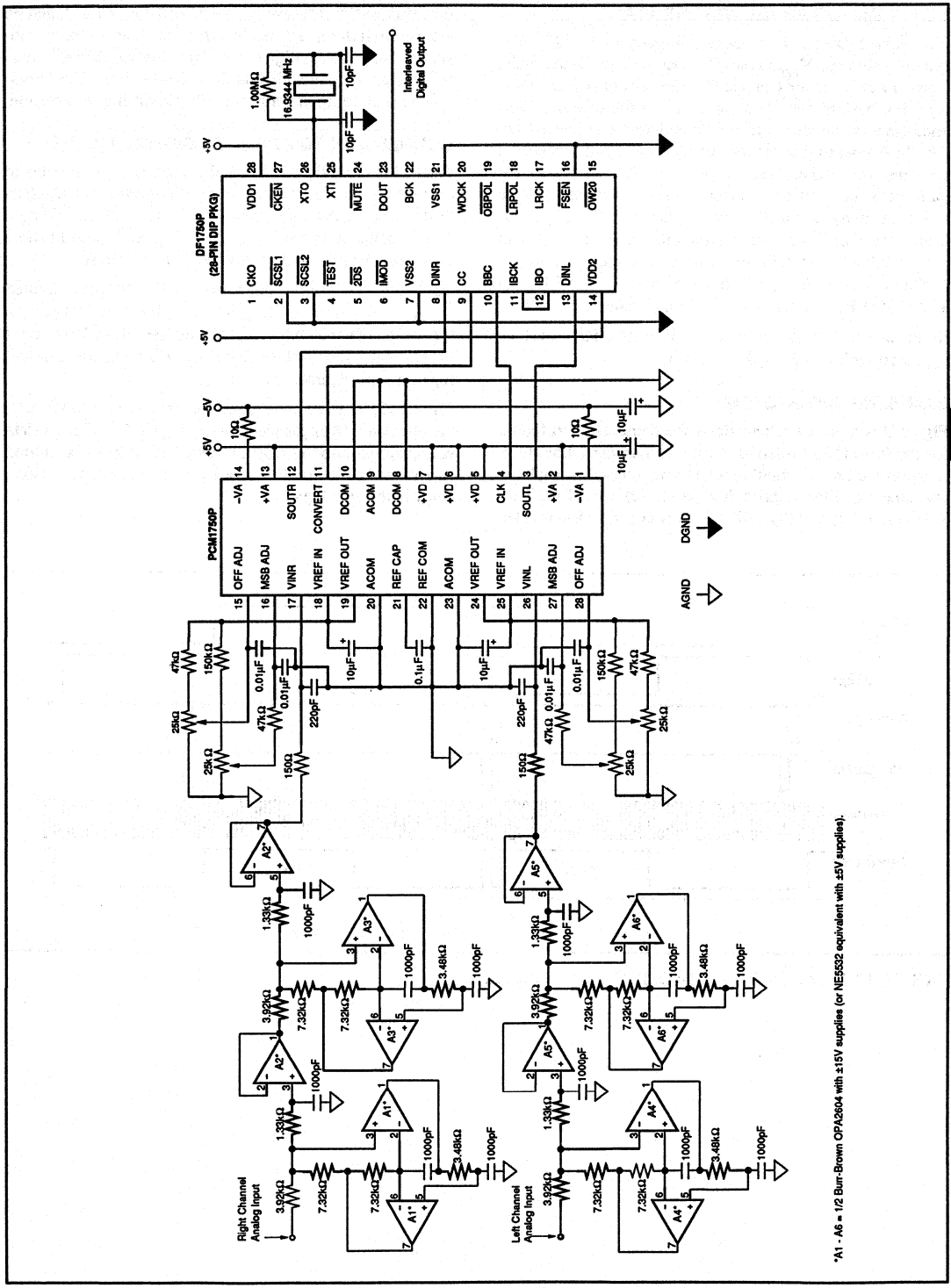


FIGURE 9. Complete Sampling A/D Circuit with Anti-aliasing and Digital Filter, (44.1kHz output data rate).

USING AN EXTERNAL REFERENCE

Normally $VREF_{OUT}$ is connected directly to $VREF_{IN}$. The typical value for V_{REF} versus Temperature is shown in the *Typical Performance Curves*. If better drift or power supply rejection performance is desired, one of the external reference circuits shown in Figures 8b and 8c can be used. Note that the decoupling capacitors are still connected to $VREF_{IN}$. External gain adjustment is now possible by using the variable output options available on some precision voltage references or by varying the gain on external buffer amplifiers. The range of acceptable external references is from +2.0V to $+V_A$ – 2.0V, with 2.5V types being the most commonly available. Full scale input voltage range will be $\pm VREF_{IN}$ (a +2.5V $VREF_{IN}$ results in a ±2.5V input range).

If an external reference is used, P19 and P24 must be bypassed with at least 1µF capacitors.

SAMPLING A/D SYSTEM

Figure 9 is a partial schematic of the demonstration fixture for the PCM1750 (orderable by model number DEM1133). It shows the implementation of (1) a 6th order, linear-phase, anti-aliasing filter (22kHz low-pass); (2) the PCM1750P A/D converter; and (3) a 4X digital decimation filter called the DF1750P. Not shown on this schematic, but included on the demo fixture, are latched parallel data outputs with strobe and a serial digital interface format (SPDIF) data transmitter. Also included on the DEM1133 are user breadboard areas for application specific circuit implementation.

CONNECTION TO DSP WITH DIGITAL FILTER

The PCM1750 and DF1750 combination can be connected to the serial ports of most popular DSP processor ICs (such as those made by AT&T, Motorola, TI, and AD) by adding a small amount of external glue logic. Figures 10 and 11 show the timing diagram and schematic for this interface.

To use this interface, the DSP processor IC must be configured for 32 bit word inputs. The glue logic generates a flag bit, as the first bit of the 32 bit word, that signifies either left or right channel data. The flag bit will be low for left channel data and high for right channel data.

The DF1750 can be configured for either 16 or 20 bit data, although only 16 bit data is shown in Figure 10. After the data is transferred into the DSP processor IC, it must be shifted toward the LSB by one bit in order to compensate for a clock delay in the glue logic.

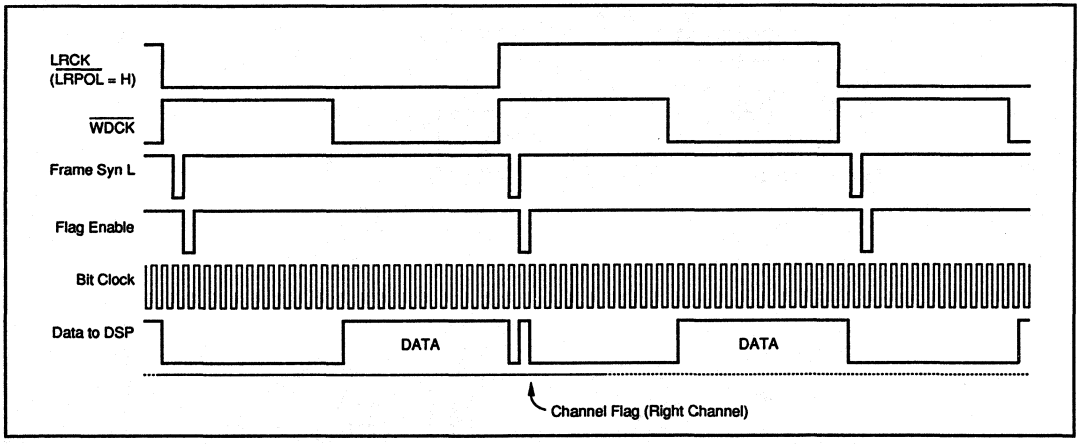


FIGURE 10. PCM1750/DF1750 To DSP IC Timing Diagram.

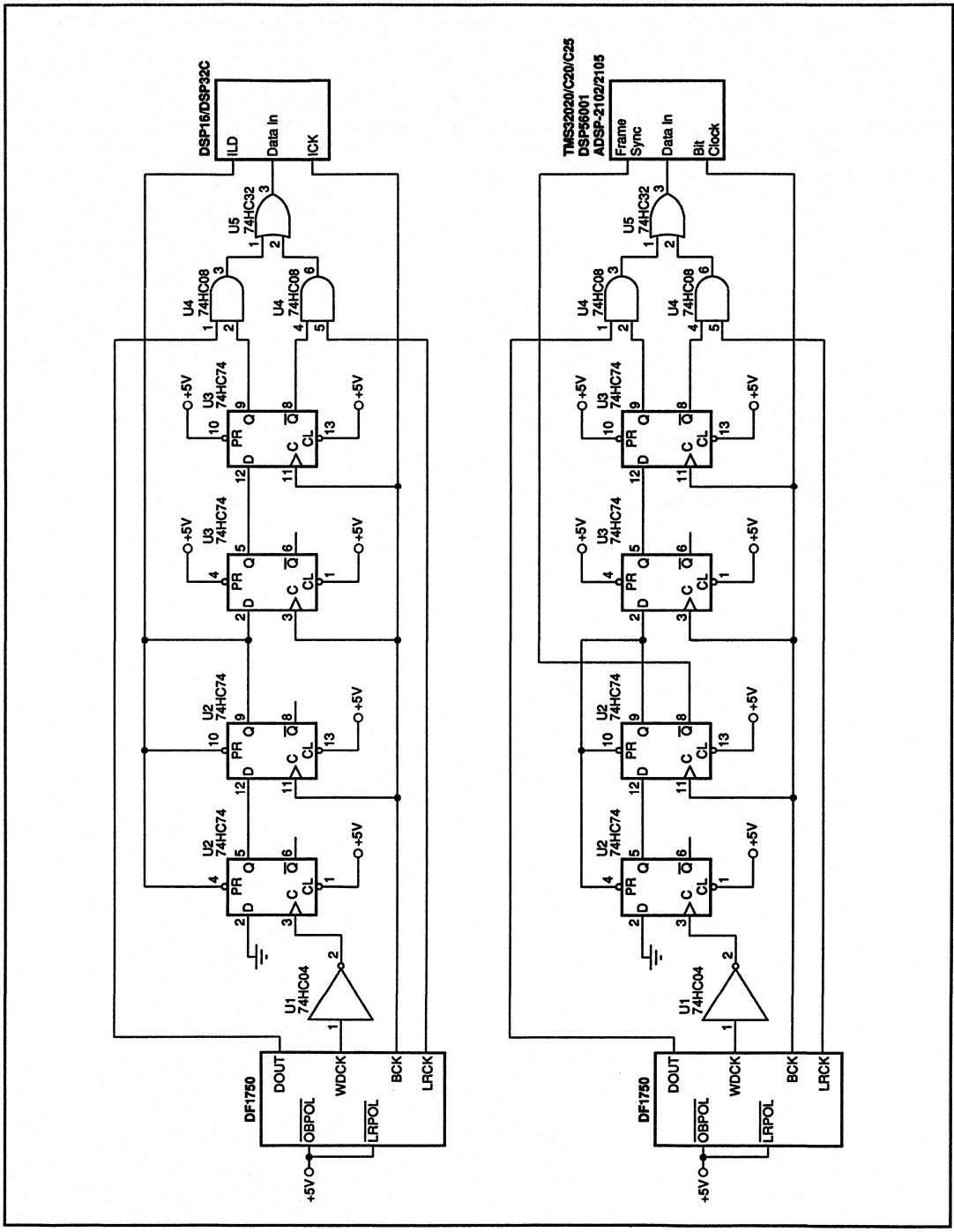


FIGURE 11. PCM1750/DF1750 to DSP IC Schematic.

7 Analog Multiplexers

Use Burr-Brown analog multiplexers to realize a very low cost-per-channel solution to multiple-channel data conversion or analog distribution systems designs. Two types are offered—a low-cost, high-quality family of devices ranging from 4 to 16 channels that can accommodate either single-ended or differential signals, and a very fast switching family, single-ended or differential, for high-throughput rate applications. All are TTL- and CMOS-compatible, have input protection in excess of the maximum power supply voltages, and can be operated singly or in multi-tiered matrices.
The Selection Guide shows parameters for all grades. Models shown in **boldface** are products included in this supplement.

ANALOG MULTIPLEXERS

Description	Model	Channels	Input Range (V)	On Resistance max (Ω)	Settling Time (to 0.01%)	Temp Range[1]	Pkg[2]	Page No.[3]
Protected Inputs	HI3-0506A-5	16-channel single ended	±15	1.8k	3.5µs	Com	28-p PDIP	7-3
	HI1-0506A-5	16-channel single ended	±15	1.8k	3.5µs	Com	28-p CDIP	7-3
	HI1-0506A-2	16-channel single ended	±15	1.5k	3.5µs	Mil	28-p CDIP	7-3
	HI3-0507A-5	8-channel differential	±15	1.8k	3.5µs	Com	28-p PDIP	7-3
	HI1-0507A-5	8-channel differential	±15	1.8k	3.5µs	Com	28-p CDIP	7-3
	HI1-0507A-2	8-channel differential	±15	1.5k	3.5µs	Mil	28-p CDIP	7-3
	HI3-0508A-5	8-channel single ended	±15	1.8k	3.5µs	Com	16-p PDIP	7-13
	HI1-0508A-5	8-channel single ended	±15	1.8k	3.5µs	Com	16-p CDIP	7-13
	HI1-0508A-2	8-channel single ended	±15	1.5k	3.5µs	Mil	16-p CDIP	7-13
	HI3-0509A-5	4-channel differential	±15	1.8k	3.5µs	Com	16-p PDIP	7-13
	HI1-0509A-5	4-channel differential	±15	1.8k	3.5µs	Com	16-p CDIP	7-13
	HI1-0509A-2	4-channel differential	±15	1.5k	3.5µs	Mil	16-p CDIP	7-13
High Speed	MPC800KG	16 single or 8 differential	±15	750	800ns	Com	CDIP	7-23
	MPC801KG	8 single or 4 differential	±15	750	800ns	Com	CDIP	7-30
	MPC801KG	8 single or 4 differential	±15	750	800ns	Com	CDIP	7-30
	MPC801SG	8 single or 4 differential	±15	700	800ns	Mil	CDIP	7-30

NOTES: (1) Temperature Range: Com = 0°C to +70°C, Mil = –55°C to +125°C. (2) CDIP = Ceramic DIP, PDIP = Plastic DIP. (3) Burr-Brown IC Data Book, Volume 33.

MODELS STILL AVAILABLE BUT NOT FEATURED IN THIS BOOK

MPC16S
MPC4D
MPC8S
MPC8D

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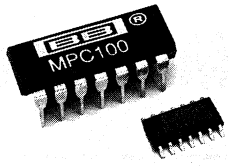


MPC100

Wide Bandwidth 4 X 1 VIDEO MULTIPLEXER

FEATURES

- LARGE SIGNAL BANDWIDTH: 100MHz (2.8Vp-p)
- LOW INTERCHANNEL CROSSTALK: ≤70dB (30MHz, DIP); ≤60dB (30MHz, SO)
- LOW SWITCHING TRANSIENTS: +2.5/–1.2mV
- LOW DIFFERENTIAL GAIN/PHASE ERRORS: 0.05%, 0.01°
- LOW QUIESCENT CURRENT: One Channel Selected: ±4.6mA No Channel Selected: ±230µA

APPLICATIONS

- VIDEO ROUTING AND MULTIPLEXING (CROSSPOINTS)
- RADAR SYSTEMS
- DATA ACQUISITION
- INFORMATION TERMINALS
- SATELLITE OR RADIO LINK IF ROUTING

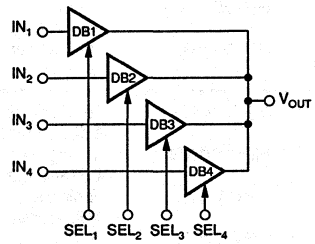
DESCRIPTION

The MPC100 is a very wide bandwidth 4 to 1 channel Video Signal Multiplexer, which can be used in a wide variety of applications.

It was designed for wide-bandwidth systems, including high-definition television and broadcast equipment. Although it is primarily used to route video signals, the harmonic and dynamic attributes of the MPC100 make it appropriate for other analog signal routing applications such as radar, communications, computer graphics, and data acquisition systems.

The MPC100 consists of four identical monolithic integrated open-loop buffer amplifiers, which are connected together internally at the output. The bipolar complementary buffers form a unidirectional transmission path and offer extremely high output-to-input isolation. The MPC100 multiplexer enables the user to connect any one of the four input channels (IN_1 - IN_4) to the output. The output of the multiplexer is in a high-impedance state when no channel is selected. When one channel is selected with a digital "1" at the corresponding SEL-input, the component acts as a buffer with high input impedance and low output impedance.

The wide bandwidth of over 100MHz at 2.8Vp-p signal level, high linearity and low distortion, and low input voltage noise of $4nV/\sqrt{Hz}$ make this crosspoint switch suitable for RF and video applications. All performance is specified with ±5V supply voltage, which reduces power consumption in comparison with ±15V designs. The multiplexer is available in a space-saving 14-pin SO and cost-saving DIP packages. Both are designed and specified for operation over the industrial temperature range (–40°C to +85°C.)



TRUTH TABLE

SEL_1	SEL_2	SEL_3	SEL_4	V_{OUT}
0	0	0	0	HI-Z
1	0	0	0	IN_1
0	1	0	0	IN_2
0	0	1	0	IN_3
0	0	0	1	IN_4

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Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

PDS-1133

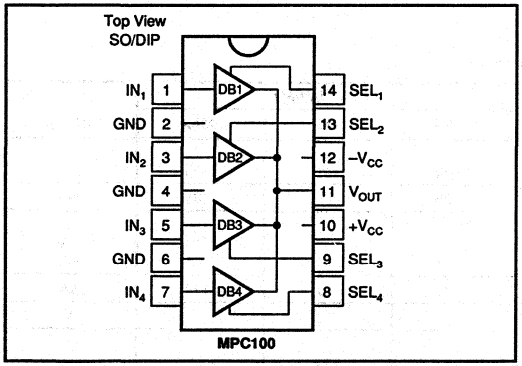
SPECIFICATIONS

ELECTRICAL

At V_{CC} = ±5VDC, R_L = 10kΩ, R_{SOURCE} = 50Ω, and T_A = +25°C, unless otherwise noted.

PARAMETER	CONDITIONS	MPC100AP/AU MIN	MPC100AP/AU TYP	MPC100AP/AU MAX	UNITS
DC CHARACTERISTICS					
INPUT OFFSET VOLTAGE					
Initial		–30	±3	+30	mV
vs Temperature			30		µV/°C
vs Supply (Tracking)	V_{CC} = ±4.5V to ±5.5V	–40	–80		dB
vs Supply (Non-tracking)	V_{CC} = +4.5V to +5.5V		–50		dB
vs Supply (Non-tracking)	V_{CC} = –4.5V to –5.5V		–50		dB
INPUT BIAS CURRENT					
Initial		–10	±3	+10	µA
vs Temperature			20		nA/°C
vs Supply (Tracking)	V_{CC} = ±4.5V to ±5.5V		±380		nA/V
vs Supply (Non-tracking)	V_{CC} = +4.5V to +5.5V		+1.0		µA/V
vs Supply (Non-tracking)	V_{CC} = –4.5V to –5.5V		–11.0		µA/V
INPUT IMPEDANCE					
Resistance	Channel On		0.88		MΩ
Capacitance	Channel On		1.0		pF
Capacitance	Channel Off		1.0		pF
INPUT NOISE					
Voltage Noise Density	f_{OUT} = 20kHz to 10MHz		4.0		nV/√Hz
Signal-to-Noise Ratio	S/N = 0.7/V_N • √5MHz		–98		dB
INPUT VOLTAGE RANGE	Gain Error = 10%		±4.2		V
TRANSFER CHARACTERISTICS	Voltage Gain				
	R_L = 1kΩ, V_{IN} = ±2V		0.982		V/V
	R_L = 10kΩ, V_{IN} = ±2V	0.98	0.992		V/V
RATED OUTPUT					
Voltage	G ≥ 0.97, R_L = 5kΩ	±2.8	±3.8		V
Resistance	One Channel Selected		11		Ω
Resistance	No Channel Selected		900		MΩ
Capacitance	No Channel Selected		1.5		pF
POWER SUPPLY					
Rated Voltage			±5		V
Derated Performance		±4.5		±5.5	V
Quiescent Current	One Channel Selected		±4.6		mA
	No Channel Selected		±230	±350	µA
Rejection Ratio			–80		dB

CONNECTION DIAGRAM



MPC100

FUNCTIONAL DESCRIPTION

IN_1-IN_4	Four analog input channels
GND	Analog input shielding grounds, not internally connected
SEL_1-SEL_4	Channel selection inputs
V_{OUT}	Analog output; tracks selected channel
$-V_{CC}$	Negative supply voltage; typical –5VDC
$+V_{CC}$	Positive supply voltage; typical +5VDC

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SPECIFICATIONS

ELECTRICAL

At V_{CC} = ±5VDC, R_L = 10kΩ, R_{SOURCE} = 50Ω, and T_A = +25°C; unless otherwise noted.

PARAMETER	CONDITIONS	MPC100AP/AU MIN	MPC100AP/AU TYP	MPC100AP/AU MAX	UNITS
AC CHARACTERISTICS					
FREQUENCY DOMAIN					
LARGE SIGNAL BANDWIDTH (–3dB)	V_O = 5.0Vp-p, C_{OUT} = 1pF		55		MHz
	V_O = 2.8Vp-p, C_{OUT} = 1pF		100		MHz
	V_O = 1.4Vp-p, C_{OUT} = 1pF		250		MHz
SMALL SIGNAL BANDWIDTH	V_O = 0.2Vp-p, C_{OUT} = 1pF		390		MHz
GROUP DELAY TIME			450		ps
DIFFERENTIAL GAIN	f = 4.43MHz, V_{IN} = 0.3Vp-p				
	VDC = 0 to 0.7V		0.05		%
	VDC = 0 to 1.4V		0.06		%
DIFFERENTIAL PHASE	f = 4.43MHz, V_{IN} = 0.3Vp-p				
	VDC = 0 to 0.7V		0.01		Degrees
	VDC = 0 to 1.4V		0.02		Degrees
GAIN FLATNESS PEAKING	V_O = 0.2Vp-p, DC to 30MHz		0.04		dB
	V_O = 0.2Vp-p, 30MHz to 100MHz		0.05		dB
HARMONIC DISTORTION	f = 30MHz, V_O = 1.4Vp-p, R_L = 1kΩ				
Second Harmonic			–53		dBc
Third Harmonic			–67		dBc
CROSSTALK	V_I = 1.4Vp-p, Figures				
MPC100AP All Hostile	f = 5MHz,		–82		dB
	f = 30MHz,		–70		dB
Off Isolation	f = 5MHz,		–70		dB
	f = 30MHz,		–71		dB
MPC100AU All Hostile	f = 5MHz,		–78		dB
	f = 30MHz,		–60		dB
Off Isolation	f = 5MHz,		–75		dB
	f = 30MHz		–76		dB
TIME DOMAIN					
RISE TIME	V_O = 1.4Vp-p, Step 10% to 90%				
	C_{OUT} = 1pF, R_{OUT} = 22Ω		3.3		ns
SLEW RATE	V_O = 2Vp-p				
	C_{OUT} = 1pF		650		V/µs
	C_{OUT} = 22pF		460		V/µs
	C_{OUT} = 47pF		320		V/µs

SPECIFICATIONS

ELECTRICAL (FULL TEMPERATURE RANGE)

At V_{CC} = ±5VDC, R_L = 10kΩ, R_{SOURCE} = 50Ω, and T_A = T_{MIN} to T_{MAX}, unless otherwise noted.

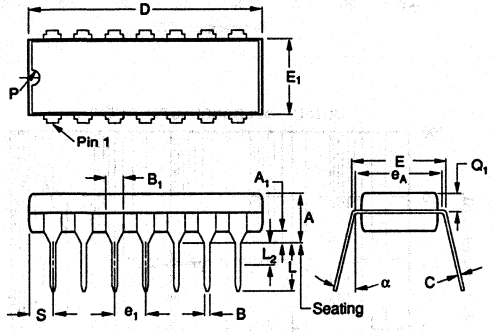
PARAMETER	CONDITIONS	MPC100AP/AU MIN	MPC100AP/AU TYP	MPC100AP/AU MAX	UNITS
TEMPERATURE RANGE					
Specification: AP, AU	Ambient Temperature	–40	+25	+85	°C
OFFSET VOLTAGE		–35	±5	+35	mV
TRANSFER CHARACTERISTICS	Voltage Gain				
	R_L = 1kΩ				V/V
	R_L = 10kΩ	0.95	0.992	0.997	V/V
INPUT BIAS CURRENT		–10	+3	+10	µA
INPUT VOLTAGE RANGE					V
RATED OUTPUT					
Voltage Output	G ≥ 0.90, R_L = 5kΩ	±2.8	±3.8	±4	V
POWER SUPPLY					
Quiescent Current	One Channel Selected		±4.6	±5.5	mA
	No Channel Selected		±230	±320	µA
SELECTION INPUTS					
Logic 1 Current	V_{SEL} = 5.0V		+100	140	µA
Logic 0 Current	V_{SEL} = 0.8V		+0.002	5	µA

CHANNEL SELECTION

PARAMETER	CONDITIONS	MPC100AP/AU MIN	MPC100AP/AU TYP	MPC100AP/AU MAX	UNITS
SELECTION INPUTS					
Logic 1 Voltage		+2.0		V_{CC} +0.6	V
Logic 0 Voltage		0		+0.8	V
Logic 1 Current	V_{SEL} = 5.0V	+75	+100	+125	µA
Logic 0 Current	V_{SEL} = 0.8V	0	+0.6	+5	µA
SWITCHING CHARACTERISTICS	V_I = –0.3V to +0.7V, f = 5MHz				
SEL to Channel ON Time	90% Point of V_O = 1Vp-p		0.25		µs
SEL to Channel OFF Time	10% Point of V_O = 1Vp-p		0.25		µs
Switching Transient, Positive	Measured While Switching		+2.5		mV
Switching Transient, Negative	Between Two Grounded Channels		–1.2		mV

MECHANICAL

P Package — 14-Pin Plastic DIP



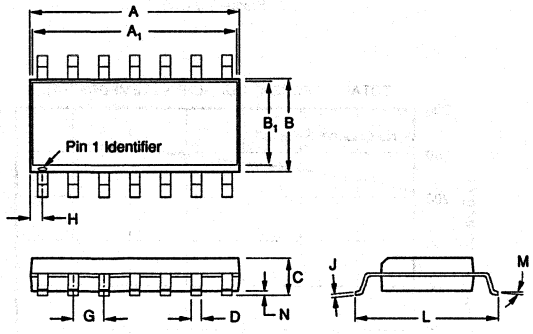
DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.120	.160	3.048	4.064
A1	.015	.065	.381	1.651
B	.014	.020	.355	.508
B1	.050	.065	1.270	1.651
C	.008	.012	.203	.304
D	.745	.770	18.923	19.558
E	.300	.325	7.620	8.255
E1	.240	.260	6.096	6.604
e1	.100 BASIC		2.540 BASIC	
eA	.300 BASIC		7.620 BASIC	
L	.125	.150	3.175	3.810

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
L2 (4)	0	.030	0	.762
α	0°	15°	0°	15°
N (1)	14		14	
N1 (2)	0		0	
P	—	.050	—	1.270
Q1	.050	.085	1.270	2.159
S (3)	.065	.090	1.651	2.286

(1) N = Total number of pins.
(2) N_1 = Total number of missing pins.
(3) Not per JEDEC Std.
(4) e_1 and e_A applies in zone L_2 when unit installed.

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

U Package — 14-Pin SOIC



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.332	.348	8.44	8.84
A1	.325	.348	8.26	8.84
B	.146	.162	3.71	4.11
B1	.128	.146	3.25	3.71
C	.052	.068	1.32	1.73
D	.014	.019	0.36	0.48
G	.050 BASIC		1.27 BASIC	
H	.016	.024	0.41	0.61
J	.008	.012	0.20	0.30
L	.226	.246	5.74	6.25
M	5° TYP		5° TYP	
N	.000	.012	0.00	0.30

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage (±V_{CC})	±6VDC
Analog Input Voltage (IN_1 through IN_4)	±V_{CC}, ±0.7V
Operating Temperature	–40°C to +85°C
Storage Temperature	–40°C to +125°C
Output Current	±6mA
Junction Temperature	+150°C
Lead Temperature (soldering, 10s)	+300°C
Digital Input Voltages (SEL_1 through SEL_4)	–0.5V to +V_{CC} +0.7V

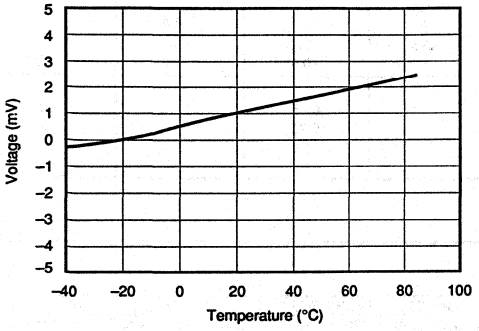
ORDERING INFORMATION

MODEL	DESCRIPTION	TEMPERATURE RANGE
MPC100AP	Plastic 14-Pin DIP	–40°C to +85°C
MPC100AU	SO 14-Pin Surface Mount	–40°C to +85°C

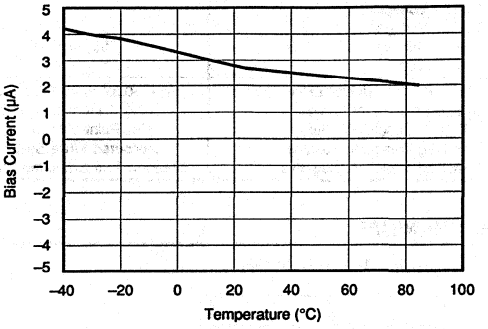
TYPICAL PERFORMANCE CURVES

At V_{CC} = ±5VDC, R_{LOAD} = 10kΩ, R_{SOURCE} = 50Ω, and T_A = +25°C, unless otherwise noted.

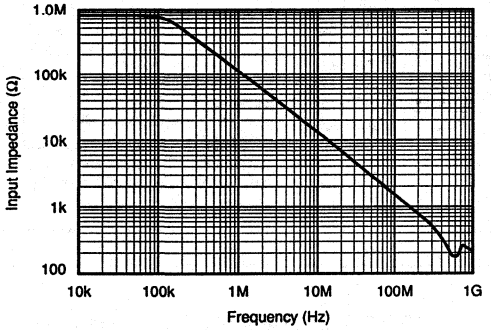
OFFSET VOLTAGE vs TEMPERATURE



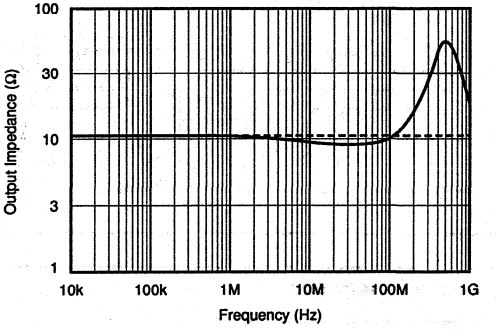
INPUT BIAS CURRENT vs TEMPERATURE



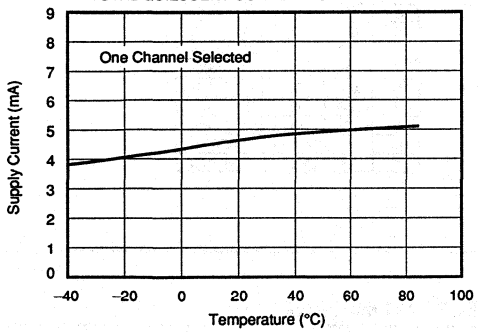
INPUT IMPEDANCE vs FREQUENCY



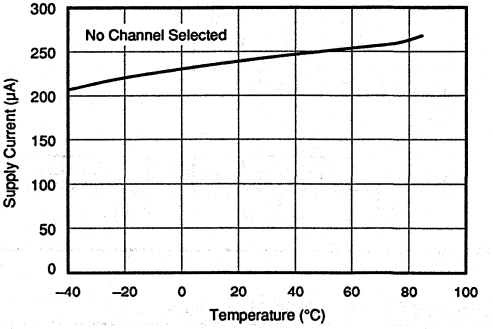
OUTPUT IMPEDANCE vs FREQUENCY



TOTAL QUIESCENT CURRENT vs TEMPERATURE



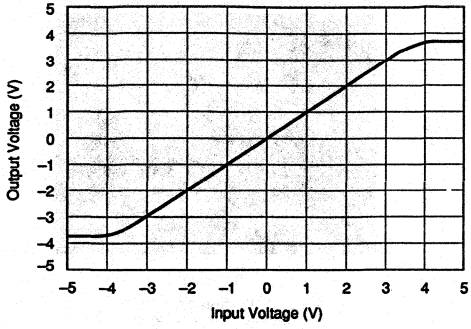
TOTAL QUIESCENT CURRENT vs TEMPERATURE



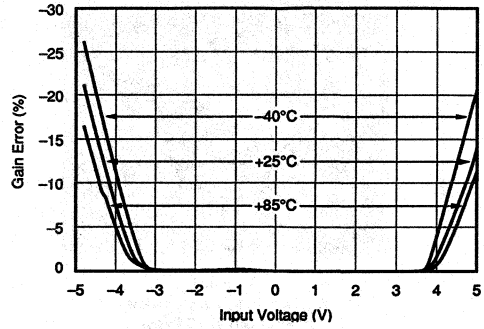
TYPICAL PERFORMANCE CURVES (CONT)

At V_{CC} = ±5VDC, R_{LOAD} = 10kΩ, R_{SOURCE} = 50Ω, and T_A = +25°C, unless otherwise noted.

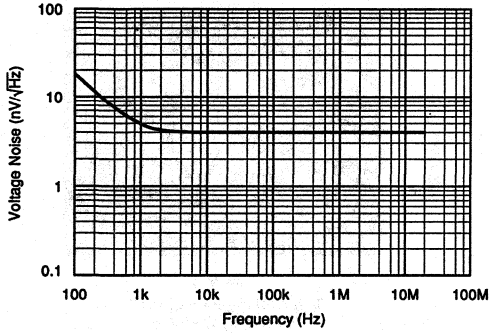
TRANSFER FUNCTION



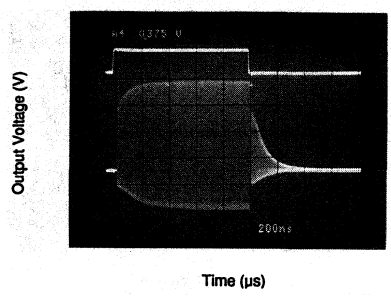
GAIN ERROR vs INPUT VOLTAGE



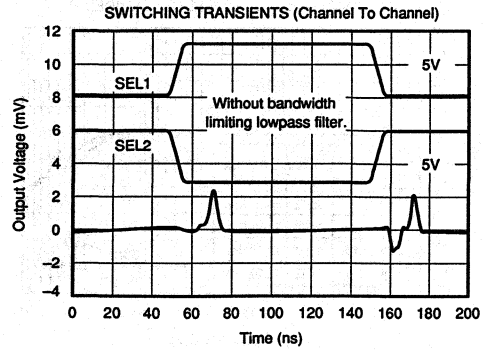
INPUT VOLTAGE NOISE SPECTRAL DENSITY



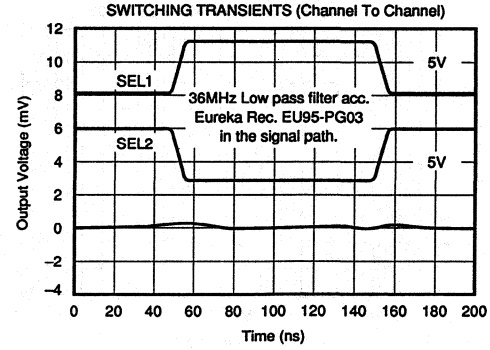
SWITCHING ENVELOPE



SWITCHING TRANSIENTS (Channel To Channel)



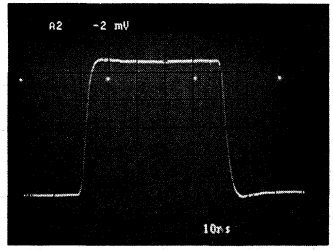
SWITCHING TRANSIENTS (Channel To Channel)



TYPICAL PERFORMANCE CURVES (CONT)

At V_{CC} = ±5VDC, R_{LOAD} = 10kΩ, R_{SOURCE} = 50Ω, and T_A = +25°C, unless otherwise noted.

SMALL SIGNAL PULSE RESPONSE

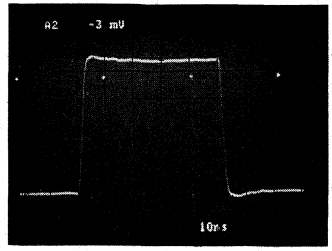


Output Voltage (mV)

Time (ns)

C_{OUT} = 1pF, t_{RISE} = t_{FALL} = 2ns
(Generator) V_I = 0.2Vp-p

SMALL SIGNAL PULSE RESPONSE

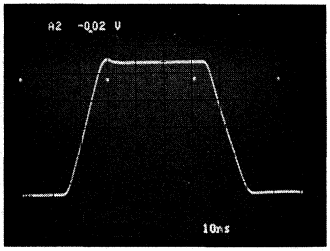


Output Voltage (mV)

Time (ns)

C_{OUT} = 47pF, t_{RISE} = t_{FALL} = 2ns
(Generator) V_I = 0.2Vp-p

LARGE SIGNAL PULSE RESPONSE

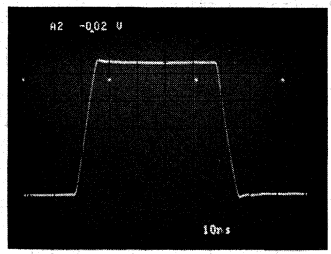


Output Voltage (mV)

Time (ns)

C_{OUT} = 47pF, t_{RISE} = t_{FALL} = 5ns
(Generator) V_I = 5Vp-p

LARGE SIGNAL PULSE RESPONSE

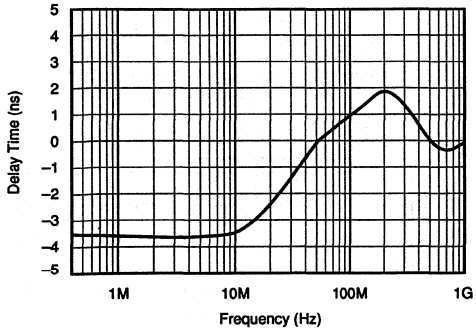


Output Voltage (mV)

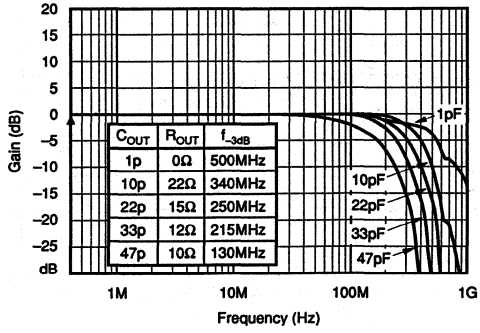
Time (ns)

C_{OUT} = 1pF, t_{RISE} = t_{FALL} = 5ns
(Generator) V_I = 5Vp-p

GROUP DELAY TIME vs FREQUENCY



BANDWIDTH vs C_{OUT} WITH RECOMMENDED R_{OUT}

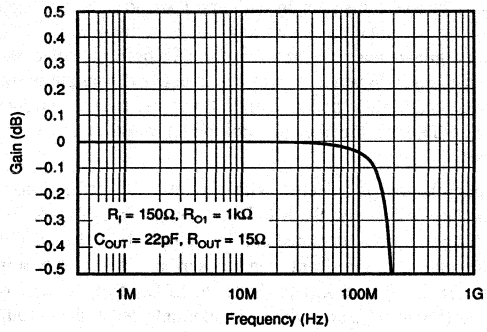


C_{OUT}	R_{OUT}	f_{-3dB}
1p	0Ω	500MHz
10p	22Ω	340MHz
22p	15Ω	250MHz
33p	12Ω	215MHz
47p	10Ω	130MHz

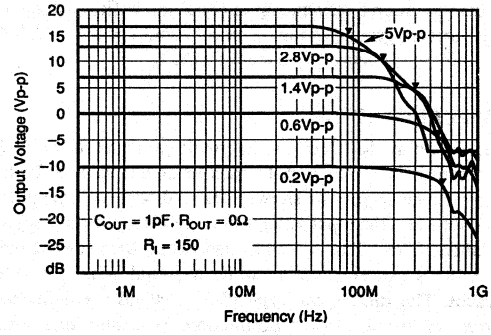
TYPICAL PERFORMANCE CURVES (CONT)

At V_{CC} = ±5VDC, R_{LOAD} = 10kΩ, R_{SOURCE} = 50Ω, and T_A = +25°C, unless otherwise noted.

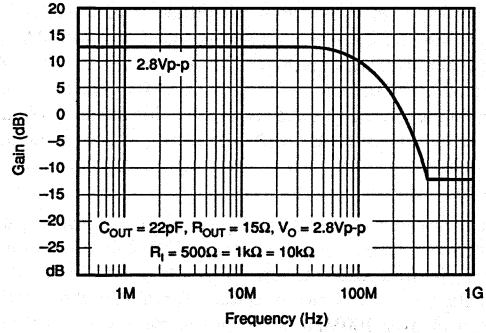
GAIN FLATNESS



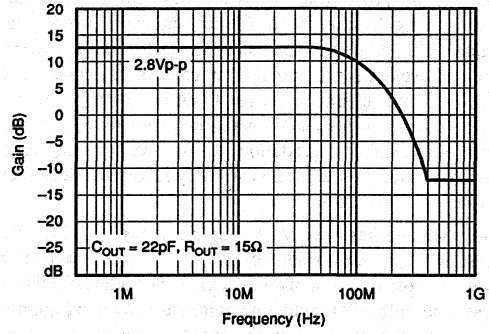
BANDWIDTH vs OUTPUT VOLTAGE



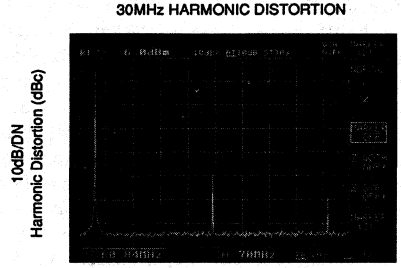
BANDWIDTH vs R_{LOAD}



BANDWIDTH MATCHING (DB1...DB4)



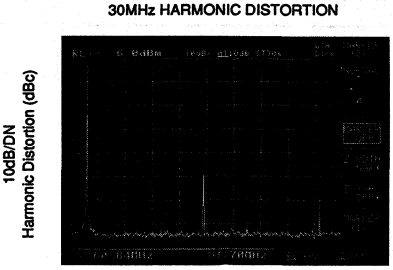
30MHz HARMONIC DISTORTION



Frequency (Hz)

V_{OUT} = 2.8Vp-p, R_L = 1kΩ, C_{OUT} = 1pF

30MHz HARMONIC DISTORTION



Frequency (Hz)

V_{OUT} = 2.8Vp-p, R_L = 10Ωk, C_{OUT} = 1pF

APPLICATIONS INFORMATION

The MPC100 operates from ±5V power supplies (±6V maximum). Do not attempt to operate with larger power supply voltages or permanent damage may occur. The buffer outputs are not current-limited or protected. If the output is shorted to ground, currents up to 18mA could flow. Momentary shorts to ground (a few seconds) should be avoided, but are unlikely to cause permanent damage.

INPUT PROTECTION

All pins on the MPC100 are internally protected from ESD by means of a pair of back-to-back reverse-biased diodes to either power supply as shown. These diodes will begin to conduct when the input voltage exceeds either power supply by about 0.7V. This situation can occur with loss of the amplifier's power supplies while a signal source is still present. The diodes can typically withstand a continuous current of 30mA without destruction. To insure long term reliability, however, diode current should be externally limited to 10mA or so whenever possible.

The internal protection diodes are designed to withstand 2.5kV (using Human Body Model) and will provide adequate ESD protection for most normal handling procedures. However, static damage can cause subtle changes in amplifier input characteristics without necessarily destroying the device. In precision operational amplifiers, this may cause a noticeable degradation of offset voltage and drift. Therefore, static protection is strongly recommended when handling the MPC100.

Static damage has been well recognized for MOSFET devices, but any semiconductor device deserves protection from this potentially damaging source. The MPC100 incorporates on-chip ESD protection diodes as shown in Figure 1. This eliminates the need for the user to add external protection diodes, which can add capacitance and degrade AC performance.

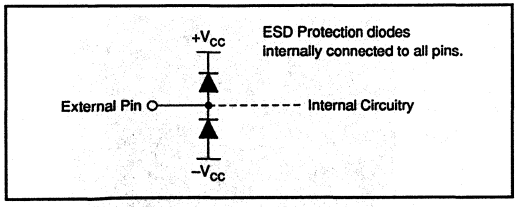


FIGURE 1. Internal ESD Protection.

DISCUSSION OF PERFORMANCE

The MPC100 video multiplexer allows the user to connect any one of four analog input channels (IN_1-IN_4) to the output of the component and to switch between channels within less than 0.5µs. It consists of four identical unity-gain buffer amplifiers, which are connected together internally at the output. The open loop buffers consisting of complementary emitter followers applies no feedback, so their low frequency gain is slightly less than unity and somewhat dependent on loading. Unlike devices using MOS bilateral switching elements the bipolar complementary buffers form an unidirectional transmission path and thus provide high output-to-input isolation. Switching stages compatible to TTL level digital signals are provided for each buffer to select the input channel. When no channel is selected, the output of the device is a high-impedance and allows the user to wire–or more MPC100s together to form switch multi-channel matrices.

If one channel is selected with a digital "1" at the corresponding SEL-input, the MPC100 acts as a buffer amplifier with high input impedance and low output impedance. The truth table on the front page describes the relationship between the digital inputs (SEL_1 to SEL_4) and the analog inputs (IN_1 to IN_4), and which signal is selected at the output.

The 2-4 address decoder and chip select logic is not integrated. The selected design increases the flexibility of address decoding in complex distribution fields, eases BUS-controlled channel selection, simplifies channel selection monitoring for the user, and lowers transient peaks. All of these characteristics make the 1 of 4 multiplexer, in effect, a quad switchable high-speed buffer. They require DC coupling and termination resistors when directly driven from a low impedance cable. High-current output amplifiers are recommended when driving low-impedance transmission lines or inputs.

An advanced complementary bipolar process, consisting of pn-junction isolated high-frequency NPN and PNP transistors, provides wide bandwidth while maintaining low crosstalk and harmonic distortion. The single chip bandwidth of over 100MHz at an output voltage of 2.8Vp-p allows the design of large crosspoint or distribution fields in HDTV-quality with an overall system bandwidth of 36MHz. The buffer amplifiers also offer low differential gain (0.05%) and phase (0.01°) errors. These parameters are essential for video applications and demonstrate how well the signal path maintains a constant small-signal gain and phase for the low-level color subcarrier at 4.43MHz (PAL) or 3.58MHz (NSTC) as the brightness (luminance) signal is ramped through its specified range. The bipolar construction also ensures that the input impedance remains high and constant between ON and OFF states. The ON/OFF input capacitance ratio is near unity, and does not vary with power supply voltage variations. The low output capacitance of 1.0pF when no channel is selected is a very important parameter for large distribution fields. Each parallel output capacitance is an additional load and reduces the overall system bandwidth.

Bipolar video crosspoint switches are virtually glitch-free when compared to signal switches using CMOS or DMOS devices. The MPC100 operates with a fast make-before-break switching action to keep the output switching transients small and short. Switching from one channel to

another causes the signal to mix at the output for a short time, but it hardly interferes with the input signals. The transient peaks remain less than +2.5mV and –1.2mV. Subsequent equipment might interpret large negative output glitches as synchronization pulses. To remove this problem, the output must be clamped during the switching dead time. With the MPC100, the generated output transients are extremely small and clamping is unnecessary. The switching time between two channels is less than 0.5µs. This short time period allows easy switching during the vertical blanking time. The signal envelope during the transition from one channel to another rises and falls symmetrically and shows less overshooting or DC settling transients.

Power consumption is a serious problem when designing large crosspoint fields with high component density. Most of the buffers are always in offstate. One important design goal was to attain low offstate quiescent current when no channel is selected. The low supply current of ±230µA in offstate and ±4.6mA when one channel is selected, as well as the reduced ±5V supply voltage, conserves power, simplifies the power supply design, and results in cooler, more reliable operation.

CIRCUIT LAYOUT

The high-frequency performance of the MPC100 can be greatly affected by the physical layout of the circuit. The following tips are offered as suggestions, not as absolutes. Oscillations, ringing, poor bandwidth and settling, higher crosstalk, and peaking are all typical problems which plague high-speed components when they are used incorrectly.

- Bypass power supplies very close to the device pins. Use tantalum chip capacitors (approximately 2.2µF), a parallel 470F ceramic chip capacitor may be added if desired. Surface-mount types are recommended due to their low lead inductance.
- PC board traces for signal and power lines should be wide to reduce impedance or inductance.
- Make short and low inductance traces. The entire physical circuit should be as small as possible.
- Use a low-impedance ground plane on the component side to ensure that low-impedance ground is available throughout the layout. Grounded traces between the input traces are essential to achieve high interchannel crosstalk rejection. Refer to the suggested layout shown in Figure 9.
- Do not extend the ground plane under high-impedance nodes sensitive to stray capacitances, such as the buffer's input terminals.
- Sockets are not recommended, because they add significant inductance and parasitic capacitance. If sockets must be used, consider using zero-profile solderless sockets.
- Use low-inductance and surface-mounted components. Circuits using all surface mount components with the MPC100 will offer the best AC-performance.
- A resistor (100Ω to 200Ω) in series with the input of the buffers may help to reduce peaking. Place the resistor as close as possible to the pin.
- Plug-in prototype boards and wire-wrap boards will not function well. A clean layout using RF techniques is essential—there are no shortcuts.

SUGGESTED LAYOUT

A completely assembled and tested demonstration board is available for the MPC100 to speed prototyping. This board allows easy and fast performance testing during the design phase and for product qualification. The user can qualify the most important parameters within hours instead of days, while avoiding the hassles of an optimized board layout and power supply bypassing. The complete AC characterization was performed with the same type. Figure 10 shows the schematic and Figure 9 the silk screen and the double-sided layout. Request DEM-MPC100-1GC.

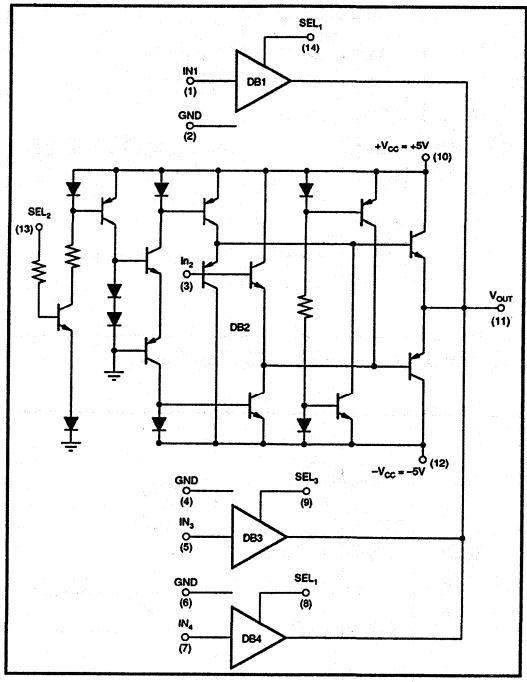


FIGURE 2. Simplified Circuit Diagram.

CROSSTALK

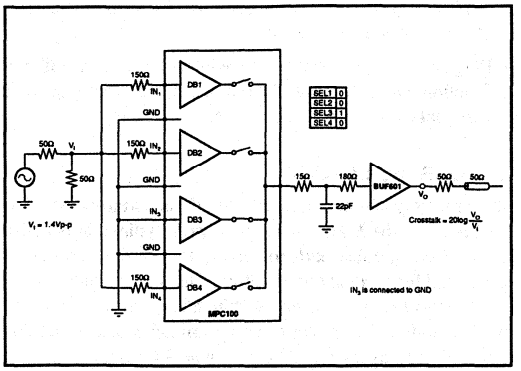


FIGURE 3. All Hostile Crosstalk Test Circuit 1.

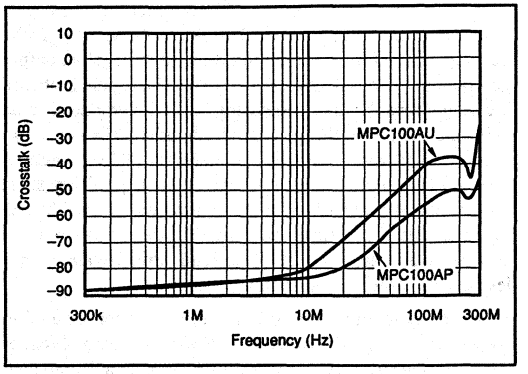


FIGURE 4. All Hostile Crosstalk.

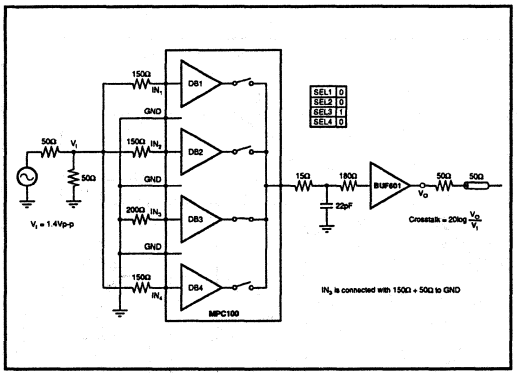


FIGURE 5. All Hostile Crosstalk Test Circuit 2.

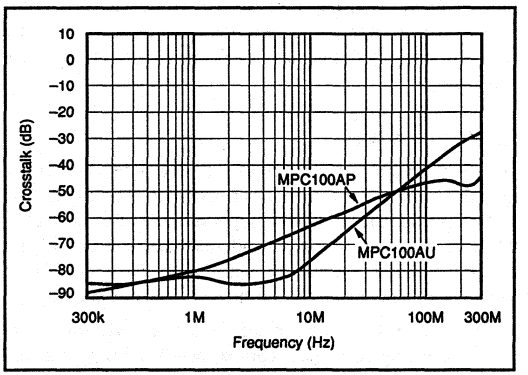


FIGURE 6. All Hostile Crosstalk.

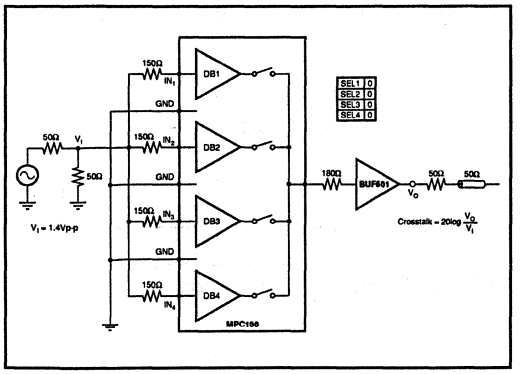


FIGURE 7. Off Isolation Crosstalk Test Circuit.

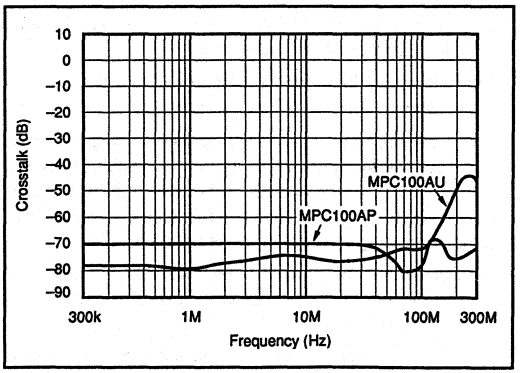


FIGURE 8. Off Isolation Crosstalk.

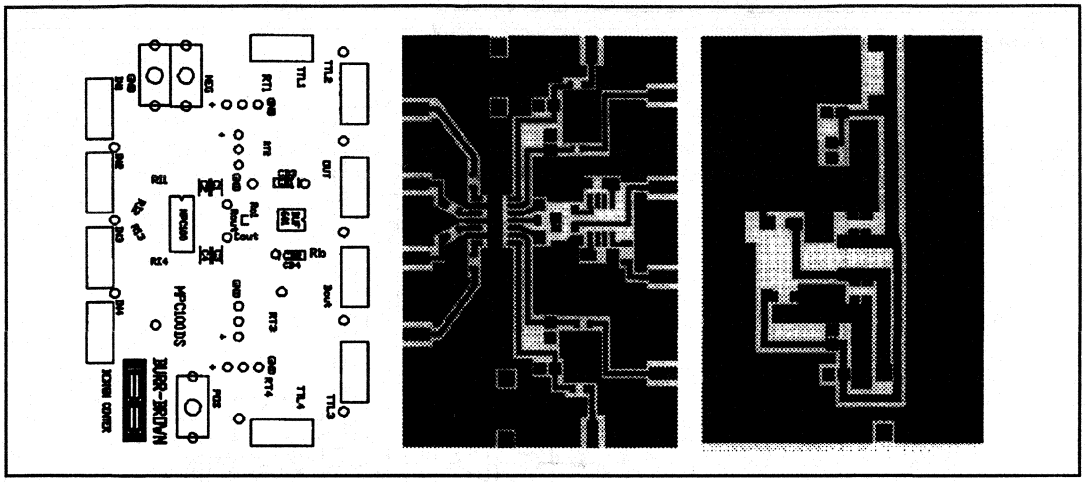


FIGURE 9. Silk Screen and Board Layout of DEM-MPC100-1GC.

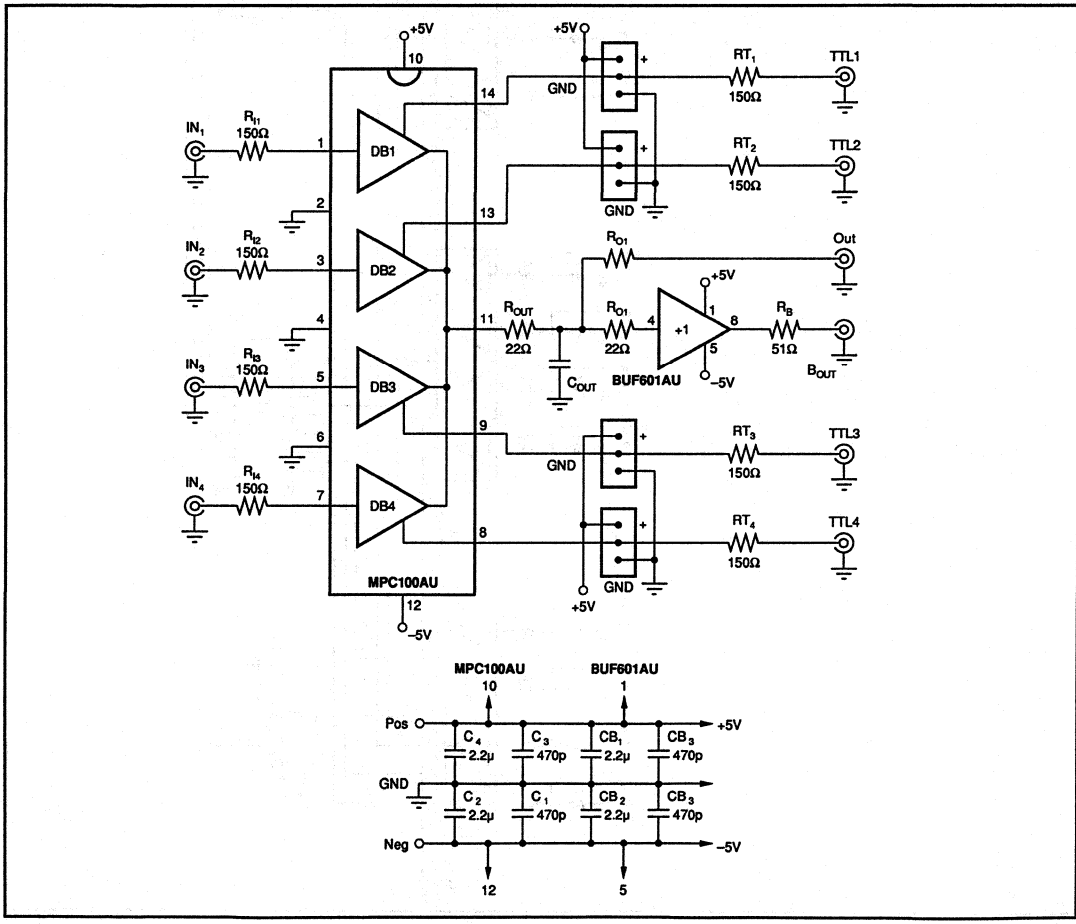


FIGURE 10. Circuit Schematic DEM-MPC100-1GC.

APPLICATIONS INFORMATION

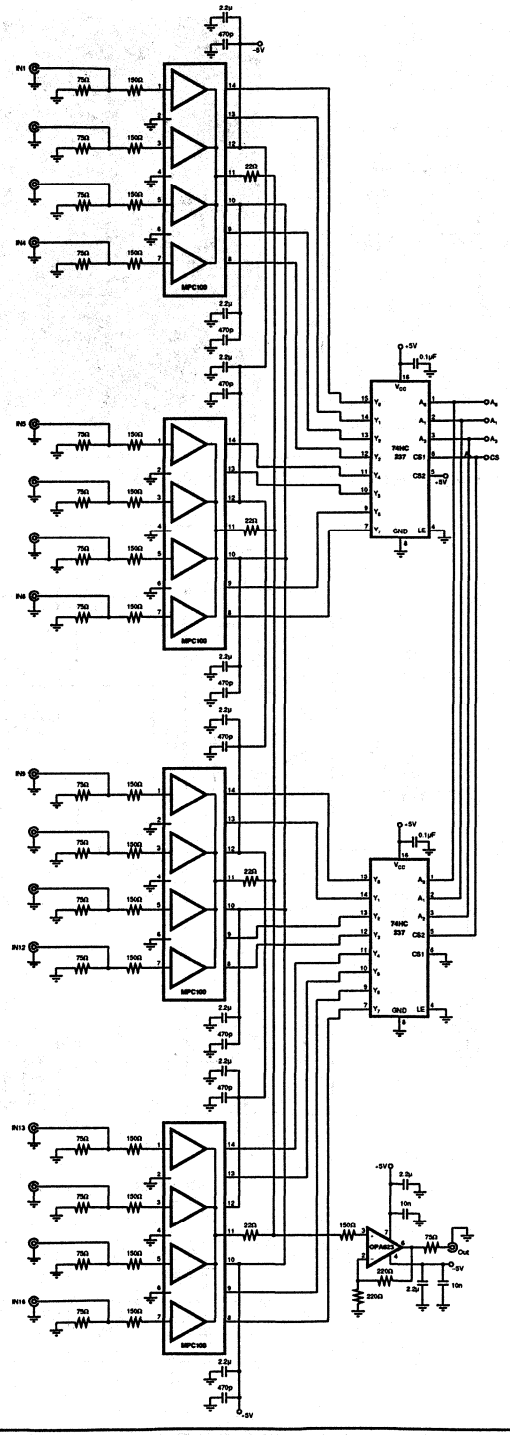


FIGURE 11. Video Distribution Field.

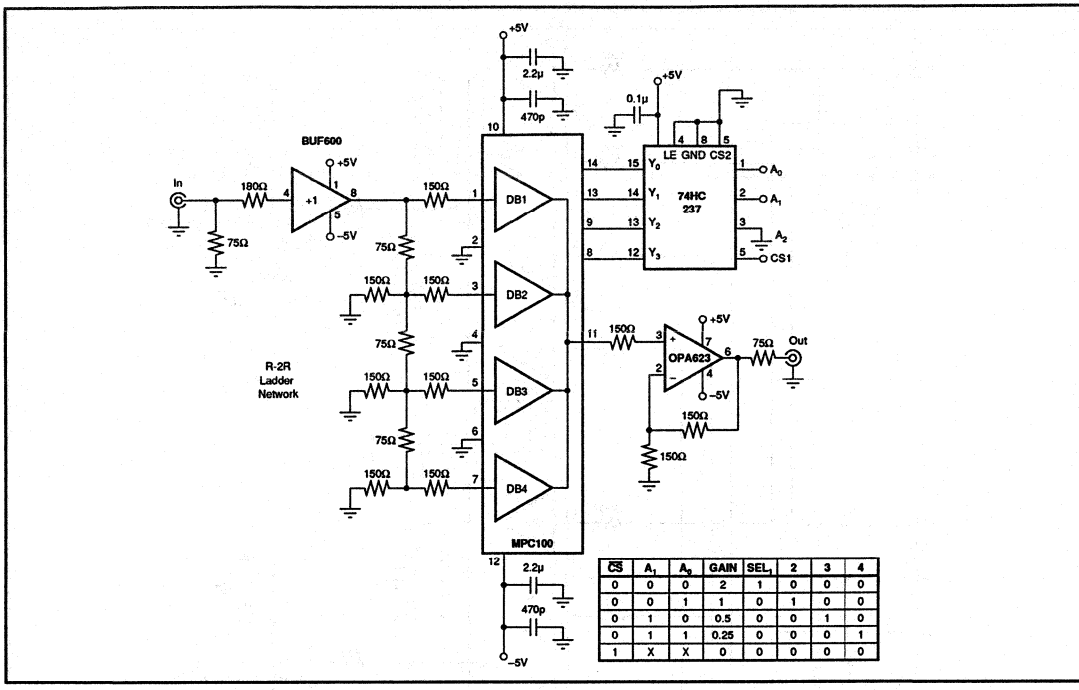


FIGURE 12. Digital Gain Control.

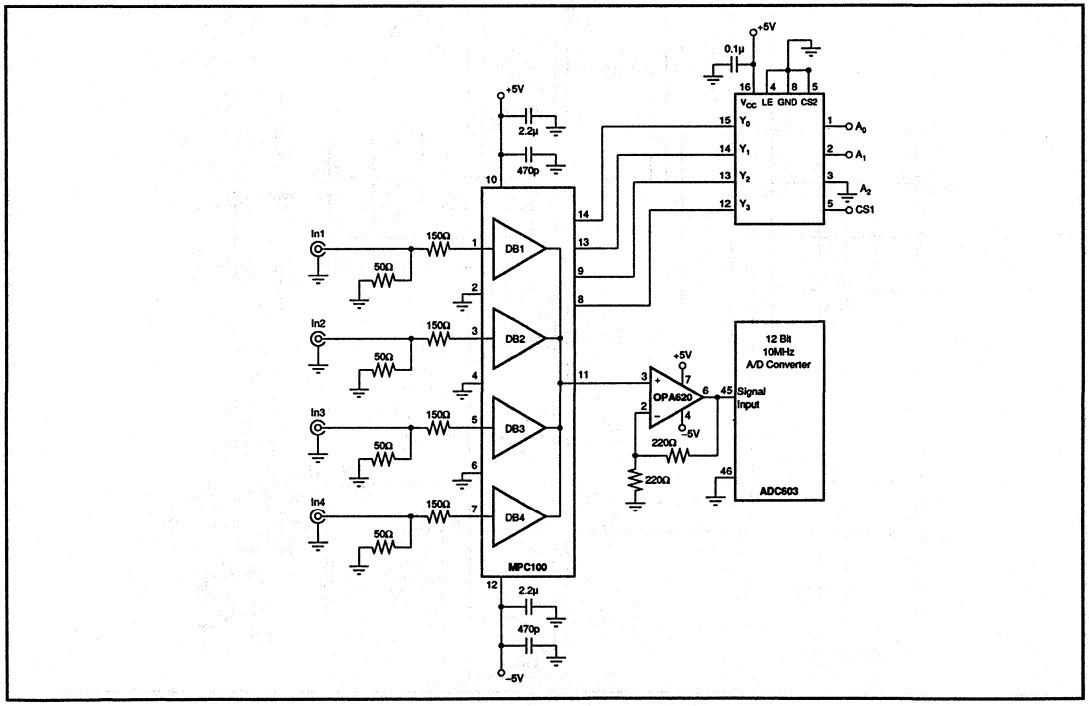


FIGURE 13. High Speed Data Acquisition System.

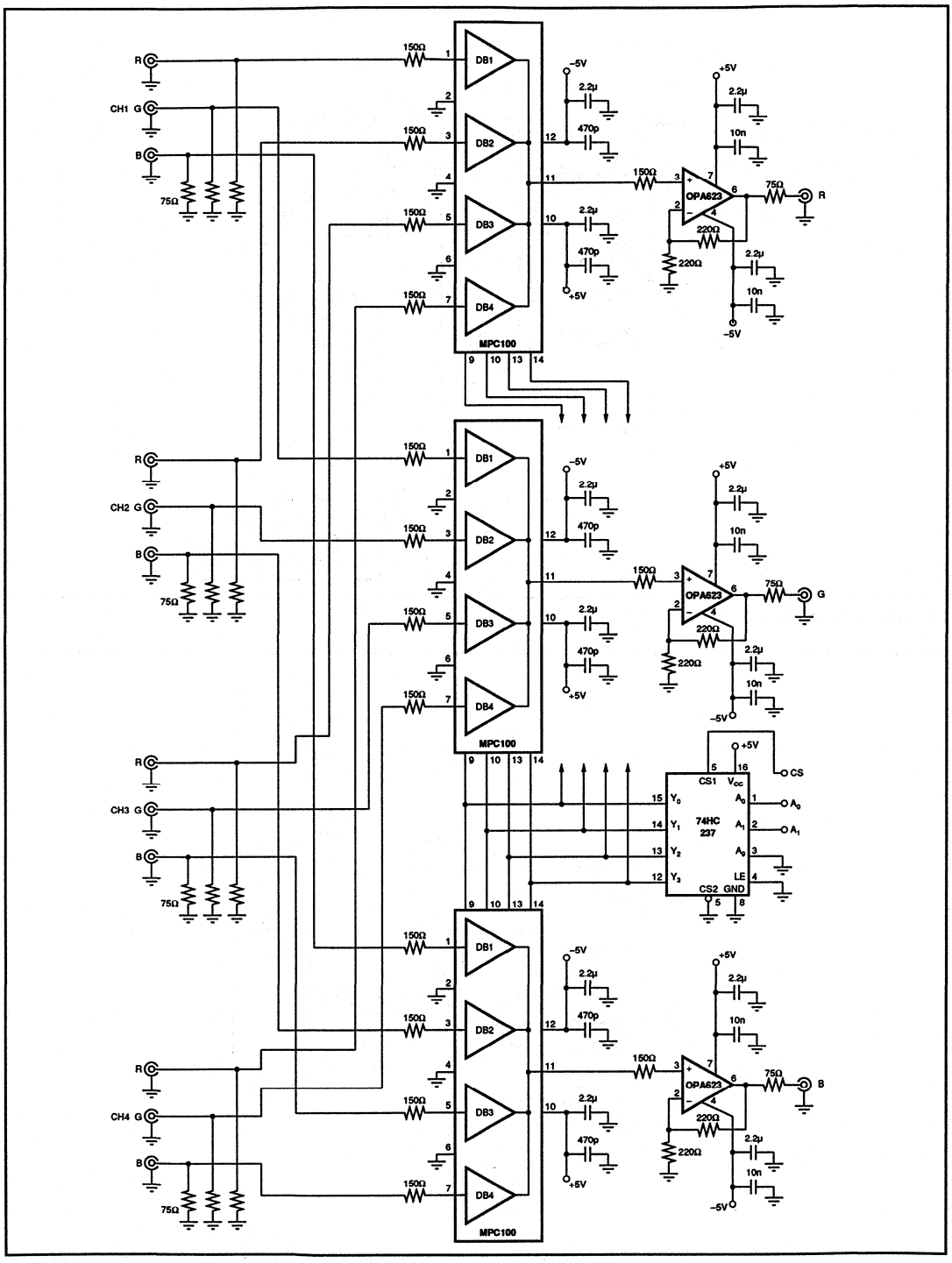


FIGURE 14. Distribution Field for High Resolution Graphic Cards, Cameras.

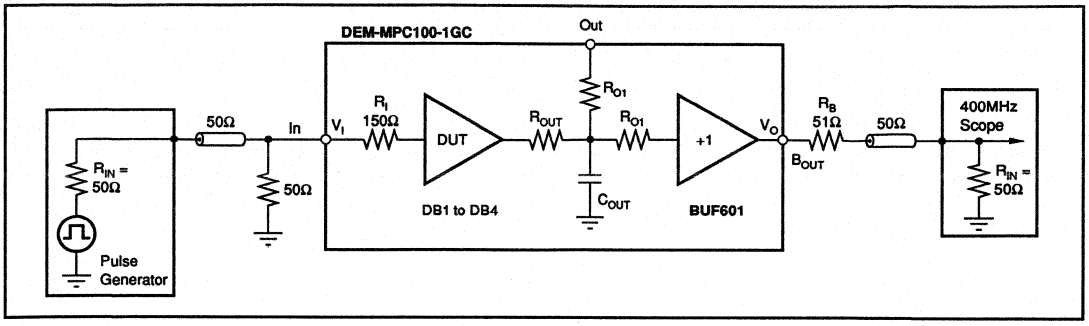


FIGURE 15. Test Circuit Pulse Response.

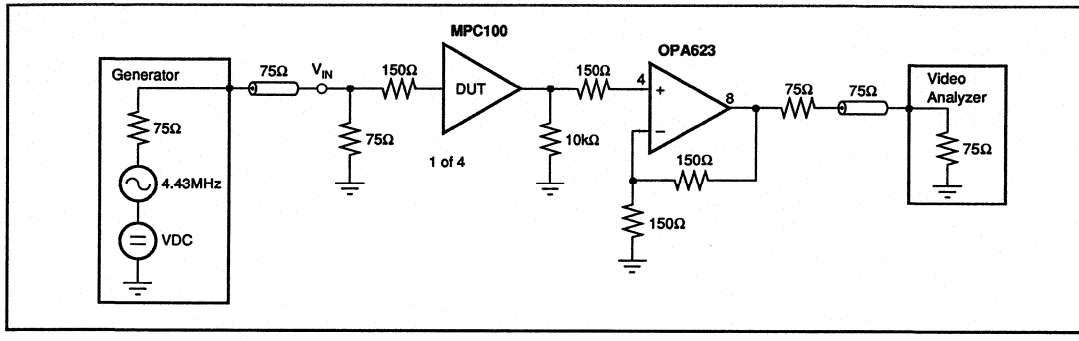


FIGURE 16. Test Circuit Differential Gain and Phase.

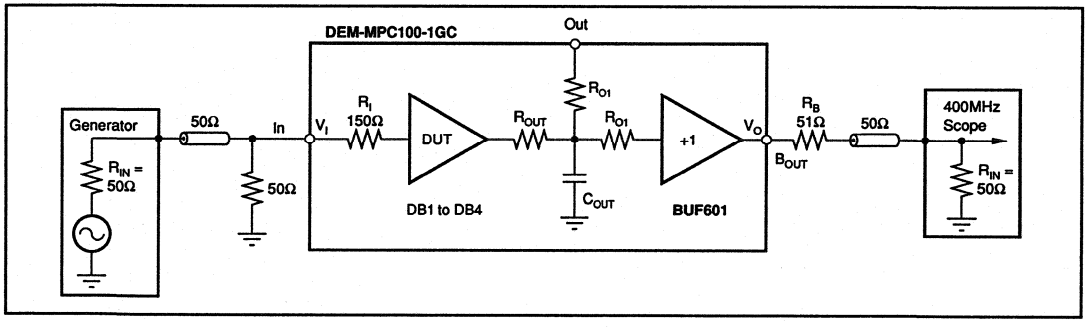


FIGURE 17. Test Circuit Frequency Response.

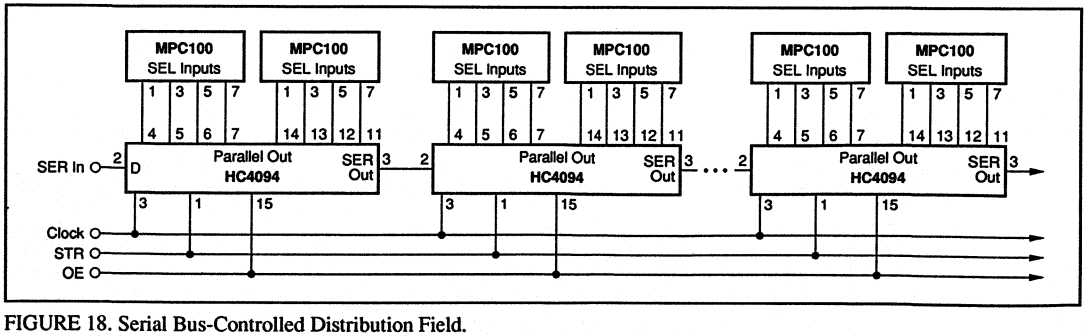


FIGURE 18. Serial Bus-Controlled Distribution Field.

8 Sample/Hold Amplifiers

Sample/hold amplifiers are a key part of the complete data acquisition solution. For any application requiring use of a sample/hold amplifier, consider the variety of products listed in the following Selection Guides. Products range from the SHC298, a low cost solution for your medium-speed 12-bit system, to the SHC600, a high-speed sample/hold optimized for high-bandwidth requirements.

Use of a carefully selected sample/hold can increase the sampling bandwidth of an analog-to-digital converter by up to four orders of magnitude, while insuring that an accurate value of the signal is captured at a specific point in time. In many applications not viewed as requiring high bandwidth data acquisition, optimum performance and cost may still be achieved by using combinations of very high speed multiplexers, sample/holds, and analog-to-digital converters.

The Selection Guides show parameters for the high grade. Models shown in **boldface** are products included in this supplement.

SAMPLE/HOLD AMPLIFIERS

Description	Model	Gain Error (%)	Offset Error (mV)	Charge Offset (mV)	Acq Time (µs max)	Droop Rate (µV/ms)	Temp Range[1]	Pkg[2]	Q, BI[3] Screen	Page No.
Fast, High Accuracy	SHC76	±0.02	±3	±6 typ	3	1	Ind, Com, Miil	HMD	—	8-3
Fast, Industry Std	SHC85	±0.01	±2	±2 max	4.5	125	Com, Mil	HMD MC, SOIC	Q	8-7
Low Cost, Fast Industry Std	SHC5320	NA	±0.5	±1 typ	1.5	0.5	Com, Mil	HCD	BI	8-32
Lowest Cost Industry Std	SHC298	±0.01	±7	±25 max	10	100	Com, Ind	PDIP, MC, SOIC	BI	8-11

HIGH-SPEED SAMPLE/HOLD AMPLIFIERS

Description	Model	Gain Error (%)	Offset Error (mV)	Ampl BW –3dB, (MHz)	Acq Time (µs max)	Droop Rate (µV/µs)	Temp Range[1]	Input Range (Vp-p)	Pkg[2]	Q[3] Screen	Page
High Speed	**SHC804**	**±0.1**	**±3**	**16**	**0.35**	**±5**	**Ind**	**20**	**HDIP**	**Q**	**S-8.6**
High Speed with Buffer	**SHC803**	**±0.1**	**±3**	**16**	**0.35**	**±5**	**Ind**	**20**	**HDIP**	**Q**	**S-8.6**
Ultra-High Speed	**SHC600**	**±0.1**	**±5**	**70**	**0.05**	**±180**	**Ind**	**2.5**	**CDIP**	**Q**	**S-8.2**
	SHC601	±2	±50	100	0.022	±100	Ind	2.5	CDIP	Q	8-22
High Linearity	SHC702	±0.1	±3	3	0.8	±2	Ind	20	24-p DIP	—	9.2-118

NOTES: (1) Temperature Range: Com = 0°C to +70°C, Ind = –25°C to +85°C, Mil = –55°C to +125°C. (2) MC = Metal Can, PDIP = Plastic DIP, HCD = Hermetic Ceramic DIP, CD = Ceramic DIP, HMD = Hermetic Metal DIP, SOIC = Surface Mount Package. (3) Q indicates optional reliability screening is available for this model. BI indicates that an optional 160 hour burn-in is available for the model.

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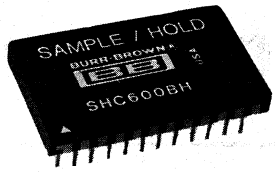


SHC600BH

Ultra-High Speed SAMPLE/HOLD AMPLIFIER

FEATURES

- CLOSED-LOOP OUTPUT AMPLIFIER
- ±0.01% FSR LINEARITY max
- ACQUISITION TIME (2.5V STEP):
  1% FSR 17ns typ
  0.1% FSR 27ns typ
  0.02% FSR 40ns typ
- 300V/µs SLEW RATE
- 24-PIN CERAMIC DIP
- VERY LOW DISTORTION

APPLICATIONS

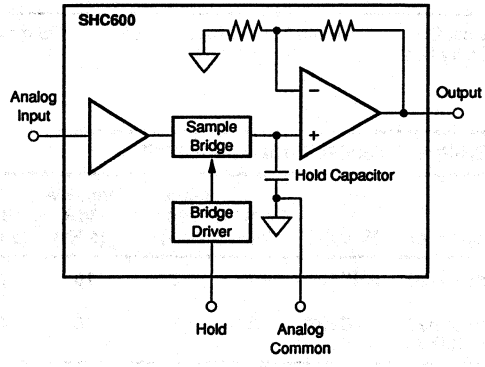
- SUCCESSIVE-APPROXIMATION ADCs
- IMPROVING FLASH ADCs
- WAVEFORM DIGITIZERS
- VIDEO
- PEAK DETECTORS
- BOXCAR INTEGRATORS
- DOWN CONVERTERS

DESCRIPTION

The SHC600 is a high speed S/H amplifier designed for use in ultra-fast, 12-bit data acquisition and signal processing systems. It acquires input step changes of 2.5V to 1% accuracy in 17ns and 0.02% accuracy in 40ns, typically. The closed-loop output amplifier provides a maximum linearity error of ±0.01% with a low output impedance of 0.4Ω. The gain has been optimized to drive 100Ω loads with a gain error of less than ±0.1%.

In the sample mode the SHC600 operates as a unity-gain buffer with a small signal bandwidth of 70MHz. Input voltage range is ±2V.

The hold command is ECL-compatible.



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Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

PDS-644A

SPECIFICATIONS

ELECTRICAL

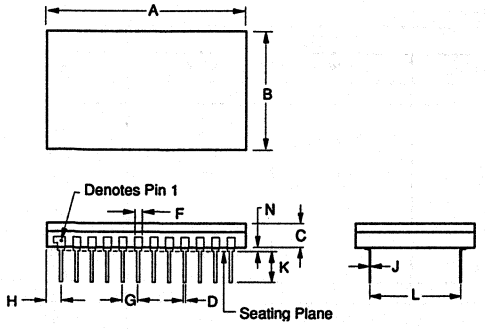
At +25°C and rated power supplies and 100Ω in parallel with 3pF load unless otherwise specified.

PARAMETER	SHC600BH MIN	SHC600BH TYP	SHC600BH MAX	UNITS
SAMPLE/HOLD INPUTS				
ANALOG				
Voltage Range		±1.25	±2	V
R_{IN}		1.5		MΩ
Input Bias Current		20	35	µA
DIGITAL (ECL Compatible)				
V_{IH} (HOLD)	−1.1		−0.8	V
V_{IL} (SAMPLE)	−1.8		−1.5	V
I_{IH}, V_{IN} = −1.1V			265	µA
I_{IL}, V_{IN} = −1.8V	0.5			µA
SAMPLE/HOLD OUTPUT				
Voltage Range		±1.25	±2	V
Output Current	±40			mA
Short Circuit Protection		Momentary (1s)		
Output Impedance (at DC)		0.4		Ω
Noise in Track Mode (Wideband 200MHz into 50Ω Load)		400		µVrms
SAMPLE/HOLD TRANSER CHARACTERISTICS				
DC ACCURACY/STABILITY				
Gain		+1		V/V
Gain Error		±0.1		%
Temperature Coefficient		±5	±20	ppm/°C
Linearity Error (±1.25V Input)		±0.002	±0.01	% of FSR[1]
Zero Offset		±2	±5	mV
Temperature Coefficient		±50	±150	µV/°C
Power Supply Sensitivity of Offset: V_{DD1} (+5V)		±1	±3	mV/V
V_{DD2} (−5.2V)		±4	±13	mV/V
$+V_{CC}$ (+15V)		±5	±10	mV/V
$-V_{CC}$ (−15V)		±9	±15	mV/V
HOLD-TO-TRACK (SAMPLE) DYNAMICS				
Acquisition Time (With 2.5V Step)[1]: To Within ±1% of FSR (25mV)		17	25	ns
To Within ±0.1% of FSR (2.5mV)		27	35	ns
To Within ±0.02% of FSR (0.5mV)		40	50	ns
Switch Delay Time		2		ns
TRACK (SAMPLE)-TO-HOLD DYNAMICS				
Aperture Delay Time		4	8	ns
Aperture Uncertainty (Jitter)		5	9	ps (rms)
Offset Step (Pedestal)		±2	±10	mV
Temperature Coefficient		±30	±60	µV/°C
Sensitivity to V_{DD2} (−5.2V)		±2.5	±10	mV/V
Switch Delay Time		2		ns
Switching Transient: Amplitude		7	20	mVpk
Settling to Within ±1mV		10	15	ns
TRACK (SAMPLE) MODE DYNAMICS				
Frequency Response: Full Power Bandwidth		40		MHz
Small Signal Bandwidth		70		MHz
Output Slew Rate	200	300		V/µs
Harmonic Distortion (2.5Vp-p Input at 4MHz): R_L = 200Ω		−78		dB
R_L = 50Ω		−65		dB
HOLD MODE DYNAMICS				
Droop Rate: at +25°C Case Temp		±60	±180	µV/µs
at +85°C Case Temp		±1.5	±4	mV/µs
Feedthrough Rejection: 2.5Vp-p Input at 1MHz	62			dB
at 10MHz	58			dB
POWER SUPPLY REQUIREMENTS				
Supply Voltages: V_{DD1}	+4.75	+5.0	+5.25	V
V_{DD2}	−4.95	−5.2	−5.46	V
$+V_{CC}$	+14.25	+15	+15.75	V
$-V_{CC}$	−14.25	−15	−15.75	V
Quiescent Current: V_{DD1}		40	55	mA
V_{DD2}		−93	−120	mA
$+V_{CC}$		30	45	mA
$-V_{CC}$		−15	−25	mA
Power Dissipation		1.3	2.0	W
TEMPERATURE RANGE				
Specification (Case Temperature)	−25		+85	°C
Storage	−55		+125	°C

NOTES: (1) FSR means Full-Scale Range. For SHC600 FSR = 2.5V.

MECHANICAL

H-Package—24-Pin Ceramic DIP



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.280	1.310	32.51	33.27
B	.780	.800	19.81	20.32
C	.130	.180	3.30	4.57
D	.016	.020	0.41	0.51
F	.045	.055	1.14	1.40
G	.100 BASIC		2.54 BASIC	
H	.088	.108	2.24	2.74
J	.009	.012	0.23	0.30
K	.200	.210	5.08	5.33
L	.600 BASIC		15.24 BASIC	
N	.015	.035	0.38	0.89

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

PIN ASSIGNMENTS

1	V_{DD1} (+5V)	13	Analog Input
2	V_{DD2} (–5.2V)	14	NIC(1)
3	NIC(1)	15	NIC(1)
4	V_{DD2} (–5.2V)	16	NIC(1)
5	Hold Command	17	NIC(1)
6	Digital Common	18	Analog Common
7	Power Common	19	Analog Common
8	$+V_{CC}$ (+15V)	20	NIC(1)
9	NIC(1)	21	NIC(1)
10	V_{DD2} (–5.2V)	22	$+V_{CC}$ (+15V)
11	Power Common	23	NIC(1)
12	$-V_{CC}$ (–15V)	24	Analog Output

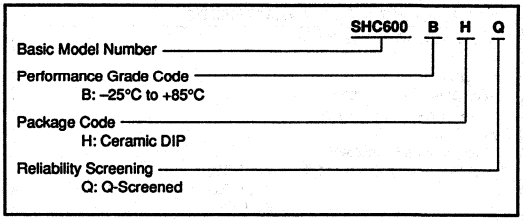
NOTE: (1) NIC = No Internal Connection.

ABSOLUTE MAXIMUM RATINGS

$\pm V_{CC}$	16.5V
V_{DD1}	+7.0V
V_{DD2}	–7.0V
Analog Input	±5.0V
Logic Input	V_{DD2} to +0.5V
Case Temperature	+100°C
Junction Temperature	+150°C
Storage Temperature	–40°C to +100°C

NOTE: Stresses above these ratings may cause permanent damage to the device.

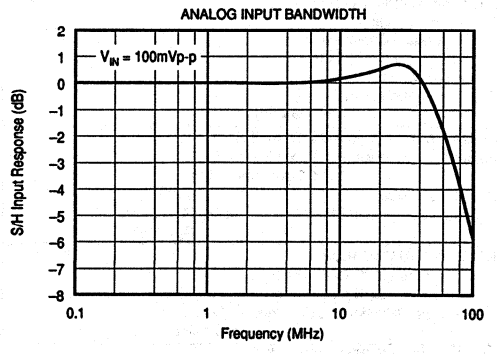
ORDERING INFORMATION



THEORY OF OPERATION

The SHC600 is a high-speed S/H amplifier with low distortion, fast acquisition time and very low aperture uncertainty (jitter). A diode bridge sampling switch is used to achieve an acceptable compromise between speed and accuracy. The diode bridge switching transients are buffered from the analog input by a high input impedance buffer amplifier. Since the hold capacitor does not appear in the feedback of the diode bridge output buffer, the capacitor can acquire the signal in 25ns. The low-bias-current output buffer droop appears as only an offset error and does not affect linearity.

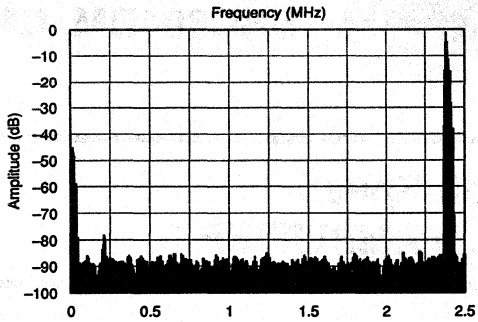
TYPICAL PERFORMANCE CURVE



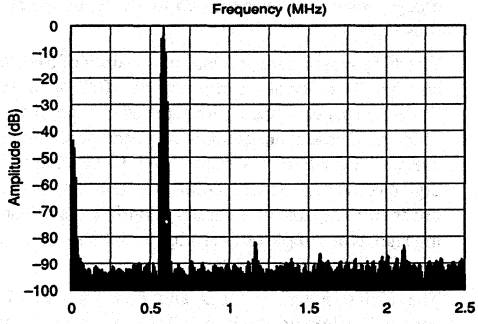
TYPICAL FFT SPECTRAL PERFORMANCE

All FFT data: 512-point FFT, 10-sample average; minimum 4-sample Blackman-Harris Window. Tested in ADC600K high speed ADC.

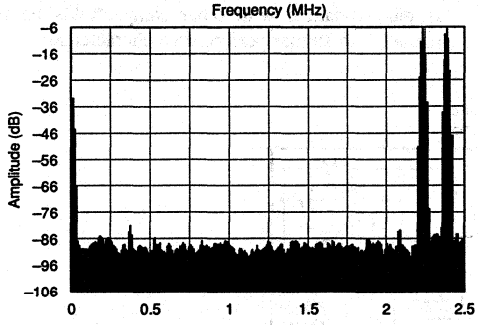
Sample Rate = 5MHz, Input Voltage = Full-Scale (0dB)



	Level re: Full-Scale (dB)
2.4121MHz Fundamental	–0.6
Harmonics: 2f	–77.9
3f	–83.1
4f	–85.3
SINAD	67.3dB
TND	–68.5dBc
THD	–73.3dBc



	Level re: Full-Scale (dB)
0.5859MHz Fundamental	–0.7
Harmonics: 2f	–81.4
3f	–87.2
4f	–87.0
SINAD	69.6dB
TND	–70.7dBc
THD	–76.1dBc



	Level re: Full-Scale (dB)
F_1: 2.2461MHz	–6.3
F_2: 2.4023MHz	–6.4
Peak Envelope	–0.7
IMD: 0.3809MHz	–81.2
2.0996MHz	–82.9
2.4707MHz	–83.9

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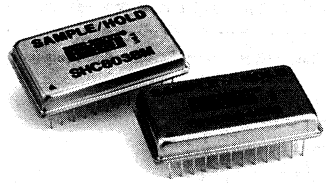


SHC803BM, CM
SHC804BM, CM

Ultra-High Speed SAMPLE/HOLD AMPLIFIER

FEATURES

- **350ns max ACQUISITION TIME**
- **±0.01% THROUGHPUT NONLINEARITY**
- **150ns max SAMPLE-TO-HOLD SETTLING TIME**
- **INPUT BUFFER (SHC803)**
- **24-PIN HERMETICALLY-SEALED METAL PACKAGE**

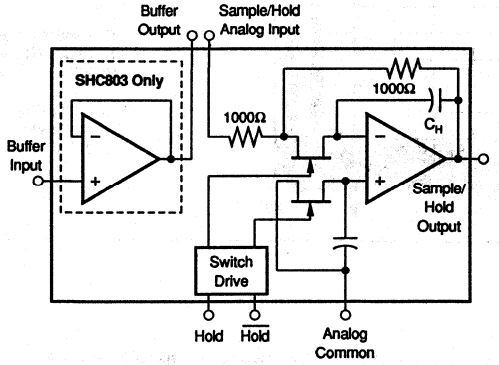
DESCRIPTION

The SHC803 and SHC804 are high speed sample/hold amplifiers designed for use in fast 12-bit data acquisition systems and signal processing systems. The SHC803 contains a fast-settling unity-gain amplifier for buffering high impedance sources or for use with CMOS multiplexers.

The SHC804 acquires a 10V signal change in less than 350ns to ±1/2LSB at 12 bits. Throughput nonlinearity error is guaranteed to be within ±1/2LSB for 12-bit systems. Stability over temperature is excellent, with only ±5ppm/°C of gain drift and ±4ppm of FSR/°C of charge offset drift over the –25 to +85°C temperature range.

The ±25ps maximum aperture uncertainty of SHC803 and SHC804 permits sampling (to ±0.01% of Full Scale Range) of signals with rates of change of up to 100V/µs. These sample/holds have been optimized for use with Burr-Brown's high speed 12-bit analog-to-digital converter, model ADC803. Together these components are capable of accurately digitizing fast changing signals at sample rates as high as 500k samples per second.

The digital inputs (HOLD and $\overline{\text{HOLD}}$) are TTL-compatible. Power supply requirements are ±15V and +5V and the specification temperature range is –25°C to +85°C. The SHC803 and SHC804 are packaged in a 24-pin dual-in-line hermetic metal package. SHC804 is pin-compatible with other sample/holds on the market with similar performance characteristics.



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SPECIFICATIONS

ELECTRICAL

At +25°C, rated power supplies and a 1kΩ output load, unless otherwise specified.

PARAMETER	SHC803/SHC804BM MIN	SHC803/SHC804BM TYP	SHC803/SHC804BM MAX	SHC803/SHC804CM MIN	SHC803/SHC804CM TYP	SHC803/SHC804CM MAX	UNITS
SAMPLE/HOLD INPUTS (without Input Buffer)							
ANALOG							
Voltage Range	±10.25	±11		*	*		V
R_{IN}		1.00			*		kΩ
DIGITAL (HOLD, $\overline{HOLD}$)							
V_{IH}	+2.0			*			V
V_{IL}			+0.8			*	V
I_{IH}, V_{IN} = +2.7V			+60			*	µA
I_{IL}, V_{IN} = +0.4V			−1.2			*	mA
SAMPLE/HOLD TRANSFER CHARACTERISTICS (without Input Buffer)							
ACCURACY							
Sample Mode							
Gain		−1			*		V/V
Gain Error			±0.1			*	%
Temperature Coefficient		±3	±10		±1	±5	ppm/°C
Linearity Error		±0.001	±0.005		*	*	% of FSR[1]
Zero Offset		±1	±5		±0.5	±3	mV
Temperature Coefficient		±1	±2.5		±0.5	±1.5	ppm of FSR/°C
Hold Mode							
Charge Offset		±2	±10		±1	±5	mV
Temperature Coefficient		±3	±10		±2	±4	ppm of FSR/°C
Droop Rate: at +25°C		±0.5	±5		*	*	µV/µs
+85°C			±0.5			±0.1	mV/µs
Throughput Nonlinearity			±0.01			*	% of FSR
Power Supply Sensitivity[2]: ±V_{CC}			±0.002			*	% of FSR/%V_{CC}
V_{DD}			±0.003			*	% of FSR/%V_{DD}
DYNAMIC CHARACTERISTICS							
Acquisition Time (with 10V Step)							
to within: ±0.1% (±10mV)		220			*		ns
±0.01% (±1mV)		250	350		*	*	ns
Sample-to-Hold Settling Time							
to within ±0.01% (±1mV)		100	150		*	*	ns
Sample-to-Hold Transient Amplitude		60	150		*	*	mV_{PEAK}
Aperture Delay Time[3]		15	25		*	*	ns
Aperture Uncertainty		±10	±25		*	*	ps
Sample Mode: Output Slew Rate		160			*		V/µs
Full Power Bandwidth		1			*		MHz
Small Signal Bandwidth		16			*		MHz
Hold Mode Feedthrough Rejection							
(10V Square Wave Input)	±0.03	±0.005			*		%
SAMPLE/HOLD OUTPUT							
Voltage Range	±10.25	±11		*	*		V
Output Current	±50			*			mA
Short Circuit Protection		Indefinite to Common			*		
Output Impedance (at DC)		0.01	0.1		*	*	Ω
INPUT BUFFER CHARACTERISTICS (SHC803 only)							
INPUT							
Offset Voltage		±1/2	±5		*	*	mV
vs Temperature		±1.5	±2.5		*	*	ppm of FSR/°C
Bias Current			±25			*	nA
Impedance		10^8 || 5			*		Ω || pF
V_{IN} Range	±10.25	±11		*	*		V
DYNAMIC CHARACTERISTICS							
Full Power Bandwidth		320			*		kHz
Slew Rate[4]		10			*		V/µs
Settling Time[4] to ±2mV for 10V Step		2.5			*		µs
OUTPUT							
V_{OUT} Range	±10.25			*			V
Output Current	±10.25			*			mA

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

SPECIFICATIONS (CONT)

ELECTRICAL

At +25°C, rated power supplies and a 1kΩ output load, unless otherwise specified.

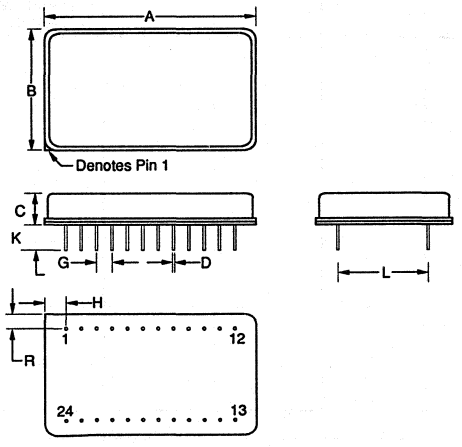
PARAMETER	SHC803/SHC804BM			SHC803/SHC804CM			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	
POWER SUPPLY REQUIREMENTS							
Rated Voltage: $\pm V_{CC}$	±13.5	±15	±16.5	*	*	*	V
V_{DD}	+4.75	+5.00	+5.25	*	*	*	V
Quiescent Current (No Load)							
SHC804: $+V_{CC}$		30	35		*	*	mA
$-V_{CC}$		15	20		*	*	mA
V_{DD}		5	10		*	*	mA
SHC803: $+V_{CC}$		33	40		*	*	mA
$-V_{CC}$		18	25		*	*	mA
V_{DD}		5	10		*	*	mA
Power Dissipation: SHC804		700	875		*	*	mW
SHC803		790	1100		*	*	mW
TEMPERATURE RANGE							
Specification	–25		+85	*		*	°C
Storage	–55		+125	*		*	°C

* Specification same as SHC803/SHC804BM.

NOTES: (1) FSR means Full Scale Range and is 20V for SHC803 and SHC804. (2) Sensitivity of offset plus charge offset. (3) With respect to HOLD. For $\overline{\text{HOLD}}$ add 5ns typical. (4) With buffer connected to the sample/hold amplifier.

MECHANICAL

M Package — 24-Pin



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.365	1.385	34.67	35.18
B	.790	.810	20.07	20.57
C	.170	.250	4.32	6.35
D	.016	.021	0.41	0.53
G	.100 BASIC		2.54 BASIC	
H	.125	.150	3.18	3.81
K	.150	.300	3.81	7.62
L	.600 BASIC		15.24 BASIC	
R	.080	.110	2.03	2.79

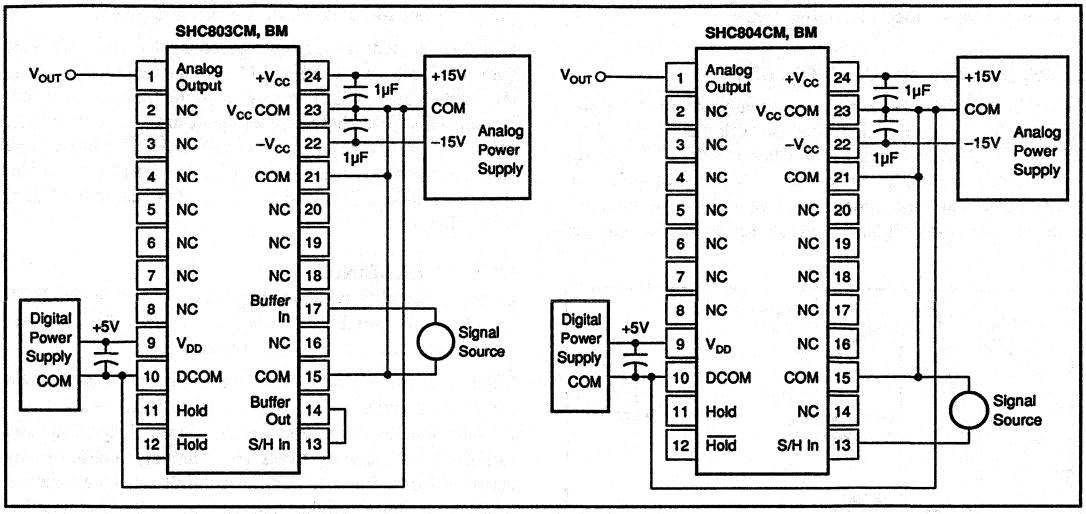
NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only.

ABSOLUTE MAXIMUM RATINGS

Input Overvoltage	±15V
$+V_{CC}$ to V_{CC} COMMON	0 to +18V
$-V_{CC}$ to V_{CC} COMMON	0 to –18V
Voltage on Digital Inputs (pins 11 and 12)	–0.5V to +7V
Power Dissipation	1500mW
V_{DD} to DCOM	–0.5V
Analog Output	Indefinite Short to V_{CC} COM

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliablility.

CONNECTION DIAGRAMS



PIN ASSIGNMENTS

PIN	NAME	DESCRIPTION
1	Sample/Hold Output	Analog voltage output
2	NC	Not connected
3	NC	Not connected
4	NC	Not connected
5	NC	Not connected
6	NC	Not connected
7	NC	Not connected
8	NC	Not connected
9	V_{DD}	Logic supply
10	DCOM	Logic supply common
11	HOLD	Logic "1" = HOLD
12	$\overline{HOLD}$	Logic "0" = HOLD
13	S/H In	SHC804 input; for SHC803 connect pin 13 to pin14
14	Buffer Out, SHC803 only	Not connected for SHC804
15	COM	Signal common
16	NC	Not connected
17	Buffer In, SHC803 only	Not connected for SHC804
18	NC	Not connected
19	NC	Not connected
20	NC	Not connected
21	COM	Signal common
22	$-V_{CC}$	-15V supply
23	V_{CC} COM	Analog to power common, connected to case
24	$+V_{CC}$	+15V supply

DISCUSSION OF SPECIFICATIONS

Throughput Nonlinearity is defined as total Hold mode, nonadjustable, input to output error caused by charge offset, gain nonlinearity, droop, feedthrough, and thermal transients. It is the inaccuracy due to these errors which cannot be corrected by Offset and Gain adjustments.

Gain Error is the difference between the input and output voltage magnitude (in the Sample mode) due to the amplifier gain errors.

Droop Rate is the voltage decay at the output when in the Hold mode due to storage capacitor and FET switch leakage current and the input bias current of the output amplifier.

Feedthrough is the amount of output voltage change caused by an input voltage change when the sample/hold is in the Hold mode.

Aperture Delay Time is the time required to switch from Sample to Hold. The time is measured from the 50% point of the Hold mode control transition to the time at which the output stops tracking the input.

Aperture Uncertainty Time is the nonrepeatibility of aperture delay time.

Acquisition Time is the time required for the sample/hold output to settle to within a given error band of its final value when the sample/hold is switched from Hold to Sample.

Charge Offset (Pedestal) is the output voltage change that results from charge coupled into the Hold capacitor through the gate capacitance of the switching field effect transistor. This charge appears as an offset at the output.

Sample-to-Hold Switching Transient is the switching transient which appears on the output when the sample/hold is switched from Sample to Hold. Both the magnitude and the settling time of the transient are specified.

OPERATION

A simplified circuit diagram of SHC803/804 is shown on page 1. The SHC803 includes a noninverting unity-gain op amp to serve as a source-impedance buffer when the sample/hold is used with CMOS analog multiplexers. The SHC804 and SHC803 are identical except for this buffer.

In the Sample (track) mode the circuit acts as a unity-gain inverting amplifier. In the Hold mode, the capacitor, C_H, holds the value of the output at the time the unit was switched to the Hold mode. Additional circuits compensate for switching transients and provide switch leakage current

cancellation. The amplifier provides high current drive and low output impedance to external loads.

GAIN, OFFSET, CHARGE OFFSET

SCH803 and SCH804 have been internally-trimmed to eliminate the need for external trim potentiometers for Gain, Offset (in Sample mode) and Charge Offset (Pedestal). System Gain and Offset errors can be adjusted elsewhere in the system, at an input amplifier preceding the sample/hold, or at an analog-to-digital converter following the sample/hold.

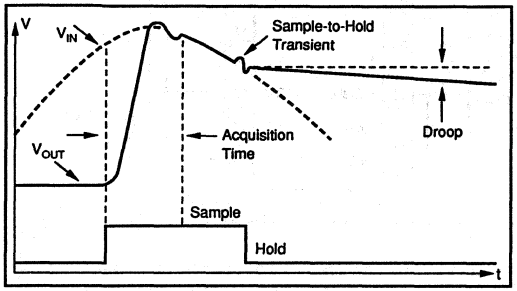


FIGURE 1. Definition of Acquisition Time, Droop and Sample-to-Hold Transient.

INSTALLATION

GROUNDING AND BYPASSING

SHC803 and SHC804 have four COMMON pins (pins 10, 15, 21 and 23) and all must be tied together and connected to the system analog common (V_{CC} COM) as close to the package as possible. It is preferable to have a large ground plane surrounding the sample/hold and have all four common pins soldered directly to it. Note that the metal case is internally connected to pin 23; therefore, care must be taken to avoid a ground loop if the case is allowed to contact the ground plane.

Most digital return currents pass through pin 10. Noise from the switch-drive circuit may couple directly into the main op amp summing junction, a very noise-sensitive node. Care must be taken to insure that no voltage differences occur between pin 10 and the other common pins. This is the reason pin 10 must be connected directly to the ground plane.

For the same reason, the logic supply should be kept as free of noise as possible. $\pm V_{CC}$ supply lines (pins 24 and 22) are internally bypassed to common with 0.01µF capacitors. It is recommended that the user install additional external 0.1µF to 1µF tantalum bypass capacitors at each supply pin.

SAMPLE/HOLD CONTROL

A TTL logic "0" at pin 11 (or a logic "1" at pin 12) switches the SHC803/804 into the Sample (track) mode. In this mode, the device acts as a unity-gain inverting amplifier, the output following the inverse of the input. A logic "1" at pin 11 (or a logic "0" at pin 12) will switch the SHC803/804 into the Hold mode. The output voltages will be held constant at the value present when the Hold command is given.

If pin 11 is used, pin 12 must be connected to the DCOM (pin 10). If pin 12 is used, pin 11 must be tied to V_{DD}. Using the HOLD and $\overline{HOLD}$ inputs as logic function may adversely affect the charge offset (pedestal). A clean digital signal (no overshoot) at the HOLD of $\overline{HOLD}$ inputs will also reduce charge offset errors. Pins 11 and 12 present less than one standard TTL load (two LSTTL loads) to the digital drive circuit.

OUTPUT LOADING

Care must be taken when loading the output of the SHC803/804 to avoid possible oscillations, current limiting and performance variations over temperature.

The maximum capacitive load to avoid oscillations is about 300pF. Recommended resistive load is 500Ω or more, although values as low as 250Ω may be used. Acquisition and sample-to-hold settling times are relatively unaffected by resistive loads down to 250Ω in parallel with capacitive loads up to 100pF. Higher capacitances will affect acquisition and settling times.

ANALOG SIGNAL SOURCE CONSIDERATIONS

The output impedance of the signal source driving the SHC804 will affect the accuracy of the sample and hold operation both statically (at DC) and dynamically. The output impedance of the signal source should be low and remain low over a wide bandwidth. A small capacitor at the driving source may help to improve the charge offset errors that are affected by dynamic source impedance.

SHC803 BUFFER AMPLIFIER

The buffer amplifier incorporated in the SHC803 provides appropriate drive characteristics to the sample/hold amplifier. Again a 20pF to 50pF capacitor added to the output of the buffer amplifier may improve charge offset performance.

The buffer amplifier is optimized for fast settling with 10Vp-p signals. However, for step input signals greater than 10V, a protection network (Figure 2) is required to prevent the buffer from overload, resulting in excessive settling time.

The data sheet for the Burr-Brown model ADC803 analog-to-digital converter contains a sample printed circuit board layout incorporating many of the above considerations.

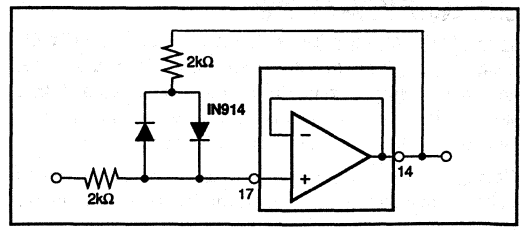


FIGURE 2. SHC803 Buffer Amplifier Protection For Input Steps Greater Than 10V.

APPLICATIONS

SIGNAL DIGITIZATION

Sample/hold amplifiers are commonly used to hold input voltages to an A/D converter constant during conversion. Digitizing errors result if the analog signal being digitized varies excessively during conversion.

For example, the Burr-Brown ADC803 is a 12-bit successive-approximation converter with a 1.5µs conversion time. To insure the accuracy of the output data, the analog input signal to the A/D converter must not change more than 1/2LSB during the conversion.

The maximum rate of change for sine wave inputs is dv/dt (max) = $2\pi Af$ (V/s). If one allows a 1/2LSB change (2.44mV) for a ±10V input swing to the A/D converter, the allowable input rate-of-change limit would be 2.44mV/1.5µs = 1.63mV/µs. Thus the sampled sinusoidal signal frequency limit is

$$f = (1.63 \times 10^3)/2\pi A = 259/A(Hz)$$

where A is the amplitude of the sine wave. For a ±10V sine wave this corresponds to a frequency of 26Hz.

A sample/hold in front of the A/D converter "freezes" the converter's input signal whenever it is necessary to make a conversion. The rate-of-change limitation calculated above no longer exists. If a sample/hold has acquired an input signal and is tracking it, the sample/hold can be commanded to hold at any instant. There is a short delay between the time the hold command is asserted and the time the circuit actually holds. This delay is called aperture delay. The hold command signal can usually be advanced in time to cause the amplifier to hold when one wants it to hold.

The uncertainty in aperture delay, called aperture jitter, is a key consideration. For the SHC803/804 there is a 25ps maximum period during which the input signal should not change, for example, more than 1/2LSB for 12-bit systems. For a ±10V input range (1/2LSB = 2.44mV), the input signal rate of change limitation is 2.44mV/25ps = 97.6V/µs. The equivalent input sine wave frequency is

$$f = 97.6 \times 10^6/2\pi A = 15.5/A(MHz),$$

60,000 times higher than using the A/D alone.

However, there are other considerations. The resampling rate of an ADC803 is 1.5µs (A/D conversion time) + 0.3µs (sample/hold acquisition time) = 1.8µs. If one samples a sine wave at the Nyquist rate this permits sampling a frequency of 278kHz. The above analysis assumed that the droop rate of the sample/hold is negligible—less than 1/2LSB during the conversion time—and that the large signal bandwidth response of the sample/hold causes negligible waveform distortion.

USING THE SHC804 WITH THE ADC803

ADC803 is a 1.5µs, 12-bit successive approximation A/D converter. Its input circuitry has been designed to minimize high frequency current transients that appear at the input of successive approximation A/D converters. The SHC803 and SHC804 have been designed with a fast-settling, low output-impedance amplifier to further minimize the effects of high frequency transient currents present in an output load.

A typical SHC804/ADC803 connection for high-speed digitization is illustrated in Figure 3. A short delay must occur before the A/D start command is asserted since the ADC803 makes its first conversion decision 100ns after the start command is asserted. Because the SHC804 sample-to-hold settling time is 150ns (maximum) the additional delay required is about 50ns. This can be achieved using a one-shot or by using the delay provided by the six inverters of a hex inverter integrated circuit. This combination can be triggered at rates of over 500k samples per second.

Using the input buffer of the SHC803 provides a high input impedance sample/hold for CMOS analog multiplexers such as the high speed Burr-Brown MPC800. The high input impedance of the SHC803 buffer minimizes DC errors caused by the ON resistance of the multiplexer switches and/or relatively high impedance signal sources (Figure 4). The multiplexer can be switched to a new channel as soon as the SHC803 is switched to the Hold mode. The multiplexer/buffer combination settles to the new input value during the sample/hold acquisition time and A/D conversion time. This "overlap" technique results in little or no loss in throughput rate.

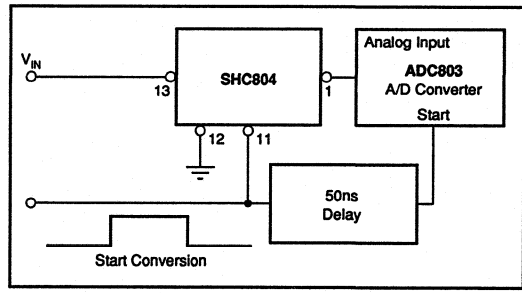


FIGURE 3. SHC804 and ADC803 Provide Sampling Rates Over 500k Samples Per Second.

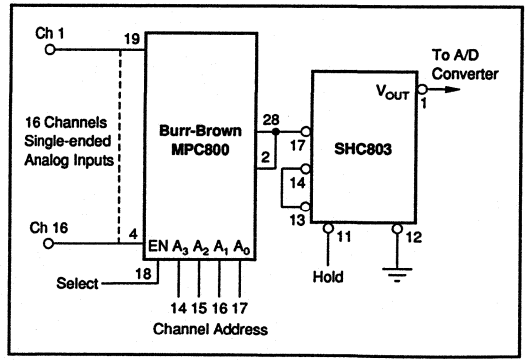


FIGURE 4. Using SHC803 With The MPC800 Analog Multiplexer.

9 Analog-to-Digital Converters

The Burr-Brown Analog-to-Digital (A/D) converter product line offers a broad selection of devices that enable you to choose the performance and price range ideally suited for your application. For example, the high-performance 12-bit ADC80, which converts to 12-bit accuracy in 25µs, was originated by Burr-Brown in 1975 and has become an industry standard. The ADC603 is a 12-bit, 10MHz A/D converter that offers the industry's highest performance for RF signal processing applications. A high-resolution converter, the ADC76, converts 16 bits to ±0.003% absolute accuracy in only 15µs and is packaged in a 32-pin triple-wide dual-in-line package. Another performance category is total harmonic distortion for audio digital recording.

All devices are complete and fully specified, with a track record of high reliability proven both in the field as well as in internal qualification testing.

The Selection Guide shows parameters for the high grade. Models shown in **boldface** are products included in this supplement.

INSTRUMENTATION ANALOG-TO-DIGITAL CONVERTERS

Description	Model	Resolution (Bits)	Linearity Error (%FSR)	Input Range (V)[1]	Conversion Time or Sampling Rate	NMC Resolution	Temp Range[2]	Pkg[3]	Q, BI[4] Screen	Page No.
Data-Bus Interface	**ADC700**	**16**	**±0.003**	**5, 10, 20 U/B**	**17µs**	**14**	**Mil, Ind, Com**	**TDIP**	**—**	**S-9.1.3**
Industry Std Pinouts	ADC71	16	±0.003	5, 10, 20 U/B	50µs	14	Ind, Com	TDIP	—	9.1-4
	ADC76	16	±0.003	5, 10, 20 U/B	17µs	14	Ind, Com	TDIP	—	9.1-12
Sampling 574 Type	**ADS574**	**12**	**±0.012**	**10, 20, U/B**	**40kHz**	**12**	**Ind**	**DIP, DDIP SO**	**—**	**S9.1.25**
Sampling 774 Type	**ADS774**	**12**	**±0.012**	**10, 20, U/B**	**8.5µs**	**12**	**Ind**	**DIP, DDIP SO**	**—**	**S9.1.48**
Sampling, Interface	**ADS7800**	**12**	**±0.012**	**10, 20 B**	**333kHz**	**12**	**Com, Ind**	**DIP SO**	**—**	**S9.1.63**
High-Accuracy,	**ADC7802**	**12**	**±0.012**	**0 to +5**	**8.5µs**	**12**	**Ind**	**DDIP, PLCC**	**—**	**S-9.2.184**
4-Channel, Auto-Calibration, Sampling	**ADS7803**	**12**	**±0.018**	**0 to +5**	**8.5µs**	**12**	**Ind**	**DDIP, PLCC**		**S-9.1.74**
Industry Std Pinout and Interface	ADC574A	12	±0.012	10, 20 U/B	25µs	12	Mil,Ind,Com	DDIP	BI	9.1-52
	ADC674A	12	±0.012	10, 20 U/B	15µs	12	Mil,Ind,Com	DDIP	BI	9.1-62
	ADC774	**12**	**±0.012**	**10, 20 U/B**	**8.5µs**	**12**	**Mil,Ind,Com**	**DDIP**	**BI**	**S-9.1.15**
Sampling	ADS807	12	±0.012	10, 20 U/B	100kHz	12	Mil,Ind,Com	DDIP	BI	9.1-86
Sampling	ADS808	12	±0.012	10, 20 U/B	100kHz	12	Mil,Ind,Com	DDIP	BI	9.1-86
Medium Speed Monolithic	ADC80AG	12	±0.012	5, 10, 20 U/B	25µs	12	Ind	TDIP	BI	9.1-20
	ADC80MAH	12	±0.012	5, 10, 20 U/B	25µs	12	Ind	TDIP	BI	9.1-36
Medium Speed	ADC84KG	12	±0.012	5, 10, 20 U/B	10µs	12	Ind	TDIP	BI	9.1-44
	ADC85H	12	±0.012	5, 10, 20 U/B	10µs	12	Com	TDIP	Q, BI	9.1-44
Mil Temperature Range	ADC87H	12	±0.012	5, 10, 20 U/B	10µs	12	Mil	TDIP	Q	9.1-44
Serial Output	ADC804	12	±0.012	5,10,20 U/B	17µs	12	Mil,Ind,Com	DDIP	Q, BI	9.1-78

NOTES: (1) U/B indicates the input voltage range for the model: U = unipolar, B = Bipolar. (2) Com = 0°C to +70°C, Ind = –25°C to +85°C, Mil = –55°C to +125°C. (3) DIP = 0.3" wide DIP, DDIP = 0.6" wide DIP, TDIP = 0.9" wide DIP, PLCC = Plastic Leaded Chip Carrier, SO = Small Outline Surface Mount. (4) Q indicates optional reliability screening is available for this model. BI indicates that an optional 160 hour burn-in is available for this model.

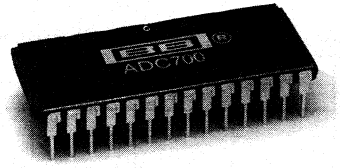
AUDIO, COMMUNICATIONS, DSP ANALOG-TO-DIGITAL CONVERTERS

Description	Model	Resolution (Bits)	Linearity Error, max(%FSR)	Input Range (V)	Sampling Rate	THD (dB, typ)	Temp Range[1]	Pkg[2]	Q[3] Screen	Page No.
High Accuracy, High Resolution	**ADC701**	**16**	**±0.003**	**10V/20V**	**1.5MHz**	**94w/SHC702**	**Com**	**TDIP**	**—**	**S-9.2.161**
	ADC750	**22**	**±0.003**	**10V**	**2.5MHz**	**—**	**Com**	**Board**	**—**	**S-9.2.177**
Sampling,	**ADC614**	**14**	**±0.003**	**±1.25**	**5.12MHz**	**88/N4QUIST**	**Com**	**DIP**	**—**	**S-9.2.147**
	ADC603	**12**	**±0.018**	**±1.25**	**10MHz**	**68**	**Com, Mil**	**DIP**	**—**	**S-9.2.128**
	ADC604	**12**	**±0.024**	**±1.25**	**5MHz**	**83**	**Com**	**DIP**	**—**	**S-9.2.119**
	ADC601	**12**	**±0.012**	**10V/20V**	**1.0MHz**	**70w/SHC802**	**Com**	**TDIP**		**S-9.2.112**
	ADS602	**12**	**±0.03**	**10V/20V**	**1MHz**	**66**	**Com**	**TDIP**	**—**	**S-9.1.40**

Description	Model	Resolution (Bits)	Typical Linearity Error	Input Range (V)	Conversion Time (µs)	THD+N dB, max (V_{IN} = ±FS)	Output Format	Pkg[1]	Page No.[4]
High Performance	PCM75	16	15-Bit 14-Bit	±2.5, ±5 ±10V	17	–84 (J) –88 (K)	Parallel or Serial	TDIP	9.2-136
Low Cost	**PCM78**	**16**	**14-Bit**	**±3**	**5**	**–88**	**Serial**	**DDIP**	**S-9.2.209**
Dual	**PCM1750**	**18**	**14-Bit**	**±2.75**	**5**	**–90 (P)**	**Serial**	**DDIP**	**S-6.2.196**
Single Channel	**DSP101**	**18**	**14-Bit**	**±2.75**	**5**	**–90**	**Serial**	**DDIP**	**S-9.1.89**
Dual Channel	**DSP102**	**18**	**14-Bit**	**±2.75**	**5**	**–90**	**Serial**	**DDIP**	**S-9.1.89**

NOTES: (1) DIP = 0.3" wide DIP, DDIP = 0.6" wide DIP, TDIP = 0.9" wide DIP, PLCC = Plastic Leaded Chip Carrier, SO = Small Outline Surface Mount.

BURR-BROWN®



ADC700

16-Bit Resolution With Microprocessor Interface A/D CONVERTER

FEATURES

- COMPLETE WITH REFERENCE, CLOCK, 8-BIT PORT MICROPROCESSOR INTERFACE
- CONVERSION TIME: 17µs max
- LINEARITY ERROR: ±0.003% FSR max
- NO MISSING CODES TO 14 BITS OVER TEMPERATURE
- SPECIFIED AT ±12V AND ±15V SUPPLIES
- OUTPUT BUFFER LATCH FOR IMPROVED INTERFACE TIMING FLEXIBILITY
- PARALLEL AND SERIAL DATA OUTPUT
- SMALL PACKAGE: 28-Pin DIP

DESCRIPTION

The ADC700 is a complete 16-bit resolution successive approximation analog-to-digital converter.

The reference circuit, containing a buried zener, is laser-trimmed for minimum temperature coefficient.

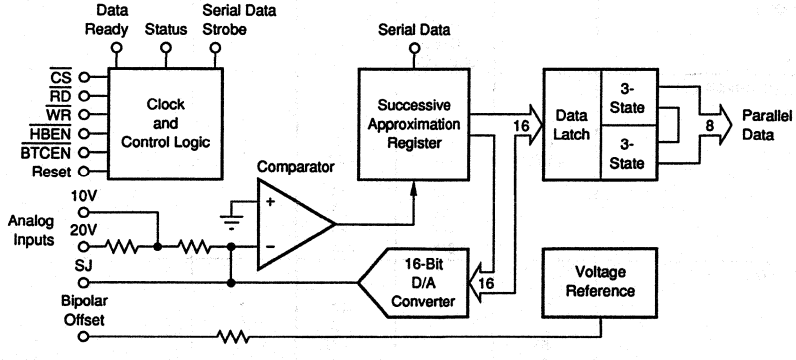
The clock oscillator is current-controlled for excellent stability over temperature. Gain and Zero errors may be externally trimmed to zero. Analog input ranges of 0V to +5V, 0V to +10V, 0V to +20V, ±2.5V, ±5V, and ±10V are available.

The conversion time is 17µs max for a 16-bit conversion over the three specification temperature ranges.

After a conversion, output data is stored in a latch separate from the successive approximation logic. This permits reading data during the next conversion, a feature that provides flexible interface timing, especially for interrupt-driven interfaces.

Data is available in two 8-bit bytes from TTL-compatible three-state output drivers. Output data is coded in Straight Binary for unipolar input signals and Bipolar Offset Binary or Twos complement for bipolar input signals. BOB or BTC is selected by a logic function available on one of the pins.

The ADC700 is available in commercial, industrial and military temperature ranges. It is packaged in a hermetic 28-pin side-braze ceramic DIP.



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Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL

T_A = 25°C and at rated supplies: V_{DD} = +5V, $+V_{CC}$ = +12V or +15V, $-V_{CC}$ = −12V or −15V unless otherwise noted.

CHARACTERISTICS	ADC700JH/AH/RH MIN	ADC700JH/AH/RH TYP	ADC700JH/AH/RH MAX	ADC700KH/BH/SH MIN	ADC700KH/BH/SH TYP	ADC700KH/BH/SH MAX	UNITS
RESOLUTION			16			*	Bits
ANALOG INPUTS							
Voltage Ranges							
Bipolar		±2.5, ±5, ±10			*		V
Unipolar		0 to +5, 0 to +10, 0 to +20			*		V
Impedance (Direct Input)							
0V to +5V, ±2.5V		2.5 ±1%			*		kΩ
0V to +10V, ±5V		5 ±1%			*		kΩ
0V to +20V, ±10V		10 ±1%			*		kΩ
DIGITAL SIGNALS (Over Specification Temperature Range)							
Inputs							
Logic Levels[1]							
V_{IH}	+2.0		+5.5	*		*	V
V_{IL}	0		+0.8	*		*	V
I_{IH} (V_I = +2.7V)			±10			*	µA
I_{IL} (V_I = +0.4V)			±20			*	µA
Outputs							
Logic Levels							
V_{OL} (I_{OL} = −1.6mA)			+0.4			*	V
V_{OH} (I_{OH} = +20µA)	+2.4			*			V
$I_{LEAKAGE}$							
Data Outputs Only, High Z		10			*		nA
TRANSFER CHARACTERISTICS							
ACCURACY							
Linearity Error			±0.006			±0.003	% of FSR[2]
Differential Linearity Error			±0.012			±0.006	% of FSR
Gain Error[3]		±0.1	±0.2		*	*	%
Zero Error[3]							
Bipolar Zero		±0.1	±0.2		*	*	% of FSR
Unipolar Zero		±0.05	±0.1		*	*	% of FSR
Noise at Transitions (3σp-p)		±0.001	±0.003		*	*	% of FSR
Power Supply Sensitivity							
$+V_{CC}$		±0.0015			*		%FSR/%V_{CC}
$-V_{CC}$		±0.0015			*		%FSR/%V_{CC}
V_{DD}		±0.0005			*		%FSR/%V_{DD}
DRIFT (Over Specification Temperature Range)							
Gain Drift		±8	±15		*	*	ppm/°C
Zero Drift							
Bipolar Zero		±5	±10		*	*	ppm of FSR/°C
Unipolar Zero		±2	±4		*	*	ppm of FSR/°C
Linearity Drift		±1	±3		*	±2	ppm of FSR/°C
No Missing Codes Temperature Range							
JH (13-bit), KH (14-bit)	0		+70	*		*	°C
AH (13-bit), BH (14 bit)	−25		+85	*		*	°C
RH (13-bit), SH (14-bit)	−55		+125	*		*	°C
CONVERSION TIME 16 bits		15	17		*	*	µs
WARM-UP TIME	5			*			min
OUTPUT DATA CODES[4]							
Unipolar Parallel		USB			*		
Bipolar Parallel[5]		BTC, BOB			*		
Serial Output (NRZ)		USB, BOB			*		
POWER SUPPLY REQUIREMENTS							
Voltage Range							
$+V_{CC}$	+11.4	+15	+16	*	*	*	VDC
$-V_{CC}$	−11.4	−15	−16	*	*	*	VDC
V_{DD}	+4.75	+5	+5.25	*	*	*	VDC
Current[5]							
$+V_{CC}$		+10	+15		*	*	mA
$-V_{CC}$		−28	−35		*	*	mA
V_{DD}		+17	+20		*	*	mA
Power Dissipation		645	765		*	*	mW
TEMPERATURE RANGE							
Specification							
J, K Grades	0		+70	*		*	°C
A, B Grades	−25		+85	*		*	°C
R, S Grades	−55		+125	*		*	°C
Storage	−65		+150	*		*	°C

TIMING SPECIFICATIONS[6]

V_{DD} = +5V, $+V_{CC}$ = +12V or +15V, $-V_{CC}$ = −12V or −15V unless otherwise noted.

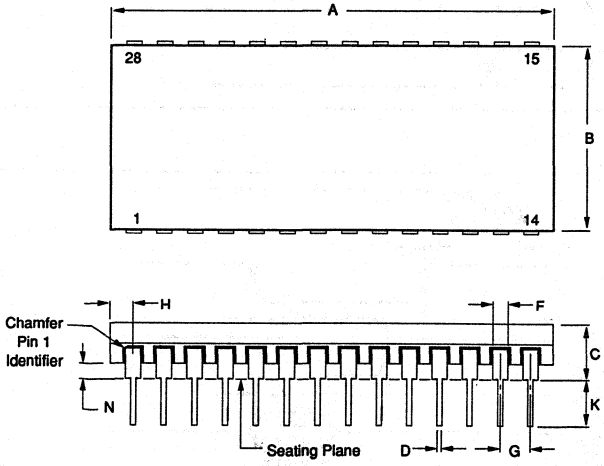
PARAMETER	LIMIT AT T_A = 25°C	LIMIT AT T_A = 0, +70°C −25°C, +85°C	LIMIT AT T_A = −55°C, +125°C	UNITS	DESCRIPTION
CONVERSION AND SERIAL DATA OUTPUT TIMING					
t_1	0	0	0	ns, min	$\overline{CS}$ to $\overline{WR}$ Setup time
t_2	110	130	145	ns, max	$\overline{WR}$ to Status delay
t_3	40	40	40	ns, min	$\overline{WR}$ pulse width
t_4	0	0	0	ns, min	$\overline{CS}$ to $\overline{WR}$ Hold time
t_5	15	17	17	µs, max	Conversion time
t_6	550	600	650	ns, max	Data Ready to Status time
t_7	1100	1150	1250	ns, max	$\overline{WR}$ to first Serial Data Strobe
t_8	250	210	200	ns, min	First Serial Data to first Serial Data Strobe
t_9	310	360	400	ns, max	Last Serial Data Strobe to Status
t_{10}	0	0	0	ns, min	Status to $\overline{WR}$ Setup time
PARALLEL DATA OUTPUT TIMING					
t_{11}	0	0	0	ns, min	$\overline{HBEN}$ to $\overline{RD}$ Setup time
t_{12}	0	0	0	ns, min	$\overline{CS}$ to $\overline{RD}$ Setup time
t_{13}[7]	50	58	66	ns, max	High Byte Data Valid after $\overline{RD}$ C_L = 20pF (High Byte bus access time)
	70	81	95	ns, max	High Byte Data Valid after $\overline{RD}$ C_L = 100pF (High Byte bus access time)
t_{14}	40	40	40	ns, min	$\overline{RD}$ pulse width
t_{15}	40	45	50	ns, max	Data Ready delay from $\overline{RD}$ ($\overline{HBEN}$ asserted)
t_{16}[8]	50	60	65	ns, max	Data Hold time after $\overline{RD}$ (bus relinquish time)
t_{17}	0	0	0	ns, min	$\overline{RD}$ to $\overline{CS}$ Hold time
t_{18}	0	0	0	ns, min	$\overline{RD}$ to $\overline{HBEN}$ Hold time
RESET TIMING					
t_{19}	60	70	80	ns, max	Data Ready low delay from $\overline{Reset}$
t_{20}	70	81	95	ns, max	Status low delay from $\overline{Reset}$

*Same specs as ADC700JH, AH, RH.

NOTES: (1) TTL, LSTTL, and 5V CMOS compatible. (2) FSR means Full Scale Range. For example, unit connected for ±10V range has 20V FSR. (3) Externally adjustable to zero. (4) See Table I. USB – Unipolar Straight Binary; BTC – Binary Two's Complement; BOB – Bipolar Offset Binary; NRZ – Non Return to Zero. (5) Max supply current is specified at rated supply voltages. (6) All input control signals are specified with $t_{RISE} = t_{FALL}$ = 5ns (10% to 90% of 5V) and timed from a voltage level of 1.6V. (7) t_{13} is measured with the load circuits of Figure 1 and defined as the time required for an output to cross 0.8V or 2.4V. (8) t_{16} is defined as the time required for the data lines to change 0.5V when loaded with the circuits of Figure 2.

MECHANICAL

H Package — 28-Pin Ceramic DIP



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.435	1.465	36.45	37.21
B	.610 BASIC		15.49 BASIC	
C	.160	.205	4.06	5.21
D	.015	.019	.38	.48
F	.045	.055	1.14	1.40
G	.100 BASIC		2.54 BASIC	
H	.055	.095	1.40	2.41
J	.009	.012	.23	.30
K	.125	.180	3.18	4.57
L	.600 BASIC		15.24 BASIC	
N	.040	.060	1.02	1.52

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.

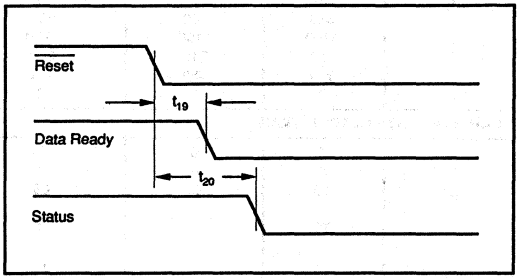
ORDERING INFORMATION

MODEL	TEMPERATURE RANGE	LINEARITY ERROR (%FSR)
ADC700JH	0°C to 70°C	±0.006
ADC700KH	0°C to 70°C	±0.003
ADC700AH	–25°C to +85°C	±0.006
ADC700BH	–25°C to +85°C	±0.003
ADC700RH	–55°C to +125°C	±0.006
ADC700SH	–55°C to +125°C	±0.003

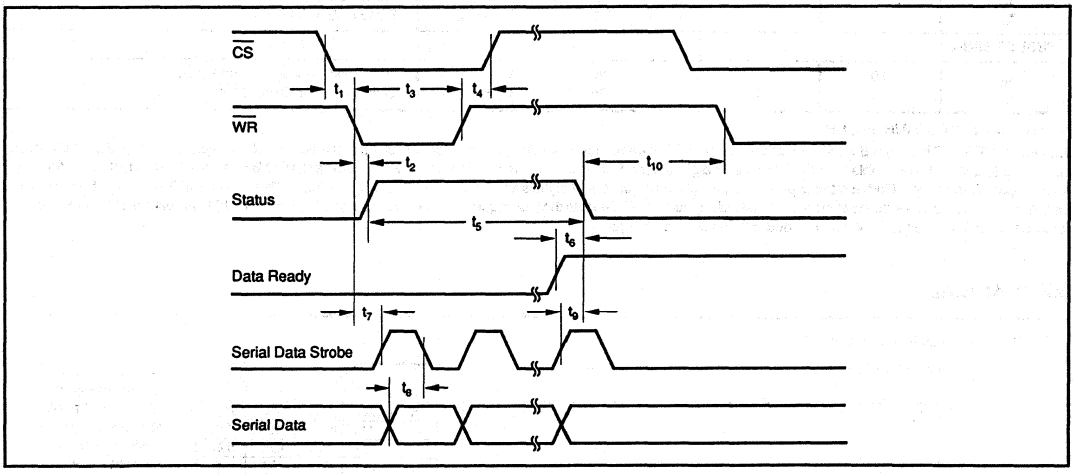
ABSOLUTE MAXIMUM RATINGS

$+V_{DD}$ to Digital Common	0V to +7V
$+V_{CC}$ to Analog Common	0V to +18V
$-V_{CC}$ to Analog Common	0V to –18V
Digital Common to Analog Common	–1V to +1V
Digital Inputs to Digital Common	–0.5V to V_{DD} + 0.5V
Analog Inputs	+16.5V
Power Dissipation	1000mW
Storage Temperature	–60°C to +150°C
Lead Temperature, (soldering, 10s)	+300°C

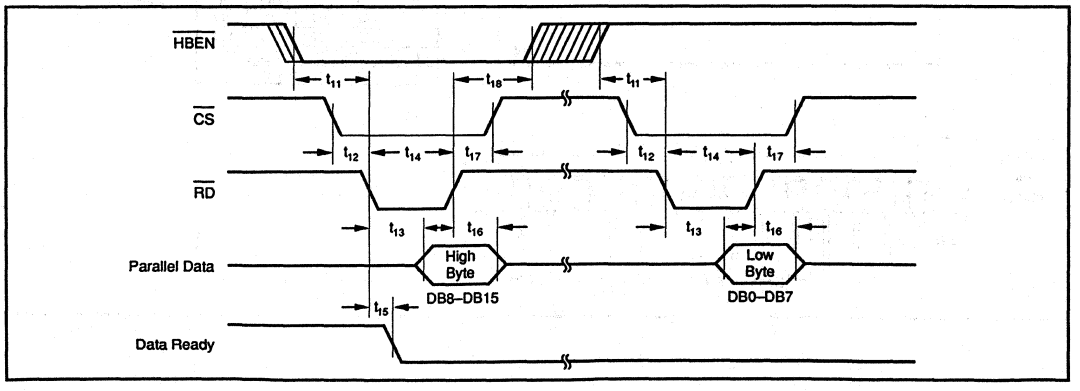
NOTES: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



ADC700 Reset Function Timing Diagram.

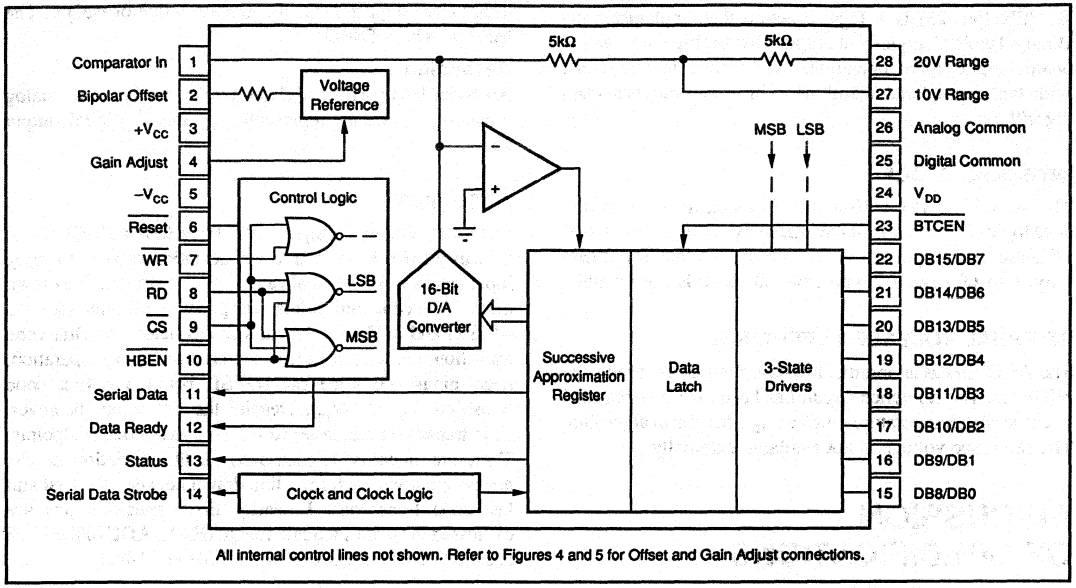


Start of Conversion and Serial Data Output Timing.



ADC700 Parallel Output Timing.

PIN CONFIGURATION



All internal control lines not shown. Refer to Figures 4 and 5 for Offset and Gain Adjust connections.

DESCRIPTION AND OPERATING FEATURES

The ADC700 is a 16-bit resolution successive approximation A/D converter. Parallel digital data as well as serial data is available. Several features have been included in the ADC700 making it easier to interface with microprocessors and/or serial data systems. Several analog input ranges are available.

Some of the key operating features are described here. More detail is given in later sections of the data sheet. Refer to the block diagram above.

RESET

The ADC700 has a $\overline{\text{Reset}}$ input that must be asserted upon power-up or after a power interruption. This initializes the SAR, the output buffer register and Data Ready flag. Since microprocessor systems already use a power-on reset circuit, the same system reset signal can be used to initialize the ADC700.

PARALLEL DATA

The parallel data output is available through an 8-bit port with 3-state output drivers. High byte and low byte are selected by $\overline{\text{HBEN}}$ (pin 10).

A buffer/latch is included between the successive approximation register (SAR) and the 3-state drivers. This feature permits more flexible interface timing than is possible from most successive approximation converters.

The "old" word can be read during the next conversion. A Data Ready flag (pin 12) is asserted when a "new" word is in the buffer register. The Data Ready flag goes low ("0") when the most significant byte (high byte) is read. If the "old" word is not read, or if only the least significant byte (low byte) is read, Data Ready is not reset. The next conversion output will overwrite the data latch when the conversion is complete. The Data Ready flag remains high. Refer to timing diagrams in the Specifications section.

SERIAL DATA

Sixteen-bit serial data output is available (pin 11) along with a serial output strobe (pin 14). This serial data strobe is not the internal SAR clock but is a special strobe for serial data consisting of 16 negative-going edges (during conversion) occurring about 200ns after each serial data bit is valid. This feature eases the interface to shift registers or through opto-couplers for applications requiring galvanic isolation.

STATUS

The familiar Status (or Busy) flag, present in successive approximation A/D converters, is available (pin 13) and indicates that a conversion is in progress. Status is valid 110ns after assertion of the convert command ($\overline{\text{WR}}$ low). Status cannot be used as a sample-hold control because there is not enough time for the sample-hold to settle to the required error band before the ADC700 makes its first conversion decision.

CHIP SELECT

$\overline{\text{CS}}$ (pin 9) selects the ADC700. No other functions can be implemented unless $\overline{\text{CS}}$ is asserted. $\overline{\text{WR}}$ (pin 7) is the start-of-conversion strobe. $\overline{\text{RD}}$ strobes each output data byte, selected by $\overline{\text{HBEN}}$ (pin 10), to the 3-state drivers.

TWO'S COMPLEMENT DATA CODE

$\overline{\text{BTCEN}}$ (pin 23) is a logic function that implements the Binary Two's Complement output code for bipolar (+ and –) analog input signal operation. This feature is compatible with twos complement arithmetic in microprocessor math algorithms.

INTERNAL CLOCK

The ADC700 has a self-contained clock to sequence the A/D logic. The clock is not available externally. An external 16-pulse strobe (pin 14) is brought out to clock serial data only. Use of ADC700 with external clock is not possible.

INTERNAL VOLTAGE REFERENCE

The ADC700 has an internal low-noise buried-zener voltage reference. The reference circuit has been drift compensated over the MIL temperature range using a laser trim algorithm. The reference voltage is not available externally.

DISCUSSION OF SPECIFICATIONS

BASIC DEFINITIONS

Refer to Figure 3 for an illustration of A/D converter terminology and to Table II in the Calibration section.

Full Scale Range, FSR

The nominal range of the A/D converter. For ADC700, the FSR is 20V for the 0V to +20V and the –10V to +10V input ranges or 10V for the 0V to +10V and –5V to +5V input ranges.

Least Significant Bit, LSB

The smallest analog input change resolved by the A/D converter. For an A/D converter with N bits output, the input value of the LSB is FSR(2^{-N}).

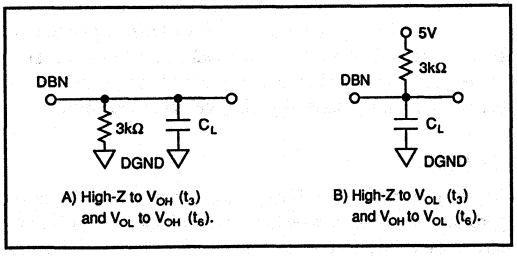


FIGURE 1. Load Circuits for Access Time.

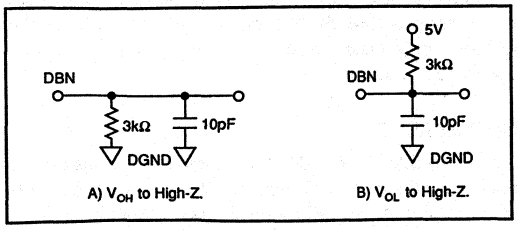


FIGURE 2. Load Circuits for Output Float Delay.

Most Significant Bit, MSB

That binary digit that has the greatest value or weight. The MSB weight is FSR/2.

Resolution

An N-bit binary-coded A/D converter resolves the analog input into 2^N values represented by the 2^N digital output codes.

ACCURACY

Linearity Error, Integral Linearity Error (ILE)

Linearity Error is defined as the deviation of actual analog input values from the ideal values about a straight line drawn through the code mid-points near positive full scale (at $+V_{FS}$ –1LSB) and at Zero input (at 1/2LSB below the first code transition, i.e. at Zero) or, in the case of bipolar operation, near minus full scale (at 1/2LSB below the first code transition, i.e. at $-V_{FS}$). Despite the definition, however, code transitions are easier to measure than code midpoints. Therefore linearity is measured as the deviation of the analog input values from a line drawn between the first and last code transitions. Linearity Error specifications are expressed in % of Full Scale Range (FSR). ADC700KH ILE is ±0.003% of FSR which is 1/2 LSB at 14-bits.

Differential Linearity Error (DLE), No Missing Codes

Differential Linearity Error is defined as the deviation in code width from the ideal value of 1LSB. If the DLE is greater than –1LSB anywhere along the range, the A/D will have at least one missing code. ADC700KH is specified to have a DLE of ±0.006% of FSR, which is ±1LSB at 14 bits. ADC700KH is specified to have *no missing codes* at the 14-bit level over specified temperature ranges.

Gain Error

The deviation from the ideal magnitude of the input span between the first code midpoint (at $-V_{FS}$ + 1/2LSB, for bipolar operation; at Zero for unipolar operation) to the last code midpoint (V_{FS} –1LSB). As with the linearity error

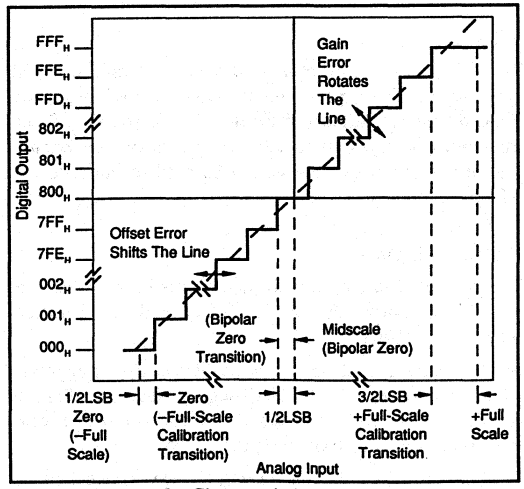


FIGURE 3. Transfer Characteristic Terminology.

measurements, code transition values are the locations actually measured for this spec. The ideal gain is V_{FSR} –2LSB. Gain Error is expressed in % (of reading). See Figure 3.

Gain Error of the ADC700 may be trimmed to zero using external trim potentiometers.

Offset Error

Unipolar Offset Error—The deviation of the actual code-midpoint value of the first code from the ideal value located at 1/2LSB below the ideal first transition value (i.e. at zero volts).

Bipolar Offset Error—The deviation of the actual code-midpoint of the first code from the ideal value located at 1/2LSB below the ideal first transition value located at – V_{FS} +1/2LSB.

Again, transition values are the actual measured parameters. Offset and Zero errors of the ADC700 may be trimmed to zero using external trim potentiometers. Offset Error is expressed as a percentage of FSR.

Bipolar Zero Error—The deviation of the actual mid-scale-code midpoint value from zero. Transition values are the actual measured parameter and it is 1/2 LSB below zero volts. The error is comprised of Bipolar Offset Error, 1/2 the Gain Error, and the Linearity Error of bit 1. Bipolar Zero Error is expressed as a percentage of FSR.

Power Supply Sensitivity

Power Supply Sensitivity describes the maximum change in the full-scale transition value from the initial value for a change in each power supply voltage. PSR is specified in units of %FSR/% change in each supply voltage.

The major effect of power supply voltage deviations from the rated values will be a small change in the Gain (scale factor). Power Supply Sensitivity is also a function of ripple frequency. Figure 4 illustrates typical Power Supply Sensitivity performance of ADC700 versus ripple frequency.

INSTALLATION

POWER SUPPLY SELECTION

Linear power supplies are preferred. Switching power supply specifications may appear to indicate low noise output, but these specifications are rms specs. The spikes generated in switchers may be hard to filter. Their high-frequency components may be extremely difficult to keep out of the power supply return system. If switchers must be used, their outputs must be carefully filtered and the power supply itself should be shielded and located as far away as possible from precision analog circuits.

LAYOUT CONSIDERATIONS

Because of the high resolution and linearity of the ADC700, system design problems such as ground path resistance and contact resistance become very important. For a 16-bit resolution converter with a +10V Full-Scale Range, 1LSB is 153µV. Circuit situations that cause only second- or third-order errors in 8-, 10-, or 12-bit A/D converters can induce first-order errors in 16-bit resolution devices.

Power Supply Wiring

Use heavy power supply and power supply common (ground) wiring. A ground plane is usually the best solution for preserving dynamic performance and reducing noise coupling into sensitive converter circuits.

When passing converter power through a connector, use every available spare pin for making power supply return connections, and use some of the pins as a Faraday shield to separate the analog and digital common lines.

Power Supply Returns (Analog Common and Digital Common)

Connect Analog Common and Digital Common together right at the converter with the ground plane. This will usually give the best performance. However, it may cause problems for the system designer. Where it is absolutely necessary to separate analog and digital power supply returns, each should be separately returned to the power supply. Do not connect Analog Common and Digital Common together and then run a single wire to the power supply. Connect a 1 to 47µF tantalum capacitor between Digital Common and Analog Common pins as close to the package as possible.

Power Supply Bypassing

Every power-supply line leading into an A/D converter must be bypassed to its common pin. The bypass capacitor should be located as close to the converter package as possible and tied to a solid ground—connecting the capacitors to a noisy ground defeats the purpose of the bypass. Use tantalum capacitors with values of from 10µF to 100µF and parallel them with smaller ceramic capacitors for high frequency filtering if necessary.

Separate Analog and Digital Signals

Digital signals entering or leaving the layout should have minimum length to minimize crosstalk to analog wiring. Keep analog signals as far away as possible from digital signals. If they must cross, cross them at right angles. Coaxial cable may be necessary for analog inputs in some situations.

Shield Other Sensitive Points

The most critical of these is the comparator input (pin 1). If this pin is not used for offset adjustment, then it should be surrounded with ground plane or low-impedance power

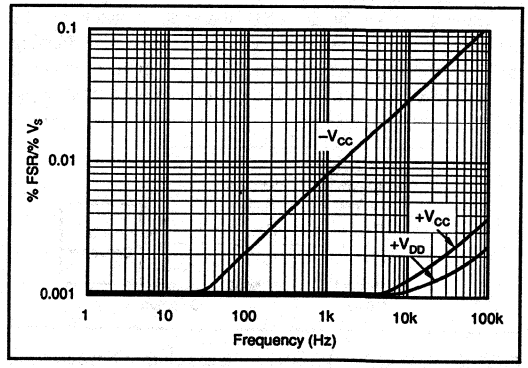


FIGURE 4. Power Supply Rejection Ripple vs Frequency.

supply plane. If it is used for offset adjustment, the series resistor and potentiometer should be located as close to the converter as possible.

The Gain Adjust (pin 4) is an input that has a relatively high input impedance and is susceptible to noise pickup. The Gain Adjust pin should be bypassed with a 0.01µF to 0.1µF capacitor whether or not the gain adjust feature is used.

If the 20V Analog input range is used (pin 28), the 10V Range input (pin 27) may need to be shielded with ground plane to reduce noise pickup.

ANALOG SIGNAL SOURCE IMPEDANCE

The input impedance of the ADC700, typical of most successive approximation A/D converters, is relatively low (2.5kΩ to 10kΩ). The input current of a successive approximation A/D converter changes rapidly during the conversion algorithm as each bit current is compared to the analog input current. Since the output impedance of a closed-loop amplifier or a sample-hold amplifier increases with frequency and, in addition, the amplifier must settle to the required accuracy in time for the next comparison/decision after such a disturbance, care must be taken to select the proper driving amplifier.

Unfortunately, high-accuracy operational amplifiers tend to have low bandwidth, while wide-band amplifiers tend to have lower accuracy. One solution is to use a wide-band but perhaps less precise amplifier. Another solution is to add a wide-band buffer amplifier such as the Burr-Brown OPA633 inside the feedback loop of a slower (but precision) amplifier, Figure 5. This reduces the output impedance at high frequencies yet preserves the accuracy at low frequencies. When a sample/hold is needed, a high-linearity, high-speed sample/hold such as the Burr-Brown SHC76 should be used to drive the ADC700.

ANALOG INPUT RANGES

The analog input circuits of the ADC700 can be connected to accept unipolar or bipolar input signals. These ranges and connections are tabulated in Table I. Circuit connections are shown in Figures 6 and 7. Gain and offset adjustments are described in the calibration section.

To operate the ADC700 with a range that gives other convenient values for the LSB, the input resistor may be increased or decreased slightly without seriously affecting the Gain Drift of the converter. Since the input resistors of the ADC700 are within ±2% from unit to unit, this can be consistently done with a fixed series or parallel resistor. The ADC700 can then be calibrated using the Gain and Offset adjustments described in the calibration section. For example, using the ±10V input range, one can decrease the range slightly by paralleling the 10kΩ input resistor (pin 28 to pin 1) with a 610kΩ metal film resistor to achieve a 300µV LSB instead of the nominal standard 305.17578µV binary LSB.

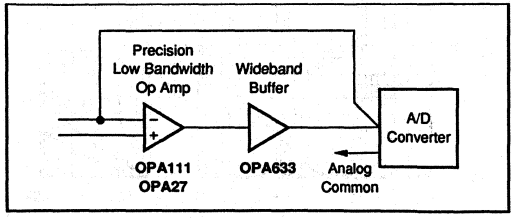


FIGURE 5. Wideband Buffer Reduces Output Impedance at High Frequencies.

OPTIONAL EXTERNAL GAIN AND OFFSET TRIM

Gain and Offset Error may be trimmed to zero using external Gain and Offset trim potentiometers connected to the ADC700 as shown in Figures 6 and Figure 7. A calibration procedure in described in the Operating Instructions section.

Multiturn potentiometers with 100ppm/°C or better TCR are recommended for minimum drift over temperature. These potentiometers may be any value from 10kΩ to 100kΩ. All resistors should be 20% carbon or better. Pin 1 (Comparator In) and pin 4 (Gain Adjust) may be left open if no external adjustment is planned; however, pin 4 should always be bypassed with 0.01µF or larger to Analog Common.

OPERATING INSTRUCTIONS

CALIBRATION

Offset and Gain may be trimmed by external Offset and Gain potentiometers. Offset is adjusted first and then Gain. Calibration values are listed in Table II for all ADC700 input ranges. Offset and Gain calibration can be accomplished to a precision of about ±1/2LSB using a static adjustment procedure described below. By summing a small sine or triangular wave voltage with the accurate calibration voltage applied to the analog input, the output can be swept through each of the calibration codes to more accurately determine the transition points listed in Table II. NOTE: The transition points are not the same as the code midpoints used in the static calibration example.

OFFSET ADJUSTMENT, 14-BIT RESOLUTION EXAMPLE

Static Adjustment Procedure (At Code Midpoints)

0V to +10V Range—Set the analog input to $+1LSB_{14}$ = 0.00061V. Adjust the Offset potentiometer for a digital output of 0004_H. Set the analog input to +Full Scale $-2LSB_{14}$ = +9.9987V. Adjust the Gain potentiometer for a digital output of $FFFC_H$. For a half-scale calibration check, set the analog input to +5.0000V and read a digital output code of 8000_H.

INPUT SIGNAL RANGE	OUTPUT CODE		CONNECT PIN 2 TO PIN	CONNECT PIN 28 TO PIN	CONNECT SIGNAL TO PIN
	$\overline{BTCEN}$ = 1	$\overline{BTCEN}$ = 0			
-10V	BOB	BTC	1	Input Signal	28
-5V	BOB	BTC	1	Open	27
-2.5V	BOB	BTC	1	Pin 1	27
0V to +5V	USB		26	Pin 1	27
0V to +10V	USB		26	Open	27
0V to +20V	USB		26	Input Signal	28

TABLE I. ADC700 Input Range Connections.

ANALOG INPUT RANGE	VOLTAGE (V)					
	±10	±5	±2.5	0 TO +20	0 TO +10	0 TO +5
$+V_{FS}$	+10	+5	+2.5	+20	+10	+5
$-V_{FS}$	–10	–5	–2.5	0	0	0
FSR	20	10	5	20	10	5
TRANSITION CODES (Hexadecimal)	**TRANSITION VALUES (V)**					
For 16-bit Resolution (Reading all 16 bits)						
$FFFE_H$ to $FFFF_H$	+9.999542	+4.999771	+2.499886	+19.999542	+9.99971	+4.999886
$7FFF_H$ to 8000_H	–152.5µV	–38µV	–19µV	+9.999847	+4.999924	+2.499962
0000_H to 0001_H	–9.999847	–4.999924	–2.499962	+152µV	+76µV	+38µV
LSB (FSR/2^{16})	305µV	153µV	38µV	305µV	153µV	76µV
For 15-bit Resolution (Reading all 16 bits, ignoring DB_0)						
$FFFD_H$ to $7FFE_H$	+9.999084	+4.999542	+2.499771	+19.999084	+9.999542	+4.999771
$7FFE_H$ to 8000_H	–305µV	–153µV	–76µV	+9.999625	+4.999847	+2.499924
0000_H to 0002_H	–9.999695	–4.999847	–2.499924	+305µV	+152µV	+76µV
LSB (FSR/2^{15})	610µV	305µV	153µV	610µV	305µV	153µV
For 14-bit Resolution (Reading all 16 bits, ignoring DB_0 and DB_1)						
$FFFC_H$ to $FFFD_H$	+9.99817	+4.99908	+2.49954	+19.99817	+9.99908	+4.99954
$7FFD_H$ to 8000_H	–610µV	–305µV	–153µV	+9.99939	+4.999695	+2.499847
0000_H to 0004_H	–9.999390	–4.999694	–2.499847	+610µV	+305µV	+153µV
LSB (FSR/2^{14})	1221µV	610µV	305µV	1221µV	610µV	305µV

TABLE II. Transition Values for Calibration.

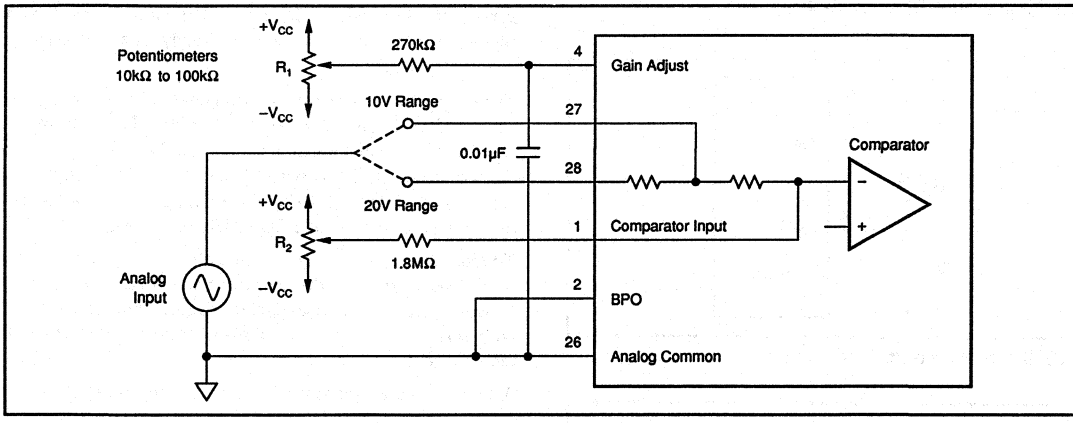


FIGURE 6. Unipolar Input Configuration with Gain and Offset Adjust Connections.

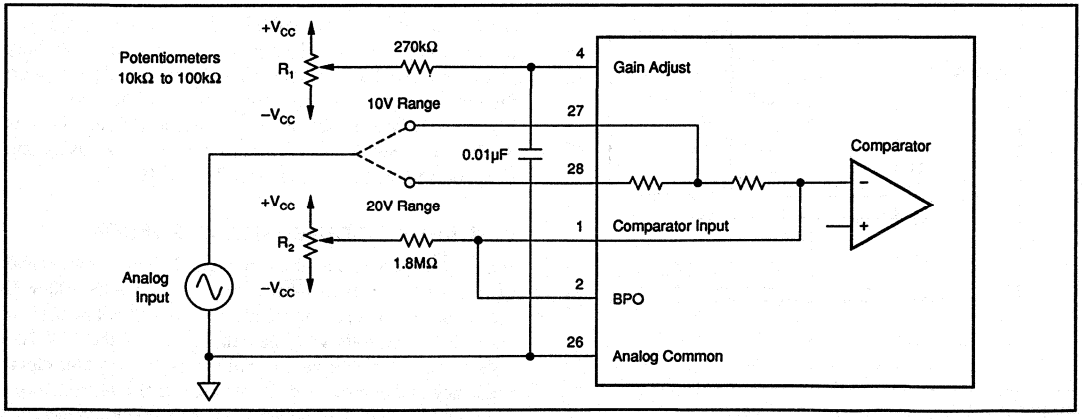


FIGURE 7. Bipolar Input Configuration with Gain and Offset Adjust Connections.

–10V to +10V Range—Set the analog input to –FS + $1LSB_{14}$ = –9.99878V. Adjust the Offset potentiometer for a digital output of 0004_H (8004_H if $\overline{BTCEN}$ is asserted). Set the analog input to +9.9976V. Adjust the Gain potentiometer for a digital output of $FFFC_H$ ($7FFC_H$ if $\overline{BTCEN}$ is assrted). For a half-scale calibration check, set the analog input to 0.0000V and read a digital output code of 8000_H (0000_H if $\overline{BTCEN}$ is asserted).

CONTROLLING AND INTERFACING THE ADC700

RESET

The ADC700 requires a Reset command upon power-up or after a power interruption to guarantee the condition of internal registers. If Status powers-up High, no conversion can be started. Reset initializes the SAR, the output buffer register, and the Data Ready flag and terminates a conversion in progress. Since microprocessor systems already use a power-on reset circuit, the same system reset signal can be used to initialize the ADC700. A power-up circuit is shown in Figure 8. Refer to Reset function timing diagram following the Timing Specifications Table.

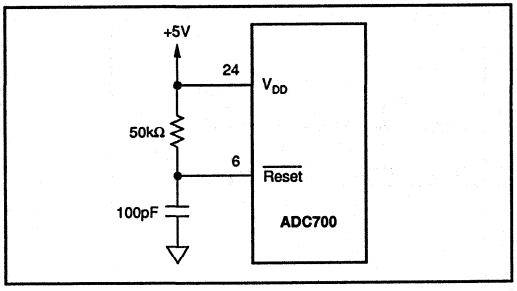


FIGURE 8. Power-Up Reset Circuit.

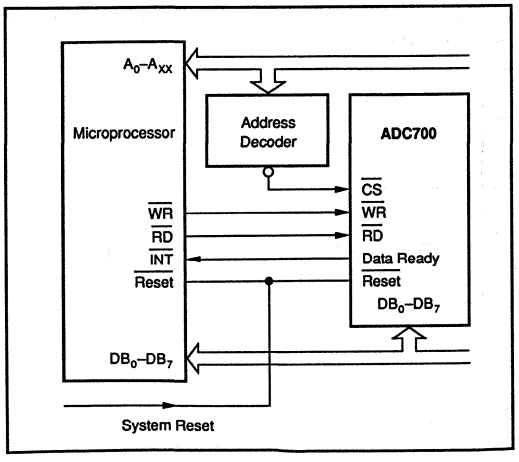


FIGURE 9. Parallel Data Bus Interface.

START OF CONVERSION

A conversion is started by asserting $\overline{CS}$ and $\overline{WR}$ Low. Status goes high about $t = t_1 + t_2$ = 110ns later. The first successive approximation decision occurs about 900ns after $\overline{WR}$ is asserted. Status goes Low after the conversion is complete. Refer to Start of Conversion and Serial Data Output Timing following the Timing Specifications Table.

DATA READY FLAG

The data latch feature permits data to be read during the following conversion. The Data Ready flag indicates that the data from the most recent conversion is latched in the output data latch and that it hasn't been read. Data Ready remains High until the most significant data byte is read. If a subsequent conversion is initiated and completed, the new word will be stored in the output data latch regardless of the state of the Data Ready flag. The preceding word will be overwritten and lost.

READING PARALLEL DATA

Parallel data is latched in the output data latch at the end of a conversion. Data can be read any time, even during the subsequent conversion. The output data latch is not cleared by reading the data. Only the Data Ready flag is cleared by reading the MSB.

The output three-state drivers are enabled by asserting the $\overline{CS}$ and $\overline{RD}$ inputs Low. When $\overline{HBEN}$ is Low, the most significant eight bits are enabled and the Data Ready flag is cleared. When $\overline{HBEN}$ is High, the least significant eight bits are enabled. Refer to Parallel Data Output Timing information following the Timing Specifications Table.

To reduce noise interference to the absolute minimum, data should be read after the current conversion is complete. However, data can be read during the following conversion, with minimal interference, to maximize the sampling rate of the converter.

A typical parallel interface is illustrated in Figure 9.

READING SERIAL DATA

Serial data output of the ADC700 is facilitated by a Serial Data Strobe that provides 16 negative-going edges for strobing an external serial to parallel shift register located perhaps on the other side of an opto-coupler. Refer to the Serial Data Timing information following the Timing Specifications Table. An example of an isolation connection using the serial port feature is illustrated in Figure 10.

CONTINUOUS CONVERSION OPERATION

When $\overline{CS}$ is permanently connected to Digital Common and Status is connected to $\overline{WR}$, Figure 11, the ADC700 will continuously convert. The repetition time will not be precise and will vary slightly with the temperature for the ADC700 because the time will be determined by the internal clock frequency and control-circuit gate delays. If a precise repetition rate is needed, the continuous conversion connection should not be used.

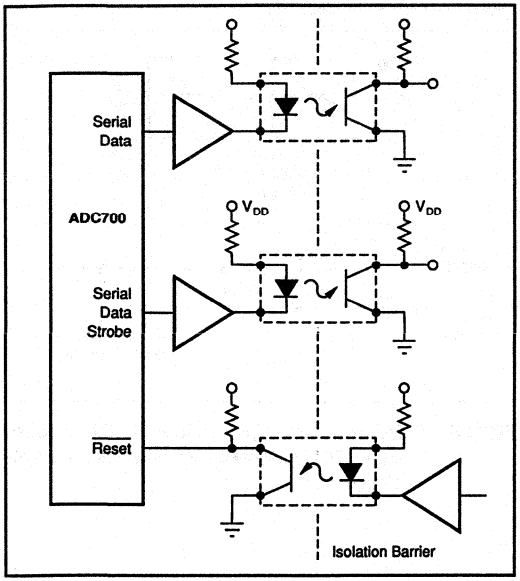


FIGURE 10. Serial Data Output Providing Convenient Isolation.

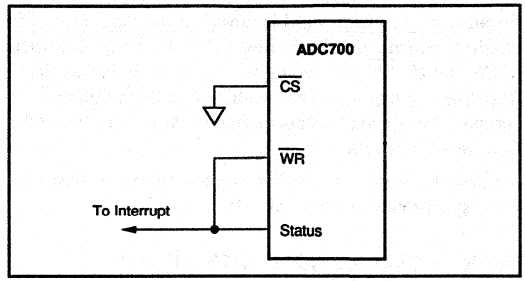


FIGURE 11. Continuous Conversion Circuit Connection.

PIN DESIGNATION	DEFINITION	FUNCTION
$\overline{CS}$ (Pin 9)	Chip Select	Must be Low to either initiate a conversion or read output data.
$\overline{WR}$ (Pin 7)	Write (Convert)	Conversion begins after the High-to-Low transition.
$\overline{RD}$ (Pin 8)	Read	Turns ON the three-state output drivers upon being asserted low.
$\overline{HBEN}$ (Pin 10)	High Byte Enable "1" = Low Byte "0" = High Byte	Selects the MSB or the LSB for readout. Data Ready is cleared when $\overline{HBEN}$ is Low and $\overline{RD}$ is asserted.
$\overline{Reset}$ (Pin 6)	Reset	Resets internal logic. Must be asserted after power-up or a power interruption clears Status and Data Ready to Low.
$\overline{BTCEN}$ (Pin 23)	BTC Enable	Sets the output code to Binary Twos Complement (BTC) when Low. Output code is Bipolar Offset Binary (BOB) when High.

TABLE III. Control Line Functions.

CONTROL LINE					
$\overline{RESET}$	$\overline{WR}$	$\overline{RD}$	$\overline{HBEN}$	$\overline{CS}$	OPERATION
0	X	X	X	X	Reset converter logic. Status and Data Ready set Low.
1	X	X	X	1	No operation.
1	0	X	X	0	Initiate conversion.
1	1	0	0	0	Places High Byte on output port. Clears Data Ready flag.
1	1	0	1	0	Placed Low Byte on output port. Does not clear Data Ready flag.
1	0	0	0	0	Initiates conversion and places High Byte or output port. Clears Data Ready.
1	0	0	1	0	Initiates conversion and places Low Byte on output port. Does not clear Data Ready flag.
NOTE: If a conversion command is asserted while a conversion is in progress, the command is ignored. If the conversion command remains asserted when a conversion is finished, a new conversion will begin.					

TABLE IV. Control Input Truth Table.

Because the last data-word is stored in the data latch, it is possible to read it during the next A/D conversion. Assertion of $\overline{CS}$ and $\overline{HBEN}$ for reading parallel data should be timed from Status going low. The two-byte read operation must be complete before the conversion in process is complete or the Data Read is invalid.

Serial Data is available during continuous conversion with word synchronization available from STATUS.

USING A SAMPLE/HOLD WITH ADC700

Figure 12 illustrates using ADC700 with the Burr-Brown SHC76. The sample-to-hold settling time (to 14 bits, ±0.003%FSR) of the SHC76 is 1µs typ, 3µs max. The time from the Status going High to the first conversion decision is about 900ns. Therefore a time delay between the Sample-to-Hold command to the $\overline{WR}$ command to the ADC700 is required.

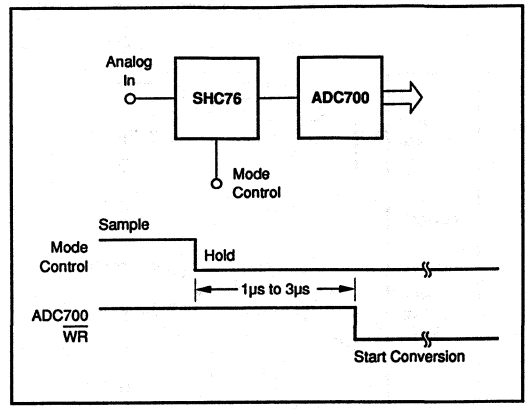
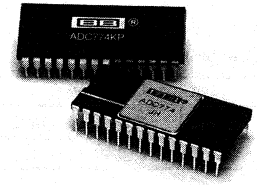


FIGURE 12. Using Sample/Hold with ADC700 Requires Time Delay Between Sample and Start-of-Conversion.

BURR-BROWN®



ADC774

Microprocessor-Compatible ANALOG-TO-DIGITAL CONVERTER

FEATURES

- **COMPLETE 12-BIT A/D CONVERTER WITH REFERENCE, CLOCK, AND 8-, 12-, or 16-BIT MICROPROCESSOR BUS INTERFACE**
- **ALTERNATE SOURCE FOR HI774 A/D CONVERTER: 8.5µs Conversion Time, 150ns Bus Access Time**
- **FULLY SPECIFIED FOR OPERATION ON ±12V OR ±15V SUPPLIES**
- **NO MISSING CODES OVER TEMPERATURE:**
  0°C to +75°C: ADC774J, K
  –55°C to +125°C: ADC774SH, TH

DESCRIPTION

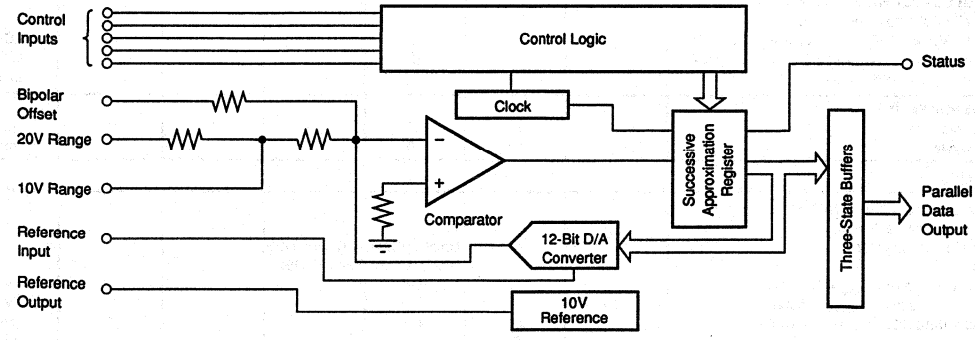
The ADC774 is a 12-bit successive approximation analog-to-digital converter, utilizing state-of-the-art CMOS and laser-trimmed bipolar die custom-designed for freedom from latch-up and for optimum AC performance. It is complete with a self-contained +10V reference, internal clock, digital interface for microprocessor control, and three-state outputs.

The reference circuit, containing a buried zener, is laser-trimmed for minimum temperature coefficient. The clock oscillator is current-controlled for excellent stability over temperature. Full-scale and offset errors may be externally trimmed to zero. Internal scaling resistors are provided for the selection of analog input signal ranges of 0V to +10V, 0V to +20V, ±5V, and ±10V.

The converter may be externally programmed to provide 8- or 12-bit resolution. The conversion time for 12 bits is factory set for 8.5µs maximum.

Output data are available in a parallel format from TTL-compatible three-state output buffers. Output data are coded in straight binary for unipolar input signals and bipolar offset binary for bipolar input signals.

The ADC774, available in both industrial and military temperature ranges, requires supply voltages of +5V and ±12V or ±15V. It is packaged in a 28-pin plastic DIP, or a hermetic side-brazed ceramic DIP.



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Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL

T_A = +25°C, V_{CC} = +12V or +15V, V_{EE} = –12V or –15V, V_{LOGIC} = +5V unless otherwise specified.

PARAMETER	ADC774J, ADC774SH MIN	ADC774J, ADC774SH TYP	ADC774J, ADC774SH MAX	ADC774K, ADC774TH MIN	ADC774K, ADC774TH TYP	ADC774K, ADC774TH MAX	UNITS
RESOLUTION			12			•	Bits
INPUTS							
ANALOG							
Voltage Ranges: Unipolar		0 to +10, 0 to +20			•		V
Bipolar		±5, ±10			•		V
Impedance: 0 to +10V, ±5V	3.75	5	6.25	•	•	•	kΩ
±10V, 0V to +20V	7.5	10	12.5	•	•	•	kΩ
DIGITAL (CE, $\overline{CS}$, R/$\overline{C}$, A_0, 12/$\overline{8}$)							
Over Temperature Range							
Voltages: Logic 1	+2		+5.5	•		•	V
Logic 0	–0.5		+0.8	•		•	V
Current	–5	0.1	+5	•	•	•	µA
Capacitance		5			•		pF
TRANSFER CHARACTERISTICS							
ACCURACY							
At +25°C							
Linearity Error			±1			±1/2	LSB
Unipolar Offset Error (Adjustable to Zero)			±2			•	LSB
Bipolar Offset Error (Adjustable to Zero)			±10			±4	LSB
Full-Scale Calibration Error[1] (Adjustable to Zero)			±0.25			•	% of FS[2]
No Missing Codes Resolution (Diff. Linearity)	11			12			Bits
Inherent Quantization Error		±1/2			•		LSB
T_{MIN} to T_{MAX}							
Linearity Error: J, K Grades			±1			±1/2	LSB
S, T Grades			±1			±3/4	LSB
Full-Scale Calibration Error							
Without Initial Adjustment [1] : J, K Grades			±0.47			±0.37	% of FS
S, T Grades			±0.75			±0.5	% of FS
Adjusted to Zero at +25°C: J, K Grades			±0.22			±0.12	% of FS
S, T Grades			±0.5			±0.25	% of FS
No Missing Codes Resolution (Diff. Linearity)	11			12			Bits
TEMPERATURE COEFFICIENTS (T_{MIN} to T_{MAX})[3]							
Unipolar Offset: J, K Grades			±10			±5	ppm/°C
S, T Grades			±5			±2.5	ppm/°C
Max Change: All Grades			±2			±1	LSB
Bipolar Offset: All Grades			±10			±5	ppm/°C
Max Change: J, K Grades			±2			±1	LSB
S, T Grades			±4			±2	LSB
Full-Scale Calibration: J, K Grades			±45			±25	ppm/°C
S, T Grades			±50			±25	ppm/°C
Max Change: J, K Grades			±9			±5	LSB
S, T Grades			±20			±10	LSB
POWER SUPPLY SENSITIVITY							
Change in Full-Scale Calibration							
+13.5V < V_{CC} <+16.5V or +11.4V < V_{CC} < +12.6V			±2			±1	LSB
–16.5V < V_{EE} <–13.5V or –12.6V < V_{EE} < –11.4V			±2			±1	LSB
+4.5V < V_{LOGIC} <+5.5V			±1/2			•	LSB
CONVERSION TIME [4,5]							
8-Bit Cycle		5	5.3		•	•	µs
12-Bit Cycle		7.5	8.5		•	•	µs
OUTPUTS							
DIGITAL (DB11 – DB0, STATUS)							
(Over Temperature Range)							
Output Codes: Unipolar			Unipolar Straight Binary (USB)				
Bipolar			Bipolar Offset Binary (BOB)				
Logic Levels: Logic 0 (I_{SINK} = 1.6mA)			+0.4			•	V
Logic 1 (I_{SOURCE} = 500µA)	+2.4			•			V
Leakage, Data Bits Only, High-Z State	–5	0.1	+5	•	•	•	µA
Capacitance		5			•		pF

SPECIFICATIONS (CONT)

ELECTRICAL

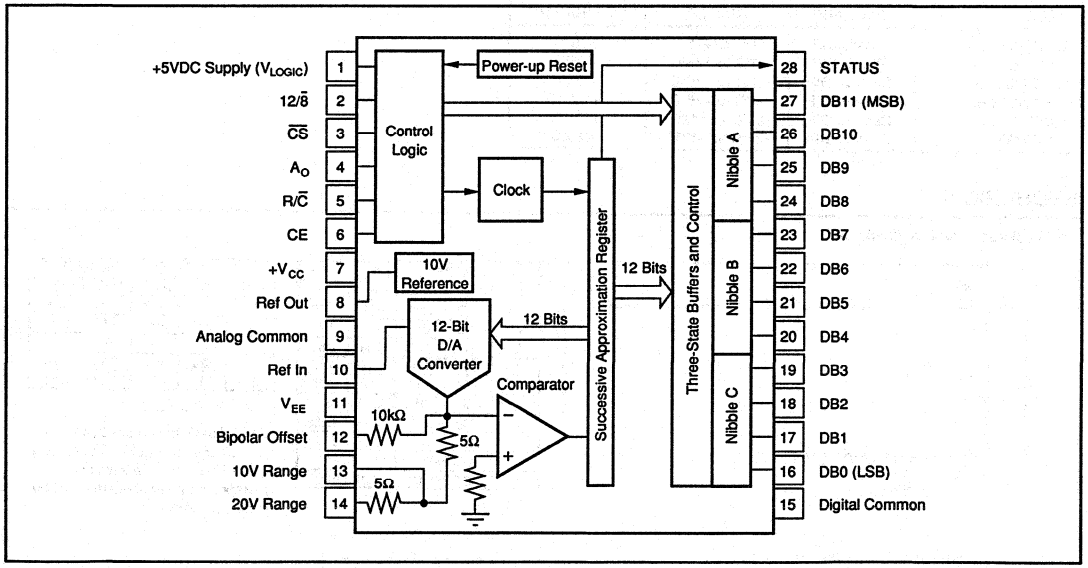
T_A = +25°C, V_{CC} = +12V or +15V, V_{EE} = –12V or –15V, V_{LOGIC} = +5V unless otherwise specified.

PARAMETER	ADC774J, ADC774SH			ADC774K, ADC774TH			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	
INTERNAL REFERENCE VOLRAGE							
Voltage	+9.9	+10	+10.1	*	*	*	V
Source Current Available for External Loads (6)	2.0			*			mA
POWER SUPPLY REQUIREMENTS							
Voltage: V_{CC}	+11.4		+16.5	*		*	V
V_{EE}	–11.4		–16.5	*		*	V
V_{LOGIC}	+4.5		+5.5	*		*	V
Current: I_{CC}		3.5	5		*	*	mA
I_{EE}		15	20		*	*	mA
I_{LOGIC}		9	15		*	*	mA
Power Dissipation (±15V Supplies)		325	450		*	*	mW
TEMPERATURE RANGE (Ambient: T_{MIN}, T_{MAX})							
Specifications: J, K Grades	0		+75	*		*	°C
S, T Grades	–55		+125	*		*	°C
Storage	–65		+150	*		*	°C

*Same specification as ADC774JH, JP, SH.

NOTES: (1) With fixed 50Ω resistor from Ref Out to Ref In. This parameter is also adjustable to zero at +25C. (2) FS in this specification table means Full Scale Range. That is, for a ±10V input range FS means 20V; for a 0V to +10V range, FS means 10V. The term Full Scale for these specification instead of Full-Scale Range is used to be consistent with other vendors' specifications tables. (3) Using internal reference. (4) See "Controlling the ADC774" section for detailed information concerning digital timing. (5) The Harris HI-774 uses a subranging/error correction technique that allows one to begin conversion before a preceding sample-hold or multiplexer has settled to ±1/2LSB. For 12-bit accurate conversions, the input transient to the ADC774 must settle to less than ±1/2LSB before conversion is started. The ADC774 is compatible with HI-774 in all other respects. (6) External loading must be constant during conversion. The reference output requires no buffer amplifier with either ±12V or ±15V power supplies.

PIN CONFIGURATION



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ABSOLUTE MAXIMUM RATINGS

V_{CC} to Digital Common ..... 0V to +16.5V
V_{EE} to Digital Common ..... 0V to –16.5V
V_{LOGIC} Digital Common ..... 0V to +7V
Analog Common to Digital Common ..... ±1V
Control Inputs (CE, $\overline{CS}$, A_0, 12/$\overline{8}$, R/$\overline{C}$)
to Digital Common ..... –0.5V to V_{LOGIC} +0.5V
Analog Inputs (Ref In, Bipolar Offset, $10V_{IN}$)
to Analog Common ..... ±16.5V
$20V_{IN}$ to Analog Common ..... ±24V
Ref Out ..... Indefinite Short to Common, Momentary Short to V_{CC}
Max Junction Temperature ..... +165°C
Power Dissipation 1000mW
Lead Temperature (soldering,10s) ..... +300°C
Thermal Resistance, θ_{JA} : Ceramic ..... 50°C/W
Plastic ..... 100°C/W

CAUTION: These devices are sensitive to electrostatic discharge. Appropriate I.C. handling procedures should be followed.

BURN-IN SCREENING

Burn-in screening is available for both plastic and ceramic package ADC774s. Burn-in duration is 160 hours at the temperature (or equivalent combination of time and temperature) indicated below:

Plastic "-BI" models: +85°C
Ceramic "-BI" models: +125°C

All units are 100% electrically tested after burn-in is completed. To order burn-in, add "-BI" to the base model number (e.g. ADC774KP-BI). See Ordering Information for pricing.

ORDERING INFORMATION

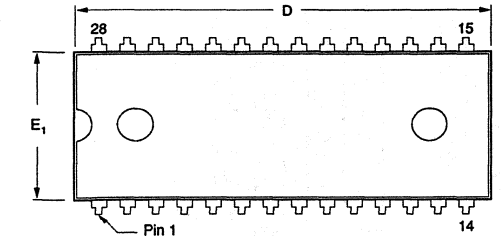
MODEL	PACKAGE	TEMPERATURE RANGE	LINEARITY ERROR MAX (T_{MIN} TO T_{MAX})
ADC774JP	Plastic DIP	0°C TO +75°C	±1LSB
ADC774KP	Plastic DIP	0°C to +75°C	±1/2LSB
ADC774JH	Ceramic DIP	0°C to +75°C	±1LSB
ADC774KH	Ceramic DIP	0°C to +75°C	±1/2LSB
ADC774SH	Ceramic DIP	–55°C to +125°C	±1LSB
ADC774TH	Ceramic DIP	–55°C to +125°C	±3/4LSB

BURN-IN SCREENING OPTION
See text for details.

MODEL	PACKAGE	TEMPERATURE RANGE	BURN-IN TEMP (160 HOURS)[1]
ADC774JP-BI	Plastic DIP	0°C to +75°C	+85°C
ADC774KP-BI	Plastic DIP	0°C to +75°C	+85°C
ADC774JH-BI	Ceramic DIP	0°C to +75°C	+125°C
ADC774KH-BI	Ceramic DIP	0°C to +75°C	+125°C
ADC774SH-BI	Ceramic DIP	–55°C to +125°C	+125°C
ADC774TH-BI	Ceramic DIP	–55°C to +125°C	+125°C

MECHANICAL

P Package — 28-Pin Plastic DIP

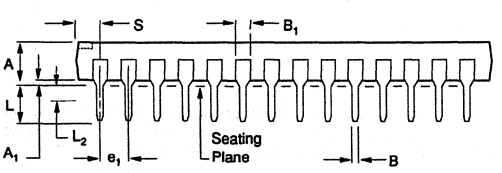


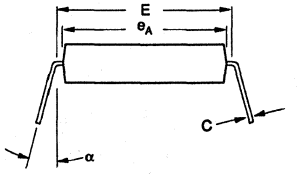
DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A[1]	.169	.200	4.29	5.08
A1[1]	.015	.070	0.38	1.78
B	.015	.020	0.38	0.51
B1	.015	.055	0.38	1.40
C	.008	.012	0.20	0.30
D[1]	1.380	1.455	35.05	36.96
E	.600	.625	15.24	15.88
E1[1]	.485	.550	12.32	13.97
e1	.100 BASIC		2.54 BASIC	
eA	.600 BASIC		15.24 BASIC	

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
L	.100	.200	2.54	5.08
L2	.000	.030	0.00	0.76
α	0°	15°	0°	15°
Q1	.020	.070	0.51	1.78
S1	.040	.080	1.02	2.03

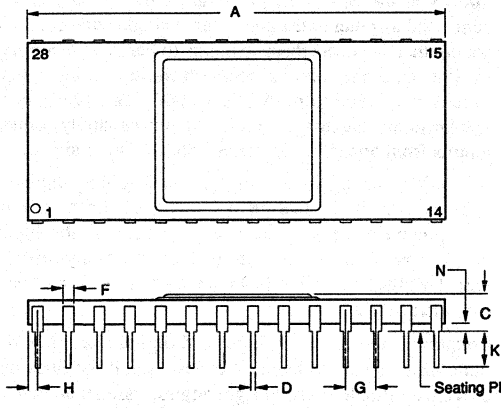
(1) Not JEDEC Standard

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.





H Package — 28-Pin Ceramic



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.386	1.414	35.20	35.92
C	.115	.175	2.92	4.45
D	.015	.021	0.38	0.53
F	.035	.060	0.89	1.52
G	.100 BASIC		2.54 BASIC	
H	.036	.064	0.91	1.63
J	.008	.012	0.20	0.30
K	.120	.240	3.05	6.10
L	.600 BASIC		15.24 BASIC	
M	—	10°	—	10°
N	.025	.060	0.64	1.52

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.

DISCUSSION OF SPECIFICATIONS

LINEARITY ERROR

Linearity error is defined as the deviation of actual code transition values from the ideal transition values. Ideal transition values lie on a line drawn through zero (or minus full scale for bipolar operation) and plus full scale. The zero value is located at an analog input value 1/2LSB before the first code transition (000_H to 001_H). The full-scale value is located at an analog value 3/2LSB beyond the last code transition (FFE_H to FFF_H) (see Figure 1).

Thus, for a converter connected for biopolar operation and with a full-scale range (or span) of 20V (±10V), the zero value of –10V is 2.44mV below the first code transition (000_H to 001_H at –9.99756V) and the plus full-scale value of +10V is 7.32mV above the last code transition (FFE_H to FFF_H at +9.99268) (see Table I).

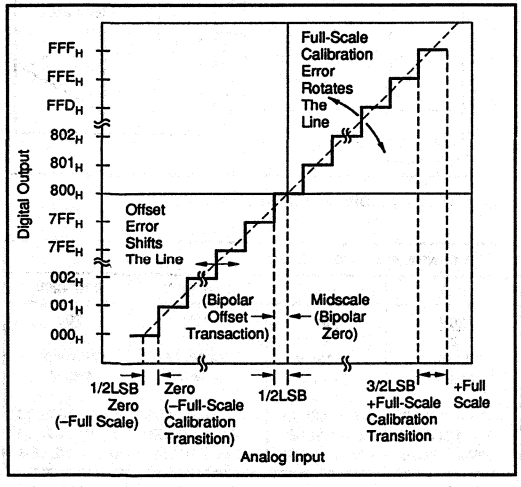


FIGURE 1. ADC774 Transfer Characteristics Terminology.

NO MISSING CODES (DIFFERENTIAL LINEARITY ERROR)

A specification which guarantees no missing codes requires that every code combination to appear in a monotonically-increasing sequence as the analog input is increased throughout the range. Thus, every input code width (quantum) must have a finite width. If an input quantum has a value of zero (a differential linearity error of –1LSB), a missing code will occur.

ADC774KP, KH and TH grades are guaranteed to have no missing codes to 12-bit resolution over their respective specification temperature ranges.

UNIPOLAR OFFSET ERROR

An ADC774 connected for unipolar operation has an analog input range of 0V to plus full scale. The first output code transition should occur at an analog input value 1/2LSB above 0V. Unipolar offset error is defined as the deviation of the acutal transition value from the ideal value. The unipolar offset temperature coefficient specifies the change of this transition value versus a change in ambient temperature.

BIPOLAR OFFSET ERROR

A/D converter specifications have historically defined bipolar offset as the first transition value above the minus full-scale value. The ADC774 specification, however, follows the terminology defined for the 574 converter several years ago. Thus, bipolar offset is located near the midscale value of 0V (bipolar zero) at the output code transition $7FF_H$ to 800_H.

Bipolar offset error for the ADC774 is defined as the deviation of the actual transition value from the ideal transition value located 1/2LSB below 0V. The bipolar offset temperature coefficient specifies the maximum change of the code transition value versus a change in ambient temperature.

FULL SCALE CALIBRATION ERROR

The last output code transition (FFE_H to FFF_H) occurs for an analog input value 3/2LSB below the nominal full-scale value. The full-scale calibration error is the deviation of the actual analog value at the last transition point from the ideal value. The full-scale calibration temperature coefficient specifies the maximum change of the code transition value versus a change in ambient temperature.

POWER SUPPLY SENSITIVITY

Electrical specifications for the ADC774 assume the application of the rated power supply voltages of +5V and ±12V or ±15V. The major effect of power supply voltage deviations from the rated values will be a small change in the full-scale calibration value. This change, of course, results in a proportional change in all code transition values (i.e., a gain error). The specification describes the maximum change in the full-scale calibration value from the initial value for a change in each power supply voltage.

TEMPERATURE COEFFICIENTS

The temperature coefficients for full-scale calibration, unipolar offset and bipolar offset specify the maximum change from the +25°C value to the value at T_{MIN} or T_{MAX}.

QUANTIZATION UNCERTAINTY

Analog-to-digital converters have an inherent quantization error of ±1/21LSB. This error is a fundamental property of the quantization process and cannot be eliminated.

CODE WIDTH (QUANTUM)

Code width, or quantum, is defined as the range of analog input values for which a given output code will occur. The ideal code width is 1LSB.

INSTALLATION

LAYOUT PRECAUTIONS

Analog (pin 9) and digital (pin 15) commons are not connected together internally in the ADC774, but should be connected together as close to the unit as possible and to an analog common ground plane beneath the converter on the component side of the board. In addition, a wide conductor pattern should run directly from pin 9 to the analog supply common, and a separate wide conductor pattern from pin 15 to the digital supply common. Analog common (pin 9) typically carries +8mA.

If the single-point system common cannot be established directly at the converter, pin 9 and pin 15 should still be connected together at the converter; a single wide conductor pattern then connects these two pins to the system common. In either case, the common return of the analog input signal should be referred to pin 9 of the ADC. This prevents any voltage drops that might occur in the power supply common returns from appearing in series with the input signal.

If the 20V analog input range is used (either bipolar or unipolar), the 10V range input (pin 13) should be shielded with ground plane to reduce noise pickup. If the bipolar offset input (pin 12) is not used to externally trim the unipolar offset as shown in Figure 2, connect it to Analog Common (pin 9).

Coupling between analog input and digital lines should be minimized by careful layout. For instance, if the lines must cross, they should do so at right angles. Parallel analog and digital lines should be separated from each other by a pattern connected to common.

If external full scale and offset potentiometers are used, the potentiometers and associated resistors should be located as close to the ADC774 as possible. If no trim adjustments are used, the fixed resistors should likewise be as close as possible.

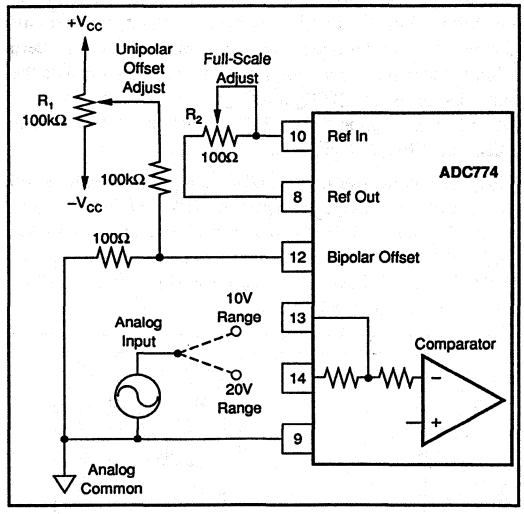


FIGURE 2. Unipolar Configuration.

BINARY (BIN) OUTPUT	INPUT VOLTAGE RANGE AND LSB VALUES				
Analog Input Voltage Range	Defined as:	±10V	±5V	0 to +10V	0 to +20V
One Least Significant Bit (LSB)	$\frac{FSR}{2^n}$	$\frac{20V}{2^n}$	$\frac{10V}{2^n}$	$\frac{10V}{2^n}$	$\frac{20V}{2^n}$
	n = 8	78.13mV	39.06mV	39.06mV	78.13mV
	n =12	4.88mV	2.44mV	2.44mV	4.88mV
Output Transition Values					
FFE_H to FFF_H	+Full-Scale Calibration	+10V – 3/2LSB	+5 – 3/2LSB	+10V – 3/2LSB	+20V – 3/2LSB
$7FF_H$ to 800_H	Midscale Calibration (Bipolar Offset)	0 – 1/2LSB	0 – 1/2LSB	+5V – 1/2LSB	+10V – 1/2LSB
000_H to 001_H	Zero Calibration (– Full-Scale Calibration)	–10V + 1/2LSB	–5V + 1/2LSB	0 to + 1/2LSB	0 to + 1/2 LSB

TABLE I. Input Voltages, Transition Values, and LSB Values.

POWER SUPPLY DECOUPLING

Logic and analog power supplies should be bypassed with 10µF tantalum-type capacitors located close to the converter to obtain noise-free operation. Noise on the power supply lines can degrade the converter's performance. Noise and spikes from a switching power supply are especially troublesome.

ANALOG SIGNAL SOURCE IMPEDANCE

The signal source supplying the analog input signal to the ADC774 will be driving into a nominal DC input impedance of either 5kΩ or 10kΩ. However, the output impedance of the driving source should be very low, such as the output impedance provided by a wideband, fast-settling operational amplifier. Transients in A/D input current are caused by the changes in output current of the internal D/A converter as it tests the various bits. The output voltage of the driving source must remain constant while furnishing these fast current changes. If the application requires a sample/hold, select a sample/hold with sufficient bandwidth to preserve the accuracy or use a separate wideband buffer amplifier to lower the output impedance.

RANGE CONNECTIONS

The ADC774 offers four standard input ranges: 0V to +10V, 0V to +20V, ±5V, and ±10V. If a 10V input range is required, the analog input signal should be connected to pin 13 of the converter. A signal requiring a 20V range is connected to pin 14. In either case the other pin of the two is left unconnected. Full-scale and offset adjustments are described below.

To operate the converter with a 10.24V (2.5mV LSB) or 20.48V (5mV LSB) input range, insert a 120Ω 1% metal-film resistor in series with pin 13 for the 10.24V range, or a 240Ω 1% metal-film resistor in series with pin 14 for the 20.48V range. Offset adjustments are still perfomed as described below. A fixed metal-film resistor can be used because the input impedance of the ADC774 is trimmed to typically less than ±2% of the nominal value.

CALIBRATION

OPTIONAL EXTERNAL FULL-SCALE AND OFFSET ADJUSTMENTS

Offset and full-scale errors may be trimmed to zero using external offset and full-scale trim potentiometers connected to the ADC774 as shown in Figures 2 and 3 for unipolar and bipolar operation.

CALIBRATION PROCEDURE—UNIPOLAR RANGES

If adjustment of unipolar offset and full scale is not required, replace R_2 with a 50Ω, 1% metal film resistor and connect pin 12 to pin 9, omitting the adjustment network.

If adjustment is required, connect the converter as shown in Figure 2. Sweep the input through the end-point transition voltage (0V + 1/2LSB; +1.22mV for the 10V range, +2.44mV for the 20V range) that causes the output code to be DB0 ON (high). Adjust potentiometer R_1 until DB0 is alternately toggling ON and OFF with all other bits OFF. Then adjust full scale by applying an input voltage of nominal full-scale value minus 3/2LSB, the value which should cause all bits to be ON. This value is +9.9963V for the 10V range and +19.9927V for the 20V range. Adjust potentiometer R_2 until bits DB1-DB11 are ON and DB0 is toggling ON and OFF.

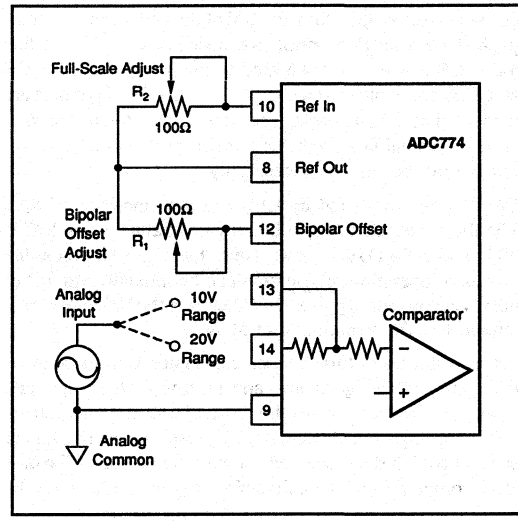


FIGURE 3. Bipolar Configuration.

CALIBRATION PROCEDURE—BIPOLAR RANGES

If external adjustments of full-scale and bipolar offset are not required, the potentiometers may be replaced by 50Ω, 1% metal film resistors.

If adjustments are required, connect the converter as shown in Figure 3. The calibration procedure is similar to that described above for unipolar operation, except that the offset adjustment is performed with an input voltage which is 1/2LSB above the minus full-scale value (–4.9988V for the ±5V range, –9.9976V for the ±10V range). Adjust R_1 for DB0 to toggle ON and OFF with all other bits OFF. To adjust full-scale, apply a DC input signal which is 3/2LSB below the nominal plus full-scale value (+4.9963V for ±5V range, +9.9927V for ±10V range) and adjust R_2 for DB0 to toggle ON and OFF with all other bits ON.

CONTROLLING THE ADC774

The Burr-Brown ADC774 can be easily interfaced to most microprocessor systems and other digital systems. The microprocessor may take full control of each conversion, or the converter may operate in a stand-alone mode, controlled only by the R/$\overline{C}$ input. Full control consists of selecting an 8- or 12-bit conversion cycle, initiating the conversion, and reading the output data when ready—choosing either 12 bits

all at once, or 8 bits followed by 4 bits in a left-justified format. The five control inputs (12/$\overline{8}$, $\overline{CS}$, A_0, R/$\overline{C}$, and CE) are all TTL/CMOS-compatible. The functions of the control inputs are described in Table II. The control function truth table is listed in Table III.

Read footnote 5 to the Electrical Specifications table if using ADC774 to replace the HI-774.

STAND-ALONE OPERATION

For stand-alone operation, control of the converter is accomplished by a single control line connected to R/$\overline{C}$. In this mode $\overline{CS}$ and A_0 are connected to digital common and CE and 12/$\overline{8}$ are connected to V_{LOGIC} (+5V). The output data are presented as 12-bit words. The stand-alone mode is used in systems containing dedicated input ports which do not require full bus interface capability.

Conversion is initiated by a high-to-low transition of R/$\overline{C}$. The three-state data output buffers are enabled when R/$\overline{C}$ is high and STATUS is low. Thus, there are two possible modes of operation; conversion can be initiated with either positive or negative pulses. In either case the R/$\overline{C}$ pulse must remain low for a minimum of 50ns.

Figure 4 illustrates timing when conversion is initiated by an R/$\overline{C}$ pulse which goes low and returns to the high state during the conversion. In this case, the three-state outputs go to the high-impedance state in response to the falling edge of R/$\overline{C}$ and are enabled for external access of the data after completion of the conversion. Figure 5 illustrates the timing when conversion is initiated by a positive R/$\overline{C}$ pulse. In this mode the output data from the previous conversion is enabled during the positive portion of R/$\overline{C}$. A new conversion is started on the falling edge of R/$\overline{C}$, and the three-state outputs return to the high-impedance state until the next occurrence of a high R/$\overline{C}$ pulse. Timing specifications for stand-alone operation are listed in Table IV.

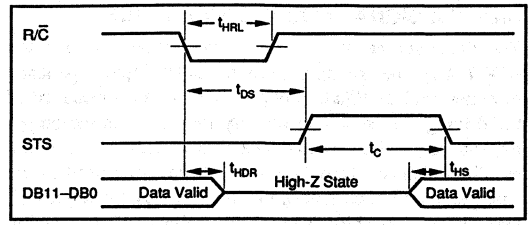


FIGURE 4. R/$\overline{C}$ Pulse Low—Outputs Enabled After Conversion.

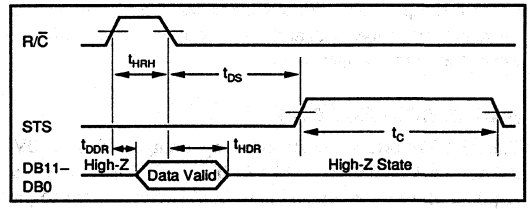


FIGURE 5. R/$\overline{C}$ Pulse High—Outputs Enabled Only While R/$\overline{C}$ Is High.

PIN DESIGNATION	DEFINITION	FUNCTION
CE (Pin 6)	Chip Enable (active high)	Must be high ("1") to either initiate a conversion or read output data. 0-1 edge may be used to initiate a conversion.
$\overline{CS}$ (Pin 3)	Chip Select (active low)	Must be low ("0") to either initiate a conversion or read output data. 1-0 edge may be used to initiate a conversion.
R/$\overline{C}$ (Pin 5)	Read/Convert ("1" = read) ("0" = convert)	Must be low ("0") to initiate either 8- or 12-bit conversions. 1-0 edge may be used to initiate a conversion. Must be high ("1") to read output data. 0-1 edge may be used to initiate a read operation.
A_0 (Pin 4)	Byte Address Short Cycle	In the start-convert mode, A_0 selects 8-bit (A_0 = "1") or 12-bit (A_0 = "0") conversion mode. When reading output data in two 8-bit bytes, A_0 = "0" accesses 8 MSBs (high byte) and A_0 = "1" accesses 4 LSBs and trailing "0s" (low byte).
12/$\overline{8}$ (Pin 2)	Data Mode Select ("1" = 12 bits) ("0" = 8 bits)	When reading output data, 12/$\overline{8}$ = "1" enables all 12 output bits simultaneously. 12/$\overline{8}$ = "0" will enable the MSBs or LSBs as determined by the A_0 line.

TABLE II. ADC774 Control Line Functions.

CE	$\overline{CS}$	R/$\overline{C}$	12/$\overline{8}$	A_0	OPERATION
0	X	X	X	X	None
X	1	X	X	X	None
↑	0	0	X	0	Initiate 12-bit conversion
↑	0	0	X	1	Initiate 8-bit conversion
1	↓	0	X	0	Initiate 12-bit conversion
1	↓	0	X	1	Initiate 8-bit conversion
1	0	↓	X	0	Initiate 12-bit conversion
1	0	↓	X	1	Initiate 8-bit conversion
1	0	1	1	X	Enable 12-bit output
1	0	1	0	0	Enable 8 MSBs only
1	0	1	0	1	Enable 4 LSBs plus 4 trailing zeros

TABLE III. Control Input Truth Table.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
t_{HRL}	Low R/$\overline{C}$ Pulse Width	50			ns
t_{DS}	STS Delay from R/$\overline{C}$			200	ns
t_{HDR}	Data Valid After R/$\overline{C}$ Low	25			ns
t_{HS}	STS Delay After Data Valid		150	375	ns
t_{HRH}	High R/$\overline{C}$ Pulse Width	150			ns
t_{DDR}	Data Access Time			150	ns

TABLE IV. Stand-Alone Mode Timing.

FULLY CONTROLLED OPERATION

Conversion Length

Conversion length (8-bit or 12-bit) is determined by the state of the A_0 input, which is latched upon receipt of a conversion start transition (described below). If A_0 is latched high, the conversion continues for 8 bits. The full 12-bit conversion will occur if A_0 is low. If all 12 bits are read following an 8-bit conversion, the 3 LSBs (DB0–DB2) will be low (logic 0) and DB3 will be high (logic 1). A_0 is latched because it is also involved in enabling the output buffers. No other control inputs are latched.

CONVERSION START

The converter is commanded to initiate a conversion by a transition occuring on any of three logic inputs (CE, $\overline{CS}$, and R/$\overline{C}$) as shown in Table III. Conversion is initiated by the last of the three to reach the required state and thus all three may be dynamically controlled. If necessary, all three may change state simultaneously, and the nominal delay time is the same regardless of which input actually starts conversion. If it is desired that a particular input establish the actual start of conversion, the other two should be stable a minimum of 50ns prior to the transition of that input. Timing relationships for start of conversion timing are illustrated in Figure 6. The specifications for timing are contained in Table V.

The STATUS output indicates the current state of the converter by being in a high state only during conversion.

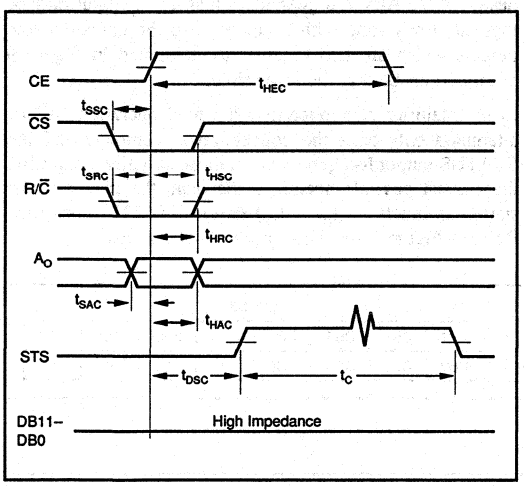


FIGURE 6. Conversion Cycle Timing.

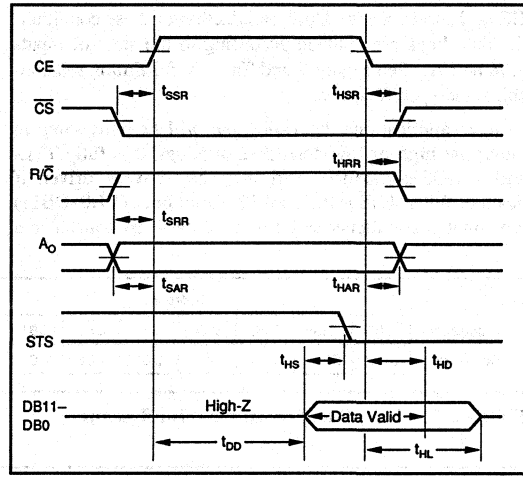


FIGURE 7. Read Cycle Timing.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
t_{DSC}	STS Delay from CE		60	200	ns
t_{HEC}	CE Pulse Width	50	30		ns
t_{SSC}	$\overline{CS}$ to CE Setup time	50	20		ns
t_{HSC}	$\overline{CS}$ low during CE high	50	20		ns
t_{SRC}	R/$\overline{C}$ to CE setup	50	0		ns
t_{HRC}	R/$\overline{C}$ low during CE high	50	20		ns
t_{SAC}	A_0 to CE setup	0			ns
t_{HAC}	A_0 valid during CE high	50	20		ns
t_C	Conversion time				
	12-bit cycle at 25°C		7.5	8.5	µs
	0 to +75°C			9.0	µs
	–55°C to +125°C			9.5	µs
	8-bit cycle at 25°C		5	5.3	µs
	0 to +75°C			5.6	µs
	–55° to +125°C			6	µs
Read Mode					
t_{DD}	Access time from CE		75	150	ns
t_{HD}	Data valid after CE low	25	35		ns
t_{HL}	Output float delay		100	150	ns
t_{SSR}	$\overline{CS}$ to CE setup	50	0		ns
t_{SAR}	R/$\overline{C}$ to CE setup	0			ns
t_{HSR}	$\overline{CS}$-valid after CE low	0			ns
t_{HRR}	R/C high after CE low	0			ns
t_{HAR}	A_0 valid after CE low	50			ns
t_{HS}	STS delay after data valid		150	375	ns

TABLE V. Timing Specifications.

During this time the three-state output buffers remain in a high-impedance state, and therefore data cannot be read during conversion. During this period additional transitions of the three digital inputs which control conversion will be ignored, so that conversion cannot be prematurely terminated or restarted. However, if A_0 changes state after the beginning of conversion, any additional start conversion transition will latch the new state of A_0, possibly resulting in an incorrect conversion length (8 bits vs 12 bits) for that conversion.

READING OUTPUT DATA

After conversion is initiated, the output data buffers remain in a high-impedance state until the following four logic conditions are simultaneously met: R/$\overline{C}$ high, STATUS low, CE high, and $\overline{CS}$ low. Upon satisfaction of these conditions the data lines are enabled according to the state of inputs 12/$\overline{8}$ and A_0. See Figure 7 and Table V for timing relationships and specifications.

In most applications the 12/$\overline{8}$ input will be hard-wired in either the high or low condition, although it is fully TTL- and CMOS-compatible and may be actively driven if desired. When 12/$\overline{8}$ is high, all 12 output lines (DB0–DB11) are enabled simultaneously for full data word transfer to a 12-bit or 16-bit bus. In this situation the A_0 state is ignored.

When 12/$\overline{8}$ is low, the data is presented in the form of two 8-bit bytes, with selection of the byte of interest accomplished by the state of A_0 during the read cycle. Connection of the ADC774 to an 8-bit bus for transfer of left-justified data is illustrated in Figure 9. The A_0 input is usually driven by the least significant bit of the address bus, allowing storage of the output data word in two consecutive memory locations.

When A_0 is low, the byte addressed contains the 8MSBs. When A_0 is high, the byte addressed contains the 4LSBs from the conversion followed by four logic zeros which have been forced by the control logic. The left-justified formats of the two 8-bit bytes are shown in Figure 8. The design of the ADC774 guarantees that the A_0 input may be toggled at any time with no damage to the converter; the outputs which are tied together as illustrated in Figure 9 cannot be enabled at the same time.

In the majority of applications the read operation will be attempted only after the conversion is complete and the STATUS output has gone low. In those situations requiring the earliest possible access to the data, the read may be started as much as (t_{DD} + t_{HS}) before STATUS goes low. Refer to Figure 7 for these timing relationships.

	Word 1								Word 2							
Processor	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Converter	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	0	0	0	0

FIGURE 8. 12-Bit Data Format for 8-Bit Systems.

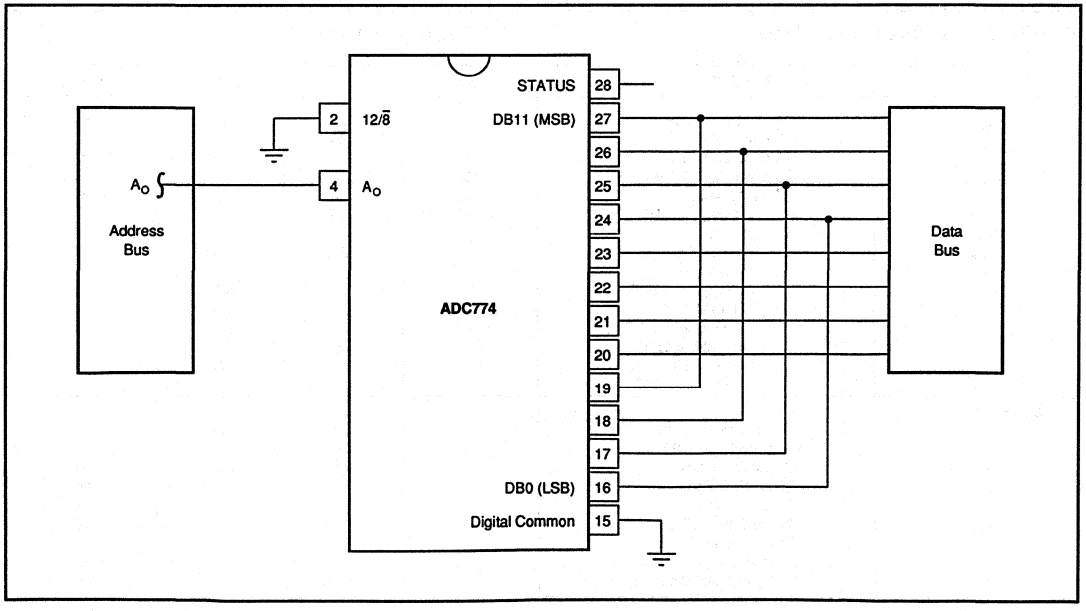


FIGURE 9. Connection to an 8-Bit Bus.

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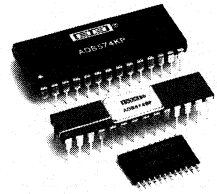


ADS574

Microprocessor-Compatible Sampling CMOS ANALOG-to-DIGITAL CONVERTER

FEATURES

- COMPATIBLE WITH ADC574
- COMPLETE SAMPLING A/D WITH REFERENCE, CLOCK AND MICROPROCESSOR INTERFACE
- FAST ACQUISITION AND CONVERSION: 25µs max
- ELIMINATES EXTERNAL SAMPLE/HOLD IN MOST APPLICATIONS
- GUARANTEED AC AND DC PERFORMANCE
- SINGLE +5V SUPPLY OPERATION
- LOW POWER: 100mW max
- PACKAGE OPTIONS: 0.6" and 0.3" DIPs, SOIC

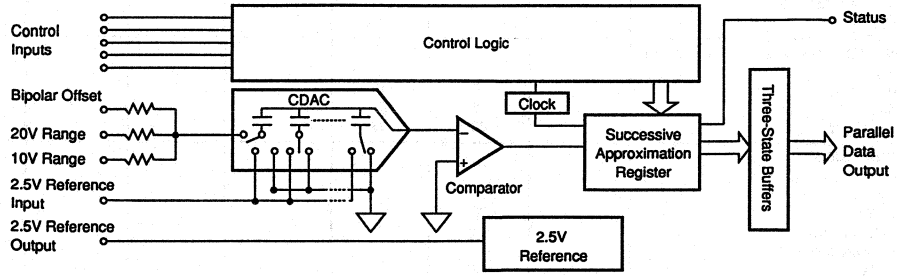
DESCRIPTION

The ADS574 is a 12-bit successive approximation analog-to-digital converter using an innovative capacitor array (CDAC) implemented in low-power CMOS technology. This is a drop-in replacement for ADC574 models in most applications, with internal sampling, much lower power consumption, and capability to operate from a single +5V supply.

The ADS574 is complete with internal clock, microprocessor interface, three-state outputs, and internal scaling resistors for input ranges of 0V to +10V, 0V to +20V, ±5V, or ±10V. The maximum throughput time for 12-bit conversions is 25µs over the full operating temperature range, including both acquisition and conversion.

Complete user control over the internal sampling function facilitates elimination of external sample/hold amplifiers in most existing designs.

The ADS574 is available in both commercial (0°C to +70°C) and military (–55°C to +125°C) ranges, and requires +5V, with –12V or –15V optional, depending on usage. No +15V supply is required. Available packages include 0.3" or 0.6" wide 28-pin plastic or hermetic ceramic DIPs, and 28-pin SOICs. The ADS574 is also available in die form.



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Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL

$T_A = T_{MIN}$ to T_{MAX}, V_{DD} = +5V, V_{EE} = –15V to +5V, sampling frequency of 40kHz, f_{IN} = 10kHz; unless otherwise specified.

PARAMETER	ADS574JE/JH/JP/JU/SF/SH			ADS574KE/KH/KP/KU/TF/TH			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	
RESOLUTION			12			•	Bits
INPUTS							
ANALOG							
Voltage Ranges: Unipolar			0 to +10, 0 to +20				V
Bipolar			±5, ±10				V
Impedance: 0 to +10V, ±5V	15	21		•	•		kΩ
±10V, 0V to +20V	60	84		•	•		kΩ
DIGITAL (CE, $\overline{CS}$, R/$\overline{C}$, A_0, 12/$\overline{8}$)							
Voltages: Logic 1	+2.0		+5.5	•		•	V
Logic 0	–0.5		+0.8	•		•	V
Current	–5	0.1	+5	•	•	•	µA
Capacitance		5			•		pF
TRANSFER CHARACTERISTICS							
DC ACCURACY							
At +25°C							
Linearity Error			±1			±1/2	LSB
Unipolar Offset Error (adjustable to zero)			±2			•	LSB
Bipolar Offset Error (adjustable to zero)			±10			±4	LSB
Full-Scale Calibration Error [1]							
(adjustable to zero)			±0.25			•	% of FS [2]
No Missing Codes Resolution (Diff. Linearity)	12			12			Bits
Inherent Quantization Error		±1/2			•		LSB
T_{MIN} to T_{MAX}							
Linearity Error: J, K Grades			±1			±1/2	LSB
S, T Grades			±1			±3/4	LSB
Full-Scale Calibration Error							
Without Initial Adjustment [1]: J, K Grades			±0.47			±0.37	% of FS
S, T Grades			±0.75			±0.5	% of FS
Adjusted to Zero at +25°C: J, K Grades			±0.22			±0.12	% of FS
S, T Grades			±0.5			±0.25	% of FS
No Missing Codes Resolution (Diff. Linearity)	12			12			Bits
AC ACCURACY [3]							
Spurious Free Dynamic Range	73	78		76	•		dB
Total Harmonic Distortion		–77	–72		•	–75	dB
Signal-to-Noise Ratio	69	72		71	•		dB
Signal-to-(Noise + Distortion) Ratio	68	71		70	•		dB
Intermodulation Distortion		–75			•		
(F_{IN1} = 10kHz, F_{IN2} = 11.5kHz)							
TEMPERATURE COEFFICIENTS [4]							
Unipolar Offset			±5			±2.5	ppm/°C
Max Change			±2			±1	LSB
Bipolar Offset			±10			±5	ppm/°C
Max Change: J, K Grades			±2			±1	LSB
S, T Grades			±4			±2	LSB
Full-Scale Calibration			±45			±25	ppm/°C
Max Change: J, K Grades			±9			±5	LSB
S, T Grades			±20			±10	LSB
POWER SUPPLY SENSITIVITY							
Change in Full-Scale Calibration[5]							
+4.75V < V_{DD} < +5.25V			±1/2			•	LSB
CONVERSION TIME (Including Acquisition Time)							
$t_{AQ} + t_C$ at 25°C:							
8-Bit Cycle		16	18		•	•	µs
12-Bit Cycle		22	25		•	•	µs
12-Bit Cycle, T_{MIN} to T_{MAX}		22	25		•	•	µs
SAMPLING DYNAMICS							
Sampling Rate	40			•			kHz
Aperture Delay, t_{AP}							
With V_{EE} = +5V		20			•		ns
With V_{EE} = 0V to –15V		4.0			•		µs
Aperture Uncertainty (Jitter)							
With V_{EE} = +5V		300			•		ps, rms
With V_{EE} = 0V to –15V		30			•		ns,rms

SPECIFICATIONS (CONT)

ELECTRICAL

$T_A = T_{MIN}$ to T_{MAX}, V_{DD} = +5V, V_{EE} = –15V to +5V, sampling frequency of 40kHz, f_{IN} = 10kHz; unless otherwise specified.

PARAMETER	ADS574JE/JH/JP/JU/SF/SH MIN	ADS574JE/JH/JP/JU/SF/SH TYP	ADS574JE/JH/JP/JU/SF/SH MAX	ADS574KE/KH/KP/KU/TF/TH MIN	ADS574KE/KH/KP/KU/TF/TH TYP	ADS574KE/KH/KP/KU/TF/TH MAX	UNITS
OUTPUTS							
DIGITAL (DB_{11} - DB_0, STATUS)							
Output Codes: Unipolar			Unipolar Straight Binary (USB)				
Bipolar			Bipolar Offset Binary (BOB)				
Logic Levels: Logic 0 (I_{SINK} = 1.6mA)			+0.4			*	V
Logic 1 (I_{SOURCE} = 500µA)	+2.4			*			V
Leakage, Data Bits Only, High-Z State	–5	0.1	+5	*	*	*	µA
Capacitance		5			*		pF
INTERNAL REFERENCE VOLTAGE							
Voltage	+2.4	+2.5	+2.6	*	*	*	V
Source Current Available for External Loads	0.5			*			mA
POWER SUPPLY REQUIREMENTS							
Voltage: V_{EE} [6]	–16.5		V_{DD}	*		*	V
V_{DD}	+4.5		+5.5	*		*	V
Current: I_{EE} [6] (V_{EE} = –15V)		–1			*		mA
I_{DD}		+13	+20		*	*	mA
Power Dissipation (T_{MIN} to T_{MAX})							
(V_{EE} = 0V to +5V)		65	100		*	*	mW
TEMPERATURE RANGE							
Specification: J, K Grades	0		+70	*		*	°C
S, T Grades	–55		+125	*		*	°C
Operating: J, K Grades	–40		+85	*		*	°C
S, T Grades	–55		+125	*		*	°C
Storage	–65		+150	*		*	°C

*Same specification as ADS574JE/JH/JP/JU/SF/SH.

NOTES: (1) With fixed 50Ω resistor from REF OUT to REF IN. This parameter is also adjustable to zero at +25°C. (2) FS in this specification table means Full Scale Range. That is, for a ±10V input range, FS means 20V; for a 0 to +10V range, FS means 10V. (3) Based on using V_{EE} = +5V, which starts a conversion immediately upon a convert command. Using V_{EE} = 0V to –15V makes the ADS574/ADS774 emulate standard ADC574 operation. In this mode, the internal sample/hold acquires the input signal after receiving the convert command, and does not assume that the input level has been stable before the convert command arrives. (4) Using internal reference. (5) This is worst case change in accuracy from accuracy with a +5V supply. (6) V_{EE} is optional, and is only used to set the mode for the internal sample/hold. When V_{EE} = –15V, I_{EE} = –1mA typ; when V_{EE} = 0V, I_{EE} = ±5µA typ; when V_{EE} = +5V, I_{EE} = +167µA typ.

ABSOLUTE MAXIMUM RATINGS

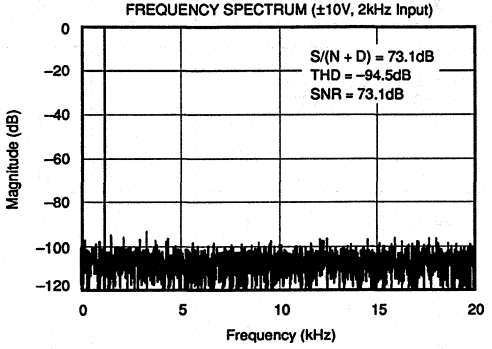
V_{EE} to Digital Common	+V_{DD} to –16.5V
V_{DD} to Digital Common	0V to +7V
Analog Common to Digital Common	±1V
Control Inputs (CE, $\overline{CS}$, A_0, 12/$\overline{8}$, R/$\overline{C}$) to Digital Common	–0.5V to V_{DD} +0.5V
Analog Inputs (Ref In, Bipolar Offset, $10V_{IN}$) to Analog Common	±16.5V
$20V_{IN}$ to Analog Common	±24V
Ref Out	Indefinite Short to Common, Momentary Short to V_{DD}
Max Junction Temperature	+165°C
Power Dissipation	1000mW
Lead Temperature (soldering,10s)	+300°C
Thermal Resistance, θ_{JA} : Ceramic DIPs	50°C/W
Plastic DIPs	100°C/W
SOIC	100°C/W

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

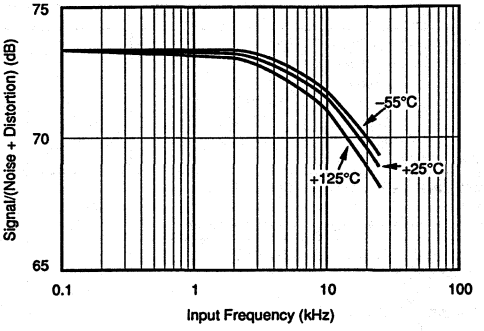
TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_{DD} = V_{EE} = +5V; Bipolar ±10V Input Range; sampling frequency of 40kHz; unless otherwise specified. All plots use 4096 point FFTs.

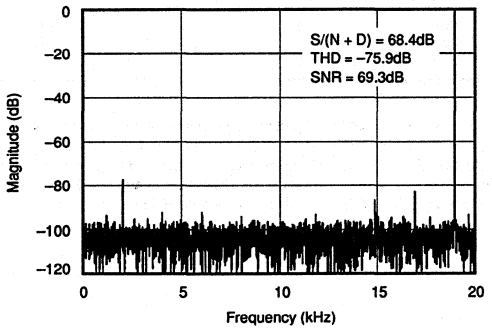
FREQUENCY SPECTRUM (±10V, 2kHz Input)



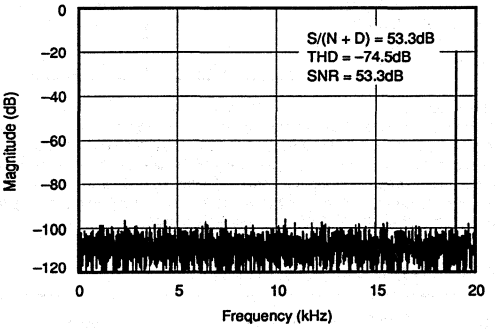
SIGNAL/(NOISE + DISTORTION) vs
INPUT FREQUENCY AND AMBIENT TEMPERATURE



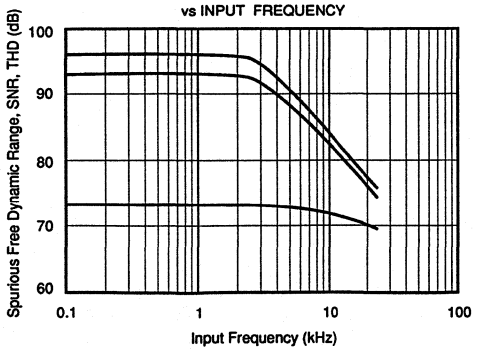
FREQUENCY SPECTRUM (±10V, 19kHz Input)



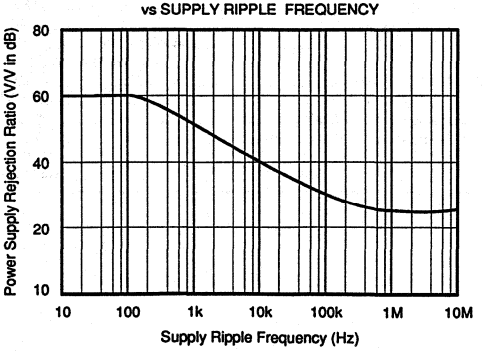
FREQUENCY SPECTRUM (±1V, 19kHz Input)



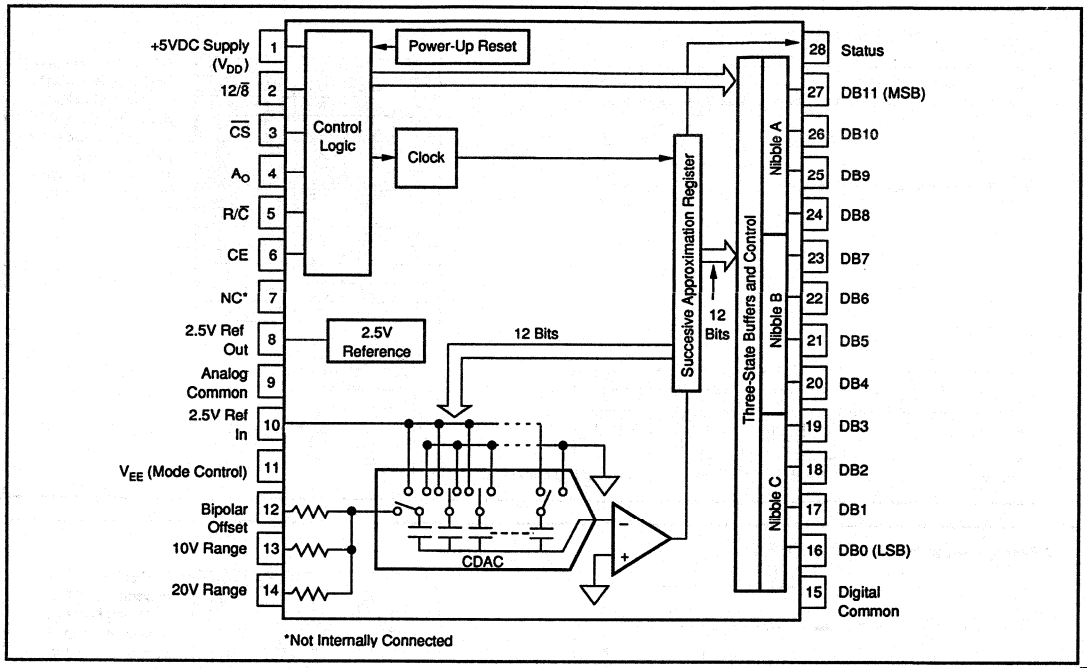
SPURIOUS FREE DYNAMIC RANGE, SNR AND THD
vs INPUT FREQUENCY



POWER SUPPLY REJECTION
vs SUPPLY RIPPLE FREQUENCY



CONNECTION DIAGRAM



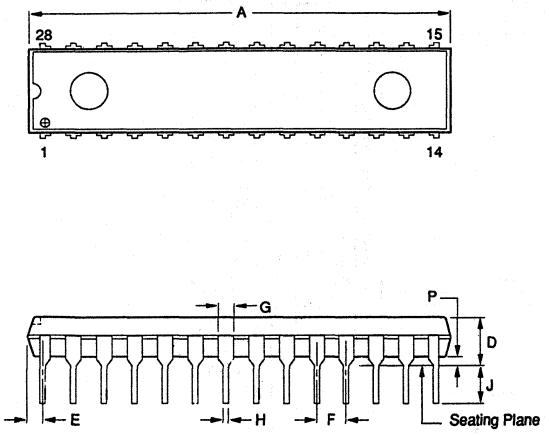
ORDERING INFORMATION

MODEL	PACKAGE	SINAD(1)	TEMPERATURE RANGE	LINEARITY ERROR
ADS574JE	0.3" Plastic DIP	68	0°C to +70°C	±1LSB
ADS574KE	0.3" Plastic DIP	70	0°C to +70°C	±1/2LSB
ADS574JP	0.6" Plastic DIP	68	0°C to +70°C	±1LSB
ADS574KP	0.6" Plastic DIP	70	0°C to +70°C	±1/2LSB
ADS574JU	SOIC	68	0°C to +70°C	±1LSB
ADS574KU	SOIC	70	0°C to +70°C	±1/2LSB
ADS574SF	0.3" Ceramic DIP	68	–55°C to +125°C	±1LSB
ADS574TF	0.3" Ceramic DIP	70	–55°C to +125°C	±1/2LSB
ADS574SH	0.6" Ceramic DIP	68	–55°C to +125°C	±1LSB
ADS574TH	0.6" Ceramic DIP	70	–55°C to +125°C	±1/2LSB
ADS574JH	0.6" Ceramic DIP	68	0°C to +70°C	±1LSB
ADS574KH	0.6" Ceramic DIP	70	0°C to +70°C	±1/2LSB

NOTE: (1) SINAD is Signal to (Noise and Distortion) expressed in dB.

MECHANICAL

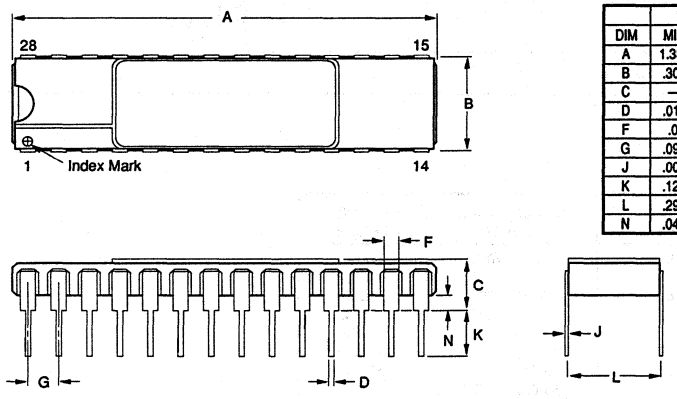
E Package — 0.3" Wide 28-Pin Plastic DIP



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.255	1.355	31.88	34.42
B	.270	.290	6.86	7.37
D	.150	.170	3.81	4.32
E	.010	.080	0.25	2.03
F	.100 BASIC		2.54 BASIC	
G	.045	.055	1.14	1.40
H	.016	.020	0.41	0.51
J	.125	N/A	3.18	N/A
K	.300 BASIC		7.62 BASIC	
M	0°	15°	0°	15°
N	.008	.015	0.20	0.38
P	.020	.040	0.51	1.02

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.

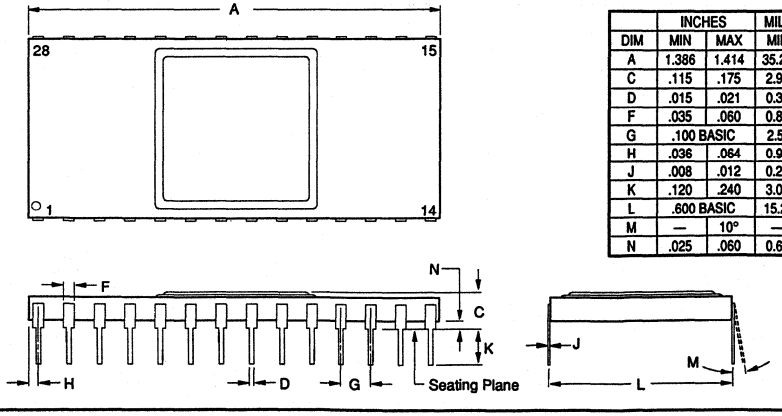
F Package — 0.3" Wide 28-Pin Hermetic DIP



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.388	1.412	35.26	35.86
B	.300	.320	7.62	8.13
C	—	.160	—	4.06
D	.016	.020	0.41	0.51
F	.050 BASIC		1.27 BASIC	
G	.095	.105	2.41	2.67
J	.009	.012	0.23	0.30
K	.125	.180	3.18	4.57
L	.290	.310	7.37	7.87
N	.040	.060	1.02	1.52

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.

H Package — 0.6" Wide 28-Pin Hermetic DIP

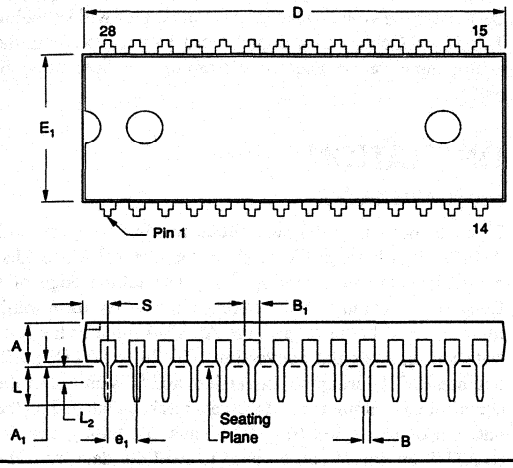


	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.386	1.414	35.20	35.92
C	.115	.175	2.92	4.45
D	.015	.021	0.38	0.53
F	.035	.060	0.89	1.52
G	.100 BASIC		2.54 BASIC	
H	.036	.064	0.91	1.63
J	.008	.012	0.20	0.30
K	.120	.240	3.05	6.10
L	.600 BASIC		15.24 BASIC	
M	—	10°	—	10°
N	.025	.060	0.64	1.52

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.

MECHANICAL

P Package — 0.6" Wide 28-Pin Plastic DIP



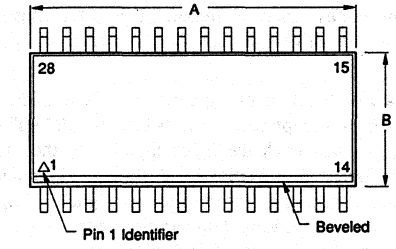
DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A(1)	.169	.200	4.29	5.08
A1(1)	.015	.070	0.38	1.78
B	.015	.020	0.38	0.51
B1	.015	.055	0.38	1.40
C	.008	.012	0.20	0.30
D(1)	1.380	1.455	35.05	36.96
E	.600	.625	15.24	15.88
E1(1)	.485	.550	12.32	13.97
e1	.100 BASIC		2.54 BASIC	
eA	.600 BASIC		15.24 BASIC	

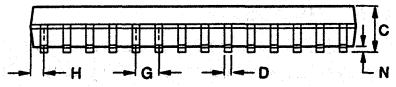
DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
L	.100	.200	2.54	5.08
L2	.000	.030	0.00	0.76
α	0°	15°	0°	15°
S(1)	.040	.080	1.02	2.03

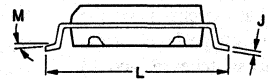
(1) Not JEDEC Standard

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.

U Package — 28-Pin Plastic SOIC







DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.700	.716	17.78	18.19
B	.286	.302	7.26	7.67
C	.093	.109	2.36	2.77
D	.016 BASIC		0.41 BASIC	
G	.050 BASIC		1.27 BASIC	
H	.022	.038	0.56	0.97
J	.008	.012	0.20	0.30
L	.398	.414	10.11	10.52
M	5° TYP		5° TYP	
N	.000	.012	0.00	0.30

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.

THEORY OF OPERATION

In the ADS574, the advantages of advanced CMOS technology—high logic density, stable capacitors, precision analog switches—and Burr-Brown's state of the art laser trimming techniques are combined to produce a fast, low power analog-to-digital converter with internal sample/hold.

The charge-redistribution successive-approximation circuitry converts analog input voltages into digital words.

A simple example of a charge-redistribution A/D converter with only 3 bits is shown in Figure 1.

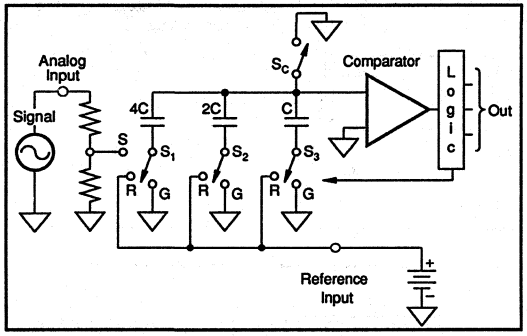


FIGURE 1. 3-Bit Charge Redistribution A/D.

INPUT SCALING

Precision laser-trimmed scaling resistors at the input divide standard input ranges (0V to +10V, 0V to +20V, ±5V or ±10V) into levels compatible with the CMOS characteristics of the internal capacitor array.

SAMPLING

While sampling, the capacitor array switch for the MSB capacitor (S_1) is in position "S", so that the charge on the MSB capacitor is proportional to the voltage level of the analog input signal. The remaining array switches (S_2 and S_3) are set to position "G". Switch S_c is closed, setting the comparator input offset to zero.

CONVERSION

When a conversion command is received, switch S_1 is opened to trap a charge on the MSB capacitor proportional to the analog input level at the time of the sampling command, and switch S_c is opened to float the comparator input. The charge trapped in the capacitor array can now be moved between the three capacitors in the array by connecting switches S_1, S_2, and S_3 to positions "R" (to connect to the reference) or "G" (to connect to GND), thus changing the voltage generated at the comparator input.

During the first approximation, the MSB capacitor is connected through switch S_1 to the reference, while switches S_2 and S_3 are connected to GND. Depending on whether the comparator output is HIGH or LOW, the logic will then latch S_1 in position "R" or "G". Similarly, the second approximation is made by connecting S_2 to the reference and S_3 to GND, and latching S_2 according to the output of the comparator. After three successive approximation steps have been made the voltage level at the comparator will be within 1/2LSB of GND, and a digital word which represents the analog input can be determined from the positions of S_1, S_2 and S_3.

OPERATION

BASIC OPERATION

Figure 2 shows the minimum circuit required to operate the ADS574 in a basic ±10V range in the Control Mode (discussed in detail in a later section.) The falling edge of a Convert Command (a pulse taking pin 5 LOW for a minimum of 25ns) both switches the ADS574 input to the hold state and initiates the conversion. Pin 28 (STATUS) will output a HIGH during the conversion, and falls only after the conversion is completed and the data has been latched on the data output pins (pins 16 to 27.) Thus, the falling edge of STATUS on pin 28 can be used to read the data from the conversion. Also, during conversion, the STATUS signal puts the data output pins in a High-Z state and inhibits the input lines. This means that pulses on pin 5 are ignored, so that new conversions cannot be initiated during the conversion, either as a result of spurious signals or to short-cycle the ADS574.

The ADS574 will begin acquiring a new sample as soon as the conversion is completed, even before the STATUS output falls, and will track the input signal until the next conversion is started. The ADS574 is designed to complete a conversion and accurately acquire a new signal in 25µs max over the full operating temperature range, so that conversions can take place at a full 40kHz.

CONTROLLING THE ADS574

The Burr-Brown ADS574 can be easily interfaced to most microprocessor systems and other digital systems. The microprocessor may take full control of each conversion, or the converter may operate in a stand-alone mode, controlled only by the R/$\overline{C}$ input. Full control consists of selecting an 8- or 12-bit conversion cycle, initiating the conversion, and reading the output data when ready—choosing either 12 bits all at once, or the 8 MSB bits followed by the 4 LSB bits in a left-justified format. The five control inputs (12/$\overline{8}$, $\overline{CS}$, A_0, R/$\overline{C}$, and CE) are all TTL/CMOS-compatible. The functions of the control inputs are described in Table II. The control function truth table is shown in Table III.

STAND-ALONE OPERATION

For stand-alone operation, control of the converter is accomplished by a single control line connected to R/$\overline{C}$. In this mode $\overline{CS}$ and A_0 are connected to digital common and CE and 12/$\overline{8}$ are connected to +5V. The output data are presented as 12-bit words. The stand-alone mode is used in systems containing dedicated input ports which do not require full bus interface capability.

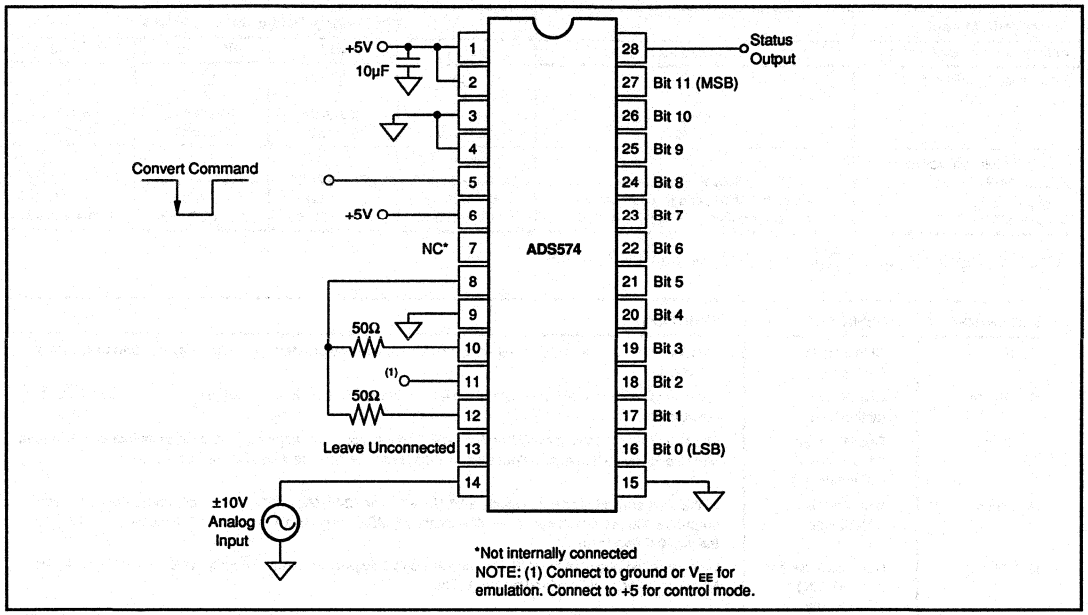


FIGURE 2. Basic ±10V Operation.

Conversion is initiated by a HIGH-to-LOW transition of R/$\overline{C}$. The three-state data output buffers are enabled when R/$\overline{C}$ is HIGH and STATUS is LOW. Thus, there are two possible modes of operation; data can be read with either a positive pulse on R/$\overline{C}$, or a negative pulse on STATUS. In either case the R/$\overline{C}$ pulse must remain LOW for a minimum of 25ns.

Figure 3 illustrates timing with an R/$\overline{C}$ pulse which goes LOW and returns HIGH during the conversion. In this case, the three-state outputs go to the high-impedance state in response to the falling edge of R/$\overline{C}$ and are enabled for external access of the data after completion of the conversion.

Figure 4 illustrates the timing when a positive R/$\overline{C}$ pulse is used. In this mode the output data from the previous conversion is enabled during the time R/$\overline{C}$ is HIGH. A new conversion is started on the falling edge of R/$\overline{C}$, and the three-state outputs return to the high-impedance state until the next occurrence of a HIGH R/$\overline{C}$ pulse. Timing specifications for stand-alone operation are listed in Table IV.

FULLY CONTROLLED OPERATION

Conversion Length

Conversion length (8-bit or 12-bit) is determined by the state of the A_0 input, which is latched upon receipt of a conversion start transition (described below). If A_0 is latched HIGH, the conversion continues for 8 bits. The full 12-bit conversion will occur if A_0 is LOW. If all 12 bits are read following an 8-bit conversion, the 4LSBs (DB0-DB3) will be LOW (logic 0). A_0 is latched because it is also involved in enabling the output buffers. No other control inputs are latched.

CONVERSION START

The converter initiates a conversion based on a transition occurring on any of three logic inputs (CE, $\overline{CS}$, and R/$\overline{C}$) as shown in Table III. Conversion is initiated by the last of the three to reach the required state and thus all three may be dynamically controlled. If necessary, all three may change state simultaneously, and the nominal delay time is the same regardless of which input actually starts the conversion. If it is desired that a particular input establish the actual start of conversion, the other two should be stable a minimum of 50ns prior to the transition of the critical input. Timing relationships for start of conversion timing are illustrated in Figure 5. The specifications for timing are contained in Table V.

The STATUS output indicates the current state of the converter by being in a high state only during conversion. During this time the three state output buffers remain in a high-impedance state, and therefore data cannot be read during conversion. During this period additional transitions of the three digital inputs which control conversion will be ignored, so that conversion cannot be prematurely terminated or restarted. However, if A_0 changes state after the beginning of conversion, any additional start conversion transition will latch the new state of A_0, possibly resulting in an incorrect conversion length (8 bits vs 12 bits) for that conversion.

Binary (BIN) Output		Input Voltage Range and LSB Values			
Analog Input Voltage Range	Defined As:	±10V	+5V	0V to +10V	0V to +20V
One Least Significant Bit (LSB)	$\frac{FSR}{2^n}$	$\frac{20V}{2^n}$	$\frac{10V}{2^n}$	$\frac{10V}{2^n}$	$\frac{20V}{2^n}$
	n = 8	78.13mV	39.06mV	39.06mV	78.13mV
	n = 12	4.88mV	2.44mV	2.44mV	4.88mV
Output Transition Values					
FFE_H to FFF_H	+ Full-Scale Calibration	+10V – 3/2LSB	+5V – 3/2LSB	+10V – 3/2LSB	+10V – 3/2LSB
$7FFF_H$ to 800_H	Midscale Calibration (Bipolar Offset)	0 – 1/2LSB	0 – 1/2LSB	+5V – 1/2LSB	±10V – 1/2LSB
000_H to 001_H	Zero Calibration (– Full-Scale Calibration)	–10V + 1/2LSB	–5V + 1/2LSB	0 to +1/2LSB	0 to +1/2LSB

TABLE I. Input Voltages, Transition Values, and LSB Values.

DESIGNATION	DEFINITION	FUNCTION
CE (Pin 6)	Chip Enable (active high)	Must be HIGH ("1") to either initiate a conversion or read output data. 0-1 edge may be used to initiate a conversion.
$\overline{CS}$ (Pin 3)	Chip Select (active low)	Must be LOW ("0") to either initiate a conversion or read output data. 1-0 edge may be used to initiate a conversion.
R/$\overline{C}$ (Pin 5)	Read/Convert ("1" = read) ("0" = convert)	Must be LOW ("0") to initiate either 8- or 12-bit conversions. 1-0 edge may be used to initiate a conversion. Must be HIGH ("1") to read output data. 0-1 edge may be used to initiate a read operation.
A_0 (Pin 4)	Byte Address Short Cycle	In the start-convert mode, A_0 selects 8-bit (A_0 = "1") or 12-bit (A_0 = "0") conversion mode. When reading output data in two 8-bit bytes, A_0 = "0" accesses 8 MSBs (high byte) and A_0 = "1" accesses 4 LSBs and trailing "0s" (low byte).
12/$\overline{8}$ (Pin 2)	Data Mode Select ("1" = 12 bits) ("0" = 8 bits)	When reading output data, 12/$\overline{8}$ = "1" enables all 12 output bits simultaneously. 12/$\overline{8}$ = "0" will enable the MSBs or LSBs as determined by the A_0 line.

TABLE II. Control Line Functions.

CE	$\overline{CS}$	R/$\overline{C}$	12/$\overline{8}$	A_0	OPERATION
0	X	X	X	X	None
X	1	X	X	X	None
↑	0	0	X	0	Initiate 12-bit conversion
↑	0	0	X	1	Initiate 8-bit conversion
1	↓	0	X	0	Initiate 12-bit conversion
1	↓	0	X	1	Initiate 8-bit conversion
1	0	↓	X	0	Initiate 12-bit conversion
1	0	↓	X	1	Initiate 8-bit conversion
1	0	1	1	X	Enable 12-bit output
1	0	1	0	0	Enable 8 MSBs only
1	0	1	0	1	Enable 4 LSBs plus 4 trailing zeroes

TABLE III. Control Input Truth Table.

READING OUTPUT DATA

After conversion is initiated, the output data buffers remain in a high-impedance state until the following four logic conditions are simultaneously met: R/$\overline{C}$ HIGH, STATUS LOW, CE HIGH, and $\overline{CS}$ LOW. Upon satisfaction of these conditions the data lines are enabled according to the state of inputs 12/$\overline{8}$ and A_0. See Figure 6 and Table V for timing relationships and specifications.

In most applications the 12/$\overline{8}$ input will be hard-wired in either the high or low condition, although it is fully TTL and CMOS-compatible and may be actively driven if desired. When 12/$\overline{8}$ is HIGH, all 12 output lines (DB0-DB11) are enabled simultaneously for full data word transfer to a 12-bit or 16-bit bus. In this situation the A_0 state is ignored when reading the data.

When 12/$\overline{8}$ is LOW, the data is presented in the form of two 8-bit bytes, with selection of the byte of interest accomplished by the state of A_0 during the read cycle. When A_0 is LOW, the byte addressed contains the 8MSBs. When A_0 is HIGH, the byte addressed contains the 4LSBs from the conversion followed by four logic zeros which have been forced by the control logic. The left-justified formats of the two 8-bit bytes are shown in Figure 7. Connection of the ADS574 to an 8-bit bus for transfer of the data is illustrated in Figure 8. The design of the ADS574 guarantees that the A_0 input may be toggled at any time with no damage to the converter; the outputs which are tied together in Figure 8 cannot be enabled at the same time. The A_0 input is usually driven by the least significant bit of the address bus, allowing storage of the output data word in two consecutive memory locations.

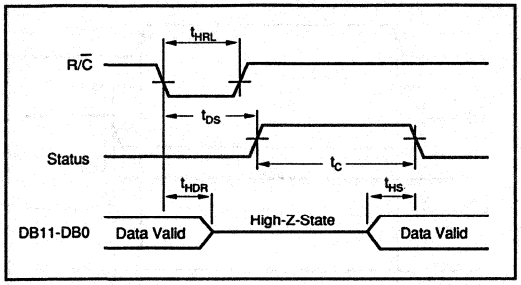


FIGURE 3. R/C Pulse Low—Outputs Enabled After Conversion.

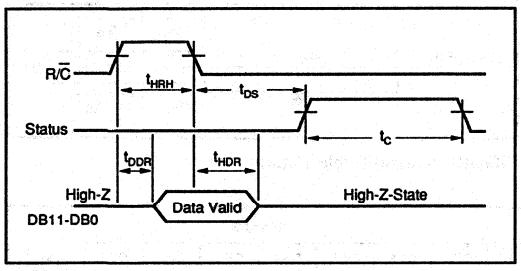


FIGURE 4. R/C Pulse High — Outputs Enabled Only While R/C Is High.

S/H CONTROL MODE AND ADC574 EMULATION MODE

The basic difference between these two modes is the assumptions about the state of the input signal both before and during the conversion. The differences are shown in Figure 9 and Table VI. In the Control Mode it is assumed that during the required 4µs acquisition time the signal is not slewing faster than the slew rate of the ADS574. No assumption is made about the input level after the convert command arrives, since the input signal is sampled and conversion begins immediately after the convert command.

This means that a convert command can also be used to switch an input multiplexer or change gains on a programmable gain amplifier, allowing the input signal to settle before the next acquisition at the end of the conversion. Because aperture jitter is minimized by the internal sample/hold circuit, a high input frequency can be converted without an external sample/hold.

In the Emulation Mode, no assumption is made about the input signal prior to the convert command. A delay time is introduced between the convert command and the start of conversion to allow the ADS574 enough time to acquire the input signal before converting. The delay increases the effective aperture time from 0.02µs to 4µs, but allows the ADS574 to replace the ADC574 in any circuit. Any slewing of the analog input prior to the convert command in existing

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
t_{HRL}	Low R/C Pulse Width	25			ns
t_{DS}	STS Delay from R/C			200	ns
t_{HDR}	Data Valid After R/C Low	25			ns
t_{HRH}	High R/C Pulse Width	100			ns
t_{DDR}	Data Access Time			150	ns

TABLE IV. Stand-Alone Mode Timing. ($T_A = T_{MIN}$ to T_{MAX}).

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
Convert Mode					
t_{DSC}	STS delay from CE		60	200	ns
t_{HEC}	CE Pulse width	50	30		ns
t_{SSC}	CS to CE setup	50	20		ns
t_{HSC}	CS low during CE high	50	20		ns
t_{SRC}	R/C to CE setup	50	0		ns
t_{HRC}	R/C low during CE high	50	20		ns
t_{SAC}	A_0 to CE setup	0			ns
t_{HAC}	A_0 valid during CE high	50	20		ns
Read Mode					
t_{DD}	Access time from CE		75	150	ns
t_{HD}	Data valid after CE low	25	35		ns
t_{HL}	Output float delay		100	150	ns
t_{SSR}	CS to CE setup	50	0		ns
t_{SRR}	R/C to CE setup	0			ns
t_{SAR}	A_0 to CE setup	50	25		ns
t_{HSR}	CS valid after CE low	0			ns
t_{HRR}	R/C high after CE low	0			ns
t_{HAR}	A_0 valid after CE low	50			ns
t_{HS}	STC delay after data valid	300	400	1000	

TABLE V. Timing Specifications, Fully Controlled Operation. ($T_A = T_{MIN}$ to T_{MAX}).

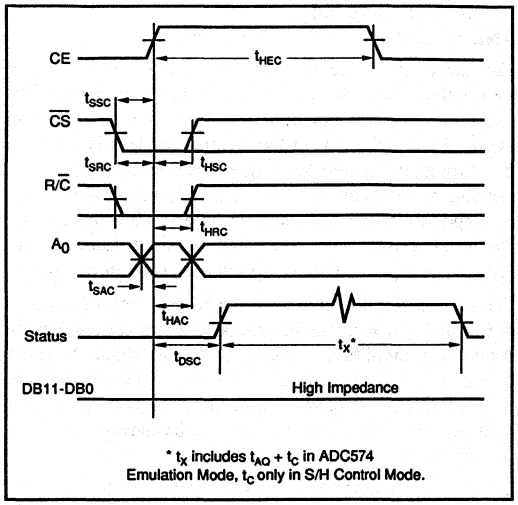


FIGURE 5. Conversion Cycle Timing.

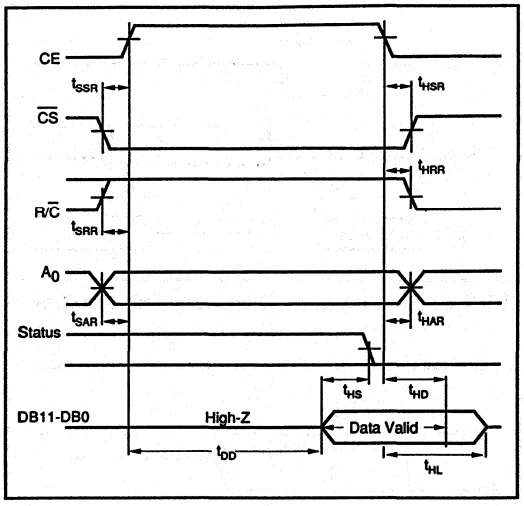


FIGURE 6. Read Cycle Timing.

	Word 1								Word 2							
Processor	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Converter	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	0	0	0	0

FIGURE 7. 12-Bit Data Format for 8-Bit Systems.

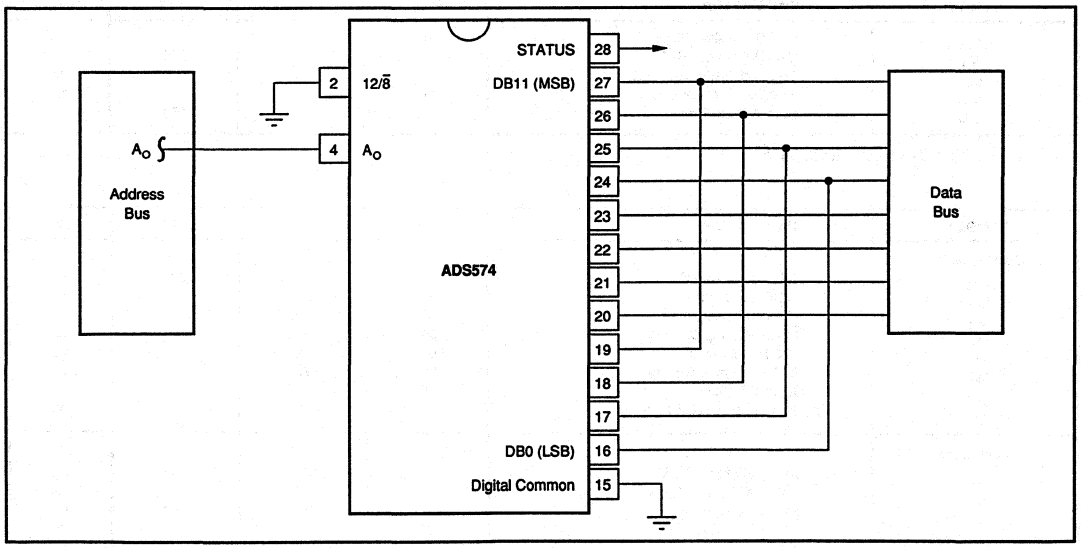


FIGURE 8. Connection to an 8-Bit Bus.

systems (due to multiplexers, sample/holds, etc. in front of the converter) does not affect the accuracy of the ADS574 conversion in the Emulation Mode.

In both modes, as soon as the conversion is completed the internal sample/hold circuit immediately begins slewing to track the input signal.

Basically, the Control Mode is provided to allow full use of the internal sample/hold, eliminating the need for an external sample/hold in most applications. As compared with systems using separate sample/hold and A/D, the ADS574 in the Control Mode also eliminates the need for one of the control signals, usually the convert command. The command that puts the internal sample/hold in the hold state also initiates a conversion, reducing timing constraints in many systems.

The Emulation Mode allows the ADS574 to be dropped into almost all existing ADC574 sockets without changes to any other existing system hardware or software. The input to the ADS574 in the Emulation Mode does not need to be stable before a convert command is received, so that multiplexers, programmable gain amplifiers, etc., can be slewing quickly any time before a convert command is given as long as the analog input to the ADS574 is stable after the convert command is received, as it needs to be in existing ADC574 systems for accurate operation. In fact, even in the Emulation Mode, system throughput can be speeded up, since the input to the ADS574 can start slewing before the end of a conversion (after the acquisition time), which is not possible with existing ADC574s.

INSTALLATION

LAYOUT PRECAUTIONS

Analog (pin 9) and digital (pin 15) commons are not connected together internally in the ADS574, but should be connected together as close to the unit as possible and to an analog common ground plane beneath the converter on the component side of the board. In addition, a wide conductor pattern should run directly from pin 9 to the analog supply common, and a separate wide conductor pattern from pin 15 to the digital supply common.

If the single-point system common cannot be established directly at the converter, pin 9 and pin 15 should still be connected together at the converter. A single wide conductor pattern then connects these two pins to the system common. In either case, the common return of the analog input signal should be referenced to pin 9 of the ADC. This prevents any voltage drops that might occur in the power supply common returns from appearing in series with the input signal.

SYMBOL	PARAMETER	S/H CONTROL MODE (Pin 11 Connected to +5V) MIN	TYP	MAX	ADC574 EMULATION MODE (Pin 11 Connected to 0V to –15V) MIN	TYP	MAX	UNITS
$t_{AQ} + t_C$	Throughput Time:							
	12-bit Conversions		22	25		22	25	µs
	8-bit Conversions		16	18		16	18	µs
t_C	Conversion Time:							
	12-bit Conversions		18			18		µs
	8-bit Conversions		12			12		µs
t_{AQ}	Acquisition Time		4			4		µs
t_A	Aperture Delay		20			4000		ns
t_J	Aperture Uncertainty		0.3			30		ns

TABLE VI. Conversion Timing, T_{MIN} to T_{MAX}.

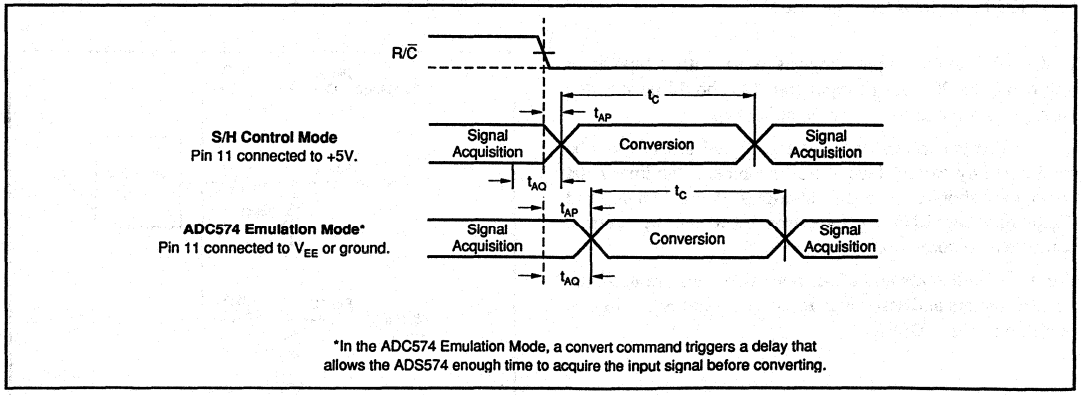


FIGURE 9. Signal Acquisition and Conversion Timing.

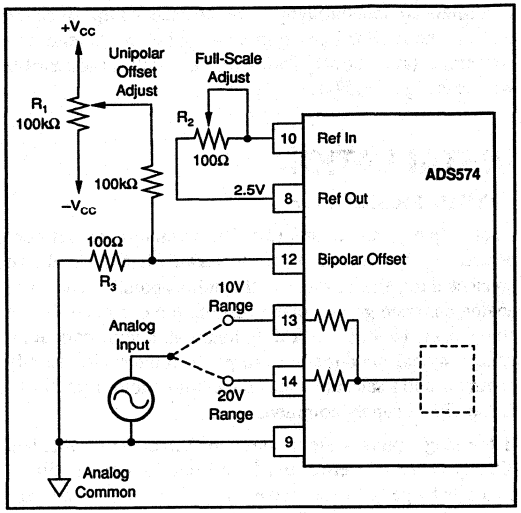


FIGURE 10. Unipolar Configuration.

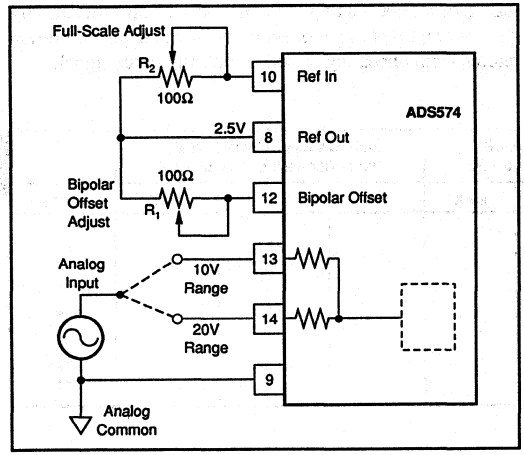


FIGURE 11. Bipolar Configuration.

If the 10V analog input range is used (either bipolar or unipolar), the 20V range input (pin 14) should be shielded with ground plane to reduce noise pickup.

Coupling between analog input and digital lines should be minimized by careful layout. For instance, if the lines must cross, they should do so at right angles. Parallel analog and digital lines should be separated from each other by a pattern connected to common.

If external full scale and offset potentiometers are used, the potentiometers and associated resistors should be as close as possible to the ADS574.

POWER SUPPLY DECOUPLING

On the ADS574, +5V (to Pin 1) is the only power supply required for correct operation. Pin 7 is not connected internally, so there is no problem in existing ADC574 sockets where this is connected to +15V. Pin 11 (V_{EE}) is only used as a logic input to select modes of control over the sampling function as described above. When used in an existing ADC574 socket, the –15V on pin 11 selects the ADC574 Emulation Mode. Since pin 11 is used as a logic input, it is immune to typical supply variations.

The +5V supply should be bypassed with a 10µF tantalum capacitor located close to the converter to promote noise-free operations, as shown in Figure 2. Noise on the power supply lines can degrade the converter's performance. Noise and spikes from a switching power supply are especially troublesome.

RANGE CONNECTIONS

The ADS574 offers four standard input ranges: 0V to +10V, 0V to +20V, ±5V, or ±10V. Figures 10 and 11 show the necessary connections for each of these ranges, along with the optional gain and offset trim circuits. If a 10V input range is required, the analog input signal should be connected to pin 13 of the converter. A signal requiring a 20V range is connected to pin 14. In either case the other pin of the two is left unconnected. Pin 12 (Bipolar Offset) is connected either to Pin 9 (Analog Common) for unipolar operation, or to Pin 8 (2.5V Ref Out), or the external reference, for bipolar operation. Full-scale and offset adjustments are described below.

The input impedance of the ADS574 is typically 84kΩ in the 20V ranges and 21kΩ in the 10V ranges. This is significantly higher than that of traditional ADC574 architectures, reducing the load on the input source in most applications.

INPUT STRUCTURE

Figure 12 shows the resistor divider input structure of the ADS574. Since the input is driving a capacitor in the CDAC during acquisition, the input is looking into a high imped-

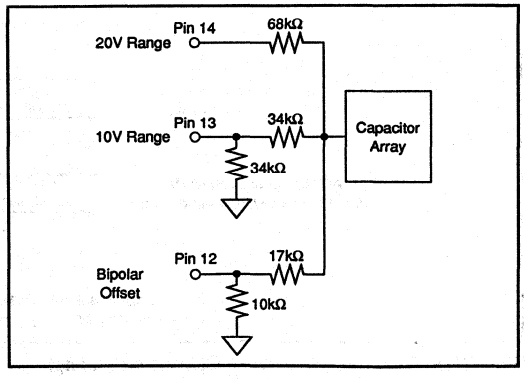


FIGURE 12. ADS574 Input Structure.

ance node as compared with traditional ADC574 architectures, where the resistor divider network looks into a comparator input node at virtual ground.

To understand how this circuit works, it is necessary to know that the input range on the internal sampling capacitor is from 0V to +3.33V, and the analog input to the ADS574 must be converted to this range. Unipolar 20V range can be used as an example of how the divider network functions. In 20V operation, the analog input goes into pin 14. Pin 13 is left unconnected and pin 12 is connected, through 50Ω, to analog common. From Figure 12, it is clear that the input to the capacitor array will be the analog input voltage on pin 14 divided by the resistor network (68kΩ + 68kΩ || 17kΩ). A 20V input at pin 14 is divided to 3.33V at the capacitor array, while a 0V input at pin 14 gives 0V at the capacitor array.

The main effect of the 10kΩ internal resistor on pin 12 is to provide offset adjust response the same as that of traditional ADC574 architectures without needing to change the external trimpot values.

SINGLE SUPPLY OPERATION

The ADS574 is designed to operate from a single +5V supply, and handle all of the unipolar and bipolar input ranges, in either the Control Mode or the Emulation Mode as described above. Pin 7 is not connected internally. This is where +12V or +15V is supplied on traditional ADC574s. Pin 11, the –12V or –15V supply input on traditional ADC574s, is used only as a logic input on the ADS574. There is a resistor divider internally on pin 11 to reduce that input to a correct logic level within the ADS574, and this resistor will add 10mW to 15mW to the power consumptionof the ADS574 when –15V is supplied to pin 11. To minimize power consumption in a system, pin 11 can be simply grounded (for Emulation Mode) or tied to +5V (for Control Mode.)

There are no other modifications required for the ADS574 to function with a single +5V supply.

CALIBRATION

OPTIONAL EXTERNAL FULL-SCALE AND OFFSET ADJUSTMENTS

Offset and full-scale errors may be trimmed to zero using external offset and full-scale trim potentiometers connected to the ADS574 as shown in Figures 10 and 11 for unipolar and bipolar operation.

CALIBRATION PROCEDURE— UNIPOLAR RANGES

If external adjustments of full-scale and offset are not required, replace R_2 in Figure 10 with a 50Ω, 1% metal film resistor, omitting the other adjustment components.

If adjustment is required, connect the converter as shown in Figure 10. Sweep the input through the end-point transition voltage (0V + 1/2LSB; +1.22mV for the 10V range, +2.44mV for the 20V range) that causes the output code to be DB0 ON (HIGH). Adjust potentiometer R_1 until DB0 is alternately toggling ON and OFF with all other bits OFF. Then adjust full scale by applying an input voltage of nominal full-scale minus 3/2LSB, the value which should cause all bits to be ON. This value is +9.9963V for the 10V range and +19.9927V for the 20V range. Adjust potentiometer R_2 until bits DB1-DB11 are ON and DB0 is toggling ON and OFF.

CALIBRATION PROCEDURE—BIPOLAR RANGES

If external adjustments of full-scale and bipolar offset are not required, the potentiometers in Figure 11 may be replaced by 50Ω, 1% metal film resistors.

If adjustments are required, connect the converter as shown in Figure 11. The calibration procedure is similar to that described above for unipolar operation, except that the offset adjustment is performed with an input voltage which is 1/2LSB above the minus full-scale value (–4.9988V for the ±5V range, –9.9976V for the ±10V range). Adjust R_1 for DB0 to toggle ON and OFF with all other bits OFF. To adjust full-scale, apply a DC input signal which is 3/2LSB below the nominal plus full-scale value (+4.9963V for ±5V range, +9.9927V for ±10V range) and adjust R_2 for DB0 to toggle ON and OFF with all other bits ON.

BURR-BROWN®

ADS602

12-Bit 1MHz Sampling ANALOG-TO-DIGITAL CONVERTER

FEATURES

- LOW LINEARITY ERROR
- SAMPLE RATE: 1MHz
- INPUT RANGES: ±5V, 0V to +10V
- COMPLETE SUBSYSTEM: Contains Sample/Hold and Reference
- 32-PIN CERAMIC DIP PACKAGE

APPLICATIONS

- DIGITAL SIGNAL PROCESSING
- HIGH-SPEED DATA ACQUISITION SYSTEMS
- MEDICAL INSTRUMENTATION
- ANALYTICAL INSTRUMENTATION
- TEST AND IMAGING SYSTEMS
- WAVEFORM ANALYZERS

DESCRIPTION

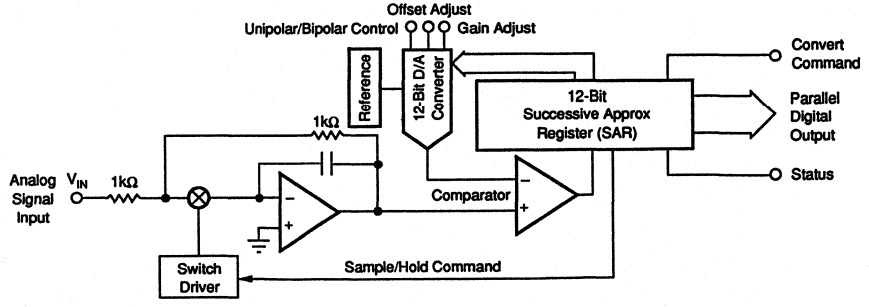
The ADS602 is a high-speed successive approximation analog-to-digital converter with internal sample/hold amplifier. This unique design utilizes a bipolar technology with on-chip thin film resistors to preserve analog accuracy and a high-speed CMOS chip to perform digital logic control. Outstanding linearity, noise, and dynamic range are achieved by this converter design. The ADS602 is thoroughly tested for dynamic performance.

The ADS602 is complete with internal reference, clock, and comparator and is packaged in a 32-pin ceramic DIP. Sample rate is set at the factory to 1MHz. Performance is guaranteed with no missing codes over the input voltage, power supply, and operating temperature range. The gain and offset errors are laser trimmed to specification. Optionally they may be externally adjusted to zero.

The user can switch between unipolar (0V to +10V) and bipolar (±5V) operation through one digital logic level input.

Output codes are available in complementary binary for unipolar inputs and complementary offset binary for bipolar inputs.

All digital input and output are TTL-compatible. Power supply requirements are ±15V and +5V.



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Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL

T_{CASE} = +25°C, 1MHz sampling rate, $\pm V_{CC}$ = ±15V, $+V_{DD}$ = +5V, and 6-minute warm-up in a normal convection environment unless otherwise noted.

PARAMETER	CONDITIONS	ADS602JG MIN	ADS602JG TYP	ADS602JG MAX	ADS602KG MIN	ADS602KG TYP	ADS602KG MAX	UNITS
RESOLUTION				12			*	Bits
ANALOG CHARACTERISTICS								
INPUTS								
Voltage Ranges: Bipolar	Full Scale (FSR) [1, 2]	–5		+5	*		*	V
Unipolar	Full Scale (FSR) [1, 2]	0		+10	*		*	V
Input Resistance			1			*		kΩ
Input Capacitance			5	10		*	*	pF
TRANSFER CHARACTERISTICS								
STATIC ACCURACY								
Gain Error [3, 4]			±0.2	±0.3		±0.1	±0.2	% of FSR
Input Offset Error [3, 4]: Unipolar			±0.1	±0.8		*	±0.4	% of FSR
Bipolar			±0.1	±0.6		*	±0.4	% of FSR
Integral Linearity Error			1.2	1.5		0.9	1.25	LSB
Differential Linearity Error			1.2	1.5		0.9	1.25	LSB
No Missing Codes			Guaranteed			*		
Power Supply Rejection of Offset and Gain	$\Delta \pm V_{CC}$ = ±10%		±0.0036	0.5		*	*	%FSR/%V_{CC}
	$\Delta \pm V_{DD}$ = ±10%		±0.001	0.5		*	*	%FSR/%V_{DD}
CONVERSION CHARACTERISTICS								
Sample Rate	Without User Adjustment	DC		1M	*		*	samples/s
Power Supply Rejection of Conversion Time	$\Delta +V_{DD}$ = ±5%		±1			*		ns/%V_{DD}
DYNAMIC CHARACTERISTICS (The sampling frequency [f_S] = 1MHz and the input signal level = –0.5dB, unless otherwise stated.)								
Differential Linearity Error[5]	f_C = 480kHz, 68% of All Codes		0.35			0.25		LSB
	99% of All Codes		0.6			0.5		LSB
	100% of All Codes		1.2			0.9	1.25	LSB
Spurious Free Dynamic Range	f_C = 10kHz		–74			–86	–76	dB
	f_C = 480kHz		–68			–73	–70	dB
Total Harmonic Distortion[6]	f_C = 10kHz		–79			–83	–75	dBc
	f_C = 480kHz		–70			–72	–70	dBc
Two-Tone Intermodulation Distortion [6, 7]	f_C = 90kHz and 110kHz (–6.5dB)		–77			*		dBc
Signal-to-Noise and Distortion	f_C = 10kHz		71		70	72		dB
(SINAD) Ratio	f_C = 480kHz		63		64	67		dB
Signal-to-Noise Ratio (SNR)	f_C = 10kHz		71		70	73		dB
	f_C = 480kHz		67		67	69		dB
Analog Input Bandwidth (–3dB)								
Small Signal	–20dB Input		16			*		MHz
Full Power	0dB Input		4			*		MHz
DIGITAL CHARACTERISTICS								
INPUT								
Logic Family			TTL-Compatible CMOS		*	*	*	
Convert Command Logic Voltages	Logic Low	0		+0.8	*		*	V
	Logic High	+2		$+V_{DD}$	*		*	V
Convert Command Currents	Logic Low			–150			*	µA
Convert Command			High Level When Converting		*	*	*	
OUTPUT								
Logic Family			TTL-Compatible CMOS		*	*	*	
Bits 1 through 12, Status	Logic Low, I_{OL} = 3.2mA		+0.1	+0.4		*	*	V
	Logic High, I_{OH} = –1mA	+2.7	+4.9		*	*		V
Internal Clock Frequency			17			*		MHz
Status			Low Level When Data Valid		*	*	*	
POWER SUPPLY REQUIREMENTS								
Supply Voltages: $+V_{CC}$	Operating	+14.25	+15	+15.75	*	*	*	V
$-V_{CC}$		–14.25	–15	–15.75	*	*	*	V
$+V_{DD}$		+4.75	+5	+5.25	*	*	*	mA
Supply Currents: $+I_{CC}$	Operating		26	30		*	*	mA
$-I_{CC}$			–110	–140		*	*	mA
$+I_{DD}$			60	80		*	*	mA
Power Consumption	Operating		2.3	2.8		*	*	W
Thermal Resistance, θ_{JC}[8]			8.7			*		°C/W

* Specification same as ADS602JG.

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SPECIFICATIONS (CONT)

ELECTRICAL (FULL TEMPERATURE SPECIFICATIONS)

$\pm V_{CC}$ = ±15V, $+V_{DD}$ = +5V, and 6-minute warm-up in a normal convection environment unless otherwise noted.

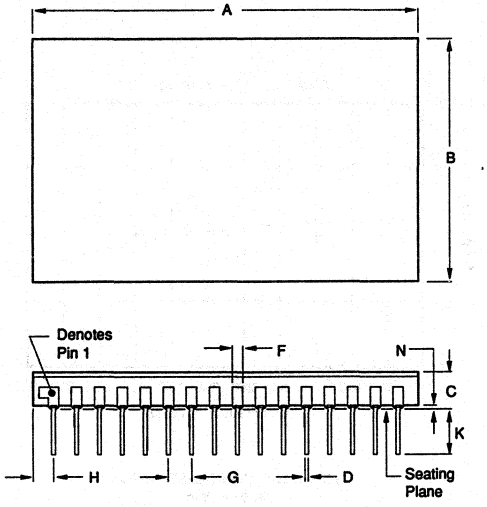
PARAMETER	CONDITIONS	ADS602JG MIN	ADS602JG TYP	ADS602JG MAX	ADS602KG MIN	ADS602KG TYP	ADS602KG MAX	UNITS
TEMPERATURE RANGE SPECIFICATION	T_{CASE}	0		+70	*		*	°C
TRANSFER CHARACTERISTICS								
STATIC ACCURACY								
Gain Error [4]			±0.2	±0.5		±0.1	±0.4	% of FSR
Input Offset Error [4]: Unipolar			±0.1	±0.8		*	±0.4	% of FSR
Bipolar			±0.1	±0.6		*	±0.4	% of FSR
Integral Linearity Error			1.25	1.5		1	1.25	LSB
Differential Linearity Error			1.25	1.5		1	1.25	LSB
No Missing Codes			Guaranteed			*		
Power Supply Rejection of Offset and Gain			±0.0036	0.5		*	*	%FSR/%V_{CC}
			±0.001	0.5		*	*	%FSR/%V_{DD}
CONVERSION CHARACTERISTICS								
Sample Rate	Without User Adjustment	DC		1M	*		*	samples/s
Power Supply Rejection of Conversion Time	Δ $+V_{DD}$ = ±5%		±1			*		ns/%V_{DD}
DYNAMIC CHARACTERISTICS (The sampling frequency [f_S] = 1MHz and the input signal level = –0.5dB, unless otherwise stated.)								
Differential Linearity Error	f_C = 480kHz, 68% of All Codes		0.35			0.25		LSB
	99% of All Codes		0.7			0.6		LSB
	100% of All Codes		1.3			1	1.25	LSB
Spurious Free Dynamic Range	f_C = 10kHz		73			85	71	dB
	f_C = 480kHz		62			65		dB
Total Harmonic Distortion	f_C = 10kHz		–81			–83	–70	dBc
	f_C = 480kHz		–63			–65		dBc
Two-Tone Intermodulation Distortion [7]	f_C = 90kHz and 110kHz (–6.5dB)		–77			–79		dBc
Signal-to-Noise and Distortion	f_C = 10kHz		71		68	70		dB
(SINAD) Ratio	f_C = 480kHz		63			64		dB
Signal-to-Noise Ratio (SNR)	f_C = 10kHz		71		70	73		dB
	f_C = 480kHz		67		67	69		dB
Analog Input Bandwidth (–3dB)								
Small Signal	–20dB Input		16			*		MHz
Full Power	0dB		4			*		MHz
DIGITAL CHARACTERISTICS								
INPUT								
Logic Family			TTL-Compatible CMOS		*	*	*	
Convert Command Logic Voltages	Logic Low	0		+0.8	*		*	V
	Logic High	+2		$+V_{DD}$	*		*	V
Convert Command Currents	Logic Low			–150			*	µA
Convert Command			High Level When Converting		*	*	*	
OUTPUT								
Logic Family			TTL-Compatible CMOS		*	*	*	
Bits 1 through 12, Status	Logic Low, I_{OL} = 3.2mA		+0.1	+0.4		*	*	V
	Logic High, I_{OH} = –1mA	+2.7	+4.9		*	*		V
Internal Clock Frequency			17			*		MHz
Status			Low Level When Data Valid		*	*	*	
POWER SUPPLY REQUIREMENTS								
Supply Voltages: $+V_{CC}$	Operating	+14.25	+15	+15.75	*	*	*	V
$-V_{CC}$		–14.25	–15	–15.75	*	*	*	V
$+V_{DD}$		+4.75	+5	+5.25	*	*	*	mA
Supply Currents: $+I_{CC}$	Operating		26	30		*	*	mA
$-I_{CC}$			–110	–140		*	*	mA
$+I_{DD}$			60	80		*	*	mA
Power Consumption	Operating		2.3	2.8		*	*	W
Thermal Resistance, θ_{JC} [8]			8.7			*		°C/W

* Specification same as ADS602JG.

NOTES: (1) Over or under range on the analog input results in constant maximum or minimum digital output. (2) FSR = Full Scale Range. (3) Adjustable to zero. (4) If gain and offset adjust pins are not used, they should be grounded. (5) See Typical Performance Curves. (6) dBc = level referred to carrier input signal = –0.5dB of full scale; f_C = input frequency, f_S = sampling frequency. (7) IMD is referred to the larger of the two input test signals. If referred to the peak envelope signal (=0dB), the intermodulation products will be 6dB lower. (8) Temperature ranges refer to case temperature. Thermal resistance was measured on a small (5" diameter) handwired circuit board, with the test device in a zero-insertion-force socket. Thermal resistance will be lower if the ADS602 is soldered into the PC board, a ground plane is used directly underneath the package, multiple PC board layers are used, or forced air cooling is employed. Use heat sinking if necessary to keep the case at specified and operating temperatures.

MECHANICAL

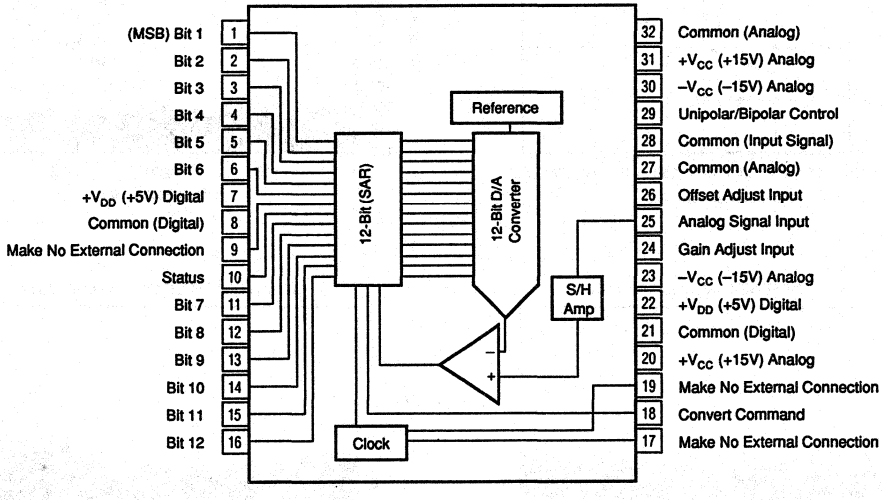
G Package — 32-Pin Ceramic Bottom-Braze



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.678	1.712	42.62	43.48
B	1.079	1.101	27.41	27.97
C	.180	.210	4.57	5.33
D	.016	.020	.41	.51
F	.045	.055	1.14	1.40
G	.100 BASIC		2.54 BASIC	
H	.089	.106	2.26	2.69
J	.009	.012	.23	.30
K	.200	.210	5.08	5.33
L	.900 BASIC		22.86 BASIC	
N	.015	.035	.38	.89

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

$\pm V_{CC}$	±18V
$+V_{DD}$	+7V
Digital Inputs	+5.5V
Analog Inputs	$\pm V_{CC}$
Case Temperature	+125°C
Junction Temperature	+150°C
Storage Temperature	–65°C to +150°C

Stresses above these ratings may permanently damage the device.

ORDERING INFORMATION

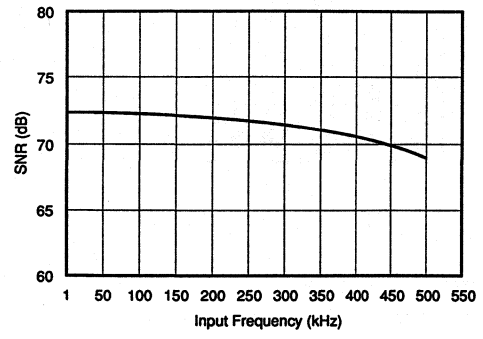
ADS602 ( ) G

- Basic Model Number
- Performance Grade Code
  J, K: 0°C to +70°C Case Temperature
- Package Code
  G: Ceramic Bottom Braze

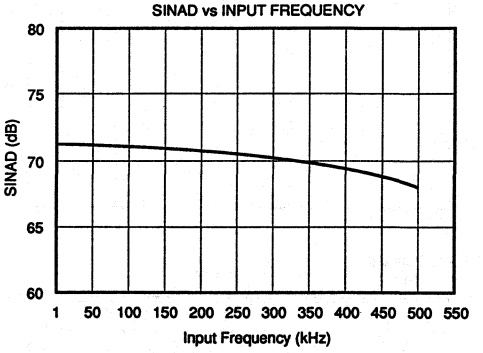
TYPICAL PERFORMANCE CURVES

$\pm V_{CC}$ = ±15V, $+V_{DD}$ = +5V, 1MHz sampling rate, 6-minute warmup, and T_C = +25°C unless otherwise noted.

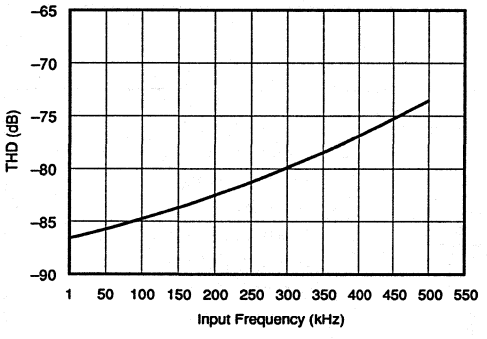
SNR vs INPUT FREQUENCY



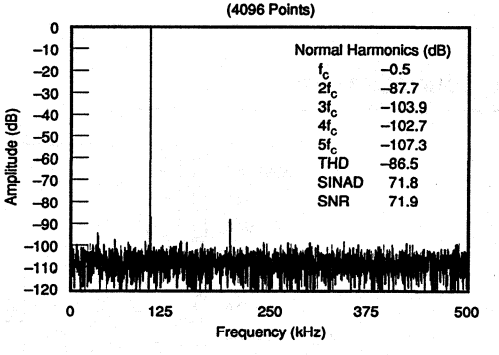
SINAD vs INPUT FREQUENCY



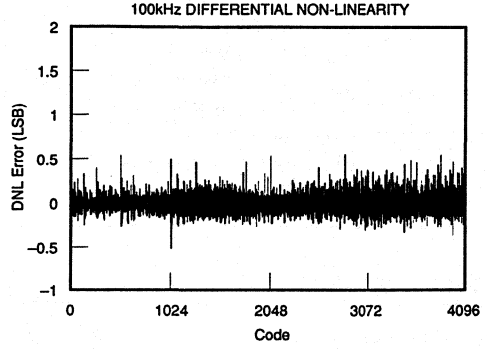
THD vs INPUT FREQUENCY



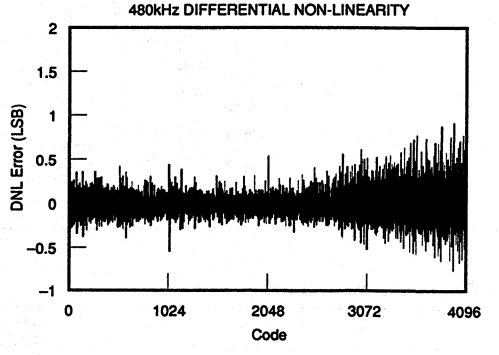
100kHz HARMONIC DISTORTION
(4096 Points)



100kHz DIFFERENTIAL NON-LINEARITY



480kHz DIFFERENTIAL NON-LINEARITY



PIN DEFINITIONS

PIN NUMBER	DESIGNATION	DESCRIPTION
1-6 and 11-16	Bit 1 to Bit 12	12-bit parallel output data.
10	Status	Conversion status strobe is high during data conversion, low when parallel data is valid.
18	Convert Command	High transition starts conversion, and should remain high during conversion. Low will reset clock and SAR logic. Rising edge may be used to latch data from previous conversion.
24	Gain Adjust Input	Allows gain error to be externally adjusted to zero. Ground this pin if it is not used.
25	Analog Signal Input	Signal input to internal S/H amplifier.
26	Offset Adjust Input	Allows offset error to be externally adjusted to zero. Ground this pin if it is not used.
29	Unipolar/Bipolar Control	Ground on this pin engages unipolar operation (0V to +10V). Leaving this pin open engages bipolar (±5V).

The ADS602 is a sampling A/D converter that employs a successive approximation architecture. The ideal transfer function for an ADS602 in the bipolar mode is described in Figure 1. Initial gain and offset errors may be adjusted to zero, gain drift over temperature rotates the transfer function about –full scale end point, and offset drift shifts the transfer function left or right over the operating temperature range. Integral linearity error is the deviation of an actual bit transition from the best fit straight line transfer function of the converter. A differential linearity error of 0.012% means that the width of each bit step over the range of the converter is 1LSB, ±0.5LSB. The ADS602 is guaranteed to have no missing codes over its temperature range.

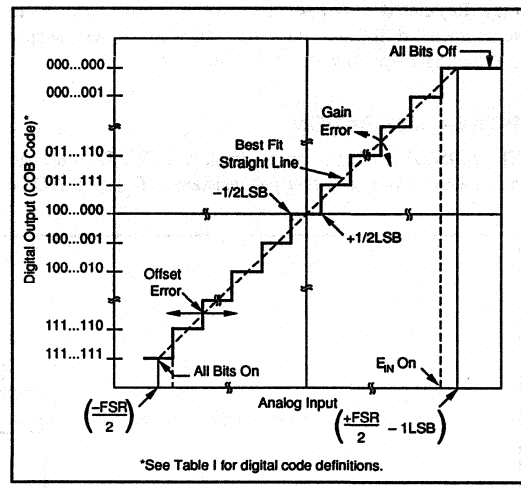


FIGURE 1. Input vs Output for an Ideal Bipolar A/D Converter.

INSTALLATION AND OPERATING INSTRUCTIONS

BASIC CONNECTION

The basic connection for the ADS602 is shown in Figure 2. It is shown connected for ±5V bipolar operation. For unipolar operation, pin 29 should be grounded.

INTERFACING

The ADS602 has an impedance of approximately 1k; therefore, to maintain gain accuracy it must be driven from a low impedance source. The digital output lines should be buffered by a latch such as the 74AS574. These three-state drivers can then be connected directly to the data bus.

LAYOUT PRECAUTIONS

The ADS602 is a high-speed sampling analog-to-digital converter which requires more attention to circuit board layout than general purpose lower speed A/D converters.

The ADS602 has two pins for analog common, two pins for digital common, and two pins for each power supply input. Each pair of these pins must be connected together since they are not connected together internally. Connecting all commons to a ground plane close to the ADS602 is the best method to maximize performance. The ground plane minimizes noise and provides additional heat dissipation.

ANALOG INPUT VOLTAGE RANGE	±5V	0V TO +10V
Code Designation	COB (1)	CSB (2)
One Least Significant Bit (LSB)	2.44mV	2.44mV
Transition Values MSB LSB (3)		
111...111)		
111...110)	–5V + 1/2LSB	0V + 1/2LSB
100...000)		
011...111)	–1/2LSB	+5 – 1/2LSB
000...001)		
000...000)	+5 – 3/2LSB	10V – 3/2LSB

NOTES: (1) COB = complementary offset binary. (2) CSB = complementary straight binary. (3) Voltages given are the nominal value for the transition from the next code.

TABLE I. Input Voltages, Transition Values, LSB Values, and Code Definitions.

POWER SUPPLY DECOUPLING AND POWER SUPPLY SENSITIVITY

The +15V and +5V power supply pins should be bypassed with a 10µF tantalum capacitor as shown in Figure 2. Pin 30 requires bypassing with a 150µF tantalum capacitor. These capacitors should be located close to the ADS602 supply pins. Ceramic 0.01µF bypass capacitors have been provided internally for more effective bypassing and need not be added externally.

Changes in the DC power supply voltages will affect accuracy. Regulated power supplies with 1% or less ripple are recommended for use with the ADS602. Power supply decoupling helps to keep ripple low.

POWER DISSIPATION

The ADS602 dissipates approximately 2.3W. The package has a junction-to-case thermal resistance (θ_{JC}) of 8.7°C/W and a case-to-ambient thermal resistance (θ_{CA}) of 13.7°C/W in a normal convection environment.

OPTIONAL EXTERNAL GAIN AND OFFSET ADJUSTMENTS

Gain and offset errors may be trimmed to zero using external trim potentiometers as shown in Figure 2. Multiturn potentiometers with 100ppm/°C temperature coefficient are recommended for minimum drift. If the gain adjust or offset adjust pins are not used, they must be grounded to meet the specified accuracy.

DYNAMIC PERFORMANCE TESTING

The ADS602 is a high performance sampling A/D converter and careful attention to test techniques is necessary to achieve accurate results. Spectral analysis by application of a fast Fourier transform (FFT) to the ADC digital output will provide data on important dynamic performance parameters.

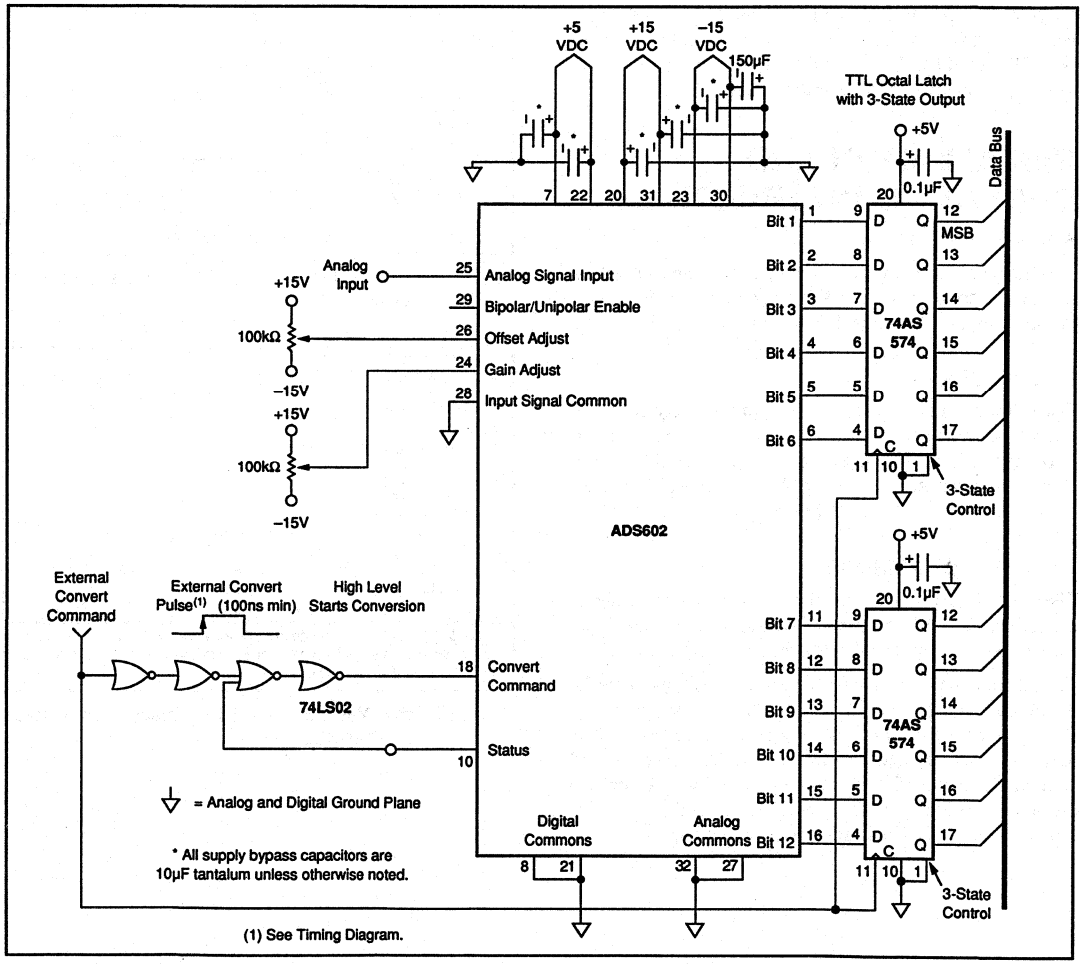


FIGURE 2. ADS602 Application Circuit.

Dynamic Performance Definitions

1. Signal-to-Noise-and-Distortion Ratio (SINAD):

$$10 \log \frac{\text{sinewave signal power}}{\text{noise + harmonic power (first 9 harmonics)}}$$

2. Signal-to-Noise Ratio (SNR):

$$10 \log \frac{\text{sinewave signal power}}{\text{noise power}}$$

3. Total Harmonic Distortion (THD):

$$10 \log \frac{\text{harmonic power (first 9 harmonics)}}{\text{sinewave signal power}}$$

4. Spurious Free Dynamic Range (SFDR):

$$10 \log \frac{\text{largest harmonic power}}{\text{sinewave signal power}}$$

5. Intermodulation Distortion (IMD):

$$10 \log \frac{\text{highest IMD product power (to 5th order)}}{\text{sinewave signal power}}$$

IMD is referred to the larger of the test signals f1 or f2. Five "bins" either side of peak are used for calculation of fundamental and harmonic power. The "0" frequency bin (DC) is not included in these calculations as it is of little importance in dynamic signal processing applications.

TIMING CONSIDERATIONS

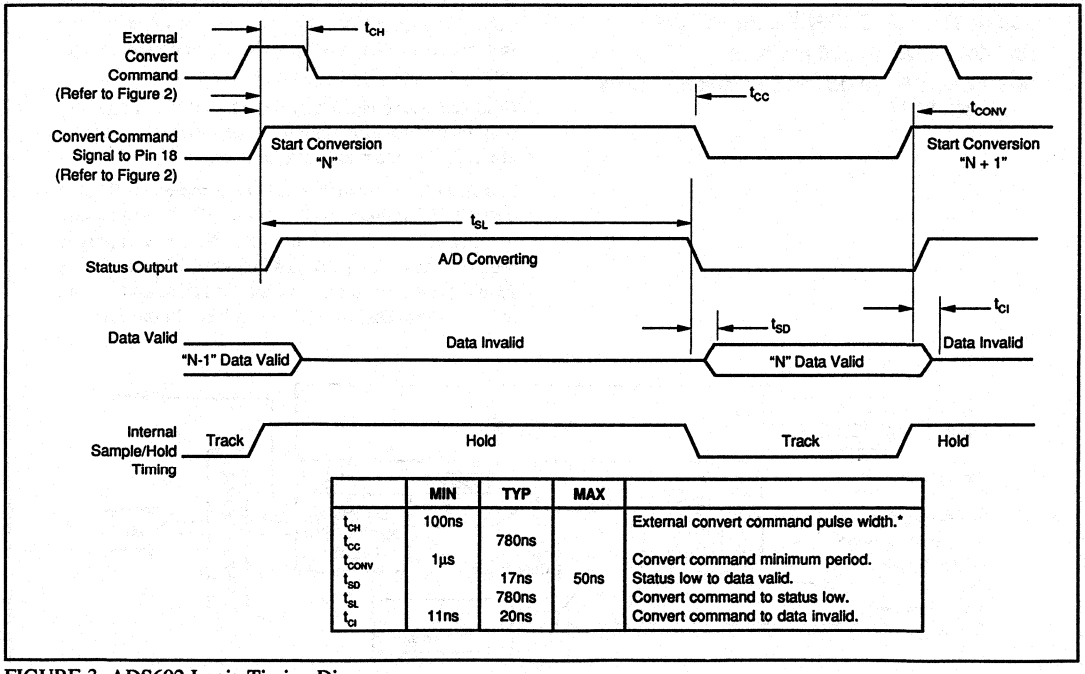
In addition to the timing details in Figure 3, the following list contains some important timing considerations for the ADS602:

1. When power is first applied, the convert command should be held low or below the +5V supply to prevent latch up.

2. The rising edge of the convert command pulse initiates a conversion. This convert command should remain high until the Status falls (i.e., the internal ADC is finished converting). A simple circuit that provides the correct convert command (pin 18) pulse length, is shown in Figure 2.

3. The ADS602 goes directly into the "hold" mode when a convert command signal is given. The Status falls approximately 780ns later, indicating that the conversion is complete. At this time, the sample-hold (internal to the ADS602) enters the track mode. The ADS602 will remain in the track mode until the next convert command is given.

4. The data from conversion "N" can be latched directly by the convert command pulse "N + 1". This approach is illustrated in Figure 2. The falling edge of Status may be used to latch the data; however, Status must be delayed by t_{SD} (see Figure 3) plus the external latch (74AS574) setup time.



	MIN	TYP	MAX	
t_{CH}	100ns			External convert command pulse width.*
t_{CC}		780ns		
t_{CONV}	1µs			Convert command minimum period.
t_{SD}		17ns	50ns	Status low to data valid.
t_{SL}		780ns		Convert command to status low.
t_{CI}	11ns	20ns		Convert command to data invalid.

FIGURE 3. ADS602 Logic Timing Diagram.

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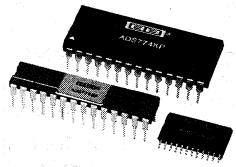


ADS774

AVAILABLE IN DIE

Microprocessor-Compatible Sampling CMOS ANALOG-to-DIGITAL CONVERTER

FEATURES

- **COMPATIBLE WITH ADC574, ADC674 AND ADC774 SOCKETS**
- **COMPLETE SAMPLING A/D WITH REFERENCE, CLOCK AND MICROPROCESSOR INTERFACE**
- **FAST ACQUISITION AND CONVERSION: 8.5µs max OVER TEMPERATURE**
- **ELIMINATES EXTERNAL SAMPLE/HOLD IN MOST APPLICATIONS**
- **GUARANTEED AC AND DC PERFORMANCE**
- **SINGLE +5V SUPPLY OPERATION**
- **LOW POWER: 120mW max**
- **PACKAGE OPTIONS: 0.6" and 0.3" DIPs, SOIC, DIE**

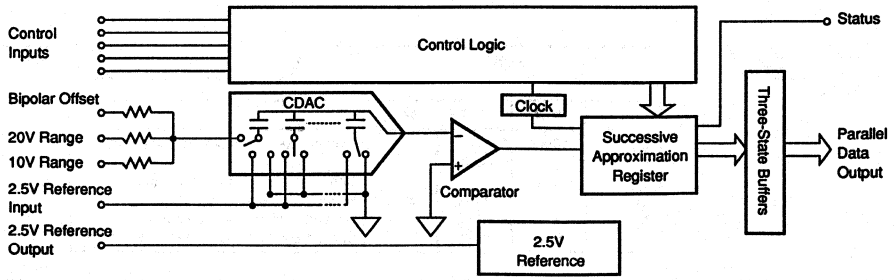
DESCRIPTION

The ADS774 is a 12-bit successive approximation analog-to-digital converter using an innovative capacitor array (CDAC) implemented in low-power CMOS technology. This is a drop-in replacement for ADC574, ADC674, and ADC774 models in most applications, with internal sampling, much lower power consumption, and the ability to operate from a single +5V supply.

The ADS774 is complete with internal clock, microprocessor interface, three-state outputs, and internal scaling resistors for input ranges of 0V to +10V, 0V to +20V, ±5V, or ±10V. The maximum throughput time is 8.5µs over the full operating temperature range, including both acquisition and conversion.

Complete user control over the internal sampling function facilitates elimination of external sample/hold amplifiers in most existing designs.

The ADS774 is available in both commercial (0°C to +70°C) and military (–55°C to +125°C) ranges, and requires +5V, with –15V optional. No +15V supply is required. Available packages include 0.3" or 0.6" wide 28-pin plastic or hermetic ceramic DIPs, and 28-pin SOICs. The ADS774 is also available in die form.



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Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL

$T_A = T_{MIN}$ to T_{MAX}, V_{DD} = +5V, V_{EE} = −15V to +5V, sampling frequency of 117kHz, f_{IN} = 10kHz; unless otherwise specified.

PARAMETER	ADS774JE/JH/JP/JU/SF/SH/D MIN	ADS774JE/JH/JP/JU/SF/SH/D TYP	ADS774JE/JH/JP/JU/SF/SH/D MAX	ADS774KE/KH/KP/KU/TF/TH MIN	ADS774KE/KH/KP/KU/TF/TH TYP	ADS774KE/KH/KP/KU/TF/TH MAX	UNITS
RESOLUTION			12			*	Bits
INPUTS							
ANALOG							
Voltage Ranges: Unipolar			0 to +10, 0 to +20				V
Bipolar			±5, ±10				V
Impedance: 0 to +10V, ±5V	8.5	12		*	*		kΩ
±10V, 0V to +20V	35	50		*	*		kΩ
DIGITAL (CE, $\overline{CS}$, R/$\overline{C}$, A_0, 12/$\overline{8}$)							
Voltages: Logic 1	+2.0		+5.5	*		*	V
Logic 0	−0.5		+0.8	*		*	V
Current	−5	0.1	+5	*	*	*	µA
Capacitance		5			*		pF
TRANSFER CHARACTERISTICS							
DC ACCURACY							
At +25°C							
Linearity Error			±1			±1/2	LSB
Unipolar Offset Error (adjustable to zero)			±2			*	LSB
Bipolar Offset Error (adjustable to zero)			±10			±4	LSB
Full-Scale Calibration Error [1] (adjustable to zero)			±0.25			*	% of FS [2]
No Missing Codes Resolution (Diff. Linearity)	12			12			Bits
Inherent Quantization Error		±1/2			*		LSB
T_{MIN} to T_{MAX}							
Linearity Error: J, K Grades			±1			±1/2	LSB
S, T Grades			±1			±3/4	LSB
Full-Scale Calibration Error							
Without Initial Adjustment [1]: J, K Grades			±0.47			±0.37	% of FS
S, T Grades			±0.75			±0.5	% of FS
Adjusted to Zero at +25°C: J, K Grades			±0.22			±0.12	% of FS
S, T Grades			±0.5			±0.25	% of FS
No Missing Codes Resolution (Diff. Linearity)	12			12			Bits
AC ACCURACY [3]							
Spurious Free Dynamic Range	73	78		76	*		dB
Total Harmonic Distortion		−77	−72		*	−75	dB
Signal-to-Noise Ratio	69	72		71	*		dB
Signal-to-(Noise + Distortion) Ratio	68	71		70	*		dB
Intermodulation Distortion (F_{IN1} = 20kHz, F_{IN2} = 23kHz)		−75			*		
TEMPERATURE COEFFICIENTS [4]							
Unipolar Offset			±5			±2.5	ppm/°C
Max Change			±2			±1	LSB
Bipolar Offset			±10			±5	ppm/°C
Max Change: J, K Grades			±2			±1	LSB
S, T Grades			±4			±2	LSB
Full-Scale Calibration			±45			±25	ppm/°C
Max Change: J, K Grades			±9			±5	LSB
S, T Grades			±20			±10	LSB
POWER SUPPLY SENSITIVITY							
Change in Full-Scale Calibration[5]							
+4.75V < V_{DD} < +5.25V							
Max Change: J, K Grades			±1/2			*	LSB
S, T Grades			±1			*	LSB
CONVERSION TIME (Including Acquisition Time)							
t_{AQ} + t_C at 25°C:							
8-Bit Cycle		5.5	5.9		*	*	µs
12-Bit Cycle		7.5	8		*	*	µs
12-Bit Cycle, T_{MIN} to T_{MAX}:		8	8.5		*	*	µs

SPECIFICATIONS (CONT)

ELECTRICAL

$T_A = T_{MIN}$ to T_{MAX}, V_{DD} = +5V, V_{EE} = –15V to +5V, sampling frequency of 117kHz, f_{IN} = 10kHz; unless otherwise specified.

PARAMETER	ADS774JE/JH/JP/JU/SF/SH/D MIN	ADS774JE/JH/JP/JU/SF/SH/D TYP	ADS774JE/JH/JP/JU/SF/SH/D MAX	ADS774KE/KH/KP/KU/TF/TH MIN	ADS774KE/KH/KP/KU/TF/TH TYP	ADS774KE/KH/KP/KU/TF/TH MAX	UNITS
SAMPLING DYNAMICS							
Sampling Rate at 25°C	125			*			kHz
T_{MIN} to T_{MAX}	117			*			kHz
Aperture Delay, t_{AP}							
With V_{EE} = +5V		20			*		ns
With V_{EE} = 0V to –15V		1.6			*		µs
Aperture Uncertainty (Jitter)							
With V_{EE} = +5V		300			*		ps, rms
With V_{EE} = 0V to –15V		10			*		ns,rms
Settling time to 0.01% for Full-Scale Input Change		1.4			*		µs
OUTPUTS							
DIGITAL (DB_{11} - DB_0, STATUS)							
Output Codes: Unipolar			Unipolar Straight Binary (USB)				
Bipolar			Bipolar Offset Binary (BOB)				
Logic Levels: Logic 0 (I_{SINK} = 1.6mA)			+0.4			*	V
Logic 1 (I_{SOURCE} = 500µA)	+2.4			*			V
Leakage, Data Bits Only, High-Z State	–5	0.1	+5	*	*	*	µA
Capacitance		5			*		pF
INTERNAL REFERENCE VOLTAGE							
Voltage	+2.4	+2.5	+2.6	*	*	*	V
Source Current Available for External Loads	0.5			*			mA
POWER SUPPLY REQUIREMENTS							
Voltage: V_{EE} (6)	–16.5		V_{DD}	*		*	V
V_{DD}	+4.5		+5.5	*		*	V
Current: I_{EE} (6) (V_{EE} = –15V)		–1			*		mA
I_{DD}		+15	+24		*	*	mA
Power Dissipation (T_{MIN} to T_{MAX})							
(V_{EE} = 0V to +5V)		75	120		*	*	mW
TEMPERATURE RANGE							
Specification: J, K Grades	0		+70	*		*	°C
S, T Grades	–55		+125	*		*	°C
Operating: J, K Grades	–40		+85	*		*	°C
S, T Grades	–55		+125	*		*	°C
Storage Temperature Range	–65		+150	*		*	°C

*Same specification as ADS774JE/JH/JP/JU/SF/SH.

NOTES: (1) With fixed 50Ω resistor from REF OUT to REF IN. This parameter is also adjustable to zero at +25°C. (2) FS in this specification table means Full Scale Range. That is, for a ±10V input range, FS means 20V; for a 0 to +10V range, FS means 10V. (3) Based on using V_{EE} = +5V, which is the Control Mode. See the section "S/H Control Mode and ADC774 Emulation Mode." (4) Using internal reference. (5) This is worst case change in accuracy from accuracy with a +5V supply. (6) V_{EE} is optional, and is only used to set the mode for the internal sample/hold. When V_{EE} = –15V, I_{EE} = –1mA typ; when V_{EE} = 0V, I_{EE} = ±5µA typ; when V_{EE} = +5V, I_{EE} = +167µA typ.

ABSOLUTE MAXIMUM RATINGS

V_{EE} to Digital Common ..... $+V_{DD}$ to –16.5V
V_{DD} to Digital Common ..... 0V to +7V
Analog Common to Digital Common ..... ±1V
Control Inputs (CE, $\overline{CS}$, A_0, 12/$\overline{8}$, R/$\overline{C}$)
to Digital Common ..... –0.5V to V_{DD} +0.5V
Analog Inputs (Ref In, Bipolar Offset, $10V_{IN}$)
to Analog Common ..... ±16.5V
$20V_{IN}$ to Analog Common ..... ±24V
Ref Out ..... Indefinite Short to Common, Momentary Short to V_{DD}
Max Junction Temperature ..... +165°C
Power Dissipation 1000mW
Lead Temperature (soldering,10s) ..... +300°C
Thermal Resistance, θ_{JA} : Ceramic DIPs ..... 50°C/W
Plastic DIPs ..... 100°C/W
SOIC ..... 100°C/W

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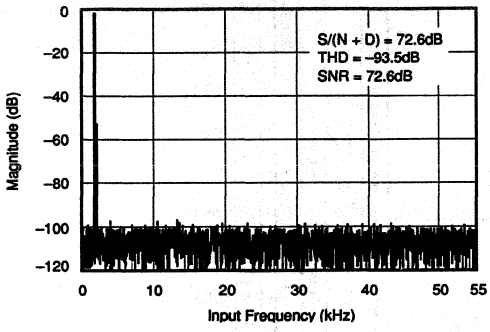
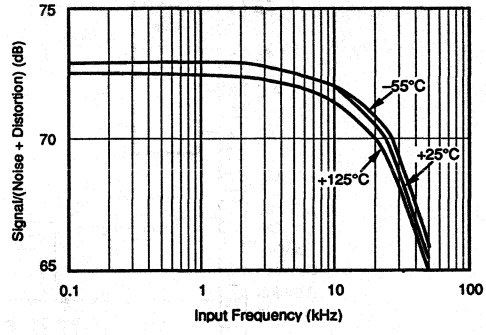
TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_{DD} = V_{EE} = +5V; Bipolar ±10V Input Range; sampling frequency of 110kHz; unless otherwise specified. All plots use 4096 point FFTs.

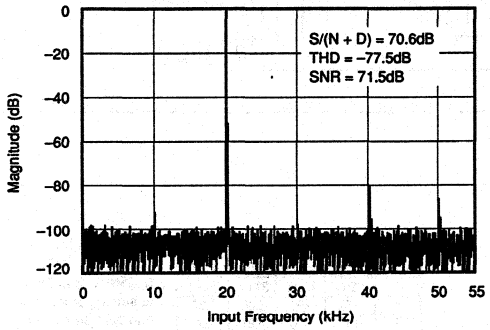
FREQUENCY SPECTRUM (±10V, 2kHz Input)



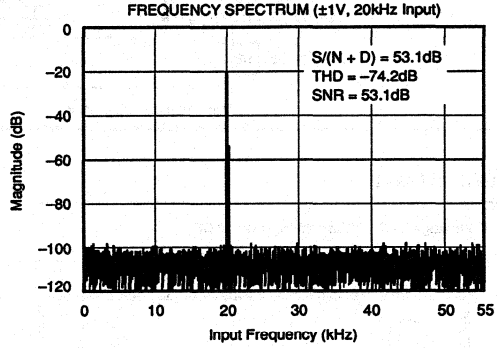
SIGNAL/(NOISE + DISTORTION) vs INPUT FREQUENCY AND AMBIENT TEMPERATURE



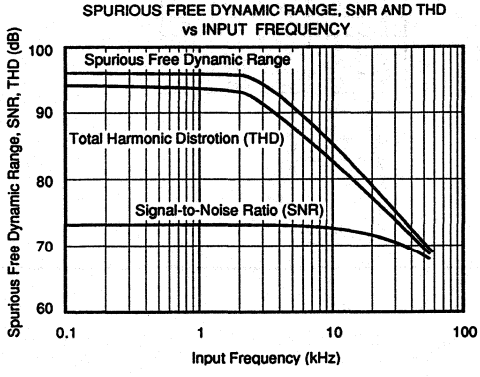
FREQUENCY SPECTRUM (±10V, 20kHz Input)



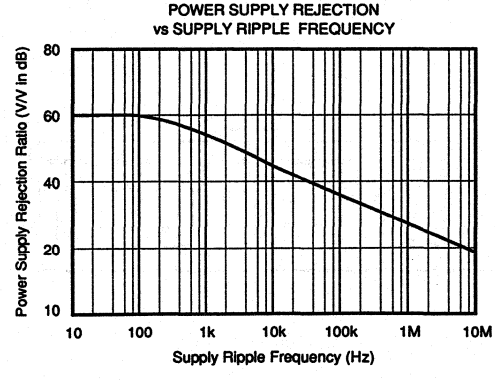
FREQUENCY SPECTRUM (±1V, 20kHz Input)



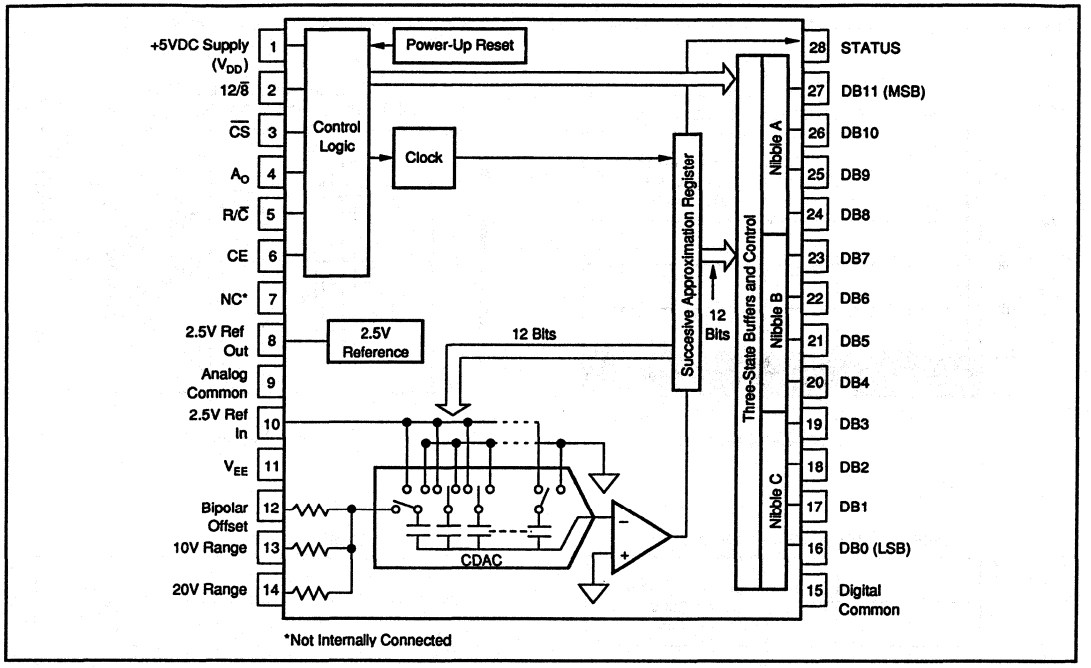
SPURIOUS FREE DYNAMIC RANGE, SNR AND THD vs INPUT FREQUENCY



POWER SUPPLY REJECTION vs SUPPLY RIPPLE FREQUENCY

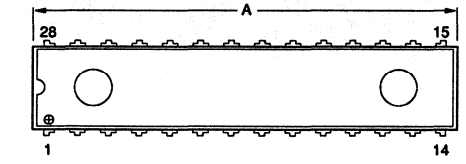


CONNECTION DIAGRAM



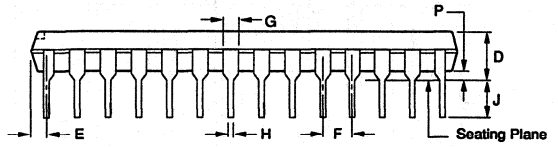
MECHANICAL

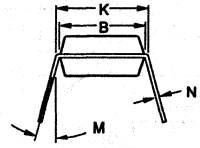
E Package — 0.3" Wide 28-Pin Plastic DIP



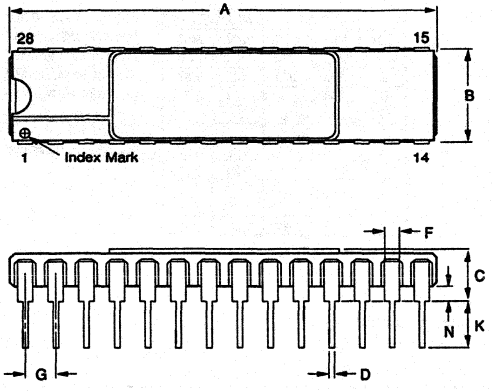
DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.255	1.355	31.88	34.42
B	.270	.290	6.86	7.37
D	.150	.170	3.81	4.32
E	.010	.080	0.25	2.03
F	.100 BASIC		2.54 BASIC	
G	.045	.055	1.14	1.40
H	.016	.020	0.41	0.51
J	.125	N/A	3.18	N/A
K	.300 BASIC		7.62 BASIC	
M	0°	15°	0°	15°
N	.008	.015	0.20	0.38
P	.020	.040	0.51	1.02

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.





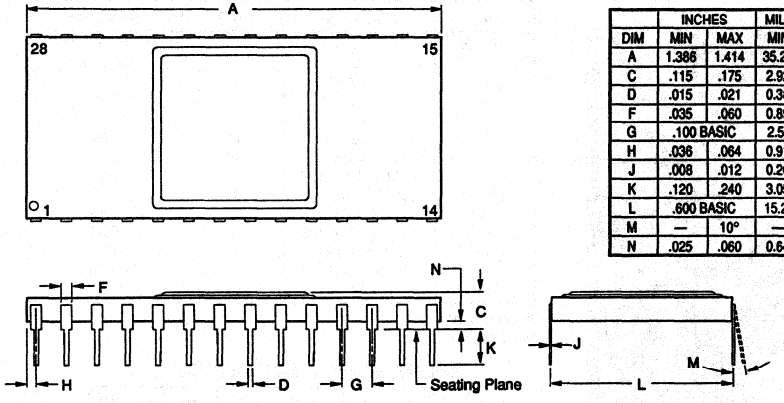
F Package — 0.3" 28-Pin Hermetic DIP



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.388	1.412	35.26	35.86
B	.300	.320	7.62	8.13
C	—	.160	—	4.06
D	.016	.020	0.41	0.51
F	.050 BASIC		1.27 BASIC	
G	.095	.105	2.41	2.67
J	.009	.012	0.23	0.30
K	.125	.180	3.18	4.57
L	.290	.310	7.37	7.87
N	.040	.060	1.02	1.52

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.

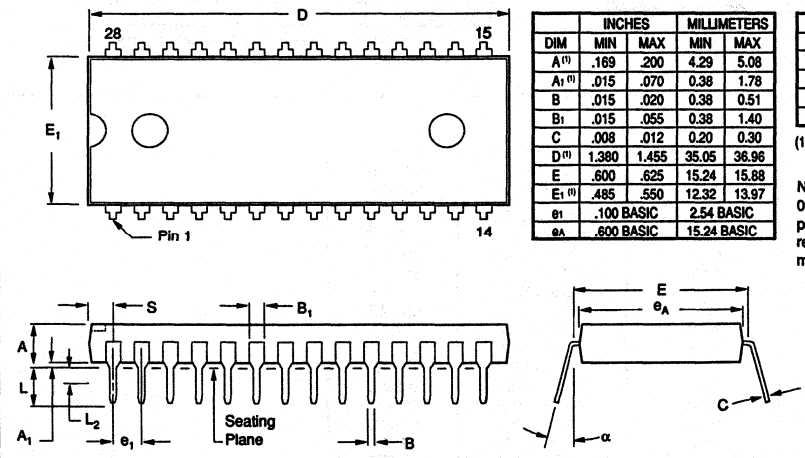
H Package — 0.6" Wide 28-Pin Hermetic DIP



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.386	1.414	35.20	35.92
C	.115	.175	2.92	4.45
D	.015	.021	0.38	0.53
F	.035	.060	0.89	1.52
G	.100 BASIC		2.54 BASIC	
H	.036	.064	0.91	1.63
J	.008	.012	0.20	0.30
K	.120	.240	3.05	6.10
L	.600 BASIC		15.24 BASIC	
M	—	10°	—	10°
N	.025	.060	0.64	1.52

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.

P Package — 0.6" Wide 28-Pin Plastic DIP



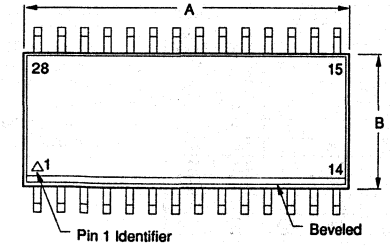
DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A(1)	.169	.200	4.29	5.08
A1(1)	.015	.070	0.38	1.78
B	.015	.020	0.38	0.51
B1	.015	.055	0.38	1.40
C	.008	.012	0.20	0.30
D(1)	1.380	1.455	35.05	36.96
E	.600	.625	15.24	15.88
E1(1)	.485	.550	12.32	13.97
e1	.100 BASIC		2.54 BASIC	
eA	.600 BASIC		15.24 BASIC	

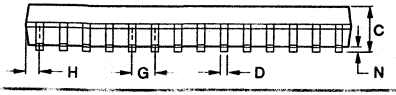
DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
L	.100	.200	2.54	5.08
L2	.000	.030	0.00	0.76
α	0°	15°	0°	15°
S(1)	.040	.080	1.02	2.03

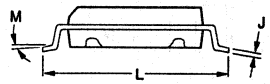
(1) Not JEDEC Standard

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.

U Package — 28-Pin Plastic SOIC



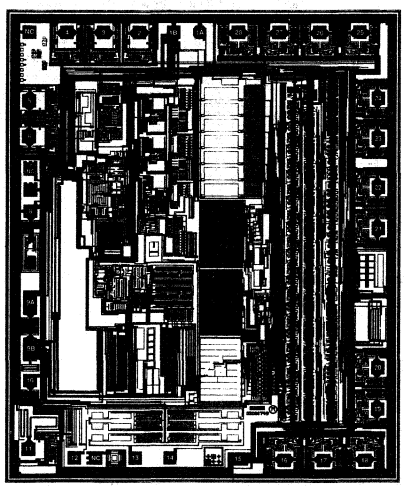




DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.700	.716	17.78	18.19
B	.286	.302	7.26	7.67
C	.093	.109	2.36	2.77
D	.016 BASIC		0.41 BASIC	
G	.050 BASIC		1.27 BASIC	
H	.022	.038	0.56	0.97
J	.008	.012	0.20	0.30
L	.398	.414	10.11	10.52
M	5° TYP		5° TYP	
N	.000	.012	0.00	0.30

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.

DICE INFORMATION



ADS774 DIE TOPOGRAPHY

PAD	FUNCTION	PAD	FUNCTION
1A, 1B	V_{DD}	15	Digital Common
2	12/$\overline{8}$	16	DB0 (LSB)
3	$\overline{CS}$	17	DB1
4	A_0	18	DB2
5	R/$\overline{C}$	19	DB3
6	CE	20	DB4
7	NC	21	DB5
8	2.5V Ref Out	22	DB6
9A, 9B	Analog Common	23	DB7
10	2.5 Ref In	24	DB8
11	V_{EE} (Mode Control)	25	DB9
12	Bipolar Offset	26	DB10
13	10V Range	27	DB11 (MSB)
14	20V Range	28	Status

Substrate Bias: $+V_{DD}$
NC: No Connection.

MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	172 x 142 ±5	4.37 x 3.61 ±0.13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.10 x 0.10
Metalization	Aluminum	

See "DICE PRODUCTS" Section 17 in Data Book Supplement Volume 33c, or contact Burr-Brown for current information.

ORDERING INFORMATION

MODEL	PACKAGE	SINAD[1]	TEMPERATURE RANGE	LINEARITY ERROR
ADS774JE	0.3" Plastic DIP	68dB	0°C to +70°C	±1LSB
ADS774KE	0.3"Plastic DIP	70dB	0°C to +70°C	±1/2LSB
ADS774JH	0.6" Ceramic DIP	68dB	0°C to +70°C	±1LBB
ADS774KH	0.6" Ceramic DIP	70dB	0°C to +70°C	±1/2LSB
ADS774JP	0.6" Plastic DIP	68dB	0°C to +70°C	±1LSB
ADS774KP	0.6"Plastic DIP	70dB	0°C to +70°C	±1/2LSB
ADS774JU	SOIC	68dB	0°C to +70°C	±1LSB
ADS774KU	SOIC	70dB	0°C to +70°C	±1/2LSB
ADS774SF	0.3" Ceramic DIP	68dB	–55°C to +125°C	±1LSB
ADS774TF	0.3" Ceramic DIP	70dB	–55°C to +125°C	±1/2LSB
ADS774SH	0.6" Ceramic DIP	68dB	–55°C to +125°C	±1LSB
ADS774TH	0.6" Ceramic DIP	70dB	–55°C to +125°C	±1/2LSB
ADS774D	25 Die per pack	68dB	0°C to +70°C	±1LSB

NOTE: (1) SINAD is Signal to (Noise and Distortion) expressed in dB.

THEORY OF OPERATION

In the ADS774, the advantages of advanced CMOS technology—high logic density, stable capacitors, precision analog switches—and Burr-Brown's state of the art laser trimming techniques are combined to produce a fast, low power analog-to-digital converter with internal sample/hold.

The charge-redistribution successive-approximation circuitry converts analog input voltages into digital words.

A simple example of a charge-redistribution A/D converter with only 3 bits is shown in Figure 1.

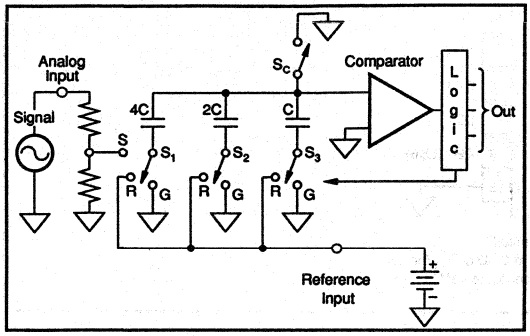


FIGURE 1. 3-Bit Charge Redistribution A/D.

INPUT SCALING

Precision laser-trimmed scaling resistors at the input divide standard input ranges (0V to +10V, 0V to +20V, ±5V or ±10V) into levels compatible with the CMOS characteristics of the internal capacitor array.

SAMPLING

While sampling, the capacitor array switch for the MSB capacitor (S_1) is in position "S", so that the charge on the MSB capacitor is proportional to the voltage level of the analog input signal. The remaining array switches (S_2 and S_3) are set to position "G". Switch S_c is closed, setting the comparator input offset to zero.

CONVERSION

When a conversion command is received, switch S_1 is opened to trap a charge on the MSB capacitor proportional to the analog input level at the time of the sampling command, and switch S_c is opened to float the comparator input. The charge trapped in the capacitor array can now be moved between the three capacitors in the array by connecting switches S_1, S_2, and S_3 to positions "R" (to connect to the reference) or "G" (to connect to GND), thus changing the voltage generated at the comparator input.

During the first approximation, the MSB capacitor is connected through switch S_1 to the reference, while switches S_2 and S_3 are connected to GND. Depending on whether the comparator output is HIGH or LOW, the logic will then latch S_1 in position "R" or "G". Similarly, the second approximation is made by connecting S_2 to the reference and S_3 to GND, and latching S_2 according to the output of the comparator. After three successive approximation steps have been made the voltage level at the comparator will be within 1/2LSB of GND, and a digital word which represents the analog input can be determined from the positions of S_1, S_2 and S_3.

OPERATION

BASIC OPERATION

Figure 2 shows the minimum connections required to operate the ADS774 in a basic ±10V range in the Control Mode (discussed in detail in a later section.) The falling edge of a Convert Command (a pulse taking pin 5 LOW for a minimum of 25ns) both switches the ADS774 input to the hold state and initiates the conversion. Pin 28 (STATUS) will output a HIGH during the conversion, and falls only after the conversion is completed and the data has been latched on the data output pins (pins 16 to 27.) Thus, the falling edge of STATUS on pin 28 can be used to read the data from the conversion. Also, during conversion, the STATUS signal puts the data output pins in a High-Z state and inhibits the input lines. This means that pulses on pin 5 are ignored, so that new conversions cannot be initiated during the conversion, either as a result of spurious signals or to short-cycle the ADS774.

The ADS774 will begin acquiring a new sample as soon as the conversion is completed, even before the STATUS output falls, and will track the input signal until the next conversion is started. The ADS774 is designed to complete a conversion and accurately acquire a new signal in 8.5µs max over the full operating temperature range, so that conversions can take place at a full 117kHz.

CONTROLLING THE ADS774

The Burr-Brown ADS774 can be easily interfaced to most microprocessor systems and other digital systems. The microprocessor may take full control of each conversion, or the converter may operate in a stand-alone mode, controlled only by the R/$\overline{C}$ input. Full control consists of selecting an 8- or 12-bit conversion cycle, initiating the conversion, and reading the output data when ready—choosing either 12 bits all at once, or the 8 MSB bits followed by the 4 LSB bits in a left-justified format. The five control inputs (12/$\overline{8}$, $\overline{CS}$, A_0, R/$\overline{C}$, and CE) are all TTL/CMOS-compatible. The functions of the control inputs are described in Table II. The control function truth table is shown in Table III.

STAND-ALONE OPERATION

For stand-alone operation, control of the converter is accomplished by a single control line connected to R/$\overline{C}$. In this mode $\overline{CS}$ and A_0 are connected to digital common and CE and 12/$\overline{8}$ are connected to +5V. The output data are

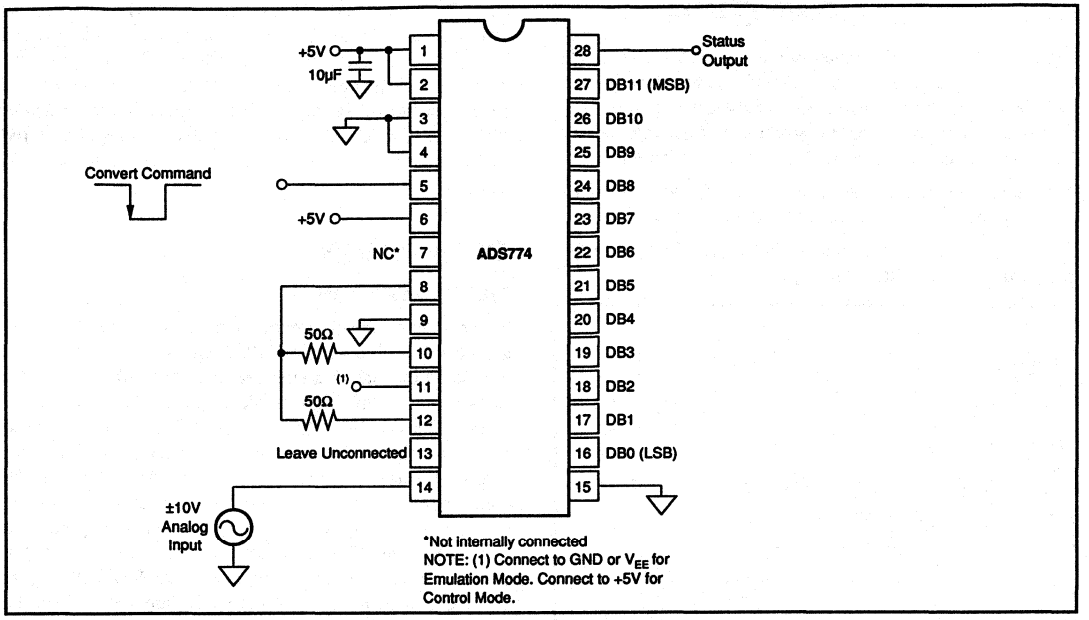


FIGURE 2. Basic ±10V Operation.

presented as 12-bit words. The stand-alone mode is used in systems containing dedicated input ports which do not require full bus interface capability.

Conversion is initiated by a HIGH-to-LOW transition of R/$\overline{C}$. The three-state data output buffers are enabled when R/$\overline{C}$ is HIGH and STATUS is LOW. Thus, there are two possible modes of operation; data can be read with either a positive pulse on R/$\overline{C}$, or a negative pulse on STATUS. In either case the R/$\overline{C}$ pulse must remain LOW for a minimum of 25ns.

Figure 3 illustrates timing with an R/$\overline{C}$ pulse which goes LOW and returns HIGH during the conversion. In this case, the three-state outputs go to the high-impedance state in response to the falling edge of R/$\overline{C}$ and are enabled for external access of the data after completion of the conversion.

Figure 4 illustrates the timing when a positive R/$\overline{C}$ pulse is used. In this mode the output data from the previous conversion is enabled during the time R/$\overline{C}$ is HIGH. A new conversion is started on the falling edge of R/$\overline{C}$, and the three-state outputs return to the high-impedance state until the next occurrence of a HIGH R/$\overline{C}$ pulse. Timing specifications for stand-alone operation are listed in Table IV.

FULLY CONTROLLED OPERATION

Conversion Length

Conversion length (8-bit or 12-bit) is determined by the state of the A_0 input, which is latched upon receipt of a conversion start transition (described below). If A_0 is latched HIGH, the conversion continues for 8 bits. The full 12-bit conversion will occur if A_0 is LOW. If all 12 bits are read following an 8-bit conversion, the 4LSBs (DB0-DB3) will be LOW (logic 0). A_0 is latched because it is also involved in enabling the output buffers. No other control inputs are latched.

CONVERSION START

The converter initiates a conversion based on a transition occurring on any of three logic inputs ($\overline{CE}$, $\overline{CS}$, and R/$\overline{C}$) as shown in Table III. Conversion is initiated by the last of the three to reach the required state and thus all three may be dynamically controlled. If necessary, all three may change state simultaneously, and the nominal delay time is the same regardless of which input actually starts the conversion. If it is desired that a particular input establish the actual start of conversion, the other two should be stable a minimum of 50ns prior to the transition of the critical input. Timing relationships for start of conversion timing are illustrated in Figure 5. The specifications for timing are contained in Table V.

The STATUS output indicates the current state of the converter by being in a high state only during conversion. During this time the three state output buffers remain in a high-impedance state, and therefore data cannot be read during conversion. During this period additional transitions of the three digital inputs which control conversion will be ignored, so that conversion cannot be prematurely terminated or restarted. However, if A_0 changes state after the beginning of conversion, any additional start conversion transition will latch the new state of A_0, possibly resulting in an incorrect conversion length (8 bits vs 12 bits) for that conversion.

Binary (BIN) Output		Input Voltage Range and LSB Values			
Analog Input Voltage Range	Defined As:	±10V	±5V	0V to +10V	0V to +20V
One Least Significant Bit (LSB)	$\frac{FSR}{2^n}$	$\frac{20V}{2^n}$	$\frac{10V}{2^n}$	$\frac{10V}{2^n}$	$\frac{20V}{2^n}$
	n = 8	78.13mV	39.06mV	39.06mV	78.13mV
	n = 12	4.88mV	2.44mV	2.44mV	4.88mV
Output Transition Values					
FFE_H to FFF_H	+ Full-Scale Calibration	+10V – 3/2LSB	+5V – 3/2LSB	+10V – 3/2LSB	+20V – 3/2LSB
$7FFF_H$ to 800_H	Midscale Calibration (Bipolar Offset)	0V – 1/2LSB	0V – 1/2LSB	+5V – 1/2LSB	+10V – 1/2LSB
000_H to 001_H	Zero Calibration (– Full-Scale Calibration)	–10V + 1/2LSB	–5V + 1/2LSB	0V +1/2LSB	0V +1/2LSB

TABLE I. Input Voltages, Transition Values, and LSB Values.

DESIGNATION	DEFINITION	FUNCTION
CE (Pin 6)	Chip Enable (active high)	Must be HIGH ("1") to either initiate a conversion or read output data. 0-1 edge may be used to initiate a conversion.
$\overline{CS}$ (Pin 3)	Chip Select (active low)	Must be LOW ("0") to either initiate a conversion or read output data. 1-0 edge may be used to initiate a conversion.
R/$\overline{C}$ (Pin 5)	Read/Convert ("1" = read) ("0" = convert)	Must be LOW ("0") to initiate either 8- or 12-bit conversions. 1-0 edge may be used to initiate a conversion. Must be HIGH ("1") to read output data. 0-1 edge may be used to initiate a read operation.
A_0 (Pin 4)	Byte Address Short Cycle	In the start-convert mode, A_0 selects 8-bit (A_0 = "1") or 12-bit (A_0 = "0") conversion mode. When reading output data in two 8-bit bytes, A_0 = "0" accesses 8 MSBs (high byte) and A_0 = "1" accesses 4 LSBs and trailing "0s" (low byte).
12/$\overline{8}$ (Pin 2)	Data Mode Select ("1" = 12 bits) ("0" = 8 bits)	When reading output data, 12/$\overline{8}$ = "1" enables all 12 output bits simultaneously. 12/$\overline{8}$ = "0" will enable the MSBs or LSBs as determined by the A_0 line.

TABLE II. Control Line Functions.

CE	$\overline{CS}$	R/$\overline{C}$	12/$\overline{8}$	A_0	OPERATION
0	X	X	X	X	None
X	1	X	X	X	None
↑	0	0	X	0	Initiate 12-bit conversion
↑	0	0	X	1	Initiate 8-bit conversion
1	↓	0	X	0	Initiate 12-bit conversion
1	↓	0	X	1	Initiate 8-bit conversion
1	0	↓	X	0	Initiate 12-bit conversion
1	0	↓	X	1	Initiate 8-bit conversion
1	0	1	1	X	Enable 12-bit output
1	0	1	0	0	Enable 8 MSBs only
1	0	1	0	1	Enable 4 LSBs plus 4 trailing zeroes

TABLE III. Control Input Truth Table.

READING OUTPUT DATA

After conversion is initiated, the output data buffers remain in a high-impedance state until the following four logic conditions are simultaneously met: R/$\overline{C}$ HIGH, STATUS LOW, CE HIGH, and $\overline{CS}$ LOW. Upon satisfaction of these conditions the data lines are enabled according to the state of inputs 12/$\overline{8}$ and A_0. See Figure 6 and Table V for timing relationships and specifications.

In most applications the 12/$\overline{8}$ input will be hard-wired in either the HIGH or LOW condition, although it is fully TTL and CMOS-compatible and may be actively driven if desired. When 12/$\overline{8}$ is HIGH, all 12 output lines (DB0-DB11) are enabled simultaneously for full data word transfer to a 12-bit or 16-bit bus. In this situation the A_0 state is ignored when reading the data.

When 12/$\overline{8}$ is LOW, the data is presented in the form of two 8-bit bytes, with selection of the byte of interest accomplished by the state of A_0 during the read cycle. When A_0 is LOW, the byte addressed contains the 8MSBs. When A_0 is HIGH, the byte addressed contains the 4LSBs from the conversion followed by four logic zeros which have been forced by the control logic. The left-justified formats of the two 8-bit bytes are shown in Figure 7. Connection of the ADS774 to an 8-bit bus for transfer of the data is illustrated in Figure 8. The design of the ADS774 guarantees that the A_0 input may be toggled at any time with no damage to the converter; the outputs which are tied together in Figure 8 cannot be enabled at the same time. The A_0 input is usually driven by the least significant bit of the address bus, allowing storage of the output data word in two consecutive memory locations.

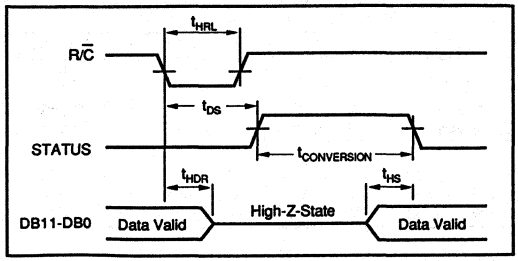


FIGURE 3. R/$\overline{C}$ Pulse Low—Outputs Enabled After Conversion.

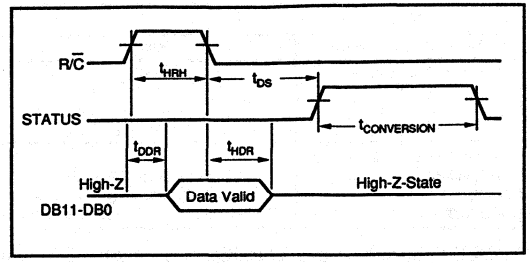


FIGURE 4. R/$\overline{C}$ Pulse High — Outputs Enabled Only While R/$\overline{C}$ Is High.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
t_{HRL}	Low R/$\overline{C}$ Pulse Width	25			ns
t_{DS}	STS Delay from R/$\overline{C}$			200	ns
t_{HDR}	Data Valid After R/$\overline{C}$ Low	25			ns
t_{HRH}	High R/$\overline{C}$ Pulse Width	100			ns
t_{DDR}	Data Access Time			150	ns

TABLE IV. Stand-Alone Mode Timing. ($T_A = T_{MIN}$ to T_{MAX}).

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
Convert Mode					
t_{DSC}	STS delay from CE		60	200	ns
t_{HEC}	$\overline{CE}$ Pulse width	50	30		ns
t_{SSC}	$\overline{CS}$ to CE setup	50	20		ns
t_{HSC}	$\overline{CS}$ low during CE high	50	20		ns
t_{SRC}	R/$\overline{C}$ to CE setup	50	0		ns
t_{HRC}	R/$\overline{C}$ low during CE high	50	20		ns
t_{SAC}	A_0 to CE setup	0			ns
t_{HAC}	A_0 valid during CE high	50	20		ns
Read Mode					
t_{DD}	Access time from CE		75	150	ns
t_{HD}	Data valid after CE low	25	35		ns
t_{HL}	Output float delay		100	150	ns
t_{SSR}	$\overline{CS}$ to CE setup	50	0		ns
t_{SRR}	R/$\overline{C}$ to CE setup	0			ns
t_{SAR}	A_0 to CE setup	50	25		ns
t_{HSR}	$\overline{CS}$ valid after CE low	0			ns
t_{HRR}	R/$\overline{C}$ high after CE low	0			ns
t_{HAR}	A_0 valid after CE low	50			ns
t_{HS}	STATUS delay after data valid	75	150	375	ns

TABLE V. Timing Specifications, Fully Controlled Operation. ($T_A = T_{MIN}$ to T_{MAX}).

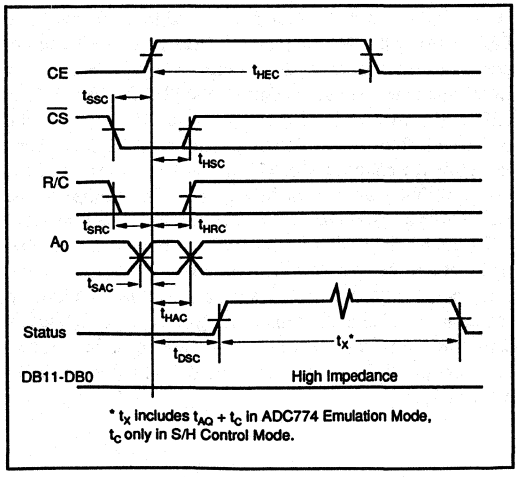


FIGURE 5. Conversion Cycle Timing.

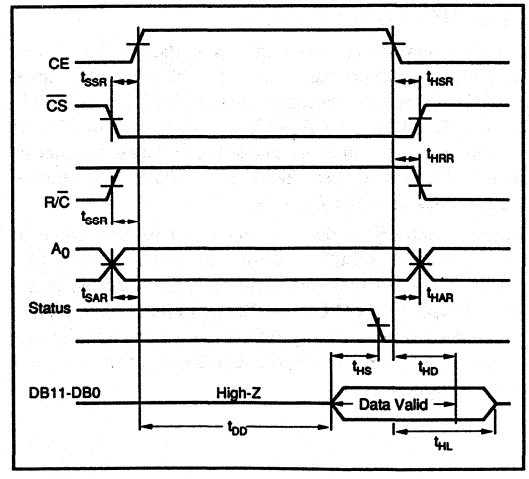


FIGURE 6. Read Cycle Timing.

	Word 1								Word 2							
Processor	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Converter	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	0	0	0	0

FIGURE 7. 12-Bit Data Format for 8-Bit Systems.

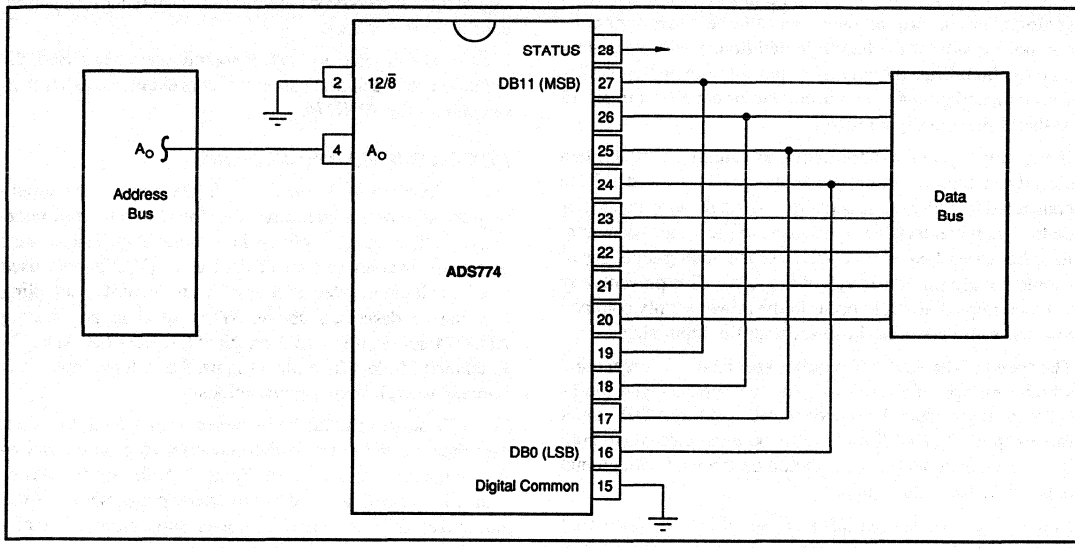


FIGURE 8. Connection to an 8-Bit Bus.

S/H CONTROL MODE AND ADC774 EMULATION MODE

The Emulation Mode allows the ADS774 to be dropped into most existing ADC774 sockets without changes to other system hardware or software. In existing sockets, the analog input is held stable during the conversion period so that accurate conversions can proceed, but the input can change rapidly at any time before the conversion starts. The Emulation Mode uses the stability of the analog input during the conversion period to both acquire and convert in a maximum of 8µs (8.5µs over temperature.) In fact, system throughput can be increased, since the input to the ADS774 can start slewing before the end of a conversion (after the acquisition time), which is not possible with existing ADC774s.

The Control Mode is provided to allow full use of the internal sample/hold, eliminating the need for an external sample/hold in most applications. As compared with systems using separate sample/hold and A/D, the ADS774 in the Control Mode also eliminates the need for one of the control signals, usually the convert command. The command that puts the internal sample/hold in the hold state also initiates a conversion, reducing timing constraints in many systems.

The basic difference between these two modes is the assumptions about the state of the input signal both before and during the conversion. The differences are shown in Figure 9 and Table VI. In the Control Mode, it is assumed that during the required 1.4µs acquisition time the signal is not changing faster than the ADS774 can track. No assumption is made about the input level after the convert command arrives, since the input signal is sampled and conversion begins immediately after the convert command. This means that a convert command can also be used to switch an input multiplexer or change gains on a programmable gain amplifier, allowing the input signal to settle before the next acquisition at the end of the conversion. Because aperture jitter is minimized in the Control Mode, a high input frequency can be converted without an external sample/hold.

In the Emulation Mode, a delay time is introduced between the convert command and the start of conversion to allow the ADS774 enough time to acquire the input signal before converting. This increases the effective aperture delay time from 0.02µs to 1.6µs, but allows the ADS774 to replace the ADC774 in most circuits without additional changes. In designs where the input to the ADS774 is changing rapidly in the 200ns prior to a convert command, system performance may be enhanced by delaying the convert command by 200ns.

When using the ADS774 in the Emulation Mode to replace existing converters in current designs, a sample/hold amplifier often precedes the converter. In these cases, no additional delay in the convert command will be needed. The existing sample/hold will not be slewing excessively when going from the sample mode to the hold mode prior to a conversion.

In both modes, as soon as the conversion is completed the internal sample/hold circuit immediately begins slewing to track the input signal.

INSTALLATION

LAYOUT PRECAUTIONS

Analog (pin 9) and digital (pin 15) commons are not connected together internally in the ADS774, but should be connected together as close to the unit as possible and to an analog common ground plane beneath the converter on the component side of the board. In addition, a wide conductor pattern should run directly from pin 9 to the analog supply common, and a separate wide conductor pattern from pin 15 to the digital supply common.

If the single-point system common cannot be established directly at the converter, pin 9 and pin 15 should still be connected together at the converter. A single wide conductor pattern then connects these two pins to the system common. In either case, the common return of the analog input signal should be referenced to pin 9 of the ADC. This prevents any voltage drops that might occur in the power supply common returns from appearing in series with the input signal.

The speed of the ADS774 requires special caution regarding whichever input pin is unused. For 10V input ranges, pin 14 (20V Range) must be unconnected, and for 20V input ranges, pin 13 (10V Range) must be unconnected. In both cases, the unconnected input should be shielded with ground plane to reduce noise pickup.

In particular, the unused input pin should not be connected to any capacitive load, including high impedance switches. Even a few pF on the unused pin can degrade acquisition time.

Coupling between analog input and digital lines should be minimized by careful layout. For instance, if the lines must cross, they should do so at right angles. Parallel analog and digital lines should be separated from each other by a pattern connected to common.

If external full scale and offset potentiometers are used, the potentiometers and associated resistors should be as close as possible to the ADS774.

POWER SUPPLY DECOUPLING

On the ADS774, +5V (to Pin 1) is the only power supply required for correct operation. Pin 7 is not connected internally, so there is no problem in existing ADC774 sockets where this is connected to +15V. Pin 11 (V_{EE}) is only used as a logic input to select modes of control over the sampling function as described above. When used in an existing ADC774 socket, the –15V on pin 11 selects the ADC774 Emulation Mode. Since pin 11 is used as a logic input, it is immune to typical supply variations.

The +5V supply should be bypassed with a 10µF tantalum capacitor located close to the converter to promote noise-free operations, as shown in Figure 2. Noise on the power supply lines can degrade the converter's performance. Noise and spikes from a switching power supply are especially troublesome.

		S/H CONTROL MODE (Pin 11 Connected to +5V)			ADC774 EMULATION MODE (Pin 11 Connected to 0V to –15V)			
SYMBOL	PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
$t_{AQ} + t_C$	Throughput Time:							
	12-bit Conversions		8	8.5		8	8.5	µs
	8-bit Conversions		6	6.3		6	6.3	µs
t_C	Conversion Time:							
	12-bit Conversions		6.4			6.4		µs
	8-bit Conversions		4.4			4.4		µs
t_{AQ}	Acquisition Time		1.4			1.4		µs
t_A	Aperture Delay		20			1600		ns
t_J	Aperture Uncertainty		0.3			10		ns

TABLE VI. Conversion Timing, T_{MIN} to T_{MAX}.

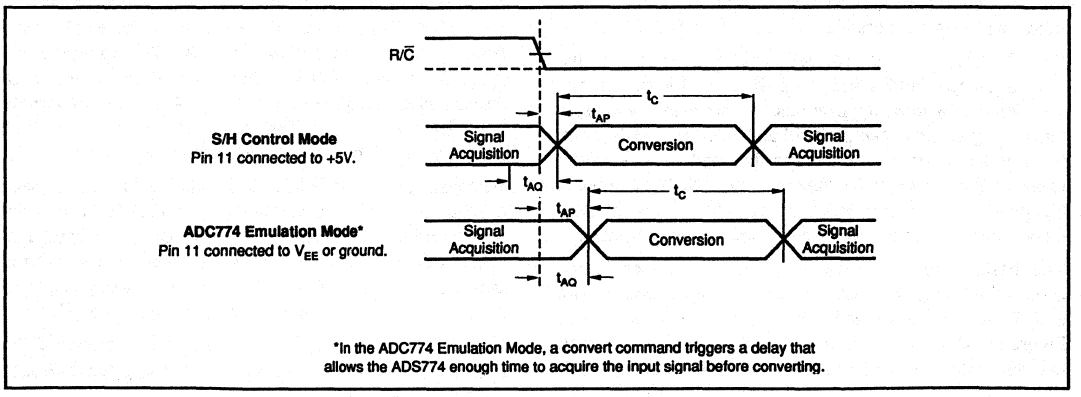


FIGURE 9. Signal Acquisition and Conversion Timing.

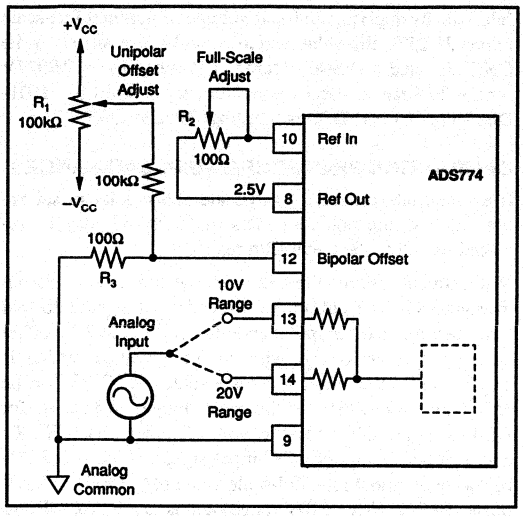


FIGURE 10. Unipolar Configuration.

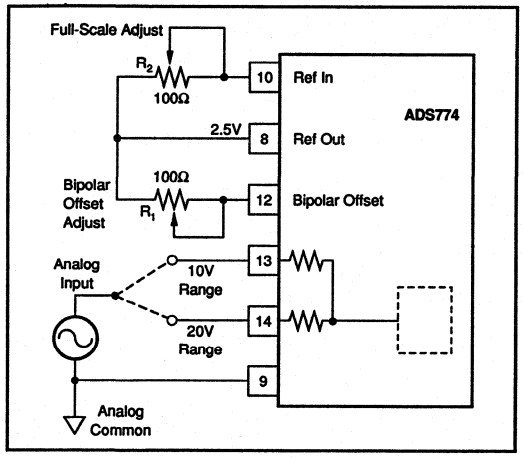


FIGURE 11. Bipolar Configuration.

RANGE CONNECTIONS

The ADS774 offers four standard input ranges: 0V to +10V, 0V to +20V, ±5V, or ±10V. Figures 10 and 11 show the necessary connections for each of these ranges, along with the optional gain and offset trim circuits. If a 10V input range is required, the analog input signal should be connected to pin 13 of the converter. A signal requiring a 20V range is connected to pin 14. In either case the other pin of the two is left unconnected. Pin 12 (Bipolar Offset) is connected either to Pin 9 (Analog Common) for unipolar operation, or to Pin 8 (2.5V Ref Out), or the external reference, for bipolar operation. Full-scale and offset adjustments are described below.

The input impedance of the ADS774 is typically 50kΩ in the 20V ranges and 12kΩ in the 10V ranges. This is significantly higher than that of traditional ADC774 architectures, reducing the load on the input source in most applications.

INPUT STRUCTURE

Figure 12 shows the resistor divider input structure of the ADS774. Since the input is driving a capacitor in the CDAC during acquisition, the input is looking into a high impedance node as compared with traditional ADC774 architectures, where the resistor divider network looks into a comparator input node at virtual ground.

To understand how this circuit works, it is necessary to know that the input range on the internal sampling capacitor is from 0V to +3.33V, and the analog input to the ADS774 must be converted to this range. Unipolar 20V range can be used as an example of how the divider network functions. In 20V operation, the analog input goes into pin 14. Pin 13 is left unconnected and pin 12 is connected, through 50Ω, to analog common. From Figure 12, it is clear that the input to the capacitor array will be the analog input voltage on pin 14 divided by the resistor network (42kΩ + 42kΩ || 10.5kΩ). A 20V input at pin 14 is divided to 3.33V at the capacitor array, while a 0V input at pin 14 gives 0V at the capacitor array.

The main effect of the 10kΩ internal resistor on pin 12 is to provide the same offset adjust response as that of traditional ADC774 architectures without changing the external trimpot values.

SINGLE SUPPLY OPERATION

The ADS774 is designed to operate from a single +5V supply, and handle all of the unipolar and bipolar input ranges, in either the Control Mode or the Emulation Mode as described above. Pin 7 is not connected internally. This is where +12V or +15V is supplied on traditional ADC774s. Pin 11, the –12V or –15V supply input on traditional ADC774s, is used only as a logic input on the ADS774. There is a resistor divider internally on pin 11 to reduce that input to a correct logic level within the ADS774, and this resistor will add 10mW to 15mW to the power consumption of the ADS774 when –15V is supplied to pin 11. To minimize power consumption in a system, pin 11 can be

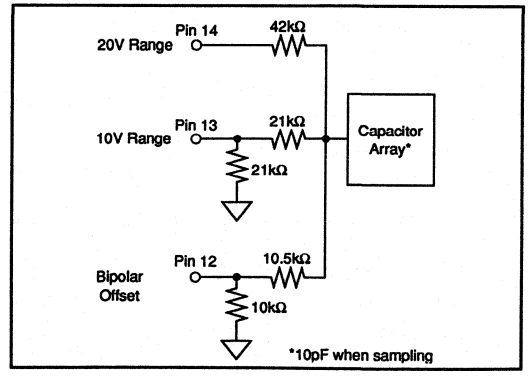


FIGURE 12. ADS774 Input Structure.

simply grounded (for Emulation Mode) or tied to +5V (for Control Mode.)

There are no other modifications required for the ADS774 to function with a single +5V supply.

CALIBRATION

OPTIONAL EXTERNAL FULL-SCALE AND OFFSET ADJUSTMENTS

Offset and full-scale errors may be trimmed to zero using external offset and full-scale trim potentiometers connected to the ADS774 as shown in Figures 10 and 11 for unipolar and bipolar operation.

CALIBRATION PROCEDURE— UNIPOLAR RANGES

If external adjustments of full-scale and offset are not required, replace R_2 in Figure 10 with a 50Ω 1% metal film resistor and connect pin 12 to pin 9, omitting the other adjustment components.

If adjustment is required, connect the converter as shown in Figure 10. Sweep the input through the end-point transition voltage (0V + 1/2LSB; +1.22mV for the 10V range, +2.44mV for the 20V range) that causes the output code to be DB0 ON (HIGH). Adjust potentiometer R_1 until DB0 is alternately toggling ON and OFF with all other bits OFF. Then adjust full scale by applying an input voltage of nominal full-scale minus 3/2LSB, the value which should cause all bits to be ON. This value is +9.9963V for the 10V range and +19.9927V for the 20V range. Adjust potentiometer R_2 until bits DB1-DB11 are ON and DB0 is toggling ON and OFF.

CALIBRATION PROCEDURE—BIPOLAR RANGES

If external adjustments of full-scale and bipolar offset are not required, the potentiometers in Figure 11 may be replaced by 50Ω, 1% metal film resistors.

If adjustments are required, connect the converter as shown in Figure 11. The calibration procedure is similar to that described above for unipolar operation, except that the offset adjustment is performed with an input voltage which is 1/2LSB above the minus full-scale value (–4.9988V for the ±5V range, –9.9976V for the ±10V range). Adjust R_1 for DB0 to toggle ON and OFF with all other bits OFF. To adjust full-scale, apply a DC input signal which is 3/2LSB below the nominal plus full-scale value (+4.9963V for ±5V range, +9.9927V for ±10V range) and adjust R_2 for DB0 to toggle ON and OFF with all other bits ON.

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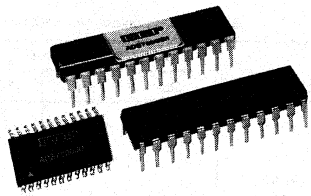


ADS7800

AVAILABLE IN DIE

12-Bit 3µs Sampling ANALOG-TO-DIGITAL CONVERTER

FEATURES

- 333k SAMPLES PER SECOND
- STANDARD ±10V AND ±5V INPUT RANGES
- DC PERFORMANCE OVER TEMP:
  No Missing Codes
  1/2LSB Integral Linearity Error
  3/4LSB Differential Linearity Error
- AC PERFORMANCE OVER TEMP:
  72dB Signal-to-Noise Ratio
  80dB Spurious-free Dynamic Range
  –80dB Total Harmonic Distortion
- INTERNAL SAMPLE/HOLD, REFERENCE, CLOCK, AND 3-STATE OUTPUTS
- POWER DISSIPATION: 215mW max
- PACKAGE: 24-Pin Single-wide DIP
  24-Lead SOIC

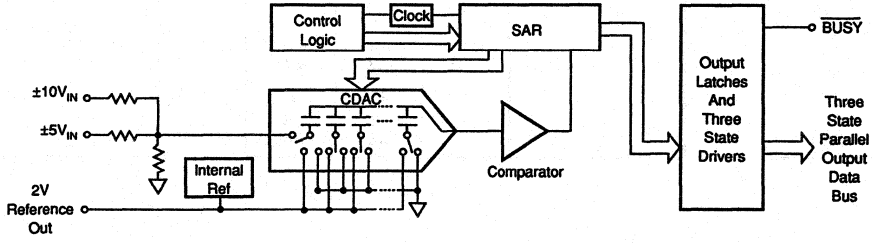
DESCRIPTION

The ADS7800 is a complete 12-bit sampling A/D converter using state-of-the-art CMOS structures. It contains a complete 12-bit successive approximation A/D converter with internal sample/hold, reference, clock, digital interface for microprocessor control, and three-state output drivers.

The ADS7800 is specified at a 333kHz sampling rate. Conversion time is factory set for 2.70µs max over temperature, and the high speed sampling input stage insures a total acquisition and conversion time of 3µs max over temperature. Precision, laser-trimmed scaling resistors provide industry-standard input ranges of ±5V or ±10V.

AC and DC performance are completely specified. Two grades based on linearity and dynamic performance are available to provide the optimum price/performance fit in a wide range of applications.

The 24-pin ADS7800 is available in plastic and side-braze hermetic 0.3" wide DIPs, and in an SOIC package. It operates from a +5V supply and either a –12V or –15V supply. The ADS7800 is available in grades specified over 0°C to +70°C and –40°C to +85°C temperature ranges.



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Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL

$T_A = T_{MIN}$ to T_{MAX}, Sampling Frequency, f_S, = 333kHz, $-V_S = -15V$, $V_S = +5V$, unless otherwise specified.

PARAMETER	CONDITIONS	ADS7800JP/JU/AH/D			ADS7800KP/KU/BH			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
RESOLUTION				12			•	Bits
ANALOG INPUT								
Voltage Ranges			±10V/±5V			•		V
Impedance	±10V Range	4.4	6.3	8.1	•	•	•	kΩ
	±5V Range	2.9	4.2	5.4	•	•	•	kΩ
THROUGHPUT SPEED								
Conversion Time	Conversion Alone		2.5	2.7		•	•	µs
Complete Cycle	Acquisition + Conversion		2.6	3.0		•	•	µs
Throughput Rate		333	380		•	•		kHz
DC ACCURACY								
Full Scale Error [1]				±0.50			±0.35	%
Full Scale Error Drift			6			•		ppm/°C
Integral Linearity Error				±1			±1/2	LSB[2]
Differential Linearity Error				±1			±3/4	LSB
No Missing Codes			Guaranteed			Guaranteed		
Bipolar Zero [1]				±4			±2	LSB
Bipolar Zero Drift			1			•		ppm/°C
Power Supply Sensitivity								
	$-16.5V < -V_S < -13.5V$			±1/2			•	LSB
	$-12.6V < -V_S < -11.4V$			±1/2			•	LSB
	$+4.75V < V_S < +5.25V$			±1			±1/2	LSB
Transition Noise [3]			0.1			•		LSB
AC ACCURACY								
Spurious-Free Dynamic Range	f_{IN} = 47kHz	74	77		77	80		dB [4]
Total Harmonic Distortion	f_{IN} = 47kHz		–77	–74		–80	–77	dB
Two-tone Intermodulation Distortion	f_{IN1} = 24.4kHz (–6dB) f_{IN2} = 28.5kHz (–6dB)		–77	–74		–80	–77	dB
Signal to (Noise + Distortion) Ratio	f_{IN} = 47kHz	67	70		69	72		dB
Signal to Noise Ratio (SNR)	f_{IN} = 47kHz	68	71		70	73		dB
SAMPLING DYNAMICS								
Aperture Delay			13			•		ns
Aperture Jitter			150			•		ps,rms
Transient Response [5]			130			•		ns
Overvoltage Recovery [6]			150			•		ns
INTERNAL REFERENCE VOLTAGE								
Voltage		1.9	2.0	2.1	•	•	•	V
Source Current Available for External Loads			10			•		µA
DIGITAL INPUTS								
Logic Levels								
V_{IL}		–0.3		+0.8	•		•	V
V_{IH}		+2.4		+5.3	•		•	V
I_{IL}		–5			•			µA
I_{IH}		+5			•			µA
DIGITAL OUTPUTS								
Data Format				Parallel, 12-bit or 8-bit/4-bit				
Data Coding				Binary Offset Binary				
V_{OL}	I_{SINK} = 1.6mA	0.0		+0.4	•		•	V
V_{OH}	I_{SOURCE} = 500µA	+2.4		+5.0	•		•	V
$I_{LEAKAGE}$ (High-Z State)			±0.1	±5		•	•	µA
POWER SUPPLIES								
Rated Voltage								
$-V_S$		–11.4	–15	–16.5	•	•	•	V
V_S (V_{SA} and V_{SD})		+4.75	+5.0	+5.25	•	•	•	V
Current								
$-I_S$			3.5	6		•	•	mA
I_S			18	25		•	•	mA
Power Consumption			135	215		•	•	mW

SPECIFICATIONS (CONT)

ELECTRICAL

$T_A = T_{MIN}$ to T_{MAX}, Sampling Frequency, f_S, = 333kHz, $-V_S = -15V$, $V_S = +5V$, unless otherwise specified.

PARAMETER	CONDITIONS	ADS7800JP/JU/AH/D			ADS7800KP/KU/BH			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
TEMPERATURE RANGE								
Specification	JP/JU/KP/KU/D	0		+70	*		*	°C
	AH/BH	–40		+85	*		*	°C
Operating	JP/KP/JU/KU/D	–40		+85	*		*	°C
Storage		–65		+150	*		*	°C

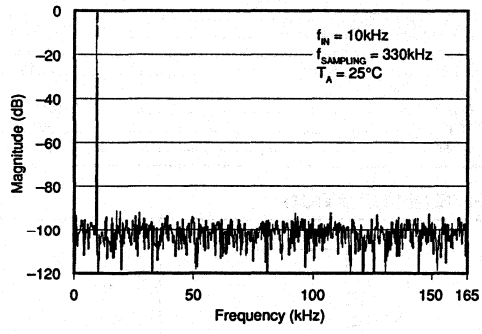
* Same as specification for ADS7800JP/JU/AH.

NOTES: (1) Adjustable to zero with external potentiometer. (2) LSB means Least Significant Bit. For ADS7800, 1LSB = 2.44mV for the ±5V range, 1LSB = 4.88mV for the ±10V range. (3) Noise was characterized over temperature near full scale, 0V, and negative full scale. 0.1LSB represents a typical rms level of noise at the worst case, which was near full scale input at +125°C. (4) All specifications in dB are referred to a full-scale input, either ±10V or ±5V. (5) For full-scale step input, 12-bit accuracy attained in specified time. (6) Recovers to specified performance in specified time after 2 x F_S input overvoltage.

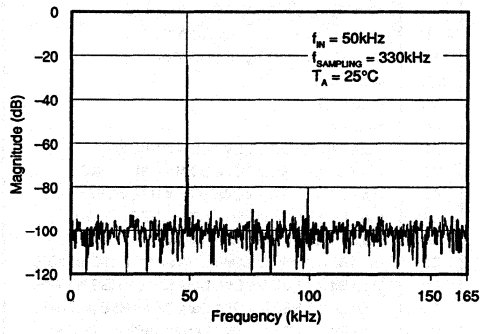
TYPICAL PERFORMANCE CURVES

$+V_S = +5V$, $-V_S = -15V$, and $T_A = +25°C$, unless otherwise noted. All plots use 1024 point FFTs.

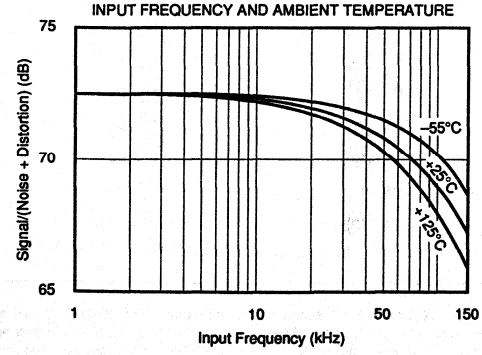
FREQUENCY SPECTRUM (10kHz f_{IN})



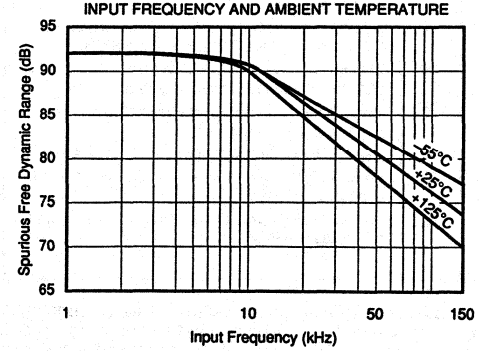
FREQUENCY SPECTRUM (50kHz f_{IN})



SIGNAL/(NOISE + DISTORTION) vs INPUT FREQUENCY AND AMBIENT TEMPERATURE



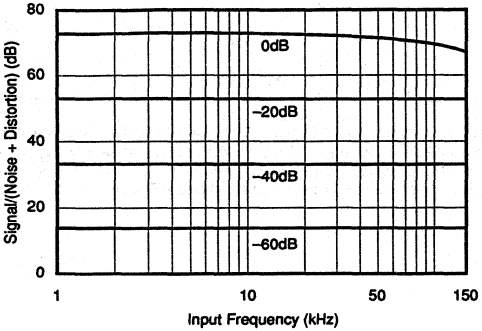
SPURIOUS FREE DYNAMIC RANGE vs INPUT FREQUENCY AND AMBIENT TEMPERATURE



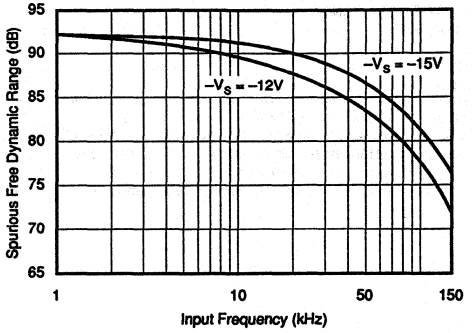
TYPICAL PERFORMANCE CURVES (CONT)

$+V_S$ = +5V, $-V_S$ = –15V, and T_A = +25°C, unless otherwise noted. All plots use 1024 point FFTs.

SIGNAL/(NOISE + DISTORTION) vs FREQUENCY AND AMPLITUDE



SPURIOUS FREE DYNAMIC RANGE vs INPUT FREQUENCY AND NEGATIVE SUPPLY VOLTAGE



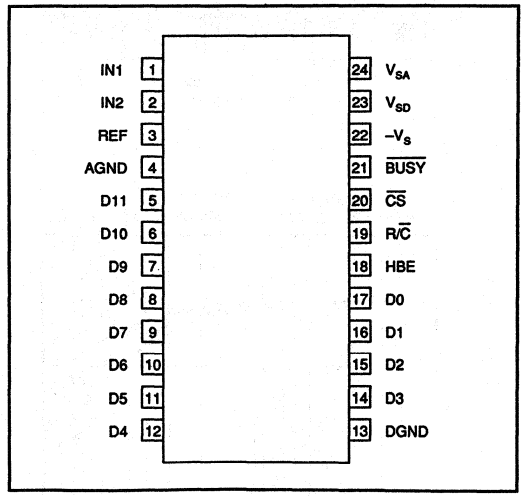
PIN ASSIGNMENTS

PIN #	NAME	DESCRIPTION
1	IN1	±10V Analog Input. Connected to GND for ±5V range.
2	IN2	±5V Analog Input. Connected to GND for ±10V range.
3	REF	+2V Reference Output. Bypass to GND with 22µF to 47µF Tantalum. Buffer for external loads.
4	AGND	Analog Ground. Connect to pin 13.
5	D11	Data Bit 11. Most Significant Bit (MSB).
6	D10	Data Bit 10.
7	D9	Data Bit 9.
8	D8	Data Bit 8.
9	D7	Data Bit 7 if HBE is LOW; LOW if HBE is HIGH.
10	D6	Data Bit 6 if HBE is LOW; LOW if HBE is HIGH.
11	D5	Data Bit 5 if HBE is LOW; LOW if HBE is HIGH.
12	D4	Data Bit 4 if HBE is LOW; LOW if HBE is HIGH.
13	DGND	Digital Ground. Connect to pin 4.
14	D3	Data Bit 3 if HBE is LOW; Data Bit 11 if HBE is HIGH.
15	D2	Data Bit 2 if HBE is LOW; Data Bit 10 if HBE is HIGH.
16	D1	Data Bit 1 if HBE is LOW; Data Bit 9 if HBE is HIGH.
17	D0	Data Bit 0 if HBE is LOW. Least Significant Bit (LSB); Data Bit 8 if HBE is HIGH.
18	HBE	High Byte Enable. When held LOW, data output as 12-bits in parallel. When held HIGH, four MSBs presented on pins 14-17, pins 9-12 output LOWs. Must be LOW to initiate conversion.
19	R/$\overline{C}$	Read/Convert. Falling edge initiates conversion when $\overline{CS}$ is LOW, HBE is LOW, and $\overline{BUSY}$ is HIGH.
20	$\overline{CS}$	Chip Select. Outputs in Hi-Z state when HIGH. Must be LOW to initiate conversion or read data.
21	$\overline{BUSY}$	Busy. Output LOW during conversion. Data valid on rising edge in Convert Mode.
22	$-V_S$	Negative Power Supply. –12V or –15V. Bypass to GND.
23	V_{SD}	Positive Digital Power Supply. +5V. Connect to pin 24, and bypass to GND.
24	V_{SA}	Positive Analog Power Supply. +5V. Connect to pin 23, and bypass to GND.

ABSOLUTE MAXIMUM RATINGS

$-V_S$ to ANALOG COMMON	–16.5V
V_S to DIGITAL COMMON	+7V
Pin 23 (V_{SD}) to Pin 24 (V_{SA})	±0.3V
ANALOG COMMON to DIGITAL COMMON	±1V
Control Inputs to DIGITAL COMMON	–0.3 to V_S + 0.3V
Analog Input Voltage	±20V
Maximum Junction Temperature	160°C
Internal Power Dissipation	750mW
Lead Temperature (soldering, 10s)	+300°C
Thermal Resistance, θ_{JA}:	
Plastic DIP	100°C/W
SOIC	100°C/W
Ceramic	50°C/W

PIN CONFIGURATION



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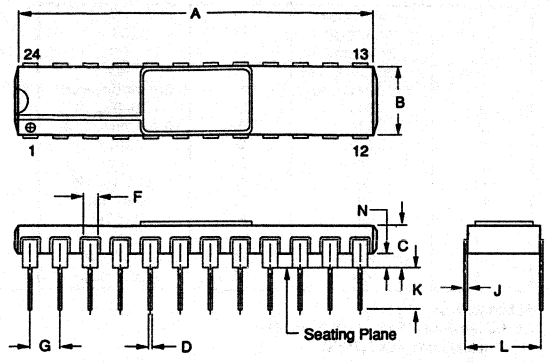
MECHANICAL

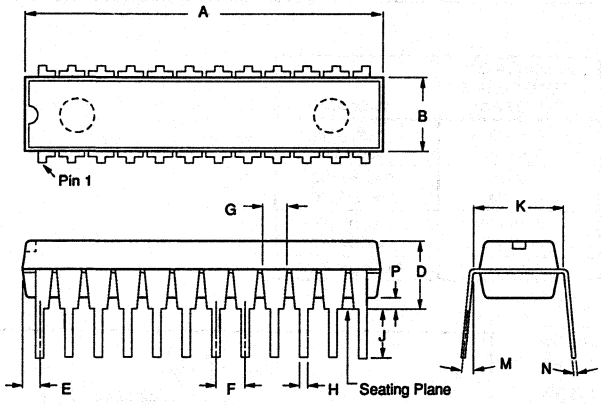
H Package — 24-Pin Side Braze Ceramic



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.188	1.212	30.18	30.78
B	.300	.320	7.62	8.13
C	—	.160	—	4.06
D	.016	.020	0.41	0.51
F	.050 TYP		1.27 TYP	
G	.095	.105	2.41	2.67
J	.009	.012	0.23	0.31
K	.170 BASIC		4.32 BASIC	
L	.290	.310	7.37	7.87
N	.040	.060	1.02	1.52

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.

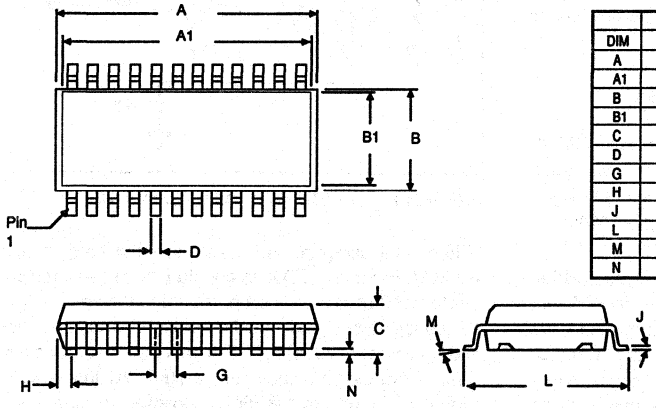
P Package — 24-Pin Plastic DIP



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.125	1.255	28.58	31.88
B	.250	.290	6.35	7.37
D	.150	.170	3.81	4.32
E	.010	.080	.25	2.03
F	.100 BASIC		2.54 BASIC	
G	.050	.070	1.27	1.78
H	.016	.025	0.41	0.64
J	.125		3.18	
K	.300 BASIC		7.63 BASIC	
M	0°	15°	0°	15°
N	.008	.015	0.20	0.38
P	.010	.030	.25	.76

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

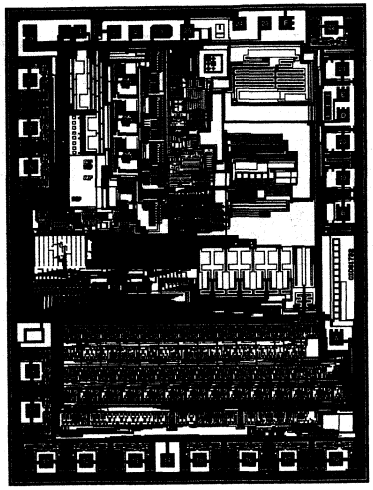
U Package—24-Pin SOIC



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.602	.618	15.29	15.70
A1	.595	.618	15.11	15.70
B	.286	.302	7.26	7.67
B1	.270	.285	6.86	7.24
C	.093	.108	2.36	2.74
D	.015	.019	0.38	0.48
G	.050 BASIC		1.27 BASIC	
H	.026	.034	0.66	0.86
J	.008	.012	0.20	0.30
L	.390	.422	9.91	10.72
M	0°	10°	0°	10°
N	.000	.012	0.00	0.30

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.

DICE INFORMATION



PAD	FUNCTION	PAD	FUNCTION
1	±10V Range	16	D2
2	±5V Range	17	D1
3	Reference	18	D0
4	Analog Gnd Sense	A	NC
5	Analog Ground	B	Bipolar/Unipolar
6	D11	19	Hi Bite
7	D10	20	Read/Convert Not
8	D9	D	NC
9	D8	E	NC
10	D7	21	Chip Select Not
11	D6	22	Busy Not
12	D5	F	Flag Tie
13	D4	23	–15
14	Digital Ground	24	+5V Digital
15	D3	25	+5V Analog

Substrate Bias: $+V_s$
Die Dimensions: 136 x 181 mils (±5mils)
Die Thickness: 20 mils (±3mils)
Metalization: Aluminum

ADS7800 DIE TOPOGRAPHY

ORDERING INFORMATION

MODEL	INTEGRAL LINEARITY ERROR (LSB)	SIGNAL-TO-(NOISE+DISTORTION) RATIO (dB min)	SPECIFICATION TEMPERATURE RANGE (°C)	PACKAGE
ADS7800JP	±1	67	0 to +70	Plastic DIP
ADS7800KP	±1/2	69	0 to +70	Plastic DIP
ADS7800JU	±1	67	0 to +70	Plastic SOIC
ADS7800KU	±1/2	69	0 to +70	Plastic SOIC
ADS7800AH	±1	67	–40 to +85	Ceramic DIP
ADS7800BH	±1/2	69	–40 to +85	Ceramic DIP
ADS7800D	±1	67	0 to +70	25 Die per Pack

CAUTION

The ADS7800 is an ESD (electrostatic discharge) sensitive device. The digital control inputs have a special FET structure, which turns on when the input exceeds the supply by 18V, to minimize ESD damage. However, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. When not in use, devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

THEORY OF OPERATION

The ADS7800 combines the advantages of advanced CMOS technology (logic density, stable capacitors, and good analog switches) with Burr-Brown's proven skills in laser-trimmed thin-film resistors to provide a complete sampling analog-to-digital converter.

A basic charge-redistribution successive approximation architecture converts analog input voltages into digital words. Figure 1 shows the operation of a simplified three bit charge redistribution A-to-D. Precision laser-trimmed scaling resistors at the input divide standard input ranges (±10V or ±5V for the ADS7800) into levels compatible with the CMOS characteristics of the internal capacitor array.

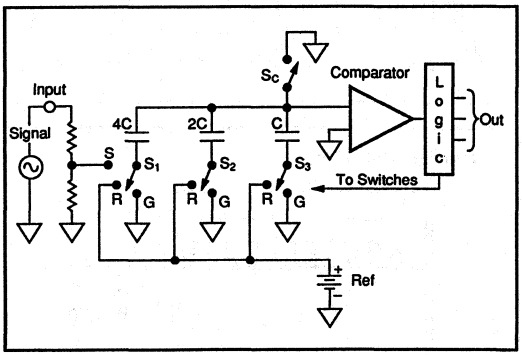


FIGURE 1. 3-Bit Charge Redistribution A-to-D.

While in the sampling mode, the capacitor array switch for the MSB capacitor (S_1) is in position "S", so that the charge on the MSB capacitor is proportional to the voltage level of the analog input signal, and the remaining array switches (S_2 and S_3) are set to position "R" to provide an accurate bipolar offset from the reference source REF. At the same time, switch S_c is also in the closed position to auto-zero any offset errors in the CMOS comparator.

When a convert command is received, switch S_1 is opened to trap a charge on the MSB capacitor proportional to the input level at the time of the sampling command, switches S_2 and S_3 are opened to trap an offset charge, and switch S_C is opened to float the comparator input. The charge trapped on the capacitor array can now be moved between the three capacitors in the array by connecting switches S_1, S_2 and S_3 to positions "R" (to connect to REF) or "G" (to connect to GND) successively, changing the voltage generated at the comparator input node.

The first approximation connects the MSB capacitor via switch S_1 to REF, while switches S_2 and S_3 are connected to GND. Depending on whether the comparator output is HIGH or LOW, the logic will then latch S_1 in position "R" or "G", and moves on to make the next approximation by connecting S_2 to REF and S_3 to GND. When the three successive approximation steps are made for this simple converter, the voltage level at the comparator will be within 1/2LSB of GND, and the data output word will be based on reading the positions of S_1, S_2 and S_3.

OPERATION

BASIC OPERATION

Figure 2 shows the simple hookup circuit required to operate the ADS7800 in a ±10V range in the Convert Mode. A convert command arriving on pin 19, R/$\overline{C}$, (a pulse taking pin 19 LOW for a minimum of 40ns) puts the ADS7800 in the hold mode, and a conversion is started. Pin 21, $\overline{BUSY}$, will be held LOW during the conversion, and rises only after the conversion is completed and the data has been transferred to the output latches. Thus, the rising edge of the signal on pin 21 can be used to read the data from the conversion. Also, during conversion, the $\overline{BUSY}$ signal puts the output data lines in Hi-Z states and inhibits input lines. This means that pulses on pin 19 are ignored, so that new conversions cannot be initiated during a conversion, either as a result of spurious signals or to short-cycle the ADS7800.

In the Read Mode, the input to pin 19 is kept normally LOW, and a HIGH pulse is used to read data and initiate a conversion. In this mode, the rising edge of R/$\overline{C}$ on pin 19 will enable the output data pins, and the data from the previous conversion becomes valid. The falling edge then puts the ADS7800 in a hold mode, and initiates a new conversion.

The ADS7800 will begin acquiring a new sample as soon as the conversion is completed, even before the $\overline{BUSY}$ output rises on pin 21, and will track the input signal until the next conversion is started, whether in the Convert Mode or the Read Mode.

For use with an 8-bit bus, the data can be read out in two bytes under the control of pin 18, HBE. With a LOW input on pin 18, at the end of a conversion, the 8 LSBs of data are loaded into the latches on pins 9 through 12 and 14 through 17. Taking pin 18 HIGH then loads the 4 MSBs on pins 14 through 17, with pins 9 through 12 being forced LOW.

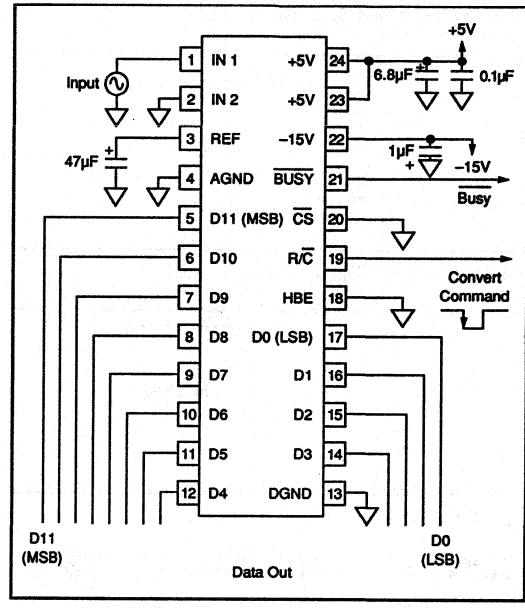


FIGURE 2. Basic ±10V Operation.

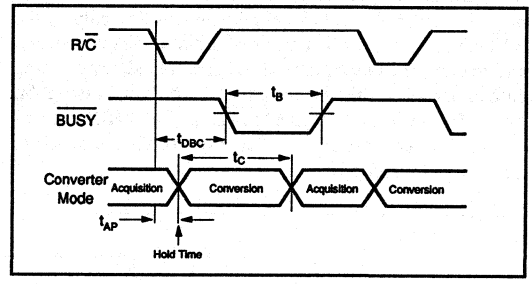


FIGURE 3. Acquisition and Conversion Timing.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
t_{DBC}	$\overline{BUSY}$ delay from R/$\overline{C}$		80	150	ns
t_B	$\overline{BUSY}$ Low		2.5	2.7	µs
t_{AP}	Aperture Delay		13		ns
Δt_{AP}	Aperture Jitter		150		ps, rms
t_C	Conversion Time		2.47	2.70	µs

TABLE I. Acquisition and Conversion Timing.

ANALOG INPUT RANGES

The ADS7800 offers two standard bipolar input ranges: ±10V and ±5V. If a ±10V range is required, the analog input signal should be connected to pin 1. A signal requiring a ±5V range should be connected to pin 2. In either case, the other pin of the two must be grounded or connected to the adjustment circuits described in the section on calibration. (See Figures 4 and 5, or 10 and 11.)

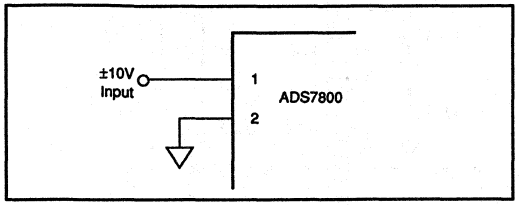


FIGURE 4. ±10V Range Without Trims.

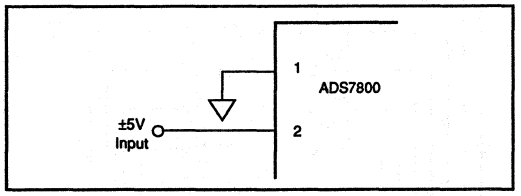


FIGURE 5. ±5V Range Without Trims.

CONTROLLING THE ADS7800

The ADS7800 can be easily interfaced to most microprocessor-based and other digital systems. The microprocessor may take full control of each conversion, or the ADS7800 may operate in a stand-alone mode, controlled only by the R/$\overline{C}$ input. Full control consists of initiating the conversion and reading the output data at user command, transmitting data either all 12-bits in one parallel word, or in two 8-bit bytes. The three control inputs ($\overline{CS}$, R/$\overline{C}$ and HBE) are all TTL/CMOS compatible. The functions of the control lines are shown in Table II.

$\overline{CS}$	R/$\overline{C}$	HBE	$\overline{BUSY}$	OPERATION
1	X	X	1	None - Outputs In Hi-Z State.
0	1↓0	0	1	Holds Signal and Initiates Conversion.
0	1	0	1	Output Three-State Buffers Enabled once Conversion has Finished.
0	1	1	1	Enable HI-Byte in 8-bit Bus Mode.
0	1↓0	1	1	Inhibit Start of Conversion.
0	0	1	1	None - Outputs In Hi-Z State.
X	X	X	0	Conversion In Progress. Outputs HI-Z State. New Conversion Inhibited until Present Conversion has Finished.

TABLE II. Control Line Functions.

For stand-alone operation, control of the ADS7800 is accomplished by a single control line connected to R/$\overline{C}$. In this mode, $\overline{CS}$ and HBE are connected to GND. The output data are presented as 12-bit words. The stand-alone mode is used in systems containing dedicated input ports which do not require full bus interface capability.

Conversion is initiated by a HIGH-to-LOW transition on R/$\overline{C}$. The three-state data output buffers are enabled when R/$\overline{C}$ is HIGH and $\overline{BUSY}$ is HIGH. Thus, there are two possible modes of operation: conversion can be initiated with either positive or negative pulses. In either case, the R/$\overline{C}$ pulse must remain LOW a minimum of 40ns.

Figure 6 illustrates timing when conversion is initiated by an R/$\overline{C}$ pulse which goes LOW and returns HIGH during the conversion. In this case (Convert Mode), the three-state outputs go into the Hi-Z state in response to the falling edge of R/$\overline{C}$, and are enabled for external access of the data after completion of the conversion.

Figure 7 illustrates the timing when conversion is initiated by a positive R/$\overline{C}$ pulse. In this mode (Read Mode), the output data from the previous conversion is enabled during the HIGH portion of R/$\overline{C}$. A new conversion starts on the falling edge of R/$\overline{C}$, and the three-state outputs return to the Hi-Z state until the next occurrence of a HIGH on R/$\overline{C}$.

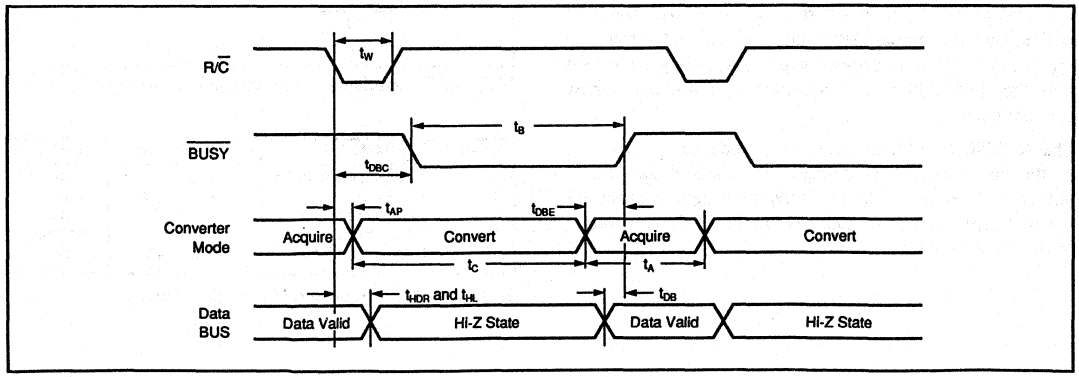


FIGURE 6. Convert Mode: R/$\overline{C}$ Pulse LOW — Outputs Enabled After Conversion.

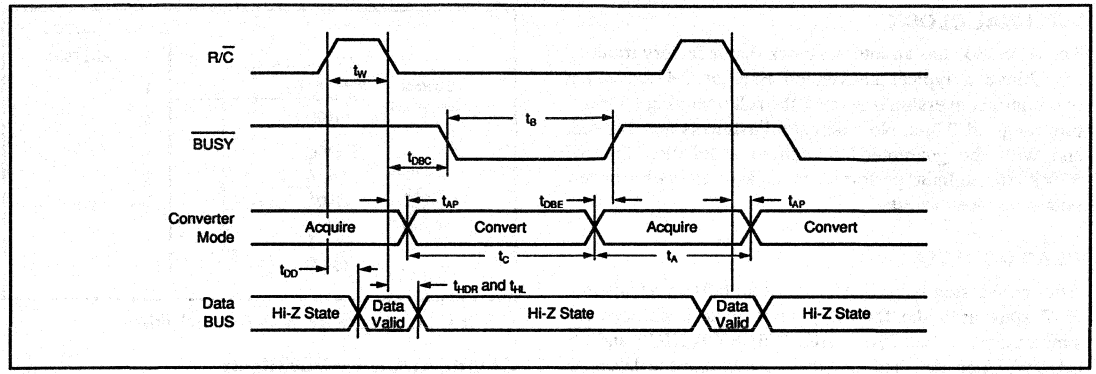


FIGURE 7. Read Mode: R/$\overline{C}$ Pulse HIGH— Outputs Enabled Only When R/$\overline{C}$ is High.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
t_W	R/$\overline{C}$ Pulse Width	40	10		ns
t_{DBC}	$\overline{BUSY}$ delay from R/$\overline{C}$		80	150	ns
t_B	$\overline{BUSY}$ LOW		2.5	2.7	µs
t_{AP}	Aperture Delay		13		ns
Δt_{AP}	Aperture Jitter		150		ps, rms
t_C	Conversion Time		2.47	2.70	µs
t_{DBE}	$\overline{BUSY}$ from End of Conversion		100		ns
t_{DB}	$\overline{BUSY}$ Delay after Data Valid	25	75	200	ns
t_A	Acquisition Time		130	300	ns
t_A+t_C	Throughput Time		2.6	3.0	µs
t_{HDR}	Valid Data Held After R/$\overline{C}$ LOW	20	50		ns
t_S	$\overline{CS}$ or HBE LOW before R/$\overline{C}$ Falls	25	5		ns
t_H	$\overline{CS}$ or HBE LOW after R/$\overline{C}$ Falls	25	0		ns
t_{DD}	Data Valid from $\overline{CS}$ LOW, R/$\overline{C}$ HIGH, and HBE in Desired State (Load = 100pF)		65	150	ns
t_{HDR}	Valid Data Held After R/$\overline{C}$ Low	20	50		ns
t_{HL}	Delay to Hi-Z State after R/$\overline{C}$ Falls or $\overline{CS}$ Rises (3kΩ Pullup or Pulldown)		50	150	ns

TABLE III. Timing Specifications (T_{MIN} to T_{MAX}).

CONVERSION START

A conversion is initiated on the ADS7800 only by a negative transition occurring on R/$\overline{C}$, as shown in Table I. No other combination of states or transitions will initiate a conversion. Conversion is inhibited if either $\overline{CS}$ or HBE are HIGH, or if $\overline{BUSY}$ is LOW. $\overline{CS}$ and HBE should be stable a minimum of 25ns prior to the transition on R/$\overline{C}$. Timing relationships for start of conversion are illustrated in Figure 8.

The $\overline{BUSY}$ output indicates the current state of the converter by being LOW only during conversion. During this time the three-state output buffers remain in a Hi-Z state, and therefore data cannot be read during conversion. During this period, additional transitions on the three digital inputs ($\overline{CS}$, R/$\overline{C}$ and HBE) will be ignored, so that conversion cannot be prematurely terminated or restarted.

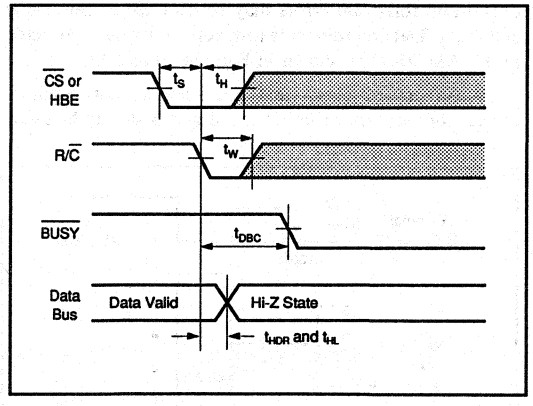


FIGURE 8. Conversion Start Timing.

INTERNAL CLOCK

The ADS7800 has an internal clock that is factory trimmed to achieve a typical conversion time of 2.47µs, and a maximum conversion time over the full operating temperature range of 2.7µs. No external adjustments are required, and with the guaranteed maximum acquisition time of 300ns, throughput performance is assured with convert pulses as close as 3µs.

READING DATA

After conversion is initiated, the output buffers remain in a Hi-Z state until the following three logic conditions are simultaneously met: R/$\overline{C}$ is HIGH, $\overline{BUSY}$ is HIGH and $\overline{CS}$ is LOW. Upon satisfaction of these conditions, the data lines are enabled according to the state of HBE. See Figure 9 and Table III for timing relationships and specifications.

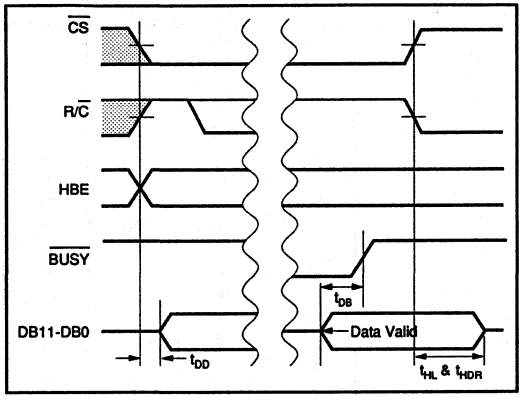


FIGURE 9. Read Cycle Timing.

CALIBRATION

OPTIONAL EXTERNAL GAIN AND OFFSET TRIM

Offset and full-scale errors may be trimmed to zero using external offset and full-scale trim potentiometers connected to the ADS7800 as shown in Figures 10 and 11.

If adjustment of offset and full scale is not required, connections as shown in Figures 4 and 5 should be used.

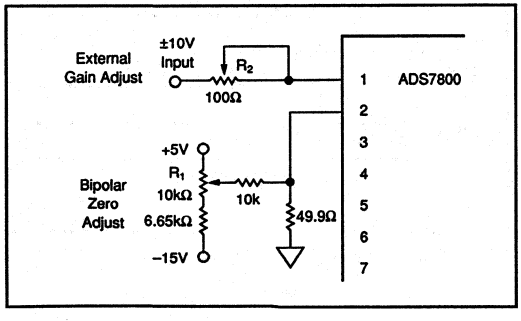


FIGURE 10. ±10V Range With External Trims.

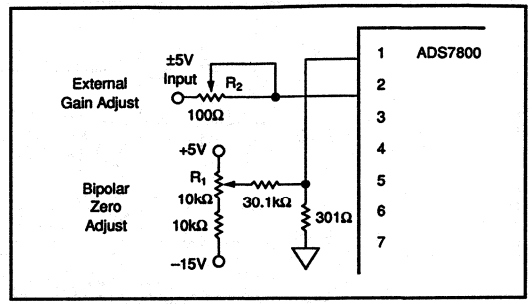


FIGURE 11. ±5V Range With External Trims.

CALIBRATION PROCEDURE

First, trim offset, by applying at the input (pin 1 or 2) the mid-point transition voltage (–2.44mV for the ±10V range, –1.22mV for the ±5V range.) With the ADS7800 converting continually, adjust potentiometer R_1 until the MSB (D11 on pin 5) is toggling alternately HIGH and LOW.

Next adjust full scale, by applying at the input a DC input signal that is 3/2LSB below the nominal full scale voltage (+9.9927V for the ±10V range, +4.9963V for the ±5V range.) With the ADS7800 converting continually, adjust R_2 until the LSB (D0 on pin 17) is toggling HIGH and LOW with all of the other bits HIGH.

LAYOUT CONSIDERATIONS

Because of the high resolution and linearity of the ADS7800, system design problems such as ground path resistance and contact resistance become very important.

ANALOG SIGNAL SOURCE IMPEDANCE

The input resistance of the ADS7800 is 6.3kΩ or 4.2kΩ (for the ±10V and ±5V ranges respectively.) To avoid introducing distortion, the source resistance must be very low, or constant with signal level. The output impedance provided by most op amps is ideal.

Pins 23 (V_{SD}) and 24 (V_{SA}) are not connected internally on the ADS7800, to maximize accuracy on the chip. They should be connected together as close as possible to the unit. Pin 24 may be slightly more sensitive than pin 23 to supply variations, but to maintain maximum system accuracy, both should be well isolated from digital supplies with wide load variations.

To limit the effects of digital switching elsewhere in a system on the analog performance of the system, it often makes sense to run a separate +5V supply conductor from the supply regulator to any analog components requiring +5V, including the ADS7800.

The V_S pins (23 and 24) should be connected together and bypassed with a parallel combination of a 6.8µF tantalum capacitor and a 0.1µF ceramic capacitor located close to the converter to obtain noise-free operation. (See Figure 2.) The $-V_S$ pin 22 should be bypassed with a 1µF tantalum capacitor, again as close as possible to the ADS7800.

Noise on the power supply lines can degrade converter performance, especially noise and spikes from a switching power supply. Appropriate supplies or filters must be used.

The GND pins (4 and 13) are also separated internally, and should be directly connected to a ground plane under the converter if at all possible. A ground plane is usually the best solution for preserving dynamic performance and reducing noise coupling into sensitive converter circuits. Where any compromises must be made, the common return of the analog input signal should be referenced to pin 4, AGND, on the ADS7800, which prevents any voltage drops that might occur in the power supply common returns from appearing in series with the input signal.

Coupling between analog input and digital lines should be minimized by careful layout. For instance, if the lines must cross, they should do so at right angles. Parallel analog and digital lines should be separated from each other by a pattern connected to common.

If external full scale and offset potentiometers are used, the potentiometers and related resistors should be located as close to the ADS7800 as possible.

REFERENCE BYPASS

Pin 3 (REF) should be bypassed with a 22µF to 47µF tantalum capacitor. A rated working voltage of 2V or more is acceptable here. This pin is used to enhance the system accuracy of the internal reference circuit, and is not recommended for driving external signals. If there are important system reasons for using the ADS7800 reference externally, the output of pin 3 must be appropriately buffered.

"HOT SOCKET" PRECAUTION

Two separate +5V V_S pins, 23 and 24, are used to minimize noise caused by digital transients. If one pin is powered and the other is not, the ADS7800 may "Latch Up" and draw excessive current. In normal operation, this is not a problem because both pins will be soldered together. However, during evaluation, incoming inspection, repair, etc., where the potential of a "Hot Socket" exists, care should be taken to power the ADS7800 only after it has been socketed.

MINIMIZING "GLITCHES"

Coupling of external transients into an analog-to-digital converter can cause errors which are difficult to debug. In addition to the discussions earlier on layout considerations for supplies, bypassing and grounding, there are several other useful steps that can be taken to get the best analog performance out of a system using the ADS7800. These potential system problem sources are particularly important to consider when developing a new system, and looking for the causes of errors in breadboards.

First, care should be taken to avoid glitches during critical times in the sampling and conversion process. Since the ADS7800 has an internal sample/hold function, the signal that puts it into the hold state (R/$\overline{C}$ going LOW) is critical, as it would be on any sample/hold amplifier. The R/$\overline{C}$ falling edge should be sharp and have minimal ringing, especially during the 20ns after it falls.

Although not normally required, it is also good practice to avoid glitching the ADS7800 while bit decisions are being made. Since the above discussion calls for a fast, clean rise and fall on R/$\overline{C}$, it makes sense to keep the rising edge of the convert pulse outside the time when bit decisions are being made. In other words, the convert pulse should either be short (under 100ns so that it transitions before the MSB decision), or relatively long (over 2.75µs to transition after the LSB decision).

Next, although the data outputs are forced into a Hi-Z state during conversion, fast bus transients can still be capacitively coupled into the ADS7800. If the data bus experiences fast transients during conversion, these transients can be attenuated by adding a logic buffer to the data outputs. The $\overline{BUSY}$ output can be used to enable the buffer.

Naturally, transients on the analog input signal are to be avoided, especially at times within ±20ns of R/$\overline{C}$ going LOW, when they may be trapped as part of the charge on the capacitor array. This requires careful layout of the circuit in front of the ADS7800.

Finally, in multiplexed systems, the timing on when the multiplexer is switched may affect the analog performance of the system. In most applications, the multiplexer can be switched as soon as R/$\overline{C}$ goes LOW (with appropriate delays), but this may affect the conversion if the switched signal shows glitches or significant ringing at the ADS7800 input. Whenever possible, it is safer to wait until the conversion is completed before switching the multiplexer. The extremely fast acquisition time and conversion time of the ADS7800 make this practical in many applications.

INPUT VOLTAGE RANGE AND LSB VALUES			
Input Voltage Range Defined As:		±10V	±5V
Analog Input Connected to Pin		1	2
Pin Connected to GND		2	1
One Least Significant Bit (LSB)	$FSR/2^{12}$	$20V/2^{12}$	$10V/2^{12}$
		4.88mV	2.44mV
OUTPUT TRANSITION VALUES			
FFE_H to FFF_H	+Full Scale	+10V–3/2LSB	+5V–3/2LSB
		+9.9927V	+4.9963V
$7FF_H$ to 800_H	Mid Scale	0V–1/2LSB	0V–1/2LSB
	(Bipolar Zero)	–2.44mV	–1.22mV
000_H to 001_H	–Full Scale	–10V+1/2LSB	–5V+1/2LSB
		–9.9976V	–4.9988V

TABLE IV. Input Voltages, Transition Values, and LSB Values.

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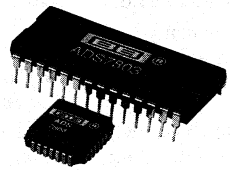


ADS7803

Autocalibrating, 4-Channel, 12-Bit ANALOG-TO-DIGITAL CONVERTER

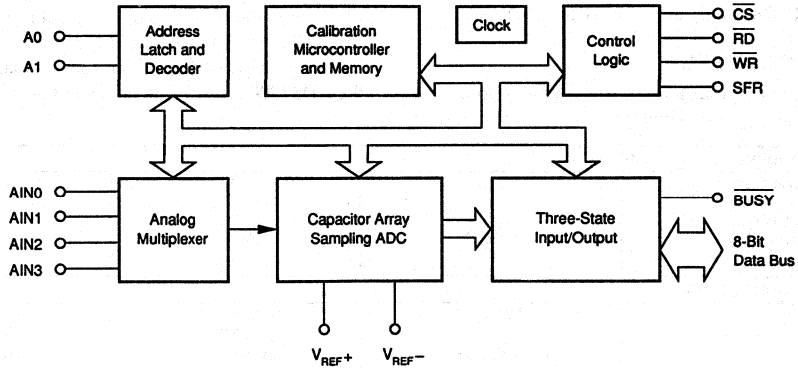
FEATURES

- LOW POWER: 10mW plus Power Down
- SIGNAL-TO-(NOISE + DISTORTION) RATIO OVER TEMPERATURE:
  69dB min with f_{IN} = 1kHz
  66dB min with f_{IN} = 50kHz
- FAST CONVERSION TIME: 8.5µs Including Acquisition (117kHz Sampling Rate)
- DC PERFORMANCE OVER TEMPERATURE:
  ±3/4 LSB max Total Error
  ±1/4 LSB max Channel Mismatch
- FOUR-CHANNEL INPUT MULTIPLEXER
- SINGLE SUPPLY: +5V
- PIN COMPATIBLE WITH ADC7802

DESCRIPTION

The ADS7803 is a monolithic CMOS 12-bit A/D converter with internal sample/hold and four-channel multiplexer. It is designed and tested for full dynamic performance with input signals to 50kHz. An autocalibration cycle guarantees a total unadjusted error within ±3/4LSB over the specified temperature range, eliminating the need for offset or gain adjustment. The 5V single-supply requirements and standard $\overline{CS}$, $\overline{RD}$, and $\overline{WR}$ control signals make the part easy to use in microprocessor applications. Conversion results are available in two bytes through an 8-bit three-state output bus.

The ADS7803 is available in a 28-pin plastic DIP and 28-lead PLCC, fully specified for operation over the industrial –40°C to +85°C temperature range.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL

$V_A = V_D = V_{REF}+ = 5V \pm 5\%$; $V_{REF}- = AGND = DGND = 0V$; CLK = 2MHz external, $T_A = -40°C$ to $+85°C$, after calibration cycle at any temperature; unless otherwise specified.

PARAMETER	CONDITIONS	ADS7803BP/ADS7803BN MIN	TYP	MAX	UNITS
RESOLUTION				12	Bits
ANALOG INPUT					
Voltage Input Range	$V_{REF}+ = 5V$, $V_{REF}- = 0V$	0		5	V
Input Capacitance			50		pF
On State Bias Current			100		nA
Off State Bias Current	$T_A = 25°C$			10	nA
	$T_A = -40°C$ to $+85°C$			100	nA
On Resistance Multiplexer			2		kΩ
Off Resistance Multiplexer			10		MΩ
Channel Separation	500Hz		92		dB
REFERENCE INPUT					
For Specified Performance: $V_{REF}+$	$V_{REF}+ \le V_A$		5		V
$V_{REF}-$			0		V
For Derated Performance: [1] $V_{REF}+$		2.5		V_A	V
$V_{REF}-$		0		1	V
Input Reference Current	$V_{REF}+ = 5V$, $V_{REF}- = 0V$		10	100	µA
THROUGHPUT TIMING					
Conversion Time With External Clock (Including	CLK = 2MHz			8.5	µs
Multiplexer Settling Time and Acquisition Time)	CLK = 1MHz			17	µs
	CLK = 500kHz			34	µs
With Internal Clock Using	$T_A = +25°C$			10	µs
Recommended Clock Components	$T_A = -40°C$ to $+85°C$		10		µs
Multiplexer Settling Time to 0.01%			460		ns
Multiplexer Access Time				20	ns
DC ACCURACY					
Total Error, All Channels[2]			±1/2	±3/4	LSB
Differential Nonlinearity			±1/4	±1/2	LSB
No Missing Codes			Guaranteed		
Gain Error	All Channels		±1/8	±1/4	LSB
Gain Error Drift	Between Calibration Cycles		±0.2		ppm/°C
Offset Error	All Channels		±1/8	±1/4	LSB
Offset Error Drift	Between Calibration Cycles		±0.2		ppm/°C
Channel-to-Channel Mismatch				±1/4	LSB
Power Supply Sensitivity	$V_A = V_D = 4.75V$ to $5.25V$		±1/8		LSB
AC ACCURACY					
Signal-to-(Noise + Distortion) Ratio	$f_{IN} = 1kHz$	69	71		dB
	$f_{IN} = 50kHz$	66	69		dB
Total Harmonic Distortion	$f_{IN} = 50kHz$		–75		dB
Signal-to-Noise Ratio	$f_{IN} = 50kHz$		70		dB
Spurious Free Dynamic Range	$f_{IN} = 1kHz$		90		dB
	$f_{IN} = 50kHz$		82		dB
SAMPLING DYNAMICS					
Full Power Bandwidth	–3dB		4		MHz
Aperture Delay	SFR D2 LOW		2500		ns
	SFR D2 HIGH		5		ns
Offset Error	SFR D2 LOW		±1/8	±1/4	LSB
	SFR D2 HIGH, Internal Clock or Sampling Command Synchronous to External Clock		±1/2	±1	LSB
	SFR D2 HIGH, Sampling Command Asynchronous to External Clock		±4		LSB
DIGITAL INPUTS					
All Pins Other Than CLK: V_{IL}				0.8	V
V_{IH}		2.4			V
Input Current	$T_A = +25°C$, $V_{IN} = 0$ to V_D			1	µA
	$T_A = -40°C$ to $+85°C$, $V_{IN} = 0$ to V_D			10	µA
CLK Input: V_{IL}				0.8	V
V_{IH}		3.5			V
I_{IL}				10	µA
I_{IH}				1.5	mA
I_{IH}	Power Down Mode (D3 in SFR HIGH)			100	nA

NOTES: (1) For $(V_{REF}+) - (V_{REF}-)$ as low as 2.5V, the total error will typically not exceed ±1LSB. (2) After calibration cycle, without external adjustment. Includes gain (full scale) error, offset error, integral nonlinearity, differential nonlinearity, and drift.

SPECIFICATIONS (CONT)

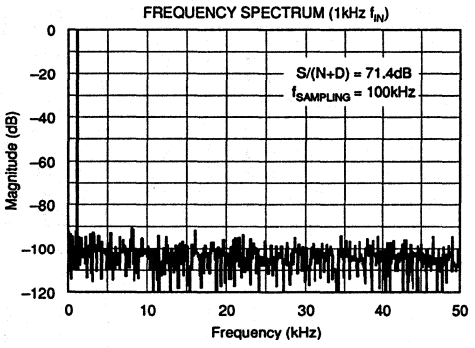
ELECTRICAL

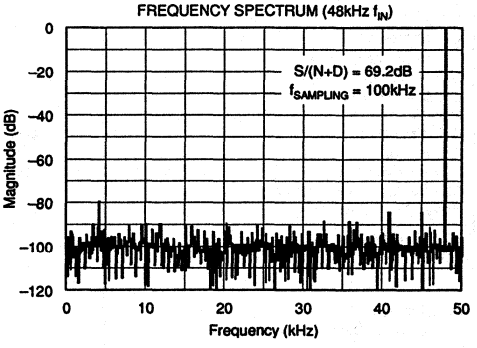
$V_A = V_D = V_{REF}+ = 5V \pm 5\%$; $V_{REF}- = AGND = DGND = 0V$; CLK = 2MHz external, $T_A = -40°C$ to $+85°C$, after calibration cycle at any temperature; unless otherwise specified.

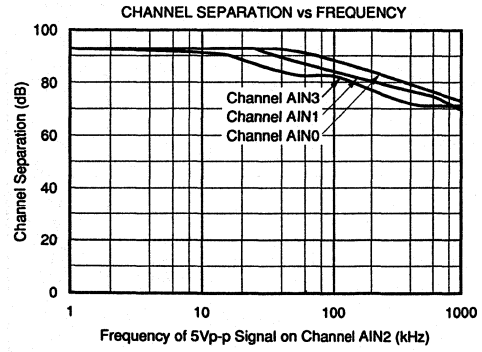
PARAMETER	CONDITIONS	ADS7803BP/ADS7803BN MIN	TYP	MAX	UNITS
DIGITAL OUTPUTS					
V_{OL}	$I_{SINK} = 1.6mA$			0.4	V
V_{OH}	$I_{SOURCE} = 200\mu A$	4			V
Leakage Current	High-Z State, $V_{OUT} = 0V$ to V_D			±1	µA
Output Capacitance	High-Z State		4	15	pF
POWER SUPPLIES					
Supply Voltage for Specified Performance: V_A		4.75	5	5.25	V
V_D	$V_A \geq V_D$	4.75	5	5.25	V
Supply Current: I_A			1	2.5	mA
I_D	Logic Input Pins HIGH or LOW		1	2	mA
Power Dissipation	$\overline{WR} = \overline{RD} = \overline{CS} = \overline{BUSY}$ = HIGH		10		mW
Power Down Mode	See Table III		50		µW
TEMPERATURE RANGE					
Specification		–40		+85	°C
Storage		–65		+150	°C

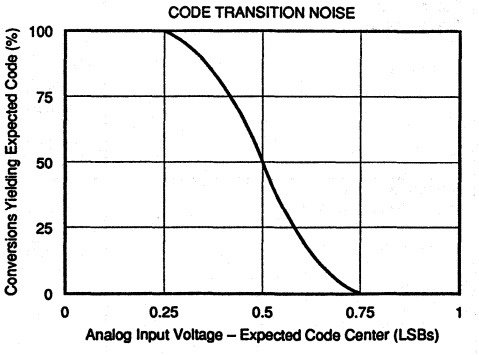
TYPICAL PERFORMANCE CURVES

$V_A = V_D = V_{REF}+ = 5V$, $V_{REF}- = AGND = 0V$, $T_A = +25°C$, dynamic performance based on 2048 point FFTs, unless otherwise specified.



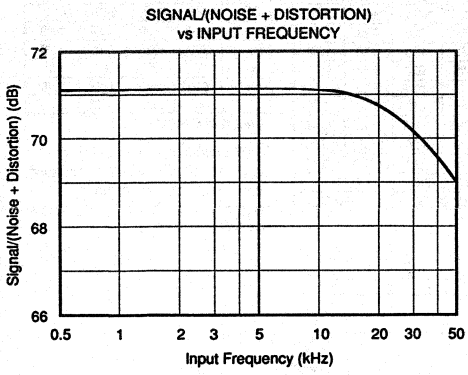


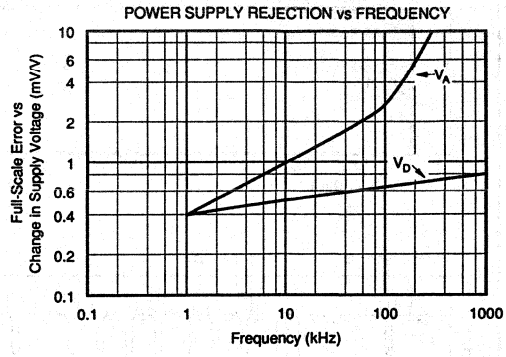


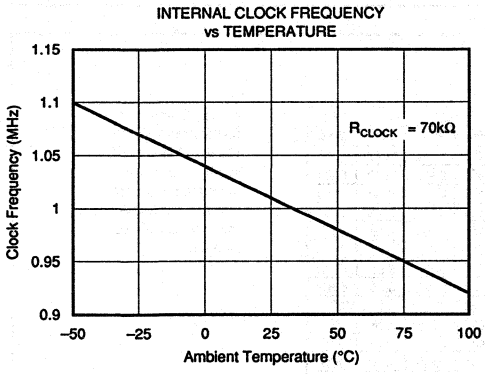


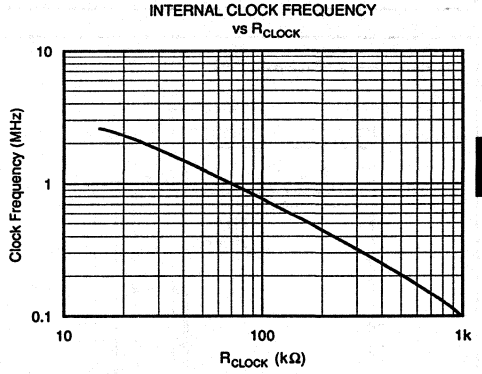
TYPICAL PERFORMANCE CURVES

$V_A = V_D = V_{REF}+ = 5V$, $V_{REF}- = AGND = 0V$, $T_A = +25°C$, dynamic performance based on 2048 point FFTs, unless otherwise specified.









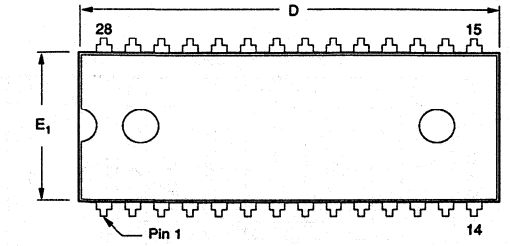
ORDERING INFORMATION

MODEL	MINIMUM SIGNAL-TO-(NOISE + DISTORTION) RATIO, dB	MAXIMUM TOTAL ERROR, LSB	SPECIFICATION TEMPERATURE RANGE, °C	PACKAGE
ADS7803BN	69	±3/4	–40 to +85	PLCC
ADS7803BP	69	±3/4	–40 to +85	Plastic DIP

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

MECHANICAL

P Package — 28-Pin Plastic DIP

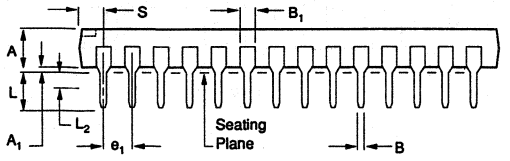


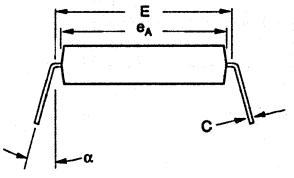
DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A(1)	.169	.200	4.29	5.08
A1(1)	.015	.070	0.38	1.78
B	.015	.020	0.38	0.51
B1	.015	.055	0.38	1.40
C	.008	.012	0.20	0.30
D(1)	1.380	1.455	35.05	36.96
E	.600	.625	15.24	15.88
E1(1)	.485	.550	12.32	13.97
e1	.100 BASIC		2.54 BASIC	
eA	.600 BASIC		15.24 BASIC	

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
L	.100	.200	2.54	5.08
L2	.000	.030	0.00	0.76
α	0°	15°	0°	15°
Q1	.020	.070	0.51	1.78
S1	.040	.080	1.02	2.03

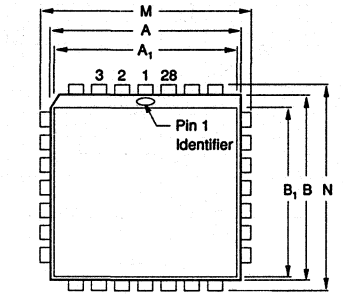
(1) Not JEDEC Standard.

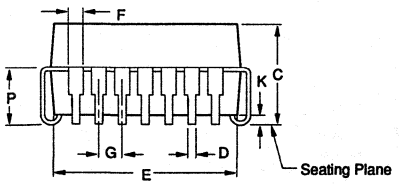
NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.





N Package — 28-Pin Plastic LCC





DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.450	0.460	11.43	11.68
A1	0.450	0.460	11.43	11.68
B	0.450	0.460	11.43	11.68
B1	0.450	0.460	11.43	11.68
C	0.165	0.180	4.19	4.57
D	0.013	0.023	0.33	0.58
E	0.390	0.430	9.91	10.92
F	0.026	0.032	0.66	0.81
G	0.050 BASIC		1.27 BASIC	
K	0.015	0.025	0.38	0.64
M	0.485	0.495	12.32	12.57
N	0.485	0.495	12.32	12.57
P	0.100	0.110	2.54	2.79

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.

ABSOLUTE MAXIMUM RATINGS

V_A to Analog Ground	6.5V
V_D to Digital Ground	6.5V
Pin V_A to Pin V_D	±0.3V
Analog Ground to Digital Ground	±1V
Control Inputs to Digital Ground	–0.3V to V_D + 0.3V
Analog Input Voltage to Analog Ground	–0.3V to V_D + 0.3V
Maximum Junction Temperature	150°C
Internal Power Dissipation	875mW
Lead Temperature (soldering, 10s)	+300°C
Thermal Resistance, θ_{JA}: Plastic DIP	75°C/W
PLCC	75°C/W

THEORY OF OPERATION

ADS7803 uses the advantages of advanced CMOS technology (logic density, stable capacitors, precision analog switches, and low power consumption) to provide a precise 12-bit analog-to-digital converter with on-chip sampling and four-channel analog-input multiplexer.

The input stage consists of an analog multiplexer with an address latch to select from four input channels.

The converter stage consists of an advanced successive approximation architecture using charge redistribution on a capacitor network to digitize the input signal. A temperature-stabilized differential auto-zeroing circuit is used to minimize offset errors in the comparator.

Linearity errors in the binary weighted main capacitor network are corrected using a capacitor trim network and correction factors stored in on-chip memory. The correction terms are calculated by an on-chip microcontroller during a calibration cycle, initiated either by power-up or by applying an external calibration signal at any time. During conversion, the correct trim capacitors are switched into the main capacitor array as needed to correct the conversion accuracy. With all of the capacitors in both the main array and the trim array on the same chip, excellent stability is achieved, both over temperature and over time.

For flexibility, timing circuits include both an internal clock generator and an input for an external clock to synchronize with external systems. Standard control signals and three-state input/output registers simplify interfacing ADS7803 to most micro-controllers, microprocessors or digital storage systems.

The on-chip sampling provides excellent dynamic performance for input signals to 50kHz, and has a full-power –3dB bandwidth of 4MHz. Full control over sample-to-hold timing is available for applications where this is critical.

Finally, this performance is matched with the low-power advantages of CMOS structures to allow a typical power consumption of 10mW, with a 50µW power down option.

OPERATION

BASIC OPERATION

Figure 1 shows the simple circuit required to operate ADS7803 in the Transparent Mode, converting a single input channel. A convert command on pin 20 ($\overline{WR}$) starts a conversion. Pin 22 ($\overline{BUSY}$) will output a LOW during the conversion process

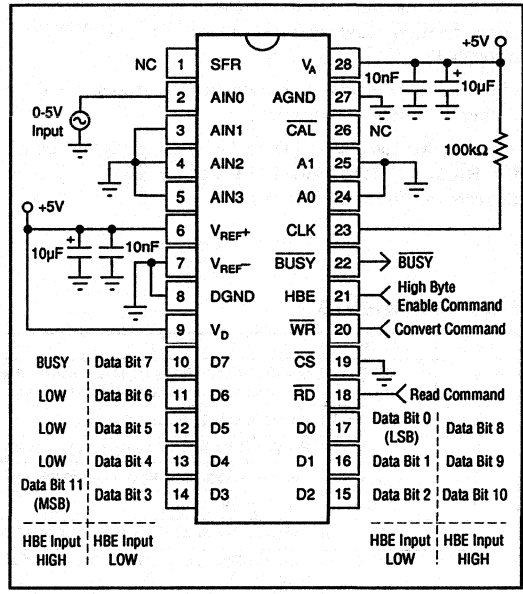
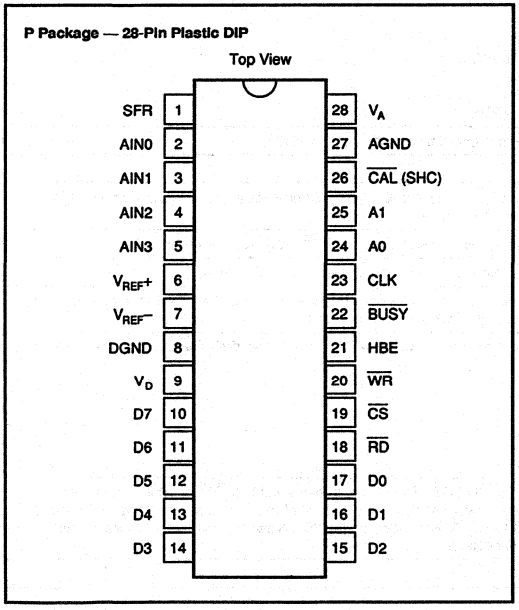
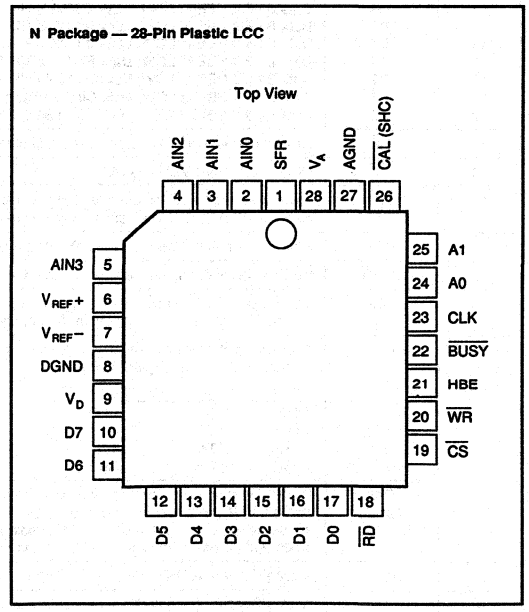


FIGURE 1. Basic Operation.

PIN CONFIGURATIONS





(including sample acquisition and conversion), and rises only after the conversion is completed. The two bytes of output data can then be read using pin 18 ($\overline{RD}$) and pin 21 (HBE).

STARTING A CONVERSION

A conversion is initiated on the rising edge of the $\overline{WR}$ input, with valid signals on A0, A1 and $\overline{CS}$. The selected input channel is sampled for five clock cycles. The successive approximation conversion takes place during clock cycles 6 through 17.

Figures 2 and 3 show the full conversion sequence and the timing to initiate a conversion.

A conversion can also be initiated by a rising edge on pin 26, if a HIGH has been written to D2 of the Special Function Register, as discussed below.

CALIBRATION

A calibration cycle is initiated automatically upon power-up (or after a power failure). Calibration can also be initiated by the user at any time by the rising edge of a minimum 100ns-wide LOW pulse on the $\overline{CAL}$ pin (pin 26), or by setting D1 HIGH in the Special Function Register (see SFR section). A calibration command will initiate a calibration cycle, regardless of whether a conversion is in process. During a calibration cycle, convert commands are ignored.

Calibration takes 168 clock cycles, and a normal conversion (17 clock cycles) is added automatically. Thus, at the end of a calibration cycle, there is valid conversion data in the output registers. For maximum accuracy, the supplies and reference need to be stable during the calibration procedure. To ensure that supply voltages and reference voltages have settled and are stable, an internal timer provides a waiting period of 42,425 clock cycles between power-up/power-failure and the start of the calibration cycle.

PIN ASSIGNMENTS

PIN #	NAME	DESCRIPTION
1	SFR	Special Function Register. When connected to a microprocessor address pin, allows access to special functions through D0 to D7. See the sections discussing the Special Function Register. If not used, connect to DGND. This pin has an internal pull-down.
2 to 5	AIN0 to AIN3	Analog inputs. Channel 0 to channel 3.
6	$V_{REF}+$	Positive voltage reference input. Normally +5V. Must be ≤ V_A.
7	$V_{REF}-$	Negative voltage reference input. Normally 0V.
8	DGND	Digital ground. DGND = 0V.
9	V_D	Logic supply voltage. V_D = +5V. Must be ≤ V_A and applied after V_A.
10 to 17	D0 to D7	Data Bus Input/Output Pins. Normally used to read output data. See section on SFR (Special Function Register) for other uses. When SFR is LOW, these function as follows:
10	D7	Data Bit 7 if HBE is LOW; if HBE is HIGH, acts as converter status pin and is HIGH during conversion or calibration, goes LOW after the conversion is completed. (Acts as an inverted $\overline{BUSY}$.)
11	D6	Data Bit 6 if HBE is LOW; LOW if HBE is HIGH.
12	D5	Data Bit 5 if HBE is LOW; LOW if HBE is HIGH.
13	D4	Data Bit 4 if HBE is LOW; LOW if HBE is HIGH.
14	D3	Data Bit 3 if HBE is LOW; Data Bit 11 (MSB) if HBE is HIGH.
15	D2	Data Bit 2 if HBE is LOW; Data Bit 10 if HBE is HIGH.
16	D1	Data Bit 1 if HBE is LOW; Data Bit 9 if HBE is HIGH.
17	D0	Data Bit 0 (LSB) if HBE is LOW; Data Bit 8 if HBE is HIGH.
18	$\overline{RD}$	Read Input. Active LOW; used to read the data outputs in combination with $\overline{CS}$ and HBE.
19	$\overline{CS}$	Chip Select Input. Active LOW.
20	$\overline{WR}$	Write Input. Active LOW; used to start a new conversion and to select an analog channel via address inputs A0 and A1 in combination with $\overline{CS}$. The minimum $\overline{WR}$ pulse LOW width is 100ns.
21	HBE	High Byte Enable. Used to select high or low data output byte in combination with $\overline{CS}$ and $\overline{RD}$, or to select SFR.
22	$\overline{BUSY}$	$\overline{BUSY}$ is LOW during conversion or calibration. $\overline{BUSY}$ goes HIGH after the conversion is completed.
23	CLK	Clock Input. For internal or external clock operation. For external clock operation, connect pin 23 to a 74HC-compatible clock source. For internal clock operation, connect pin 23 per the clock operation description.
24 to 25	A0 to A1	Address Inputs. Used to select one of four analog input channels in combination with $\overline{CS}$ and $\overline{WR}$. The address inputs are latched on the rising edge of $\overline{WR}$ or $\overline{CS}$. A1 / A0 / Selected Channel LOW / LOW / AIN0 LOW / HIGH / AIN1 HIGH / LOW / AIN2 HIGH / HIGH / AIN3
26	$\overline{CAL}$ (SHC)	Calibration Input. A calibration cycle is initiated when $\overline{CAL}$ is LOW. The minimum pulse width of $\overline{CAL}$ is 100ns. If not used, connect to V_D. In this case calibration is only initiated at power on, or with SFR. If D2 of the SFR is programmed HIGH, pin 26 will be used as an input to control the sample-to-hold timing. A rising edge on pin 26 will switch from sample-mode to hold-mode and initiate a conversion. This pin has an internal pull-up.
27	AGND	Analog Ground. AGND = 0V.
28	V_A	Analog Supply. V_A = +5V. Must be ≥ V_D and $V_{REF}+$.

READING DATA

Data from the ADS7803 is read in two 8-bit bytes, with the Low byte containing the 8 LSBs of data, and the High byte containing the 4 MSBs of data. The outputs are coded in straight binary (with 0V = 000 hex, 5V = FFF hex), and the data is presented in a right-justified format (with the LSB as the most right bit in the 16-bit word). Two read operations are required to transfer the High byte and Low byte, and the bytes are presented according to the input level on the High Byte Enable pin (HBE).

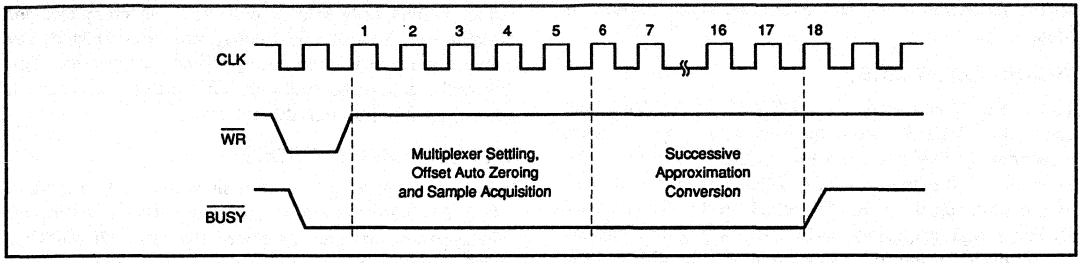


FIGURE 2. Converter Timing.

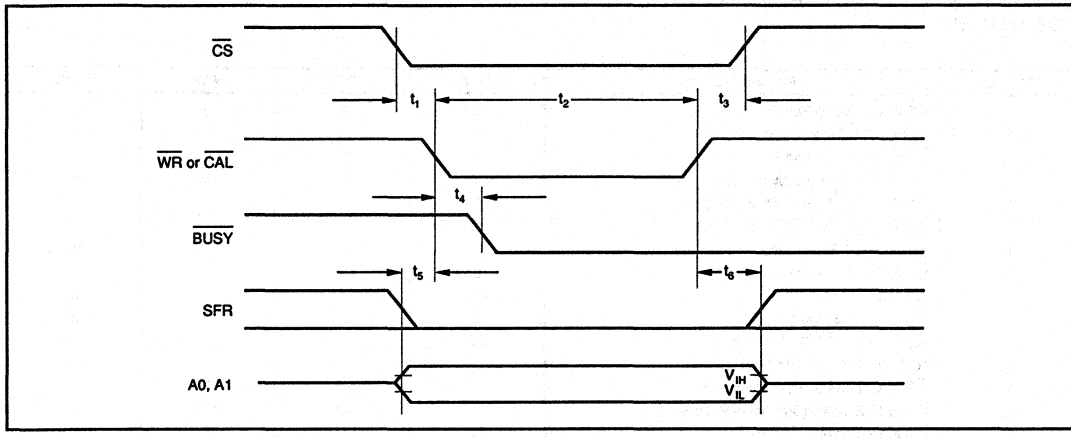


FIGURE 3. Write Cycle Timing (for initiating conversion or calibration).

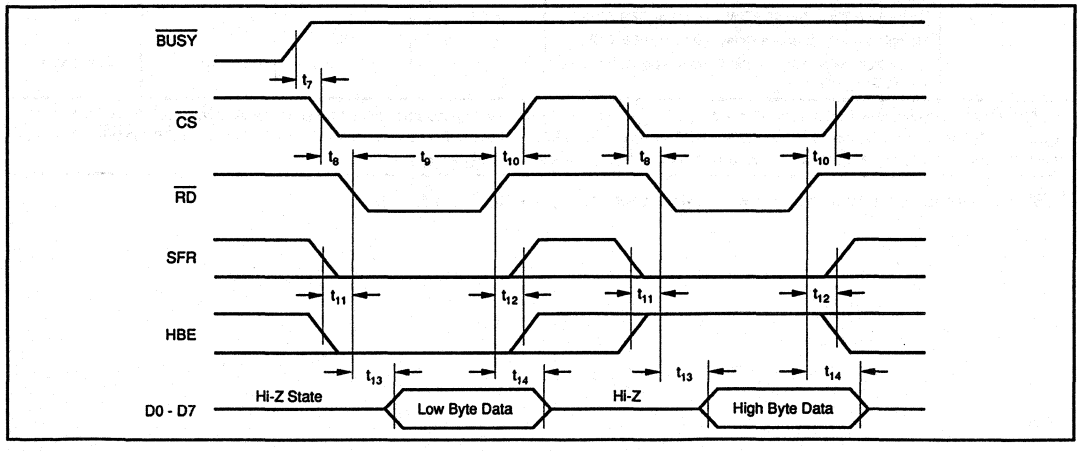


FIGURE 4. Read Cycle Timing.

The bytes can be read in either order, depending on the status of the HBE input. If HBE changes while $\overline{CS}$ and $\overline{RD}$ are LOW, the output data will change to correspond to the HBE input. Figure 4 shows the timing for reading first the Low byte and then the High byte.

ADS7803 provides two modes for reading the conversion results. At power-up, the converter is set in the Transparent Mode.

TRANSPARENT MODE

This is the default mode for ADS7803. In this mode, the conversion decisions from the successive approximation register are latched into the output register as they are made. Thus, the High byte (the 4 MSBs) can be read after the end of the ninth clock cycle (five clock cycles for the mux settling, sample acquisition and auto-zeroing of the comparator, followed by the four clock cycles for the 4MSB decisions.) The complete 12-bit data is available after $\overline{BUSY}$ has gone HIGH, or the internal status flag goes LOW (D7 when HBE is HIGH).

LATCHED OUTPUT MODE

This mode is activated by writing a HIGH to D0 in the Special Function Register with $\overline{CS}$ and $\overline{WR}$ LOW and SFR and HBE HIGH. (See the discussion of the Special Function Register below.)

In this mode, the data from a conversion is latched into the output buffers only after a conversion is complete, and remains there until the next conversion is completed. The conversion result is valid during the next conversion. This allows the data to be read even after a new conversion is started, for faster system throughput.

TIMING CONSIDERATIONS

Table I and Figures 3 through 9 show the digital timing of ADS7803 under the various operating modes. All of the critical parameters are guaranteed over the full –40°C to +85°C operating range for ease of system design.

SYMBOL	PARAMETER [1]	MIN	TYP	MAX	UNITS
t_1	$\overline{CS}$ to $\overline{WR}$ Setup Time [2]	0	0	0	ns
t_2	$\overline{WR}$ or $\overline{CAL}$ Pulse Width	100			ns
t_3	$\overline{CS}$ to $\overline{WR}$ Hold Time [2]	0	0	0	ns
t_4	$\overline{WR}$ to $\overline{BUSY}$ Propagation Delay	20	50	150	ns
t_5	A0, A1, HBE, SFR Valid to $\overline{WR}$ Setup Time	0			ns
t_6	A0, A1, HBE, SFR Valid to $\overline{WR}$ Hold Time	20			ns
t_7	$\overline{BUSY}$ to $\overline{CS}$ Setup Time	0			ns
t_8	$\overline{CS}$ to $\overline{RD}$ Setup Time [2]	0	0	0	ns
t_9	$\overline{RD}$ Pulse Width	100			ns
t_{10}	$\overline{CS}$ to $\overline{RD}$ Hold Time [2]	0	0	0	ns
t_{11}	HBE, SFR to $\overline{RD}$ Setup Time	50			ns
t_{12}	HBE, SFR to $\overline{RD}$ Hold Time	0			ns
t_{13}	$\overline{RD}$ to Valid Data (Bus Access Time) [3]		80	150	ns
t_{14}	$\overline{RD}$ to Hi-Z Delay (Bus Release Time) [3]		90	180	ns
t_{15}	$\overline{RD}$ to Hi-Z Delay For SFR [3]	20		60	ns
t_{16}	Data Valid to $\overline{WR}$ Setup Time	100			ns
t_{17}	Data Valid to $\overline{WR}$ Hold Time	20			ns
t_{18}	Acquisition Time. Pin 26 LOW with D2 in SFR HIGH	2.5			µs
t_{19}	Sample-to-Hold Aperture Delay. (D2 in SFR HIGH)		5		ns
t_{20}	Delay from rising edge on pin 26 to start of conversion. (D2 in SFR HIGH)			1.5	CLK cycles

NOTES: (1) All input control signals are specified with $t_{RISE} = t_{FALL} = 20ns$ (10% to 90% of 5V) and timed from a voltage level of 1.6V. Data is timed from V_{IH}, V_{IL}, V_{OH} or V_{OL}. (2) The internal RD pulse is performed by a NOR wiring of $\overline{CS}$ and $\overline{RD}$. The internal WR pulse is performed by a NOR wiring of $\overline{CS}$ and $\overline{WR}$. (3) Figures 8 and 9 show the measurement circuits and pulse diagrams for testing transitions to and from Hi-Z states.

TABLE I. Timing Specifications (CLK = 2MHz external, T_A = –40°C to +85°C).

SPECIAL FUNCTION REGISTER (SFR)

An internal register is available, either to determine additional data concerning the ADS7803, or to write additional instructions to the converter.

Table II shows the data in the Special Function Register that will be transferred to the output bus by driving HBE HIGH (with SFR HIGH) and initiating a read cycle (driving $\overline{RD}$ and $\overline{CS}$ LOW with $\overline{WR}$ HIGH.) The Power Fail flag in the SFR is set when the power supply falls below about 3V. The flag also means that a new calibration has been started, and any data written to the SFR has been lost. Thus, the ADS7803 will again be in the Transparent Mode. Writing a LOW to D5 in the SFR resets the Power Fail flag. The Cal Error flag in the SFR is set when an overflow occurs during calibration, which may happen in very noisy systems. It is reset by starting a calibration, and remains low after a calibration without an overflow is completed.

Table III shows how instructions can be transferred to the Special Function Register by driving HBE HIGH (with SFR HIGH) and initiating a write cycle (driving $\overline{WR}$ and $\overline{CS}$ LOW with $\overline{RD}$ HIGH.) Note that writing to the SFR also initiates a new conversion.

POWER DOWN MODE

Writing a HIGH to D3 in the SFR puts the ADS7803 in the Power Down Mode. Power consumption is reduced to 50µW and D3 remains HIGH. The internal clock and analog circuitry are turned off, although the output registers and SFR can still be accessed normally. To exit Power Down Mode, either write a LOW to D3 in the SFR, or initiate a calibration by sending a LOW to the $\overline{CAL}$ pin or writing a HIGH to D1. Note that if the power supply falls below 3V and then recovers, a calibration is automatically initiated, and the SFR will be reset. D3 will be LOW, and the ADS7803 will not be in the Power Down Mode.

PIN	FUNCTION	DESCRIPTION
D0	Mode Status	If LOW, Transparent Mode enabled for data latches. If HIGH, Latched Output Mode enabled.
D1	CAL Flag	If HIGH, calibration cycle in progress.
D2	Pin 26 Status	If LOW, pin 26 used as input to initiate calibration cycle. If HIGH, pin 26 used as input to control sample-to-hold timing.
D3	Power Down Status	If HIGH, in Power Down Mode.
D4		Reserved for factory use.
D5	POWER FAIL Flag	If HIGH, a power supply failure has occurred. (Supply fell below 3V.)
D6	CAL ERROR Flag	If HIGH, an overflow occurred during calibration.
D7	BUSY Flag	If HIGH, conversion or calibration in progress.
NOTE: These data are transferred to the bus when a read cycle is initiated with SFR and HBE HIGH. Reading the SFR with SFR HIGH and HBE LOW is reserved for factory use at this time, and will yield unpredictable data.		

TABLE II. Reading the Special Function Register.

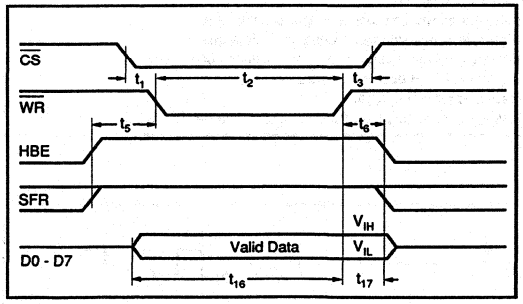


FIGURE 5. Writing to the SFR.

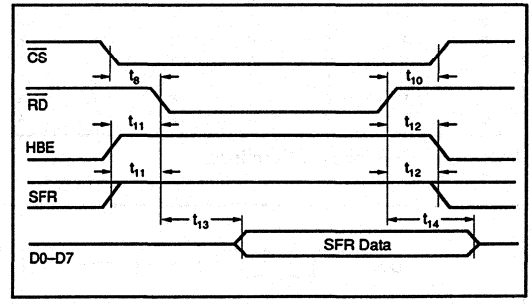


FIGURE 6. Reading the SFR.

	$\overline{CS}/\overline{WR}$	SFR/HBE	D0	D1	D2	D3	D5	D4/D6/D7
Enables Transparent Mode for Data Latches.	LOW	HIGH	LOW	X	X	X	X	LOW
Enables Latched Output Mode for Data Latches.	LOW	HIGH	HIGH(1)	X	X	X	X	LOW
Initiates Calibration Cycle.	LOW	HIGH	X	HIGH	X	X	X	LOW
Activates Sample/Hold Control Mode	LOW	HIGH	X	X	HIGH(1)	X	X	LOW
Activates Power Down Mode(2)	LOW	HIGH	X	X	X	HIGH(1)	X	LOW
Resets Power Fail Flag.	LOW	HIGH	X	X	X	X	LOW	LOW
NOTES: (1) Writing a LOW here reactivates the standard mode of operation. (2) In Power Down Mode, a pulse on $\overline{CS}$ and $\overline{WR}$ will initiate a single conversion, then the ADS7803 will revert to power down. (3) X means it can be either HIGH or LOW without affecting this action. Writing HIGH to D4 or D6, or writing with SFR HIGH and HBE LOW, may result in unpredictable behavior. These modes are reserved for factory use at this time.								

TABLE III. Writing to the Special Function Register.

During Power Down Mode, a pulse on $\overline{CS}$ and $\overline{WR}$ will initiate a single conversion, then the ADS7803 will revert to power down. Also, writing to D1 and D3 in the SFR will initiate a calibration, do a single conversion and revert to the Power Down Mode, in 185 clock cycles. Accurate conversion results will be available in the output registers.

The activation delay from power down to normal operation is included in the sampling time. No extra time is required, either when coming out of the Power Down Mode or when making a single conversion in the Power Down Mode.

SAMPLE/HOLD CONTROL MODE

With D2 in the SFR HIGH, a rising edge input on pin 26 will switch the ADS7803 from sample-mode to hold-mode with a 5ns aperture delay. This also initiates a conversion, which will start within 1.5 CLK cycles.

This mode allows full control over the sample-to-hold timing, which is especially useful where external events trigger sampling timing.

In the Sample/Hold Control Mode, pin 26 must be held LOW a minimum of 2.5µs between conversions to allow accurate acquisition of input signals. Also, offset error will increase in this mode, since auto-zeroing of the comparator is not synchronized to the sampling. Minimum offset is achieved by synchronizing the sampling signal to CLK, whether internal or external. Ideally, the sampling signal rising edge should be delayed 20ns from the falling edge of CLK. This will keep offset error to about 1LSB.

In the Sample/Hold Control Mode, a LOW pulse on $\overline{WR}$ (with $\overline{CS}$ LOW) will not initiate a conversion, but the rising edge will latch the multiplexer channel according to the inputs on A0 and A1. When changing channels, this must be done at least 2.5µs before pin 26 goes HIGH (to start a conversion.)

CONTROL LINES

Table IV shows the functions of the various control lines on the ADS7803. The use of standard $\overline{CS}$, $\overline{RD}$ and $\overline{WR}$ control signals simplifies use with most microprocessors. At the same time, flexibility is assured by availability of status information and control functions, both through the SFR and directly on pins.

INSTALLATION

INPUT IMPEDANCE

ADS7803 has a very high input impedance (input bias current over temperature is 100nA max), and a low 50pF input capacitance. To ensure a conversion accurate to 12 bits, the analog source must be able to charge the 50pF and settle

$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	SFR	HBE	$\overline{CAL}$	$\overline{BUSY}$	OPERATION
X	X	X	X	X	0↑1	X	Initiates calibration cycle. (see SFR section for alternate use as Sample/Hold Control Mode input.)
X	X	X	X	X	X	0	Conversion or calibration in process. Inhibits new conversion from starting.
1	X	X	X	X	1	X	None. Outputs in HI-Z State.
0	1	0↑1	0	X	1	1	Initiates conversion.
0	0	1	0	0	1	X	Low byte conversion results output on data bus.
0	0	1	0	1	1	X	High byte conversion results output on data bus.
0	1	0	1	1	1	1	Write to SFR and rising edge on WR initiates conversion.
0	0	1	1	1	1	X	Contents of SFR output on data bus.
0	1	0	1	0	1	X	Reserved for factory use.
0	0	1	1	0	1	X	Reserved for factory use. (Unpredictable data on data bus.)

TABLE IV. Control Line Functions.

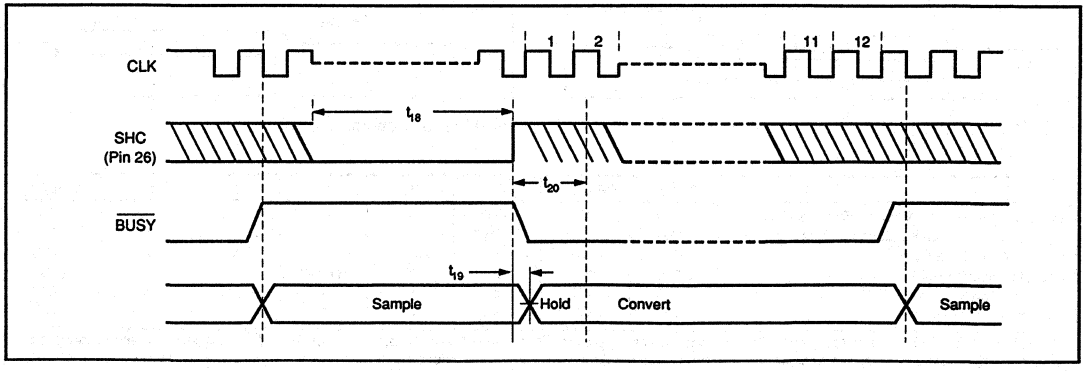


FIGURE 7. Timing for Initiating Conversion in Sample/Hold Control Mode (D2 in SFR HIGH).

within the first five clock cycles after a conversion is initiated. During this time, the input is also very sensitive to noise at the analog input, since it could be injected into the capacitor array.

In many applications, a simple passive low-pass filter as shown in Figure 10a can be used to improve signal quality. In this case, the source impedance needs to be less than 5kΩ to keep the induced offset errors below 1/2LSB, and to meet the acquisition time of five clock cycles. The values in Figure 10a meet these requirements, and will maintain the full power bandwidth of the system. For higher source impedances, a buffer like the one in Figure 10b should be used.

INPUT PROTECTION

The input signal range must not exceed $\pm V_{REF}$ or V_A by more than 0.3V.

The analog inputs are internally clamped to V_A. To prevent damage to the ADS7803, the current that can flow into the inputs must be limited to 20mA. One approach is to use an external resistor in series with the input filter resistor. For example, a 1kΩ input resistor allows an overvoltage to 20V without damage.

REFERENCE INPUTS

A 10µF tantalum capacitor is recommended between $V_{REF}+$ and $V_{REF}-$ to insure low source impedance. These capacitors should be located as close as possible to the ADS7803 to reduce dynamic errors, since the reference provides packets of current as the successive approximation steps are carried out.

$V_{REF}+$ must not exceed V_A. Although the accuracy is specified with $V_{REF}+ = 5V$ and $V_{REF}- = 0V$, the converter can function with $V_{REF}+$ as low as 2.5V and $V_{REF}-$ as high as 1V. As long as there is at least a 2.5V difference between $V_{REF}+$ and $V_{REF}-$, the absolute value of errors does not change significantly, so that accuracy will typically be within ±1LSB. (1/2LSB for a 5V span is 610µV, which is 1LSB for a 2.5V span.)

The power supply to the reference source needs to be considered during system design to prevent $V_{REF}+$ from exceeding (or overshooting) V_A, particularly at power-on. Also, after power-on, if the reference is not stable within 42,425 clock cycles, an additional calibration cycle may be needed.

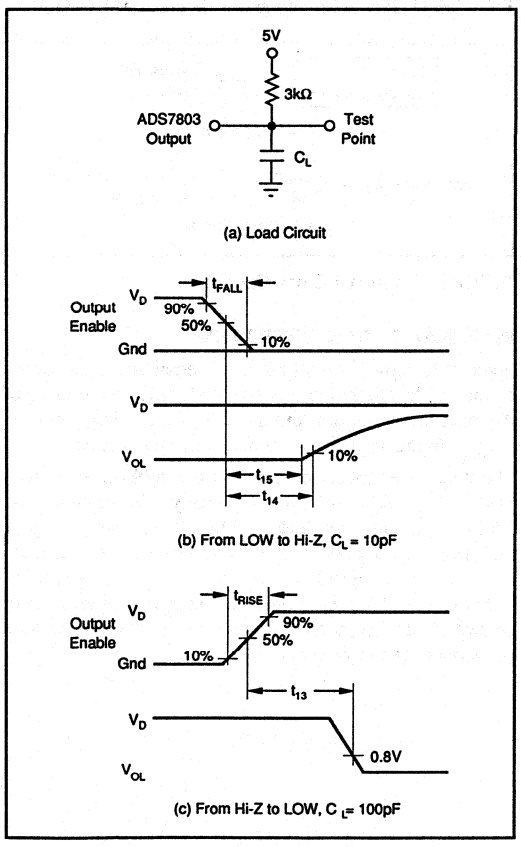


FIGURE 8. Measuring Active LOW to/from Hi-Z State.

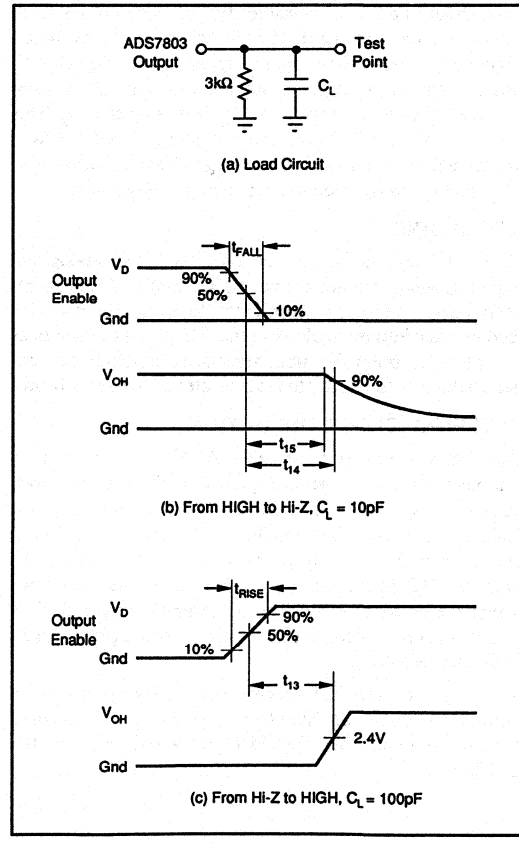


FIGURE 9. Measuring Active HIGH to/from Hi-Z State.

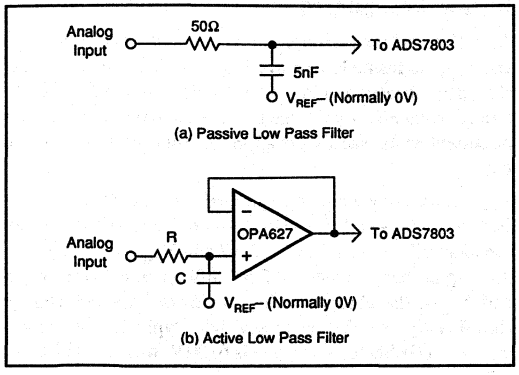


FIGURE 10. Input Signal Conditioning.

POWER SUPPLIES

The digital and analog power supply lines to the ADS7803 should be bypassed with 10µF tantalum capacitors as close to the part as possible. Although ADS7803 has excellent power supply rejection, even for higher frequencies, linear regulated power supplies are recommended.

Care should be taken to insure that V_D does not come up before V_A, or permanent damage to the part may occur. Figure 10 shows a good supply approach, powering both V_A and V_D from a clean linear supply, with the 10Ω resistor between V_A and V_D insuring that V_D comes up after V_A. This is also a good method to further isolate the ADS7803 from digital supplies in a system with significant switching currents that could degrade the accuracy of conversions.

GROUNDING

To maximize accuracy of the ADS7803, the analog and digital grounds are not connected internally. These points should have very low impedance to avoid digital noise feeding back into the analog ground. The V_{REF}– pin is used as the reference point for input signals, so it should be connected directly to AGND to reduce potential noise problems.

EXTERNAL CLOCK OPERATION

The circuitry required to drive the ADS7803 clock from an external source is shown in Figure 12a. The external clock must provide a 0.8V max for LOW and a 3.5V min for HIGH, with rise and fall times that do not exceed 200ns. The duty cycle of the external clock can vary as long as the LOW time and HIGH time are each at least 200ns wide. Synchronizing the conversion clock to an external system clock is recommended in microprocessor applications to prevent beat-frequency problems.

Note that the electrical specification tables are based on using an external 2MHz clock. Typically, the specified accuracy is maintained for clock frequencies between 0.5 and 2.4MHz.

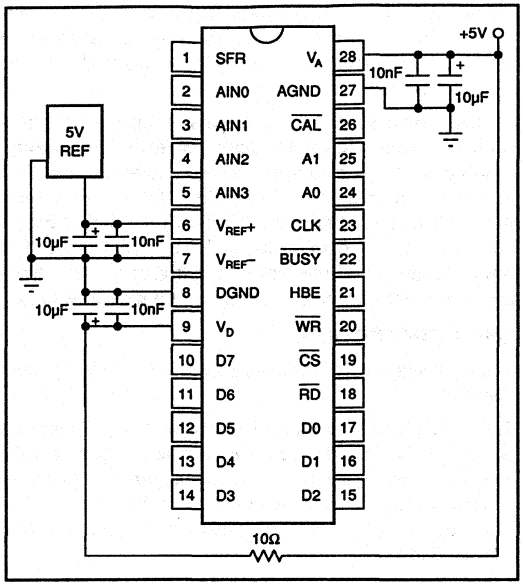


FIGURE 11. Power Supply and Reference Decoupling.

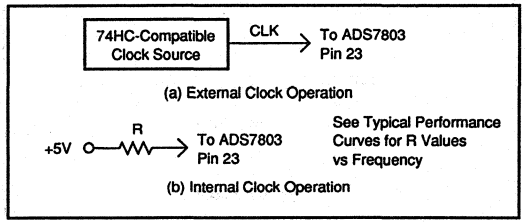


FIGURE 12. Internal Clock Operation.

INTERNAL CLOCK OPERATION

Figure 12b shows how to use the internal clock generating circuitry. The clock frequency depends only on the value of the resistor, as shown in "Internal Clock Frequency vs R_{CLOCK}" in the Typical Performance Curves section.

The clock generator can operate between 100kHz and 2MHz. With R = 100kΩ, the clock frequency will nominally be 800kHz. The internal clock oscillators may vary by up to 20% from device to device, and will vary with temperature, as shown in the typical performance curves. Therefore, use of an external clock source is preferred in applications where control of the conversion timing is critical, or where multiple converters need to be synchronized.

APPLICATIONS

BIPOLAR INPUT RANGES

Figure 13 shows a circuit to accurately and simply convert a bipolar ±5V input signal into a unipolar 0 to 5V signal for conversion by the ADS7803, using a precision, low-cost complete difference amplifier, INA105.

Figure 14 shows a circuit to convert a bipolar ±10V input signal into a unipolar 0 to 5V signal for conversion by the ADS7803. The precision of this circuit will depend on the matching and tracking of the three resistors used.

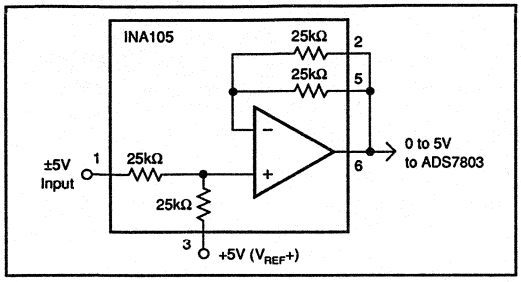


FIGURE 13. ±5V Input Range.

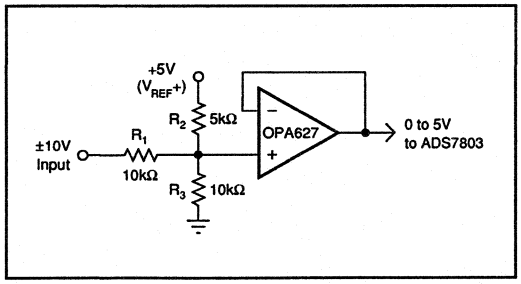


FIGURE 14. ±10V Input Range.

To trim this circuit for full 12-bit precision, R2 and R3 need to be adjustable over appropriate ranges. To trim, first have the ADS7803 converting continually and apply +9.9927V (+10V – 1.5LSB) at the input. Adjust R3 until the ADS7803 output toggles between the codes FFE hex and FFF hex. This makes R3 extremely close to R1. Then, apply –9.9976V (–10V + 0.5LSB) at the input, and adjust R2 until the ADS7803 output toggles between 000 hex and 001 hex. At each trim point, the current through the third resistor will be almost zero, so that one trim iteration will be enough in most cases. More iterations may be required if the op amp selected has large offset voltage or bias currents, or if the +5V reference is not precise.

This circuit can also be used to adjust gain and offset errors due to the components preceding the ADS7803, to match the performance of the self-calibration provided by the converter.

INTERFACING TO MOTOROLA MICROPROCESSORS

Figure 15 shows a typical interface to Motorola microprocessors, while Figure 16 shows how the result can be placed in register D0.

Conversion is initiated by a write instruction decoded by the address decoder logic, with the lower two bits of the address bus selecting an ADC input channel, as follows:

MOVE.W D0, ADC-ADDRESS

The result of the conversion is read from the data bus by a read instruction to ADC-ADDRESS as follows:

MOVEP.W $000 (ADC-ADDRESS), D0

This puts the 12-bit conversion result in the DO register, as shown in Figure 15. The address decoder must pull down $\overline{\text{ADC\_CS}}$ at ADC-ADDRESS to access the Low byte and ADC-ADDRESS +2 to access the High byte.

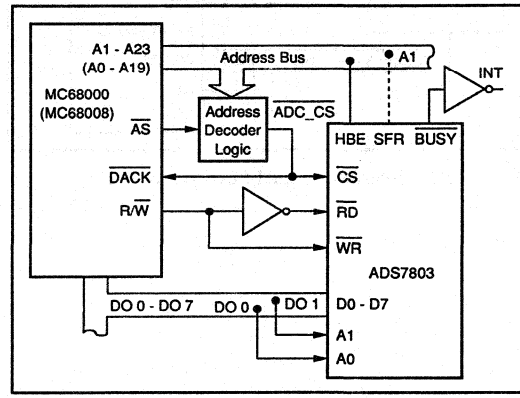


FIGURE 15. Interface to Motorola Microprocessors.

INTERFACING TO INTEL MICROPROCESSORS

Figure 17 shows a typical interface to Intel.

A conversion is initiated by a write instruction to address $\overline{\text{ADC\_CS}}$. Data pins DO0 and DO1 select the analog input channel. The $\overline{\text{BUSY}}$ signal can be used to generate a microprocessor interrupt (INT) when the conversion is completed.

A read instruction from the $\overline{\text{ADC\_CS}}$ address fetches the Low byte, and a read instruction from the ADC_CS address +2 fetches the High byte.

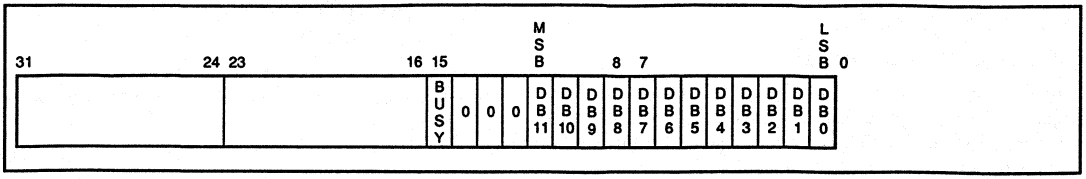


FIGURE 16. Conversion Results in Motorola Register D0.

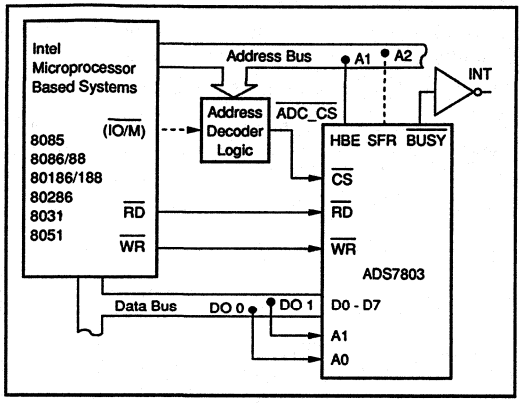
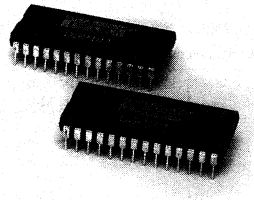


FIGURE 17. Interface to Intel Microprocessors.

BURR-BROWN®



DSP101
DSP102

DSP-Compatible Sampling Single/Dual ANALOG-TO-DIGITAL CONVERTERS

FEATURES

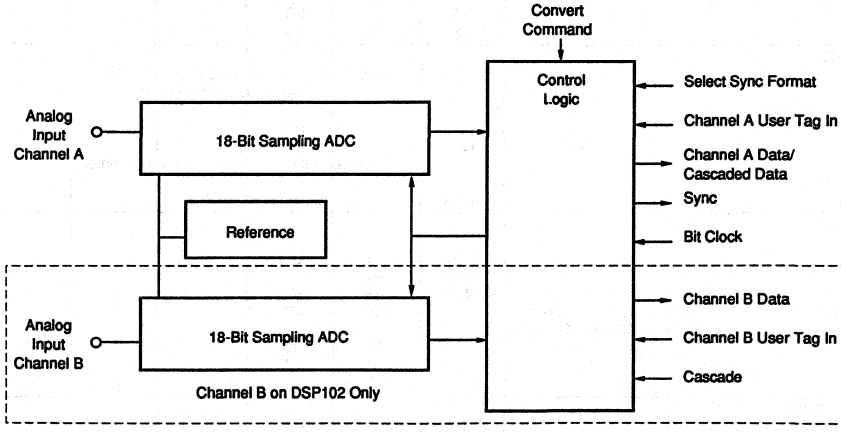
- ZERO-CHIP INTERFACE TO STANDARD DSP ICs: AD, AT&T, MOTOROLA, TI
- SINGLE CHANNEL: DSP101
- DUAL CHANNEL: DSP102
  Two Serial Outputs or Cascade to Single 32-Bit Word
- SAMPLING RATE TO 200kHz
- DYNAMIC SPECIFICATIONS:
  Signal/(Noise + Distortion) = 88dB;
  Spurious-Free Dynamic Range = 94dB;
  THD = –91dB
- SERIAL OUTPUT DATA COMPATIBLE WITH 16-, 24-, AND 32-BIT DSP IC FORMATS

DESCRIPTION

The DSP101 and DSP102 are high performance sampling analog-to-digital converters designed for simplicity of use with modern digital signal processing ICs. Both are complete with all interface logic for use directly with DSP ICs, and provide full sampling and conversion at rates up to 200kHz.

The DSP101 offers a single conversion channel, with 18 bits of serial data output, allowing the user to drive 16-bit, 24-bit, or 32-bit DSP ports. The DSP102 offers two complete conversion channels, with either two full 18-bit output ports, or a mode to cascade two 16-bit conversions into a 32-bit port as one word.

Both the DSP101 and DSP102 are packaged in standard, low-cost 28-pin plastic DIP packages. Each is offered in two performance grades to match application requirements.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL

T_A = 0°C to 70°C, ±2.75V input signal, sampling frequency (f_S) = 200kHz, $V_A+ = V_D = +5V$, $V_A- = -5V$, 16MHz external clock on OSC1, CLKOUT tied to CLKIN, 8MHz data transfer clock on XCLK, data analysis band-limited to 20kHz, unless otherwise specified.

		DSP101JP DSP102JP			DSP101KP DSP102KP			
PARAMETER	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
RESOLUTION				18			•	Bits
ANALOG INPUT								
Voltage Range			±2.75V			•		V
Impedance			1			•		kΩ
Capacitance			20			•		pF
THROUGHPUT SPEED								
Complete Cycle	Acquisition + Conversion			5			•	µs
Throughput Rate		200			•			kHz
AC ACCURACY [1]								
Signal to (Noise + Distortion) Ratio	f_{IN} = 1kHz	83	86		86	88		dB[2]
	f_{IN} = 1kHz (–60dB)		32			•		dB
	f_{IN} = 25kHz		82			•		dB
Total Harmonic Distortion	f_{IN} = 1kHz		–90	–86		–91	–89	dB
Spurious-Free Dynamic Range	f_{IN} = 1kHz	89	92		92	94		dB
Signal to Noise Ratio (SNR)	f_{IN} = 1kHz	84	88		87	89		dB
DC ACCURACY								
Gain Error				±5			•	%
Gain Error Mismatch	DSP102 Channels			±2			•	%
Integral Linearity	±2.75V Input Range		Sufficient to meet AC Accuracy Specifications					
Differential Linearity	±2.75V Input Range		Sufficient to meet AC Accuracy Specifications					
Integral Linearity Error	±0.7V Input Range		±0.003			•		%
Differential Linearity Error	±0.7V Input Range		±0.002			•		%
No Missing Codes	±0.7V Input Range		14			•		Bits
Bipolar Zero Error [3]			±2					mV
Bipolar Zero Mismatch [3]	DSP102 Channels		±2					mV
Power Supply Sensitivity	$-5.25V < V_A- < -4.75V$		–60			•		dB
	$+4.75V < V_A+, V_D+ < +5.25V$		–60			•		dB
SAMPLING DYNAMICS								
Aperture Delay			30			•		ns
Aperture Jitter			100			•		ps,rms
Transient Response			1			•		µs
Overvoltage Recovery			5			•		µs
DIGITAL INPUTS								
Logic Levels (Except OSC1)								
V_{IL}	I_L = ±10µA	0		+0.8	•		•	V
V_{IH}	I_H = ±10µA	+2.4		+5	•		•	V
OSC1 Clock				74HC Compatible				
Frequency				16				MHz
Data Transfer Clock (XCLK)								
Frequency		0.1		12	•		•	MHz
Duty Cycle		40	50	60	•		•	%
Conversion Clock (CLKIN)								
Frequency		0.5		5.33	•		•	MHz
Duty Cycle		25	33	55	•	•	•	%
DIGITAL OUTPUTS								
Format			Serial; MSB first; 16/18-bit and Cascaded 32-bit Mode					
Coding			Binary Two's Complement					
Logic Levels (Except OSC2)								
V_{OL}	I_{SINK} = 4mA	0		+0.4	•		•	V
V_{OH}	I_{SOURCE} = 4mA	+2.4		+5	•		•	V
OSC2			Can only be used to drive crystal oscillator.					
Conversion Clock (CLKOUT)								
Drive Capability		±2mA			•			mA
POWER SUPPLIES								
Rated Voltage								
V_A+		+4.75	+5	+5.25	•	•	•	V
V_A-		–5.25	–5	–4.75	•	•	•	V
V_D		+4.75	+5	+5.25	•	•	•	V
Power Consumption	XCLK = OSC1 = 12MHz		250	425		•	•	mW
Supply Current	XCLK = OSC1 = 12MHz							
I_A+			30	45		•	•	mA
I_A-			–18	–25		•	•	mA
I_D			5	15		•	•	mA
TEMPERATURE RANGE								
Specification		0		+70	•		•	°C
Storage		–65		+125	•		•	°C

NOTES: (1) All dynamic specifications are based on 2048-point FFTs, using four-term Blackman-Harris window. (2) All specifications in dB are referred to a full-scale input, ±2.75Vp-p. (3) Adjustable to zero with external potentiometer.

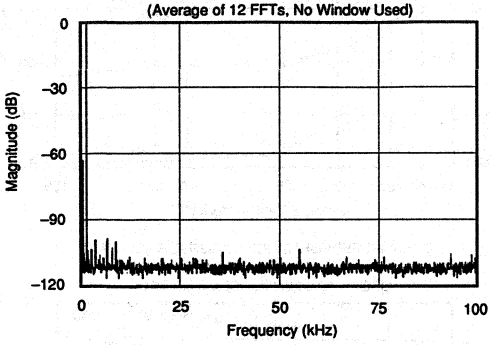
TYPICAL PERFORMANCE CURVES

At T_A = +25°C, $V_A+ = V_D+ = +5V$, $V_A- = V_D- = -5V$, Sampling Frequency f_S = 200kHz; External Clock Input at OSC1 = $80f_S$ = 16MHz, XCLK = $40f_S$ = 8MHz; Using 2048 Point FFT; Data analysis limited to 0 to 20kHz band; Unless otherwise specified.

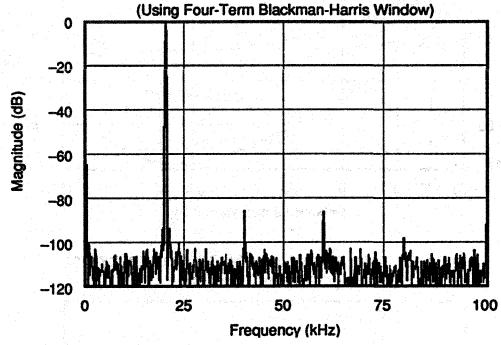
SINAD means Signal-to-(Noise + Distortion) Ratio.
SNR means Signal-to-Noise Ratio excluding harmonics thru the 8th.

THD means Total Harmonic Distortion thru 8th harmonic.
SFDR means Spurious Free Dynamic Range, including harmonics.

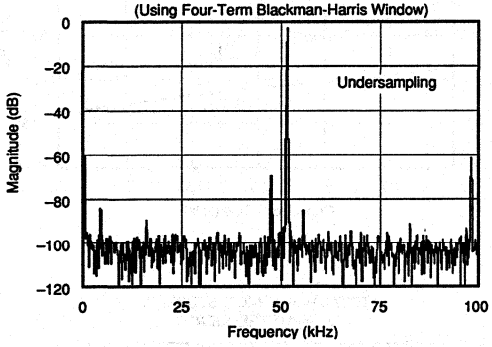
FREQUENCY SPECTRUM of ±2.75V, 1kHz INPUT
(Average of 12 FFTs, No Window Used)



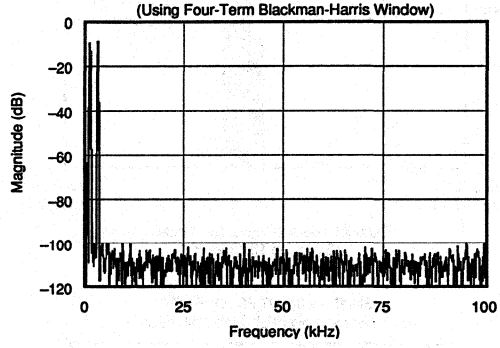
FREQUENCY SPECTRUM of ±2.75V, 20kHz INPUT
(Using Four-Term Blackman-Harris Window)



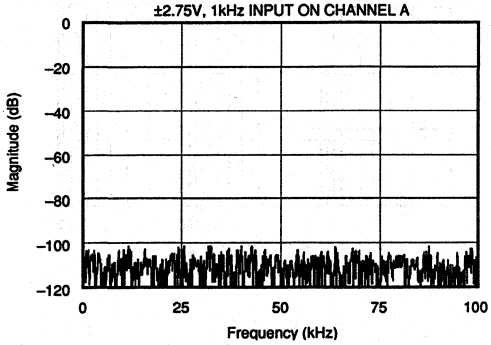
FREQUENCY SPECTRUM of ±2.75V, 451kHz INPUT
(Using Four-Term Blackman-Harris Window)



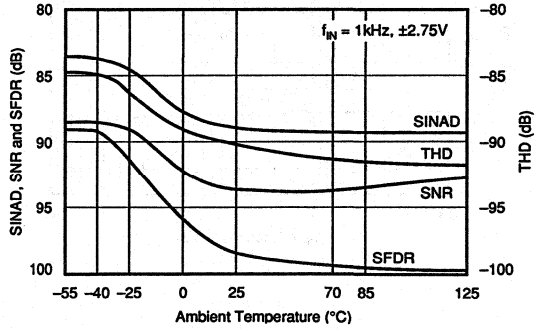
INTERMODULATION DISTORTION WITH 1kHz AND 3kHz INPUTS
(Using Four-Term Blackman-Harris Window)



DSP102 CHANNEL SEPARATION ON CHANNEL B WITH
±2.75V, 1kHz INPUT ON CHANNEL A



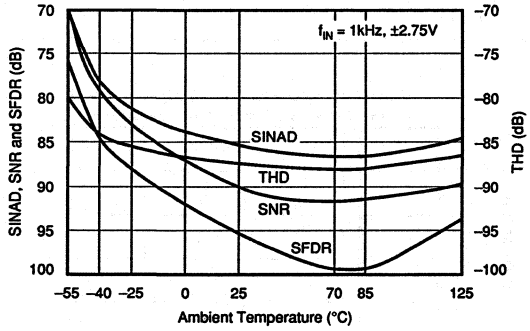
DYNAMIC PERFORMANCE vs TEMPERATURE



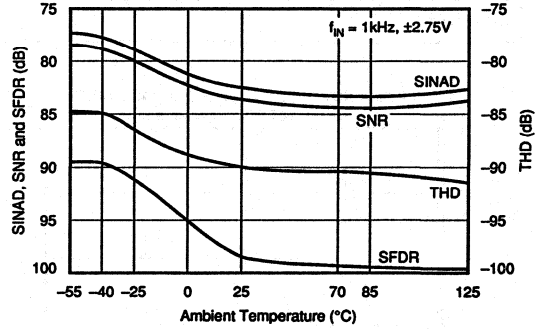
TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C, V_{A+} = V_{D+} = +5V, V_{A-} = V_{D-} = –5V, Sampling Frequency f_S = 200kHz; External Clock Input at OSC1 = 80f_S = 16MHz, XCLK = 40f_S = 8MHz; Using 2048 Point FFT; Data analysis limited to 0 to 20kHz band; Unless otherwise specified.

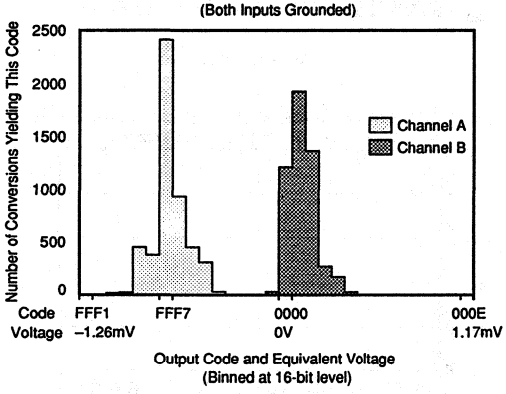
DYNAMIC PERFORMANCE vs TEMPERATURE
(f_S = 180kHz Asychronous to 12.288MHz
Crystal Between OSC1 and OSC2)



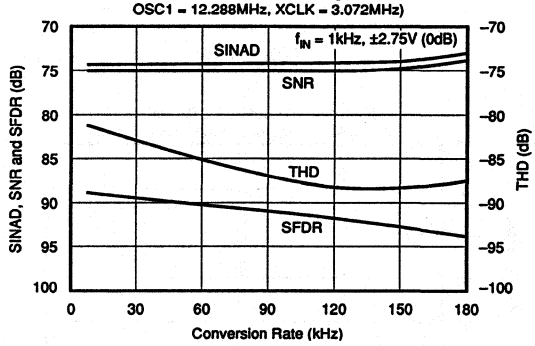
DYNAMIC PERFORMANCE vs TEMPERATURE
(Data Analysis Over Full 0 to 100kHz Band)



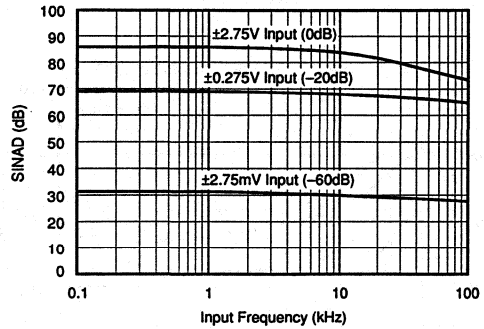
HISTOGRAM OF 5k CONVERSION RESULTS ON DSP102
(Both Inputs Grounded)



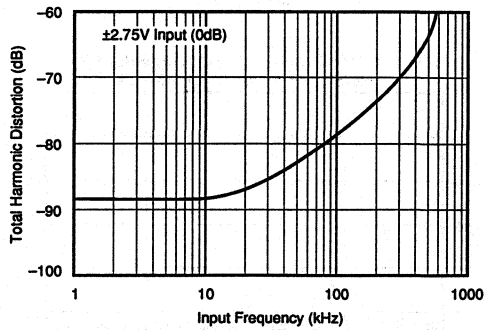
DYNAMIC PERFORMANCE vs CONVERSION RATE
(Data Analysis over Full 0 to f_S/2 Band,
OSC1 = 12.288MHz, XCLK = 3.072MHz)



SINAD vs INPUT FREQUENCY
(Data Analysis over Full 0 to 100kHz Band)

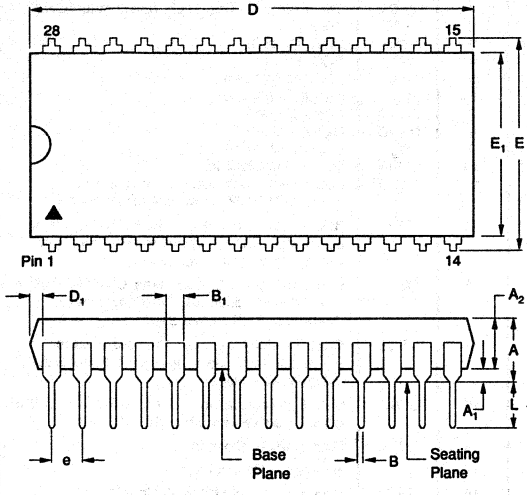


TOTAL HARMONIC DISTORTION
vs INPUT FREQUENCY



MECHANICAL

P Package — 28-Pin Plastic, Double-Wide DIP



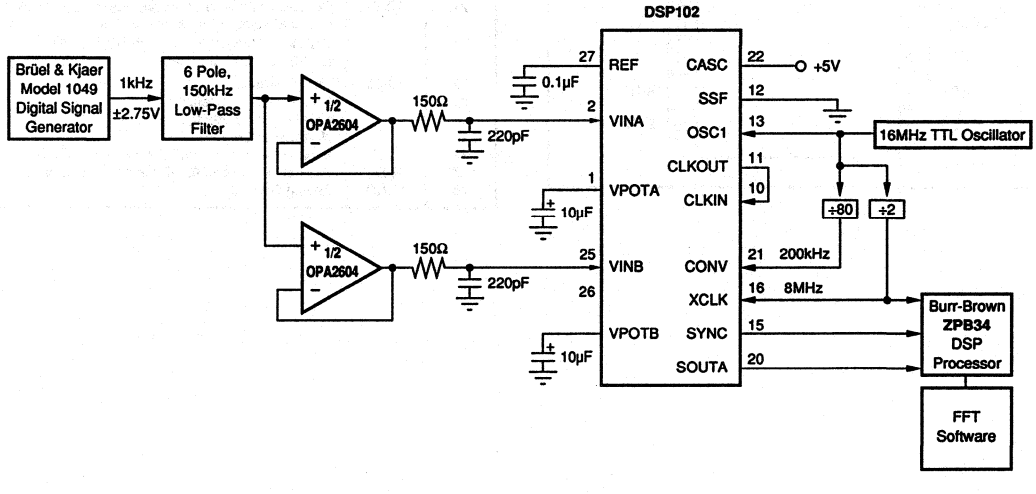
DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.155	.250	3.94	6.35
A_1	.015	.070	.381	1.78
A_2	.140	.185	3.57	4.70
B	.014	.022	.356	.559
B_1	.040	.070	1.02	1.78
C	.008	.015	.20	.381
D	1.435	1.480	36.45	37.59
D_1	.040	.100	1.020	2.540
E	.600	.625	15.24	15.88
E_1	.525	.565	13.34	14.35

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
e	.100 BASIC		2.54 BASIC	
eA	.600 BASIC		15.24 BASIC	
eB	.600	.700	15.24	17.78
L	.115	.200	2.91	5.08

NOTES:
(1) Not JEDEC Standard.
(2) Controlling dimension: INCH.
(3) Dimensioning and tolerancing per ANSI Y14.5M-1982.
(4) Dimensions A, A_1 and L are measured with package seated in JEDEC Seating Plane Gauge GS-3.
(5) D and E_1 does not include mold flash. Mold flash shall not exceed .010 inches, 0.25mm.
(6) eB and eC are measured at the lead tips with the leads unconstrained. eC must be zero or greater.

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

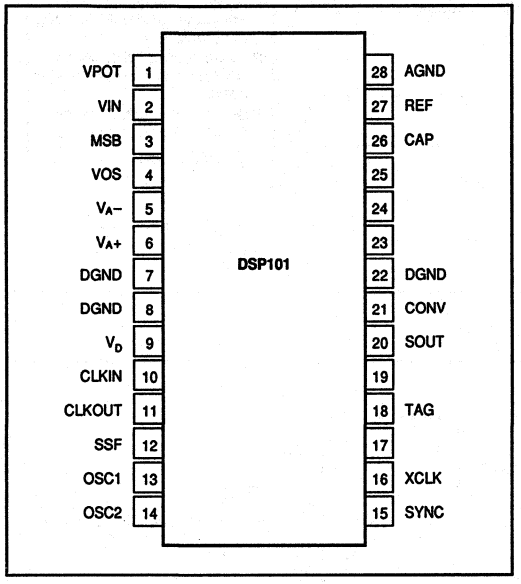
TYPICAL DSP102 FFT SETUP



ABSOLUTE MAXIMUM RATINGS

V_A+ to Analog Common	+7V
V_A– to Analog Common	–7V
V_D to Digital Common	+7V
Analog Common to Digital Common	±1V
Control Inputs to Digital Common	–0.5 to V_D + 0.5V
Analog Input Voltage	±5V
Maximum Junction Temperature	150°C
Internal Power Dissipation	825mW
Lead Temperature (soldering, 10s)	+300°C
Thermal Resistance, θ_{JA}, Plastic DIP	50°C/W

DSP101 PIN CONFIGURATION



DSP101 PIN ASSIGNMENTS

PIN #	NAME	DESCRIPTION
1	VPOT	Trim Reference Out. 10µF Tantalum to AGND.
2	VIN	Analog In.
3	MSB	MSB Adjust In.
4	VOS	VOS Adjust In.
5	V_A–	–5V Analog Power.
6	V_A+	+5V Analog Power.
7	DGND	Digital Ground.
8	DGND	Digital Ground.
9	V_D	+5V Digital Power.
10	CLKIN	Conversion Clock In.
11	CLKOUT	Conversion Clock Out. Can drive multiple DSP101/DSP102s to synchronize conversion.
12	SSF	Select Synch Format In. If HIGH, SYNC will be active High. If LOW, SYNC will be active Low. See timing diagram (Figure 1).
13	OSC1	Oscillator Point 1 Input/External Clock In. If using external clock, drive with 74HC logic levels. Connect to DGND if not used.
14	OSC2	Oscillator Point 2 Output. Provides drive for crystal oscillator. Make no electrical connection if using external clock.
15	SYNC	Data Synchronization Out. Active High when SSF is HIGH; active Low when SSF is LOW.
16	XCLK	Data Transfer Clock In.
17		No Internal Connection.
18	TAG	User Tag In. Data clocked into this pin is appended to the conversion results on SOUT. See timing diagram (Figure 1).
19		No Internal Connection.
20	SOUT	Serial Data Out. MSB first, Binary Two's Complement format.
21	CONV	Convert Command In. Falling edge puts converter into hold state, initiates conversion, and transmits previous conversion results to DSP IC with appropriate SYNC pulse.
22	DGND	Digital Ground.
23		No Internal Connection.
24		No Internal Connection.
25		No Internal Connection.
26	CAP	Bypass Capacitor. 10µF Tantalum to AGND.
27	REF	Reference Bypass. 0.1µF Ceramic to AGND.
28	AGND	Analog Ground.

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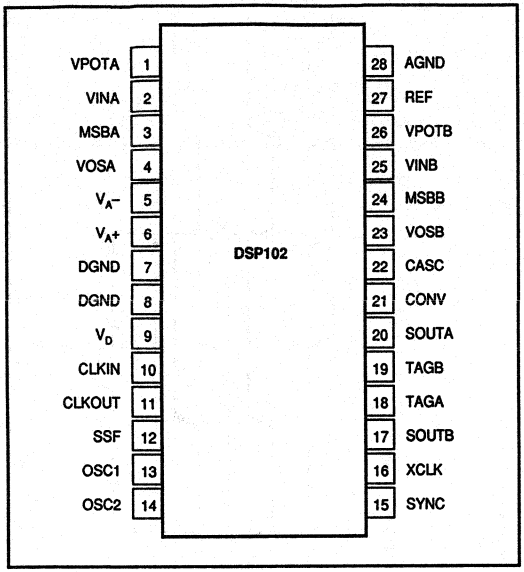
DSP102 PIN CONFIGURATION

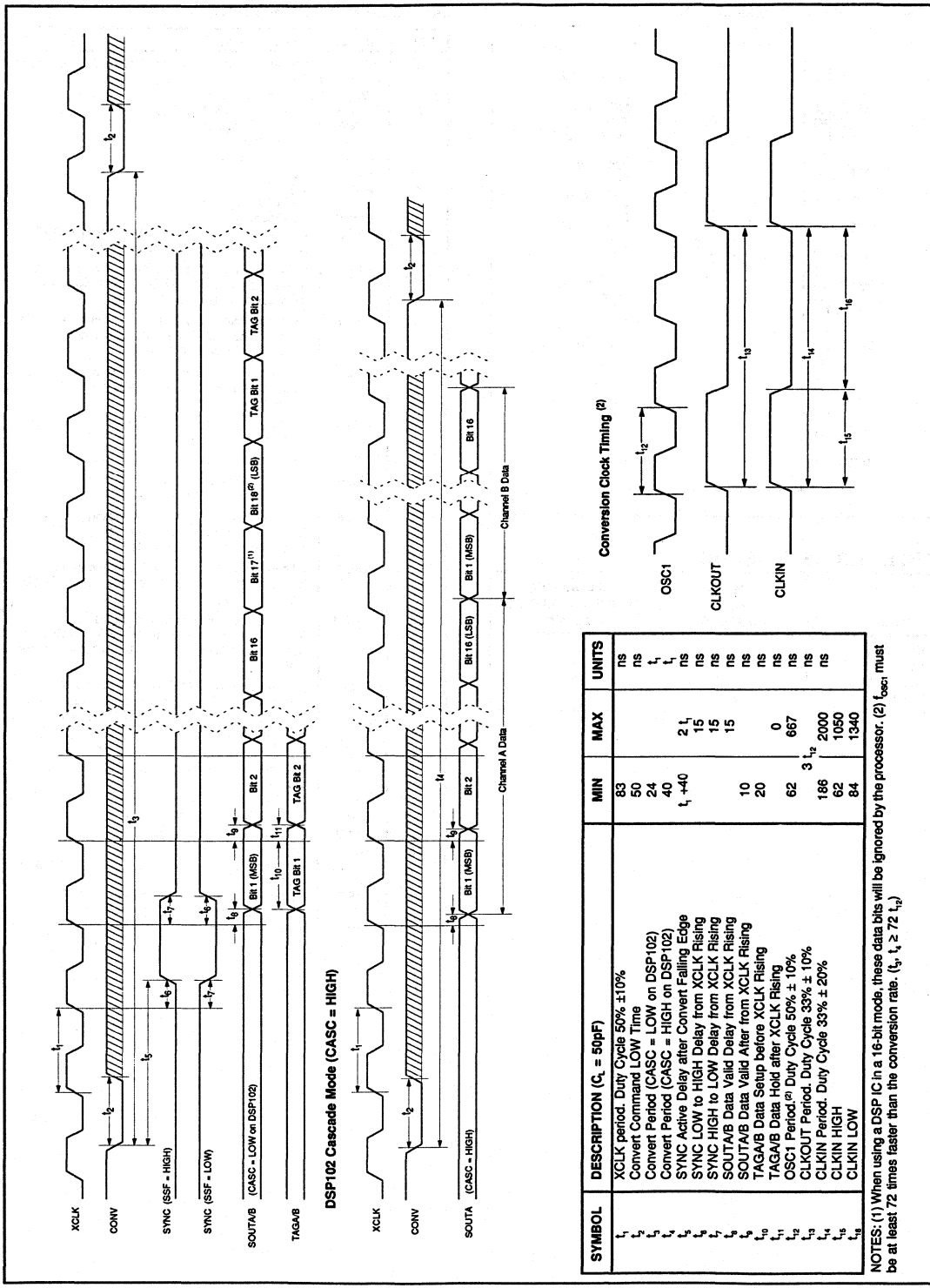


ORDERING INFORMATION

MODEL	NUMBER OF CHANNELS	SIGNAL-TO-(NOISE + DIST.) RATIO dB min
DSP101JP	1	83
DSP101KP	1	86
DSP102JP	2	83
DSP102KP	2	86

DSP102 PIN ASSIGNMENTS

PIN #	NAME	DESCRIPTION
1	VPOTA	Channel A Trim Reference Out. 10µF Tantalum to AGND.
2	VINA	Channel A Analog In.
3	MSBA	Channel A MSB Adjust In.
4	VOSA	Channel A VOS Adjust In.
5	V_A-	–5V Analog Power.
6	V_A+	+5V Analog Power.
7	DGND	Digital Ground.
8	DGND	Digital Ground.
9	V_D	+5V Digital Power.
10	CLKIN	Conversion Clock In.
11	CLKOUT	Conversion Clock Out. Can drive multiple DSP101/DSP102s to synchronize conversion.
12	SSF	Select Synch Format In. If HIGH, SYNC will be active High. If LOW, SYNC will be active Low. See timing diagram (Figure 1).
13	OSC1	Oscillator Point 1 Input / External Clock In. If using external clock, drive with 74HC logic levels. Connect to DGND if not used.
14	OSC2	Oscillator Point 2 Output. Provides drive for crystal oscillator. Make no electrical connection if using external clock.
15	SYNC	Data Synchronization Out. Active High when SSF is HIGH; active Low when SSF is LOW.
16	XCLK	Data Transfer Clock In.
17	SOUTB	Channel B Serial Data Out. MSB first, Binary Two's Complement format.
18	TAGA	Channel A User Tag In. Data clocked into this pin is appended to the conversion results of SOUTA. See timing diagram (Figure 1).
19	TAGB	Channel B User Tag In. Data clocked into this pin is appended to the conversion results of SOUTB. See timing diagram (Figure 1).
20	SOUTA	Channel A Serial Data Out. MSB first, Binary Two's Complement format. If CASC is HIGH, 32 bits of data output, with first 16 bits being Channel A data.
21	CONV	Convert Command In. Falling edge puts converter into hold state, initiates conversion, and transmits previous conversion results to DSP IC with appropriate SYNC pulse.
22	CASC	Select Cascade Mode In. If HIGH, DSP102 transmits a 32-bit word on SOUTA, with the first 16 bits being data on Channel A. If LOW, DSP102 transmits data for both channels simultaneously.
23	VOSB	Channel B VOS Adjust In.
24	MSBB	Channel B MSB Adjust In.
25	VINB	Channel B Analog In.
26	VPOTB	Channel B Trim Reference Out. 10µF Tantalum to AGND.
27	REF	Reference Bypass. 0.1µF Ceramic to AGND.
28	AGND	Analog Ground.



SYMBOL	DESCRIPTION (C_L = 50pF)	MIN	MAX	UNITS
t_1	XCLK period. Duty Cycle 50% ±10%	83		ns
t_2	Convert Command LOW Time	50		ns
t_3	Convert Period (CASC = LOW on DSP102)	24		t_1
t_4	Convert Period (CASC = HIGH on DSP102)	40		t_1
t_5	SYNC Active Delay after Convert Falling Edge	t_1 +40	2 t_1	ns
t_6	SYNC LOW to HIGH Delay from XCLK Rising		15	ns
t_7	SYNC HIGH to LOW Delay from XCLK Rising		15	ns
t_8	SOUTA/B Data Valid Delay from XCLK Rising		15	ns
t_9	SOUTA/B Data Valid After from XCLK Rising	10		ns
t_{10}	TAGA/B Data Setup before XCLK Rising	20		ns
t_{11}	TAGA/B Data Hold after XCLK Rising		0	ns
t_{12}	OSC1 Period.(2) Duty Cycle 50% ± 10%	62	667	ns
t_{13}	CLKOUT Period. Duty Cycle 33% ± 10%		3 t_{12}	ns
t_{14}	CLKIN Period. Duty Cycle 33% ± 20%	186	2000	ns
t_{15}	CLKIN HIGH	62	1050	
t_{16}	CLKIN LOW	84	1340	

NOTES: (1) When using a DSP IC in a 16-bit mode, these data bits will be ignored by the processor. (2) f_{OSC1} must be at least 72 times faster than the conversion rate. (t_3, $t_4 \geq 72\ t_{12}$)

FIGURE 1. DSP101 and DSP102 Timing.

THEORY OF OPERATION

The DSP101 and DSP102 are sampling analog-to-digital converters optimized for handling dynamic signals. They have complete logic interface circuitry for ease of use with standard digital signal processing ICs, and transmit data words in a serial stream. The successive approximation conversion architecture is combined with an inherently sampling switched capacitor array to provide maximum user flexibility over sampling and conversion timing.

The DSP101 and DSP102 are pipelined internally. When the user gives a convert command at time (t), two actions are initiated. First, the internal sample/holds are switched to the hold state, and a conversion cycle is initiated. At the same time, the DSP101 or DSP102 transmits a synchronization pulse and starts shifting out the conversion results from the previous convert command at (t-1) using the system bit clock. The data from the conversion at time (t) is shifted out of the converter after the next convert command is received.

Both the DSP101 and the DSP102 are 18-bit A/Ds internally. When the DSP IC is programmed to accept 16-bit word lengths, the processor will ignore the last two data bits transmitted from the DSP101 or DSP102. A Cascade Mode on the DSP102 can be invoked to transmit data for both conversion channels over a single serial line as a 32-bit word. In this mode, the first 16 bits of data transmitted after the Sync pulse contain data from channel A, followed by 16 bits of information from channel B, allowing a single 32-bit word to contain data for both channels.

A unique Tag feature allows additional digital data to be appended to the conversion results, so that a single data word contains conversion results plus other signal information, such as gain settings or multiplexer channel settings in front of the converter.

The DSP101 and DSP102 are high-resolution A/D converters complete with sampling capability and on-board references. They can acquire and convert analog signals at up to a 200kHz sampling rate. Both operate from ±5V supplies, and have full-scale analog input ranges of ±2.75V.

BASIC OPERATION

Figure 2 shows the minimum connections required to operate the DSP101. The falling edge of a convert command on pin 21 puts the internal sampling capacitor array into the hold state. The falling edge on pin 21 also starts the process to initiate a conversion and transmit data from the previous conversion, synchronizing both appropriately to the 10MHz clock input on pin 13. Figure 1 shows the timing relationship between the convert command, the output data, and the synchronization pulse.

In this basic system, the 10MHz clock is used both to generate a 3.33MHz conversion clock and as the data transfer bit clock for outputting data. Per Figure 1, there must be at least 72 clock pulses on pin 13 between convert commands, so that this circuit can sample and convert at up to 138kHz.

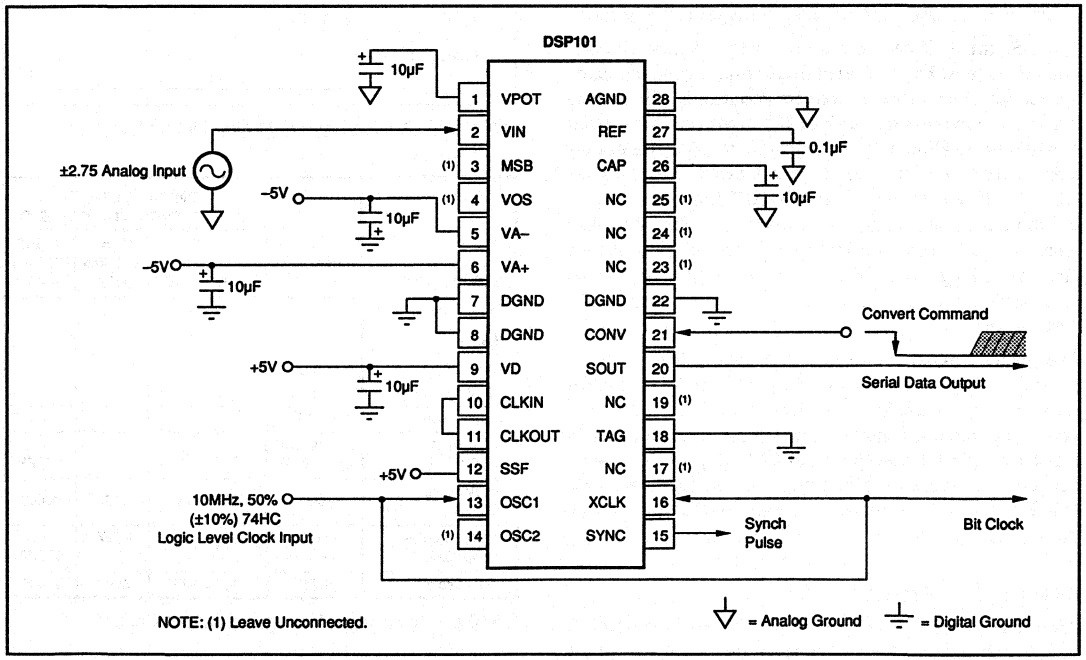


FIGURE 2. DSP101 Basic Operation.

The convert command at pin 21 causes a Sync pulse to be output on pin 15, followed by the data from the previous conversion output on pin 20. The Sync pulse will be HIGH for one bit clock cycle, since pin 12 is tied HIGH. (A LOW Sync pulse will be output on pin 15 if pin 12 is tied LOW.) Data is serially transmitted in an MSB-first data stream, in Binary Two's Complement format. Both the Sync pulse (pin 15) and the data stream (pin 20) are synchronized to the bit clock (at pins 13 and 16), with the timing relationships shown in Figure 1.

After the 18 bits of data from the previous conversion have been transmitted, pin 20 will continue to clock out LOWs until a new convert command restarts the process, since pin 18 (the Tag input) is grounded. If pin 18 is tied HIGH, pin 20 will clock out HIGHs between conversion cycles.

CONVERSION

A falling edge on pin 21 (CONV) puts the internal sampling capacitors in the hold state with minimum aperture jitter, initiates a conversion synchronized to the conversion clock, and outputs the data from the previous conversion with an appropriate Sync pulse. On the DSP102, a single convert command simultaneously samples both channels. The timing relationship between the convert command, Sync and the output data is shown in Figure 1. Both Sync and the output data are synchronized to XCLK, the system bit clock. Following a convert command falling edge, pin 21 must be held LOW at least 50ns.

Convert commands can be sent to the DSP101 and DSP102 completely asynchronous to other clocks in the system. This allows external events to be used to trigger conversions.

From Figure 1, it can be seen that two different clocking conditions must be considered in determining the minimum acceptable time between convert commands. First, there need to be a minimum of 24 XCLK periods between convert commands, to allow internal synchronization and transmission of Sync and the data. (In the Cascade Mode on the DSP102, there need to be at least 40 XCLK periods between convert commands, to allow transmission of the 32-bit data words.) When used with DSP processors programmed for data words longer than 16-bits, the transmission time to the processor may determine the minimum time between convert commands.

The second limitation on convert commands is the requirement that the internal analog-to-digital converter be given enough time to complete a conversion, shift the data to the output register, and acquire a new sample. This condition is met by having a minimum of 24 CLKIN periods between convert commands, or a minimum of 72 clock cycles on OSC1, if it is used to generate the conversion clock (CLKOUT driving CLKIN).

SIGNAL ACQUISITION

After a conversion is completed, the DSP101 or DSP102 will switch back to the sampling mode. With at least 24 CLKIN periods between convert commands, the A/D will have had sufficient time to acquire a new input sample to full rated accuracy.

DATA FORMAT AND INPUT LEVELS

The DSP101 and DSP102 output serial data, MSB first, in Binary Two's Complement format. In the Cascade Mode on the DSP102, the serial data will first contain 16 bits of data for channel A, MSB-first, followed by channel B data, again MSB-first. The analog input levels that generate specific output codes are shown in Table I.

As with all standard A/Ds, the first output transition will occur at an analog input voltage 1/2 LSB above negative full scale (–2.75V + 1/2 LSB) and the last transition will occur 3/2 LSB below positive full scale (+2.75V – 3/2 LSB.) See Figure 3.

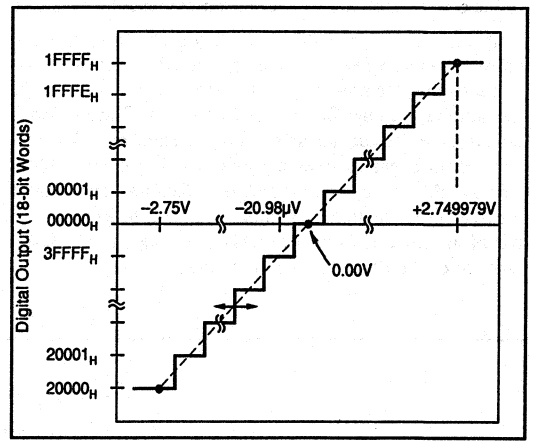


FIGURE 3. Analog Input to Digital Output Diagram.

DESCRIPTION	ANALOG INPUT	DIGITAL OUTPUT (BINARY TWO'S COMPLEMENT) BINARY CODE	16-BIT WORDS (HEX)	18-BIT WORDS (HEX)
Least Significant Bit (LSB = $\frac{5.5V}{2^n}$)				
16-bit Words	84µV			
18-bit Words	21µV			
Input Range	±2.75V			
+ Full Scale (2.75V–1LSB)	+2.749916V +2.749979V	011...111	7FFF	1FFFF
Bipolar Zero (Midscale)	0V	000...000	0000	00000
One LSB below Bipolar Zero	–84µV –21µV	111...111	FFFF	3FFFF
– Full Scale	–2.75V	100...000	8000	20000

TABLE I. Ideal Input Voltage vs Output Code.

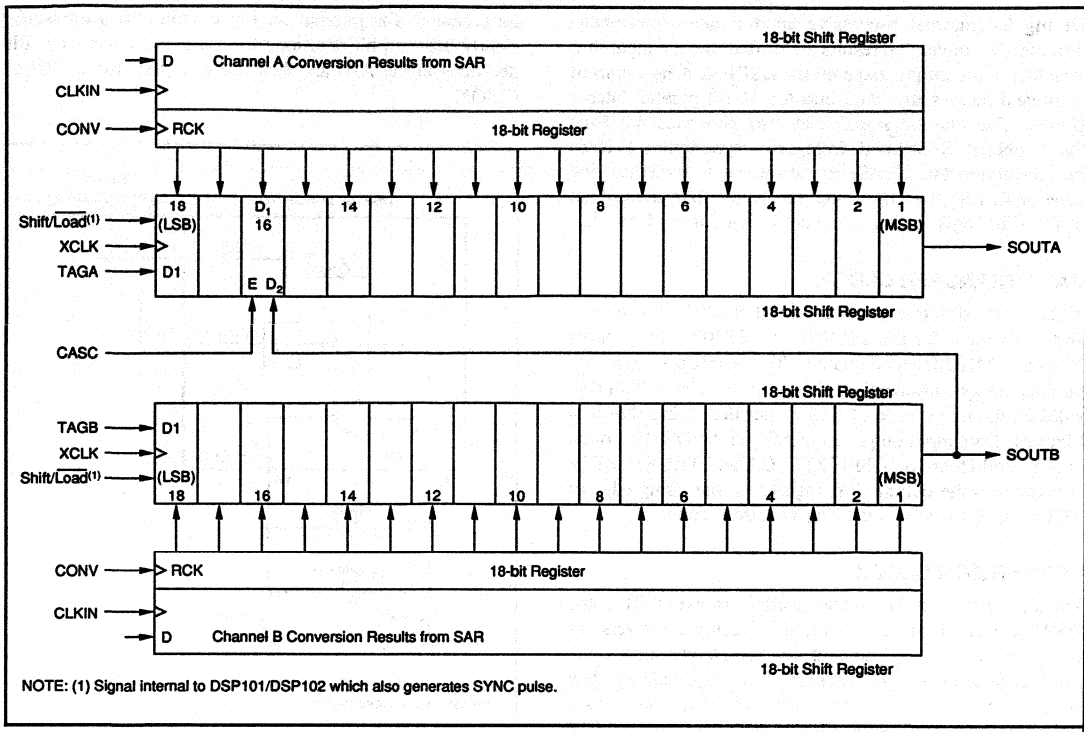


FIGURE 4. Output Structure of DSP102.

DATA TRANSFER

The internal A/Ds generate 18 bits of data, transmitting the data MSB first. When read by a DSP IC programmed to accept 16 bits of data, the first 16 MSB bits of data from the DSP101, or each channel of the DSP102, will be shifted into the processor's input shift register, and the last two least significant bits of data from the A/D will be ignored, although they will still be present on the serial data line. When the DSP processor is programmed to accept words of more than 16-bit length (typically 24-bit or 32-bit), the DSP101 and DSP102 will transmit the full 18-bit conversion results, after which the information input on the TAG input (or TAGA and TAGB on the DSP102) will be appended to the output word. (See Tag Feature below.)

In the Cascade Mode, the DSP102 will first transmit the 16 MSBs from channel A, followed by the full 18-bits from channel B, although DSP processors programmed to accept 32 bits of data will ignore the final two bits of information on Channel B. See the DSP102 Cascade Mode section below for details of the Cascade mode.

DATA SYNCHRONIZATION

A convert command both initiates a conversion and starts the process for transmitting data from the previous conversion. Convert commands can come at any time, completely asynchronous to the conversion clock or the bit clock, and the conversion clock may also be independent of the bit clock. The DSP101 and DSP102 internally synchronize the output data, Sync pulse, and Tag inputs to the bit clock.

While the convert command, conversion clock and bit clock can be asynchronous, system performance is usually enhanced by synchronizing all of them to a system master clock, whenever the application permits. This minimizes changes in digital loads and currents when the critical S/H transition and A/D bit decisions are occurring. Within the DSP101 and DSP102 themselves, running asynchronous convert commands, conversion clocks and bit clocks typically degrades performance only several dB, as shown in the various typical performance curves, but the system board design can easily have more effect.

When a convert command is received, the internal logic generates an appropriate Sync pulse, synchronized to XCLK, as shown in Figure 1. The output Sync pulse will be active High or active Low depending on whether a HIGH or a LOW, respectively, is input at SSF (pin 12).

The convert command also causes the conversion results from the previous conversion to be loaded into the output shift register, synchronous to XCLK. Figure 4 shows the operation of the internal data shift registers on the DSP102. The DSP101 is basically similar, but includes only the top of the figure, showing the SOUTA path.

During the internal successive approximation conversion process, the conversion results are shifted into the input shift registers of the output stage on the DSP102. A new convert command latches that data into the 18-bit parallel latches shown. The internal signal that also generates the Sync pulse, labeled "Shift/Load" in Figure 4, synchronously loads the conversion data into the output shift register on the rising edge of XCLK. The conversion results are then clocked out of the shift register on subsequent rising edges of XCLK.

DATA TRANSFER CLOCK

XCLK is the data transfer clock, or bit clock, for the system, and is an input for the DSP101 or DSP102. This input is TTL- and 74HC-level compatible. The serial data and SYNC outputs are synchronized internally to this clock, with data valid on the rising edge of XCLK, per the timing shown in Figure 1. Data input on pin 18 (TAG) on the DSP101, or on pins 18 and 19 on the DSP102 (TAGA and TAGB), will be clocked into the output shift register on the rising edge of XCLK, as discussed in the Tag Feature section.

CONVERSION CLOCK

The analog-to-digital converter sections in the DSP101 and DSP102 were designed to provide accurate conversions under worst case conditions of supplies, temperatures, etc. In order to achieve a full 200kHz sampling capability, they were designed to use a 33% duty cycle conversion clock (CLKIN on pin 10) as shown in Figure 1. The clock is LOW long enough for internal analog circuitry to settle sufficiently between bit decisions to insure rated accuracy. Bit decisions in the A/D are then made on the rising edge of CLKIN.

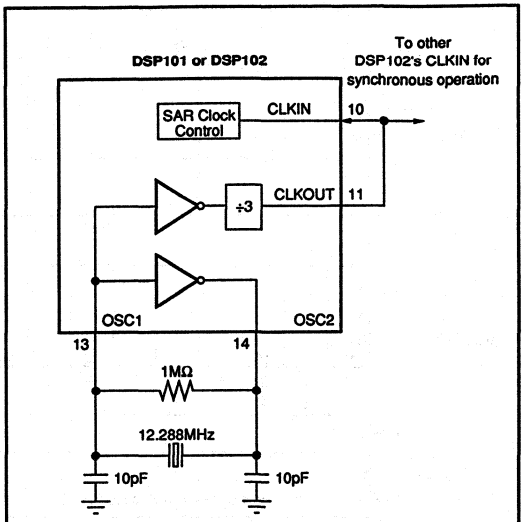


FIGURE 5. DSP101 or DSP102 Conversion Clock Circuit.

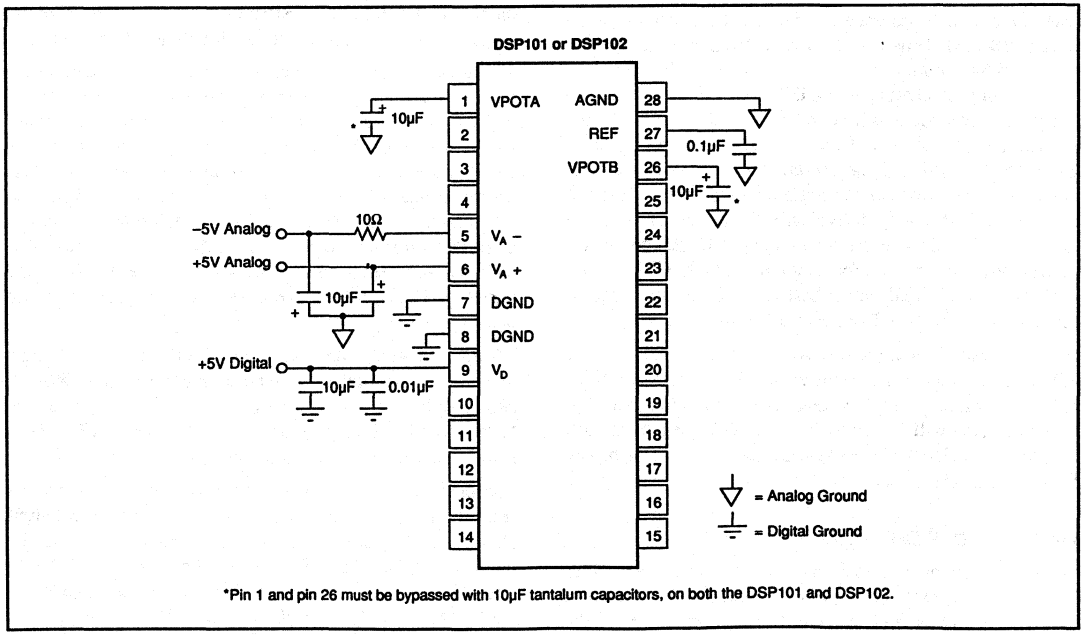


FIGURE 6. DSP101 or DSP102 Power Supply Connections.

When a convert command is received, the DSP101 or DSP102 immediately switches the sampling capacitors to the hold state, and then internally gates the conversion clock to the A/D appropriately. Allowing a minimum of 24 CLKIN pulses between conversions insures that there is sufficient time for complete, accurate conversions, and allows the input sampling capacitor to fully acquire the next sample, regardless of the timing between the convert command and CLKIN.

In most applications, CLKIN (pin 10) can be driven from a 50% duty cycle clock without performance degradation. During characterization of the DSP101 and DSP102, the performance of a number of parts was measured under various conditions with a 4.8MHz, 50% duty cycle input to CLKIN at a full 200kHz conversion rate without noticeable degradation.

OSCILLATOR INPUTS AND CLKOUT

The DSP101 or DSP102 can generate a 33% duty cycle conversion clock output on CLKOUT (pin 11). This is accomplished by dividing by three a clock from either an external 74HC-level clock or from a crystal oscillator. CLKOUT can deliver ±2mA, and can be used to drive multiple DSP101 or DSP102 CLKINs. See Figure 1 for the timing relationship between OSC1 and CLKOUT.

To use an external 74HC-level clock, drive the clock into OSC1 (pin 13), and leave OSC2 (pin 14) unconnected.

To use a crystal oscillator to generate the conversion clock, refer to Figure 5. Connect the oscillator between OSC1 and OSC2. OSC2 provides the drive for the crystal oscillator. This pin cannot be used elsewhere in the system.

If CLKOUT is not used, both it and OSC2 should be left unconnected, and OSC1 should be grounded.

TAG FEATURE

Figure 4 shows the implementation of the TAG feature on the DSP101 and DSP102. When a convert command is received, the internal Shift/$\overline{\text{Load}}$ signal loads conversion result data into the output shift register synchronous to XCLK. Between convert commands, the information input on TAG (on the DSP101) or on TAGA and TAGB (on the DSP102) will be clocked into the output shift register on the rising edges of XCLK. Since this is an 18-bit shift register, the data input on the Tag lines will be output on SOUT (DSP101) or SOUTA and SOUTB (DSP102) delayed by 18 bit clocks.

The Tag Feature can be used in various ways. The Tag inputs can be tied HIGH or LOW to differentiate between two converters in a system. As discussed in the Applications section below, the Tag feature can be used to append to the serial output data word information on multiplexer channel address, or other digital data related to the input signal (such as the setting on a programmable gain amplifier.) Another option would be to daisy-chain multiple DSP101 or DSP102 converters, linking the serial output of one to the Tag input of the next. This can simplify the transmission of data from multiple A/Ds over a single optical isolation channel.

DSP102 CASCADE MODE

If pin 22 (CASC) is tied HIGH, the DSP102 will be in the Cascade Mode. In this mode, when a convert command is received, the DSP102 will transmit a 32-bit data word on pin

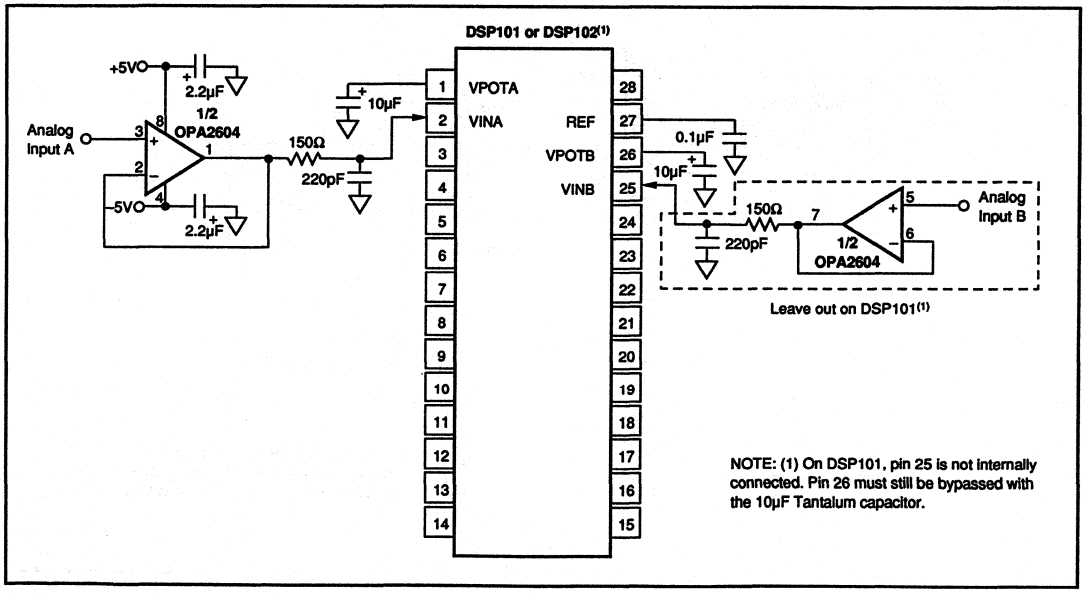


FIGURE 7. DSP101 or DSP102 Input Buffering.

20 (SOUTA) containing data for both input channels in two 16-bit words. Referring to Figure 1, the first 16 bits of data will be the results for channel A, followed by 16 bits of information for channel B. The data will be transferred MSB first. A convert command at time (t) will initiate the transmission of the results of the conversion initiated at time (t – 1).

From the descriptions above of the internal shift registers shown in Figure 4, it can be seen that the DSP102 in the Cascade Mode actually continues to shift out data after the 32nd bit of the data word. The next two bits clocked out will be the last two data bits from the full 18-bit conversion on channel B, after which the information output on SOUTA will be the information clocked into TAGB 35 bit clock cycles earlier.

In the Cascade mode on the DSP102, SOUTB will still output channel B conversion data and tag data as usual.

ANALOG PERFORMANCE

LINEARITY

The DSP101 and DSP102 are optimized for signal processing applications with wide dynamic range requirements. Linearity is trimmed for best performance in the range around 0V, which is critical for handling low amplitude signals. The DSP101 and DSP102 typically have integral and differential non-linearity below ±0.003% in the input range of ±0.7V, with there being no missing codes at the 14-bit level in this range. Over the full ±2.75V input range, the largest non-linearities are centered around the bit #2 transition points at +1.375V and –1.375V levels.

NOISE AND BIPOLAR ZERO ERROR

The equivalent input noise and bipolar zero error of the DSP101 and DSP102 is shown in the typical performance section for both channels on a DSP102. The inputs to both channels were grounded, and the results of 5,000 conversions was recorded. The data shown is binned at the 16-bit level. The noise results from all sources in the circuit, including clocks, reference noise, etc.

In a theoretically ideal converter with no offset and no noise, the results of all 5,000 conversion for each channel would lie in the bin corresponding to bipolar zero, code 0000. The typical DSP101 or DSP102 will have offset errors in the range of 1 to 2mV, and the two channels on the DSP102 will be matched closer than 2mV. The DSP102 shown in the typical performance section has the worst offset, –0.8mV, on channel A, with channel B being less than 1mV different, and the three sigma noise on either channel being less than 250µV.

INPUT BANDWIDTH

From the typical performance curves, it can be seen that there is very little degradation in Signal-to-(Noise + Distortion) for input signals up to 100kHz. The wideband sampling input typically maintains a 60dB Signal-to-(Noise + Distortion) Ratio undersampling 500kHz input signals.

LAYOUT CONSIDERATIONS

Because of the high resolution, linearity and speed of the DSP101 and DSP102, system design problems such as ground path resistance, contact resistance and power supply quality become very important.

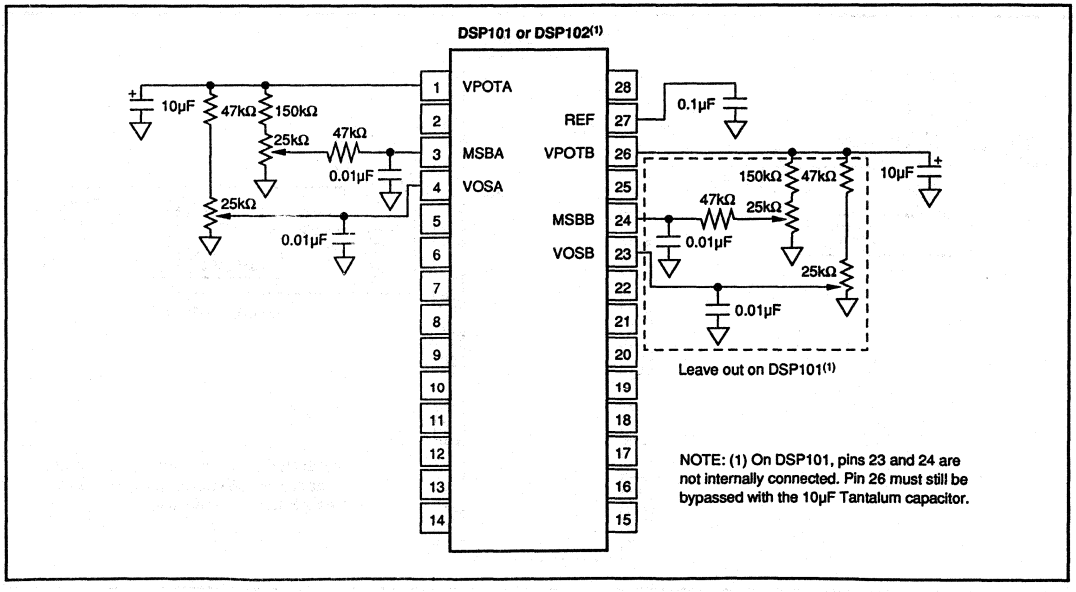


FIGURE 8. DSP101 or DSP102 Optional MSB and Offset Adjust.

Optimal dynamic performance is achieved by soldering the parts directly into boards, to keep the A/Ds as close as possible to ground. The use of sockets will often degrade AC performance. Zero-Insertion-Force sockets are particularly poor because longer lead lengths create inductance.

Short traces on the board, and bypass capacitors as close as possible to the A/D, will further improve dynamic performance.

GROUNDS

To achieve the maximum performance from the DSP101 or DSP102, care should be taken to minimize the effect of changes in current flowing in the system grounds, particularly while bit decisions are being made in the successive approximation converter's comparator. Pin 28 (AGND) on both the DSP101 and the DSP102 is the most critical, and care should be taken to make this pin as close as possible to the same potential as the system analog ground.

Whenever possible, it is strongly recommended that separate analog and digital ground planes be used. With an LSB level of 84µV at the 16-bit level, and one-quarter of that at the 18-bit level, the currents switched in a typical DSP system can easily corrupt the accuracy of the A/Ds unless great care is taken to analyze and design for current flows.

POWER SUPPLY DECOUPLING

All of the supplies should be decoupled to the appropriate grounds using tantalum capacitors in parallel with ceramic capacitors, as shown in Figure 6. For optimum performance of any high resolution A/D, all of the supplies should be as clean as possible. If separate digital and analog supplies are available in a system, care should be taken to insure that the difference between the analog and the digital supplies is not more than 0.5V for more than a few hundred milliseconds, as may occur at power-on.

INPUT SIGNAL CONDITIONING

To avoid introducing distortion, the DSP101 and DSP102 analog inputs must be driven by a source with low impedance over the input bandwidth needed in the application. Op amps such as the NE5532 or Burr-Brown's OPA2604 work well over audio bandwidths. Figure 7 shows an appropriate input driver circuit. The 150Ω and 220pF shown on the input help reduce the dynamic load on the input signal conditioning amp in front of the A/D, since all switched capacitor array architectures exhibit fast changes in input current load as the input sampling switch is opened and closed. These dynamic changes in the load can affect any signal conditioning circuit at the input. Other R and C combinations can be

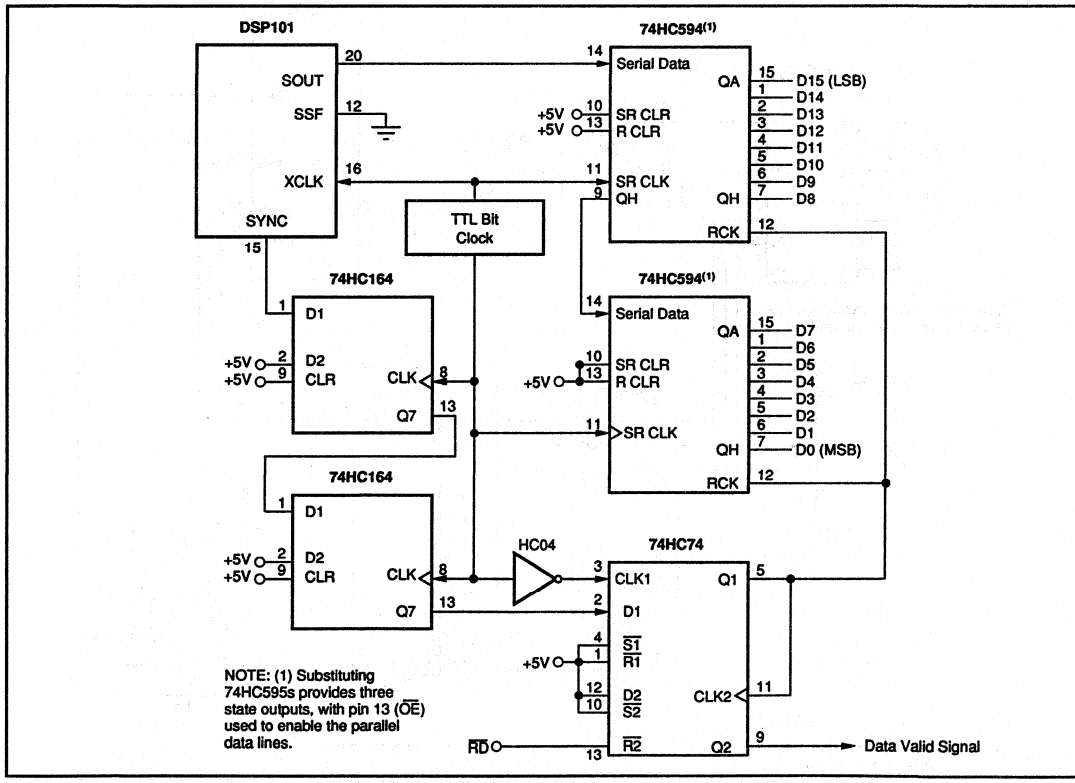


FIGURE 9. Driving a 16-bit Parallel Port from the DSP101.

used, but the resistor should not exceed 200Ω, or the output settling time of the signal conditioning amplifier may be too long.

EXTERNAL ADJUSTMENTS

All of the specifications for the DSP101 and DSP102, plus the typical performance curves, are based on the performance of these A/Ds without external trims. In most applications, external trims are not required.

OFFSET ADJUST

Where required by specific applications, offsets can be adjusted using Figure 8. When not adjusted, VOS (pin 4) on the DSP101, and VOSA (pin 4) and VOSB (pin 23) on the DSP102, should be left open. If these pins are connected to traces on the board, they should be bypassed to ground with 0.01µF capacitors, as close as possible to the A/D.

To trim offset, one alternative is to ground the analog input while converting continually. Then adjust the trimpot (on VOS for the DSP101, on VOSA and VOSB for the DSP102) until the output code is toggling between the codes FFFF and 0000 (Hex) at the 16-bit level (3FFFF and 00000 at the 18-bit level.) This will center the offset at 1/2 LSB below 0V, which is respectively –42µV or –10µV at the 16- and 18-bit levels.

The offset can also be adjusted by providing a sine wave to the A/D input. Using FFT, or even simple averaging of several thousand conversion results at a time, the trimpots can be adjusted until there is no DC offset of the signal.

Grounding the input, or providing the sine wave, as far in front of the A/D as possible allows offset from intervening signal conditioning components to be also corrected by this procedure.

MSB ADJUST

In most applications, adjustment of the Most Significant Bit weight will not be required. When not adjusted, MSB (pin 3) on the DSP101, and MSBA (pin 3) and MSBB (pin 24) on the DSP102, should be left open. If these pins are connected to traces on the board, they should be bypassed to ground with 0.01µF capacitors, as close as possible to the A/D.

MSB (pin 3) on the DSP101, and MSBA (pin 3) and MSBB (pin 24) on the DSP102, are internally connected to a resistor divider network that is used to laser-trim the weight of the MSB capacitor in the CDAC. These pins are nomi-

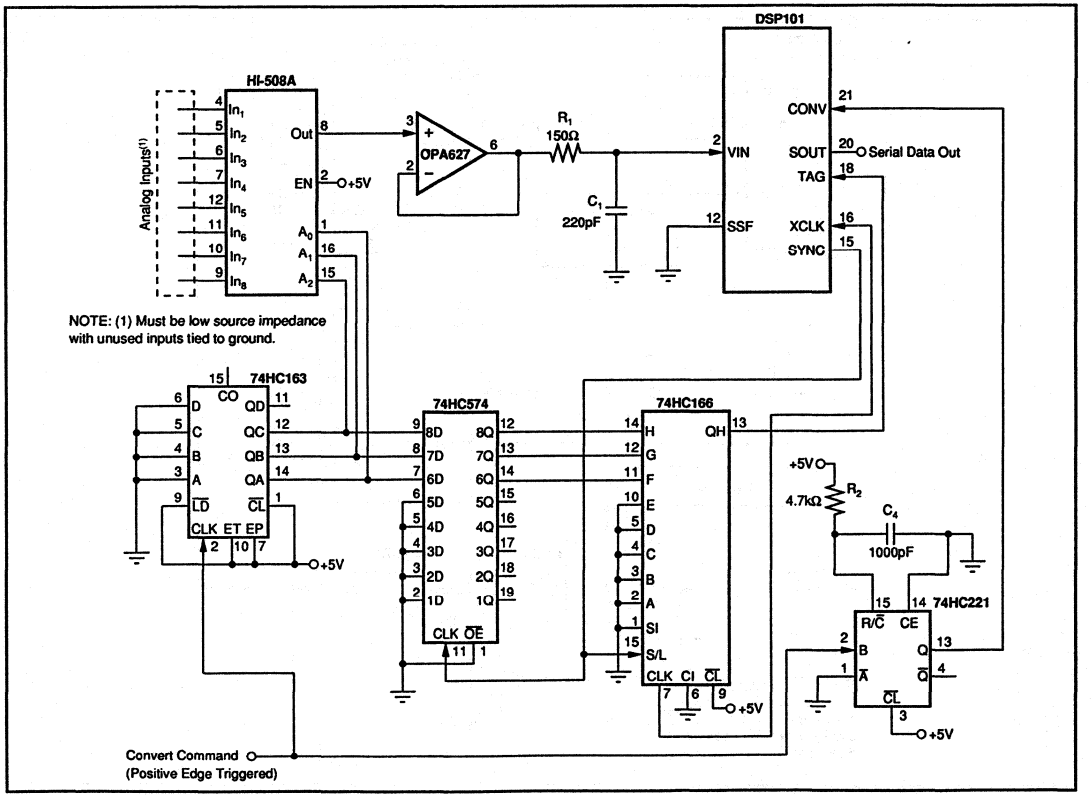


FIGURE 10. A Complete Eight-Channel Analog Input System Using the DSP202 and the HI-508A.

nally at +100mV after laser-trimming during manufacturing. They can handle external inputs up to about one diode drop below ground (–0.6V) before internal clamping circuitry is triggered.

Figure 8 shows an appropriate circuit for adjusting the weight of the most significant bit to minimize differential non-linearity at the critical major-carry transition. To adjust, provide a small amplitude sine wave to the selected A/D input pin while converting continually, and adjust for maximum Signal-to-(Noise + Distortion) ratio, using appropriate signal analysis software.

GAIN ADJUST

If circuit gain needs to be adjusted in hardware, rather than in system software, appropriate trimpots should be included in the analog signal conditioning section in front of the DSP101 or DSP102. No specific gain adjust circuitry is included in the parts.

APPLICATIONS

INTERFACING DSP101 TO PARALLEL PORTS

Figure 9 shows a circuit for converting the serial output data from the DSP101 into 16 bits of parallel data, within the timing constraints of the serial bit-stream from the DSP101. In many applications, this circuit can be easily incorporated into gate arrays or other programmed logic circuits already used in the system, since the extra gate count is not high.

This circuit adds an additional pipeline delay to the conversion data, so that the parallel data from a conversion at time (t) is valid one conversion cycle plus 17 XCLK clocks later (at t+1 plus 17 times XCLK). A convert command at time (t+1) generates a Sync and begins transmitting serial data from SOUT. The serial data is shifted into the 74HC594 shift registers, and Sync is shifted through the 74HC164 shift registers. The Q1 output of the 74HC74 dual D-type flip-flops clocks the conversion data into the output register of the 74HC594s, and triggers a data valid signal on its Q2 output. The user can then read the data at any time before the next conversion is started, and the Read signal will reset the data valid output from Q2.

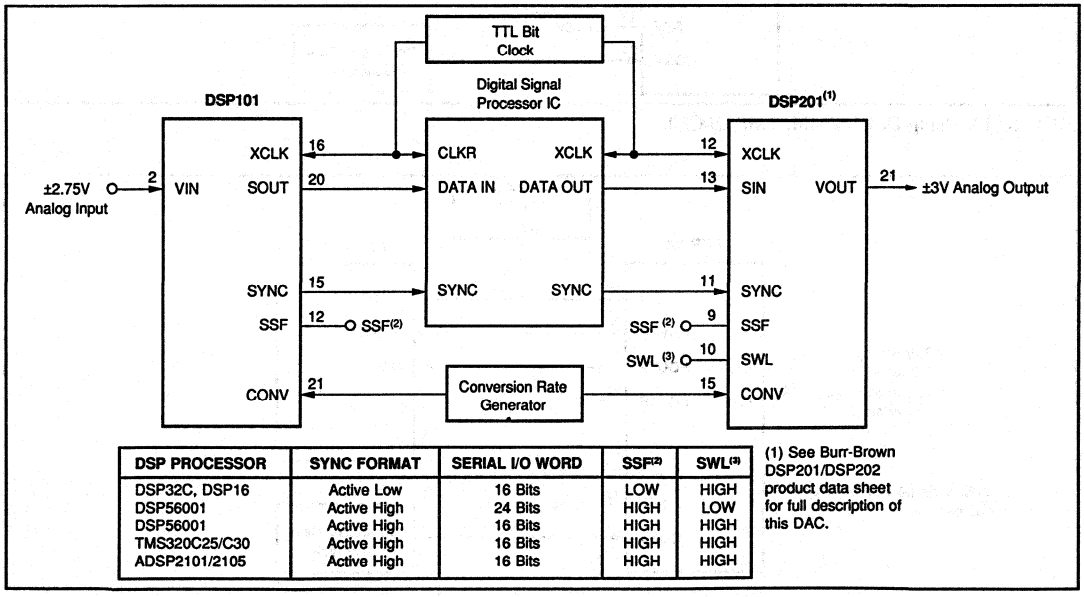
In many systems, galvanic isolation of signals is required. Using opto-couplers on the serial data lines in Figure 9 allows a fully isolated system to be built using a DSP101 and only three couplers across the barrier (for serial data, XCLK and SYNC.)

MULTIPLEXING INPUTS TO THE DSP101

Figure 10 shows a complete circuit for sequentially scanning eight analog input channels with a single DSP101, and using the Tag feature on the DSP101 to append the multiplexer channel address to the serial output conversion results.

The circuit in Figure 10 includes the required digital logic and timing logic. The 74HC163 counter provides the scan sequence to the Burr-Brown HI-508A analog multiplexer. In order to allow the HI-508A enough time to switch to the next channel and settle before the DSP101 begins a conversion, a 74HC221 one-shot introduces a 3µs delay for the DSP101 convert command input.

The Burr-Brown OPA627 provides a low impedance source for the DSP101, buffering it from the output impedance of



DSP PROCESSOR	SYNC FORMAT	SERIAL I/O WORD	SSF[2]	SWL[3]
DSP32C, DSP16	Active Low	16 Bits	LOW	HIGH
DSP56001	Active High	24 Bits	HIGH	LOW
DSP56001	Active High	16 Bits	HIGH	HIGH
TMS320C25/C30	Active High	16 Bits	HIGH	HIGH
ADSP2101/2105	Active High	16 Bits	HIGH	HIGH

(1) See Burr-Brown DSP201/DSP202 product data sheet for full description of this DAC.

FIGURE 11. Analog Input and Analog Output System.

the multiplexer. This unity-gain buffer minimizes distortion, taking full advantage of the resolution and bandwidth of the DSP101.

The 74HC574D register delays the multiplexer address data by one conversion before appending the channel data to the serial conversion results from the DSP101. This attaches the channel address to the correct conversion results. Since the channel scanning shown in Figure 10 is sequential, this delay latch could be left out and software could recognize that the time (t) conversion results have the MUX address from the time (t-1) conversion appended. However, for systems using non-sequential scan lists, this delay latch is essential to maintain the conversion data and channel address integrity.

The 74HC166 synchronous loading shift register loads the channel address tag data into the shift register on the rising edge of the bit clock, in conjunction with the Sync output of the DSP101. The channel address tag data is then clocked into the DSP101 Tag input (pin 18) by the bit clock, while the conversion data is clocked out the other end of the DSP101 shift register (discussed in another section of this data sheet.)

Figure 10 was developed and tested using a Burr-Brown ZPB34 DSP board, which contains an AT&T DSP32C, so that the SYNC output is programmed to be active LOW. The circuit needs to be modified for DSP processors from ADI, TI, and Motorola, which use active HIGH Sync pulses. For these processors, tie SSF (pin 12) on the DSP101 HIGH, and use a 74HC04 hex inverter to invert the Sync signal to the 74HC574 and 74HC166.

The same basic circuit can be duplicated to drive two channels in a DSP102, or can be easily modified for more or less than eight channels of analog input.

USING DSP101 AND DSP102 WITH TEXAS INSTRUMENTS DSP ICS

Figures 11 thru 17 show various ways to use the DSP101 and DSP102 with DSP ICs from the Texas Instruments TMS320Cxx series. For simplicity, all of these circuits are

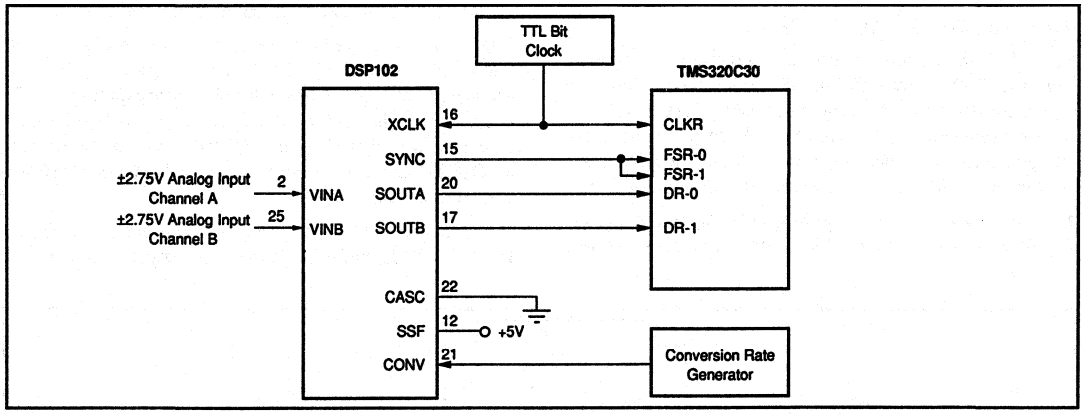


FIGURE 12. Using DSP102 with TMS320C30.

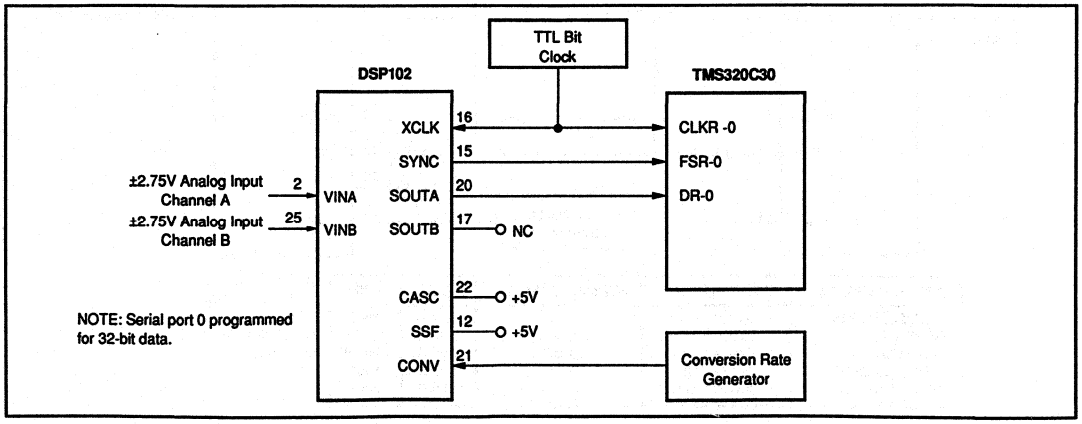


FIGURE 13. Using DSP102 with TMS320C30 in Cascade Mode.

based on using the TME320Cxx in the mode where SSF (Select Synch Format, pin 12) is tied HIGH, so that there is an active High synchronization pulse generated by the DSP101 or DSP102 after receiving a convert command. The synchronization pulse can be changed to active Low simply by making SSF LOW, where appropriate, without changing the basic operation of the A/Ds.

In all cases, the DSP101 and DSP102 will transmit data MSB-first, and the TMS320Cxx needs to be programmed for this.

Figure 11 shows a circuit for using the TMS320C25 or TMS320C30 in a complete analog input and analog output system using the DSP101 along with the Burr-Brown DSP201 D/A.

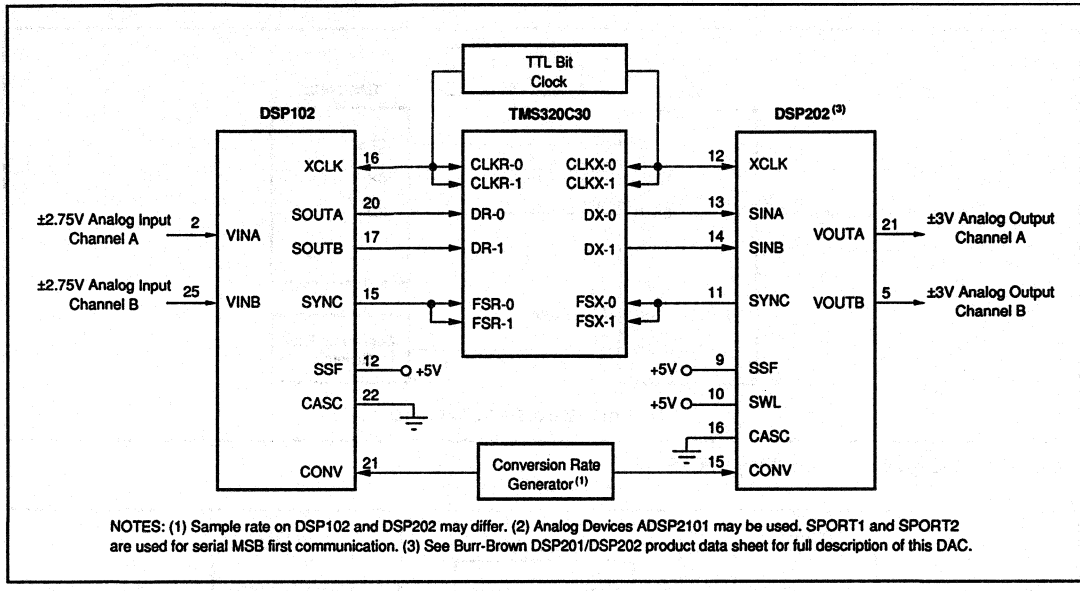


FIGURE 14. Two-Channel Analog Input and Output System with TMS320C30.

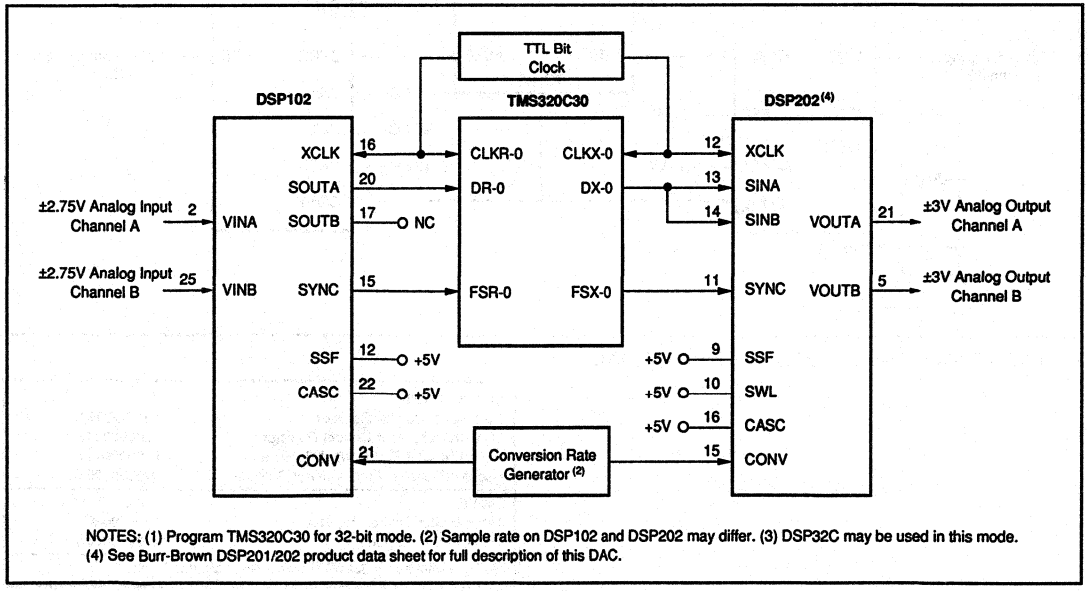


FIGURE 15. Two-Channel Analog Input and Output System with TMS320C30 in Cascade Mode.

USING TMS320C31 TO GENERATE ALL CONTROL SIGNALS

Figure 17 shows a circuit for using the TMS320C31 with a DSP102 and a Burr-Brown DSP202 D/A to provide a two channel analog I/O system. The flexibility of the TMS320C31 allows it to generate the data transfer clock (XCLK) and the Convert Command, minimizing additional circuitry and synchronizing the timing signals to the processor's master clock. In this circuit, the DSP102 and DSP202 are used in their Cascade modes, transmitting and receiving two channels of data in a single 32-bit word. (See the Cascade Mode section above.)

Table II shows how to set up the circuit in Figure 17 for a 44.1kHz conversion rate for both channels of the DSP102 A/D and both channels of the DSP202 D/A. Both inputs and outputs will be simultaneously converted.

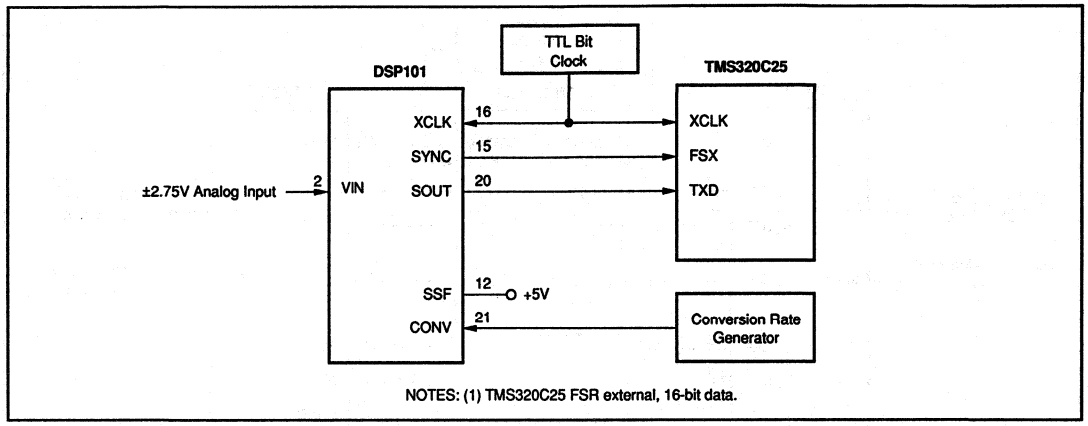


FIGURE 16. Using DSP101 with TMS320C25.

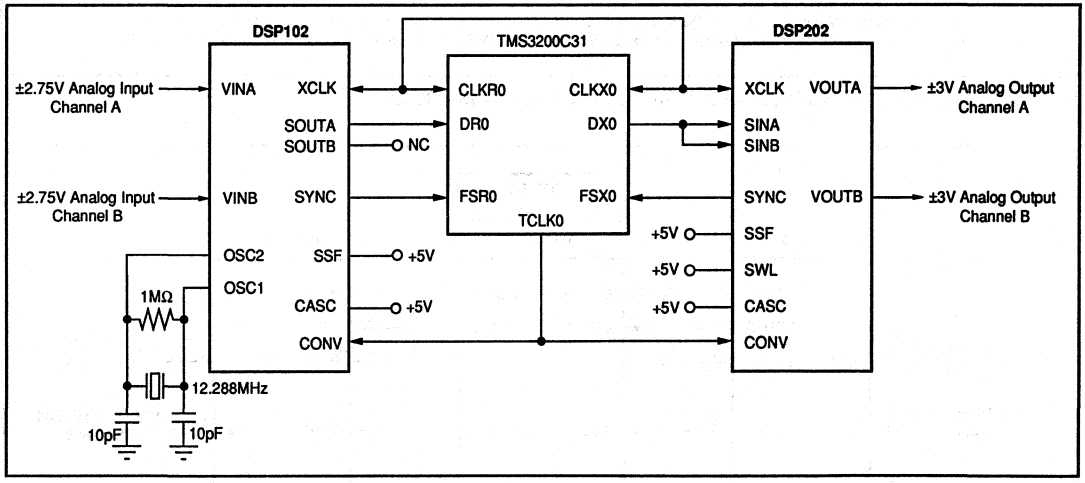


FIGURE 17. Two Channel Analog I/O Using TMS320C31.

SERIAL PORT	
Port Global Control Register	0x0EBC040
FSX/DX/CLKX Port Control Register	0x00000111
FSR/DR/CLKR Port Control Register	0x00000111
Receive/Transmit Timer Control Register	0x0000000F
TIMER	
Timer Global Control Register	0x000002C1
Timer Period Register	0x000000B5
NOTE: Assumes TMS320C31 has 32MHz Master Clock.	

TABLE II. TMS320C31 Register Settings for 44.1kHz Conversion Rate in Figure 17.

USING DSP101 AND DSP102 WITH MOTOROLA DSP ICS

Figure 18 shows how to use the DSP101 with a Motorola DSP56001. Using the DSP102 requires using two DSP56001s. The DSP56001 needs to be programmed to receive data MSB-first with SYNC in the Bit Mode.

SSF (pin 12) needs to be tied HIGH for using either the DSP101 or the DSP102 with DSP56001s. This will cause the DSP101 or DSP102 to transmit an appropriate active High synchronization pulse on SYNC (pin 15) after a convert command is received by the A/D. Timing is shown in Figure 1.

USING DSP101 AND DSP102 WITH AT&T DSP ICS

Figures 11, 19, 20, and 21 show how to use the DSP101 and DSP102 with the DSP16 and DSP32C in different modes. The AT&T processors need to be programmed to accept data MSB-first, and the DSP101 or DSP102 needs to have SSF (pin 12) tied LOW, so that an appropriate active Low synchronization pulse will be transmitted by the A/D after a convert command is received.

Figures 19 and 20 show the DSP32C and DSP16 respectively used with the DSP101 to handle a single analog input channel.

Figure 21 shows how to transmit to a single DSP32C conversion results from both DSP102 channels in a single 32-bit word, using the Cascade mode on the A/D.

Figure 11 indicates how to build a complete analog input and analog output system using a DSP32C or DSP16 with a DSP101 and a Burr-Brown DSP201 D/A.

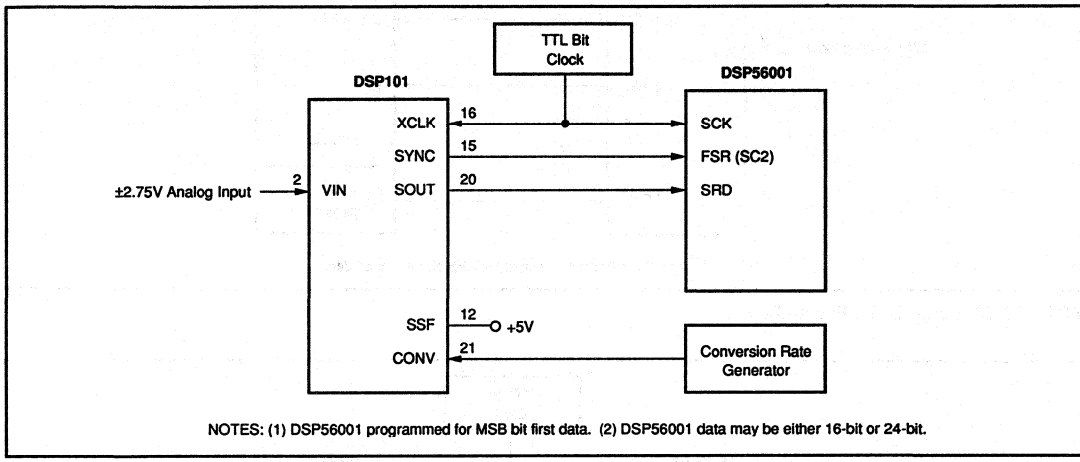


FIGURE 18. Using DSP101 with DSP56001.

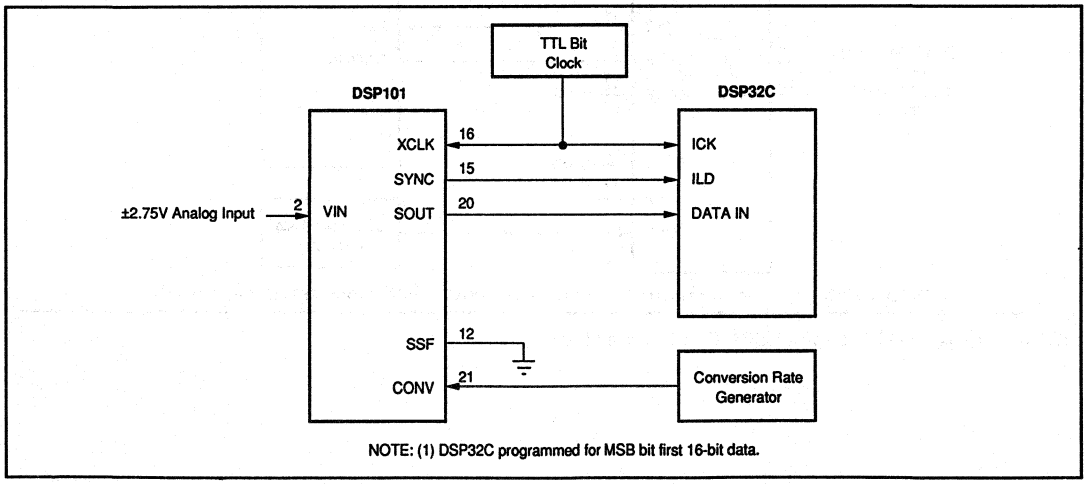


FIGURE 19. Using DSP101 with DSP32C.

USING DSP101 AND DSP102 WITH ADI DSP ICS

When using the DSP101 or DSP102 with the fixed-point ADSP21xx series, the processors need to be programmed to receive data MSB-first.

Figure 22 shows how to use the DSP102 with an ADSP2101 to provide a two-channel simultaneous sampling system.

Figure 23 shows the connections required to generate an analog input channel using an ADSP2105 with the DSP101.

The same basic circuit can be used to connect a DSP101 to the ADSP2101.

Figure 11 indicates how to build a complete analog I/O system using either the ADSP2101 or the ADSP2105 with a DSP101 and a Burr-Brown DSP201 D/A.

The two serial ports on the ADSP2101 can also be used with the DSP102 and the Burr-Brown DSP202 D/A to make two complete analog I/O channels, as indicated in footnote 2 of Figure 14.

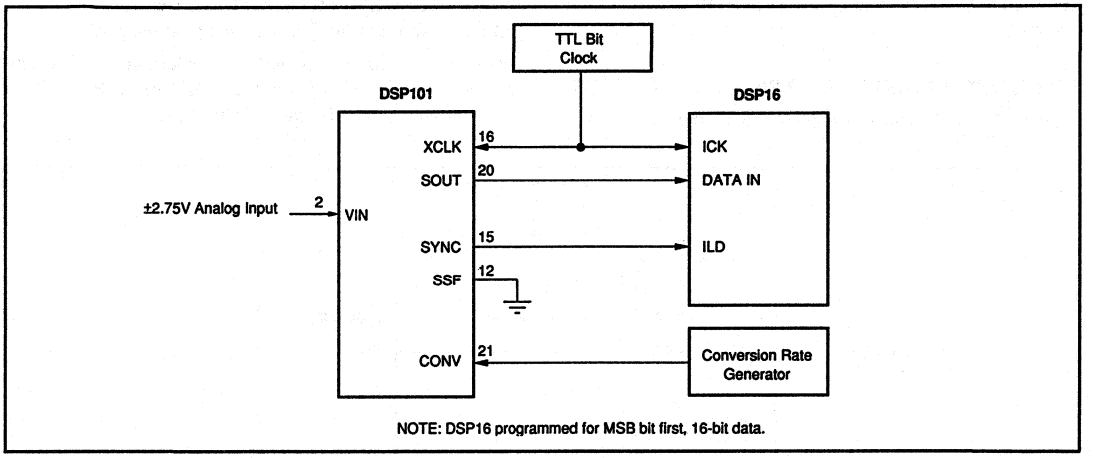


FIGURE 20. Using DSP101 with DSP16.

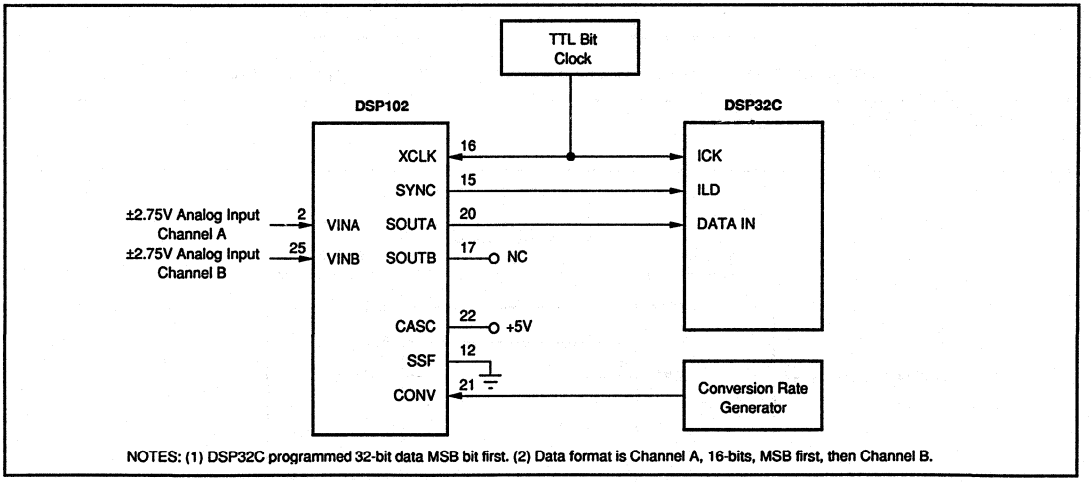


FIGURE 21. Using DSP102 with DSP32C in Cascade Mode.

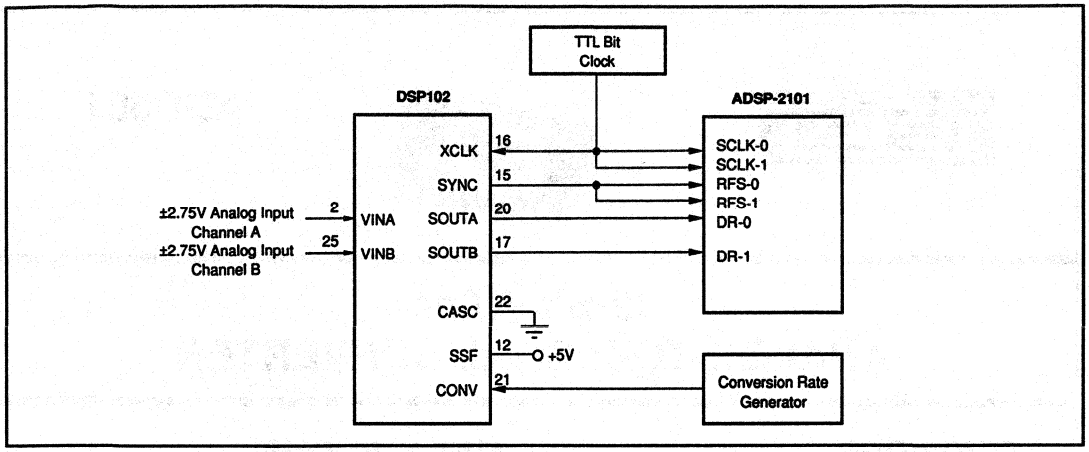


FIGURE 22. Using DSP102 with ADSP-2101.

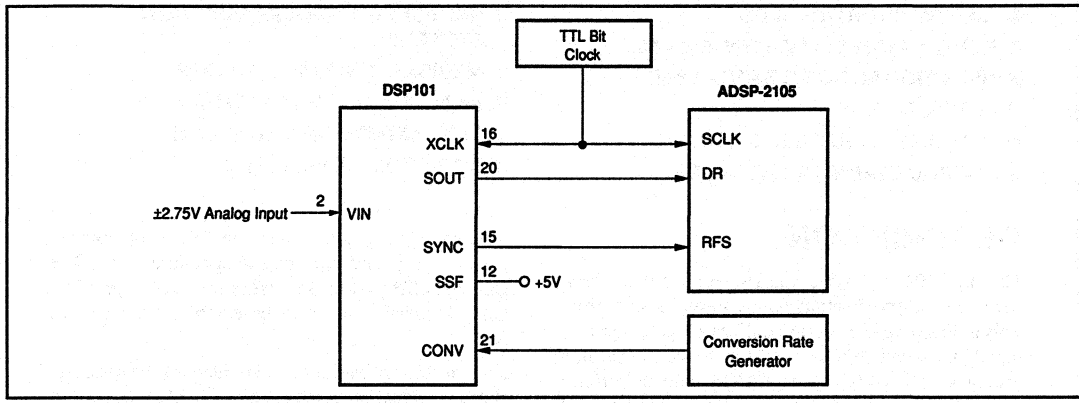


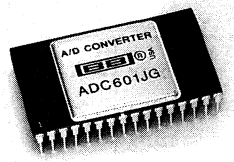
FIGURE 23. Using DSP101 with ADSP-2105.

DEM-DSP102/202 EVALUATION BOARD

An evaluation fixture, the DEM-DSP102/202, is available to simplify evaluation of the DSP101 and DSP102, and the companion digital-to-analog converters, the single DSP201 and dual DSP202. The DEM-DSP102/202 comes complete with a socketed DSP102 and DSP202, a breadboard area, TTL I/O headers and differential line drivers for data transfer options, a complete clocking circuit for the conversion clock and bit clock, and analog filter modules. The board makes it easy to go from design concept to working prototype of a DSP-based system, offering two complete analog I/O channels.

Contact your local Burr-Brown representative for a full data sheet on the DEM-DSP102/202.

BURR-BROWN®



ADC601

12-Bit 900ns ANALOG-TO-DIGITAL CONVERTER

FEATURES

- FAST CONVERSION: 900ns
- CAN BE SHORT-CYCLED
- INPUT RANGES: ±5V, ±10V, 0 to –10V
- HIGH SIGNAL/NOISE RATIO: 68dB
- LOW IMD: 75dB
- PARALLEL AND SERIAL OUTPUT
- 32-PIN CERAMIC DIP PACKAGE

APPLICATIONS

- DIGITAL SIGNAL PROCESSING
- HIGH-SPEED DATA ACQUISITION SYSTEMS
- MEDICAL INSTRUMENTATION
- ANALYTICAL INSTRUMENTATION
- TEST AND IMAGING SYSTEMS
- WAVEFORM ANALYZERS

DESCRIPTION

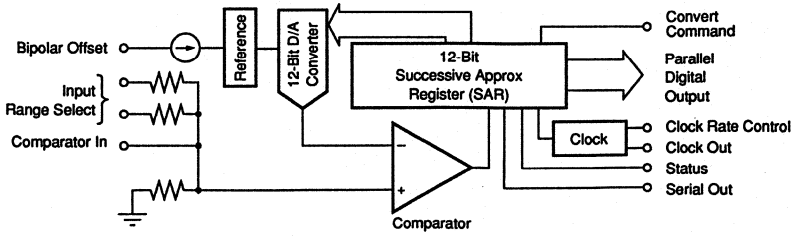
The ADC601 is a high-speed Duolithic™ (two chips) successive approximation analog-to-digital converter. This unique two-chip design utilizes a bipolar technology with on-chip thin film resistors to preserve analog accuracy and a high-speed CMOS chip to perform digital logic control. Outstanding linearity, noise, and dynamic range are achieved by this converter design. The ADC601 has been tested with several sample/hold amplifiers and distortion results are documented in this data sheet.

The ADC601 is complete with internal reference, clock, and comparator and is packaged in a 32-pin ceramic DIP. Conversion time is set at the factory to 900ns. Serial and parallel output performance is guaranteed with no missing codes over the full input voltage, power supply, and operating temperature range. The gain and offset errors are laser trimmed to specification. Optionally they may be externally adjusted to zero.

Internal scaling resistors are provided for the selection of analog signal input ranges of ±5V, ±10V and 0V to –10V. The ADC601's input is specifically designed to be easily driven with minimal disturbance to the driving amplifier.

Output codes are available in complementary binary for unipolar inputs and bipolar offset binary for bipolar inputs.

All digital inputs and outputs are TTL-compatible. Power supply requirements are ±15V and +5V.



Duolithic™ Burr-Brown Corporation

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Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL

T_{CASE} = +25°C, 900ns conversion time, $\pm V_{CC}$ = ±15V, $+V_{DD}$ = +5V, and 6-minute warm-up in a normal convection environment unless otherwise noted.

PARAMETER	CONDITIONS	ADC601JG MIN	ADC601JG TYP	ADC601JG MAX	ADC601KG MIN	ADC601KG TYP	ADC601KG MAX	UNITS
RESOLUTION				12			*	Bits
ANALOG CHARACTERISTICS								
INPUTS								
Voltage Ranges: Bipolar	Full Scale(FSR)[1][2]		±5, ±10			*		V
Unipolar	Full Scale(FSR)[1][2]		0 to –10			*		V
Impedance: –10V to 0V, ±5V			1.4			*		kΩ
±10V			2.4			*		kΩ
TRANSFER CHARACTERISTICS								
ACCURACY								
Gain Error[3]	990ns Conversion Time		±0.08	±0.55		*	±0.2	%
Input Offset Error[3]: Unipolar	990ns Conversion Time		±0.12	±1.2		*	±0.5	% of FSR
Bipolar	990ns Conversion Time		±0.08	±0.8		*	±0.25	% of FSR
Integral Linearity Error	990ns Conversion Time			±0.024			±0.012	% of FSR
Differential Linearity Error	990ns Conversion Time			±0.024			±0.012	% of FSR
No Missing Codes				Guaranteed				
Power Supply Rejection of Offset and Gain	Δ $+V_{CC}$ = ±5%		±0.0036			*		%FSR/%V_{CC}
	Δ $-V_{CC}$ = ±5%		±0.0005			*		%FSR/%V_{CC}
	Δ $+V_{DD}$ = ±5%		±0.001				*	%FSR/%V_{DD}
DIGITAL CHARACTERISTICS								
INPUT								
Logic Family				TTL-Compatible CMOS				
Convert Command Logic Voltages	Logic Low	0		+0.8	*		*	V
	Logic High	+2		$+V_{DD}$	*		*	V
Convert Command Currents	Logic Low			–150				µA
	Logic High			–150				µA
Convert Command				High Level When Converting				
CONVERSION TIME								
Factory Set	Without User Adjustment		0.9	1		*	*	µs
Power Supply Rejection of Conversion Time	D $+V_{DD}$ = ±5%		±1			*		ns/%V_{DD}
OUTPUT								
Logic Family				TTL-Compatible CMOS				
Bits 1 through 12, Serial, Status, Clock Out	Logic Low, I_{OL} = 3.2mA		+0.1	+0.4		*	*	V
	Logic High, I_{OH} = –1mA	+2.7	+4.9		*	*	*	V
Internal Clock Frequency			13			*		MHz
Status				Low Level When Data Valid				
DYNAMIC CHARACTERISTICS [4][5][6] Tested using Sample/Hold Amplifier SHC804 and ADC601 (See Typical Performance Curves)								
Differential Linearity Error	f_C = 10kHz: 68.3% of All Codes		0.5			0.4		LSB
	99.7% of All Codes		0.8			0.6		LSB
	100% of All Codes		1.0			0.7		LSB
Total Harmonic Distortion	f_C = 10kHz, f_S = 500kHz		–70			*		dBc
	f_C = 10kHz, f_S = 1MHz		–74			*		dBc
	f_C = 100kHz, f_S = 500kHz		–72			*		dBc
	f_C = 250kHz, f_S = 500kHz		–70			*		dBc
	f_C = 500kHz, f_S = 1MHz		–68			*		dBc
Two-Tone Intermodulation Distortion[7]	f_C = 11kHz and 15kHz, f_S = 500kHz		–79			*		dBc
	f_C = 50kHz and 55kHz, f_S = 500kHz		–78			*		dBc
	f_C = 90kHz and 110kHz, f_S = 500kHz		–77			*		dBc
Signal-to-Noise and Distortion (SINAD) Ratio	f_C = 100kHz, f_S = 500kHz		67			*		dB
	f_C = 250kHz, f_S = 500kHz		66			*		dB
	f_C = 500kHz, f_S = 1MHz		65			*		dB
Signal-to-Noise Ratio (SNR)	f_C = 100kHz, f_S = 500kHz		69			*		dB
	f_C = 250kHz, f_S = 500kHz		68			*		dB
	f_C = 500kHz, f_S = 1MHz		67			*		dB

SPECIFICATIONS (CONT)

ELECTRICAL

T_{CASE} = +25°C, 900ns conversion time, $\pm V_{CC}$ = ±15V, $+V_{DD}$ = +5V, and 6-minute warm-up in a normal convection environment unless otherwise noted.

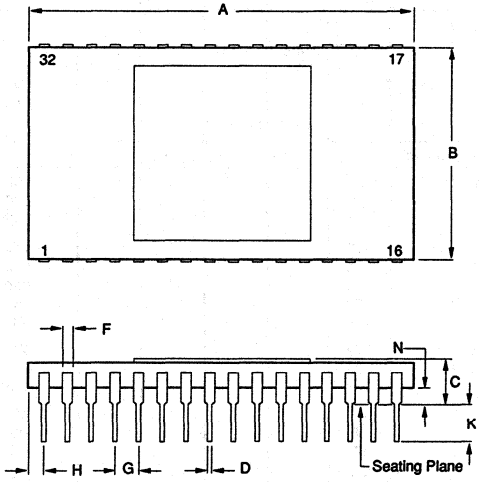
PARAMETER	CONDITIONS	ADC601JG MIN	ADC601JG TYP	ADC601JG MAX	ADC601KG MIN	ADC601KG TYP	ADC601KG MAX	UNITS
PERFORMANCE OVER TEMPERATURE								
Gain	T_{MIN} to T_{MAX}		±10	±30		*	*	ppm of FSR/°C
Input Offset: Unipolar	T_{MIN} to T_{MAX}		±2	±7		*	*	ppm of FSR/°C
Bipolar	T_{MIN} to T_{MAX}		±3	±10		*	*	ppm of FSR/°C
Internal Linearity Error	0.9µs Conversion Time T_{MIN} to T_{MAX}		±0.02			±0.015		% of FSR
Differential Linearity Error	0.9µs Conversion Time T_{MIN} to T_{MAX}		±0.02			±0.015		% of FSR
No Missing Codes	0.9µs Conversion Time T_{MIN} to T_{MAX}			Guaranteed				
Conversion Drift			2			*		ns/°C
POWER SUPPLY REQUIREMENTS								
Supply Voltages: $+V_{CC}$		+14.25	+15	+15.75	*	*	*	V
$-V_{CC}$		−14.25	−15	−15.75	*	*	*	V
$+V_{DD}$		+4.75	+5	+5.25	*	*	*	V
Supply Currents: $+I_{CC}$			5.4	7.0		*	*	mA
$-I_{CC}$			−65	−84.5		*	*	mA
$+I_{DD}$			53	68.9		*	*	mA
Power Consumption	Nominal $\pm V_{CC}$ and $+V_{DD}$		1.3	1.7		*	*	W
Thermal Resistance, θ_{JC}			25			*	*	°C/W
TEMPERATURE RANGE[6]								
Specification		0		+70	*		*	°C
Operating		−25		+85	*		*	°C

* Same specifications as for ADC601JG.

NOTES: (1) Over or under range on the analog input results in constant maximum or minimum digital output. (2) FSR = Full Scale Range. (3) Adjustable to zero. (4) Dynamic tests are performed using SHC804 with ADC601 unless otherwise specified. Performance may vary depending upon choice of sample/hold. (5) See Typical Performance Curves. (6) dBc = level referred to carrier input signal = 0dB; f_c = input frequency; f_s = sampling frequency. (7) IMD is referred to the larger of the two input test signals. If referred to the peak envelope signal (=0dB), the intermodulation products will be 6dB lower. For example, unit connected for ±10V has 20V FSR.

MECHANICAL

H Package — 32-Pin Hermetic DIP

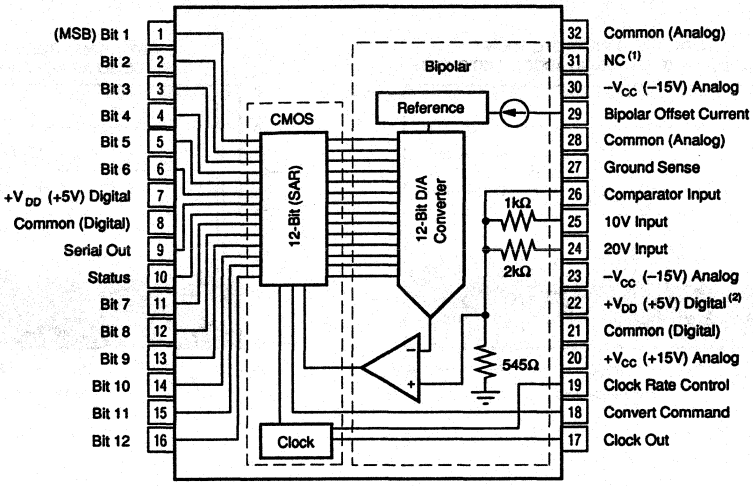


DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.580	1.620	40.13	41.15
B	.880	.900	22.35	22.86
C	.138	.186	3.51	4.72
D	.016	.020	0.41	0.51
F	.040 TYP		1.02 TYP	
G	.100 BASIC		2.54 BASIC	
H	.044	.056	1.12	1.42
J	.009	.012	0.23	0.30
K	.165	.185	4.19	4.70
L	.900	.920	22.86	23.37
N	.040	.060	1.02	1.52

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

PIN CONFIGURATION



(1) NC = No internal connection. Any voltage may be connected to pin 31, however.
(2) Pin 22 must be very cleanly decoupled to keep digital noise out of the analog circuits.

PIN DEFINITIONS

PIN NUMBER	DESIGNATION	DESCRIPTION
1-6 and 11-16	Bit 1 to Bit 12	12-bit parallel output data capable of sinking 3.2mA.
9	Serial Out	12-bit serial data output synchronized with the negative edge of each appropriate clock cycle.
10	Status	Conversion status strobe is high during data conversion; low when parallel data is valid. Negative edge may be used to latch parallel data, however, appropriate latch set-up time must be provided. Refer to t_{BBL} in the ADC601 timing diagram.
17	Clock Out	Negative edge indicates when serial data is valid. After convert command goes high, fist cycle clocks bit 1 (MSB). The clock continues to run when convert command is high and resets low with convert command.
18	Convert Command	High transition starts conversion; and should remain high during conversion. Low will reset clock and SAR logic.
19	Clock Rate Control	May be used to increase clock speed, by increasing the positive portion of the clock. High is normal operation.
24	20V Input	20V input range allows ±10Vp-p analog input signal. Short to ground when not used.
25	10V Input	10V input range allows 0 to –10Vp-p or ±5Vp-p input range.
26	Comparator In	Only used in bipolar mode when it is connected to bipolar offset pin through short lead with low resistance.
27	Ground Sense	Ground Sense pin. (See text for use).
29	Bipolar Offset Current	Bipolar offset current short to comparator In through very short lead with very low resistance for bipolar operation. Short to ground for unipolar operation.

ABSOLUTE MAXIMUM RATINGS

$\pm V_{cc}$	±18V
$+V_{DD}$	+7V
Digital Inputs	+5.5V
Analog Inputs	$\pm V_{cc}$
Comparator Input	–3.7V to +0.7V
Case Temperature	+125°C
Junction Temperature	+165°C
Storage Temperature	–65°C to +150°C

Stresses above these ratings may permanently damage the device.

ORDERING INFORMATION

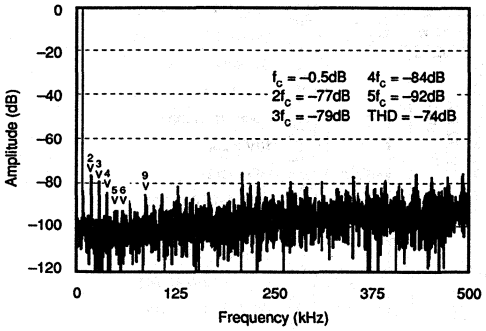
ADC601 ( ) G

Basic Model Number
Performance Grade Code
J, K: 0°C to +70°C Case Temperature
Package Code
G: Ceramic DIP

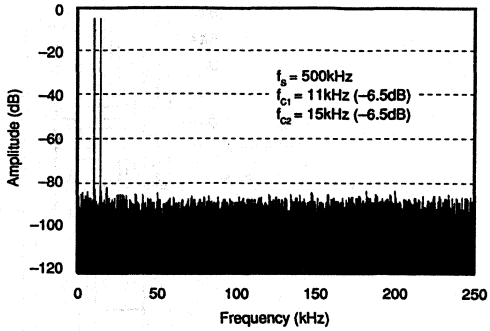
TYPICAL PERFORMANCE CURVES

$\pm V_{CC}$ = ±15V, $+V_{DD}$ = +5V, 15-minute warmup, and T_C = +25°C, unless otherwise noted. All dynamic performance curves are 4096-point FFTs.

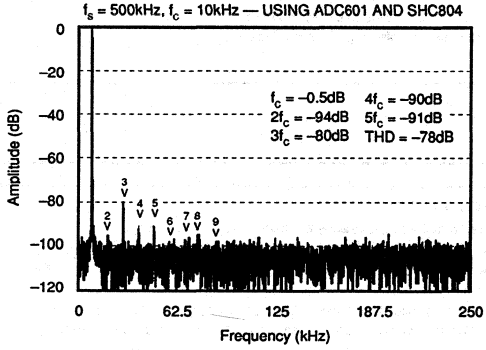
TOTAL HARMONIC DISTORTION
f_S = 1MHz, f_C = 10kHz — USING ADC601 AND SHC804



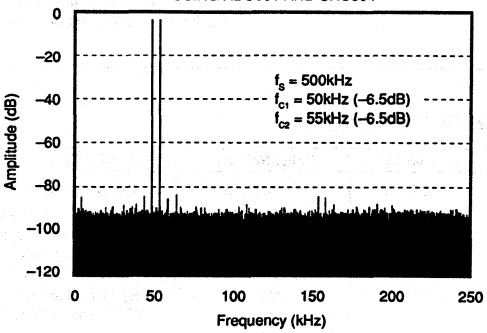
TWO-TONE INTERMODULATION
USING ADC601 AND SHC804



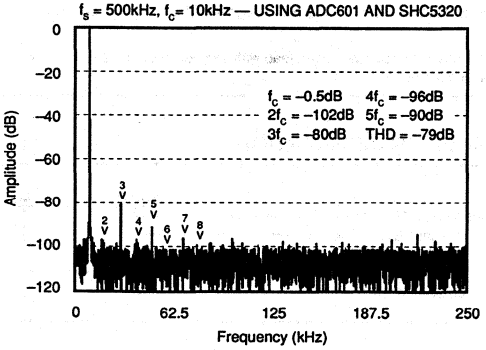
TOTAL HARMONIC DISTORTION
f_S = 500kHz, f_C = 10kHz — USING ADC601 AND SHC804



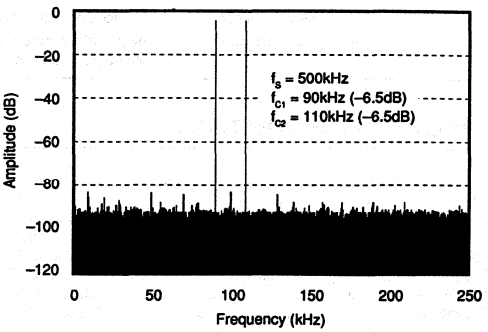
TWO-TONE INTERMODULATION
USING ADC601 AND SHC804



TOTAL HARMONIC DISTORTION
f_S = 500kHz, f_C = 10kHz — USING ADC5320

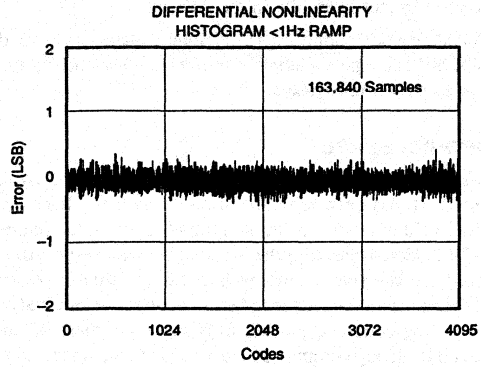


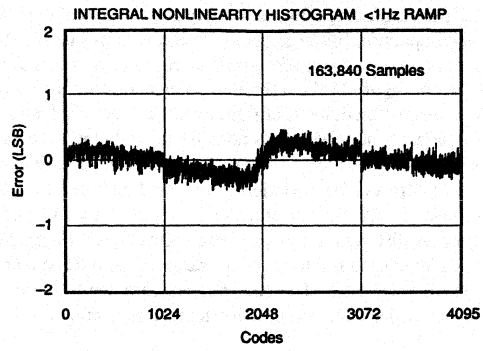
TWO-TONE INTERMODULATION
USING ADC601 AND SHC804

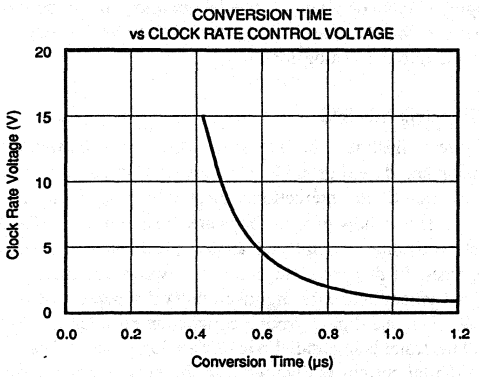


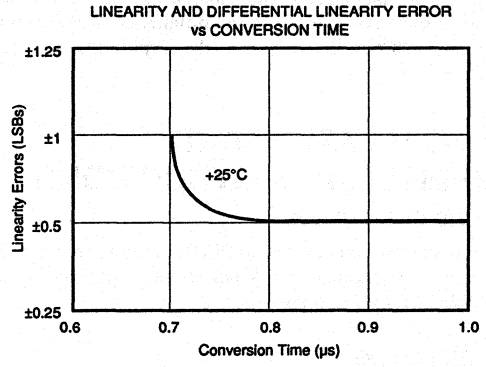
TYPICAL PERFORMANCE CURVES (CONT)

$\pm V_{CC}$ = ±15V, $+V_{DD}$ = +5V, R_S = 50Ω, 15-minute warmup, and T_C = +25°C, unless otherwise noted.









THEORY OF OPERATION

The ADC601 is a successive approximation analog-to-digital converter as shown on the front page of this product data sheet. A common problem with other successive approximation A/D converters is input current transients caused by the D/A converter's switching. This requires a fast-settling amplifier to drive the input and to provide a low source impedance at high frequency.

To minimize this problem, the ADC601's comparator is connected in a differential mode, greatly reducing the input transients. In addition, the input voltage scaling resistors reduce the voltage that is applied to the + input of the comparator. For best performance, a fast settling wideband sample/hold amplifier such as Burr-Brown's SHC804 is still recommended to drive the ADC601. The small signal settling time of this amplifier should be less than 100ns if sampling rates approach 1MHz.

The accuracy of a successive approximation analog-to-digital converter is described by the transfer function shown

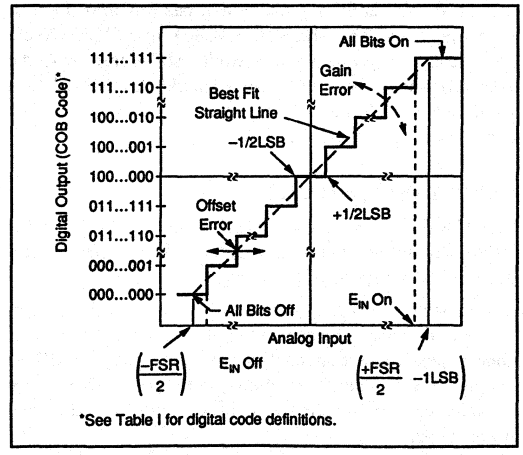


FIGURE 1. Input vs Ouput for an Ideal Bipolar A/D Converter.

in Figure 1. All successive approximation A/D converters have an inherent quantization error of ±1/2LSB. The remaining errors in the A/D converter are combinations of analog errors due to the linear circuitry matching and tracking properties of the ladder and scaling networks, power supply rejection, reference errors and the dynamic errors of the DAC and comparator. Initial gain and offset errors may be adjusted to zero, gain drift over temperature rotates the transfer function (Figure 1) about the zero point, and offset drift shifts the transfer function left or right over the operating temperature range. Linearity error is not adjustable, but it is the most meaningful indicator of A/D converter accuracy. Integral linearity error is the deviation of an actual bit transition from the best fit straight line transfer function of the A/D converter. A differential linearity error of ±1/2LSB means that the width of each bit step over the range of the A/D converter is 1LSB, ±1/2 LSB. The ADC601 is guaranteed to have no missing codes over its specified temperature range.

ACCURACY VS CONVERSION TIME

In successive approximation A/D converters, the conversion time affects integral and differential linearity error. Conversion time effects on linearity and differential linearity error for the ADC601 are shown in the Typical Performance Curves.

INSTALLATION AND OPERATING INSTRUCTIONS

BASIC CONNECTION

The basic connection for the ADC601 is shown in Figure 2. It is shown connected for ±5V bipolar input operation. Refer to Table I for other connections.

INTERFACING

Because the ADC601 is a high-speed converter, it must be driven from an amplifier source that has low impedance at high frequency. The SHC803, SHC804, and SHC5320 are specifically designed to give accurate, stable results. At the ADC601 output, the digital lines should be buffered by a latch such as the 74LS574. These three-state drivers can then connect directly to the data bus.

LAYOUT PRECAUTIONS

The ADC601 is a high-speed analog-to-digital converter that requires more attention to circuit board layout than general purpose, lower speed A/D converters.

The wideband ADC601 comparator input (pin 26) is very sensitive to noise. Any connection to this point should be as short as possible and shielded by analog common or ±15VDC supply patterns. The clock output (pin 17) is sensitive to stray capacitance, and capacitance on this pin could alter the clock wave shape.

The ADC601 has two pins for analog common, two pins for digital common, and two pins for each power supply input. Each pair of these pins **must** be connected together externally. The connection between the digital supply pins and the connection between the digital common pins must be as short as possible. The analog and digital commons are not connected together internally in the ADC601.

Connecting all commons to a ground plane close to the ADC601 is the best method to minimize noise and dissipate heat as shown in Figure 3.

GROUND SENSE

A special analog ground called "ground sense" (shown in Figure 3) has been provided to eliminate the voltage drop that would otherwise be in the ground return of the internal R-2R ladder. Measuring the input signal with respect to the sense terminal (pin 27) makes the measurement independent of the connection impedance between the sense terminal and the analog common, pin 28. This sense pin must be connected to analog common as close to the input signal source as possible or connected to the ground plane. Low impedance analog and digital common returns are essential for low noise performance. To minimize coupling between analog and digital circuits on a layout, special attention should be taken to ensure that the clock noise on the +5V supply line does not couple into the analog inputs.

GROUND LOOPS

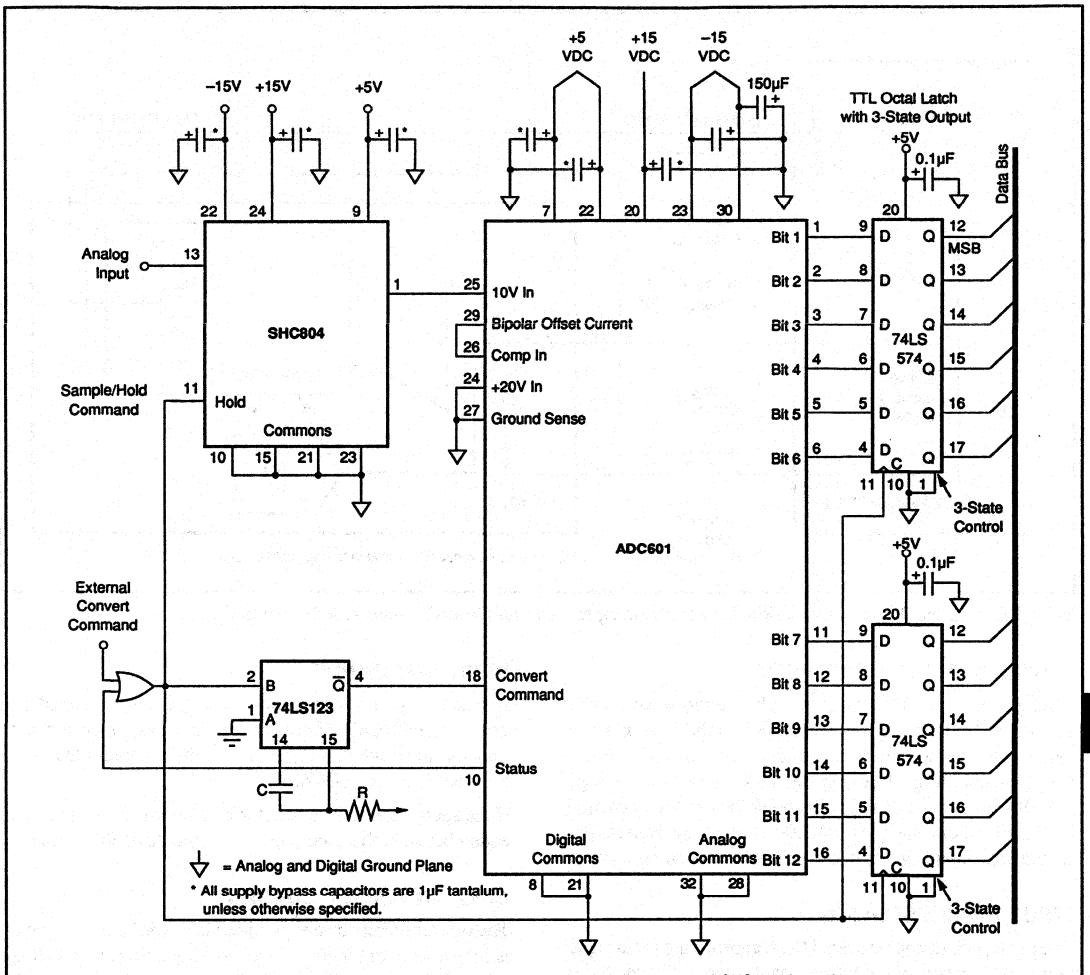
Figure 4 illustrates the interaction that occurs between the analog and digital grounds when an ADC is connected into a test circuit. This interaction is created by ground loops. The circuit shows how ground loops are created when the ADC tester combines digital and analog portions of the circuit together. In this case, the loop is between the analog test signal generator and the digital circuitry that detects the ADC code. Here the digital ground connection between the ADC and the tester is in parallel with the analog grounds. Some of the digital current is diverted into the analog signal return, which creates a code-dependent error signal due to the resistance in the analog signal return. This error distorts the linearity measurement and induces hysteresis. It can be substantially reduced if the analog and digital ground effects are isolated from each other in the ADC tester. The best method is to use a low resistance, low inductance ground plane.

POWER SUPPLY DECOUPLING

Each power supply pin should be bypassed with a 1µF or 150µF tantalum capacitor as shown in Figure 2. These capacitors should be located close to the ADC. Ceramic 0.01µF bypass capacitors have been provided internally for more effective bypassing and need not be added externally.

ADDITIONAL DECOUPLING

A 100pF capacitor may be placed on Clock Rate Adjust (pin 19) to ground in order to reduce noise on the clock. Up to 30pF may be placed on Comparator In (pin 26) without degrading conversion accuracy at Nyquist frequencies.



(1) In the circuit shown above, the rising edge of the external Convert Pulse initiates the Hold mode of the SHC804. Assuming a user-provided convert pulse with a 50% duty cycle, the 74LS123 one-shot provides a short pulse for the convert command (pin 18) on the ADC601. The actual one-shot time chosen, by setting the R-C on the one-shot, should be just long enough to allow for adequate track-to-hold settling time. For best I.L. performance, it is recommended that the one-shot time be less than 400ns, but at least 50ns.

FIGURE 2. Basic Connection Diagram in Bipolar Operation and Dynamic Test Circuit.

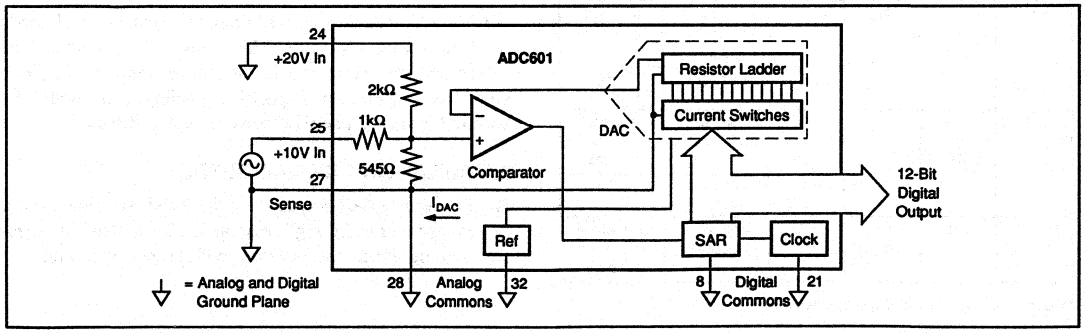


FIGURE 3. Analog and Digital Grounds, and Analog Input Sense.

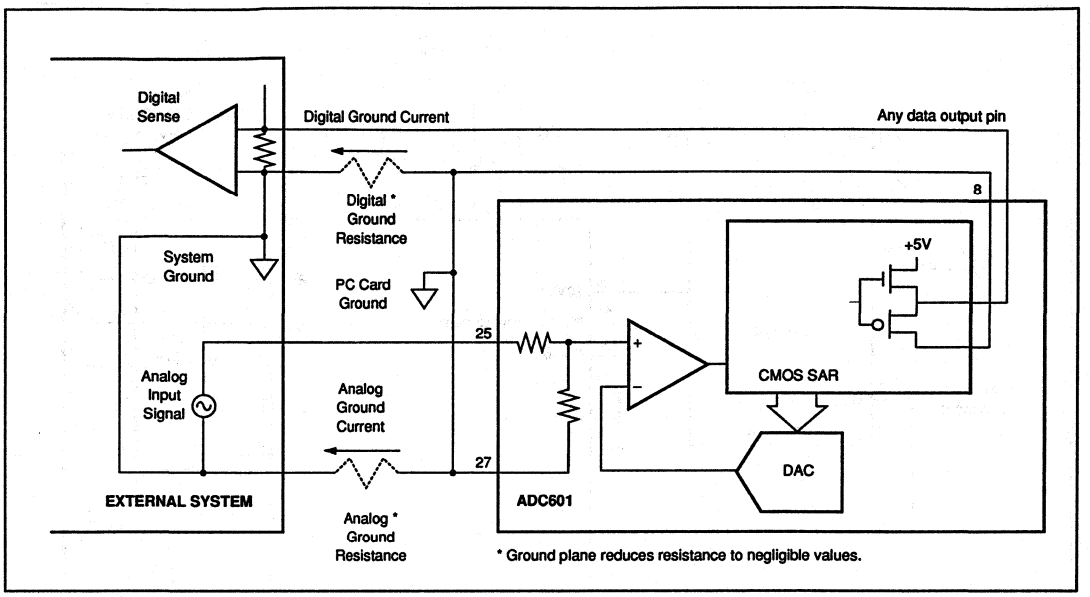


FIGURE 4. Ground Loop Interaction Between Analog and Digital Grounds when ADC Is Connected.

POWER SUPPLY SENSITIVITY

Changes in the DC power supply voltages will affect accuracy. Normally, regulated power supplies with 1% or less ripple are recommended for use with this ADC. Power supply decoupling, shown in Figure 2, helps to keep ripple low. Switching power supplies should be used with caution. EMI/RFI filters such as BNX002 made by Murata/Erie Company, Canada give good results with switching supplies.

INPUT RANGE SCALING

The analog input can be scaled to an appropriate input signal range by proper pin connections to the A/D converter. Connect input signals as shown in Table I.

Input Signal Range	Output Code	Connect Pin 29 To	Connect Gain Adjust	Connect Pin 24 To	Connect Pin 25 To
±10V	BOB or BTC*	26	Yes	40Ω resistor in series with input signal	Gain Adjust Potentiometer
			No	Input Signal	Analog Common
±5V	BOB or BTC*	26	Yes	Gain Adjust Potentiometer	10Ω resistor in series with input signal
			No	Analog Common	Input Signal
0 to −10V	CSB	Analog Common	Yes	Gain Adjust Potentiometer	10Ω resistor in series with input signal

* Obtained by inverting MSB (pin 1) externally.

TABLE I. ADC601 Input Scaling Connections.

INPUT IMPEDANCE

If external gain adjust is not used, the source impedance driving the ADC601 should be low (such as the output of an op amp) to avoid gain errors due to the relatively low input impedance of the ADC601.

If the source impedance is not low, a buffer amplifier can be added between the input signal and the ADC601 inputs.

BIPOLAR OFFSET CURRENT

The bipolar offset current provided in the ADC601 on pin 29 is for use only in bipolar operation where pins 26 and 29 are connected together. Pin 29 should be grounded for unipolar operation. To prevent noise interference, this output should not be used for any other purpose; make no other connection to pin 29.

OUTPUT DRIVE

All ADC601 data outputs will drive two standard TTL loads or 10 low-power Schottky TTL loads. If long digital lines must be driven, external logic buffers are required. The clock output is sensitive to capacitive loading and should be buffered if high capacitive loads are being driven.

PARALLEL AND SERIAL OUTPUT

Parallel and serial output may be used simultaneously, however proper buffering is essential. This will avoid excessive loading which can interfere with proper operation.

POWER DISSIPATION

The ADC601 dissipates approximately 1.3W. The package has a junction-to-case thermal resistance (θ_{JC}) of 25°C/W and a case-to-ambient thermal resistance (θ_{CA}) of 22°C/W in a normal convection environment. For operation above +85°C a heat sink is recommended. This should contact the bottom of the ADC601 for best results. See electrical specification table notes.

OPTIONAL EXTERNAL GAIN AND OFFSET ADJUSTMENTS

Gain and offset errors may be trimmed to zero using external trim potentiometers as shown in Figures 5, 6, and 7. For sufficient adjustment range, a series resistor must be connected to the analog input pin as specified in Table I. Multiturn potentiometers with 100ppm/°C temperature coefficient are recommended for minimum drift. All fixed resistors should be ±1% metal film. If the Offset adjust is not used, pin 26 should be left open except for bipolar operation when it is connected to pin 29. If Gain adjust is not used, the unused input (pin 24 or 25) must be grounded to meet specified gain accuracy.

Adjustment Procedure

Refer to Table II for LSB voltages and transition values.

For unipolar offset, connect the offset potentiometer and resistors as shown in Figure 5. Sweep the input through the end point transition voltage, from 111...110 to 111...111. Adjust the offset potentiometer until the actual end point transition voltage occurs at –1/2LSB.

For bipolar offset, connect the offset potentiometer and resistors as shown in Figure 5. Sweep the input through zero and adjust the offset potentiometer until the transition from 0111 1111 111 to 1000 0000 0000 occurs at –1/2LSB.

For gain, connect the gain potentiometer as shown in Figure 6. Sweep the input through the end point transition voltage, which should cause an output transition from 000...000... to 000...001. Adjust the gain potentiometer until this transition occurs at the correct end point transition voltage as given in Table II.

OPTIONAL CLOCK RATE CONTROL

The clock is factory-set for a conversion time between 800ns and 900ns. By use of the optional clock rate control shown in Figure 7, the 12-bit conversion time can be typically adjusted down to 700ns. It can also be used, if desired, to get slightly higher speed or to assure maximum conversion time at elevated temperature. If the clock rate control is not used, Pin 19 should be left open or bypassed with 100pF capacitor. Conversion time versus clock rate control voltage is shown in the Typical Performance Curves.

More positive voltage on clock rate control increases speed of conversion. Voltage of less than 1V may cause the clock to stop.

Analog Input Voltage Range	±10V	±5V	0 to –10V
Code Designation	BOB[1] or BTC[2]	BOB or BTC	CSB[3]
One Least Significant Bit (LSB)	4.88mV	2.44mV	2.44mV
Transition Values MSB LSB[4]			
000...000 000...001	–10V + 1/2LSB	–5V + 1/2LSB	–10V + 3/2LSB
011...111 100...000	–1/2LSB	–1/2LSB	–5V + 1/2LSB
111...110 111...111	+10V – 3/2LSB	+5V – 3/2LSB	–1/2LSB

NOTES: (1) BOB = Bipolar Offset Binary. (2) BTC = Binary Two's Complement (obtained by inverting the most significant bit (pin 1). (3) CSB = Complementary Straight Binary. (4) Voltages given are the nominal value for the transition from the next lower code.

TABLE II. Input Voltages, Transition Values, LSB Values, and Code Definitions.

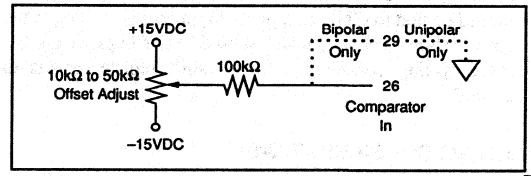


FIGURE 5. Optional Offset Adjust.

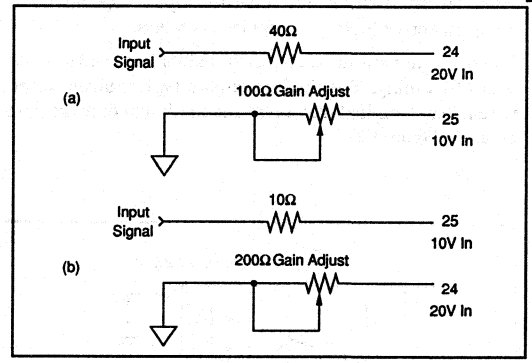


FIGURE 6. Optional Gain Adjust: (a) ±10VBipolar Operation, (b) ±15V Bipolar or 0 to –10V Unipolar Operation

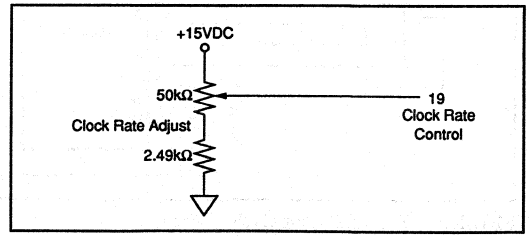


FIGURE 7. Optional Clock Rate Control.

EXTERNAL SHORT CYCLE

The ADC601 may be short-cycled for fewer bits of resolution at faster conversion speeds. The short cycle circuit (Figure 8) works by having the 74LS165 shift register count the clock pulses out of the ADC which correspond to the ADC bit becoming valid. The shift register will output a negative going pulse when the programmed 74LS165 input is shifted to the serial output Q-not. The negative pulse then resets the R-S flip/flop to a low and brings convert comand low, thus stopping the ADC conversion. At the time the ADC stops converting, status goes low which initiates a parallel load to the shift register, thus programming it for the next conversion. The R-S flip/flop made from the 74LS00 nand gates and the other 2 nand gates act as gating for the reset pulse from the shift register. For short-cycling from 9 to 11 bits, cascade two 74LS165s together.

The 74LS165 shift register is programmed on inputs A-G to short cycle the ADC601 on a given bit. For the circuit shown, input A will short cycle the ADC on bit 7, input B on bit 6, etc to input G short cycling on bit 1. All shift register inputs should be tied to GND except the input corresponding to the desired short-cycle bit, which should be tied high. To disable short cycling completely, tie all shift register inputs to ground.

TIMING CONSIDERATIONS

The timing diagram (Figure 9) shows the relationship between the convert command, clock and outputs. The digital output word uses positive logic for bipolar operation and complementary logic for unipolar operation.

The following are some important points to consider on the ADC601 timing. The times given are typical unless otherwise noted. Nominal maximum and minimum times are also given in Figure 9.

1. When power is first applied, the status of the ADC601 will be undetermined. A convert command must be applied to initialize the ADC601.
2. The convert command must be low at least 50ns prior to the rising edge that starts a conversion.
3. The clock runs continuously when the initial convert command goes high and whenever the convert command is high thereafter. It does not run when convert command is low.
4. The clock is started by a rising transition of the convert command.
5. Parallel Output Data: The successive approximation register (SAR) is reset after the leading edge of the first clock period in the conversion cycle. The MSB is set to logic "0" and all other bits are set to logic "1". The bits are determined in succession starting with the MSB, Bit 1, as shown in Figure 9. Each bit will be valid after its corresponding clock pulse.

   In most applications the rising edge of the Convert Command may be used to strobe parallel data out of the ADC601 directly. It is recommended that all outputs are buffered if large capacitive loads are being driven.
6. Status goes high after the rising edge of the first clock pulse and goes low after all 12 bits are valid.
7. Bit 12 will become valid before status goes low; a new conversion may be initiated anytime after the output data has been read.
8. The converter may be restarted during a conversion. If a convert command is held at zero for a minimum of 50ns, the SAR will be reset and a new conversion will start on the next rising transition regardless of the state of the converter prior to the convert commands being received.

Figures 10, 11, and 12 are digital oscilloscope displays of the actual pulse shapes and relationships.

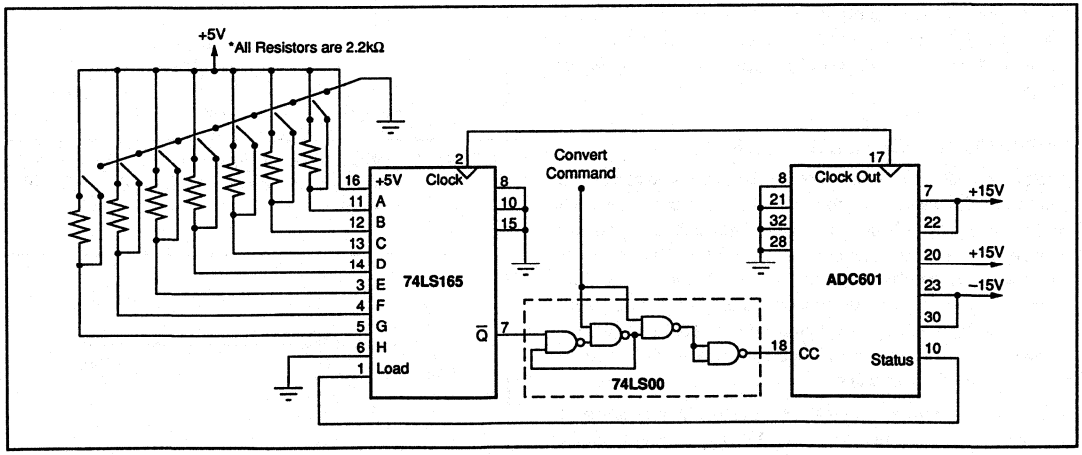
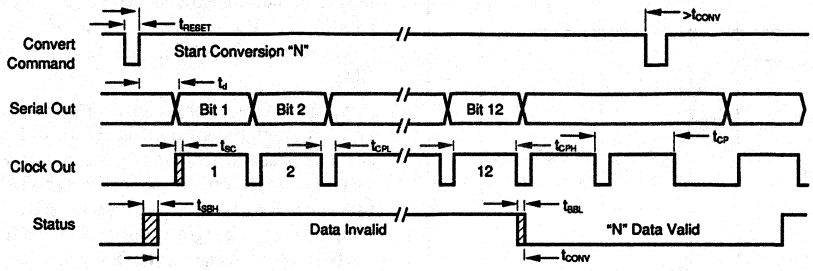


FIGURE 8. External Short Cycle Circuit.



SYMBOL	PARAMETER	MINIMUM	TYPICAL	MAXIMUM	UNITS
t_{CP}	Clock Period		73		ns
t_{CPH}	Clock Pulse High		20		ns
t_{CPL}	Clock Pulse Low		53		ns
t_{CONV}	Conversion Time		850	1µs	ns
t_{SC}	Serial to Clock Out Delay	0		5.5	ns
t_{SBH}	Start to Status High Delay			13.0	ns
t_{BBL}	Data Valid to Status Low Delay	0		3.0	ns
t_{RESET}	Convert Command Low	50		400	ns
t_d	CC to First Clock Pulse			100	ns

NOTE: Logic timing limits: T_A = +25°C and +125°C, unless otherwise specified

FIGURE 9. ADC601 Logic Timing Diagram.

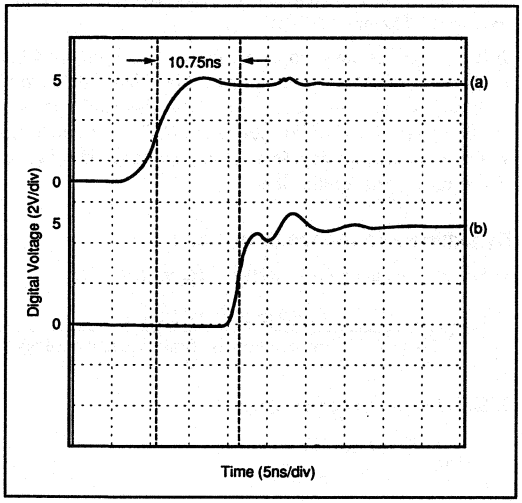
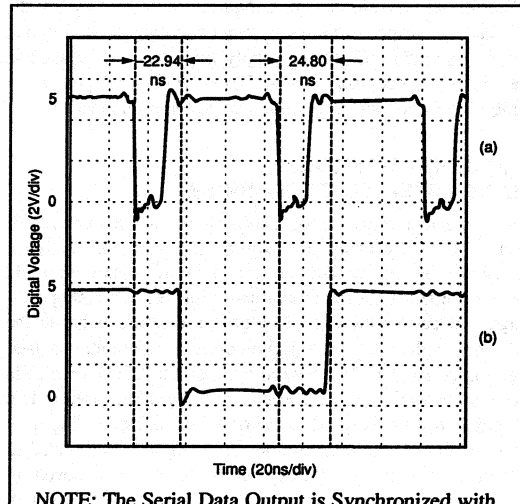


FIGURE 10. (a) Convert Command, (b) Status.



NOTE: The Serial Data Output is Synchronized with the Negative Edge of Each Appropriate Clock Cycle.

FIGURE 11. (a) Clock, (b) Serial Out.

DIGITAL CODES

Parallel Data

Two binary codes are available on the ADC601 parallel output; straight binary (logic "0" true) for unipolar input signal ranges and bipolar offset binary (logic "1" true) for bipolar input signal ranges. Binary two's complement may be obtained for bipolar input ranges by inverting the MSB. It should be noted that for unipolar input ranges –10V is full scale.

Table II shows the LSB, transition values, and code definitions for each possible analog signal range.

Serial Data (NRZ)

ADC601 serial data operation is guaranteed to match the parallel data. If an optoisolator is used to eliminate ground connections, buffer the output with an appropriate TTL line driver. It is recommended that all outputs be buffered if large capacitive loads are being driven.

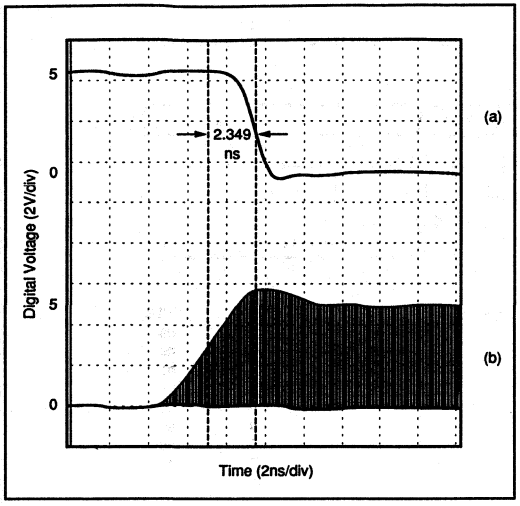


FIGURE 12. (a) Status, (b) Bit-12 Data.

TESTING OF THE ADC601

Careful test fixture design is required to accurately test the ADC601. Proper grounding, correct routing of analog and digital signals and power supply bypassing are crucial in achieving successful results. High-frequency layout techniques and copper ground planes are recommended.

ANALOG-TO-DIGITAL CONVERTER TEST TECHNIQUE

A very effective way of determining the DC performance of an ADC is by using the "servo loop method." A block diagram of this technique is shown in Figure 13. This measurement system automatically locates the analog voltage that causes the digital output to alternate between the desired code and the adjacent code. A computer is programmed to place the desired code on the I/O bus which is one input to the digital comparator. The other input to this comparator is the digital output of the ADC. Depending upon the results of this comparison, the integrator is directed to change its output until an equilibrium state is achieved, in where the comparator and the ADC digital words are equal. Once in equilibrium, the DVM measures the analog input to the ADC and transmits the information to the computer via an IEEE-488 bus. The test program checks all the desired code combinations, verifying the performance of the ADC. Test time will range from 10 seconds to several minutes depending on the speed of the test program, settling time of the DVM, and number of codes to be checked.

DYNAMIC PERFORMANCE TESTING

The ADC601 is a very high performance converter and careful attention to test techniques is necessary to achieve accurate results. Spectral analysis by application of a fast Fourier transform (FFT) to the ADC digital output will provide data on all important dynamic performance parameters: total harmonic distortion (THD), signal-to-noise ratio (SNR) or the more severe signal-to-noise-and-distortion ratio (SINAD), and intermodulation Distortion (IMD).

A typical test setup for performing high-speed FFT testing of analog-to-digital converters is shown in Figure 14. Highly accurate phase-locked signal sources allow high resolution FFT measurements to be made without using window functions. By choosing appropriate signal frequences and sample rates, an integral number of signal frequency periods can be sampled. As no spectral leakage results, a "rectangular" window (no window function) can be used. This was used to generate the typical FFT performance curves shown in the Typical Performance Curves.

If generators cannot be phase-locked and set to extreme accuracy, a very low side-lobe window must be applied to the digital data before executing an FFT. A commonly used window such as the Hanning window is not appropriate for testing high performance converters; a minimum four-sample Blackman-Harris window is strongly recommended.[1] To assure that the majority of codes are exercised in the ADC601 (12 bits), a 4096-point FFT is taken. If the data storage RAM is limited, a smaller FFT may be taken if a sufficient number of samples are averaged (ie, a 10-sample average of 512-point FFTs).

IMD two-tone testing shown in Figure 15 is referenced[3] to the larger of the test signals f_1 or f_2. Five "bins" either side of peak are used for calculation of fundamental and harmonic power. The "0" frequency bin (DC) is not included in these calculations as it is of little importance in dynamic signal processing applications.

Dynamic Performance Definitions

1. Signal-to-Noise-and-Distortion[2] Ratio (SINAD):

$$10 \log \frac{\text{Sinewave Signal Power}}{\text{Noise + Harmonic Power (first nine harmonics)}}$$

2. Signal-to-Noise Ratio (SNR):

$$10 \log \frac{\text{Sinewave Signal Power}}{\text{Noise Power}}$$

3. Total Harmonic Distortion (THD):

$$10 \log \frac{\text{Harmonic Power (first nine harmonics)}}{\text{Sinewave Signal Power}}$$

4. Intermodulation Distortion (IMD):

$$10 \log \frac{\text{IMD Product Power (RMS sum; to fifth order)}}{\text{Sinewave Signal Power}}$$

5. Spurious-Free Dynamic Range (SFDR):

$$10 \log \frac{\text{Sinewave Signal Power}}{\text{Largest Power Product}}$$

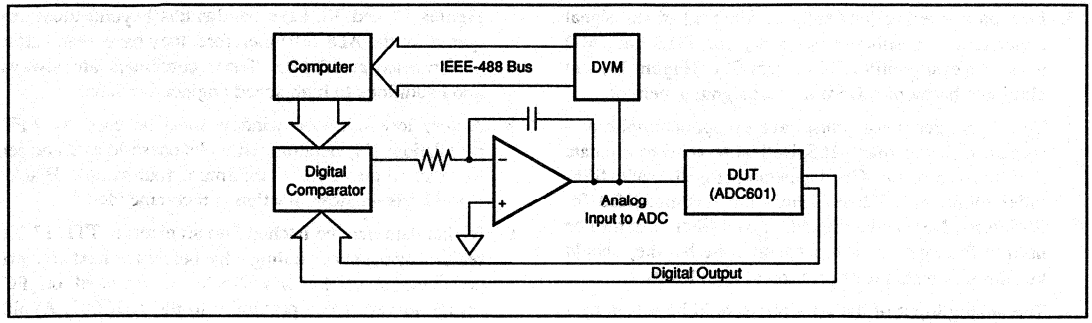


FIGURE 13. Servo Loop Analog-to-Digital Tester.

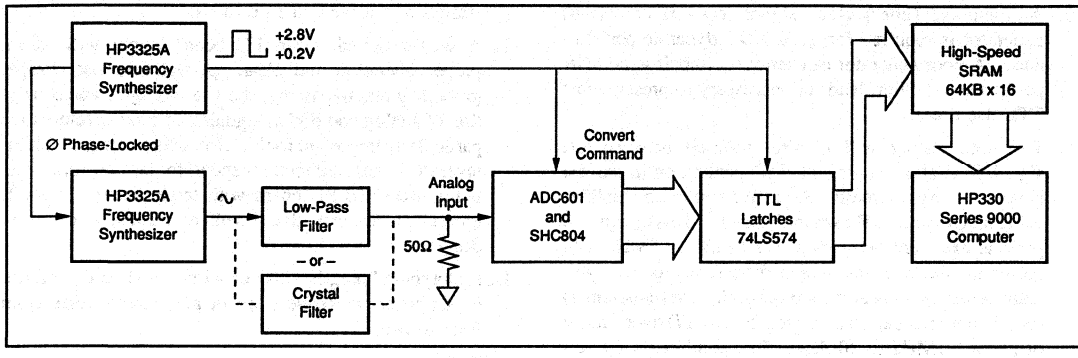


FIGURE 14. Block Diagram of FFT Test for THD, SNR, and SINAD.

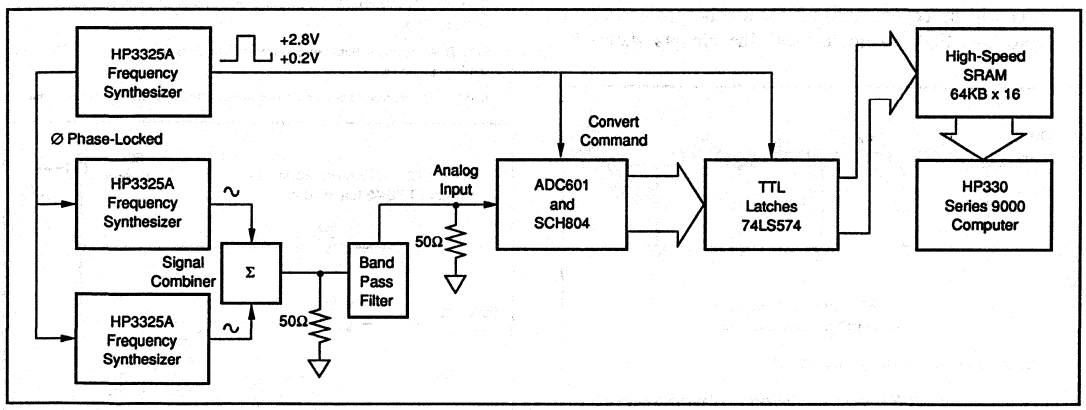


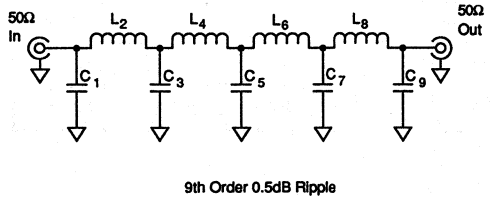
FIGURE 15. Block Diagram of FFT Test for Two-Tone IMD.

MAJOR POINTS TO CONSIDER

Attention to test set up details can prevent errors that contribute to poor test results. Important points to remember when testing high performance converters are:

1. The ADC analog input must not be overdriven. Using a signal amplitude slightly lower than FSR will allow a small amount of "headroom" so that noise or DC offset voltage will not overrange the ADC and "hard limit" on signal peaks. Overrange peaks will, however, just result in a constant full-scale digital output.
2. Two-tone tests can produce signal envelopes that exceed FSR. Set each test signal to slightly less than –6dB to prevent "hard limiting" on peaks.

3. Low-pass filtering (or bandpass filtering) of test signal generators is absolutely necessary for THD and IMD tests. An easily built LC low-pass filter (Figure 16) will eliminate harmonics from the test signal generator.
4. Test signal generators must have exceptional noise performance (better than –155dBc/Hz) to achieve accurate SNR measurements. Good generators together with fifth-order elliptical bandpass filters are recommended for SNR tests. Narrow bandwidth crystal filters can also be used to filter generator broadband noise but they should be carefully tested for operation at high levels.
5. The analog input of the ADC601 should be driven by a low output impedance S/H amplifier such as a SHC804. Short leads are necessary to prevent digital noise pickup.
6. A low-noise (jitter) clock signal (convert command) generator is required for good ADC dynamic performance. A poor generator can seriously impair good SNR performance. Short leads are necessary to preserve fast TTL rise times.
7. Two-tone testing will require isolation between test signal generators to prevent IMD generation in the test generator output circuits. An active summing amplifier using an OPA600 is shown in Figure 18. This circuit will provide excellent performance from DC to 5MHz with harmonic and intermodulation distortion products typically better than –70dBc. A passive (hybrid transformer) signal combiner can also be used (Figure 17) over a range of about 0.1MHz to 30MHz. This combiner's port-to-port isolation will be ≈45dB between signal generators and its input-output insertion loss will be ≈6dB. Distortion will be better than –85dBc for the powdered-iron core specified. Avoid ferrites. The circuits shown in Figures 17 and 18, have bandwidths beyond those required for the ADC601; therefore, they have even better performance at 500kHz. These combiners are always good additions to high-speed engineering labs.
8. A very low side-lobe window must be used for FFT calculations if generators cannot be phase-locked and set to exact frequencies. A minimum four-sample Blackman-Harris window function is recommended.[1]
9. Digital data may be latched into an external TTL 12-bit register by the status falling edge before the next convert command level. Latches should be mounted on PC boards in very close proximity to the ADC601. Avoid long leads.
10. Do not overload the data output logic. These outputs are designed to drive two TTL loads.
11. A well-designed, clean PC board layout will assure proper operation and clean spectral response. Proper grounding and bypassing, short lead lengths and separation of analog and digital signals and ground returns are particularly important for high frequency circuits. Multilayer PC boards are recommended for best performance, but a two-sided PC board with large, heavy (2oz-foil) ground planes can give excellent results, if carefully designed.
12. Prototyping "plug-boards" or wire-wrap boards will not be satisfactory. Request layout application notes from Burr-Brown.



9th Order 0.5dB Ripple
Tchebychev Low-Pass Filter

Attenuation at 2X cutoff frequency = 90dB.

Cutoff frequency = –3dB frequency; to convert cutoff frequency to –0.5dB frequency, multiply all LC values by 0.98997.

Cutoff Freq. (MHz)	C_1 (pF)	C_2 (pF)	C_3 (pF)	C_7 (pF)	C_9 (pF)	L_2 (H)	L_4 (H)	L_8 (H)	L_9 (H)
5.0	1134.6	1729.2	1765.6	1729.2	1134.6	2.056	2.216	2.216	2.056
2.5	2269	3458	3531	3458	2269	4.11	4.43	4.43	4.11
1.25	4538	6917	7062	6917	4538	8.23	8.86	8.86	8.23
0.625	9077	13,833	14,125	13,833	9077	16.45	17.73	17.73	16.45
0.50	11,346	17,292	17,656	17,292	11,346	20.56	22.16	22.16	20.56

FIGURE 16. Ninth-Order Harmonic Filter.

NOTES:

1. "On the Use of Windows for Harmonic Analysis with the Discrete Fourier Transform," Fredric J. Harris. *Proceedings of the IEEE*, Vol. 66, No. 1, January 1978, pp 51-83.
2. SINAD test includes harmonics whereas SNR does not include these important spurious products.
3. If IMD is referenced to peak envelope power, distortion will be of 6dB better.

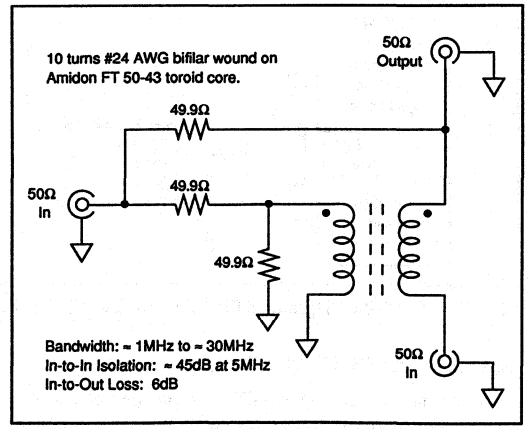


FIGURE 17. Passive Signal Combiner.

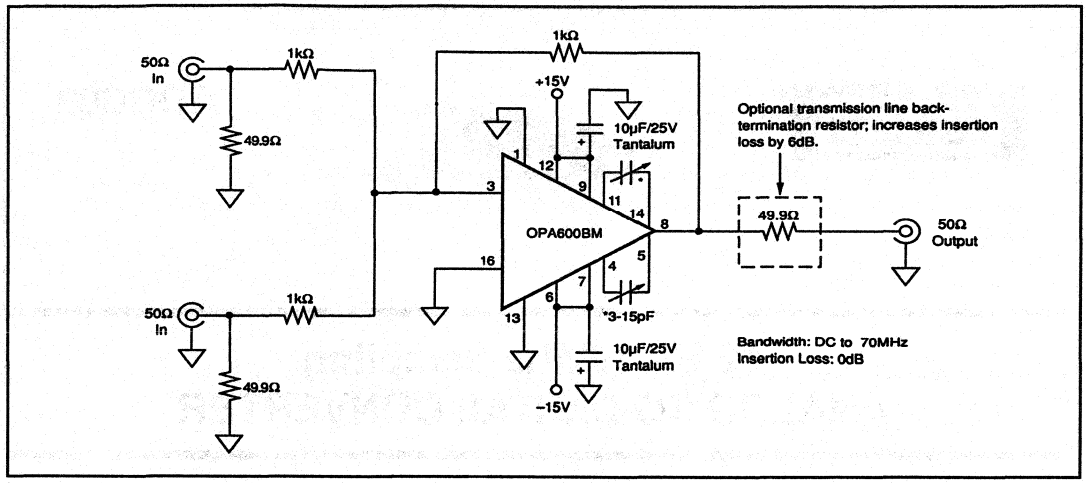


FIGURE 18. Active Signal Combiner.

BURR-BROWN®

ADC603

12-Bit 10MHz Sampling ANALOG-TO-DIGITAL CONVERTER

FEATURES

- HIGH SPURIOUS-FREE DYNAMIC RANGE
- SAMPLE RATE: DC to 10MHz
- HIGH SIGNAL/NOISE RATIO: 68.2dB
- HIGH SINAD RATIO: 66dB
- LOW HARMONIC DISTORTION: –69.6dBc
- LOW INTERMOD. DISTORTION: –77.7dBc
- COMPLETE SUBSYSTEM: Contains Sample/Hold and Reference
- 46-PIN DIP PACKAGE
- 0°C TO +70°C AND –55°C TO +125°C

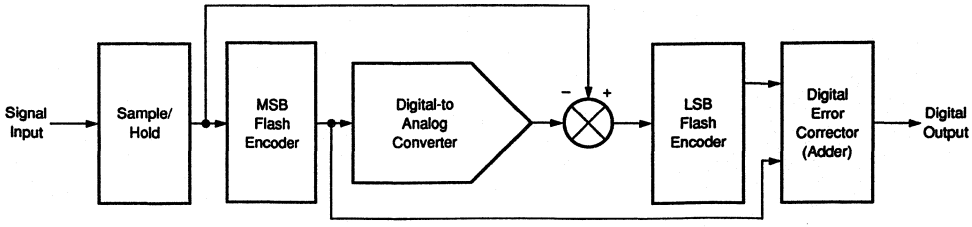
APPLICATIONS

- DIGITAL SIGNAL PROCESSING
- RADAR SIGNAL ANALYSIS
- TRANSIENT SIGNAL RECORDING
- FFT SPECTRUM ANALYSIS
- HIGH-SPEED DATA ACQUISITION
- IR IMAGING SYSTEMS
- DIGITAL RECEIVERS
- SIGINT, ECM, AND EW SYSTEMS
- DIGITAL OSCILLOSCOPES

DESCRIPTION

The ADC603 is an high performance analog-to-digital converter capable of digitizing signals at any rate from DC to 10 megasamples per second. Outstanding spurious-free dynamic range has been achieved by minimizing noise and distortion. Test summaries are furnished with each KH grade unit at no additional cost.

The ADC603 is a two-step subranging ADC subsystem containing an ADC, sample/hold amplifier, voltage reference, timing, and error-correction circuitry in a 46-pin hybrid DIP package. Logic is TTL. Two temperature ranges are available: 0°C to +70°C (JH, KH) and –55°C to +125°C (RH, SH).



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Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL

T_C = +25°C, 10MHz sampling rate, R_S = 50Ω, $\pm V_{CC}$ = ±15V, $+V_{DD1}$ = +5V, $-V_{DD2}$ = −5.2V, and 15-minute warmup in convection environment, unless otherwise noted.

PARAMETER	CONDITIONS	ADC603JH MIN	ADC603JH TYP	ADC603JH MAX	ADC603KH MIN	ADC603KH TYP	ADC603KH MAX	UNITS
RESOLUTION				12			12	Bits
INPUTS								
ANALOG								
Input Range	Full Scale	−1.25		+1.25	•		•	V
Input Impedance			1.5			•		MΩ
Input Capacitance			5			•		pF
DIGITAL								
Logic Family			TTL Compatible					
Convert Command	Start Conversion		Positive Edge					
Pulse Width	t = Conversion Period	10		t − 20	•		•	ns
TRANSFER CHARACTERISTICS								
ACCURACY								
Gain Error	f = 200Hz		±0.2	1		±0.1	0.8	%FSR[1]
Input Offset	DC		±0.2	0.75		•	0.5	%FSR
Integral Linearity Error	f = 200Hz		0.75			0.5	1	LSB
Differential Linearity Error	f = 200Hz: 68.3% of all Codes		0.3			0.25	0.5	LSB
	99.7% of all Codes		0.4			0.3	0.65	LSB
	100% of all Codes		0.5	1		0.4	0.75	LSB
No Missing Codes			Guaranteed			Guaranteed		
Power Supply Rejection	$\Delta +V_{CC}$ = ±10%		±0.03			•	±0.07	%FSR/%
	$\Delta -V_{CC}$ = ±10%		±0.04			•	±0.07	%FSR/%
	$\Delta +V_{DD1}$ = ±10%		±0.004			•	±0.03	%FSR/%
	$\Delta -V_{DD2}$ = ±10%		±0.01			•	±0.03	%FSR/%
CONVERSION CHARACTERISTICS								
Sample Rate		DC		10M	DC		10M	Samples/s
Pipeline Delay	Logic Selectable		1, 2 or 3 Convert Command Periods					
DYNAMIC CHARACTERISTICS								
Differential Linearity Error	f = 4.9MHz: 68.3% of all Codes		0.3			•		LSB
	99.7% of all Codes		0.75			0.5		LSB
	100% of all Codes		1	1.25		0.6	0.9	LSB
Spurious Free Dynamic Range								
f = 5MHz (−0.5dB)	f_S = 9.99MHz		−72	−63		−74	−66	dB
Total Harmonic Distortion[2](THD)								
f = 5MHz (−0.5dB)	f_S = 9.99MHz		−68	−61		−69.6	−64	dBc[3]
f = 100kHz			−70	−65		−72.1	−68	dBc
Two-Tone Intermodulation Distortion[2][4]								
f = 2.2MHz (−6.5dB)	f_S = 8.006MHz		−75	−67		−77.7	−71	dBc
f = 2.5MHz (−6.5dB)								
Signal-to-Noise and Distortion (SINAD) Ratio								
f = 5MHz (−0.5dB)	f_S = 9.99MHz	60	65		62	66		dB
f = 100kHz (−0.5dB)		64	67		66	68.5		dB
Signal-to-Noise Ratio (SNR)								
f = 5MHz (−0.5dB)	f_S = 9.99MHz	63	67		66	68.2		dB
f = 100kHz (−0.5dB)		66	68		67	70.1		dB
Aperture Delay Time			−5			•	+9	ns
Aperture Jitter			9			•	20	ps rms
Analog Input Bandwidth (−3dB)								
Small Signal	−20dB Input		70		50	•		MHz
Full Power	0dB Input		40		30	•		MHz
Overload Recovery Time	2x Full-Scale Input		80			•	140	ns
OUTPUTS								
Logic Family			TTL Compatible					
Logic Coding	Logic Selectable		Two's Complement or Inverted Two's Complement					
Logic Levels	Logic LO, I_{OL} = −3.2mA	0	+0.3	+0.8	0	+0.3	+0.5	V
	Logic HI, I_{OH} = 160µA	+2.4	+3.5	+5	+2.4	+3.5	+5	V
EOC Delay Time	Data Out to DV	5	35		5	35		ns
Tri-State Enable/Disable Time	I_{OL} = −6.4mA, 50% In to 50% Out		37	100		37	100	ns
Data Valid Pulse Width		20	45	60	20	45	60	ns
POWER SUPPLY REQUIREMENTS								
Supply Voltages: $+V_{CC}$	Operating	+14.25	+15	+15.75	+14.25	+15	+15.75	V
$-V_{CC}$		−14.25	−15	−15.75	−14.25	−15	−15.75	V
$+V_{DD1}$		+4.75	+5	+5.25	+4.75	+5	+5.25	V
$-V_{DD2}$		−4.95	−5.2	−5.46	−4.95	−5.2	−5.46	V
Supply Currents: $+I_{CC}$	Operating		+60			+60	+80	mA
$-I_{CC}$			−60			−60	−80	mA
$+I_{DD1}$			+280			+280	+330	mA
$-I_{DD2}$			−565			−565	−630	mA
Power Consumption	Operating		6.1			6.1		W

SPECIFICATIONS

ELECTRICAL (FULL TEMPERATURE RANGE SPECIFICATIONS)

$\pm V_{CC}$ = ±15V, $+V_{DD1}$ = +5V, $-V_{DD2}$ = –5.2V, R_S = 50Ω, 15-minute warmup, and $T_C = T_{MIN}$ to T_{MAX}, unless otherwise noted.

PARAMETER	CONDITIONS	ADC603JH			ADC603KH			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
TEMPERATURE RANGE								
Specification	T_{CASE}	0		+70	*		*	°C
TRANSFER CHARACTERISTICS								
ACCURACY								
Gain Error	f = 200Hz		±0.4	1.5		*	1	%FSR
Input Offset	DC		±0.4	1		*	0.5	%FSR
Integral Linear Error	f = 200Hz		0.75			0.6	1.25	LSB
Differential Linearity Error	f = 200Hz: 68.3% of all Codes		0.4			0.3	0.6	LSB
	99.7% of all Codes		0.5			0.4	0.75	LSB
	100% of all Codes		0.75			0.6	1	LSB
No Missing Codes			Guaranteed			Guaranteed		
Power Supply Rejection	$\Delta +V_{CC}$ = ±10%		±0.04			*	±0.08	%FSR/%
	$\Delta -V_{CC}$ = ±10%		±0.05			*	±0.08	%FSR/%
	$\Delta +V_{DD1}$ = ±10%		±0.004			*	±0.05	%FSR/%
	$\Delta -V_{DD2}$ = ±10%		±0.02			*	±0.05	%FSR/%
CONVERSION CHARACTERISTICS								
Sample Rate		DC		10M	DC		10M	Samples/s
DYNAMIC CHARACTERISTICS								
Differential Linearity Error	f = 4.9MHz: 68.3% of all Codes		0.5			0.4		LSB
	99.7% of all Codes		1			0.6		LSB
	100% of all Codes		1.25	1.5		0.7	1	LSB
Spurious Free Dynamic Range[5]	f = 5MHz (–0.5dB)		–65	–60		–72	–65	dB
Total Harmonic Distortion[2]								
f = 5MHz (–0.5dB)	f_S = 9.99MHz		–67	–58		–68.8	–62	dBc
f = 100kHz			–69	–62		–69.5	–67	dBc
Two-Tone Intermodulation Distortion								
f = 2.2MHz (–6.5dB)	f_S = 8.006MHz		–72	–64		–74.4	–68	dBc
f = 2.5MHz (–6.5dB)								
Signal-to-Noise and Distortion (SINAD) Ratio								
f = 5MHz (–0.5dB)	f_S = 9.99MHz	57	65		61	65.4		dB
f = 100kHz (–0.5dB)		62	66		64	66.5		dB
Signal-to-Noise Ratio (SNR)								
f = 5MHz (–0.5dB)	f_S = 9.99MHz	60	67		64	68		dB
f = 100kHz (–0.5dB)		64	68		66	69.5		dB
Aperture Delay Time			–6			*	+10	ns
Aperture Jitter			10			*	20	ps rms
Analog Input Bandwidth (–3dB)								
Small Signal	–20dB Input		70		50	*		MHz
Full Power	0dB Input		40		30	*		MHz
Overload Recovery Time	2x Full-Scale Input		80			*		ns
OUTPUTS								
Logic Levels	Logic LO, I_{OL} = –3.2mA	0	+0.3	+0.8	*	*	+0.5	V
	Logic HI, I_{OH} = 160µA	+2.4	+3.5	+5	*	*	*	V
EOC Delay Time	Data Out to DV	5	35		*	*		ns
Tri-State Enable/Disable Time	I_{OL} = –6.4mA, 50% In to 50% Out		42	100		*	*	ns
Data Valid Pulse Width		20	45	60	*	*	*	ns
POWER SUPPLY REQUIREMENTS								
Supply Currents: $+I_{CC}$	Operating		+65			*	+80	mA
$-I_{CC}$			–61			*	–80	mA
$+I_{DD1}$ [6]			+285			*	+333	mA
$-I_{DD2}$ [7]			–570			*	–630	mA
Power Consumption	Operating		6.1			*		W

* *Same specifications as ADC603JH/RH.*

NOTES: (1) FSR: Full-Scale Range = 2.5Vp-p. (2) Units with tested and guaranteed distortion specifications are available on special order—inquire. (3) dBC = level referred to carrier-input signal = 0dB); F = input frequency; F_S = sampling frequency. (4) IMD is referred to the larger of the two input test signals. If referred to the peak envelope signal (=0dB), the intermodulation products will be 6dB lower. (5) SFDR tested at temperature for K grade only. (6) Pins 3 and 30 (analog) typically draw 80% of the total +5V current. Pin 21 (digital) typically draws 20%. (7) Pin 6 (analog) typically draws 45% of the total –5.2V current. Pin 31 (digital) typically draws 55%.

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

SPECIFICATIONS

ELECTRICAL

T_C = +25°C, 10MHz sampling rate, R_S = 50Ω, $\pm V_{CC}$ = ±15V, $+V_{DD1}$ = +5V, $-V_{DD2}$ = −5.2V, and 15-minute warmup in convection environment, unless otherwise noted.

PARAMETER	CONDITIONS	ADC603RH[1] MIN	ADC603RH[1] TYP	ADC603RH[1] MAX	ADC603SH[1] MIN	ADC603SH[1] TYP	ADC603SH[1] MAX	UNITS
RESOLUTION				12			12	Bits
INPUTS								
ANALOG								
Input Range	Full Scale	−1.25		+1.25	*		*	V
Input Impedance			1.5			*		MΩ
Input Capacitance			5			*		pF
DIGITAL								
Logic Family			TTL Compatible					
Convert Command	Start Conversion		Positive Edge					
Pulse Width	t = Conversion Period	10		t − 20	*		*	ns
TRANSFER CHARACTERISTICS								
ACCURACY								
Gain Error	f = 200Hz		±0.2	±2		±0.1	± 1	%FSR[1]
Input Offset	DC		±0.2	±2		*	±0.75	%FSR
Integral Linearity Error	f = 200Hz		0.75			0.5	1	LSB
Differential Linearity Error	f = 200Hz:68.3% of all codes		0.3			0.25	0.5	LSB
	99.7% of all codes		0.4			0.3	0.65	LSB
	100% of all codes		0.5			0.4	0.75	LSB
No Missing Codes			Guaranteed			Guaranteed		
Power Supply Rejection	$\Delta +V_{CC}$ = ±10%		±0.03			*	±0.125	%FSR/%
	$\Delta -V_{CC}$ = ±10%		±0.04			*	±0.125	%FSR/%
	$\Delta +V_{DD1}$ = ±10%		±0.004			*	±0.03	%FSR/%
	$\Delta -V_{DD2}$ = ±10%		±0.01			*	±0.03	%FSR/%
CONVERSION CHARACTERISTICS								
Sample Rate		DC		10M	DC		10M	Samples/s
Pipeline Delay	Logic Selectable		1, 2 or 3 Convert Command Periods					
DYNAMIC CHARACTERISTICS								
Differential Linearity Error	f = 4.9MHz: 68.3% of all codes		0.3			*	0.5	LSB
	99.7% of all codes		0.75			0.5	1	LSB
	100% of all codes		1			0.6	1.25	LSB
Total Harmonic Distortion[2](THD)								
f = 5MHz (−0.5dB)	f_S = 9.99MHz		−68			−69.6	−64	dBc[3]
f = 100kHz			−70			−72.1	−66	dBc
Two-Tone Intermodulation Distortion[2][4]								
f = 2.2MHz (−6.5dB)	f_S = 8.006MHz		−75			−77.7	−71	dBc
f = 2.5MHz (−6.5dB)								
Signal-to-Noise and Distortion								
(SINAD) Ratio								
f = 5MHz (−0.5dB)	f_S = 9.99MHz		65		62	66		dB
f = 100kHz (−0.5dB)			67		64	68.5		dB
Signal-to-Noise Ratio (SNR)								
f = 5MHz (−0.5dB)	f_S = 9.99MHz		67		64	68.2		dB
f = 100kHz (−0.5dB)			68		66	70.1		dB
Aperture Delay Time			−5			*	+9	ns
Aperture Jitter			9			*	20	ps rms
Analog Input Bandwidth (−3dB)								
Small Signal	−20dB input		70		50	*		MHz
Full Power	0dB input		40		30	*		MHz
Overload Recovery Time	2x Full-Scale Input		80			*	140	ns
Logic Family			TTL Compatible					
Logic Coding	Logic Selectable		Two's Complement or Inverted Two's Complement					
Logic Levels	Logic LO, I_{OL} = −3.2mA	0	+0.3	+0.8	0	+0.3	+0.5	V
	Logic HI, I_{OH} = 160µA	+2.4	+3.5	+5	+2.4	+3.5	+5	V
EOC Delay Time	Data Out to DV	5	35		5	35		ns
Tri-State Enable/Disable Time	I_{OL} = −6.4mA, 50% In to 50% Out		37	100		37	100	ns
Data Valid Pulse Width		20	45	60	20	45	60	ns
Supply Voltages: $+V_{CC}$	Operating	+14.25	+15	+15.75	+14.25	+15	+15.75	V
$-V_{CC}$		−14.25	−15	−15.75	−14.25	−15	−15.75	V
$+V_{DD1}$		+4.75	+5	+5.25	+4.75	+5	+5.25	V
$-V_{DD2}$		−4.95	−5.2	−5.46	−4.95	−5.2	−5.46	V
Supply Currents: $+I_{CC}$	Operating		+60			+60	+80	mA
$-I_{CC}$			−60			−60	−80	mA
$+I_{DD1}$			+280			+280	+330	mA
$-I_{DD2}$			−565			−565	−630	mA
Power Consumption	Operating		6.1			6.1		W

NOTE: (1) Inquire for availability of extended temperature range versions.

SPECIFICATIONS

ELECTRICAL (FULL TEMPERATURE RANGE SPECIFICATIONS)

$\pm V_{CC}$ = ±15V, $+V_{DD1}$ = +5V, $-V_{DD2}$ = –5.2V, R_S = 50Ω, 15-minute warmup, and $T_C = T_{MIN}$ to T_{MAX}, unless otherwise noted.

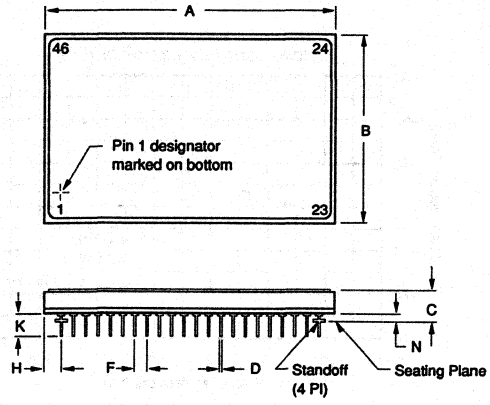
PARAMETER	CONDITIONS	ADC603RH[3] MIN	ADC603RH[3] TYP	ADC603RH[3] MAX	ADC603SH[3] MIN	ADC603SH[3] TYP	ADC603SH[3] MAX	UNITS
TEMPERATURE RANGE								
Specification	T_{CASE}	–55		+125	*		*	°C
TRANSFER CHARACTERISTICS								
ACCURACY								
Gain Error	f = 200Hz		±0.4	±2		*	±1.5	%FSR
Input Offset	DC		±0.4	±2		*	±1	%FSR
Integral Linear Error	f = 200Hz		0.75			0.6	1.25	LSB
Differential Linearity Error	f = 200Hz: 68.3% of all codes		0.4			0.3	0.6	LSB
	99.7% of all codes		0.5			0.4	0.75	LSB
	100% of all codes		0.75			0.6	1	LSB
No Missing Codes			Guaranteed			Guaranteed		
Power Supply Rejection	$\Delta +V_{CC}$ = ±10%		±0.04			*	±0.08	%FSR/%
	$\Delta -V_{CC}$ = ±10%		±0.05			*	±0.08	%FSR/%
	$\Delta +V_{DD1}$ = ±10%		±0.004			*	±0.05	%FSR/%
	$\Delta -V_{DD2}$ = ±10%		±0.02			*	±0.05	%FSR/%
CONVERSION CHARACTERISTICS								
Sample Rate		DC		10M	DC		10M	Samples/s
DYNAMIC CHARACTERISTICS								
Differential Linearity Error	f = 4.9MHz: 68.3% of all codes		0.5			0.4	0.75	LSB
	99.7% of all codes		1			0.6	1.25	LSB
	100% of all codes		1.25			0.7	1.5	LSB
Total Harmonic Distortion[2]								
f = 5MHz (–0.5dB)	f_S = 9.99MHz		–67			–68.8	–62	dBc
f = 100kHz			–69			–69.5	–64	dBc
Two-Tone Intermodulation Distortion								
f = 2.2MHz (–6.5dB)	f_S = 8.006MHz		–72			–74.4	–68	dBc
f = 2.5MHz (–6.5dB)								
Signal-to-Noise and Distortion								
(SINAD) Ratio								
f = 5MHz (–0.5dB)	f_S = 9.99MHz		65		60	65.4		dB
f = 100kHz (–0.5dB)			66		62	66.5		dB
Signal-to-Noise Ratio (SNR)								
f = 5MHz (–0.5dB)	f_S = 9.99MHz		67		62	68		dB
f = 100kHz (–0.5dB)			68		64	69.5		dB
Aperture Delay Time			–6			*	+10	ns
Aperture Jitter			10			*	20	ps rms
Analog Input Bandwidth (–3dB)								
Small Signal	–20dB Input		70		50	*		MHz
Full Power	0dB Input		40		30	*		MHz
Overload Recovery Time	2x Full-Scale Input		80			*		ns
OUTPUTS								
Logic Levels	Logic LO, I_{OL} = –3.2mA	0	+0.3	+0.8	*	*	+0.5	V
	Logic HI, I_{OH} = 160µA	+2.4	+3.5	+5	*	*	*	V
EOC Delay Time	Data Out to DV	5	35		*	*		ns
Tri-State Enable/Disable Time	I_{OL} = –6.4mA, 50% In to 50% Out		42	100		*	*	ns
Data Valid Pulse Width		20	45	60	*	*	*	ns
POWER SUPPLY REQUIREMENTS								
Supply Currents: $+I_{CC}$	Operating		+65			*	+80	mA
$-I_{CC}$			–61			*	–80	mA
$+I_{DD1}$			+285			*	+333	mA
$-I_{DD2}$			–570			*	–630	mA
Power Consumption	Operating		6.1			*		W

* Same specifications as ADC603JH/RH

NOTES: (1) FSR: Full-Scale Range = 2.5Vp-p. (2) Units with tested and guaranteed distortion specifications are available on special order—Inquire. (3) dBC = level referred to carrier-input signal = 0dB); F = input frequency; F_S = sampling frequency. (4) IMD is referred to the larger of the two input test signals. If referred to the peak envelope signal (=0dB), the intermodulation products will be 6dB lower. (5) Inquire for availability of extended temperature versions.

MECHANICAL

H Package — Metal and Ceramic



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	2.370	2.420	60.20	61.47
B	1.560	1.610	39.62	40.89
C	.200	.260	5.08	6.60
D	.018 Dia BASIC		0.46 Dia BASIC	
F	.100 BASIC		2.54 BASIC	
H	0.75	.115	1.91	2.92
K	.150	.190	3.81	4.83
L	1.300 BASIC		33.02 BASIC	
M	—	10°	—	10°
N	.040	.060	1.02	1.52

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.

PIN ASSIGNMENTS

1	Common (Case)	46	Common (Analog)
2	NC	45	Analog Signal In
3	$+V_{DD1}$ (+5V) Analog	44	$+V_{CC}$ (+15V) Analog
4	S/H Out	43	$-V_{CC}$ (–15V) Analog
5	A/D In	42	NC
6	$-V_{DD2}$ (–5.2V) Analog	41	NC
7	NC	40	NC
8	NC	39	DNC
9	Bit 1(MSB)	38	DNC
10	Bit 2	37	Gain Adjust
11	Bit 3	36	Offset Adjust
12	Bit 4	35	Common (Analog)
13	Bit 5	34	$+V_{CC}$ (+15V) Analog
14	Bit 6	33	$-V_{CC}$ (–15V) Analog
15	Bit 7	32	Common (Analog)
16	Bit 8	31	$-V_{DD2}$ (–5.2V) Digital
17	Bit 9	30	$+V_{DD1}$ (+5V) Analog
18	Bit 10	29	1 Pipeline Delay Select
19	Bit 11	28	0 Pipeline Delay Select
20	Bit 12 (LSB)	27	Output Logic Invert
21	$+V_{DD1}$ (+5V) Digital	26	Common (Digital)
22	Data Valid Output	25	Tri-State $\overline{\text{ENABLE}}$
23	Common (Digital)	24	Convert Command In

ORDERING INFORMATION

ADC603 ( ) H

Basic Model Number

Performance Grade Code
- J, K: 0°C to +70°C Case Temperature
- R, S: –55°C to +125°C Case Temperature

Package Code
- H: Metal and Ceramic

ABSOLUTE MAXIMUM RATINGS

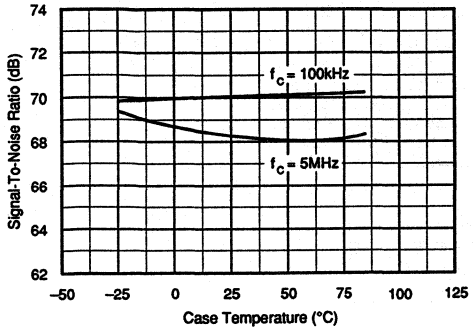
$\pm V_{CC}$	±16.5V
$+V_{DD1}$	+7V
$\pm V_{DD2}$	–7V
Analog Input	±5V
Logic Input	–0.5V to $+V_{DD1}$
Case Temperature	+125°C
Junction Temperature	+165°C
Storage Temperature	–65°C to +165°C

Stresses above these ratings may permanently damage the device.

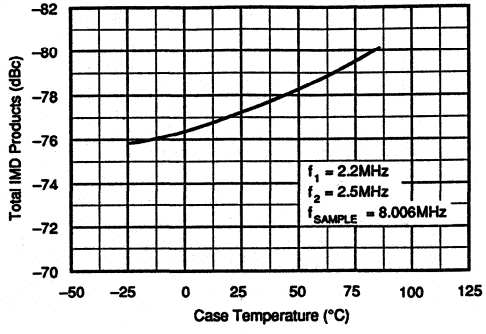
TYPICAL PERFORMANCE CURVES

$\pm V_{CC}$ = ±15V, $+V_{DD1}$ = +5V, $-V_{DD2}$ = −5.2V, R_S = 50Ω, 15-minute warmup, and T_C = +25°C, unless otherwise noted. All plots are 4096 point FFTs.

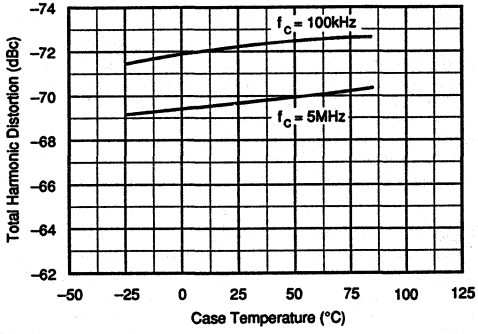
SIGNAL-TO-NOISE RATIO vs TEMPERATURE



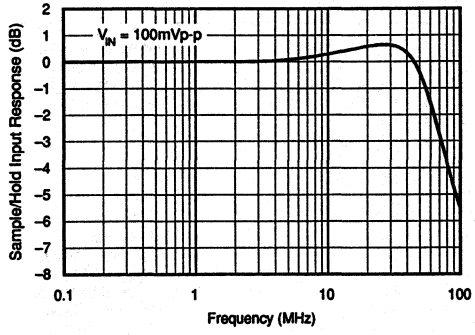
TWO-TONE IMD vs TEMPERATURE



TOTAL HARMONIC DISTORTION vs TEMPERATURE



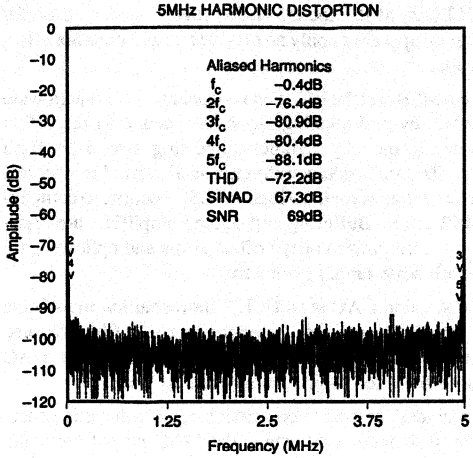
ANALOG INPUT BANDWIDTH



TYPICAL PERFORMANCE CURVES (CONT)

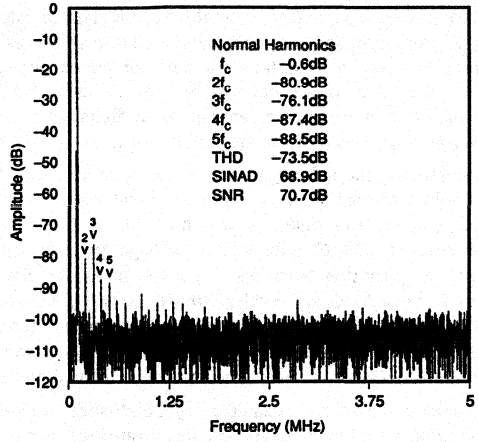
$\pm V_{CC}$ = ±15V, $+V_{DD1}$ = +5V, $-V_{DD2}$ = –5.2V, R_S = 50Ω, 10MHz sample rate, 15-minute warmup, and T_C = +25°C, unless otherwise noted. All plots are 4096-point FFTs.

5MHz HARMONIC DISTORTION



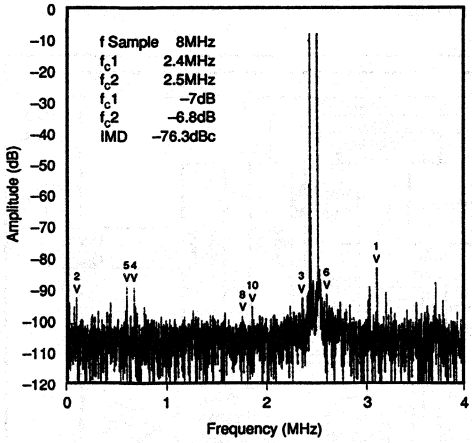
NOTE: Sample rate = 9.99 MHz; even harmonics folded to left edge and odd harmonics folded to right edge. Any non-harmonically related spurious products show clearly in the center.

100kHz HARMONIC DISTORTION



NOTE: Sample rate = 9.99 MHz; harmonics appear in normal order.

TWO-TONE INTERMODULATION DISTORTION



NOTE: Sample rate = 8MHz; highest IMD product is cursor number 1: f1 +f2. The second-order –76.3dBc product determines the wideband spurious-free dynamic range of this example. For RF applications third-order IMD products such as those at cursors 3 and 6 are the limiting spurs. Under these conditions spurious-free dynamic range is limited by 2f2+ f1 to 84.3dBc.

Sample rates of 10MHz show similar results.

TWO-TONE INTERMODULATION DISTORTION PRODUCTS

CURSOR	IMD	FREQUENCY	dB
1	2nd order : f1 + f2	3.086395621579MHz	–83.1
2	2nd order : f2 – f1	0.080140734949MHz	–91.4
3	3rd order : 2f1 – f2	2.339718530102MHz	–92.4
4	3rd order : 2f1 + f2	0.666536356529MHz	–88.4
5	3rd order : 2f2 – f1	0.586395621579MHz	–88.2
6	3rd order : 2f2 + f1	2.580140734949MHz	–91.1
7	4th order : 3f1 – f2	3.246677091478MHz	–109
8	4th order : 3f1 + f2	1.753322908522MHz	–100
9	4th order : 2f2 – 2f1	0.130281469898MHz	–114.8
10	4th order : 2f2 + 2f1	1.833463643471MHz	–95
11	4th order : 3f2 – f1	2.926114151681MHz	–115.4
12	4th order : 3f2 + f1	1.913604378421MHz	–98.2

NOTE: IMD products in this table are refered to full-scale (0dB). To refer IMD to carrier, subtract the larger of f_c1 or f_c2. In this example, IMD referred to carrier will be 6.8dB higher (worse) than the full-scale value shown.

THEORY OF OPERATION

The ADC603 is a two-step subranging analog-to-digital converter. This architecture is shown in Figure 1. The major system building blocks are: sample/hold amplifier, MSB flash encoder, DAC and error amplifier, LSB flash encoder, digital error corrector, and timing circuits. The ADC603 uses hybrid technology with laser-trimmed integrated circuits mounted in a multilayer ceramic package to integrate this complex circuit into a complete analog-to-digital converter subsystem with state-of-the-art performance.

Conceptually, the subranging technique is simple: sample and hold the input signal, convert to digital with a coarse ADC, convert back to analog with a coarse-resolution (but high-accuracy) DAC, subtract this voltage from the S/H output, amplify this "remainder," convert to digital with a second coarse ADC, and combine the digital output from the first ADC (MSB) with the digital output from the second ADC (LSB). In practice, however, achieving high conversion speed without sacrificing accuracy is a difficult task.

The analog input signal is sampled by a high-speed sample/hold amplifier with low distortion, fast acquisition time and very low aperture uncertainty (jitter). A diode bridge sampling switch is used to achieve an acceptable compromise between speed and accuracy. The diode bridge switching transients are buffered from the analog input by a high input impedance buffer amplifier. Since the hold capacitor does not appear in the feedback of the diode bridge output buffer, the capacitor can acquire the signal in 25ns. The low-bias-current output buffer is then required to settle to only the resolution (7 bits) of the first (MSB) flash encoder in 25ns, while an additional 60ns is allowed for settling to the resolution (12 bits) of the second (LSB) flash encoder. Sample/hold droop appears as only an offset error and does not effect linearity.

Both the MSB and the LSB flash encoder (ADC) function are performed by multiplexing one high-speed 7-bit resolution converter formed by parallel-connecting two 6-bit flash ADCs. The DAC voltage reference is also used to generate reference voltages for the MSB and LSB encoder to compensate drift errors. Buffering and scaling amplifiers are laser-trimmed to minimize voltage offset errors and optimize gain (input full-scale range) symmetry.

The subtraction DAC is an ECL 7-bit resolution monolithic DAC with 14-bit accuracy. Laser-trimmed thin-film nichrome resistors and high-speed bipolar circuitry allow the DAC output to settle to 14-bit accuracy in only 35ns.

A "remainder" or coarse conversion-error voltage is generated by resistively subtracting the DAC output from the output of the sample/hold amplifier. Before the second (LSB) conversion, the "remainder" is amplified by a wideband fast-settling two-input amplifier with a gain of 32V/V. To prevent overload on large amplitude transients, the active input is switched off to blank the amplifier input from the beginning of the S/H acquisition time to the end of the MSB encoder update time.

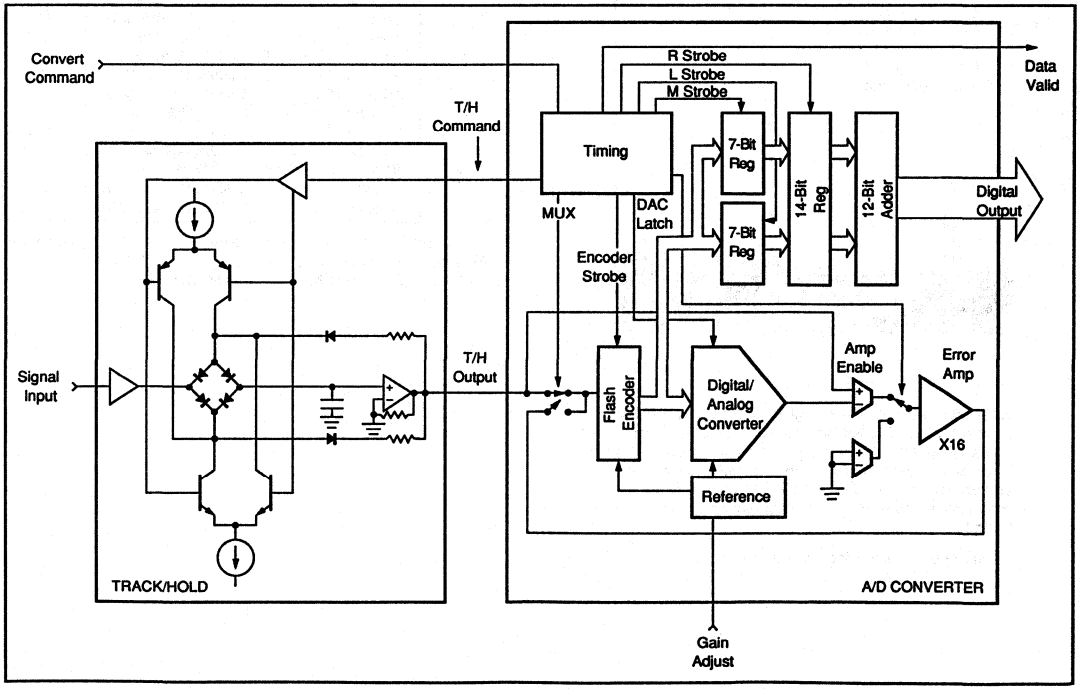


FIGURE 1. ADC603 Block Diagram—A Two-Step Subranging Architecture.

Internal timing circuits (ECL logic is used internally) supply all the critical timing signals necessary for proper operation of the ADC603. Some noncritical timing signals are also generated in the digital error correction circuitry. Timing signals are laser-trimmed for both pulse width and delay. ECL logic is used for its speed, low noise characteristics and timing delay stability over a wide range of temperatures and power supply voltages. Basic timing is derived from the output of a three-stage shift register driven by a synchronized 20MHz oscillator.

The convert command pulse is differentiated to allow triggering by pulses from as narrow as 10ns to as wide as 80% duty cycle.

The ADC603 timing technique generates a variable width S/H gate pulse which is determined by the conversion command pulse period minus a fixed 67ns ADC conversion time. ADC603 conversion rates are therefore possible somewhat above the 10MHz specification, but S/H acquisition time is sacrificed and accuracy is rapidly degraded. Converters with guaranteed operation at 10.24MHz sample rate are available on special order.

The output of the MSB and LSB encoders are read into separate 7-bit latches. The latched MSB data, along with the latched LSB data, is then read into a 14-bit latch after the leading edge of the LSB strobe and before being applied to the adder, where the actual error correction takes place. These latches eliminate any critical timing problems that could result when the converter is operated at the maximum conversion rate.

The function of the digital error correction circuitry is to assemble the 7-bit words from the two flash encoders into a 12-bit output word. A data valid (DV) pulse is also generated which is used to indicate when output data can be latched into an external register. This DV pulse is delayed 6ns after the output data has settled to allow sufficient set-up time for an external TTL data latch. A high-speed latch such as a 74F174 is recommended.

The 14-bit register output is then sent to a 12-bit adder where the final data output word is created. The MSB data forms the most significant seven bits of a 12-bit word, with the last five bits being assigned zeros. In a similar fashion, the LSB data from the least significant bits forms the other input to the adder, with the first five bits being assigned zeros. As two 12-bit words are being added, the output of the adder could exceed 12 bits in range; however, the final data output is only a 12-bit word, so a means of detecting an overrange is included to prevent reading erroneous data. The converter data output is forced to all ones for a full-scale input or overrange. The data output does not "roll-over" if the converter input exceeds its specified full-scale range of ±1.25V.

DISCUSSION OF PERFORMANCE

DYNAMIC PERFORMANCE TESTING

The ADC603 is a very high performance converter and careful attention to test techniques is necessary to achieve accurate results. Spectral analysis by application of a fast Fourier transform (FFT) to the ADC digital output will provide data on all important dynamic performance parameters: total harmonic distortion (THD), signal-to-noise ratio (SNR) or the more severe signal-to-noise-and-distortion ratio (SINAD), and intermodulation distortion (IMD).

A typical test setup for performing high-speed FFT testing of analog-to-digital converters is shown in Figure 2. Highly accurate phase-locked signal sources allow high resolution FFT measurements to be made without using window functions. By choosing appropriate signal frequencies and sample rates, an integral number of signal frequency periods can be sampled. As no spectral leakage results, a "rectangular" window (no window function) can be used. This was used to generate the typical FFT performance curves shown on page 5.

If generators cannot be phase-locked and set to extreme accuracy, a very low side-lobe window must be applied to the digital data before executing an FFT. A commonly used window such as the Hanning window is not appropriate for testing high performance converters; a minimum four-sample Blackman-Harris window is strongly recommended.[1] To

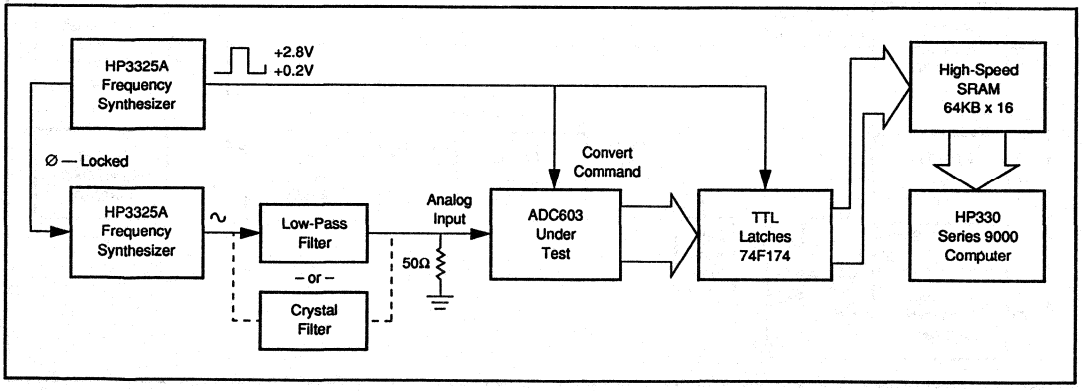


FIGURE 2. Block Diagram of FFT Test for THD, SNR, and SINAD.

assure that the majority of codes are exercised in the ADC603 (12 bits), a 4096-point FFT is taken. If the data storage RAM is limited, a smaller FFT may be taken if a sufficient number of samples are averaged (i.e., a 10-sample average of 512-point FFTs).

Dynamic Performance Definitions

1. Signal-to-Noise-and-Distortion[2] Ratio (SINAD):

$$10 \log \frac{\text{Sinewave Signal Power}}{\text{Noise + Harmonic Power (first 9 harmonics)}}$$

2. Signal-to-Noise Ratio (SNR):

$$10 \log \frac{\text{Sinewave Signal Power}}{\text{Noise Power}}$$

3. Total Harmonic Distortion (THD):

$$10 \log \frac{\text{Harmonic Power (first 9 harmonics)}}{\text{Sinewave Signal Power}}$$

4. Intermodulation Distortion (IMD):

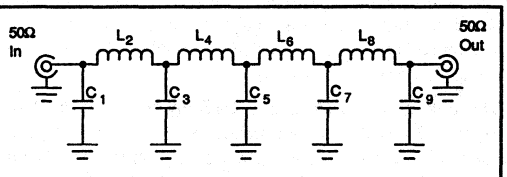
$$10 \log \frac{\text{Highest IMD Product Power (to 5th order)}}{\text{Sinewave Signal Power}}$$

IMD is referenced[3] to the larger of the test signals f_1 or f_2. Five "bins" either side of peak are used for calculation of fundamental and harmonic power. The "0" frequency bin (DC) is not included in these calculations as it is of little importance in dynamic signal processing applications.

APPLICATION TIPS

Attention to test set-up details can prevent errors that contribute to poor test results. Important points to remember when testing high performance converters are:

1. The ADC analog input must not be overdriven. Using a signal amplitude slightly lower than FSR will allow a small amount of "headroom" so that noise or DC offset voltage will not overrange the ADC and "hard limit" on signal peaks.
2. Two-tone tests can produce signal envelopes that exceed FSR. Set each test signal to slightly less than –6dB to prevent "hard limiting" on peaks.
3. Low-pass filtering (or bandpass filtering) of test signal generators is absolutely necessary for THD and IMD tests. An easily built LC low-pass filter (Figure 4) will eliminate harmonics from the test signal generator.
4. Test signal generators must have exceptional noise performance (better than –155dBC/Hz) to achieve accurate SNR measurements.[4] Good generators together with fifth-order elliptical bandpass filters are recommended for



9th Order 0.5dB Ripple
Tchebychev Low-Pass Filter

Attenuation at 2x cutoff frequency = 90dB.

Cutoff frequency = –3dB frequency; to convert cutoff frequency to –0.5dB frequency, multiply all LC values by 0.98997.

CUTOFF FREQ. (MHz)	C_1 (pF)	C_3 (pF)	C_5 (pF)	C_7 (pF)	C_9 (pF)	L_2 (H)	L_4 (H)	L_6 (H)	L_8 (H)
5	1134.6	1729.2	1765.6	1729.2	1134.6	2.056	2.216	2.216	2.056
2.5	2269	3458	3531	3458	2269	4.11	4.43	4.43	4.11
1.25	4538	6917	7062	6917	4538	8.23	8.86	8.86	8.23
0.625	9077	13,833	14,125	13,833	9077	16.45	17.73	17.73	16.45

FIGURE 4. Ninth-Order Harmonic Filter.

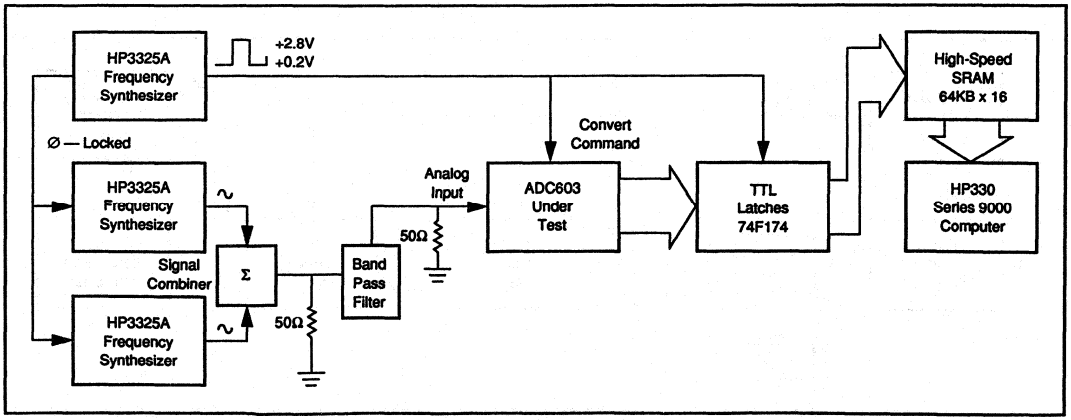


FIGURE 3. Block Diagram of FFT Test for Two-Tone IMD.

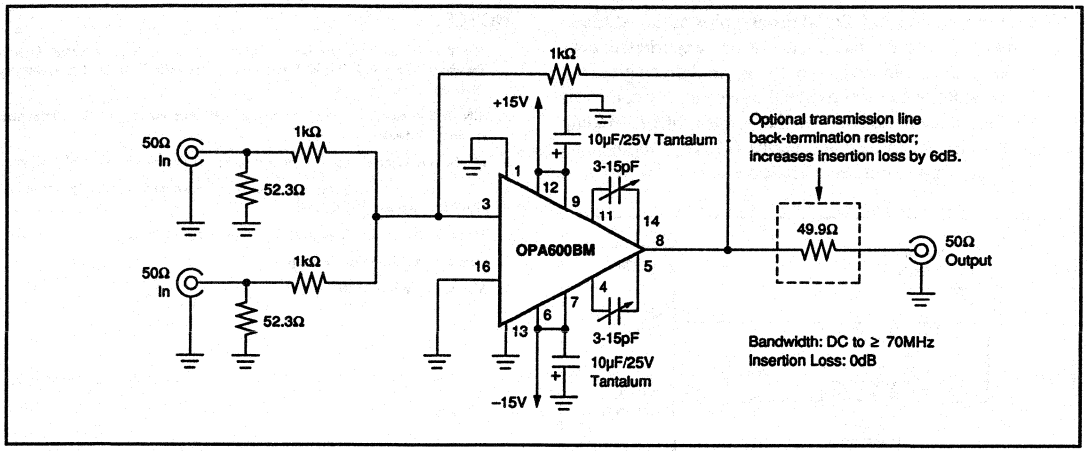


FIGURE 5. Active Signal Combiner.

SNR tests. Narrow-bandwidth crystal filters can also be used to filter generator broadband noise, but they should be carefully tested for operation at high levels.

5. The analog input of the ADC603 should be terminated directly at the input pin sockets with the correct filter terminating impedance (50Ω or 75Ω), or it should be driven by a low output impedance buffer such as an OPA675/676, OPA620/621, or OPA600. Short leads are necessary to prevent digital noise pickup.
6. A low-noise (jitter) clock signal (convert command) generator is required for good ADC dynamic performance. A poor generator can seriously impair good SNR performance. Short leads are necessary to preserve fast TTL rise times.
7. Two-tone testing will require isolation between test signal generators to prevent IMD generation in the test generator output circuits. An active summing amplifier using an OPA600 is shown in Figure 5. This circuit will provide excellent performance from DC to 5MHz with harmonic and intermodulation distortion products typically better than –70dBC. A passive (hybrid transformer) signal combiner can also be used (Figure 6) over a range of about 0.1MHz to 30MHz. This combiner's port-to-port isolation will be ≈45dB between signal generators and its input-output insertion loss will be ≈6dB. Distortion will be better than –85dBC for the powdered-iron core specified. Avoid ferrites.
8. A very low side-lobe window must be used for FFT calculations if generators cannot be phase-locked and set to exact frequencies. A minimum four-sample Blackman-Harris window function is recommended.[1]
9. Digital data must be latched into an external TTL 12-bit register by the Data Valid output pulse or by using the convert command pulse (Figures 11, 12, 13, and 14). Latches should be mounted on PC boards in very close proximity to the ADC603. Avoid long leads.

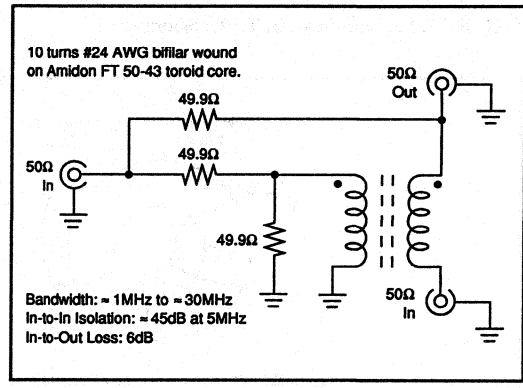


FIGURE 6. Passive Signal Combiner.

10. Do not overload the data output logic. These outputs are designed to drive 2 TTL loads. Do not connect ADC603 data output pins directly to a noisy digital bus; use external 3-state logic for noise immunity.
11. A well-designed, clean PC board layout will assure proper operation and clean spectral response.[5, 6] Proper grounding and bypassing, short lead lengths, separation of analog and digital signals, and the use of ground planes are particularly important for high frequency circuits. Multilayer PC boards are recommended for best performance, but a two-sided PC board with large, heavy (2oz-foil) ground planes can give excellent results, if carefully designed.
12. Prototyping "plug-boards" or wire-wrap boards will not be satisfactory.
13. Floating inputs can eliminate ground-loop noise. A simple common-mode choke (balun) shown in Figure 7 and 8, or a differential amplifier (Figure 9 and 10) can reduce analog input noise.

14. Connect analog and digital ground pins of the ADC603 directly to the ground plane. In our experience, connecting these pins to a common ground plane gives the best results. Analog and digital power supply commons should be tied together at the ground plane. Adding power supply and ground-return filtering[7] is optional and may improve noise rejection.

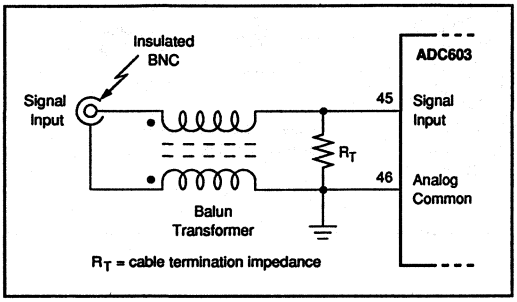


FIGURE 7. Floating-Input Balun Transformer.

NOTES:

1. "On the Use of Windows for Harmonic Analysis with the Discrete Fourier Transform", Fredric J. Harris. *Proceedings of the IEEE*, Vol. 66, No. 1, January 1978, pp 51-83.
2. SINAD test includes harmonics whereas SNR does not include these important spurious products.
3. If IMD is referenced to peak envelope power, distortion will be of 6dB better.
4. "Test Report: FFT Characterization of Burr-Brown ADC600K", Signal Conversion Ltd., Swansea, Wales, U.K.
5. *MECL System Design Handbook*, 3rd Edition, Motorola Corp.
6. Motorola MECL, Motorola Corp.
7. Murata-Erie BNX002-01.

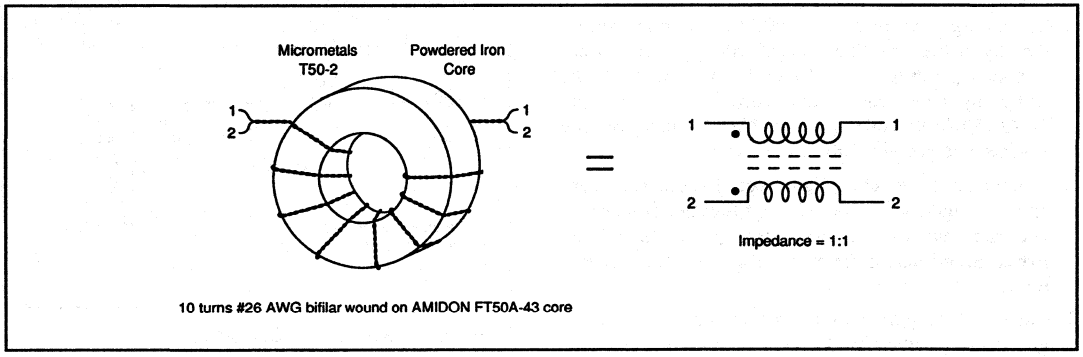


FIGURE 8. Balun Transformer Windings.

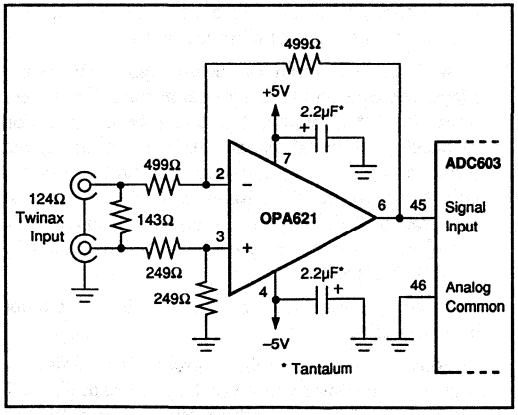


FIGURE 9. Differential Input Buffer Amplifier (Gain = –1V/V).

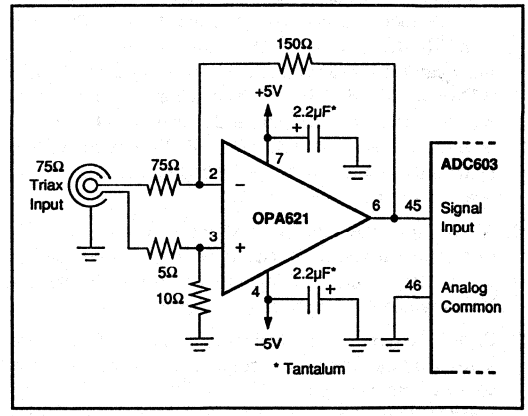


FIGURE 10. Differential Input Buffer Amplifier (Gain = –2V/V).

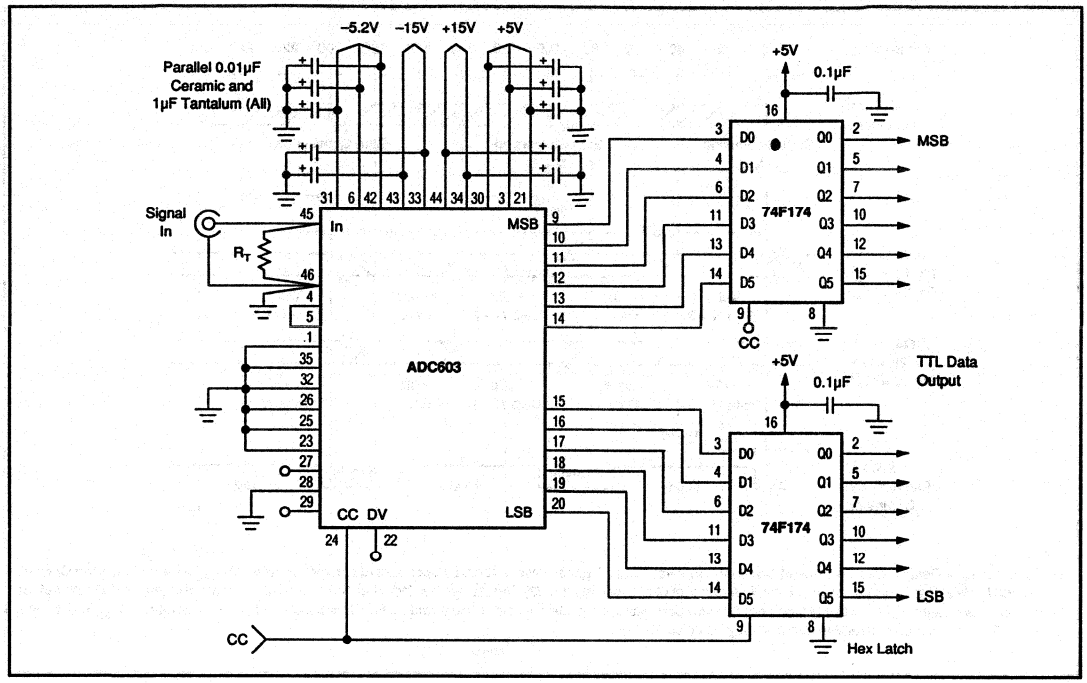


FIGURE 11. Interface Circuit—Digital Output Strobed by Convert Command. Supply connection shown: power supplies and grounds shared by analog and digital pins using common ground plane (recommended circuit).

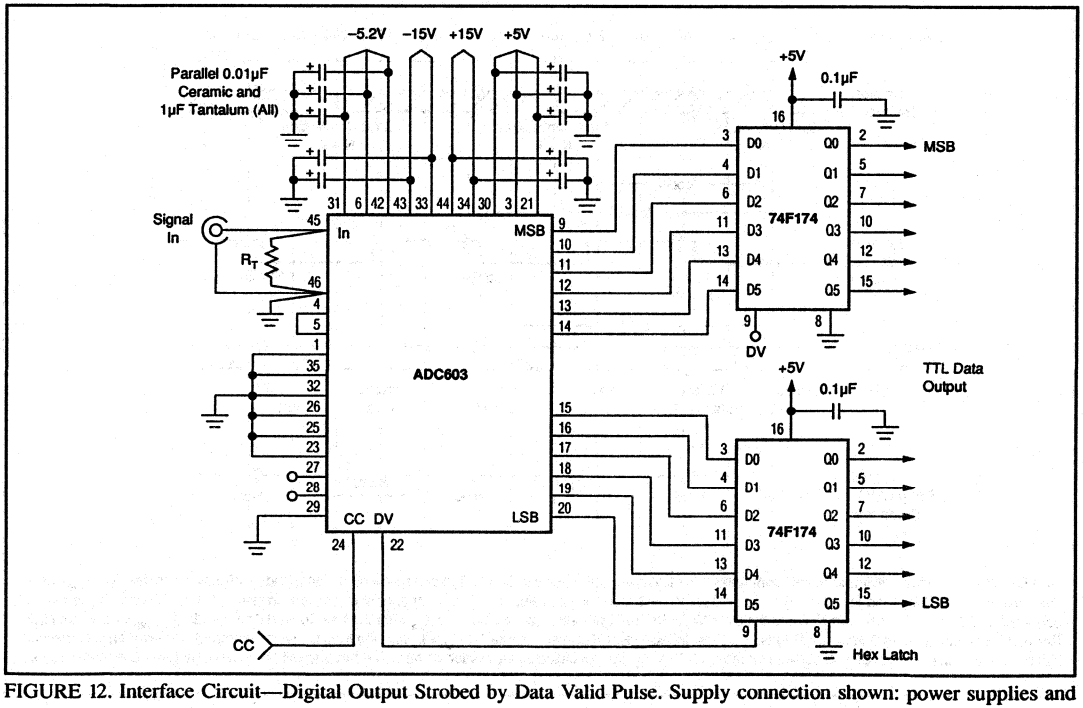
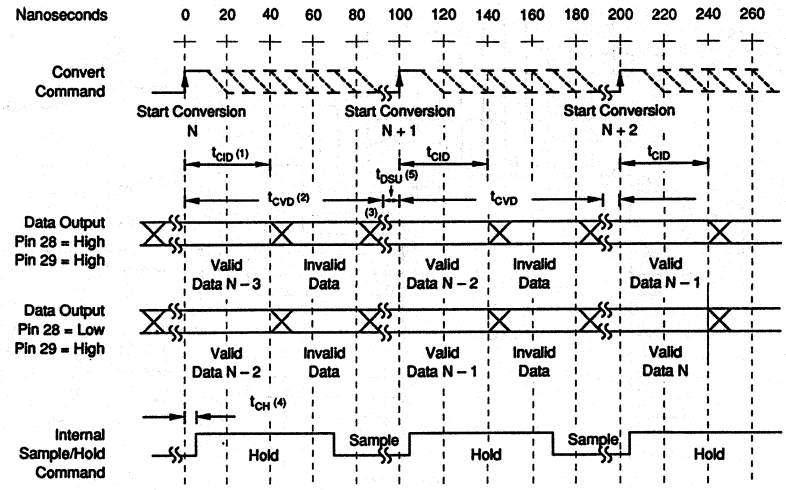


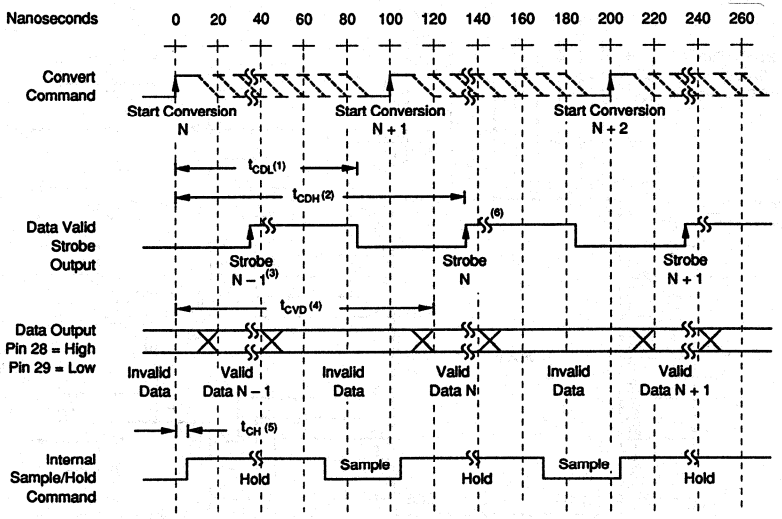
FIGURE 12. Interface Circuit—Digital Output Strobed by Data Valid Pulse. Supply connection shown: power supplies and grounds shared by analog and digital pins using common ground plane.



NOTES: (1) t_{CID} = Delay time from Convert Command to Invalid Data. Typical value = 40ns. Independent of conversion rate. (2) t_{CVD} = Delay time from Convert Command to Valid Data. Typical value = 93ns. Independent of conversion rate. (3) The ⟆ symbol indicates the portion of the waveform that will "stretch out" at lower conversion rates. (4) t_{CH} = Delay time from Convert Command to the internal hold. Typical value = 6ns. Independent of conversion rate. (5) t_{DSU} = data set-up time. This depends on conversion rate and may be calculated by:

$$t_{DSU} = \frac{1}{f_{SAMPLE}} - t_{CVD}$$

FIGURE 13. Convert Command Strobe Timing.



NOTES: (1) t_{CDL} = Delay time from Convert Command to the falling edge of Data Valid Strobe. Typical value = 85ns. Independent of conversion rate. (2) t_{CDH} = Delay time from Convert Command to the rising edge of Data Valid Strobe. Typical value = 135ns. Independent of conversion rate. (3) If Conversion "N" is the first conversion, then there is no Strobe N-1, and the Data Valid Strobe Signal will simply be high until t_{CDL} after the first Convert Command. (4) t_{CVD} = delay time from Convert Command to Valid Data. Typical value = 120ns. Independent of conversion rate. (5) t_{CH} = Delay time from Convert Command to Internal Hold Command. Typical value = 6ns. Independent of conversion rate. (6) The ⟆ symbol indicates the portion of the waveform that will "stretch out" at lower conversion rates.

FIGURE 14. Data Valid Strobe Timing.

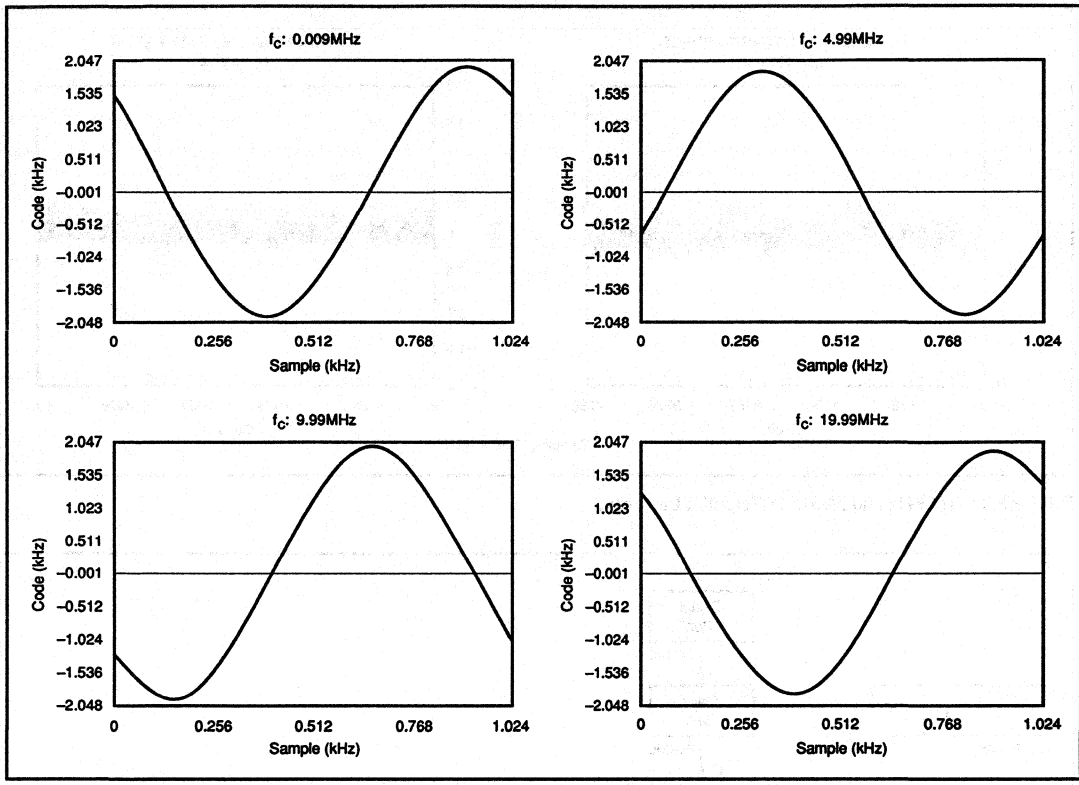


FIGURE 15. Digitized Sine Waves (f_S = 10MHz).

DIGITIZING INPUT WAVEFORMS

The response of the ADC603 is illustrated by the digitized waveforms of Figure 15. The 4.99MHz sine wave near the Nyquist limit is virtually identical to much lower frequency sine wave input. The under-sampled 19.999MHz sine wave illustrates the ADC603's excellent analog input full-power bandwidth.

HISTOGRAM TESTING

Histogram testing is used to test differential nonlinearity of the ADC603. This system's block diagram (the same for FFT testing and waveform digitizing) is shown in Figure 2 and histogram test results for a typical converter are shown in Figure 16. Note that low-frequency differential nonlinearity is 1/2LSB and it shows virtually no degradation near the Nyquist limit of 5MHz; there are no missing codes present and the peak nonlinearity does not exceed 1LSB. Histogram testing is a useful performance indicator as the width of all codes can be determined.

SPECTRUM ANALYZER TESTING

A beat-frequency technique (Figure 17) can be used to view digitized waveforms on an oscilloscope and, with care, this technique can also be used for testing high-speed ADC dynamic characteristics with an analog spectrum analyzer.

In this method a test signal is digitized by the ADC603 and the output digital data is latched into an external latch by the converter Data Valid output pulse driving a divide-by-N counter. The buffered ECL/TTL level translator latch drives a 12-bit video-speed DAC which reconstructs the digital signal back into an analog replica of the ADC603 input. This analog signal, including distortion products and noise resulting from digitization, can then be viewed on an ordinary analog RF spectrum analyzer.

It is important to realize that the distortion and noise measured by this technique include not only that from the ADC603, but also from the entire analog-to-analog test system. Nonlinearity of the reconstruction circuit must be very low to measure a high performance ADC, and this places severe requirements on the ADC, deglitcher, and buffer amplifiers.

Using a high-speed video DAC63 in the analog reconstruction circuit allows excellent test circuit linearity to be achieved. Clocking the DAC (demodulating) at f_C/N allows a longer DAC settling time and keeps linearity high in the digital-to-

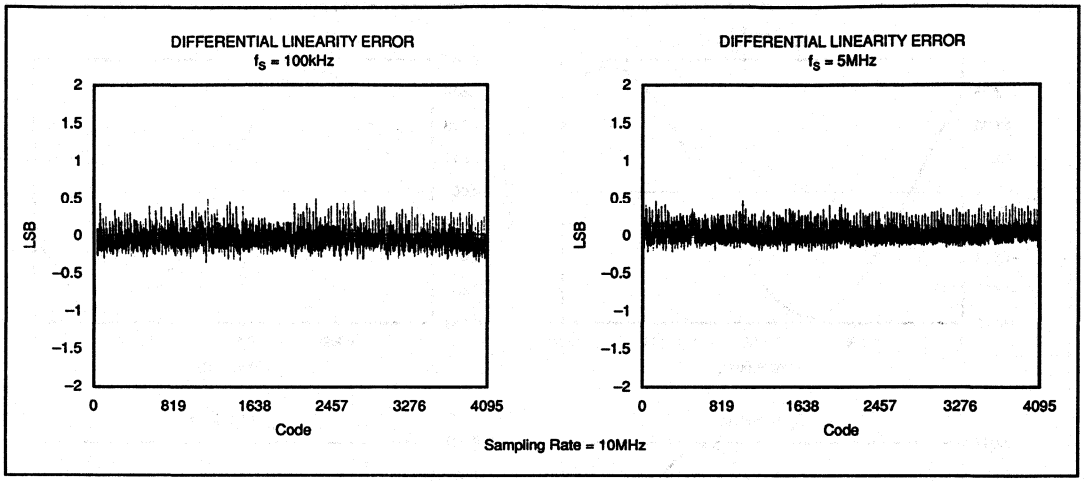


FIGURE 16. 100kHz and 5MHz Differential Linearity.

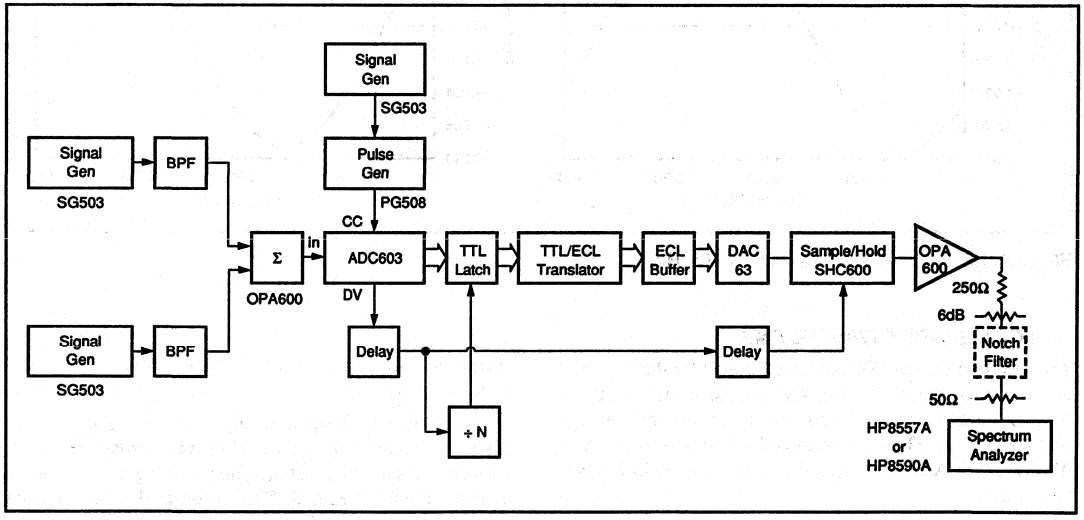


FIGURE 17. Analog-to-Analog Spectral Analysis by Beat-Frequency Techniques.

analog portion of the test circuit. Spectrum analyzer dynamic range can be a limiting factor in this method. To increase dynamic range, a sharp notch filter can be used to attenuate the high-level fundamental frequency. Attenuating the high-level fundamental signal allows the analog spectrum analyzer to be used on a more sensitive range without generating distortion products within its front end.

Note that even though the signal is demodulated at a frequency of sample rate/N, the distortion products still maintain a correct frequency relationship to the fundamental. While this analog technique can give good performance, it cannot exclude some distortion products unavoidably generated within the analog reconstruction portion of the test system. For this reason, the digital FFT technique is capable of more accurate high-speed analog/digital converter dynamic performance measurements and is the preferred method of testing high-performance A/D converters.

TIMING

The ADC603 generates all necessary timing signals internally. There are two methods for reading output data, offering three selectable levels of data pipeline delay as described below.

Convert Command Timing Option (pin 29 = HI)

With this option, the Convert Command signal is used both for initiating a new conversion and for reading valid data

from a previous conversion. This method is most useful in synchronous systems where data samples are taken continuously.

See Figure 13 for timing relationships.

Pin 28 is used to control the amount of pipeline delay. If pin 28 is held LO, then output data "N – 2" will be valid on the rising edge of Convert Command "N." If pin 28 is held HI, then output data "N – 3" will be valid on the rising edge of Convert Command "N." These timing relationships are valid at any conversion rate up to 10MHz. At rates approaching 10MHz, however, the data setup time before the rising Convert Command edge may become as short as 6ns. Therefore, the use of high-speed TTL latches such as the 74F174 hex flip-flop is recommended to capture the data. If slower latches must be used, then the setup time can effectively be improved by adding several nanoseconds of delay between the Convert Command and the latch clock signal.

Data Valid Timing Option (pin 29 = LO)

With this option, data from conversion "N" becomes valid after a fixed delay from the rising edge of Convert Command "N." The delay is approximately 135ns, at which time the Data Valid strobe signal will rise. This signal may be connected directly to the clock input of the user's data latch.

See Figure 18 for timing relationships. Pin 28 must be left HI at all times when using the Data Valid timing option.

The advantages of this method are that no subsequent conversions are required in order to read the data, and the data is available as soon as possible after the start of conversion. Therefore, the Data Valid option is most useful in systems where the ADC may be operated asynchronously, or where the very first data latch output after power-up must represent a valid conversion. Note that because the delay is fixed at approximately 135ns independent of conversion rate, the Data Valid pulse will overlap into the next conversion at rates above 7.4MHz. This does not preclude proper operation at any rate up to 10MHz.

DATA OUTPUT

Output logic inversion can be accomplished by programming pin 27. Binary Two's Complement or Inverted Binary Two's Complement output data formats are available (Table II).

The ADC603 output logic is TTL compatible. The tri-state output is controlled by $\overline{\text{ENABLE}}$ pin 25. For normal operation, pin 25 will be tied LO. A logic HI on pin 25 will switch the ouput data register to a high-impedance state (Figure 20). Output OFF leakage current I_{OZL} and I_{OZH} will be less than 50µA over the converter's specified operating temperature range. Tri-state output should be isolated from noisy digital bus lines, since the noise can couple back through the OFF data register and create noise in the ADC.

PIN NUMBER	DATA LATCHED BY CONVERT COMMAND		DATA LATCHED BY DATA VALID STROBE
	N–3	N–2	N–1
28	HI	LO	HI
29	HI	HI	LO

TABLE I. Pipeline Delay Selection Logic.

DIGITAL INPUTS

Logic inputs are TTL compatible. Open inputs will assume a HI logic state; unused inputs may be allowed to float or they may be tied to an appropriate TTL logic level.

NOTES:

1. *FAST™ Applications Handbook*, 1987. Fairchild Semiconductor Corp.
2. *Fairchild Advanced CMOS Technology*, Technology Seminar Notes, 1985.
3. "Impedance Matching Tweaks Advance CMOS IC Testing", Gerald C. Cox, *Electronic Design*, April, 1987.
4. "Grounding for Electromagnetic Compatibility", Jerry H. Boogar, *Design News*, 23 February, 1987.

OFFSET AND GAIN ADJUSTMENT

The ADC603 is carefully laser-trimmed to achieve its rated accuracy without external adjustments. If desired, both gain error and input offset voltage error may be trimmed to zero with external potentiometers (Figure 23). Trim range is typically 2%; large offsets and gain changes should be made elsewhere in the system. Using an input buffer amplifier allows a convenient point for injecting large offset voltages and making wide gain adjustments.

If offset and gain trim is not used, pins 36 and 37 should be left unconnected.

INPUT VOLTAGE (Exact Center of Code)	DIGITAL DATA OUTPUT LOGIC CODING	
	Binary Two's Complement (BTC) Pin 27 = LO	Inverted Binary Two's Complement (BTC) Pin 27 = HI
	MSB LSB	MSB LSB
+FS (+1.25V)	011111111111*	100000000000*
+FS – 1LSB (+1.2494V)	011111111111	100000000000
+FS – 2LSB (+1.2488V)	011111111110	100000000001
+3/4FS (+0.9375V)	011000000000	100111111111
+1/2FS (+0.625V)	010000000000	101111111111
+1/4FS (+0.3125V)	001000000000	110111111111
+1LSB (+610µV)	000000000001	111111111110
Bipolar Zero (0V)	000000000000	111111111111
–1LSB (–610µV)	111111111111	000000000000
–1/4FS (–0.3125V)	111000000000	000111111111
–1/2FS (+0.625V)	110000000000	001111111111
–3/4FS (–0.9375V)	101000000000	010111111111
–(FS – 1LSB) (–1.2494V)	100000000001	011111111110
–FS (–1.25V)	100000000000	011111111111

* Indicates overrange condition.

TABLE II. Digital Data Output Logic Coding.

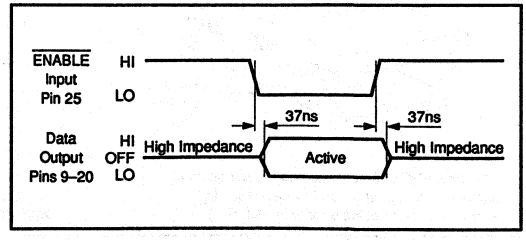


FIGURE 22. Digital Data Tri-State Output.

THERMAL REQUIREMENTS

The ADC603 is tested and specified over a temperature range of 0°C to +70°C (J, K grade) and –55°C to +125°C (R, S grade). The converters are tested in a forced-air environment with a 10 SCFM air flow. With a small heat sink (Figure 24) the ADC603 can be operated in a normal convection ambient-air environment if submodule case temperature does not exceed the upper limit of its specification.(1)

High junction temperature can be avoided by using forced-air cooling, but it is not required at moderate ambient temperatures. Thermal resistance of the ADC603 package is: θ_{JC} = 4.8°C/W, measured to the underside of the case.

NOTES:

1. "Maximizing Heat Transfer from PCBs", *Machine Design*, March 26, 1987, Jeilong Chung.

ENVIRONMENTAL SCREENING

The inherent reliability of a semiconductor device is controlled by the design, materials, and fabrication of the device —it cannot be improved by testing. However, environmental screening can eliminate the majority of those units which would fail early in their lifetimes (infant mortality) through the application of carefully selected accelerated stress levels.

Burr-Brown offers environmentally screened versions of our standard military temperature range products, designed to provide enhanced reliability at moderate cost. The screening illustrated in Table III is performed to selected methods of MIL-STD-883. Reference to these methods provides a convenient way of communicating the screening levels and basic procedures employed; it does not imply conformance to any other military standards or to any methods of MIL-STD-883 other than those specified. Burr-Brown's detailed procedures may vary slightly, model-to-model, from those in MIL-STD-883.

SCREEN	MIL-STD-883 METHOD, CONDITION	SCREENING LEVEL
Internal Visual	2017	Visual requirements only (par 3.1 through 3.1.8)
Electrical Test	Burr-Brown Test Procedure	
High Temperature Storage (Stabilization Bake)	1008	24hr, +125°C
Temperature Cycling	1010	10 cycles, –55°C to –125°C
Constant Acceleration	2001, A	2000G; Y Axis Only
Burn-In	1015, D	160hr, +125°C T_J, No PDA
Hermeticity, Gross Leak	1014, C	Bubble Test Only, Preconditioning Omitted
Final Electrical	Burr-Brown Test Procedure	
External Visual	2009	

TABLE III. Optional Screening Flow.

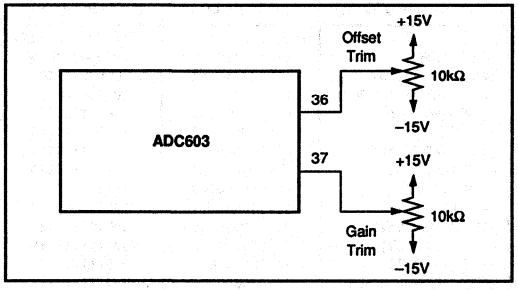


FIGURE 19. Optional Gain and Offset Trim.

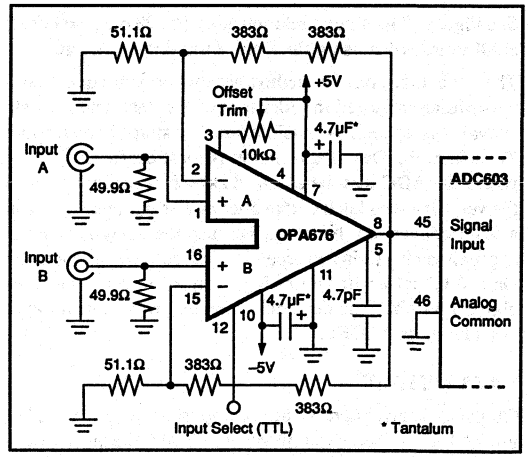


FIGURE 21. A Multiplexed-Input Buffer Amplifier (Gain = +16V/V).

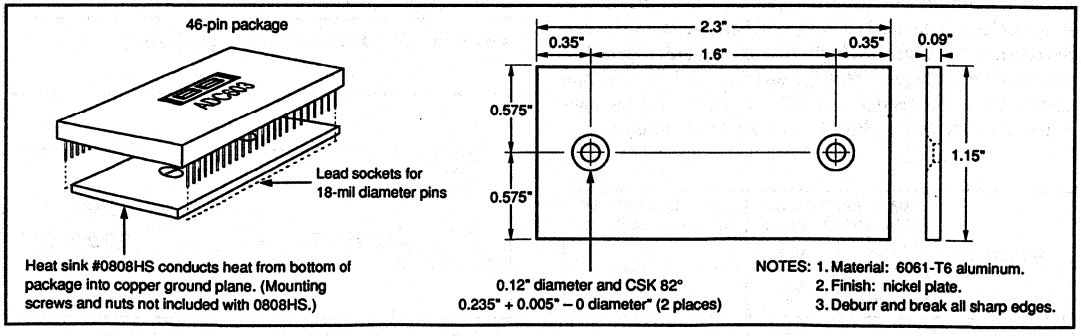


FIGURE 20. Heat Sink Transfers Heat from the DIP Package into a Copper Ground Plane.

BURR-BROWN®

ADC614

14-Bit 5.12MHz Sampling ANALOG-TO-DIGITAL CONVERTER

FEATURES

- HIGH SPURIOUS-FREE DYNAMIC RANGE: –88dB
- WIDEBAND SAMPLE/HOLD: 60MHz
- SAMPLE RATE: DC to 5.12MHz
- HIGH SIGNAL/NOISE RATIO: 75dB
- NO MISSING CODES
- SINGLE 46-PIN DIP PACKAGE
- COMPLETE SUBSYSTEM: Contains Sample/Hold and Reference

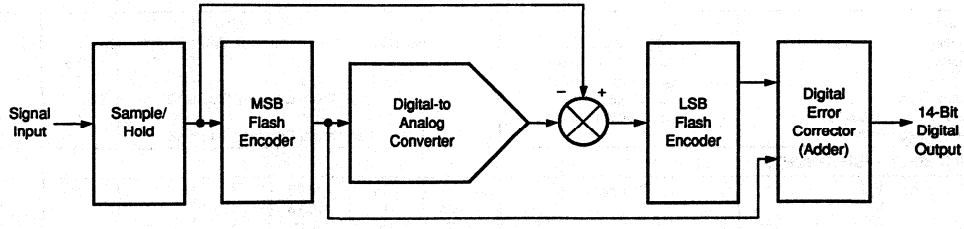
APPLICATIONS

- FFT SPECTRAL ANALYSIS
- MEDICAL IMAGING
- RADAR SIGNAL ANALYSIS
- CCD IMAGING SYSTEMS
- DIGITAL RECEIVERS
- TRANSIENT SIGNAL RECORDING
- HIGH-SPEED DATA ACQUISITION
- SIGINT, ECM, AND EW SYSTEMS

DESCRIPTION

The ADC614 is a high dynamic range analog-to-digital converter capable of digitizing signals at any rate from DC to 5.12 megasamples per second. Outstanding spurious-free dynamic range has been achieved by minimizing potential distortion sources.

The ADC614 is a two-step subranging ADC subsystem containing an ADC, sample/hold amplifier, voltage reference, timing, and error-correction circuitry in a 46-pin hybrid DIP package. The logic interface is TTL. An evaluation board (DEM 1145) is available for quick evaluation.



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SPECIFICATIONS

ELECTRICAL

T_C = +25°C, 5.12MHz sampling rate, output data latched with the convert command, R_S= 50Ω, $\pm V_{CC}$= ±15V, $+V_{DD1}$ = +5V, $-V_{DD2}$ = −5.2V, and 15-minute warmup in convection environment, unless otherwise noted.

PARAMETER	CONDITIONS	ADC614JH MIN	ADC614JH TYP	ADC614JH MAX	ADC614KH MIN	ADC614KH TYP	ADC614KH MAX	UNITS
RESOLUTION				14			14	Bits
INPUTS								
ANALOG								
Input Range	Full Scale	−1.25		+1.25	*		*	V
Input Impedance			1.5			*		MΩ
Input Capacitance			5			*		pF
DIGITAL								
Logic Family				TTL Compatible				
Convert Command	Start Conversion			Positive Edge				
Pulse Width	t = Conversion Period	10		t − 20	*		*	ns
TRANSFER CHARACTERISTICS								
ACCURACY								
Gain Error	f = 100kHz		±0.8	±2		±0.4	±1	%FSR[1]
Input Offset	DC		±0.4	±2		±0.2	±0.75	%FSR
Differential Linearity Error	f = 100kHz: 100% of all Codes		1.3	2.0		0.9	1.25	LSB
No Missing Codes			Guaranteed			Guaranteed		
Power Supply Rejection	$\Delta +V_{CC}$ = ±10%		±0.03	±0.1		*	*	%FSR/%
	$\Delta -V_{CC}$ = ±10%		±0.04	±0.1		*	*	%FSR/%
	$\Delta +V_{DD1}$ = ±10%		±0.004	±0.07		*	*	%FSR/%
	$\Delta -V_{DD2}$ = ±10%		±0.01	±0.07		*	*	%FSR/%
CONVERSION CHARACTERISTICS								
Sample Rate		DC		5.12M	*		*	Samples/s
Pipeline Delay	Logic Selectable		1, 2 or 3 Convert Command Periods					
DYNAMIC CHARACTERISTICS[1,2]								
Differential Linearity Error	f = 2.3MHz: 100% of all Codes		1.3	2.0		0.8	1.25	LSB
Spurious-Free Dynamic Range (SFDR)								
f = 2.3MHz (−0.5dB)	f_S = 5.12MHz	−77	−82		−82	−88		dBFS[3]
f = 100kHz (−0.5dB)		−79	−82		−83	−88		dBFS[3]
Two-Tone Intermodulation Distortion[4]								
f = 2.20MHz (−6.5dB)	f_S = 5.12MHz		−82			−88		dBFS[3]
f = 2.30MHz (−6.5dB)								
Signal-to-Noise Ratio (SNR)								
f = 2.3MHz (−0.5dB)	f_S = 5.12MHz		73			75		dB
f = 100kHz (−0.5dB)			75			77		dB
SINAD								
f = 2.3MHz	f_S = 5.12MHz		72			74		dB
f = 100kHz			74			76		
Aperture Delay Time		−20	−5	+20	*	*	*	ns
Aperture Jitter			9	20		*	*	ps rms
Analog Input Bandwidth (−3dB)								
Small Signal	−20dB Input	40	60		*	*		MHz
Full Power	0dB Input		30		*	*		MHz
Overload Recovery Time	2x Full-Scale Input		205	400		*	*	ns
OUTPUTS								
Logic Family				TTL Compatible				
Logic Coding	Logic Selectable		Two's Complement or Inverted Two's Complement					
Logic Levels	Logic "LO" I_{OL} = −3.2mA	0	+0.3	+0.8	*	*	+0.5	V
	Logic "HI" I_{OH} = 160µA	+2.4	+3.5	+5.0	*	*	*	V
EOC Delay Time	Data Out to DV		See Timing Diagram: Figure 13					
Tri-State Enable/Disable Time	I_{OL} = −6.4mA, 50% In to 50% Out		37	100		*	*	ns
Data Valid Pulse Width			See Timing Diagram: Figure 13					
POWER SUPPLY REQUIREMENTS								
Supply Voltages: $+V_{CC}$	Operating	+14.25	+15	+15.75	*	*	*	V
$-V_{CC}$		−14.25	−15	−15.75	*	*	*	V
$+V_{DD1}$		+4.75	+5	+5.25	*	*	*	V
$-V_{DD2}$		−4.95	−5.2	−5.46	*	*	*	V
Supply Currents: $+I_{CC}$	Operating		+60			*	+80	mA
$-I_{CC}$			−60			*	−80	mA
$+I_{DD1}$[4]			+305			*	+330	mA
$-I_{DD2}$[5]			−550			*	−630	mA
Power Consumption	Operating		6.1	6.5		*	*	W

* Same specifications as ADC614JH.

SPECIFICATIONS (CONT)

ELECTRICAL (FULL TEMPERATURE RANGE SPECIFICATIONS)

$\pm V_{CC}$ = ±15V, $+V_{DD1}$ = +5V, $-V_{DD2}$ = –5.2V, R_S = 50Ω, 5.12MHz sampling rate, output data latched with the convert command, 15-minute warmup, and $T_C = T_{MIN}$ to T_{MAX}, unless otherwise noted.

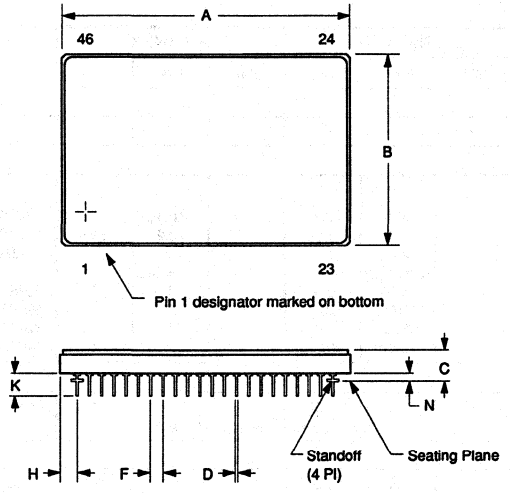
PARAMETER	CONDITIONS	ADC614JH MIN	ADC614JH TYP	ADC614JH MAX	ADC614KH MIN	ADC614KH TYP	ADC614KH MAX	UNITS
TEMPERATURE RANGE								
Specification	T_{CASE}	0		+70	*		*	°C
TRANSFER CHARACTERISTICS								
ACCURACY								
Gain Error	f = 100kHz		±0.9	±2		±0.4	±1.5	%FSR
Input Offset	DC		±0.5	±2		±0.2	±1.5	%FSR
Differential Linearity Error	f = 100kHz: 100% of all Codes		1.4	2.0		1.0	1.5	LSB
No Missing Codes			Guaranteed			Guaranteed		
Power Supply Rejection	$\Delta +V_{CC}$ = ±10%		±0.04	±0.2		*	*	%FSR/%
	$\Delta -V_{CC}$ = ±10%		±0.05	±0.2		*	*	%FSR/%
	$\Delta +V_{DD1}$ = ±10%		±0.004	±0.1		*	*	%FSR/%
	$\Delta -V_{DD2}$ = ±10%		±0.02	±0.1		*	*	%FSR/%
CONVERSION CHARACTERISTICS								
Sample Rate		DC		5.12M	*		*	Samples/s
Pipeline Delay			1, 2 or 3 Convert Command Periods					
DYNAMIC CHARACTERISTICS[2]								
Differential Linearity Error	f = 2.3MHz: 100% of all Codes		1.4	2.0		1.0	1.5	LSB
Spurious-Free Dynamic Range (SFDR)								
f = 2.3MHz (–0.5dB)	f_S = 5.12MHz	–75	–82		–80	–87		dBFS[3]
f = 100kHz (–0.5dB)		–77	–82		–80	–87		dBFS[3]
Two-Tone Intermodulation Distortion								
f = 2.20MHz (–6.5dB)	f_S = 5.12MHz		–82			–87		dBFS[3]
f = 2.30MHz (–6.5dB)								
Signal-to-Noise Ratio (SNR)								
f = 2.3MHz (–0.5dB)	f_S = 5.12MHz		71			74		dB
f = 100kHz (–0.5dB)			74			76		dB
SINAD								
f = 2.3MHz	f_S = 5.12MHz		70			73		dB
f = 100kHz			73			75		
Aperture Delay Time		–25	–6	+25	*	*	*	ns
Aperture Jitter			10			*	20	ps rms
Analog Input Bandwidth (–3dB)								
Small Signal	–20dB Input		60			*		MHz
Full Power	0dB Input		30			*		MHz
Overload Recovery Time	2x Full-Scale Input		220			*		ns
OUTPUTS								
Logic Levels	Logic "LO", I_{OL} = –3.2mA	0	+0.3	+0.8	*	*	*	V
	Logic "HI", I_{OH} = 160µA	+2.4	+3.5	+5.0	*	*	*	V
EOC Delay Time	Data Out to DV	See Figure 13; Δ Timing Typically Within ±20% Over Temperature						
Tri-State Enable/Disable Time	I_{OL} = –6.4mA, 50% In to 50% Out		42	100		*	*	ns
Data Valid Pulse Width		See Figure 13; Δ Timing Typically Within ±20% Over Temperature						
POWER SUPPLY REQUIREMENTS								
Supply Currents: $+I_{CC}$	Operating		+65	+80		*	*	mA
$-I_{CC}$			–61	–80		*	*	mA
$+I_{DD1}$[4]			+305	+333		*	*	mA
$-I_{DD2}$[5]			–550	–630		*	*	mA
Power Consumption	Operating		6.1	6.5		*	*	W

* Same specifications as ADC614JH.

NOTES: (1) FSR: Full-Scale Range = 2.5Vp-p. (2) Units with lower distortion are available on special order; inquire. (3) dBFS = level referred to full scale. The input signal is within 1dB of full scale; f = input frequency; f_S = sampling frequency. (4) Pins 3 and 30 (analog typically draw 80% of the total +5V current. Pin 21 (digital) typically draws 20%. (5) Pin 6 (analog) typically draws 45% of the total –5.2V current. Pin 31 (digital) typically draws 55%.

MECHANICAL

Package — Metal and Ceramic



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	2.370	2.420	60.20	61.47
B	1.560	1.610	39.62	40.89
C	.200	.260	5.08	6.60
D	.018 DIA. BASIC		0.46 DIA. BASIC	
F	.100 BASIC		2.54 BASIC	
H	.075	.115	1.91	2.92
K	.150	.190	3.81	4.83
L	1.300 BASIC		33.02 BASIC	
M	—	10°	—	10°
N	.040	.060	1.02	1.52

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin material and plating composition conform to method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2)

PIN ASSIGNMENTS

1	Common (Case)	46	Common (Analog)
2	DNC	45	Analog Signal In
3	$+V_{DD1}$ (+5V) Analog	44	$+V_{CC}$ (+15V) Analog
4	S/H Out	43	$-V_{CC}$ (−15V) Analog
5	A/D in	42	NC
6	$-V_{DD2}$ (−5.2V) Analog	41	NC
7	Bit 13	40	NC
8	Bit 14 (LSB)	39	DNC
9	Bit 1 (MSB)	38	DNC
10	Bit 2	37	Gain Adjust
11	Bit 3	36	Offset Adjust
12	Bit 4	35	Common (Analog)
13	Bit 5	34	$+V_{CC}$ (+15V) Analog
14	Bit 6	33	$-V_{CC}$ (−15V) Analog
15	Bit 7	32	Common (Analog)
16	Bit 8	31	$-V_{DD2}$ (−5.2V) Digital
17	Bit 9	30	$+V_{DD1}$ (+5V) Analog
18	Bit 10	29	1 Pipeline Delay Select
19	Bit 11	28	0 Pipeline Delay Select
20	Bit 12	27	Output Logic Invert
21	$+V_{DD1}$ (+5V) Digital	26	Common (Digital)
22	Data Valid Output	25	3-State $\overline{\text{ENABLE}}$
23	Common (Digital)	24	Convert Command In

NOTE: NC = no connection, DNC = do not connect.

ORDERING INFORMATION

ADC614 ( ) H

- Basic Model Number
- Performance Grade Code
  - J, K: 0°C to +70°C Case Temperature
- Package Code
  - H: Metal and Ceramic

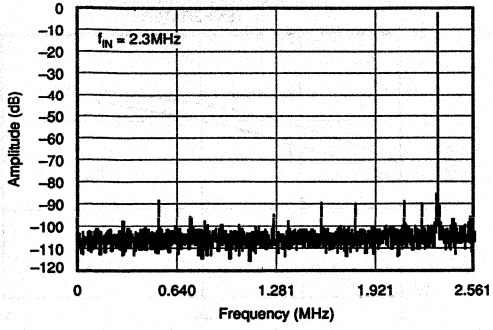
ABSOLUTE MAXIMUM RATINGS

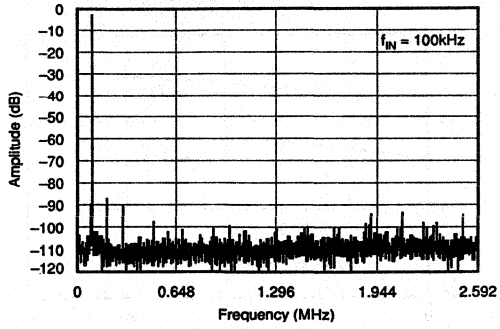
$\pm V_{CC}$	±16.5V
$+V_{DD1}$	+7.0V
$\pm V_{DD2}$	−7.0V
Analog Input	±5.0V
Logic Input	−0.5V to $+V_{DD1}$
Case Temperature (Operating)	+85°C
Junction Temperature	+100°C
Storage Temperature	−65°C to +125°C

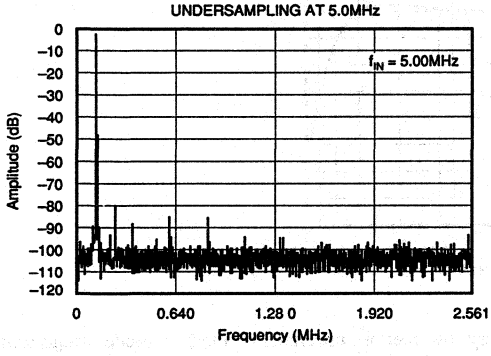
Stresses above these ratings may permanently damage the device.

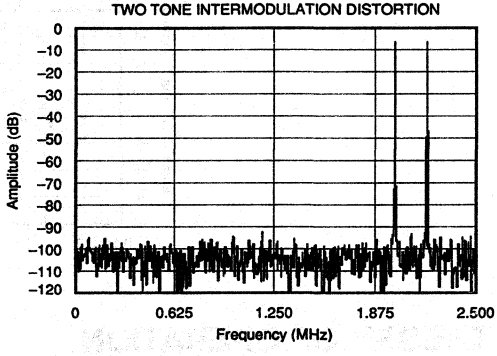
TYPICAL PERFORMANCE CURVES

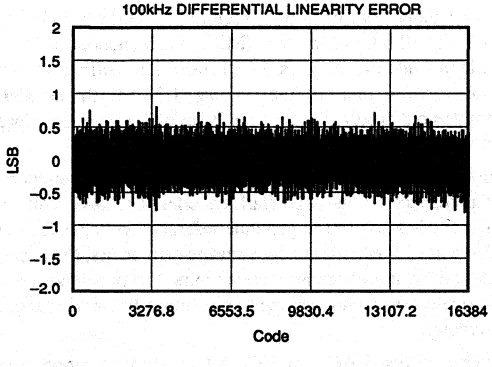
$\pm V_{CC}$ = ±15V, $+V_{DD1}$ = +5V, $-V_{DD2}$ = –5.2V, R_S = 50Ω, 5.12MHz sampling rate, 15-minute warmup, and T_C = +25°C, unless otherwise noted.

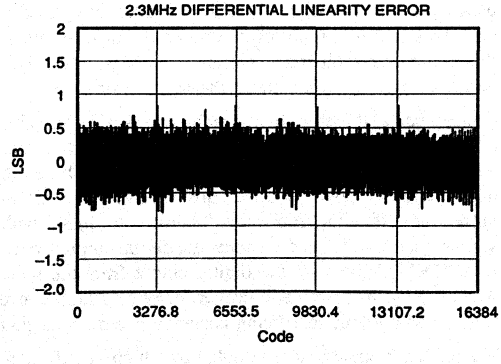








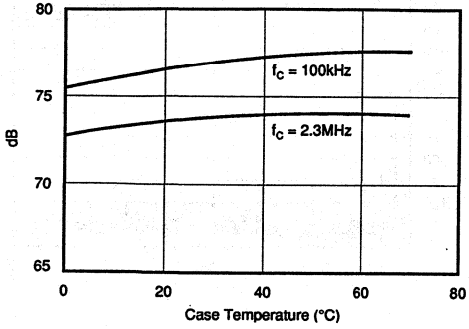




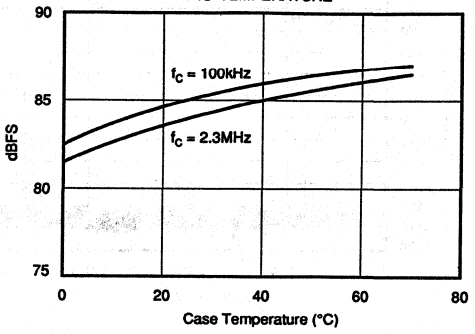
TYPICAL PERFORMANCE CURVES (CONT)

$\pm V_{CC}$ = ±15V, $+V_{DD1}$ = +5V, $-V_{DD2}$ = –5.2V, R_S = 50Ω, 5.12MHz sampling rate, 15-minute warmup, and T_C = +25°C, unless otherwise noted.

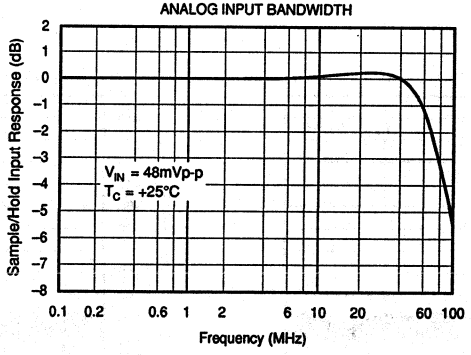
SIGNAL-TO-NOISE RATIO vs TEMPERATURE



SPURIOUS FREE DYNAMIC RANGE vs TEMPERATURE



ANALOG INPUT BANDWIDTH



THEORY OF OPERATION

The ADC614 is a two-step subranging analog-to-digital converter. This architecture is shown in Figure 1. The major system building blocks are: sample/hold amplifier, MSB flash encoder, DAC and error amplifier, LSB flash encoder, digital error corrector, and timing circuits. The ADC614 uses hybrid technology with laser-trimmed integrated circuits mounted in a multilayer ceramic package to integrate this complex circuit into a complete analog-to-digital converter subsystem with state-of-the-art performance.

Conceptually, the subranging technique is simple: sample and hold the input signal, convert to digital with a coarse ADC, convert back to analog with a coarse-resolution (but high-accuracy) DAC, subtract this voltage from the S/H output, amplify this "remainder," convert to digital with a second coarse ADC, and combine the digital output from the first ADC (MSB) with the digital output from the second ADC (LSB). In practice, however, achieving high conversion speed without sacrificing accuracy is a difficult task.

The analog input signal is sampled by a high-speed sample/hold amplifier with low distortion, fast acquisition time and very low aperture uncertainty (jitter). A diode bridge sampling switch is used to achieve an acceptable compromise between speed and accuracy. The diode bridge switching transients are buffered from the analog input by a high input impedance buffer amplifier. Since the hold capacitor does not appear in the feedback of the diode bridge output buffer, the capacitor can acquire the signal in 65ns. The low-bias-current output buffer is then required to settle to only the resolution (8 bits) of the first (MSB) flash encoder in 65ns, while an additional 85ns is allowed for settling to the resolution (14 bits) of the second (LSB) flash encoder. Sample/hold droop appears as only an offset error and does not effect linearity.

Both the MSB and the LSB flash encoder (ADC) functions are performed by one 8-bit flash encoder. The DAC voltage reference is also used to generate reference voltages for the MSB and LSB encoder to compensate drift errors. Buffering and scaling amplifiers are laser-trimmed to minimize voltage offset errors and optimize gain (input full-scale range) symmetry.

The subtraction DAC is an ECL 8-bit resolution monolithic DAC with 14-bit accuracy. Laser-trimmed thin-film nichrome

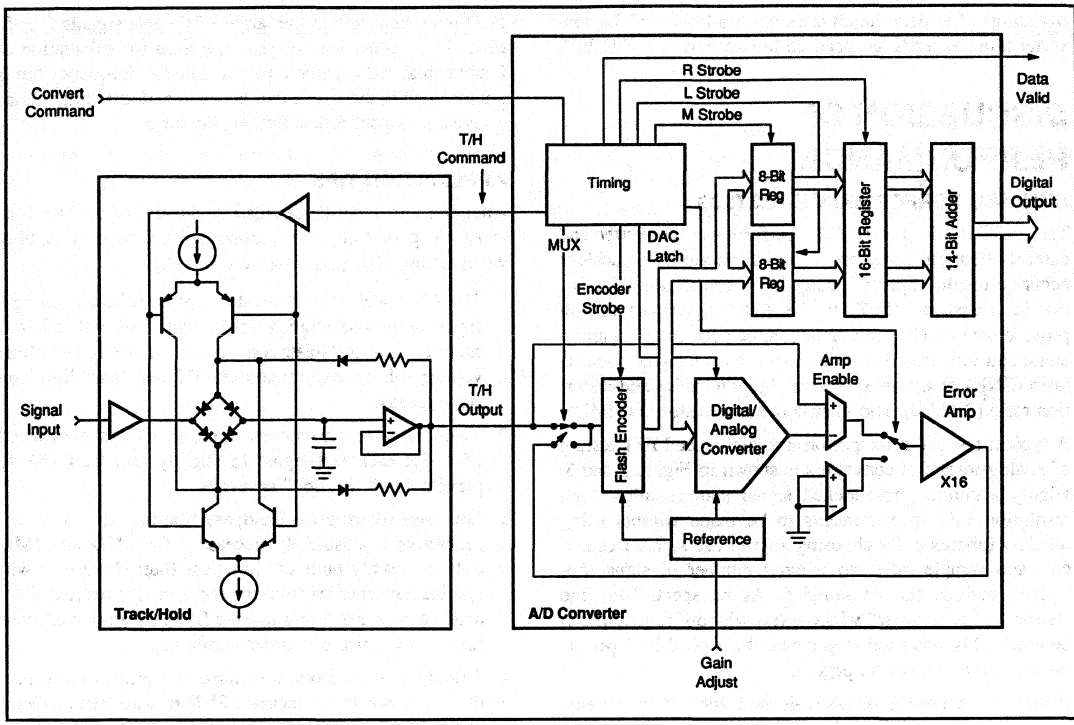


FIGURE 1. ADC614 Block Diagram—A Two-Step Subranging Architecture.

resistors and high-speed bipolar circuitry allow the DAC output to settle to 14-bit accuracy in only 35ns.

A "remainder" or coarse conversion-error voltage is generated by resistively subtracting the DAC output from the output of the sample/hold amplifier. Before the second (LSB) conversion, the "remainder" is amplified by a wideband fast-settling two-input amplifier with a gain of 32V/V. To prevent overload on large amplitude transients, the active input is switched off to blank the amplifier input from the beginning of the S/H acquisition time to the end of the MSB encoder update time.

Internal timing circuits (ECL logic is used internally) supply all the critical timing signals necessary for proper operation of the ADC614. Some noncritical timing signals are also generated in the digital error correction circuitry. Timing signals are laser-trimmed for both pulse width and delay. ECL logic is used for its speed, low noise characteristics and timing delay stability over a wide range of temperatures and power supply voltages. Basic timing is derived from the output of a three-stage shift register driven by a synchronized 20MHz oscillator.

The convert command pulse is differentiated to allow triggering by pulses from as narrow as 10ns to as wide as 80% duty cycle.

The ADC614 timing technique generates a variable width S/H gate pulse which is determined by the conversion command pulse period minus a fixed 135ns ADC conversion time. ADC614 conversion rates are therefore possible somewhat above the 5.12MHz specification but S/H acquisition time is sacrificed and accuracy is rapidly degraded.

The output of the MSB and LSB encoders are read into separate 8-bit latches. The latched MSB data, along with the latched LSB data, is then read into a 16-bit latch after the leading edge of the LSB strobe and before being applied to the adder, where the actual error correction takes place. These latches eliminate any critical timing problems that could result when the converter is operated at the maximum conversion rate.

The function of the digital error correction circuitry is to assemble the 8-bit words from the two flash encoders into a 14-bit output word.

The 16-bit register output is then sent to a 14-bit adder where the final data output word is created. The MSB data forms the most significant eight bits of a 14-bit word, with the last six bits being assigned zeros. In a similar fashion, the LSB data from the least significant bits forms the other input to the adder, with the first six bits being assigned zeros. As two 14-bit words are being added, the output of the adder could exceed 14 bits in range; however, the final data output is only a 14-bit word, so a means of detecting an overrange is included to prevent reading erroneous data. The converter data output is forced to all ones for a full-scale input or

overrange. The data output does not "roll-over" if the converter input exceeds its specified full-scale range of ±1.25V.

DISCUSSION OF PERFORMANCE

DYNAMIC PERFORMANCE TESTING

The ADC614 is a very high performance converter and careful attention to test techniques is necessary to achieve accurate results. Spectral analysis by application of a fast Fourier transform (FFT) to the ADC digital output will provide data on all important dynamic performance parameters: spurious free dynamic range (SFDR), signal-to-noise ratio (SNR) or the more severe signal-to-noise-and-distortion ratio (SINAD), and intermodulation distortion (IMD).

A typical test setup for performing high-speed FFT testing of analog-to-digital converters is shown in Figure 2 and 3. Highly accurate phase-locked signal sources allow high resolution FFT measurements to be made without using window functions. By choosing appropriate signal frequencies and sample rates, an integral number of signal frequency periods can be sampled. As no spectral leakage results, a "rectangular" window (no window function) can be used. This was used to generate the typical FFT performance curves shown on page 5.

If generators cannot be phase-locked and set to extreme accuracy, a very low side-lobe window must be applied to the digital data before executing an FFT. A commonly used window such as the Hanning window is not appropriate for testing high performance converters; a minimum four-sample Blackman-Harris window is strongly recommended.[1] To assure that the majority of codes are exercised in the ADC614 (14 bits), a 4096-point FFT is taken. If the data storage RAM is limited, a smaller FFT may be taken if a sufficient number of samples are averaged (i.e., a 10-sample average of 512-point FFTs).

DYNAMIC PERFORMANCE DEFINITIONS

1. Spurious Free Dynamic Range:

$$\frac{\text{Largest Harmonic Power (first 9 harmonics)}}{\text{Full Scale Power}}$$

2. Intermodulation Distortion (IMD):

$$\frac{\text{Highest IMD Product Power (to 5th order)}}{\text{Sinewave Signal Power}}$$

3. Signal-to-Noise Ratio (SNR):

$$\frac{\text{Sinewave Signal Power}}{\text{Noise Power}}$$

4. Signal-to-(Noise + Distortion)[2] Ratio (SINAD):

$$\frac{\text{Sinewave Signal Power}}{\text{Noise + Harmonic Power (first 9 harmonics)}}$$

IMD is referenced[3] to the larger of the test signals f_1 or f_2. Five "bins" either side of peak are used for calculation of fundamental and harmonic power. The DC frequency bin is not included in these calculations as it is of little importance in dynamic signal processing applications.

APPLICATION TIPS

Attention to test set-up details can prevent errors that contribute to poor test results. Important points to remember when testing high performance converters are:

1. The ADC analog input must not be overdriven. Using a signal amplitude slightly lower than FSR will allow a small amount of "headroom" so that noise or DC offset voltage will not overrange the ADC and "hard limit" on signal peaks.
2. Two-tone tests can produce signal envelopes that exceed FSR. Set each test signal to slightly less than –6B to prevent "hard limiting" on peaks.
3. Low-pass filtering (or bandpass filtering) of test signal generators is absolutely necessary for THD and IMD tests. An easily built LC low-pass filter (Figure 4) will eliminate harmonics from the test signal generator. Care must be taken not to saturate the filter. Saturation of these filters may cause odd order harmonics.
4. Test signal generators must have exceptional noise performance to achieve accurate SNR measurements. Good generators together with fifth-order elliptical bandpass filters are recommended for SNR tests. Recommended generators are the Fluke 6080A or HP8644A. Narrow-bandwidth crystal filters can also be used to filter generator broadband noise, but they should be carefully tested for operation at high levels.
5. The analog input of the ADC614 should be terminated directly at the input pin sockets with the correct filter terminating impedance (50Ω or 75Ω), or it should be driven by a low output impedance buffer such as an OPA600, OPA675/676, or the OPA620/621. However, these amplifiers are likely to limit the harmonic performance of the ADC624. Short leads are necessary to prevent digital noise pickup.
6. A low-noise (jitter) clock signal (convert command) generator is required for good ADC dynamic performance. A poor generator can seriously impair good SNR performance. A HP 8644A generator is a good clock source. Short leads are necessary to preserve fast TTL rise times.
7. Two-tone testing will require isolation between test signal generators to prevent IMD generation in the test generator output circuits. A passive (hybrid transformer) signal combiner can also be used (Figure 5) over a range of about 0.1MHz to 30MHz. This combiner's port-to-port isolation will be ≈45dB between signal generators and its input-output insertion loss will be ≈6dB. Distortion will be better than –85dBC for the powdered-iron core specified. Avoid ferrites.

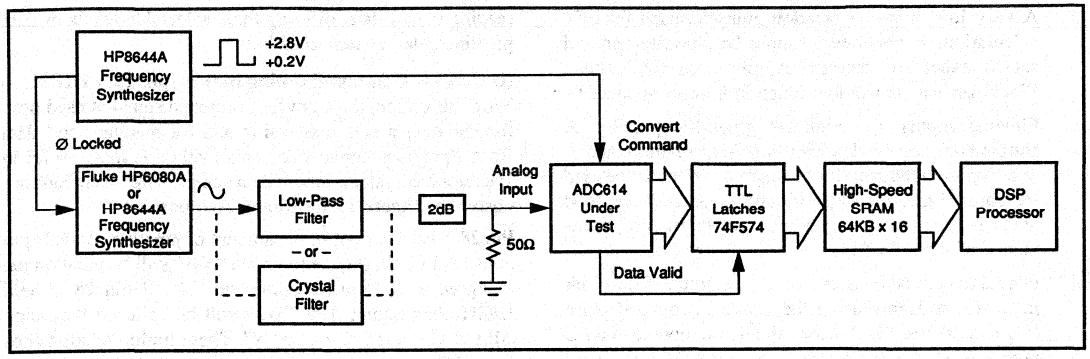


FIGURE 2. Block Diagram of FFT Test for SNR, SFDR and Swept-Power Test.

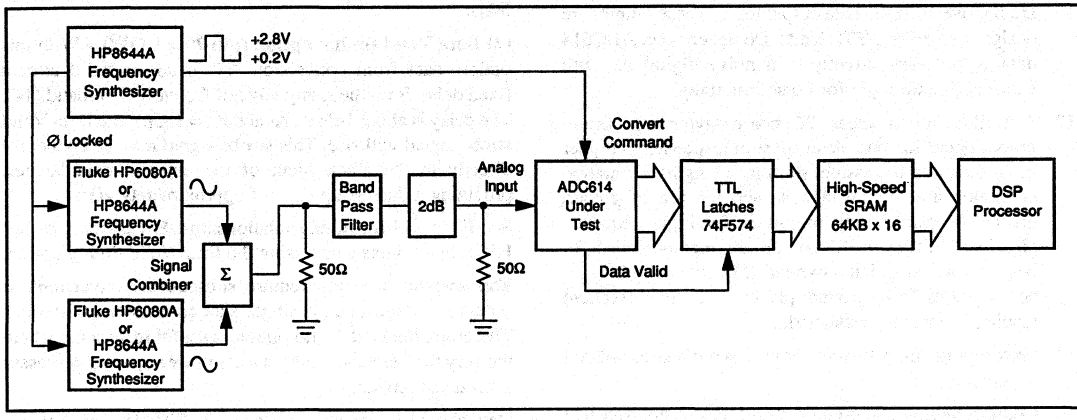
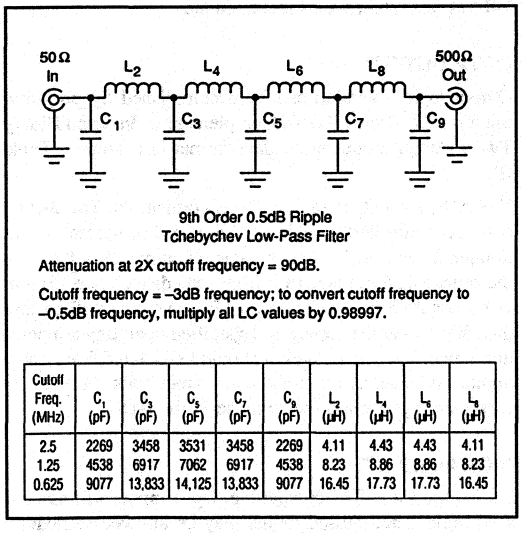


FIGURE 3. Block Diagram of FFT Test for Two-Tone IMD.



Cutoff Freq. (MHz)	C_1 (pF)	C_3 (pF)	C_5 (pF)	C_7 (pF)	C_9 (pF)	L_2 (µH)	L_4 (µH)	L_6 (µH)	L_8 (µH)
2.5	2269	3458	3531	3458	2269	4.11	4.43	4.43	4.11
1.25	4538	6917	7062	6917	4538	8.23	8.86	8.86	8.23
0.625	9077	13,833	14,125	13,833	9077	16.45	17.73	17.73	16.45

FIGURE 4. Ninth-Order Harmonic Filter.

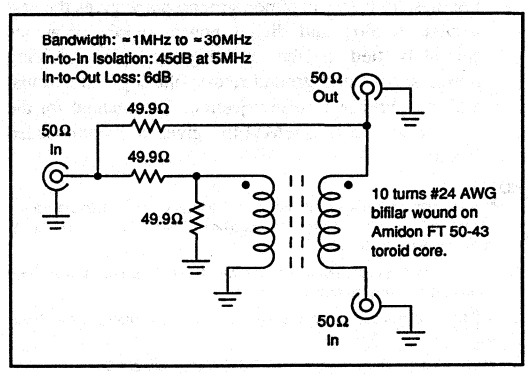


FIGURE 5. Passive Signal Combiner.

8. A very low side-lobe window must be used for FFT calculations if generators cannot be phase-locked and set to exact frequencies. A minimum four-sample Blackman-Harris window function is recommended.[1]
9. Floating inputs can eliminate ground-loop noise. A simple common-mode choke shown in Figure 6 and 7, or a single-ended amplifier (Figure 8 and 9) can be used for gain. While the OPA600 and OPA620 have good noise performance, they may limit harmonic performance of the ADC614.
10. Digital data must be latched into an external TTL 14-bit register, preferably using the convert command pulse (Figures 10 and 11). Latches should be mounted on PC boards in very close proximity to the ADC614. Avoid long leads.
11. Do not overload the data output logic. These outputs are designed to drive 2 TTL loads. Do not connect ADC614 data output pins directly to a noisy digital bus; use external 3-state logic for noise immunity.
12. A well-designed, clean PC board layout will assure proper operation and clean spectral response.[4, 5] Proper grounding and bypassing, short lead lengths, separation of analog and digital signals, and the use of ground planes are particularly important for high frequency circuits. Multilayer PC boards are recommended for best performance, but a two-sided PC board with large, heavy (20oz-foil) ground planes can give excellent results, if carefully designed.
13. Prototyping "plug-boards" or wire-wrap boards will not be satisfactory.
14. Connect analog and digital ground pins of the ADC614 directly to the ground plane. In our experience, connecting these pins to a common ground plane gives the best results. Analog and digital power supply commons should be tied together at the ground plane. Adding power supply and ground-return filtering[6] is optional and may improve noise rejection. The manual for the evaluation board (DEM1145) gives a recommended layout.

NOTES:

1. "On the Use of Windows for Harmonic Analysis with the Discrete Fourier Transform", Fredric J. Harris. *Proceedings of the IEEE*, Vol. 66, No. 1, January 1978, pp 51-83.
2. SINAD test includes harmonics whereas SNR does not include these important spurious products.
3. If IMD is referenced to peak envelope power, distortion will be of 6dB better.
4. *MECL System Design Handbook*, 3rd Edition, Motorola Corp.
5. Motorola MECL, Motorola Corp.
6. Murata-Erie BNX002-01.

TIMING

The ADC614 generates all necessary timing signals internally. Only timing between Convert Command, Output Data, and Data Valid must be considered. Proper timing is shown in Figures 12 and 13. There are two methods for reading output data, offering three selectable levels of data pipeline delay as described below:

(1) Convert Command timing option (pin 29 = HIGH)—With this option, the Convert Command signal is used both for initiating a new conversion and for reading valid data from a previous conversion. This method is most useful in synchronous systems where data samples are taken continuously. See Figure 12 for timing relationships.

Pin 28 is used to control the amount of pipeling delay. If pin 28 is held LOW, then output data "N-1" will be valid on the rising edge of Convert Command "N". If pin 28 is held HIGH, then output data "N-2" will be valid on the rising edge of Convert Command "N". These timing relationships are valid at any conversion rate up to 5.12MHz, the data setup time before the rising Convert Command edge is about 50ns.

(2) Data Valid timing option (pin 29 = LOW)—With this option, data from conversion "N" becomes valid after a fixed delay from the rising edge of Convert Command "N". The delay is about 165ns . At about t = 185ns, the Data Valid strobe signal will rise. This strobe signal may be connected directly to the clock input of the external data latches, providing a data setup time of approximately 20ns.

See Figure 13 for timing relationships. Pin 28 must be left HIGH at all times when using the Data Valid timing option.

This method does not require subsequent conversions in order to read the data (ie, single-shot conversion capability). Therefore, the Data Valid option is useful in systems where the very first data latch output after power-up must represent a valid conversion.

Data should be latched into external TTL latches that can operate reliably with a set-up time of 6ns minimum. Two 74F574 hex latches are recommended.

DATA OUTPUT

Output logic inversion can be accomplished by programming pin 27. Binary Two's Complement or Inverted Binary Two's Complement output data format is available (Table II).

The ADC614 output logic is TTL compatible. The 3-state output is controlled by ENABLE pin 25. For normal operation pin 25 will be tied LO. A logic HI on pin 25 will switch the output data register to a high-impedance state (Figure 14). Output OFF leakage current I_{OZL} and I_{OZH} will be less than 50µA over the converter's specified operating temperature range. The 3-state output should be isolated from noisy digital bus lines as the noise can couple back through the OFF data register and create noise in the ADC.

DIGITAL INPUTS

Logic inputs are TTL compatible. Open inputs will assume a HI logic state; unused inputs may be allowed to float or they may be tied to an appropriate TTL logic level.

OFFSET AND GAIN ADJUSTMENT

The ADC614 is carefully laser-trimmed to achieve its rated accuracy without external adjustments. If desired, both gain error and input offset voltage error may be trimmed with external potentiometers (Figure 15). Trim range is typically only 0.1%; large offsets and gain changes should be made elsewhere in the system. Using an input buffer amplifier is the preferred way for injecting offset voltages and making wide gain adjustments.

	DATA LATCHED BY CONVERT COMMAND		DATA LATCHED BY DATA VALID STROBE
PIN NUMBER	N-2	N-1	N-1
28	HI	LO	HI
29	HI	HI	LO

TABLE I. Pipeline Delay Selection Logic.

	DIGITAL DATA OUTPUT LOGIC CODING	
INPUT VOLTAGE	BINARY TWO'S COMPLEMENT (BTC) PIN 27 = LO	INVERTED BINARY TWO'S COMPLEMENT ($\overline{BTC}$) PIN 27 = HI
+FS (+1.25V)	01111111111111	10000000000000
+FS – 1LSB	01111111111110	10000000000001
+3/4 FS	00011111111111	11100000000000
+1/2 FS	00111111111111	11000000000000
+1 LSB	00000000000000	11111111111111
Bipolar Zero	11111111111111	00000000000000
–1 LSB	11111111111110	00000000000001
–1/2 FS	10111111111111	01000000000000
–3/4 FS	10011111111111	01100000000000
–FS – 1LSB	10000000000001	01111111111110
–FS (–1.25V)	10000000000000	01111111111111
	MSB LSB	MSB LSB

TABLE II. Digital Data Output Logic Coding.

THERMAL REQUIREMENTS

The ADC614 is tested and specified over a temperature range of 0°C to +70°C. The converters are tested in a forced-air environment with a 10 SCFM air flow. With a small heat sink (Figure 16) the ADC614 can be operated in a normal convection ambient air environment if submodule case temperature does not exceed the upper limit of its specification.

High junction temperature can be avoided by using forced-air cooling, but it is not required at moderate ambient temperatures. Thermal resistance of the ADC614 package is: θ_{JC} = 4.8°C/W. measured to the underside of the case.

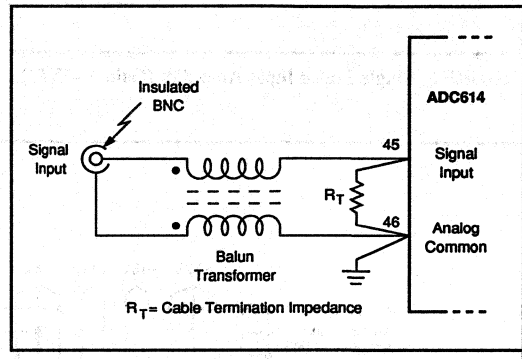


FIGURE 6. Floating-Input Balun Transformer.

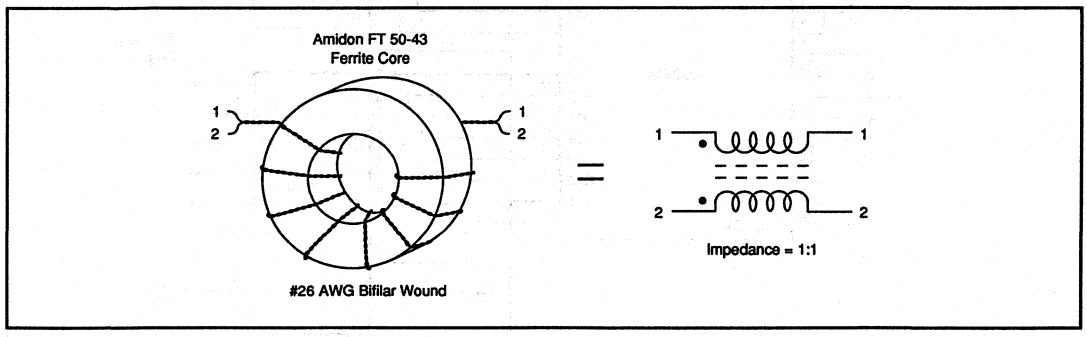


FIGURE 7. Common-Mode Choke Transformer Windings.

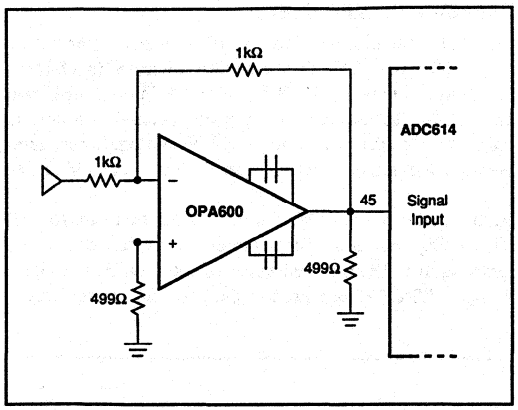


FIGURE 8. Single Ended Input Amplifier (Gain = –1V/V).

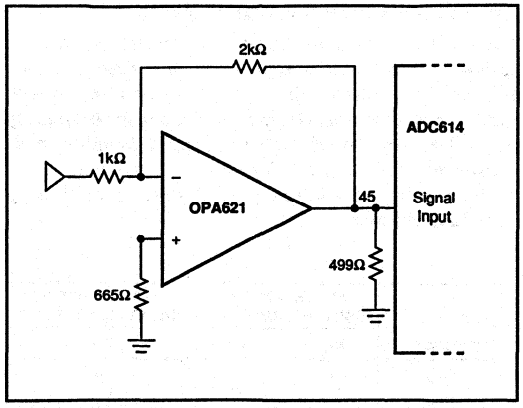


FIGURE 9. Single Ended Input Low Noise Amplifier (Gain = –2V/V).

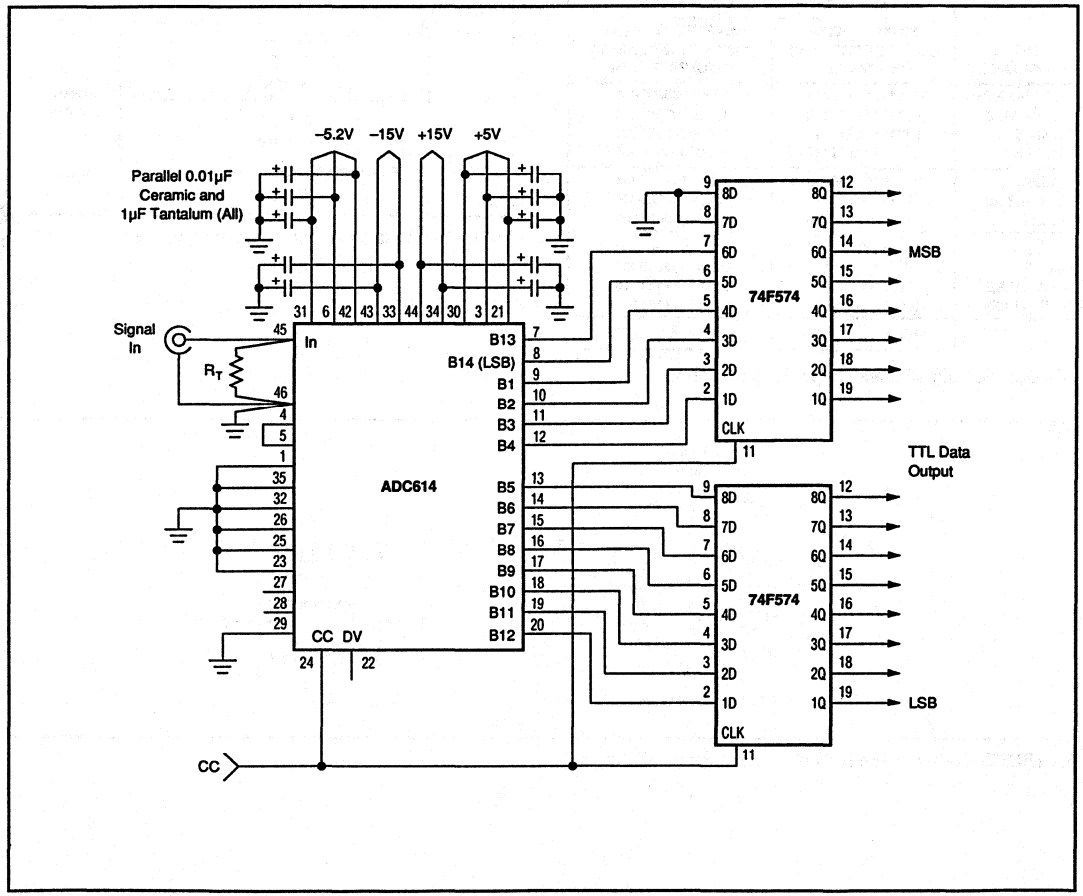


FIGURE 10. Interface Circuit—Digital Output Strobed by Convert Command. Supply connection shown: power supplies and grounds shared by analog and digital pins using common ground plane. Optimum noise performance is achieved when strobing the output data with the convert command.

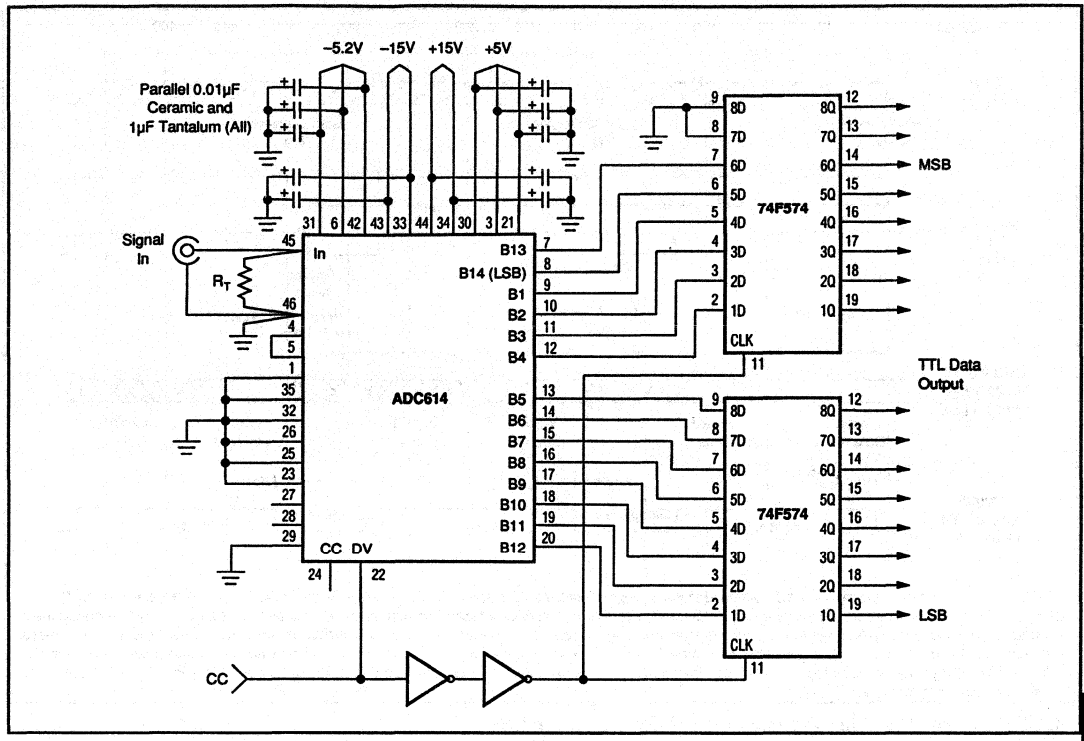
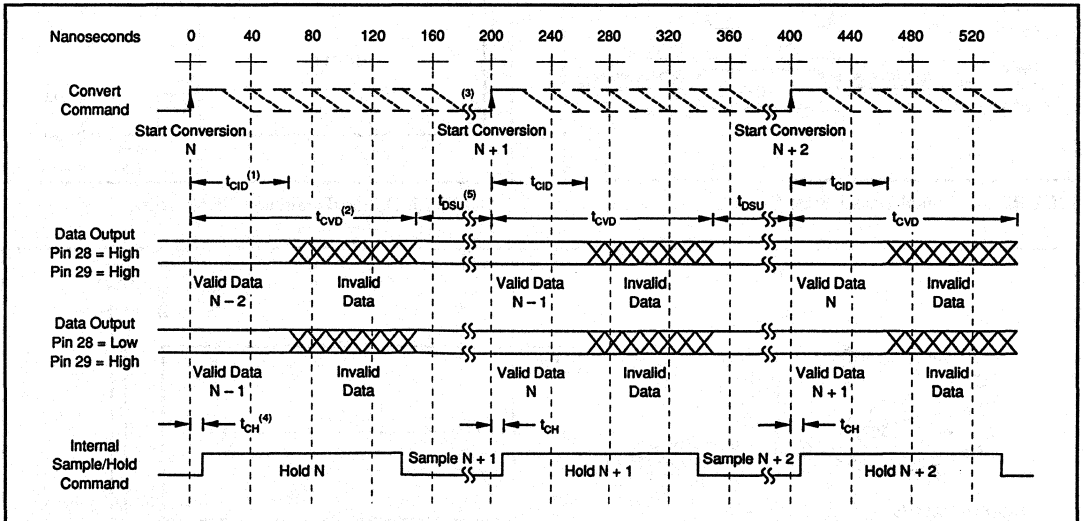
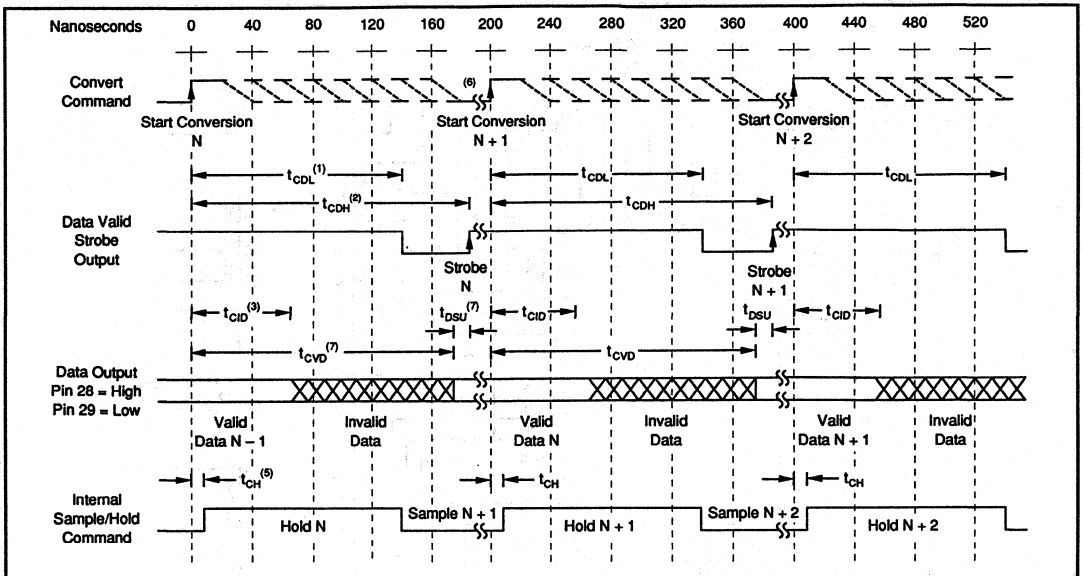


FIGURE 11. Interface Circuit—Digital Output Strobed by Data Valid Pulse. Supply connection shown: power supplies and grounds shared by analog and digital pins, using common ground plane.



NOTES: (1) t_{CID} = delay time from Convert Command to Invalid Data. Typical value = 65ns. Independent of conversion rate. (2) t_{CVD} = Delay time from Convert Command to Valid Data. Typical Value = 150ns. Independent of conversion rate. (3) The ⟆ symbol indicates the portion of the waveform that will "stretch out" at lower conversion rates. (4) t_{CH} = delay time from Convert Command to the internal hold command. Typical value = 6ns. Independent of conversion rate. (5) t_{DSU} = data set-up time. This depends on conversion rate and may be calculated by: $t_{DSU} = \frac{1}{f_{SAMPLE}} - t_{CVD}$

FIGURE 12. Convert Command Strobe Timing for a 5MHz Conversion Rate.



NOTES: (1) t_{CDL} = delay time from Convert Command to the falling edge of Data Valid strobe. Typical value = 140ns. Independent of conversion rate. (2) t_{CDH} = delay time from Convert Command to the rising edge of Data Valid strobe. Typical value = 195ns. Independent of conversion rate. (3) t_{CID} = delay time from Convert Command to Invalid Data. Typical value = 65ns. Independent of conversion rate. (4) t_{CVD} = delay time from Convert Command to Valid Data. Typical Value = 188ns. Independent of conversion rate. (5) t_{CH} = delay time from Convert Command to the internal hold command. Typical value = 6ns. Independent of conversion rate. (6) The ⌇⌇ symbol indicates the portion of the waveform that will "stretch out" at lower conversion rates. (7) t_{DSU} = data setup time. Typical value = 7ns. Independent of conversion rate.

FIGURE 13. Data Valid Strobe Timing for a 5MHz Conversion Rate.

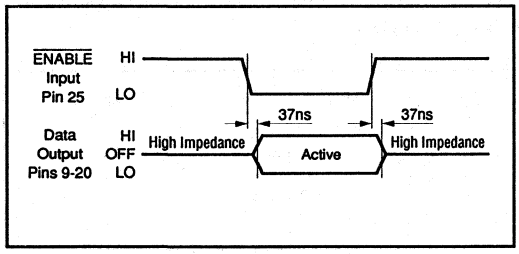


FIGURE 14. Digital Data 3-State Output.

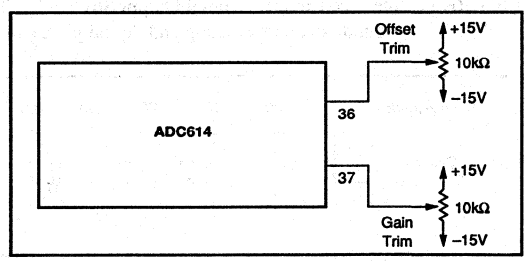


FIGURE 15. Optional Gain and Offset Trim.

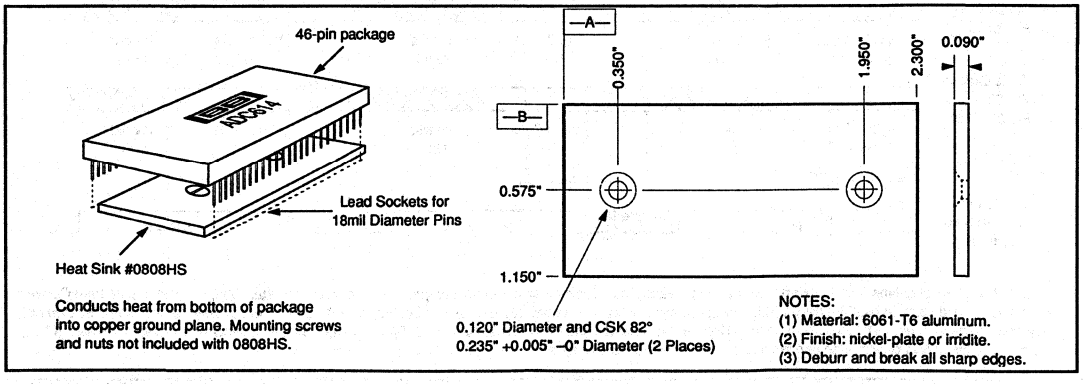


FIGURE 16. Heat Sink Transfers Heat from the DIP Package into a Copper Ground Plane.

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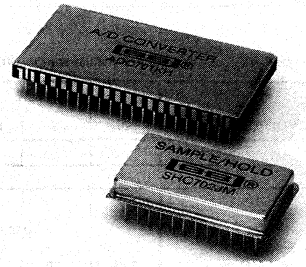


ADC701
SHC702

IMPROVED SPECIFICATIONS
NEW FEATURES

16-Bit 512kHz SAMPLING A/D CONVERTER SYSTEM

FEATURES

- CONVERSION RATE: to 512kHz Over Temp
- NO MISSING CODES AT 16 BITS
- SPURIOUS-FREE DYNAMIC RANGE: 107dB
- LOW NONLINEARITY: ±0.0015%
- SELECTABLE INPUT RANGES: ±5V, ±10V, 0 to +10V, 0 to +5V, –10V to 0
- LOW POWER DISSIPATION: 2.8W Typical Including Sample/Hold
- METAL AND CERAMIC DIP PACKAGES

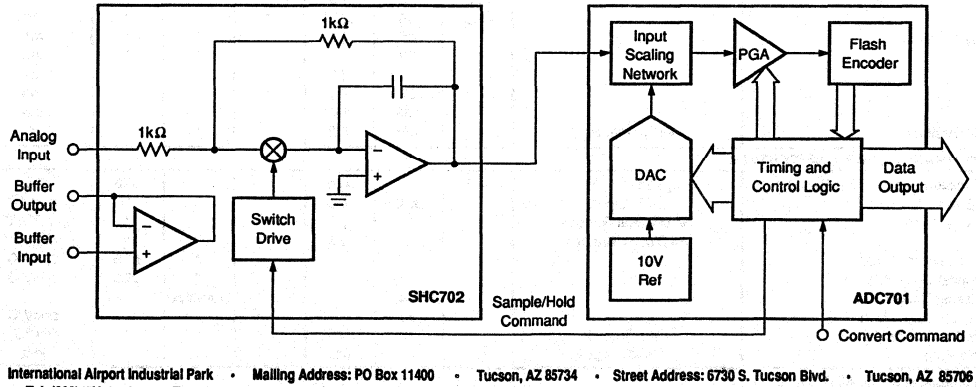
APPLICATIONS

- MEDICAL IMAGING
- SONAR
- PROFESSIONAL AUDIO RECORDING
- AUTOMATIC TEST EQUIPMENT
- HIGH PERFORMANCE FFT SPECTRUM ANALYSIS
- ULTRASOUND SIGNAL PROCESSING
- HIGH SPEED DATA ACQUISITION
- REPLACES DISCRETE MODULAR ADCs

DESCRIPTION

The ADC701 is a very high speed 16-bit analog-to-digital converter based on a three-step subranging architecture. Outstanding dynamic performance is achieved with the SHC702 companion sample/hold amplifier. Both devices use hybrid construction for applications where reliability, small size, and low power consumption are especially important.

Excellent linearity and stability are assured through use of a new ultra-precise monolithic D/A converter and a low-drift reference circuit. Custom monolithic op amps provide very high bandwidth and low noise in all sections of the analog signal path. Logic is CMOS/TTL compatible and is designed for maximum flexibility.



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Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL (ADC701 ONLY)

T_A = +25°C, 500kHz sampling rate, $\pm V_{CC}$ = ±15V, $\pm V_{DD1}$ = ±5V, $+V_{DD2}$ = +5V, and five minute warmup in a convection environment, unless otherwise noted.

PARAMETER	CONDITIONS	ADC701JH MIN	ADC701JH TYP	ADC701JH MAX	ADC701KH MIN	ADC701KH TYP	ADC701KH MAX	UNITS
RESOLUTION				16			*	Bits
INPUTS								
ANALOG								
Voltage Ranges	Unipolar			0 to +5, 0 to +10, –10 to 0				V
	Bipolar			±5, ±10				V
Resistance	0 to +5V Range	2.45	2.5	2.55	*	*	*	kΩ
	0 to +10V, –10 to 0, ±5V Ranges	4.9	5	5.1	*	*	*	kΩ
	±10V Range	9.8	10	10.2	*	*	*	kΩ
Capacitance	All Ranges		5			*		pF
DIGITAL								
Logic Family				TTL-Compatible CMOS				
Convert Command	Start Conversion			Rising Edge				
Pulse Width	t = Conversion Period	50		t – 50	*		*	ns
TRANSFER CHARACTERISTICS								
ACCURACY								
Gain Error[1]	0 to +10V Range		±0.03	±0.1		*	*	%
	±10V Range		±0.03	±0.1		*	*	%
Power Supply Sensitivity of Gain	All Ranges, All Supplies		±0.005	±0.1		*	*	%/V
Input Offset Error[1]	0 to +10V Range		±1	±3		*	*	mV
	±10V Range		±5	±10		*	*	mV
Power Supply Sensitivity of Offset	All Ranges, All Supplies		±0.006	±0.1		*	*	%FSR/V
Integral Linearity Error[2]			±0.002	±0.003		±0.0012	*	%FSR[3]
Differential Linearity Error[2]			±0.0006	±0.0012		*	*	%FSR
No Missing Codes			Guaranteed			Guaranteed		
Noise	$R_{SOURCE} \leq 50\Omega$		0.6			*		LSB rms
CONVERSION CHARACTERISTICS								
Sample Rate	Unadjusted	DC		512	*		*	kHz
Conversion Time[4]	Unadjusted		1.45	1.5		*	*	µs
OUTPUTS								
DIGITAL								
Logic Family				TTL-Compatible CMOS				
Data Coding	Unipolar Ranges			Straight Binary				
	Bipolar Ranges			Offset Binary				
Logic "0" Levels (V_{OL})	$I_{OL} \leq 3.2mA$		0.1	0.4		*	*	V
Logic "1" Levels (V_{OH})	$I_{OH} \leq 80\mu A$	4	4.9		*	*		V
Data Valid Setup Time Before Strobe	Both Edges	28	37		*	*		ns
INTERNAL REFERENCE								
Voltage	$R_{LOAD} \geq 5k\Omega$	+9.995	+10.000	+10.005	*	*	*	V
Current Available to External Loads		2	5		*	*		mA
POWER SUPPLY REQUIREMENTS								
Supply Voltages: $+V_{CC}$	Operating	+14.25	+15	+15.75	*	*	*	V
$-V_{CC}$		–14.25	–15	–15.75	*	*	*	V
$+V_{DD1}$		+4.75	+5	+5.25	*	*	*	V
$-V_{DD1}$		–4.25	–5	–6	*	*	*	V
$+V_{DD2}$		+4.25	+5	+5.25	*	*	*	V
Supply Currents: $+I_{CC}$	Operating		25	30		*	*	mA
$-I_{CC}$			33	45		*	*	mA
$+I_{DD1}$			45	55		*	*	mA
$-I_{DD1}$			37	50		*	*	mA
$+I_{DD2}$			133	150		*	*	mA
Power Dissipation	Nominal Voltages		1.95	2.3		*	*	W
PERFORMANCE OVER TEMPERATURE								
Specification Temperature Range	T_A Min to T_A Max	+15		+55	0		+70	°C
Gain Error	All Ranges		±10	±15		*	*	ppm/°C
Input Offset Error	All Unipolar Ranges		±1	±5		*	*	ppm FSR/°C
	All Bipolar Ranges		±1	±5		*	*	ppm FSR/°C
Integral Linearity Error[2]			±0.2			*	±0.5	ppm/°C
Differential Linearity Error[2]			±0.05			*	±0.3	ppm/°C
No Missing Codes			Typical			Guaranteed		
Reference Output Drift			±3			*		ppm/°C
Drift of Conversion Time	Unadjusted		+3	+4		*	*	ns/°C
Sample Rate	Unadjusted	DC		512	*		*	kHz

* Same specifications as ADC701JH.

SPECIFICATIONS

ELECTRICAL (SHC702 ONLY)

T_A = +25°C, 500kHz sampling rate, $\pm V_{CC}$ = ±15V, $+V_{DD1}$ = +5V, and five minute warmup in a convection environment, unless otherwise noted.

PARAMETER	CONDITIONS	SHC702JM MIN	SHC702JM TYP	SHC702JM MAX	UNITS
INPUTS (Without Input Buffer)					
ANALOG					
Voltage Range		±10.25	±11		V
Resistance		0.98	1	1.02	kΩ
Capacitance			3		pF
DIGITAL					
Logic Family			LSTTL		
Input Loading			2		LSTTL Loads
TRANSFER CHARACTERISTICS					
ACCURACY					
Gain	R_{SOURCE} = 0Ω		−1		V/V
Gain Error	R_{SOURCE} = 0Ω		±0.02	±0.1	%
Linearity Error	Sample Mode		±0.0003		%FSR
Offset Error	Sample Mode		±0.5	±3	mV
Charge Offset (Pedestal) Error	Sample/Hold Mode, R_{SOURCE} ≤ 50Ω		±0.5	±5	mV
Droop Rate	Hold Mode		±0.2	±2	µV/µs
Dynamic Nonlinearity	Sample/Hold Mode		±0.0005		%FSR
Power Supply Sensitivity	Offset Plus Charge Offset, All Supplies		±0.003		%FSR/V
DYNAMIC CHARACTERISTICS					
Acquisition Time	10V Step to ±150µV		600		ns
	5V Step to ±150µV		500		ns
Sample-to-Hold Settling Time[5]	to ±150µV		120		ns
Aperture Delay Time			20		ns
Aperture Uncertainty (Jitter)			10	25	ps rms
Slew Rate			150		V/µs
Small Signal Bandwidth	V_{IN} = ±1V		3.1		MHz
Full-Power Bandwidth	V_{IN} = ±10V		2		MHz
Feedthrough Rejection	Hold Mode, 10Vp-p Square Wave Input		0.001		%
OUTPUT					
Voltage Range	R_{LOAD} ≥ 1kΩ	±10.25	±11		V
Output Current		±40			mA
Short Circuit Protection	R_{LOAD} = 0Ω		Indefinite		
Output Impedance	DC		0.01	0.1	Ω
INPUT BUFFER CHARACTERISTICS					
INPUT					
Impedance			10^{13} || 3		Ω|| pF
Bias Current	V_{IN} = ±10V		±2	±15	pA
Offset Voltage	R_{SOURCE} ≤ 10kΩ		±0.3	±1.5	mV
Voltage Range		±10.25	±11		V
DYNAMIC CHARACTERISTICS					
Slew Rate		20	35		V/µs
Full-Power Bandwidth	V_{IN} = ±10V		570		kHz
Settling Time	10V Step to ±150µV		1.7		µs
OUTPUT					
Output Current		±15	±20		mA
Short Circuit Protection	R_{LOAD} = 0Ω		Indefinite		
POWER SUPPLY REQUIREMENTS					
Voltage: $+V_{CC}$	Operating	+13.5	+15	+16.5	V
$-V_{CC}$		−13.5	−15	−16.5	V
$+V_{DD1}$		+4.75	+5	+5.25	V
Current: $+I_{CC}$	Operating		33	40	mA
$-I_{CC}$			18	25	mA
$+I_{DD1}$			5	10	mA
Power Dissipation	Nominal Voltages		790	950	mW
PERFORMANCE OVER TEMPERATURE					
Specification Temperature Range	T_A Min to T_A Max	0		+70	°C
Sample/Hold Gain Error	R_{SOURCE} = 0Ω		±1	±5	ppm/°C
Sample/Hold Offset Error	R_{SOURCE} ≤ 50Ω		±10	±30	µV/°C
Sample/Hold Charge Offset Error	R_{SOURCE} ≤ 50Ω		±10	±80	µV/°C
Droop Rate				±50	µV/µs
Buffer Offset Error	R_{SOURCE} ≤ 10kΩ		±3	±15	µV/°C

NOTES: (1) Adjustable to zero. Tested and guaranteed for 0 to +10V and ±10V ranges only. (2) Peak-to-peak based on 99.9% of all codes. (3) FSR means full-scale range and depends on the input range selected. (4) ADC conversion time is defined as the time that the Sample/Hold must remain in the Hold mode; i.e., the duration of the Sample/Hold command. This time must be added to the Sample/Hold acquisition time to obtain the total system throughput time. (5) Given for reference only — this time overlaps with the ADC701 conversion time and does not affect system throughput rate.

SPECIFICATIONS

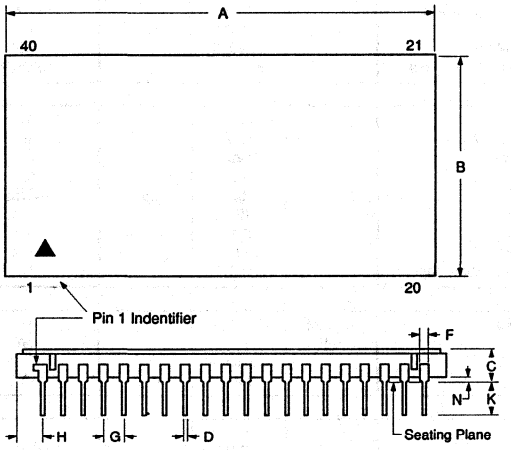
ELECTRICAL (COMBINED ADC701/SHC702)

T_A= +25°C, 500kHz sampling rate, $\pm V_{CC}$= ±15V, $\pm V_{DD1}$= ±5V, $+V_{DD2}$= +5V, and five minute warmup in a convection environment, ±5V input range unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Sample Rate	Unadjusted	DC		512	kHz
Dynamic Nonlinearity			±0.002		%FSR
Total Harmonic Distortion (THD)	f_{IN} = 20kHz (–0.3dB)		0.00068		%
	f_{IN} = 199kHz (–0.2dB)		0.0078		%
Spurious-Free Dynamic Range (SFDR)	f_{IN} = 20 kHz (–0.3dB)		107.1		dB
	f_{IN} = 199kHz (–12dB)		93.8		dB
Two-Tone Intermodulation Distortion (IMD)	f_1 = 195kHz (–6.5dB), f_2 = 200kHz (–6.5dB)		–81.4		dBC
	f_1 = 195kHz (–12.5dB), fF_2 = 200kHz (–12.5dB)		–86.2		dBC
Signal-to-Noise-Ratio (SNR)	f_{IN} = 5kHz (–0.5dB)		93		dB
Total Power Dissipation	Operating		2.8	3.25	W

ADC701 MECHANICAL

H Package— Metal and Ceramic



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	2.075	2.115	52.71	53.72
B	1.080	1.100	27.43	27.94
C	.145	.175	3.68	4.45
D	.018 TYP		0.46 TYP	
F	.040 TYP		1.02 TYP	
G	.100 TYP		2.54 TYP	
H	.093	.103	2.36	2.62
J	.020 BASIC		0.51 BASIC	
K	.205 BASIC		5.21 BASIC	
L	.900 BASIC		22.86 BASIC	
N	.015	.035	0.38	0.89

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.

ADC701 PIN ASSIGNMENTS

1	Bit 1/9 (Bit 1 = MSB)	40	$-V_{DD1}$ (–5V) Analog
2	Bit 2/10	39	Common (Analog)
3	Bit 3/11	38	$+V_{DD1}$ (+5V) Analog
4	Bit 4/12	37	Reference (Gain) Adjust
5	Bit 5/13	36	+10V Reference Output(2)
6	Bit 6/14	35	Common (Reference)
7	Bit 7/15	34	DNC
8	Bit 8/16	33	Common (Analog)
9	Clip Detect Output	32	+10V Reference Input(2)
10	$+V_{DD2}$ (+5V) Digital	31	Input D (1)
11	Common (Digital)	30	Input C (1)
12	Data Strobe	29	Common (Signal)
13	High/Low Byte Select	28	Input B (1)
14	Convert Command	27	Input A (1)
15	Sample/Hold Control(3)	26	$-V_{CC}$ (–15V) Analog
16	Common (Digital)	25	Common (Power)
17	Common (Digital)	24	$+V_{CC}$ (+15V) Analog
18	Clock Adjust	23	DNC(4)
19	Common (Digital)	22	Offset Adjust
20	$+V_{DD2}$ (+5V) Digital	21	Offset Adjust

NOTES: (1) Refer to Input Connection Table. (2) Reference Input is normally connected to Reference Output, unless an external 10V reference is used. (3) Sample/Hold Control goes high to activate Hold mode. (4) DNC = Do Not Connect.

ADC701 ORDERING INFORMATION

ADC701 ( ) H

- Basic Model Number
- Performance Grade Code
  - K: 0°C to +70°C Ambient Temperature
  - J: +15°C to +55°C Ambient Temperature
- Package Code
  - H: Metal and Ceramic

ADC701 ABSOLUTE MAXIMUM RATINGS

$\pm V_{CC}$	±18V
$\pm V_{DD1}$, $+V_{DD2}$	±7V, +7V
Analog Input	$\pm V_{CC}$
Logic Input	–0.5V to ($+V_{DD2}$ + 0.3V)
Logic Output	±25mA
Case Temperature	+150°C
Junction Temperature	+165°C
Storage Temperature	–65°C to +165°C
Power Dissipation	3W

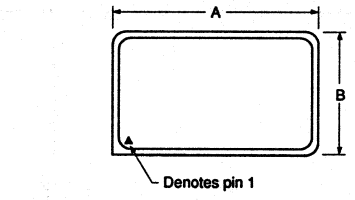
Stresses above these ratings may permanently damage the device.

ADC701 OUTPUT CODING

INPUT LEVEL (Exact Center of Code)	NOMINAL INPUT VOLTAGE TO ADC701 (Multiply by –1 for SHC702 Input Voltage) 0–10V RANGE (1LSB = 153µV)	±10V RANGE (1LSB = 305µV)	±5V RANGE (1LSB = 153µV)	OUTPUT CODE (1 = Logic High) MSB LSB	CLIP DETECT
Underrange	< –76µV	< –10.000153V	< –5.000076V	0000 0000 0000 0000	1
–FS	0V	–10V	–5V	0000 0000 0000 0000	0
–FS + 1LSB	+153µV	–9.999695V	–4.999847V	0000 0000 0000 0001	0
–3/4FS	+1.25V	–7.5V	–3.75V	0010 0000 0000 0000	0
–1/2FS	+2.5V	–5V	–2.5V	0100 0000 0000 0000	0
–1/4FS	+3.75V	–2.5V	–1.25V	0110 0000 0000 0000	0
–1LSB	+4.999847V	–305µV	–153µV	0111 1111 1111 1111	0
Mid-Scale	+5V	0V	0V	1000 0000 0000 0000	0
+1LSB	+5.000153V	+305µV	+153µV	1000 0000 0000 0001	0
+1/4FS	+6.25V	+2.5V	+1.25V	1010 0000 0000 0000	0
+1/2FS	+7.5V	+5V	+2.5V	1100 0000 0000 0000	0
+3/4FS	+8.75V	+7.5V	+3.75V	1110 0000 0000 0000	0
+FS –2LSB	+9.999695V	+9.99939V	+4.999695V	1111 1111 1111 1110	0
+FS – 1LSB	+9.999847V	+9.999695V	+4.999847V	1111 1111 1111 1111	0
Overrange	> +9.999924V	> +9.999847V	> +4.999924V	1111 1111 1111 1111	1

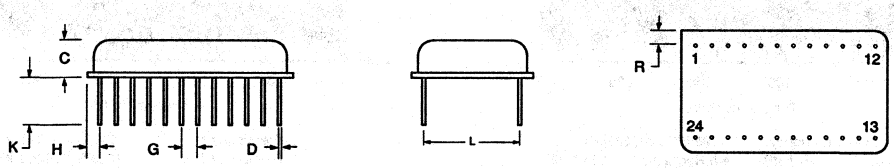
SHC702 MECHANICAL

M Package— Metal



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.365	1.385	34.67	35.18
B	.79	.810	20.07	20.57
C	.170	.250	4.32	6.35
D	.016	.021	0.41	0.53
G	.100 BASIC		2.54 BASIC	
H	.125	.150	3.18	3.81
K	.150	.300	3.81	7.62
L	.600 BASIC		15.24 BASIC	
R	.080	.110	2.03	2.79

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin material and plating composition conform to method 2003 (solderability of MIL-STD-883 (except paragraph 3.2)



SHC702 PIN ASSIGNMENTS

1	Sample/Hold Output	24	$+V_{CC}$ (+15V) Analog
2	NC[3]	23	Common (Power)
3	NC	22	$-V_{CC}$ (–15V) Analog
4	NC	21	Common (Analog)
5	NC	20	NC
6	NC	19	NC
7	NC	18	NC
8	NC	17	Buffer Amp Input[2]
9	$+V_{DD1}$ (+5V) Analog	16	NC
10	Common (Digital)	15	Common (Signal)
11	Hold Input[1]	14	Buffer Amp Output
12	Hold Input[1]	13	Analog Input

NOTES: (1) Hold mode is activated only when pin 12 is low and pin 11 is high. For normal use with ADC701, pin 12 is grounded and pin 11 is connected to ADC701 Sample/Hold control (ADC701 pin 15). (2) If the buffer amp is not used, pin 17 should be grounded. (3) NC = No Internal Connection.

SHC702 ORDERING INFORMATION

SHC702 J M

Basic Model Number

Performance Grade Code
J: 0°C to +70°C Ambient Temperature

Package Code
M: Metal

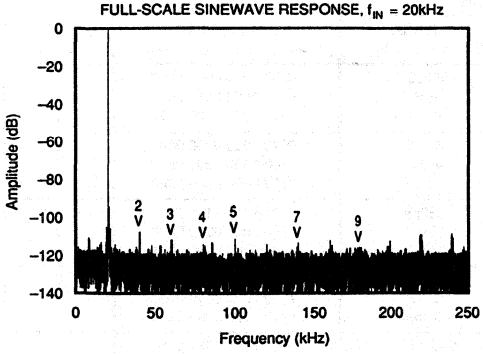
SHC702 ABSOLUTE MAXIMUM RATINGS

$\pm V_{CC}$	±18V
$+V_{DD1}$	+7V
Analog and Buffer Inputs	$\pm V_{CC}$
Outputs	Indefinite Short to Common
Logic Inputs	–0.5V to ($+V_{DD1}$ + 0.3V)
Case Temperature	+150°C
Junction Temperature	+165°C
Storage Temperature	–65°C to +165°C
Power Dissipation	1.5W

Stresses above these ratings may permanently damage the device.

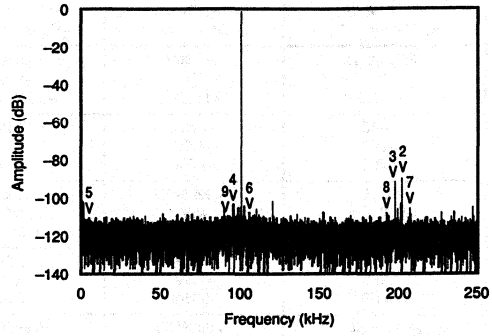
TYPICAL DYNAMIC PERFORMANCE (ADC701/SHC702)[1]

FULL-SCALE SINEWAVE RESPONSE, f_{IN} = 20kHz



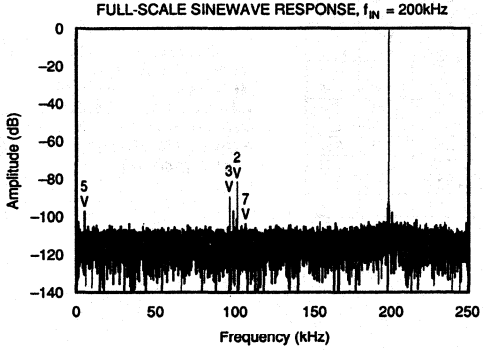
Input Frequency	19.9890136719 kHz		
Fundamental	–0.3 dB	4th Harmonic	–115.6 dB
2nd Harmonic	–107.5 dB	5th Harmonic	–111.2 dB
3rd Harmonic	–111.5 dB	6th Harmonic	–124.5 dB

FULL-SCALE SINEWAVE RESPONSE, f_{IN} = 100kHz



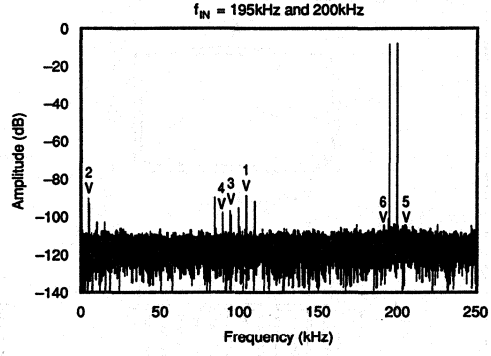
Input Frequency	100.982666016 kHz		
Fundamental	–0.5 dB	4th Harmonic	–102.5 dB
2nd Harmonic	–89.1 dB	5th Harmonic	–110.2 dB
3rd Harmonic	–90.5 dB	6th Harmonic	–106.8 dB

FULL-SCALE SINEWAVE RESPONSE, f_{IN} = 200kHz



Input Frequency	199.005126953 kHz		
Fundamental	–0.7 dB	4th Harmonic	–111.5 dB
2nd Harmonic	–81.4 dB	5th Harmonic	–97.0 dB
3rd Harmonic	–89.4 dB	6th Harmonic	–112.5 dB

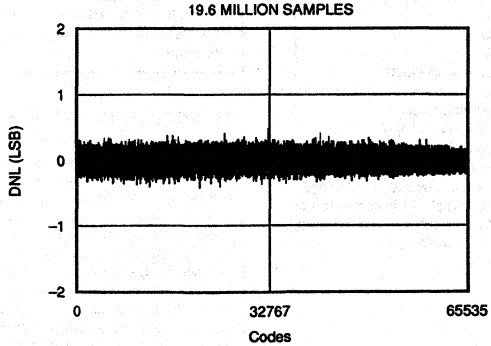
TWO-TONE INTERMODULATION RESPONSE, f_{IN} = 195kHz and 200kHz



	Frequency 1	194.976806641 kHz	
	Frequency 2	199.981689453 kHz	
f_1	–6.8 dB	3> f_1+2f_2	–96.0 dB
f_2	–6.3 dB	4> $2f_1+f_2$	–96.8 dB
1> f_1+f_2	–87.7 dB	5> f_1-2f_2	–104.9 dB
2> f_1-f_2	–88.8 dB	6> $2f_1-f_2$	–109.0 dB

NOTE: (1) For figures above, sampling rate = 500.0000000000kHz. 16,384 point FFT, non-windowed. Noise floor limited by synthesized generators.

DIFFERENTIAL NONLINEARITY OF ALL CODES, 19.6 MILLION SAMPLES



THEORY OF OPERATION

The ADC701 uses a three-step subranging architecture, meaning that the analog-to-digital conversion is performed in three passes which constitute coarse, medium and fine approximations of the input signal. Refer to Figures 1 and 2 for simplified block diagrams of the system.

Before the input signal is presented to the ADC, it must be sampled with high linearity and low aperture error by the sample/hold amplifier.

In the SHC702, the sampling switch is placed at the summing junction (virtual ground) of a high speed FET amplifier (Figure 1). This arrangement maintains constant charge injection independent of the signal amplitude, which is critically important for good linearity performance. The sampling switch itself is a high speed DMOS FET whose gate is driven from a fast-slewing control signal, thus minimizing the time aperture between the fully closed (sample mode) and the fully open (hold mode) states of the switch. The signal voltage is held across the feedback capacitor, forcing the op-amp to maintain a constant output voltage for the duration of the A/D conversion. Feedthrough from the input, already low due to the MOSFET's low capacitance, is further reduced by clamping the summing point to ground with another FET.

The ADC701 input voltage is converted to a current through the input scaling resistors (Figure 2), and this current is applied to the summing junction (virtual ground) of error amplifier A_1. The current output of the DAC (0 to 2mA) is also applied to the summing point. If bipolar operation is selected, the 10V reference output is applied to input D, creating a 1mA offset current which sums with the input current.

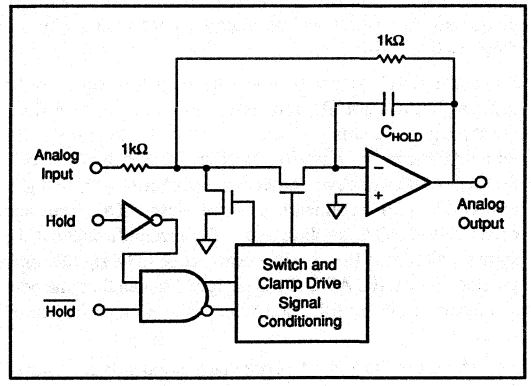


FIGURE 1. Simplified Block Diagram of the SHC702.

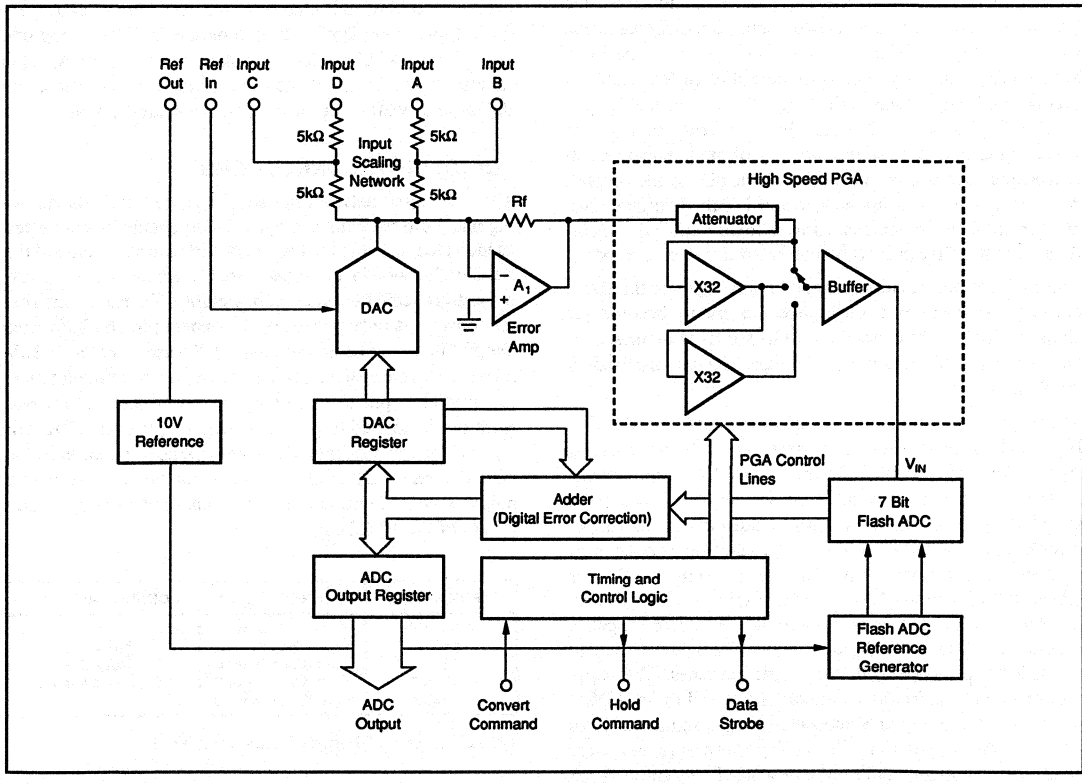


FIGURE 2. Simplified Block Diagram of the ADC701.

At the beginning of each conversion, the DAC is reset to mid-scale so that its output current is exactly 1mA. This 1mA is subtracted from the input signal current. The difference current flows through Rf and appears as an error voltage at the output of A_1.

During the first pass, the programmable gain amplifier (PGA) is set to unity gain, which matches the error voltage range to the input range of the flash ADC. The error signal is digitized to 7-bit resolution by the flash ADC, creating a coarse approximation of the digital output value, which is then applied to the DAC.

Since the DAC output is now approximately equal to the input signal current, the remaining difference current flowing through Rf is small—ideally less than 1/128 of full scale, which is due to the built-in quantizing uncertainty of the 7-bit flash ADC. However, other sources of error (e.g., integral and differential nonlinearity of the flash ADC, gain and offset of the PGA, settling and noise errors throughout the signal path) cause the possible error range to be significantly greater. In fact, the ADC701 is designed to handle remainder signals up to 1/32 of full scale, which is four times the "ideal" value.

Therefore, the PGA is set during the second pass to a gain of 32, allowing the small remainder signal to match the full range of the flash ADC. This is again digitized to 7-bit resolution and added to the previous result to create the "medium" approximation of the input signal. Because the full-scale range of the flash represents 1/32 of the input signal's full range, the 7-bit flash output is shifted right by 5 bits before being added to the original 7-bit "coarse" result, creating a 12-bit word. There is an overlap of two bits because the two least significant bits of the first-pass result correspond to the two most significant bits of the second-pass result. This overlap in the adder is called "digital error correction"—the mechanism that allows nonideal remainders from the first pass to be corrected in the second pass.

The 12-bit approximation is applied once again to the DAC, causing the remaining difference current to become yet smaller. For the third pass, the PGA's gain is increased by another factor of 32, and the remainder is again digitized by the flash ADC.

At this point in the conversion, all of the necessary data has been latched and it is no longer necessary to hold the analog signals from the sample/hold or the DAC. From a systems perspective, the conversion is now complete because the sample/hold is released to begin acquiring the next input sample and the DAC is reset to mid-scale for the next conversion. Meanwhile, the final result from the flash is added to the previous 12-bit result. Again there is a two-bit overlap to allow for error correction. The adder output is monitored to prevent a digital "rollover" condition, so that the ADC clips properly at the signal extremes. The upper sixteen bits of the final adder result are stored in the ADC's output register, ready to be presented in byte-sequential form at the eight output data lines. The overrange or "clip" condition can also be detected externally by monitoring pin 9. Refer to the section on ADC701 Digital I/O for further detail.

INSTALLATION AND OPERATING INSTRUCTIONS

The ADC701/SHC702 combination is designed to be easy to use in a wide variety of applications, without sacrificing flexibility of the analog and digital interface.

SHC702 INTERFACE

The connection diagram (Figure 3) shows the basic hookup. At the SHC702 input, the user may opt to connect the built-in FET buffer amplifier. The buffer is most useful in multichannel applications where the signal bandwidth is less than 100kHz. In those applications, it serves to isolate the multiplexer output from the 1kΩ input impedance of the sample/hold. For higher frequency applications and for any system that does not require the very high impedance, the best results (lowest noise and distortion) will be achieved by driving the SHC702's analog input directly. If the buffer is not used, its input should be grounded to avoid random noise pickup and saturation of the buffer op-amp.

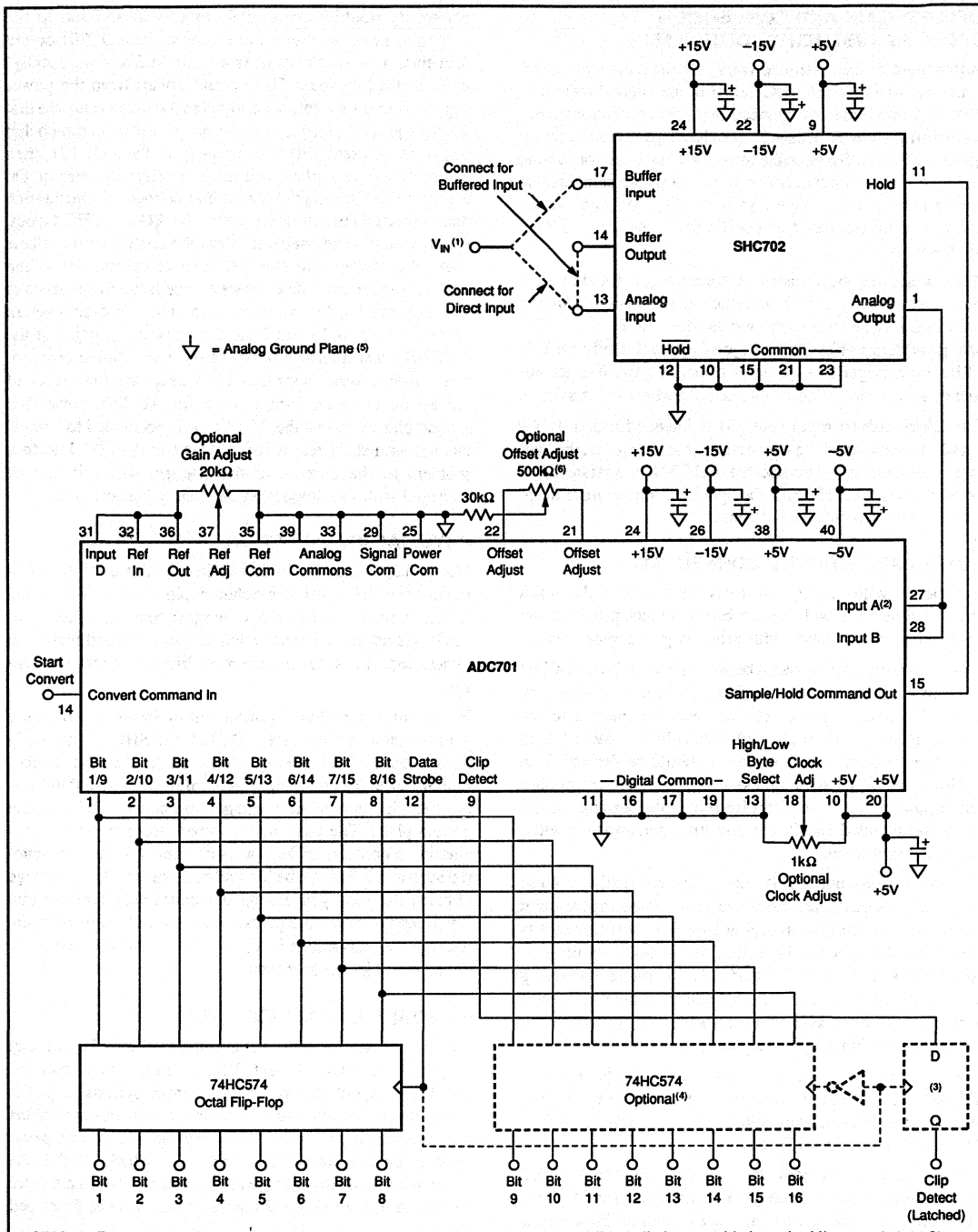
Only two connections are required between the SHC702 and the ADC701: SHC702 analog output to ADC701 input(s) and the digital Hold Command from the ADC701 to the SHC702. As always, it is best to avoid routing these analog and digital lines along parallel traces. Although the placement of the SHC702 relative to the ADC is not extremely critical, one good approach is to mount the SHC along one end of the ADC package as shown in Figure 4. This minimizes the length of the interconnections and keeps the digital lines well away from sensitive analog signals.

ADC701 INPUT CONNECTIONS

The ADC input network has four separate terminals, allowing many different input ranges. These should be connected as indicated in Table I. Most users will take advantage of the ADC701's built-in reference circuit, which has very low noise and excellent temperature stability. To use the internal reference, it is only necessary to connect pin 36 (Reference Output) to pin 32 (Reference Input). To use an external 10V reference (to cause the ADC gain to track a system reference, for example), pin 36 is left unconnected and the external reference is applied to pin 32. If required, the ADC701 will typically accommodate a five to ten percent variation in the 10V reference. External references should have very low noise to avoid degrading the excellent signal-to-noise ratio (SNR) of the ADC701.

INPUT RANGE	CONNECT V_{IN} TO	CONNECT Ref In TO
0 to +10V	Input A and Input D	—
±10V	Input A	Input D
±5V	Input A and Input B	Input D
−10V to 0	Input A and Input B	Input C and Input D
0 to +5V	Input B and Input C	—

TABLE I. ADC701 Input Connection Table.



NOTES: (1) For lowest distortion at high input frequencies the non-buffered option should be used. If the buffer is not used, its input should be grounded. (2) Shown connected for ±5V input range. Refer to Input Connection Table for other options. (3) If the Clip Detect feature is used, then the signal may be latched with a simple D type flip-flop as shown. See the section on ADC701 Digital I/O for additional applications information. (4) The second octal flip-flop is recommended but optional — it provides added digital signal isolation and buffering, and also permits three-state logic output compatibility. (5) All commons should be connected to the analog ground plane. Refer to the section on "Power and Ground Connections." (6) The Offset Adjust circuit shown provides an adjustment range of approximately ±0.25% FSR.

FIGURE 3. ADC701/SHC702 Connection Diagram.

OFFSET, GAIN AND CONVERSION SPEED ADJUSTMENTS (OPTIONAL)

Adjustment of the reference voltage is the most straightforward way to adjust the ADC gain. For the internal reference, this is accomplished by connecting a 20kΩ potentiometer as shown in Figure 3. This will provide a gain trim range of about ±3%. It is also possible to use external series or parallel resistance in the input network, but that is more cumbersome and usually will degrade the gain stability over temperature due to tempco (temperature coefficient) mismatches among the resistors.

ADC offset may be adjusted by connecting a 500kΩ potentiometer to pins 21 and 22, with the wiper connected through a series 30kΩ resistor to ground as shown in Figure 3. This will provide an offset trim range of approximately ±0.25% FSR. For a larger trim range of offset or gain, it is recommended that trims be accomplished elsewhere in the system.

The Clock Adjust input (pin 18) is intended primarily for small adjustments of the conversion time. However, this will rarely be necessary because the ADC701 is guaranteed to convert up to 512kHz over the specified temperature range without external clock adjustment.

POWER AND GROUND CONNECTIONS

Experience with testing and applying the ADC701 shows that it will perform well in most board layouts, provided that appropriate care is taken with grounding and bypassing.

Power supplies may be shared between the ADC701, SHC702 and other analog circuitry without difficulty. It is recommended that each power pin be locally bypassed to the ground plane with a high quality tantalum capacitor of at least 1µF. If at all possible, power should be derived from well-regulated linear supplies—switching power supplies will require much more effort for proper decoupling and are not recommended for this or any high performance wideband analog system.

The +5V Digital supply pins, though not as sensitive to noise as the +5V Analog pin, should nonetheless be kept as quiet as possible. If the system digital supply is noisy, then it is best to use the system +5V analog supply for all of the +5V connections on the ADC701 and SHC702 rather than trying to separate them. If only one +5V supply is available and it is shared with other system logic, then extra bypassing and/or supply filtering may be required.

The –5V supply will operate with any voltage between –4.75 and –6V. If –5V is not available from the system supplies, then an industry-standard 7905 regulator may be used to derive –5V from the –15V supply.

All ground pins on both the ADC701 and the SHC702 should be connected directly to a common ground plane. This is true for both analog and digital grounds. However, it is also helpful to recognize where the digital ground currents flow in the system, and to provide PC board return paths for potentially troublesome digital currents in addition to the ground plane connections. For example, the ADC701 output data lines will sink current (statically and/or dynamically) when in the low state. This current comes from the power supply that runs the interface logic, and so must return to that supply's ground. If the ground termination is placed such that this digital current will flow away from the ADC701, then the existing ground plane will suffice to carry the current. On the other hand, if the ground termination must be placed such that the digital current flows across the ADC or SHC layout, then it would be advisable to break the analog ground plane under the package (to stop the flow of current across the package) and to provide a separate trace (several centimeters wide) on another PC board layer to carry the digital return current from pins 11 and 19 to the termination point. If the ADC701 must interface into a fairly noisy digital environment, then another approach is to keep the first layer of latches and/or buffers connected to the ADC701 power and ground planes, so that the ADC itself is connected to "quiet" circuits with short return paths. This transfers the interface problem to the outputs of the latches, where it can be managed with less impact on the analog components.

PHYSICAL INSTALLATION

The packages may be soldered directly into a PC board or mounted in low-profile machined pin sockets with good results. Use of tall (long lead length) sockets, adapters or headers is not recommended unless a local ground plane and bypass capacitors can be mounted directly under the packages.

In a room-temperature environment or inside an enclosure with moderate airflow, the ADC701 and SHC702 normally do not require heat-sinking. However, to keep the devices running as cool as possible, it is helpful to install a thin heat-transfer plate under the packages to conduct heat into the ground plane. The plate may be made from metal (copper, aluminum or steel) or from a special heat-conductive material such as Sil-Pad[1]. The Sil-Pad material has the advantage of being electrically insulating and somewhat pliable, so that it will tend to distribute pressure evenly and conform to the package—an advantage in systems where the board may be flexed or subjected to vibration.

PC BOARD LAYOUT EXAMPLE

Figure 4 is an example of a printed circuit layout that integrates the ADC701 and SHC702 into a four-layer PC board. The layout shown includes jumper options to set the ADC input range, and shows placement of the optional offset and gain adjust potentiometers. Note that the ground plane layer is on the component (top) side, which shields the components from digital signals on other layers and provides the possibility of using a simple heat sink plate as described above.

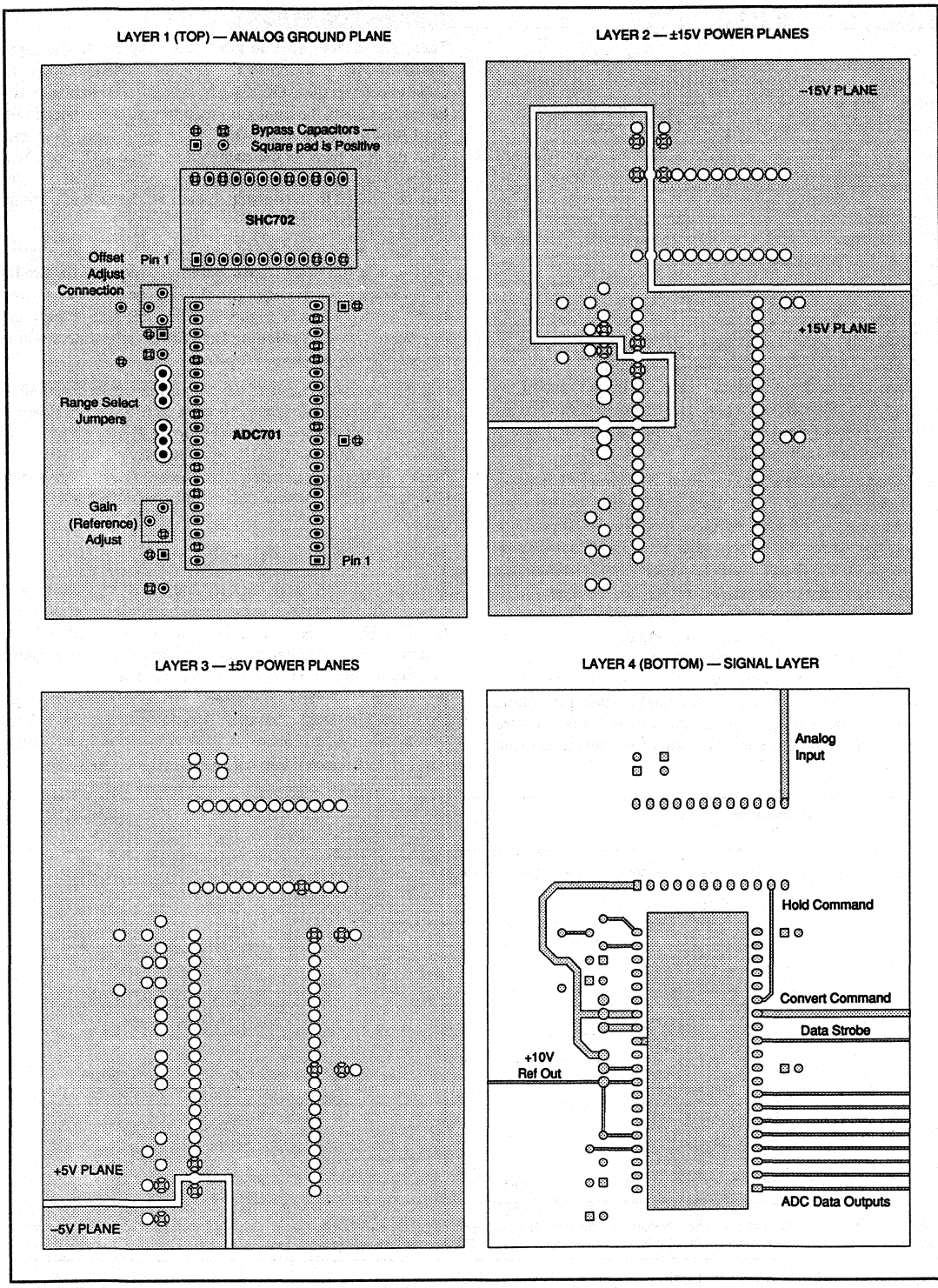


FIGURE 4. Example of Four-Layer PC Board Layout.

ADC701 DIGITAL I/O

Refer to the timing diagram, Figure 5. The conversion process is initiated by a rising edge on the Convert Command input. This will immediately bring the sample/hold command output to a logic high state (Hold mode).

After the ADC701 conversion is completed (approximately 1.5µs after the convert command edge), the Sample/Hold Command falls to a low state, enabling the sample/hold to begin acquisition of the next input sample. However, the ADC701 internal clock continues to run so that the output data may be processed.

There are two methods of reading data from the ADC:

1. Strobed Output—This will usually be the easiest and fastest method. The data are presented sequentially as high and low bytes of the total 16-bit word. The sequence High-Low or Low-High is controlled by the state of the High/Low Byte Select input. The first byte is valid on the rising edge of the Data Strobe output; the second byte is valid on the falling edge.
2. Polled output—With this method, data strobes will occur as described above, but they are ignored by the user. Instead, the user waits until the Data Strobe output falls, and then manually selects high and low output data by means of the High/Low Byte Select input. This polling procedure may be carried out during the subsequent ADC conversion cycle, but two precautions must be observed: First, the user should avoid switching the High/Low Byte Select immediately before or after the next convert command. This will prevent digital switching noise from coupling into the system at the instant of analog sampling. Second, the polling sequence must be completed before the ADC begins to strobe out data from the subsequent conversion.

OPTIONS FOR STROBED OUTPUT

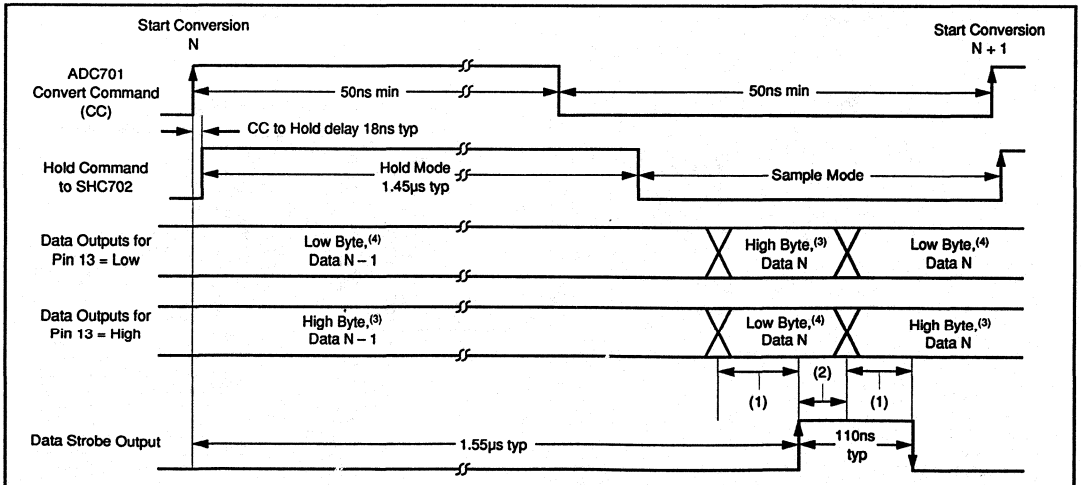
There are several ways in practice to implement the logic interface. Figure 3 shows the simplest configurations. In order to convert the ADC701's byte-sequential data into 16-bit parallel form, the minimum requirement is for one single octal flip-flop, such as a 74HC574 or equivalent. This will latch the first byte on the rising edge of the ADC701 Data Strobe. Then the second byte becomes valid, and all 16 bits may be strobed to the outside system on the falling edge of the Data Strobe.

For better noise isolation of the ADC701 from the digital system, or if full three-state capability is required for the 16 output lines, a second octal flip-flop can be added as shown in the dashed lines of Figure 3. This will also require an inverter to convert the falling Data Strobe edge into a rising clock edge for the second flip-flop IC.

If it is desirable to have all 16 output lines change simultaneously (for example when driving a D/A converter), then a third octal flip-flop (not shown in Figure 3) may be added to re-latch the output of the first byte. By driving that device's clock also from the inverted Data Strobe, fully synchronous switching of the 16 output bits will be achieved.

USING THE CLIP DETECT OUTPUT

The ADC701 provides a built-in Clip Detect signal on pin 9 which indicates an ADC overrange or underrange condition. The Clip Detect signal is only valid when the High Byte becomes valid as shown in Figure 5. Therefore, the simplest way to latch the Clip Detect signal is to provide an extra flip-flop which is clocked on the same strobe edge as the High Byte flip-flop. Such a setup is illustrated in Figure 3. The Clip Detect signal remains at logic 0 under normal conditions, and indicates a clip condition by rising to a logic 1.



NOTES: (1) Setup Time 28ns min, 37ns typ. (2) Hold Time 30ns min, 73ns typ. (3) High Byte refers to ADC bits 1–8, the most significant 8 bits. Also, the Clip Detect signal on pin 9 is valid simultaneously with High Byte. (4) Low Byte refers to ADC bits 9–16, the least significant bits.

FIGURE 5. ADC701 Interface Timing Diagram.

The latched version of Clip Detect may be used to generate an interrupt to the user's system computer, which would then launch a service routine to generate the appropriate alarms or corrective action. Another possible application would be to stretch the pulse using a monostable so that it would be easily visible when driving an LED warning lamp.

In some systems, it may be desirable to provide separate latched outputs for Underrange and Overrange. These conditions may be separately detected by using simple logic to implement the boolean equations:

$$\text{Underrange} = \text{Clip Detect AND } \overline{\text{Anybit}}$$

$$\text{Overrange} = \text{Clip Detect AND Anybit}$$

where "Anybit" is any one of the data output bits.

The Underrange and Overrange signals would then be latched into two separate flip-flops. A simple solution using a single '74 dual flip-flop and a single '00 quad NAND provides enough logic to implement the logic equations, with a spare NAND gate left over to use for creating the inverted Data Strobe signal.

USING THE ADC701 AT MAXIMUM CONVERSION RATES

The ADC701 is guaranteed to accept Convert commands at a rate of DC to 512kHz over the specified operating temperature range. At a conversion rate of 500kHz, the total throughput time of 2µs allows for the 1.5µs ADC conversion time plus 500ns for the digital output timing and sample/hold acquisition time.

If the user tries to exceed the maximum conversion rate by a large amount, the Convert Command of conversion N+1 will occur before the Data Strobe has fallen from conversion N. In such a situation, the ADC701 will simply ignore every other Convert command so the actual conversion rate will become half of the Convert command rate. Otherwise, the conversion will proceed normally. Note that the ADC timing slows down at high temperatures, so the frequency at which this occurs will vary with temperature—although it is still guaranteed to be greater than 512kHz over the specified temperature range.

Another consideration for operation at very high rates is that the sample/hold acquisition time becomes shorter as the conversion rate is increased. Users will note that the available acquisition time becomes less than 550ns at rates above 500kHz, which is less than the typical SHC702 acquisition time for a 10V step to 150µV accuracy. However, the signal degradation is gradual as the acquisition time is shortened—even at 512kHz, there is enough time to acquire a 5V step to better than 500µV. Also, most signal processing environments do not contain full-power signals at the Nyquist frequency, but rather show a rolloff of signal power at high frequencies. If the ability to acquire extremely large input changes at extremely high conversion rates is of paramount importance, the user may elect to use a Burr-Brown model SHC803 sample/hold instead—it is pin compatible with the SHC702 and provides much faster acquisition time at the expense of some extra noise and higher distortion at low input frequencies.

TESTING THE ADC701/SHC702

The ADC701 and SHC702 together form a very high performance converter system and careful attention to test techniques is necessary to achieve accurate results. Spectral analysis by application of a Fast Fourier Transform (FFT) to the ADC digital output is the best method of examining total system performance. Attempts to evaluate the system by analog reconstruction through a D/A converter will usually prove unsatisfactory; assuming that the static and dynamic distortions of the D/A can be brought below the required level (–110dB), the performance will still be beyond the range of presently available spectrum analyzers.

Even when the analysis is done using FFT techniques, several key issues must be addressed. First, the parameters of the FFT need to be adequate to perform the analysis and extract meaningful data. Second, the proper selection of test frequencies is critical for good results. Third, the limitations of commercial signal generators must be considered. These three points are addressed in later sections. Finally, the test board layout must follow the recommendations discussed on pages 8 through 10.

DYNAMIC PERFORMANCE DEFINITIONS

1. Total Harmonic Distortion (THD):

$$10 \log \frac{\text{Harmonic Power (first 9 harmonics)}}{\text{Sinewave Signal Power}}$$

2. Signal-to-Noise Ratio (SNR):

$$10 \log \frac{\text{Sinewave Signal Power}}{\text{Noise Power}}$$

3. Intermodulation Distortion (IMD):

$$10 \log \frac{\text{IMD Product Power (RMS sum; to 3rd order)}}{\text{Sinewave Signal Power}}$$

4. Spurious-Free Dynamic Range (SFDR):

$$10 \log \frac{\text{Power of Peak Spurious Component}}{\text{Sinewave Signal Power}}$$

IMD is referred to the larger of the test signals f_1 or f_2—**not** to the total signal power, which would result in a number approximately 6dB "better." The zero frequency bin (DC) is not included in these calculations—it represents total offset of the ADC, SHC and test equipment and is of little importance in dynamic signal processing applications.

FFT Parameters

Accurate FFT analysis of 16-bit systems requires adequate computing hardware and software. The FFT length (number of points) should be relatively large—at least 4K and preferably 16K or larger. There are several reasons for this:

1. The converter itself has 64K codes. Ideally, the test would guarantee that all codes are tested at least once. Practically speaking, however, that would require immensely long FFTs (>>64K points) or averaging of a large number of smaller FFTs. By using an FFT length of 4K or greater and proper selection of the test frequencies, a very good statistical picture of the ADC performance will be obtained which shows the effect of any defects in the transfer function.
2. The noise floor of the output spectrum is not low enough if less than 4K points are taken. Shorter FFTs have fewer bins to cover the output spectrum, so a larger fraction of the total system noise appears in each bin. Although the SNR of the ADC701/SCH702 system is in the range of –93dB, the noise level of the available generators may increase the total measured noise power to –80dB. Every doubling of the FFT length will spread the noise power among twice as many bins, resulting in a 3dB reduction of the spectral noise floor. In order to resolve spurious components that are at the level of –110dB, an average noise floor of less than –113dB would be barely adequate. This requires at least 2048 bins in the output half-spectrum, corresponding to a 4K-point FFT. Even at this level, it will be difficult or impossible to separate higher order harmonics in the ADC701 response from the average noise level, indicating that longer FFTs are desirable.
3. Following the guidelines for test frequency selection which are outlined in the next section, it becomes clear that longer FFTs allow a much wider choice of test frequencies without concern for sophisticated data windowing or code coverage problems.

Besides the consideration of FFT length, it is important to realize that the FFT calculations must be performed with high-precision arithmetic. The use of 32-bit fixed or floating point calculations will generally be inadequate because the noise floor due to calculation errors alone will interfere with the ADC performance data. Unfortunately, this consideration precludes the use of most DSP accelerator boards and similar hardware. In order to preserve the full dynamic range of the ADC output, it is best to use standard 64- or 80-bit arithmetic. To avoid excessively long calculation times, the FFT algorithm should be written in an efficiently compiled language and make use of techniques such as trigonometric look-up tables in software and dedicated floating-point coprocessors in hardware. There are several commercial software packages available from Burr-Brown and others that meet these requirements.

SELECTION OF TEST FREQUENCIES

The FFT (and any similar DSP operation) treats the total time-domain record length as one cycle of an infinitely long periodic signal. Therefore, if the end of the sampled record does not match up smoothly with the beginning, the output spectrum will contain serious errors known as leakage or truncation error[2]. This well-known problem is usually handled by applying a windowing function to the time-domain samples, suppressing the worst effects of the mismatch. However, the most often used windows such as Hanning, Hamming, raised cosine, etc., are completely inadequate for 16-bit ADC testing. More sophisticated functions such as the four-sample Blackman-Harris window[3] will provide much better results, although there still will be obvious spreading of the spectral lines.

The most successful approach is to eliminate the need for windowing by properly selecting the test signal frequency (or frequencies) in relation to the ADC sampling frequency[4]. If the time sample contains exactly an integer number of cycles, then there is no mismatch or truncation error. Another point to consider is that the sampling frequency should not be an exact integer multiple of the signal frequency, which would tend to reduce the number of different ADC codes that are tested and also tend to artificially concentrate quantization error in the harmonics of the test signal.

Both of these criteria are met by choosing an FFT length which is a power of two (the most standard and fastest to compute) and choosing a test frequency which causes an exact **odd** integer number of cycles to appear in the time record. In software, this selection can be accomplished very easily:

1. Determine the desired sampling frequency f_S.
2. Determine the desired input signal frequency f_{APPROX}.
3. Determine the FFT length N, which should be a power of 2 (e.g., 4096 or 16384).
4. Divide f_{APPROX} by f_S, multiply the quotient by N, and round the result to the nearest odd integer. This is M, the number of cycles in the time record.
5. Multiply M by f_S and divide by N to obtain the exact input signal frequency f_{ACTUAL}.

SIGNAL GENERATOR CONSIDERATIONS

To suppress leakage effects, the calculated ratio of f_S to f_{ACTUAL} must be precisely maintained during the test. This requirement is met easily by the use of synthesized signal generators whose reference oscillators can be locked together. Other possible approaches include external phase locking of non-synthesized generators and direct digital synthesis techniques. If it is not possible to use phase-locked signals, then a Blackman-Harris window may be used as mentioned previously.

Another key issue is the purity of both the signal and sampling frequency generators. The sampling clock's phase noise (jitter) will act as another source of SNR degradation. This is not serious as long as the jitter is random and the noise sidebands contain no sharp peaks. The HP3325 synthesizer is suitable for this purpose. The input signal generator will require more attention because its distortion will usually be greater than that of the ADC701/SHC702. Presently, the lowest distortion synthesized generator is the Brüel & Kjær Model 1051 (or 1049). This is suitable for testing the system in the audio range. The upper frequency limit of the B&K synthesizer is 200kHz. Above 20kHz, the distortion becomes a limiting factor, and low-pass filters must be inserted into the signal path to reduce the harmonic and spurious content.

As noted previously, the combined noise contributions of the signal generator and sampling clock generator far exceed the SNR of the ADC701/SHC702 itself. The SNR has been measured separately by applying a highly filtered sinewave to the input, resulting in typical SNR performance of –93dB. However, the filters employed to achieve this low-noise test stimulus are found to cause reactive loading of the signal source which results in increased distortion. Therefore it is best to separate the tests for SNR from those for THD and IMD, unless a suitably pure **and** low-noise signal can be generated.

Figures 6 and 7 show block diagrams of FFT test setups for the ADC701 and SHC702, summarizing the placement of the major components discussed above. The Typical Dynamic Performance section shows typical results obtained from testing the ADC701/SHC702 at a 500kHz conversion rate, using 16K samples for the FFT analysis.

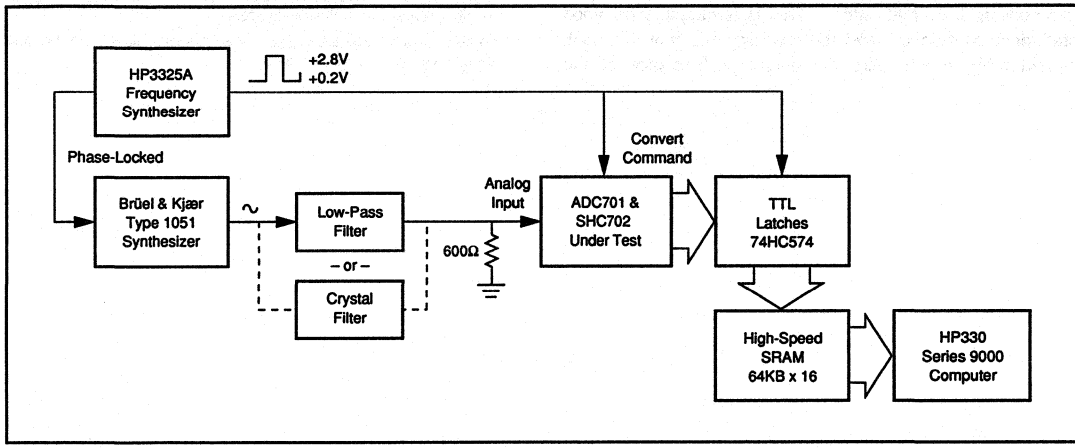


FIGURE 6. FFT Test Configuration for Single-Tone Testing.

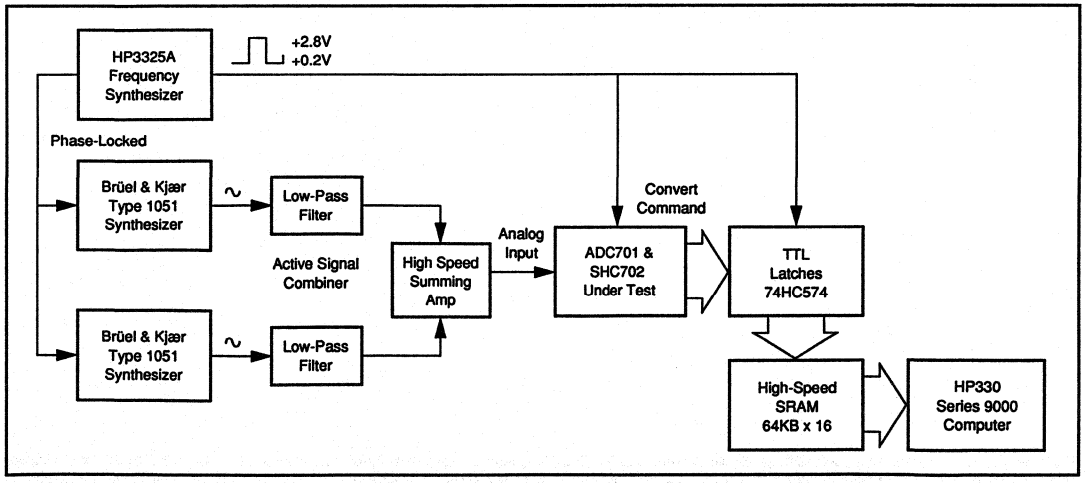


FIGURE 7. FFT Test Configuration for Two-Tone (Intermodulation) Testing.

HISTOGRAM TESTING

The FFT provides an excellent measure of harmonic and intermodulation distortion. Low-order spurious products are primarily caused by integral nonlinearity of the SHC and ADC. The influence of differential linearity errors is harder to distinguish in a spectral plot—it may show up as high-order harmonics or as very minor variations in the overall appearance of the noise floor.

A more direct method of examining the differential linearity (DL) performance is by using the popular histogram test method [5]. Application of the histogram test to the ADC701/SHC702 is relatively straightforward, though once again extra precision is required for a 16-bit system compared to 8- or 12-bit systems. Basically, this means that a very large number of samples are required to build an accurate statistical picture of each code width. If a histogram is taken using only one million points, then the average number of samples per code is less than fifteen. This is inadequate for good statistical confidence, and the resulting DL plot will look considerably worse than the actual performance of the converter. In practice 10 to 20 million samples will demonstrate good results for a 16-bit system and expose any serious flaws in the DL performance. If the memory incrementing hardware can keep pace with the ADC701, then 20 million samples can be accumulated in well under one minute. The last figure on page six shows the results of a 19.6 million point histogram taken at an input frequency of 1kHz.

NOTES:

1. Available from Bergquist, 5300 Edina Industrial Blvd., Minneapolis, MN 55435 (612) 835-2322.
2. Brigham, E. Oran, *The Fast Fourier Transform*, Englewood Cliffs, N.J.: Prentice-Hall, 1974.
3. Harris, Fredric J., "On the Use of Windows for Harmonic Analysis with the Discrete Fourier Transform", *Proceedings of the IEEE*, Vol. 66, No. 1, January 1978, pp 51-83.
4. Halbert, Joel M. and Belcher, R. Allan, "Selection of Test Signals for DSP-Based Testing of Digital Audio Systems", Journal of the Audio Engineering Society, Vol. 34, No. 7/8, July/August, 1986, pp 546-555.
5. "Dynamic Tests for A/D Converter Performance", Application Note AN-133, Burr-Brown Corporation, Tucson, AZ, 1985.

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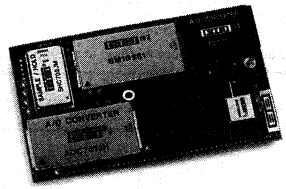


ADC750

ABRIDGED DATA SHEET— REQUEST COMPLETE DATA SHEET FROM BURR-BROWN SALES OFFICE

400kHz, Ultra-High Dynamic Range FLOATING-POINT A/D CONVERTER

FEATURES

- DYNAMIC RANGE: 116dB
- VERY HIGH RESOLUTION: 22 Bits
- FLOATING POINT FORMAT: 16 Bits Plus Gain Ranges of 1, 8 and 64
- INSTANTANEOUS GAIN RANGING: Automatic for each Conversion
- CONVERSION RATE: DC to 400kHz
- LOW POWER DISSIPATION: 5.3W
- SMALL SIZE: 3" x 5" Card

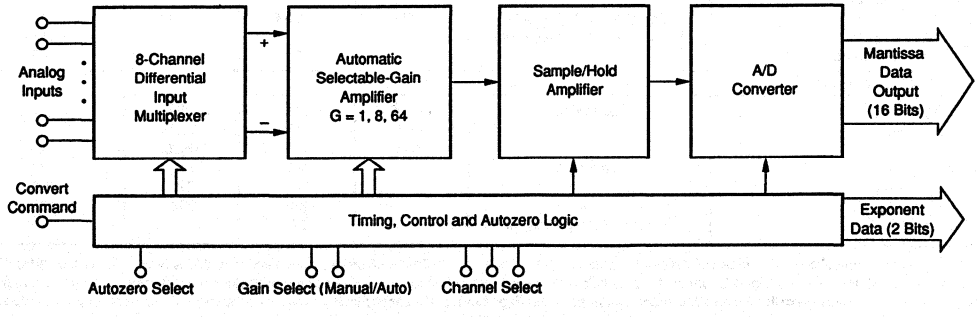
APPLICATIONS

- MEDICAL IMAGING SYSTEMS
- AUTOMATIC TEST EQUIPMENT
- SCIENTIFIC INSTRUMENTATION
- HIGH SPEED DATA ACQUISITION
- PARTICLE AND PHOTON DETECTORS
- REPLACES COMPLEX CUSTOM PRINTED CIRCUIT BOARDS

DESCRIPTION

The ADC750 provides an unusually powerful combination of speed and dynamic range in a small package. It achieves wide dynamic range with the combination of an internal 16-bit A/D converter (Burr-Brown's ADC701) and automatic gain ranging circuitry. The gain ranging amplifier, sometimes called a floating point amplifier, automatically and instantaneously selects the optimum gain range for each conversion.

The performance of the ADC750 across all gain ranges is optimized by precise design, factory calibration, and on-board autocalibration circuitry. The autocalibration feature ensures excellent differential linearity at the critical gain-switch points. The ADC750 includes a high speed, eight channel differential multiplexer and is specifically designed for applications with multiple unipolar input signals.



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SPECIFICATIONS

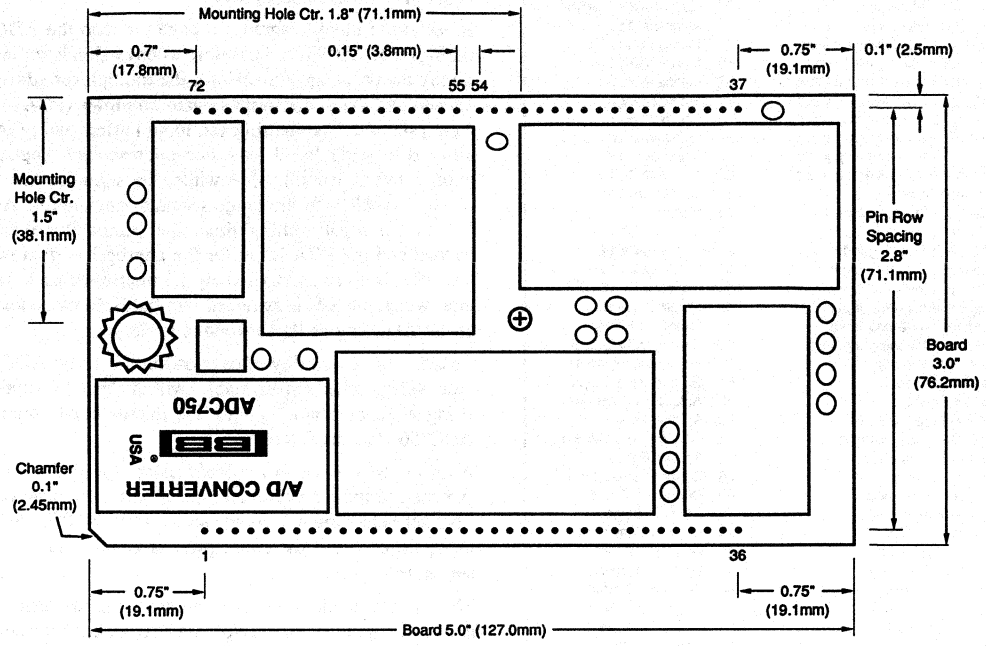
ELECTRICAL

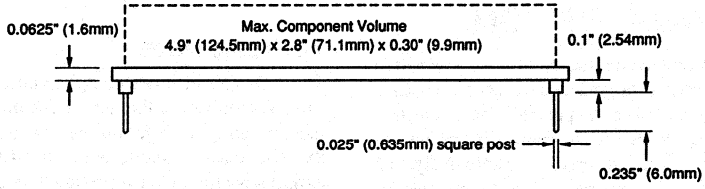
T_A = +25°C, 400kHz conversion rate, V_{CC} = ±15V, $+V_{DD}$ = +5V, and fifteen minute warmup in a convection environment, unless otherwise noted.

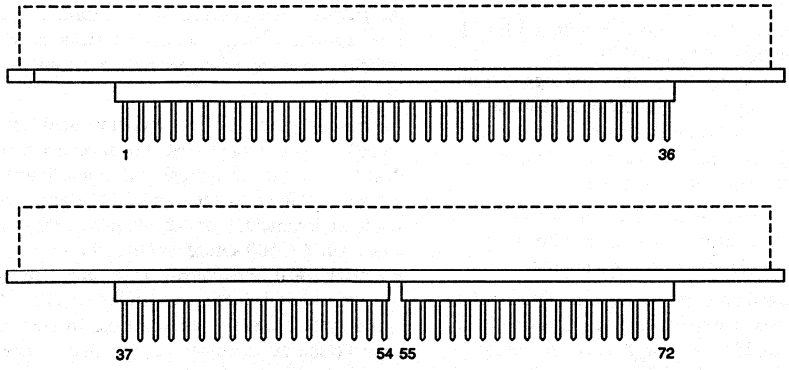
PARAMETER	CONDITIONS	ADC750 MIN	ADC750 TYP	ADC750 MAX	UNITS
FLOATING-POINT RESOLUTION				22	Bits
MANTISSA RESOLUTION				16	Bits
GAIN RANGES				1, 8, 64	
CONVERSION RATE	T_A min = +15°C to T_A max = +45°C	DC		400	kHz
INPUTS					
ANALOG					
Format			Eight Differential Channels, 10V Unipolar Range		
Voltage Range: Differential	All Channels	0		10	V
Common-Mode[1]	All Channels	–5		+5	V
Impedance	Any Selected Input		10^9 || 82		Ω || pF
Charge Injection	At Selected Input, During Switching		150		pC
DIGITAL					
Logic Family			TTL-Compatible CMOS		
Pull-Up Resistance	All Digital Inputs	10			kΩ
Convert Command Pulse Width	t = Conversion Period	50		t –50	ns
TRANSFER CHARACTERISTICS					
ACCURACY					
Gain Error	All Gain Ranges		0.1	0.2	%
Drift over Operating Temperature Range	T_A min = +15°C to T_A max = +45°C		±5		ppm/°C
Relative Gain Error of Adjacent Ranges			35		ppm
Drift over Operating Temperature Range	T_A min = +15°C to T_A max = +45°C		±4		ppm/°C
Gain Switch Threshold	Gain = 8 or 64	95	97	98.5	% Full Scale
Input Offset Error	Gain = 64 Range		25	50	µV
Drift over Operating Temperature Range	T_A min = +15°C to T_A max = +45°C		±0.1		µV/°C
Integral Linearity Error: Within Each Range	Deviation from Best-Fit Line[2]		±0.002	±0.003	% of Range
Across All Ranges	Deviation from Endpoint Line[3]			±0.015, ±0.006	% of RDG ± % of Range
Differential Linearity Error	Gain = 64 to Gain = 8 Transition		±18	±44	µV
	Gain = 8 to Gain = 1 Transition		±50	±344	µV
	Within Each Gain Range		±0.001		% of Full Scale
Input Noise Level: Gain = 64	Inputs Shorted		16	20	µVrms
Gain = 8	Inputs Shorted		34	45	µVrms
Gain = 1	Inputs Shorted		277	350	µVrms
AUTOZERO CHARACTERISTICS					
Minimum Autozero Time		1			Conversion Cycle
Minimum Autozero Frequency	In Still Air	1000			Conversions/Minute
Power-Up Calibration Requirement		500,000			Conversions
Autocalibration Duty Cycle in System	In Still Air		0.01		%
OUTPUTS					
DIGITAL					
Logic Family			TTL-Compatible CMOS		
Data Coding: Mantissa			Straight Binary		
Exponent			See Text		
Data Valid Setup Time Before Status Edge		70			ns
INTERNAL REFERENCE					
Voltage	Unadjusted, R_{LOAD} = 5kΩ	+9.995	+10.000	+10.005	V
Drift Over Operating Temperature Range	T_A min = +15°C to T_A max = +45°C		±3		ppm/°C
Current Available to External Loads		2	5		mA
POWER SUPPLY REQUIREMENTS					
Supply Voltages: $+V_{CC}$	Operating	+14.25	+15	+15.75	V
$-V_{CC}$		–14.25	–15	–15.75	V
$+V_{DD}$		+4.75	+5	+5.25	V
Supply Currents: $+I_{CC}$	Operating		115	140	mA
$-I_{CC}$			174	210	mA
$+I_{DD}$			192	230	mA
Power Dissipation	Nominal Supply Voltages		5.3		W

NOTES: (1) Common-Mode voltage is the mean of the + and – analog input voltages. (2) In Gain = 64 range, an additional ±0.003% (= ±9.5µV) is allowed to account for test system noise. (3) The overall Integral Linearity characteristic is the deviation from an ideal line, fixed at the endpoints of the transfer function. It is expressed as a first limit which is a percentage of the overall ADC reading (Mantissa and Exponent), and a second limit which is a percentage of Full Scale of the selected range. The allowable error tolerance at each reading is the sum of the first and second limits.

MECHANICAL







NOTES: (1) Pin spacing 0.1" (2.54mm) unless otherwise noted. (2) Mounting hole diameter 0.120" (3.05mm). (3) All dimensional tolerances ±0.005" unless otherwise noted.

PIN ASSIGNMENTS

1	Common (Analog)	72	Common (Digital)
2	+Ground Reference	71	Mantissa Bit 1 (MSB)
3	–Ground Reference	70	Mantissa Bit 2
4	Channel 1 Non-Inverting Input	69	Mantissa Bit 3
5	Channel 2 Non-Inverting Input	68	Mantissa Bit 4
6	Channel 3 Non-Inverting Input	67	Mantissa Bit 5
7	Channel 4 Non-Inverting Input	66	Mantissa Bit 6
8	Channel 5 Non-Inverting Input	65	Mantissa Bit 7
9	Channel 6 Non-Inverting Input	64	Mantissa Bit 8
10	Channel 7 Non-Inverting Input	63	Mantissa Bit 9
11	Channel 8 Non-Inverting Input	62	Mantissa Bit 10
12	Common (Analog)	61	Mantissa Bit 11
13	Channel 1 Inverting Input	60	Mantissa Bit 12
14	Channel 2 Inverting Input	59	Mantissa Bit 13
15	Channel 3 Inverting Input	58	Mantissa Bit 14
16	Channel 4 Inverting Input	57	Mantissa Bit 15
17	Channel 5 Inverting Input	56	Mantissa Bit 16 (LSB)
18	Channel 6 Inverting Input	55	Common (Digital)
19	Channel 7 Inverting Input	54	Exponent 8 Output
20	Channel 8 Inverting Input	53	Exponent 64 Output
21	Common (Analog)	52	Gain Select 8 Input
22	Do Not Connect	51	Gain Select 64 Input
23	Do Not Connect	50	Autozero Select Input
24	+10V Reference Input	49	Status Output
25	+10V Reference Output	48	Configuration Clock Input
26	Gain Adjust Input	47	/Output Enable
27	Common (Analog)	46	Channel Select 0
28	$+V_{CC}$ (+15V) Analog	45	Channel Select 1
29	$+V_{CC}$ (+15V) Analog	44	Channel Select 2
30	Common (Analog)	43	Convert Command
31	$-V_{CC}$ (–15V) Analog	42	Do Not Connect
32	$-V_{CC}$ (–15V) Analog	41	Do Not Connect
33	Common (Analog)	40	Common (Digital)
34	$+V_{DD1}$ (+5V) Analog	39	$+V_{DD2}$ (+5V) Digital
35	$+V_{DD1}$ (+5V) Analog	38	$+V_{DD2}$ (+5V) Digital
36	Common (Analog)	37	Common (Digital)

GENERAL DESCRIPTION

The ADC750 is a complete floating-point data acquisition system on a card. Output data consist of a 16-bit mantissa plus a two bit "exponent." The "exponent" data indicate a gain range of 1, 8 or 64, which is automatically and instantaneously selected for each conversion. Alternatively, the gain range may be specified externally prior to any conversion.

There are eight differential input channels with a full-scale range of 10V. For example, 0 to +10V, 0 to –10V, or –5V to +5V are all possible by applying the input signal to the appropriate differential inputs and, if necessary, applying an offsetting reference voltage to one input. However, the ADC transfer function is always unipolar, i.e. the "+" input must always be more positive than the "–" input.

System throughput (conversion rate) is at least 400kHz. The ADC750 is designed primarily for multiplexed input signals (switching among multiple low-frequency inputs).

Offset errors for the three different gain ranges are cancelled by a hardware autozero technique, which requires a periodic calibration cycle initiated by the user. Positive and negative ground-sense inputs are provided for maximum accuracy of autozero.

THEORY OF OPERATION

NORMAL (MEASURE) MODE

Refer to the block diagram on page one and the ADC750 timing diagram (Figure 1). Before a conversion is started (or during the previous conversion), the multiplexer address is latched and the programmable-gain amplifier (PGA) is set for a gain of 1. The multiplexer, input buffers and PGA are allowed to settle for at least one microsecond (depending upon conversion rate). Meanwhile, the signal at the PGA output is applied to the range-sensing comparators. At the end of the input settling time, the comparator data are latched and the PGA is set for the appropriate gain range. The PGA is given approximately 1.1 microseconds to settle, after which the S/H is switched into the Hold mode and the 16-bit ADC begins its conversion cycle.

To avoid the possibility of overload in the 16-bit ADC, the input voltage must remain stable (within about 1%) until the rising edge of Status—about 1.2 microseconds after the ADC750 Convert Command.

After the S/H is set to the Hold mode, the multiplexer is switched to the next channel (specified by the state of the Channel Select inputs). At the same time, the PGA is reset to a gain of 1 and the entire process begins again for the subsequent cycle.

The outputs of the gain-select comparators, besides being used to set the PGA gain factor, are also stored in the control logic circuit. These signals are used to create the Exponent 8 and Exponent 64 output data.

AUTOZERO MODE

The ADC750 includes complete autozero hardware on the card. The offsets of the three PGA gain ranges are adjusted independently to maintain the best possible transfer linearity. The autozero mode is designed to be very flexible—almost any ratio of autozero time to measurement mode time will be acceptable. Each individual conversion cycle may be designated as an autozero or a measurement cycle. Therefore, autozero operation can be suspended at any time (within one conversion period) to return to the measure mode.

Upon initial power-up, it is recommended that the autozero mode be engaged for at least 500,000 conversion cycles (less than two seconds at typical conversion rates) to bring the autozero up/down counters and DAC into adjustment. Under stable environmental conditions, an autozero "duty cycle" of about 0.01% (1500 autozero conversions/minute for $F_{CONVERT}$ = 250kHz) will be adequate. These autozero cycles may be interspersed with measurement cycles as needed to fit the user's system timing requirements. In environments with unpredictable airflow or temperature fluctuations, the autozero duty cycle may be increased as necessary to maintain stable operation.

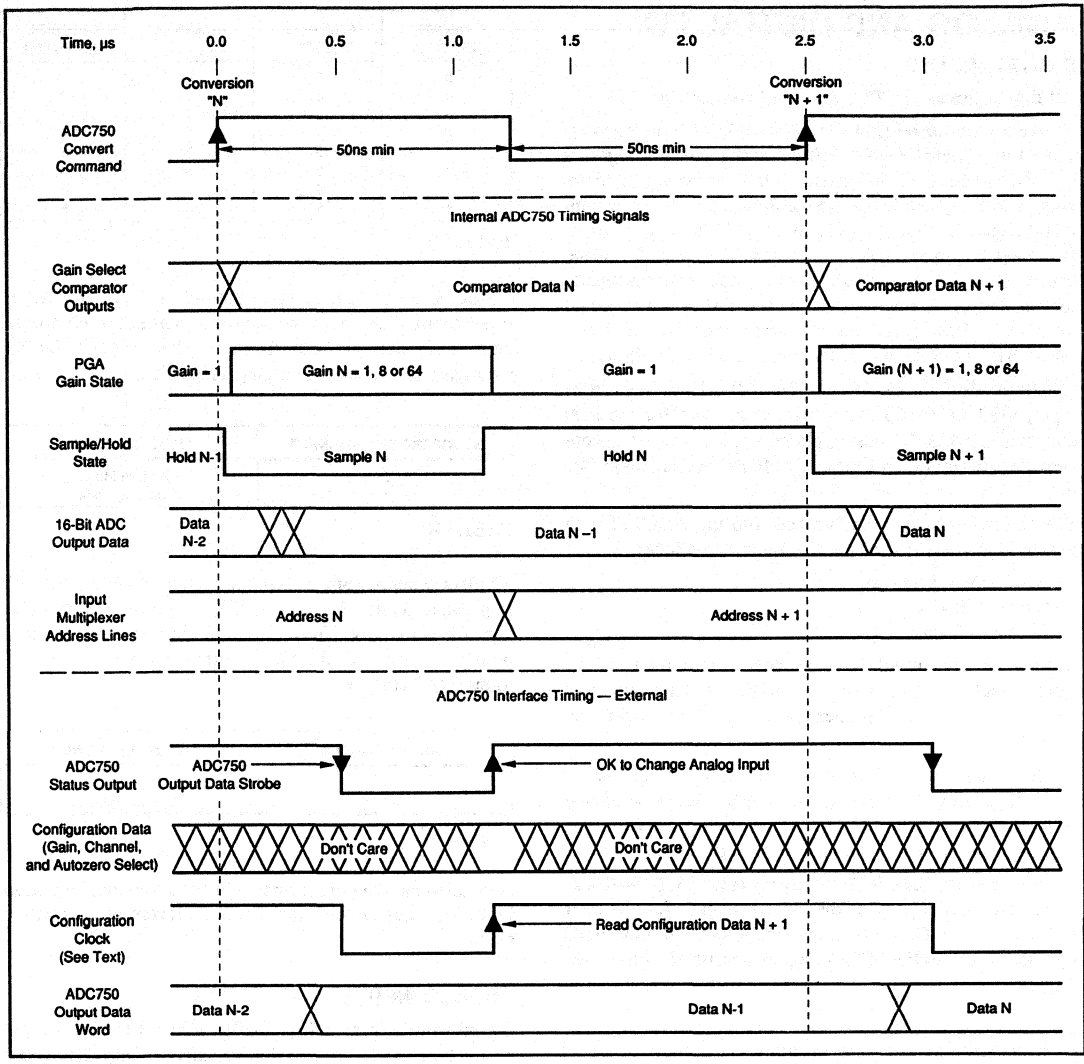


FIGURE 1. ADC750 Timing Diagram.

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ANALOG AND DIGITAL I/O

DIGITAL INPUTS

All digital inputs are TTL threshold compatible.

Convert Command (pin 43)—The ADC750 conversion is started by a low-to-high transition on this pin. The signal is edge-triggered and is not sensitive to duty cycle (minimum pulse width high or low = 50ns). Before the Convert Command signal occurs, the ADC input multiplexer and amplifiers have acquired the new input signal. Convert Command is used only to latch the outputs of the gain select comparators in Autogain mode. Note that the S/H is not triggered until approximately 1.1 microseconds after Convert Command. This method allows maximum timing flexibility.

Configuration Clock Input (pin 48)—This is a strobe input, used to set up the configuration data for the next conversion cycle. In most applications, it is easiest to connect the Configuration Clock input to the Status output (see Figure 1.)

The following signals are strobed into the ADC750 by a low-to-high transition of the Configuration Clock:

- Gain Select 8 and 64
- Channel Select 0, 1 and 2
- Autozero Mode Select

In some systems, it will be desirable to control the Configuration Clock independently of the ADC750 Status output. In such cases, the following rules apply to Configuration Clock timing:

- Configuration Clock must not rise before Status rises.
- Configuration Clock must rise at least 1300ns before the next Convert Command to allow sufficient analog settling time in the input multiplexer and PGA.

Gain Select 64, Gain Select 8 Inputs (pins 51, 52)—These inputs are used to select the ADC750 gain for the next conversion. The Gain Select data are strobed into the ADC by the Configuration Clock signal described above (see Table I.)

GAIN SELECT 64	GAIN SELECT 8	ADC750 GAIN
0	0	x 1
0	1	x 8
1	0	x 64
1	1	Autogain

TABLE I.

Channel Select 0, 1, 2 (pins 46, 45, 44)—These inputs are used to select the input channel for the next conversion. Note that it is not necessary to select input channels for Autozero Mode conversions; the Channel Select inputs are ignored in Autozero mode. The Channel Select data are strobed into the ADC by the Configuration Clock signal (see Table II.)

CHANNEL SELECT 2	CHANNEL SELECT 1	CHANNEL SELECT 0	CHANNEL SELECTED
0	0	0	1
0	0	1	2
0	1	0	3
0	1	1	4
1	0	0	5
1	0	1	6
1	1	0	7
1	1	1	8

TABLE II.

Autozero Select Input (pin 50)—This input is used to select between Autozero or Measure (normal) mode for the next conversion. It is strobed into the ADC750 by the Configuration Clock signal (see Table III.)

AUTOZERO SELECT INPUT	MODE SELECTED
0	Measure Mode
1	Autozero Mode

TABLE III.

/Output Enable (pin 47)—This signal activates the high impedance mode of the ADC750 output data word. This signal is active-low. Only the Mantissa and Exponent data outputs are affected; the Status output remains active at all times (see Table IV.)

/OUTPUT ENABLE	OUTPUT DATA LINES
0	Enabled
1	High Impedance

TABLE IV.

Note also that the output lines will be automatically placed in the high impedance state during Autozero mode conversions.

ANALOG INPUTS

Signal Inputs (pins 4-11, 13-20)—Each of the eight input channels are configured as high impedance, fully differential inputs. The maximum differential signal voltage is +10V, and the maximum common-mode signal range is –5V to +5V.

+ and – Ground Reference (pins 2, 3)—These inputs are used by the Autozero circuit to ensure that the input offset is calibrated to the user's signal ground potentials. In this manner, any small differences in ground potential between the positive and negative signal sources will be calibrated

out. If the input signal is single-ended or if the positive and negative signal inputs share a common ground potential, then the Ground Reference inputs may be connected directly to the system ground plane. Another use for the Ground Reference inputs is to create a small built-in offset in the ADC750 transfer function.

The Autozero circuit will accept up to 1.6mV between the + and – Ground Reference. Larger differential voltages on these pins may exceed the adjustment range of the Autozero circuitry, causing the ADC750 to malfunction.

+10V Reference Input (pin 24)—Normally, this pin will be connected to the ADC750's Reference Output, so that no external reference voltage is necessary. If desired, an external 10V reference may be connected to this point for system gain tracking. The load resistance presented by this pin will be greater than 5kΩ.

Gain Adjust Input (pin 26)—This pin adjusts the internal +10V reference, and so controls the gain of the ADC750 only if the internal reference is used. If it is necessary to adjust the gain, a 50kΩ potentiometer should be connected between the +10V Reference Output and Analog Common, with the wiper connected to the Gain Adjust pin.

DIGITAL OUTPUTS

Status Output (pin 49)—This signal is used for interface timing purposes. The low-to-high transition of Status indicates that the analog input signal may be switched to the next channel (i.e. the S/H is in the Hold mode and is no longer responding to the analog input). The Status signal rises approximately 1.2 microseconds after Convert Command.

The high-to-low transition of Status is used as an output data strobe. The ADC750 output data becomes valid at least 70ns before the falling edge of Status.

In most applications and for the highest throughput rate, it is recommended that the Status output signal be connected directly to the Configuration Clock input. The rising edge of Status is also very useful as a clock for switching an external multiplexer tree in systems with more than eight input channels.

Mantissa Bit 1 through Mantissa Bit 16 (pins 71 - 56)—These 16 lines represent the mantissa portion of the ADC750 output word. Mantissa 1 is the MSB and coding is straight binary. These lines are controlled by the Output Enable signal (described above). The output data become valid approximately 3.0 microseconds after Convert Command, with sufficient setup time before the falling edge of Status (described above).

Exponent 64, Exponent 8 Outputs (pins 53, 54)—These bits code the exponent of the output word. A high level on Exponent 8 indicates that the ADC is in a gain of 8, and the Mantissa data should be multiplied by 2^{-3}. Exponent 64 indicates that the ADC is in a gain of 64, and the Mantissa data should be multiplied by 2^{-6}. If Exponent 8 and Exponent 64 are both low, then the ADC is in a gain of 1, and the Mantissa data should be multiplied by $2^0 = 1$ (see Table V.)

If Exponent 8 and Exponent 64 are both high, then the ADC is overranged. In Autogain mode, this indicates that the differential input signal is either negative or it is greater than +10V. In fixed gain modes, it indicates that the input signal is beyond the limit of the selected range.

Exponent 8 and Exponent 64 are controlled by /Output Enable.

EXPONENT 64	EXPONENT 8	ADC750 GAIN
0	0	x 1
0	1	x 8
1	0	x 64
1	1	Overrange

TABLE V.

ANALOG OUTPUTS

+10V Reference Output (pin 25)—The ADC750's internal reference is brought out on this pin, and may be used as a system reference if needed. In order to use the internal reference for the ADC750, this pin must be connected back to the +10V Reference Input.

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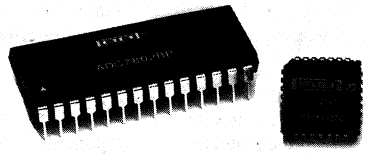


ADC7802

Autocalibrating, 4-Channel, 12-Bit ANALOG-TO-DIGITAL CONVERTER

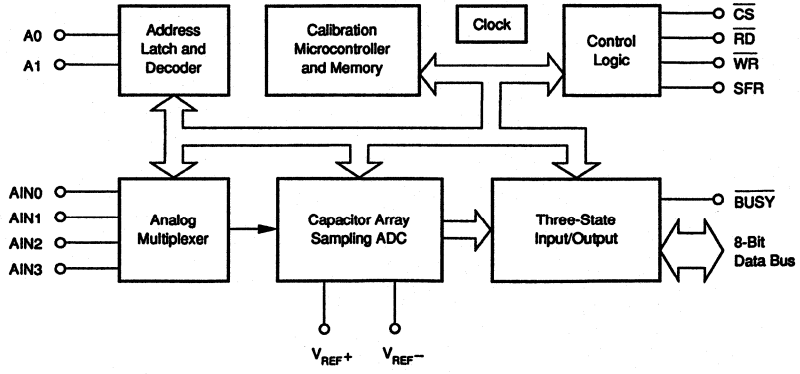
FEATURES

- **TOTAL UNADJUSTED ERROR ≤1/2LSB OVER FULL TEMPERATURE RANGE**
- **FOUR-CHANNEL INPUT MULTIPLEXER**
- **LOW POWER: 10mW plus Power Down Mode**
- **SINGLE SUPPLY: +5V**
- **FAST CONVERSION TIME: 8.5µs Including Acquisition**
- **AUTOCAL: No Offset or Gain Adjust Required**
- **UNIPOLAR INPUTS: 0V to 5V**
- **MICROPROCESSOR-COMPATIBLE INTERFACE**
- **INTERNAL SAMPLE/HOLD**

DESCRIPTION

The ADC7802 is a monolithic CMOS 12-bit A/D converter with internal sample/hold and four-channel multiplexer. An autocalibration cycle, occurring automatically at power on, guarantees a total unadjusted error within ±1/2LSB over the specified temperature range, eliminating the need for offset or gain adjustment. The 5V single-supply requirements and standard $\overline{CS}$, $\overline{RD}$, and $\overline{WR}$ control signals make the part very easy to use in microprocessor applications. Conversion results are available in two bytes through an 8-bit three-state output bus.

The ADC7802 is available in a 28-pin plastic DIP and 28-lead PLCC, fully specified for operation over the industrial –40°C to +85°C temperature range.



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Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL

$V_A = V_D = V_{REF}+ = 5V \pm 5\%$; $V_A \geq V_D \geq V_{REF}+$; $V_{REF}- = AGND = DGND = 0V$; CLK = 2MHz external with 50% duty cycle, $T_A = -40°C$ to $+85°C$, after calibration cycle at any temperature; unless otherwise specified.

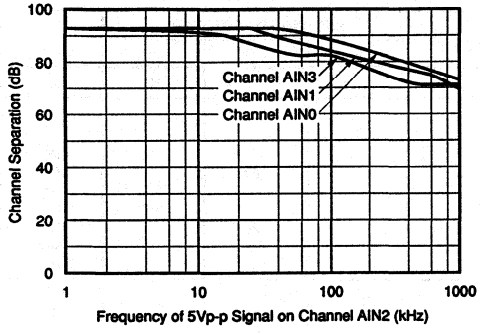
PARAMETER	CONDITIONS	ADC7802BP/ADC7802BN MIN	TYP	MAX	UNITS
RESOLUTION				12	Bits
ANALOG INPUT					
Voltage Input Range	$V_{REF}+ = 5V$, $V_{REF}- = 0V$	0		5	V
Input Capacitance			50		pF
On State Bias Current			100		nA
Off State Bias Current	$T_A = 25°C$			10	nA
	$T_A = -40°C$ to $+85°C$			100	nA
On Resistance Multiplexer			2		kΩ
Off Resistance Multiplexer			10		MΩ
Channel Separation	500Hz		92		dB
REFERENCE INPUT					
For Specified Performance: $V_{REF}+$	$V_{REF}+ \leq V_A$		5		V
$V_{REF}-$			0		V
For Derated Performance: [1] $V_{REF}+$		2.5		V_A	V
$V_{REF}-$		0		1	V
Input Reference Current	$V_{REF}+ = 5V$, $V_{REF}- = 0V$		10	100	µA
THROUGHPUT TIMING					
Conversion Time With External Clock (Including	CLK = 2MHz, 50% Duty Cycle			8.5	µs
Multiplexer Settling Time and Acquisition Time)	CLK = 1MHz, 50% Duty Cycle			17	µs
	CLK = 500kHz, 50% Duty Cycle			34	µs
With Internal Clock Using	$T_A = +25°C$			10	µs
Recommended Clock Components	$T_A = -40°C$ to $+85°C$		10		µs
Analog Signal Bandwidth [2]			500		Hz
Slew Rate [2]		8			mV/µs
Multiplexer Settling Time to 0.01%			460		ns
Multiplexer Access Time				20	ns
ACCURACY					
Total Adjusted Error,[3] All Channels				±1/2	LSB
Differential Nonlinearity				±1/2	LSB
No Missing Codes			Guaranteed		
Gain Error	All Channels			±1/4	LSB
Gain Error Drift	Between Calibration Cycles		±0.2		ppm/°C
Offset Error	All Channels			±1/4	LSB
Offset Error Drift	Between Calibration Cycles		±0.2		ppm/°C
Channel-to-Channel Mismatch				±1/4	LSB
Power Supply Sensitivity	$V_A = V_D = 4.75V$ to $5.25V$		±1/8		LSB
DIGITAL INPUTS					
All Pins Other Than CLK: V_{IL}				0.8	V
V_{IH}		2.4			V
Input Current	$T_A = +25°C$, $V_{IN} = 0$ to V_D			1	µA
	$T_A = -40°C$ to $+85°C$, $V_{IN} = 0$ to V_D			10	µA
CLK Input: V_{IL}				0.8	V
V_{IH}		3.5			V
I_{IL}				10	µA
I_{IH}				1.5	mA
I_{IH}	Power Down Mode (D3 in SFR HIGH)			100	nA
DIGITAL OUTPUTS					
V_{OL}	$I_{SINK} = 1.6mA$			0.4	V
V_{OH}	$I_{SOURCE} = 200µA$	4			V
Leakage Current	High-Z State, $V_{OUT} = 0V$ to V_D			±1	µA
Output Capacitance	High-Z State	4		15	pF
POWER SUPPLIES					
Supply Voltage for Specified Performance: V_A		4.75	5	5.25	V
V_D	$V_A \geq V_D$	4.75	5	5.25	V
Supply Current: I_A			1	2.5	mA
I_D	Logic Input Pins HIGH or LOW		1	2	mA
Power Dissipation	$\overline{WR} = \overline{RD} = \overline{CS} = \overline{BUSY}$ = HIGH		10		mW
Power Down Mode	See Table III, Page 9		50		µW
TEMPERATURE RANGE					
Specification		–40		+85	°C
Storage		–65		+150	°C

NOTES: (1) For $(V_{REF}+) - (V_{REF}-)$ as low as 2.5V, the total error will typically not exceed ±1LSB. (2) Faster signals can be accurately converted by using an external sample/hold in front of the ADC7802. (3) After calibration cycle, without external adjustment. Includes gain (full scale) error, offset error, integral nonlinearity, differential nonlinearity, and drift.

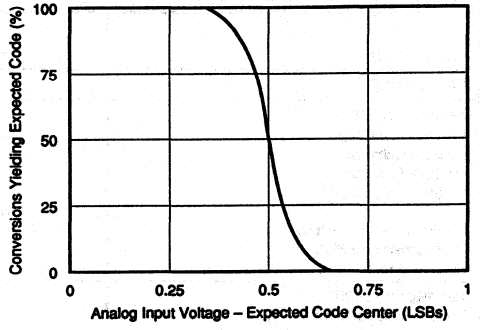
TYPICAL PERFORMANCE CURVES

$V_A = V_D = V_{REF}+ = 5V$, $V_{REF}- = AGND = 0V$, $T_A = +25°C$, unless otherwise specified.

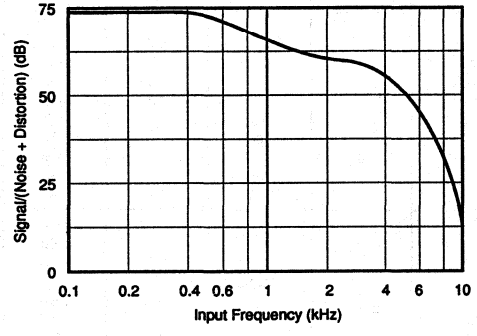
CHANNEL SEPARATION vs FREQUENCY



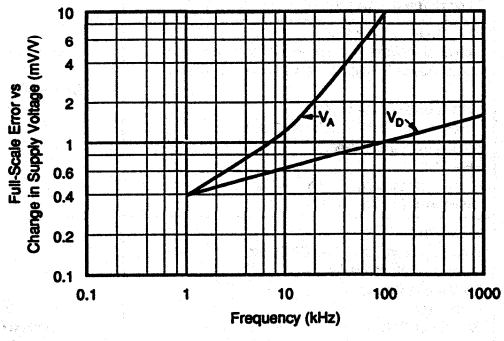
CODE TRANSITION NOISE



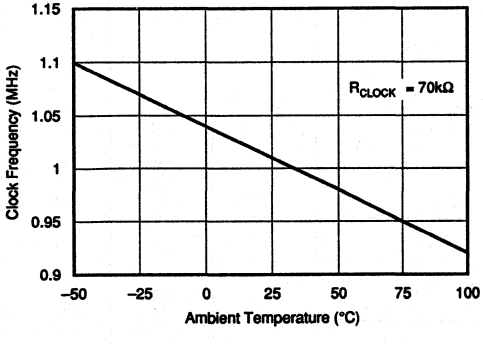
SIGNAL/(NOISE + DISTORTION) vs INPUT FREQUENCY



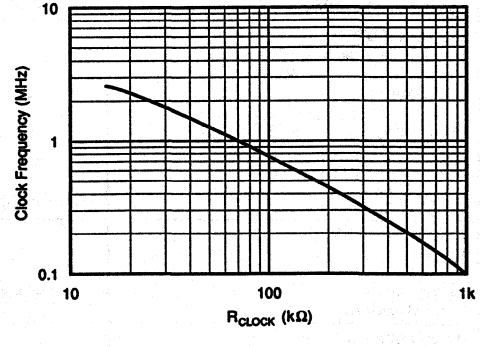
POWER SUPPLY REJECTION vs FREQUENCY



INTERNAL CLOCK FREQUENCY vs TEMPERATURE



INTERNAL CLOCK FREQUENCY vs R_{CLOCK}



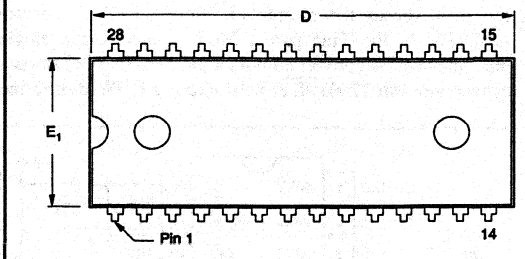
ORDERING INFORMATION

MODEL	MAXIMUM TOTAL ERROR, LSB	SPECIFICATION TEMPERATURE RANGE, °C	PACKAGE
ADC7802BN	±1/2	–40 to +85	PLCC
ADC7802BP	±1/2	–40 to +85	Plastic DIP

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

MECHANICAL

P Package — 28-Pin Plastic DIP

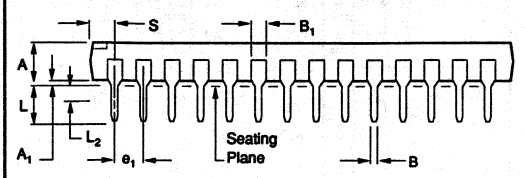


DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A(1)	.169	.200	4.29	5.08
A1(1)	.015	.070	0.38	1.78
B	.015	.020	0.38	0.51
B1	.015	.055	0.38	1.40
C	.008	.012	0.20	0.30
D(1)	1.380	1.455	35.05	36.96
E	.600	.625	15.24	15.88
E1(1)	.485	.550	12.32	13.97
e1	.100 BASIC		2.54 BASIC	
eA	.600 BASIC		15.24 BASIC	

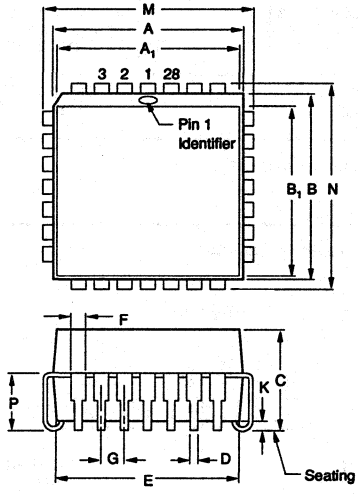
DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
L	.100	.200	2.54	5.08
L2	.000	.030	0.00	0.76
α	0°	15°	0°	15°
Q1	.020	.070	0.51	1.78
S1	.040	.080	1.02	2.03

(1) Not JEDEC Standard.

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.



N Package — 28-Pin Plastic LCC



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.450	0.460	11.43	11.68
A1	0.450	0.460	11.43	11.68
B	0.450	0.460	11.43	11.68
B1	0.450	0.460	11.43	11.68
C	0.165	0.180	4.19	4.57
D	0.013	0.023	0.33	0.58
E	0.390	0.430	9.91	10.92
F	0.026	0.032	0.66	0.81
G	0.050 BASIC		1.27 BASIC	
K	0.015	0.025	0.38	0.64
M	0.485	0.495	12.32	12.57
N	0.485	0.495	12.32	12.57
P	0.100	0.110	2.54	2.79

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.

ABSOLUTE MAXIMUM RATINGS

V_A to Analog Ground	6.5V
V_D to Digital Ground	6.5V
Pin V_A to Pin V_D	±0.3V
Analog Ground to Digital Ground	±1V
Control Inputs to Digital Ground	−0.3V to V_D + 0.3V
Analog Input Voltage to Analog Ground	−0.3V to V_D + 0.3V
Maximum Junction Temperature	150°C
Internal Power Dissipation	875mW
Lead Temperature (soldering, 10s)	+300°C
Thermal Resistance, θ_{JA}: Plastic DIP	75°C/W
PLCC	75°C/W

THEORY OF OPERATION

ADC7802 uses the advantages of advanced CMOS technology (logic density, stable capacitors, precision analog switches, and low power consumption) to provide a precise 12-bit analog-to-digital converter with on-chip sampling and four-channel analog-input multiplexer.

The input stage consists of an analog multiplexer with an address latch to select from four input channels.

The converter stage consists of an advanced successive approximation architecture using charge redistribution on a capacitor network to digitize the input signal. A temperature-stabilized differential auto-zeroing circuit is used to minimize offset errors in the comparator. This allows offset errors to be corrected during the acquisition phase of each conversion cycle.

Linearity errors in the binary weighted main capacitor network are corrected using a capacitor trim network and correction factors stored in on-chip memory. The correction terms are calculated by a microcontroller during a calibration cycle, initiated either by power-up or by applying an external calibration signal at any time. During conversion, the correct trim capacitors are switched into the main capacitor array as needed to correct the conversion accuracy. This is faster than a complex digital error correction system, which could slow down the throughput rate. With all of the capacitors in both the main array and the trim array on the same chip, excellent stability is achieved, both over temperature and over time.

For flexibility, timing circuits include both an internal clock generator and an input for an external clock to synchronize with external systems. Standard control signals and three-state input/output registers simplify interfacing ADC7802 to most micro-controllers, microprocessors or digital storage systems.

Finally, this performance is matched with the low-power advantages of CMOS structures to allow a typical power consumption of 10mW.

OPERATION

BASIC OPERATION

Figure 1 shows the simple circuit required to operate ADC7802 in the Transparent Mode, converting a single input channel. A convert command on pin 20 ($\overline{WR}$) starts a conversion. Pin 22 ($\overline{BUSY}$) will output a LOW during the

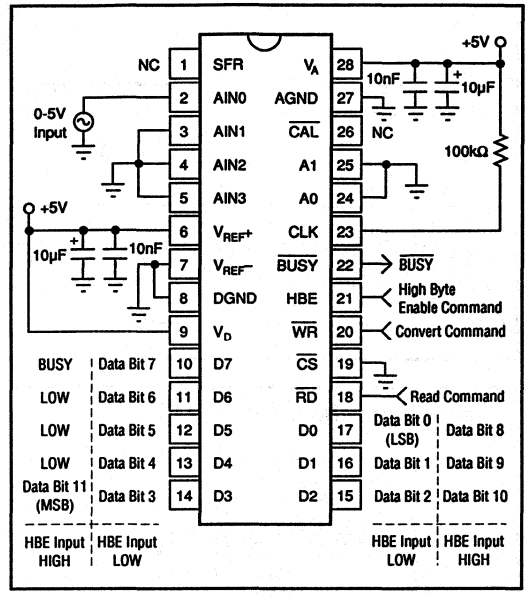
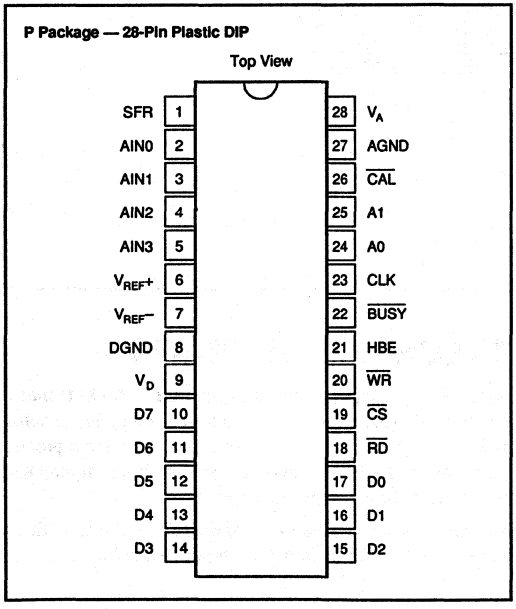
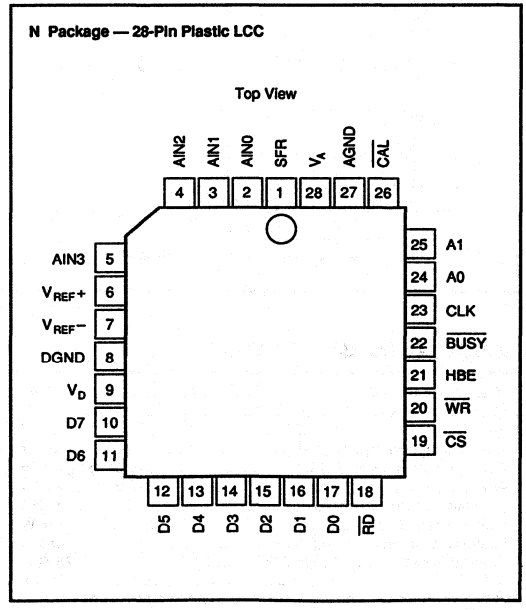


FIGURE 1. Basic Operation.

PIN CONFIGURATIONS





conversion process (including sample acquisition and conversion), and rises only after the conversion is completed. The two bytes of output data can then be read using pin 18 ($\overline{RD}$) and pin 21 (HBE).

STARTING A CONVERSION

A conversion is initiated on the rising edge of the $\overline{WR}$ input, with valid signals on A0, A1 and $\overline{CS}$. The selected input channel is sampled for five clock cycles, during which the comparator offset is also auto-zeroed to below 1/4LSB of error. The successive approximation conversion takes place during clock cycles 6 through 17.

Figures 2 and 3 show the full conversion sequence and the timing to initiate a conversion.

CALIBRATION

A calibration cycle is initiated automatically upon power-up (or after a power failure). Calibration can also be initiated by the user at any time by the rising edge of a minimum 100ns-wide LOW pulse on the $\overline{CAL}$ pin (pin 26), or by setting D1 HIGH in the Special Function Register (see SFR section). A calibration command will initiate a calibration cycle, regardless of whether a conversion is in process. During a calibration cycle, convert commands are ignored.

Calibration takes 168 clock cycles, and a normal conversion (17 clock cycles) is added automatically. For maximum accuracy, the supplies and reference need to be stable during the calibration procedure. To ensure that supply voltages and reference voltages have settled and are stable, an internal timer provides a waiting period of 42,425 clock cycles between power-up/power-failure and the start of the calibration cycle.

READING DATA

Data from the ADC7802 is read in two 8-bit bytes, with the Low byte containing the 8 LSBs of data, and the High byte containing the 4 MSBs of data. The outputs are coded in straight binary (with 0V = 000 hex, 5V = FFF hex), and the data is presented in a right-justified format (with the LSB as the most right bit in the 16-bit word). Two read operations are required to transfer the High byte and Low byte, and the bytes are presented according to the input level on the High Byte Enable pin (HBE).

PIN ASSIGNMENTS

PIN #	NAME	DESCRIPTION
1	SFR	Special Function Register. When connected to a microprocessor address pin, allows access to special functions through D0 to D7. See the sections discussing the Special Function Register. If not used, connect to DGND. This pin has an internal pull-down.
2 to 5	AIN0 to AIN3	Analog Inputs. Channel 0 to channel 3.
6	$V_{REF}+$	Positive voltage reference input. Normally +5V. Must be ≤ V_A.
7	$V_{REF}-$	Negative voltage reference input. Normally 0V.
8	DGND	Digital ground. DGND = 0V.
9	V_D	Logic supply voltage. V_D = +5V. Must be ≤ V_A and applied after V_A.
10 to 17	D0 to D7	Data Bus Input/Output Pins. Normally used to read output data. See section on SFR (Special Function Register) for other uses. When SFR is LOW, these function as follows:
10	D7	Data Bit 7 if HBE is LOW; if HBE is HIGH, acts as converter status pin and is HIGH during conversion or calibration, goes LOW after the conversion is completed. (Acts as an inverted $\overline{BUSY}$.)
11	D6	Data Bit 6 if HBE is LOW; LOW if HBE is HIGH.
12	D5	Data Bit 5 if HBE is LOW; LOW if HBE is HIGH.
13	D4	Data Bit 4 if HBE is LOW; LOW if HBE is HIGH.
14	D3	Data Bit 3 if HBE is LOW; Data Bit 11 (MSB) if HBE is HIGH.
15	D2	Data Bit 2 if HBE is LOW; Data Bit 10 if HBE is HIGH.
16	D1	Data Bit 1 if HBE is LOW; Data Bit 9 if HBE is HIGH.
17	D0	Data Bit 0 (LSB) if HBE is LOW; Data Bit 8 if HBE is HIGH.
18	$\overline{RD}$	Read Input. Active LOW; used to read the data outputs in combination with $\overline{CS}$ and HBE.
19	$\overline{CS}$	Chip Select Input. Active LOW.
20	$\overline{WR}$	Write Input. Active LOW; used to start a new conversion and to select an analog channel via address inputs A0 and A1 in combination with $\overline{CS}$. The minimum $\overline{WR}$ pulse LOW width is 100ns.
21	HBE	High Byte Enable. Used to select high or low data output byte in combination with $\overline{CS}$ and $\overline{RD}$, or to select SFR.
22	$\overline{BUSY}$	$\overline{BUSY}$ is LOW during conversion or calibration. $\overline{BUSY}$ goes HIGH after the conversion is completed.
23	CLK	Clock Input. For internal/external clock operation. For external clock operation, connect pin 23 to a 74 HC-compatible clock source. For internal clock operation, connect pin 23 per the clock operation description.
24 to 25	A0 to A1	Address Inputs. Used to select one of four analog input channels in combination with $\overline{CS}$ and $\overline{WR}$. The address inputs are latched on the rising edge of $\overline{WR}$ or $\overline{CS}$. A1 / A0 / Selected Channel LOW / LOW / AIN0 LOW / HIGH / AIN1 HIGH / LOW / AIN2 HIGH / HIGH / AIN3
26	$\overline{CAL}$	Calibration Input. A calibration cycle is initiated when $\overline{CAL}$ is LOW. The minimum pulse width of $\overline{CAL}$ is 100ns. If not used, connect to V_D. In this case calibration is only initiated at power on, or with SFR. This pin has an internal pull-up.
27	AGND	Analog Ground. AGND = 0V.
28	V_A	Analog Supply. V_A = +5V. Must be ≥ V_D and $V_{REF}+$.

The bytes can be read in either order, depending on the status of the HBE input. If HBE changes while $\overline{CS}$ and $\overline{RD}$ are LOW, the output data will change to correspond to the HBE input. Figure 4 shows the timing for reading first the Low byte and then the High byte.

ADC7802 provides two modes for reading the conversion results. At power-up, the converter is set in the Transparent Mode.

TRANSPARENT MODE

This is the default mode for ADC7802. In this mode, the conversion decisions from the successive approximation register are latched into the output register as they are made. Thus, the High byte (the 4 MSBs) can be read after the end of the ninth clock cycle (five clock cycles for the mux settling, sample acquisition and auto-zeroing of the comparator, followed by the four clock cycles for the 4MSB deci-

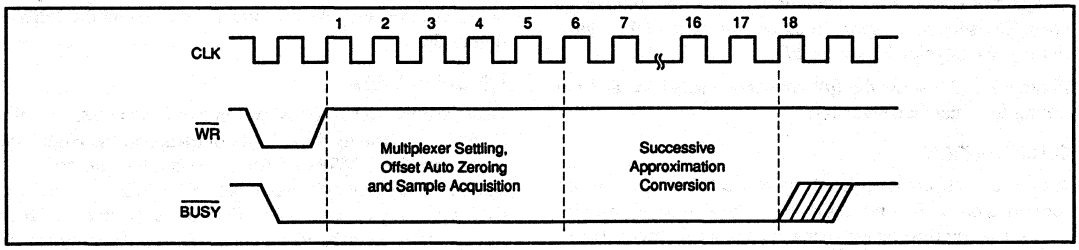


FIGURE 2. Converter Timing.

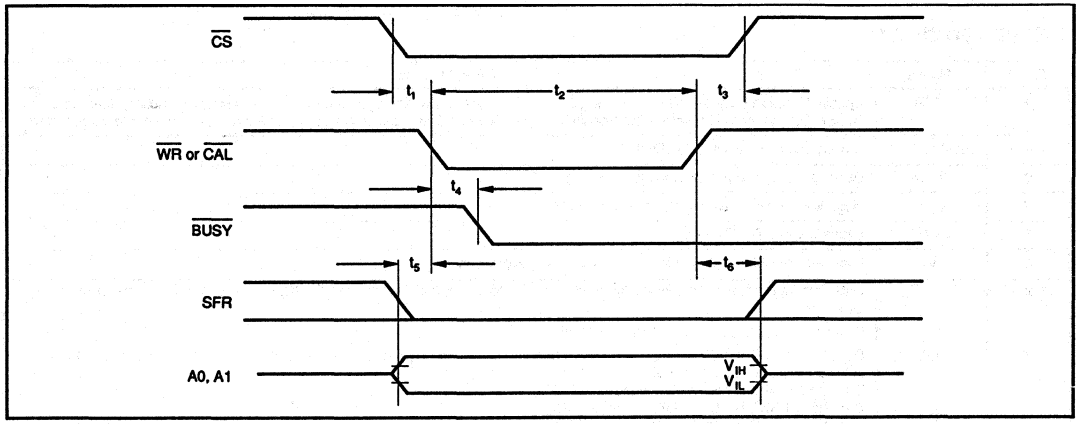


FIGURE 3. Write Cycle Timing (for initiating conversion or calibration).

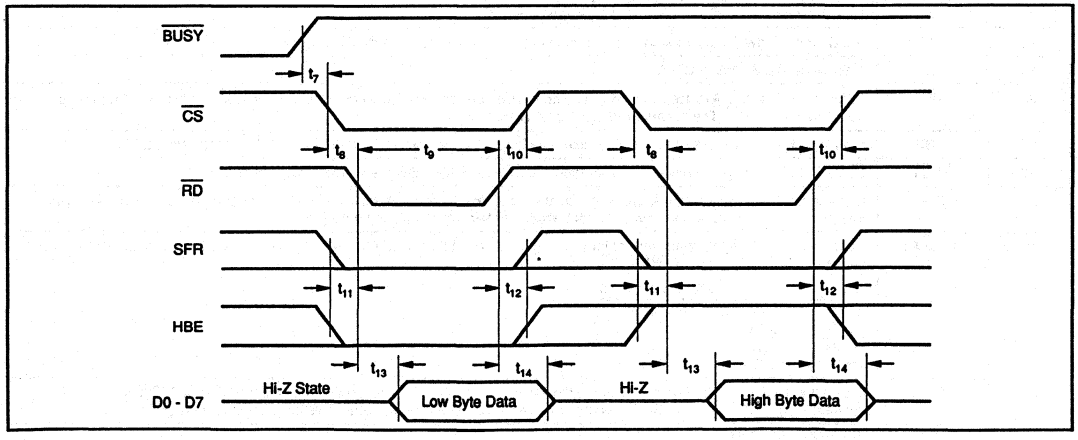


FIGURE 4. Read Cycle Timing.

sions.) The complete 12-bit data is available after $\overline{BUSY}$ has gone HIGH, or the internal status flag goes LOW (D7 when HBE is HIGH).

LATCHED OUTPUT MODE

This mode is activated by writing a HIGH to D0 and LOWs to D1 to D7 in the Special Function Register with $\overline{CS}$ and $\overline{WR}$ LOW and SFR and HBE HIGH. (See the discussion of the Special Function Register below.)

In this mode, the data from a conversion is latched into the output buffers only after a conversion is complete, and remains there until the next conversion is completed. The conversion result is valid during the next conversion. This allows the data to be read even after a new conversion is started, for faster system throughput.

TIMING CONSIDERATIONS

Table I and Figures 3 through 8 show the digital timing of ADC7802 under the various operating modes. All of the critical parameters are guaranteed over the full –40°C to +85°C operating range for ease of system design.

SPECIAL FUNCTION REGISTER (SFR)

An internal register is available, either to determine additional data concerning the ADC7802, or to write additional instructions to the converter. Access to the Special Function Register is made by driving SFR HIGH.

Table II shows the data in the Special Function Register that will be transferred to the output bus by driving HBE HIGH (with SFR HIGH) and initiating a read cycle (driving $\overline{RD}$ and $\overline{CS}$ LOW with $\overline{WR}$ HIGH as shown in Figure 4.) The Power Fail flag in the SFR is set when the power supply falls below about 3V. The flag also means that a new calibration has been started, and any data written to the SFR has been lost. Thus, the ADC7802 will again be in the Transparent Mode. Writing a LOW to D5 in the SFR resets the Power Fail flag. The Cal Error flag in the SFR is set when an overflow occurs during calibration, which may happen in very noisy systems. It is reset by starting a calibration, and remains low after a calibration without an overflow is completed.

SYMBOL	PARAMETER [1]	MIN	TYP	MAX	UNITS
t_1	$\overline{CS}$ to $\overline{WR}$ Setup Time [2]	0	0	0	ns
t_2	$\overline{WR}$ or $\overline{CAL}$ Pulse Width	100			ns
t_3	$\overline{CS}$ to $\overline{WR}$ Hold Time [2]	0	0	0	ns
t_4	$\overline{WR}$ to $\overline{BUSY}$ Propagation Delay	20	50	150	ns
t_5	A0, A1, HBE, SFR Valid to $\overline{WR}$ Setup Time	0			ns
t_6	A0, A1, HBE, SFR Valid to $\overline{WR}$ Hold Time	20			ns
t_7	$\overline{BUSY}$ to $\overline{CS}$ Setup Time	0			ns
t_8	$\overline{CS}$ to $\overline{RD}$ Setup Time [2]	0	0	0	ns
t_9	$\overline{RD}$ Pulse Width	100			ns
t_{10}	$\overline{CS}$ to $\overline{RD}$ Hold Time [2]	0	0	0	ns
t_{11}	HBE, SFR to $\overline{RD}$ Setup Time	50			ns
t_{12}	HBE, SFR to $\overline{RD}$ Hold Time	0			ns
t_{13}	$\overline{RD}$ to Valid Data (Bus Access Time) [3]		80	150	ns
t_{14}	$\overline{RD}$ to Hi-Z Delay (Bus Release Time) [3]		90	180	ns
t_{15}	$\overline{RD}$ to Hi-Z Delay For SFR [3]	20		60	ns
t_{16}	Data Valid to $\overline{WR}$ Setup Time	100			ns
t_{17}	Data Valid to $\overline{WR}$ Hold Time	20			ns

NOTES: (1) All input control signals are specified with $t_{RISE} = t_{FALL} = 20ns$ (10% to 90% of 5V) and timed from a voltage level of 1.6V. Data is timed from V_{IH}, V_{IL}, V_{OH} or V_{OL}. (2) The internal RD pulse is performed by a NOR wiring of $\overline{CS}$ and $\overline{RD}$. The internal WR pulse is performed by a NOR wiring of $\overline{CS}$ and $\overline{WR}$. (3) Figures 7 and 8 show the measurement circuits and pulse diagrams for testing transitions to and from Hi-Z states.

TABLE I. Timing Specifications (CLK = 1MHz external, T_A = –40°C to +85°C).

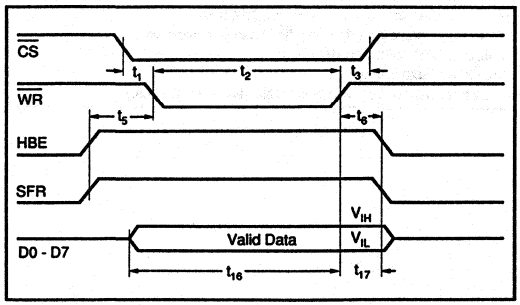


FIGURE 5. Writing to the SFR.

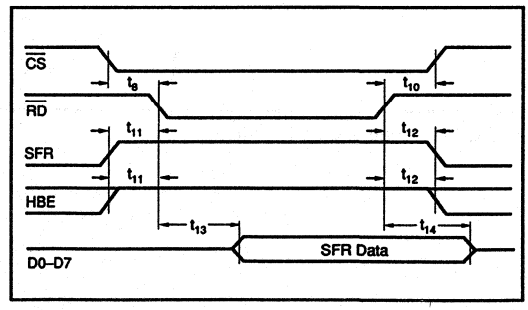


FIGURE 6. Reading the SFR.

Writing a HIGH to D3 in the FSR puts the ADC7802 in the Power Down Mode. Power consumption is reduced to 50µW and D3 remains HIGH. To exit Power Down Mode, either write a LOW to D3 in the SFR, or initiate a calibration by sending a LOW to the $\overline{CAL}$ pin or writing a HIGH to D1. During Power Down Mode, a pulse on $\overline{CS}$ and $\overline{WR}$ will initiate a single conversion, then the ADC7802 will revert to power down.

Table III shows how instructions can be transferred to the Special Function Register by driving HBE HIGH (with SFR HIGH) and initiating a write cycle (driving $\overline{WR}$ and $\overline{CS}$ LOW with $\overline{RD}$ HIGH.) The timing is shown in Figure 3. Note that writing to the SFR also initiates a new conversion.

CONTROL LINES

Table IV shows the functions of the various control lines on the ADC7802. The use of standard $\overline{CS}$, $\overline{RD}$ and $\overline{WR}$ control signals simplifies use with most microprocessors. At the same time, flexibility is assured by availability of status information and control functions, both through the SFR and directly on pins.

INSTALLATION

INPUT BANDWIDTH

From the typical performance curves, it is clear that ADC7802 can accurately digitize signals up to 500Hz, but distortion will increase beyond this point. Input signals slewing faster than 8mV/µs can degrade accuracy. This is a result of the high-precision auto-zeroing circuit used during the acquisition phase. For applications requiring higher signal bandwidth, any good external sample/hold, like the SHC5320, can be used.

INPUT IMPEDANCE

ADC7802 has a very high input impedance (input bias current over temperature is 100nA max), and a low 50pF

PIN	FUNCTION	DESCRIPTION
D0	Mode Status	If LOW, Transparent Mode enabled for data latches. If HIGH, Latched Output Mode enabled.
D1	CAL Flag	If HIGH, calibration cycle in progress.
D2		Reserved for factory use.
D3	Power Down Status	If HIGH, in Power Down Mode.
D4		Reserved for factory use.
D5	POWER FAIL Flag	If HIGH, a power supply failure has occurred. (Supply fell below 3V.)
D6	CAL ERROR Flag	If HIGH, an overflow occured during calibration.
D7	BUSY Flag	If HIGH, conversion or calibration in progress.

NOTE: These data are tranferred to the bus when a read cycle is initiated with SFR and HBE HIGH. Reading the SFR with SFR HIGH and HBE LOW is reserved for factory use at this time, and will yield unpredictable data.

TABLE II. Reading the Special Function Register.

	$\overline{CS}$/$\overline{WR}$	SFR/HBE	D0	D1	D3	D5	D7	D2/D4/D6
Enables Transparent Mode for Data Latches.	LOW	HIGH	LOW	X	LOW	X	LOW	LOW
Enables Latched Output Mode for Data Latches.	LOW	HIGH	HIGH	X	LOW	X	LOW	LOW
Initiates Calibration Cycle.	LOW	HIGH	X	HIGH	LOW	X	LOW	LOW
Resets Power Fail Flag.	LOW	HIGH	X	X	LOW	LOW	LOW	LOW
Activates Power Down Mode	LOW	HIGH	X	X	HIGH	X	LOW	LOW

NOTES: (1) In Power Down Mode, a pulse on $\overline{CS}$ and $\overline{WR}$ will initiate a single conversion, then the ADC7802 will revert to power down. (2) X means it can be either HIGH or LOW without affecting this action. Writing HIGH to D2, D3, D4 or D6, or writing with SFR HIGH and HBE LOW, may result in unpredictable behavior. These modes are reserved for factory use at this time.

TABLE III. Writing to the Special Function Register.

$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	SFR	HBE	$\overline{CAL}$	$\overline{BUSY}$	OPERATION
X	X	X	X	X	0↑1	X	Initiates calibration cycle.
X	X	X	X	X	X	0	Conversion or calibration in process. Inhibits new conversion from starting.
1	X	X	X	X	1	X	None. Outputs in HI-Z State.
0	1	0↑1	0	X	1	1	Initiates conversion.
0	0	1	0	0	1	X	Low byte conversion results output on data bus.
0	0	1	0	1	1	X	High byte conversion results output on data bus.
0	1	0	1	1	1	1	Write to SFR and rising edge on $\overline{WR}$ initiates conversion.
0	0	1	1	1	1	X	Contents of SFR output on data bus.
0	1	0	1	0	1	X	Reserved for factory use.
0	0	1	1	0	1	X	Reserved for factory use. (Unpredictable data on data bus.)

TABLE IV. Control Line Functions.

input capacitance. To ensure a conversion accurate to 12 bits, the analog source must be able to charge the 50pF and settle within the first five clock cycles after a conversion is initiated. During this time, the input is also very sensitive to noise at the analog input, since it could be injected into the capacitor array.

In many applications, a simple passive low-pass filter as shown in Figure 9a can be used to improve signal quality. In this case, the source impedance needs to be less than 5kΩ to keep the induced offset errors below 1/2LSB, and to meet the acquisition time of five clock cycles. The values in Figure 9a meet these requirements, and will maintain the full power bandwidth of the system. For higher source impedances, a buffer like the one in Figure 9b should be used.

INPUT PROTECTION

The input signal range must not exceed $\pm V_{REF}$ or V_A by more than 0.3V.

The analog inputs are internally clamped to V_A. To prevent damage to the ADC7802, the current that can flow into the inputs must be limited to 20mA. One approach is to use an external resistor in series with the input filter resistor. For example, a 1kΩ input resistor allows an overvoltage to 20V without damage.

REFERENCE INPUTS

A 10µF tantalum capacitor is recommended between $V_{REF}+$ and $V_{REF}-$ to insure low source impedance. These capacitors should be located as close as possible to the ADC7802 to reduce dynamic errors, since the reference provides packets of current as the successive approximation steps are carried out.

$V_{REF}+$ must not exceed V_A. Although the accuracy is specified with $V_{REF}+ = 5V$ and $V_{REF}- = 0V$, the converter can function with $V_{REF}+$ as low as 2.5V and $V_{REF}-$ as high as 1V. As long as there is at least a 2.5V difference between $V_{REF}+$ and $V_{REF}-$, the absolute value of errors does not change significantly, so that accuracy will typically be within ±1LSB. (1/2LSB for a 5V span is 610µV, which is 1LSB for a 2.5V span.)

The power supply to the reference source needs to be considered during system design to prevent $V_{REF}+$ from exceeding (or overshooting) V_A, particularly at power-on. Also, after power-on, if the reference is not stable within 42,425 clock cycles, an additional calibration cycle may be needed.

POWER SUPPLIES

The digital and analog power supply lines to the ADC7802 should be bypassed with 10µF tantalum capacitors as close

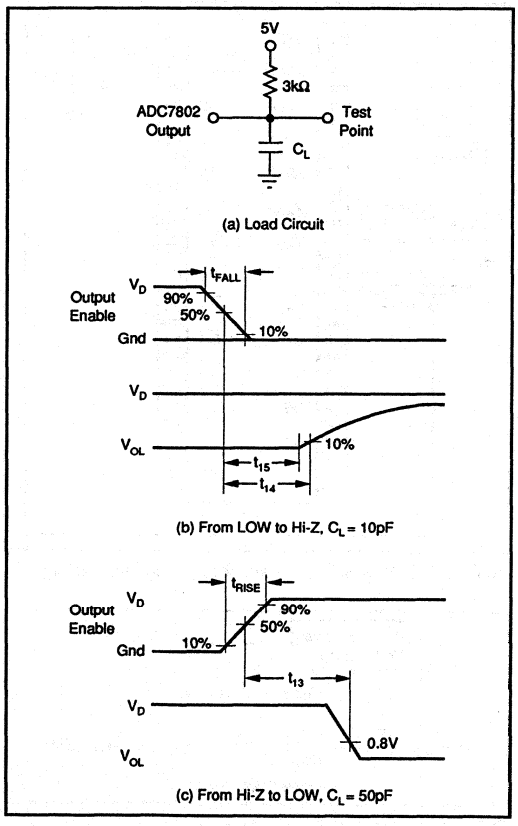


FIGURE 7. Measuring Active LOW to/from Hi-Z State.

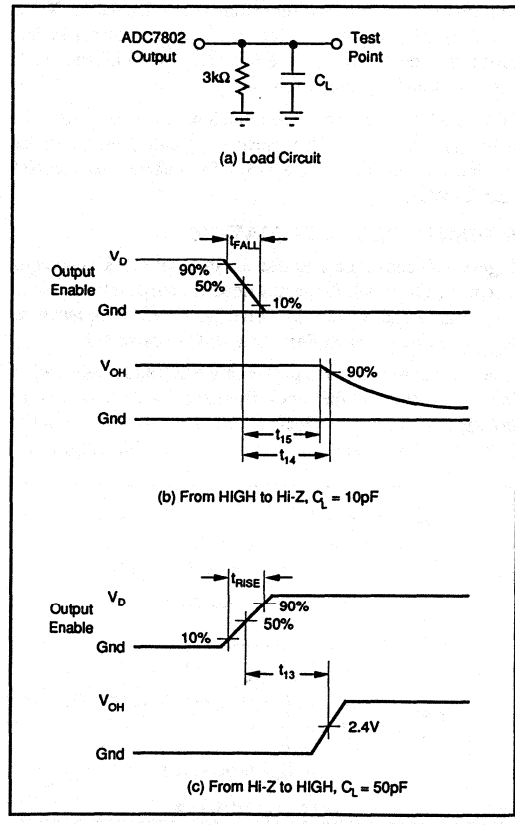


FIGURE 8. Measuring Active HIGH to/from Hi-Z State.

to the part as possible. Although ADC7802 has excellent power supply rejection, even for higher frequencies, linear regulated power supplies are recommended.

Care should be taken to insure that V_D does not come up before V_A, or permanent damage to the part may occur. Figure 10 shows a good supply approach, powering both V_A and V_D from a clean linear supply, with the 10Ω resistor between V_A and V_D insuring that V_D comes up after V_A. This is also a good method to further isolate the ADC7802 from digital supplies in a system with significant switching currents that could degrade the accuracy of conversions.

GROUNDING

To maximize accuracy of the ADC7802, the analog and digital grounds are not connected internally. These points should have very low impedance to avoid digital noise feeding back into the analog ground. The $V_{REF}-$ pin is used as the reference point for input signals, so it should be connected directly to AGND to reduce potential noise problems.

EXTERNAL CLOCK OPERATION

The circuitry required to drive the ADC7802 clock from an external source is shown in Figure 11a. The external clock must provide a 0.8V max for LOW and a 3.5V min for HIGH, with rise and fall times that do not exceed 200ns. The minimum pulse width of the external clock must be 300ns. Synchronizing the conversion clock to an external system clock is recommended in microprocessor applications to prevent beat-frequency problems.

Note that the electrical specification tables are based on using an external 2MHz clock. Typically, the specified accuracy is maintained for clock frequencies between 0.5 and 2.4MHz.

INTERNAL CLOCK OPERATION

Figure 11b shows how to use the internal clock generating circuitry. The clock frequency depends only on the value of the resistor, as shown in "Internal Clock Frequency vs R_{CLOCK}" in the Typical Performance Curves section.

The clock generator can operate between 100kHz and 2MHz. With R = 100kΩ, the clock frequency will nominally be 800kHz. The internal clock oscillators may vary by up to 20% from device to device, and will vary with temperature, as shown in the typical performance curves. Therefore, use of an external clock source is preferred in many applications where control of the conversion timing is critical, or where multiple converters need to be synchronized.

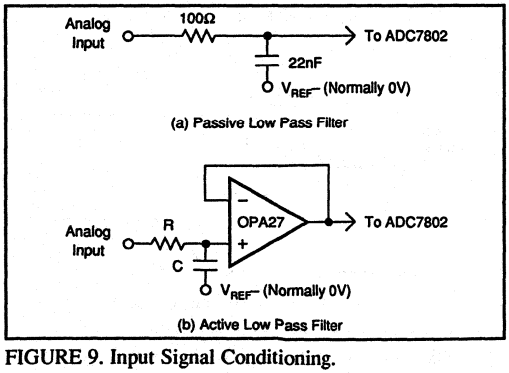


FIGURE 9. Input Signal Conditioning.

APPLICATIONS

BIPOLAR INPUT RANGES

Figure 12 shows a circuit to accurately and simply convert a bipolar ±5V input signal into a unipolar 0 to 5V signal for conversion by the ADC7802, using a precision, low-cost complete difference amplifier, INA105.

Figure 13 shows a circuit to convert a bipolar ±10V input signal into a unipolar 0 to 5V signal for conversion by the ADC7802. The precision of this circuit will depend on the matching and tracking of the three resistors used.

To trim this circuit for full 12-bit precision, R2 and R3 need to be adjustable over appropriate ranges. To trim, first have the ADC7802 converting continually and apply +9.9927V (+10V – 1.5LSB) at the input. Adjust R3 until the ADC7802 output toggles between the codes FFE hex and FFF hex. This makes R3 extremely close to R1. Then, apply –9.9976V (–10V + 0.5LSB) at the input, and adjust R2 until the ADC7802

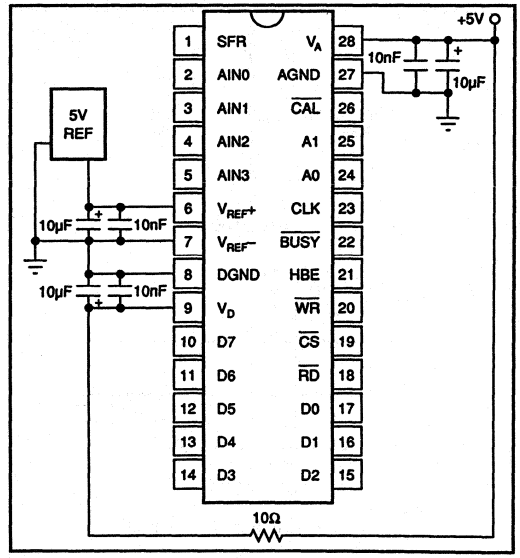


FIGURE 10. Power Supply and Reference Decoupling.

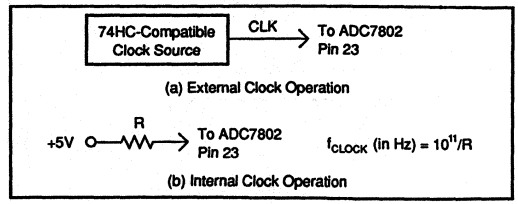


FIGURE 11. Internal Clock Operation.

output toggles between 000 hex and 001 hex. At each trim point, the current through the third resistor will be almost zero, so that one trim iteration will be enough in most cases. More iterations may be required if the op amp selected has large offset voltage or bias currents, or if the +5V reference is not precise.

This circuit can also be used to adjust gain and offset errors due to the components preceding the ADC7802, to match the performance of the self-calibration provided by the converter.

INTERFACING TO MOTOROLA MICROPROCESSORS

Figure 14 shows a typical interface to Motorola microprocessors, while Figure 15 shows how the result can be placed in register D0.

Conversion is initiated by a write instruction decoded by the address decoder logic, with the lower two bits of the address bus selecting an ADC input channel, as follows:

MOVE.W D0, ADC-ADDRESS

The result of the conversion is read from the data bus by a read instruction to ADC-ADDRESS as follows:

MOVEP.W $000 (ADC-ADDRESS), D0

This puts the 12-bit conversion result in the DO register, as shown in Figure 15. The address decoder must pull down $\overline{\text{ADC\_CS}}$ at ADC-ADDRESS to access the Low byte and ADC-ADDRESS +2 to access the High byte.

INTERFACING TO INTEL MICROPROCESSORS

Figure 16 shows a typical interface to Intel.

A conversion is initiated by a write instruction to address $\overline{\text{ADC\_CS}}$. Data pins DO0 and DO1 select the analog input channel. The $\overline{\text{BUSY}}$ signal can be used to generate a microprocessor interrupt (INT) when the conversion is completed.

A read instruction from the $\overline{\text{ADC\_CS}}$ address fetches the Low byte, and a read instruction from the $\overline{\text{ADC\_CS}}$ address +2 fetches the High byte.

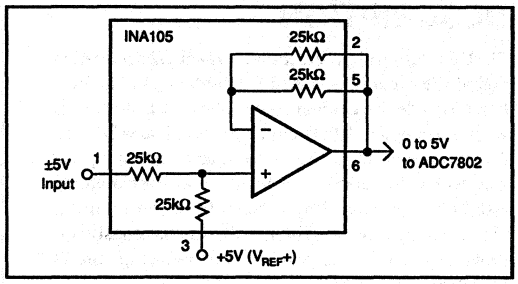


FIGURE 12. ±5V Input Range.

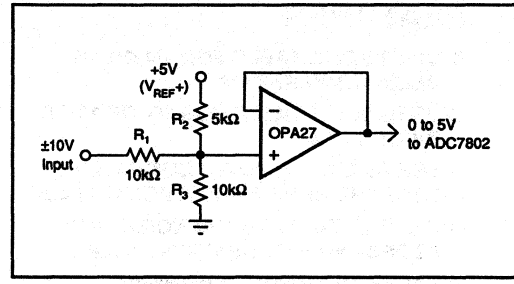


FIGURE 13. ±10V Input Range.

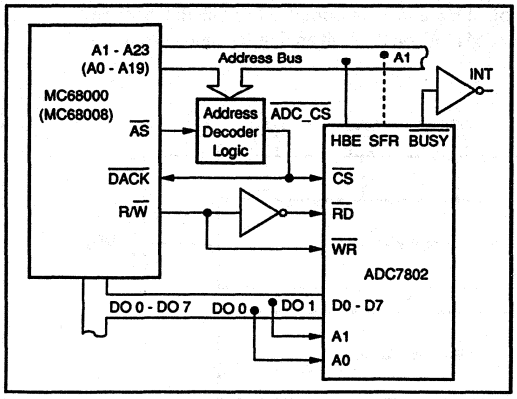


FIGURE 14. Interface to Motorola Microprocessors.

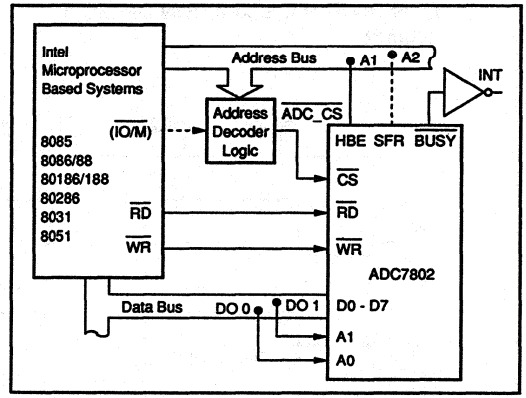


FIGURE 16. Interface to Intel Microprocessors.

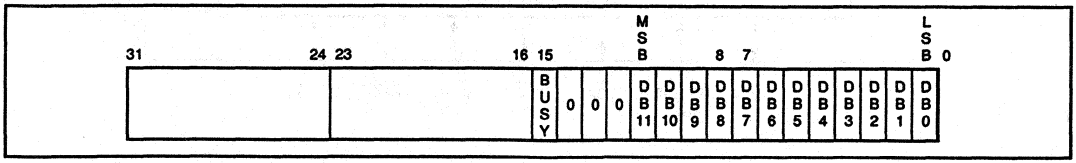
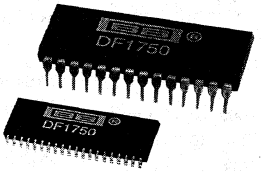


FIGURE 15. Conversion Results in Motorola Register D0.

BURR-BROWN®



DF1750

Dual Channel DIGITAL DECIMATION FILTER

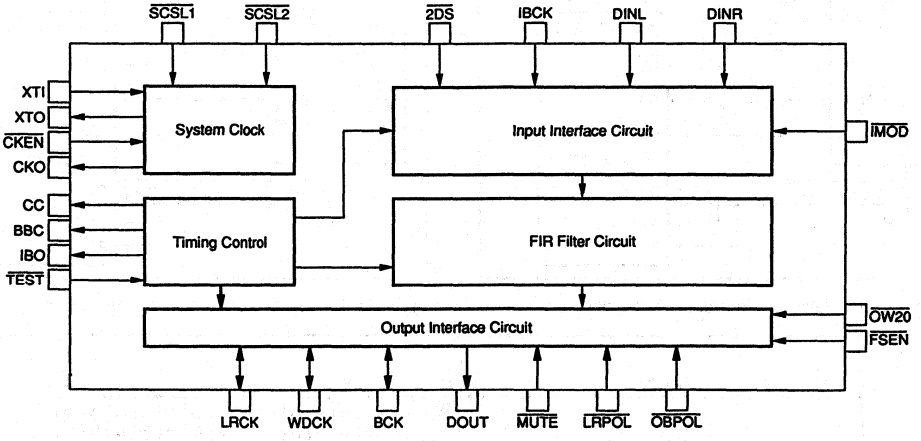
FEATURES

- **USER SELECTABLE FOR 1/4 OR 1/2 DECIMATING RATIOS**
- **USER SELECTABLE FOR 16- OR 18-BIT INPUT DATA**
- **SERIAL DATA INPUT IS COMPATIBLE WITH THE BURR-BROWN PCM1750 ADC**
- **FILTERS OUT-OF-BAND NOISE WITH STOPBAND ATTENUATION > 95dB**
- **PASSBAND RIPPLE < 0.0005dB**
- **SINGLE +5V SUPPLY OPERATION WITH LOW POWER DISSIPATION OF ONLY 250mW**

DESCRIPTION

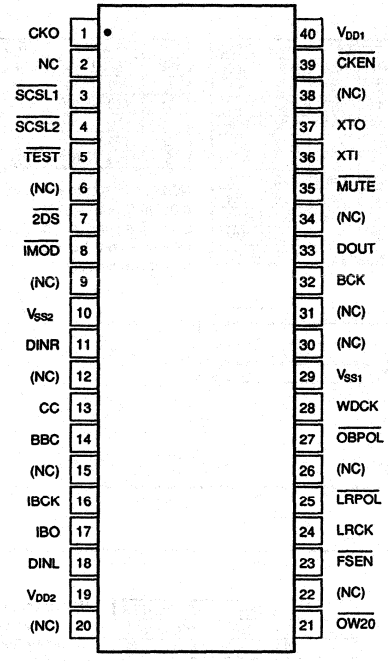
The DF1750 is a high performance 1/4 or 1/2 decimating digital filter that is designed for digital audio applications. This device decimates and filters 2X or 4X (2fs or 4fs) oversampled data from the output of an ADC to a data frequency of fs. The technique of oversampling and decimating allows the input to an oversampling ADC to be processed by a much lower order, linear phase, analog low-pass filter. This simultaneously improves system performance while reducing circuit complexity and cost.

The DF1750 provides output data word rates (fs) up to 50.5kHz and it is compatible with the Burr-Brown PCM1750, dual 18-bit analog-to-digital converter.

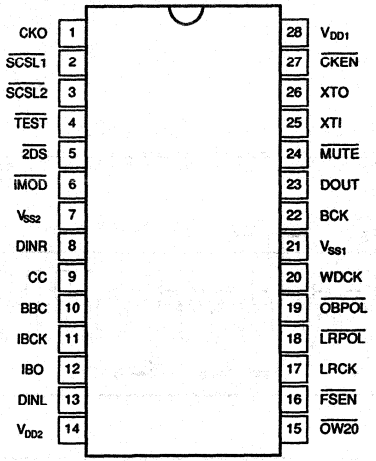


International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

PIN CONFIGURATION



40-Pin SOIC (Top View)



28-Pin Plastic DIP (Top View)

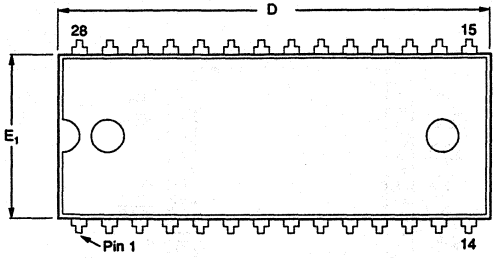
PIN DESCRIPTION

PIN NO.					PIN NO.				
DIP	SOIC	NAME	I/O*	DESCRIPTION	DIP	SOIC	NAME	I/O*	DESCRIPTION
1	1	CKO	o	Clock output (the same as XTI frequency), CKO = L when $\overline{CKEN}$ = H	15	21	$\overline{OW20}$	ip	Output data bit select (16bit: $\overline{OW20}$ = H, 20 bit: $\overline{OW20}$ = L)
–	2	(NC)			–	22	(NC)		
2	3	$\overline{SCSL1}$	ip	XTI Frequency select	16	23	$\overline{FSEN}$	ip	I/O pin select ($\overline{FSEN}$ = H: BCK, WDCK, LRCK pin = Input ($\overline{FSEN}$ = L: BCK, WDCK, LRCK pin = Output)
3	4	$\overline{SCSL2}$	ip	(Refer to XTI pin description)	17	24	LRCK	ip	fs clock
4	5	$\overline{TEST}$	ip	Test, (Test = L; test mode)	18	25	$\overline{LRPOL}$	ip	LRCK polarity select ($\overline{LRPOL}$ = H: Lch/Rch=Low/High) ($\overline{LRPOL}$ = L: Lch/Rch=High/Low)
–	6	(NC)			–	26	(NC)		
5	7	2DS	ip	1/4 or 1/2 decimating select $\overline{2DS}$ = H: 1/4 decimating,					
			ip	$\overline{2DS}$ = L: 1/2 decimating	19	27	$\overline{OBPOL}$	ip	BCK polarity select
6	8	$\overline{IMOD}$	ip	A/D converter interface mode select	20	28	WDCK	ip/o	2fs clock
–	9	(NC)			21	29	VSS1	–	GND 1
7	10	VSS2	–	GND 2	–	30	(NC)		
8	11	DINR	ip	Rch input data	–	31	(NC)		
–	12	(NC)			22	32	BCK	ip/o	Output data bit clock
9	13	CC	o	A/D converter control signal	23	33	DOUT	o	Data output (Lch or Rch serial data output).
10	14	BBC	o	A/D converter control signal	–	34	(NC)		
–	15	(NC)			24	35	$\overline{MUTE}$	ip	Data output mute, ($\overline{MUTE}$ = L: DOUT = L)
					25	36	XTI	i	Oscillator Input (512fs: $\overline{SCSL1}$ = H, $\overline{SCSL2}$ = H) (256fs: $\overline{SCSL1}$ = H, $\overline{SCSL2}$ = L) (768fs: $\overline{SCSL1}$ = L, $\overline{SCSL2}$ = H) (384fs: $\overline{SCSL1}$ = L, $\overline{SCSL2}$ = L)
11	16	IBCK	ip	Input data bit clock input					
12	17	IBO	o	Input data bit clock output	26	37	XTO	o	Oscillator Output
13	18	DINL	ip	Lch input data	–	38	(NC)		
14	19	VDD2	–	+5V	27	39	$\overline{CKEN}$	ip	CKO output select, ($\overline{CKEN}$ = H, CKO = L)
–	20	(NC)			28	40	VDD1	–	+5V

*I = Input pin ip = Input with pull-up resistor o = Output pin ip/o = Input with pull-up resistor when $\overline{FSEN}$ = H, output with $\overline{FSEN}$ = L.

MECHANICAL

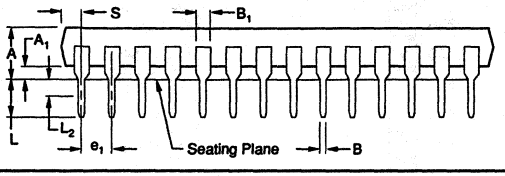
P Package — 28-Pin Plastic DIP

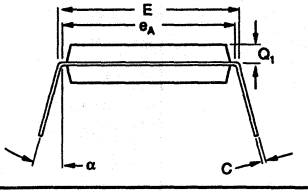


DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.165	.224	4.2	5.7
A1	.015	.070	0.38	1.78
B	.015	.023	0.38	0.58
B1	.015	.055	0.38	1.40
C	.008	.015	0.20	0.38
D	1.402	1.480	35.6	37.6
E	.590	.606	15.0	15.4
E1	.528	.575	13.4	14.6
e1	.088	.112	2.24	2.84
eA	.600 BASIC		15.24 BASIC	

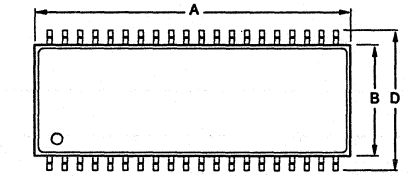
DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
L	.100	.134	2.54	3.4
L2	.000	.030	0.00	0.76
α	0°	15°	0°	15°
Q1	.020	.070	0.51	1.78
S	.040	.080	1.02	2.03

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.





U Package — 40-Pin Plastic SOIC



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.036	1.059	26.30	26.90
B	.362	.378	9.20	9.60
C	.099	.107	2.50	2.70
D	.453	.476	11.50	12.10
E	.042	.058	1.07	1.47
F	.012	.020	0.30	0.50
G	.043	.051	1.10	1.30

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{DD})	−0.3V to +7.0V
Input Voltage (V_{IN})	−0.3V to V_{DD} + 0.3V
Soldering Temperature	+255°C
Soldering Time	10s
Storage Temperature	−40°C to +125°C

ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

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DC SPECIFICATIONS

ELECTRICAL

V_{DD} = 4.5V to 5.5V, V_{SS} = 0V, T_A = –20°C to +80°C unless otherwise specified.

PARAMETER	PIN	SYMBOL	CONDITION	DF1750P/U MIN	DF1750P/U TYP	DF1750P/U MAX	UNIT
INPUTS							
Logic Family					CMOS		
Logic Voltages	XTI	V_{IL1}	For Clock Input			$0.3V_{DD}$	V
	XTI	V_{IH1}	For Clock Input	$0.7V_{DD}$			V
	XTI	V_{CLK}	For AC Coupling	1.8			V_{P-P}
	(1),(2)	V_{IL2}	$\overline{FSEN}$ = H			0.5	V
	(1),(2)	V_{IH2}	$\overline{FSEN}$ = H	2.4			V
Logic Currents	XTI	I_{IL1}	V_{IN} = 0V		5	10	µA
	XTI	I_{IH1}	V_{IN} = V_{DD}		5	10	µA
	(1),(2)	I_{IL2}	V_{IN} = 0V, $\overline{FSEN}$ = H		10	20	µA
Input Leakage Current	(1),(2)	I_{LH1}	V_{IN} = V_{DD}, $\overline{FSEN}$ = H			1.0	µA
OUTPUTS							
Logic Family					CMOS		
Logic Voltages	(2),(3)	V_{OL}	I_{OL} = 1.6mA, $\overline{FSEN}$ = L			0.4	V
	(2),(3)	V_{OH}	I_{OH} = –0.4mA, $\overline{FSEN}$ = L	2.5			
POWER SUPPLY REQUIREMENTS							
Supply Voltage		V_{DD1}, V_{DD2}			+5		V
Supply Current		I_{DD}	V_{DD} = 5V(4), $\overline{FSEN}$ = H			30	mA
Power Dissipation		P_D	Nominal V_{DD}			250	mW
TEMPERATURE RANGE (AMBIENT, T_A)							
Specification				–20		+80	°C
Operating				–20		+80	°C

NOTES: (1) Refers to pins $\overline{SCSL1}$, $\overline{SCSL2}$, $\overline{TEST}$, $\overline{2DS}$, $\overline{IMOD}$, DINR, IBCK, DINL, $\overline{OW20}$, $\overline{MUTE}$, $\overline{OBPOL}$, $\overline{LRPOL}$, $\overline{FSEN}$, $\overline{CKEN}$. (2) Refers to pins BCK, WDCK, LRCK. (3) Refers to pins CKO, CC, BBC, IBO, DOUT. (4) Test Condition; $\overline{SCSL1}$ = H, $\overline{SCSL2}$ = H, $\overline{TEST}$ = H, $\overline{2DS}$ = H, $\overline{IMOD}$ = H, $\overline{OW20}$ = H, $\overline{MUTE}$ = H, $\overline{OBPOL}$ = H, $\overline{LRPOL}$ = H, $\overline{FSEN}$ = L, $\overline{CKEN}$ = L. T_{CY} = 38ns (XTI Clock Period), C_L = 0pF (Capacitive Load), DINL, DINR (Applicable Input Data).

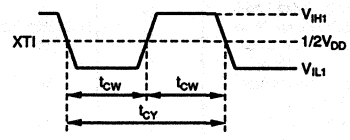
AC SPECIFICATIONS

ELECTRICAL

V_{DD} = 4.5V to 5.5V, V_{SS} = 0V, T_A = –20°C to +80°C unless otherwise specified.

XTI Clock

PARAMETER	SYMBOL	CONDITION $\overline{SCSL1}$	CONDITION $\overline{SCSL2}$	SYS FREQ	DF1750P/U MIN	DF1750P/U TYP	DF1750P/U MAX	UNIT
Crystal Oscillator Frequency	F_{OSC}	H	H	512fs(1)	8		26	MHz
		H	L	256fs	4		13	MHz
		L	H	768fs	12		26	MHz
		L	L	384fs	6		20	MHz
External Clock Pulse Width	t_{CW}	H	H	512fs	15		70	ns
		H	L	256fs	38		140	ns
		L	H	768fs	15		50	ns
		L	L	384fs	25		100	ns
External Clock Pulse Period	t_{CY}	H	H	512fs	38		125	ns
		H	L	256fs	77		250	ns
		L	H	768fs	38		84	ns
		L	L	384fs	50		167	ns

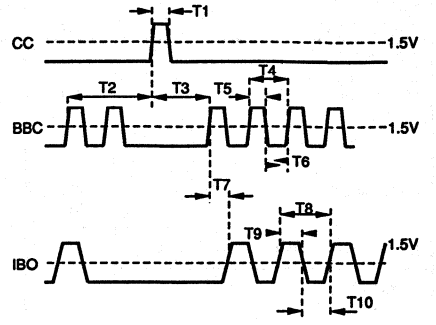


AC Coupling is required with an external clock.

NOTE: (1) fs = Sampling frequency.

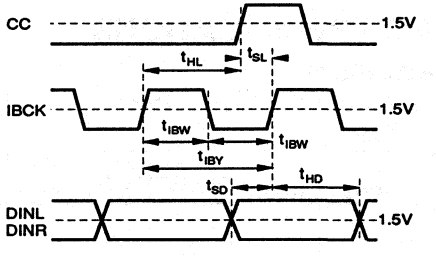
ADC CONTROL SIGNAL TIMING (CC, BBC, AND IBO) WITH $\overline{IMOD}$ = H

PARAMETER	SYMBOL	DF1750P/U MIN	DF1750P/U TYP	DF1750P/U MAX	UNIT
$\overline{2DS}$ = H					
CC Pulse Width (H)	T1	65	1/256fs		ns
S/H Acquisition Time	T2	670	9/256fs		ns
CC-BBC Time	T3	285	4/256fs		ns
BBC Pulse Period	T4	228	3/256fs		ns
BBC Pulse Width (H)	T5	65	1/256fs		ns
BBC Pulse Width (L)	T6	140	2/256fs		ns
BBC-IBO Time	T7	140	2/256fs		ns
IBO Pulse Period	T8	228	3/256fs		ns
IBO Pulse Width (H)	T9	140	2/256fs		ns
IBO Pulse Width (L)	T10	65	1/256fs		ns
$\overline{2DS}$ = L					
CC Pulse Width (H)	T1	130	1/256fs		ns
S/H Acquisition Time	T2	1350	9/256fs		ns
CC-BBC Time	T3	570	4/256fs		ns
BBC Pulse Period	T4	456	3/256fs		ns
BBC Pulse Width (H)	T5	130	1/256fs		ns
BBC Pulse Width (L)	T6	280	2/256fs		ns
BBC-IBO Time	T7	280	2/256fs		ns
IBO Pulse Period	T8	456	3/256fs		ns
IBO Pulse Width (H)	T9	280	2/256fs		ns
IBO Pulse Width (L)	T10	130	1/256fs		ns



SERIAL INPUT TIMING (IBCK, DINL, DINR) WITH $\overline{IMOD}$=H

PARAMETER	SYMBOL	DF1750P/U MIN	DF1750P/U TYP	DF1750P/U MAX	UNIT
$\overline{2DS}$ = H					
IBCK Pulse Width	t_{IBW}	50	1/256fs		ns
IBCK Pulse Period	t_{IBY}	3/12.928MHz[1]	3/256fs		ns
Data Word Latch Set-up Time	t_{SL}	50			ns
Data Word Latch Hold Time	t_{HL}	50			ns
DINL, DINR Set-up Time	t_{SD}	25			ns
DINL, DINR Hold Time	t_{HD}	25			ns
$\overline{2DS}$ = L					
IBCK Pulse Width	t_{IBW}	50	1/128fs		ns
IBCK Pulse Period	t_{IBY}	3/12.928MHz[1]	3/128fs		ns
Data Word Latch Set-up Time	t_{SL}	50			ns
Data Word Latch Hold Time	t_{HL}	50			ns
DINL, DINR Set-up Time	t_{SD}	25			ns
DINL, DINR Hold Time	t_{HD}	25			ns

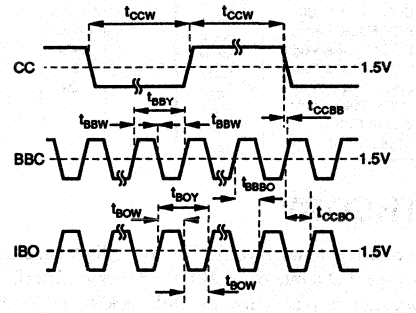


Normally, IBO output is connected to IBCK
(Refer to the applications diagram).

NOTE: (1) 12.928MHz = 256 x 50.5kHz (max sampling frequency).

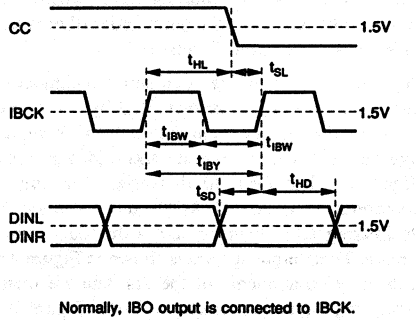
ADC CONTROL SIGNAL TIMING (CC, BBC, AND IBO) WITH $\overline{IMOD}$ = L

PARAMETER	SYMBOL	DF1750P/U MIN	DF1750P/U TYP	DF1750P/U MAX	UNIT
$\overline{2DS}$ = H					
CC Pulse Width (H)	t_{CCW}		1/8fs		ns
BBC Pulse Width	t_{BBW}	130	1/128fs		ns
BBC Pulse Period	t_{BBY}		1/64fs		ns
IBO Pulse Width	t_{BOW}	130	1/128fs		ns
IBO Pulse Period	t_{BOY}		1/64fs		ns
CC-BBC Time	t_{CCBB}	-5	0	20	ns
CC-IBO Time	t_{CCBO}	130	1/128fs		ns
BBC-IBO Time	t_{BBBO}	130	1/128fs		ns
$\overline{2DS}$ = L					
CC Pulse Width (H)	t_{CCW}		1/4fs		ns
BBC Pulse Width	t_{BBW}	280	1/64fs		ns
BBC Pulse Period	t_{BBY}		1/32fs		ns
IBO Pulse Width	t_{BOW}	280	1/64fs		ns
IBO Pulse Period	t_{BOY}		1/32fs		ns
CC-BBC Time	t_{CCBB}	-5	0	20	ns
CC-IBO Time	t_{CCBO}	280	1/64fs		ns
BBC-IBOTime	t_{BBBO}	280	1/64fs		ns



SERIAL INPUT TIMING (IBCK, DINL, DINR) WITH $\overline{IMOD}$ = L

PARAMETER	SYMBOL	DF1750P/U MIN	DF1750P/U TYP	DF1750P/U MAX	UNIT
$\overline{2DS}$ = H					
IBCK Pulse Width	t_{IBW}	100	1/128fs		ns
IBCK Pulse Period	t_{IBY}	1/3.232MHz[1]	1/64fs		ns
Data Word Latch Set-up Time	t_{SL}	50			ns
Data Word Latch Hold Time	t_{HL}	50			ns
DINL, DINR Set-up Time	t_{SD}	25			ns
DINL, DINR Hold Time	t_{HD}	25			ns
$\overline{2DS}$ = L					
IBCK Pulse Width	t_{IBW}	100	1/64fs		ns
IBCK Pulse Period	t_{IBY}	1/3.232MHz[1]	1/32fs		ns
Data Word Latch Set-up Time	t_{SL}	50			ns
Data Word Latch Hold Time	t_{HL}	50			ns
DINL, DINR Set-up Time	t_{SD}	25			ns
DINL, DINR Hold Time	t_{HD}	25			ns

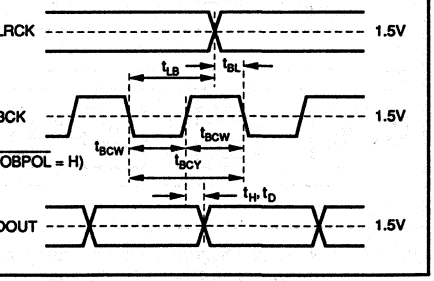


Normally, IBO output is connected to IBCK.
(Refer to the application diagram).

NOTE: (1) 3.232MHz = 64 x 50.5kHz (max sampling frequency).

SERIAL OUTPUT TIMING WITH $\overline{FSEN}$ = H

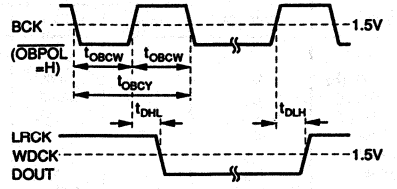
PARAMETER	SYMBOL	DF1750P/U MIN	DF1750P/U TYP	DF1750P/U MAX	UNIT	REMARKS
BCK Pulse Width	t_{BCW}	100	1/128fs		ns	
BCK Pulse Period	t_{BCY}	1/3.232MHz[1]	1/64fs		ns	
LRCK Pulse Width	t_{LCW}		1/2fs		µs	Duty = 50%
LRCK Pulse Period	t_{LCY}	1/50.5kHz	1/fs		µs	
LRCK Set-up Time	t_{BL}	50			ns	
LRCK Hold Time	t_{LB}	50			ns	
Output Data Hold Time	t_H	0			ns	C_L = 0pF
Output Data Delay Time	t_D			100	ns	C_L = 15pF



NOTE: (1) 3.232MHz = 64 x 50.5kHz (max sampling frequency).

SERIAL OUTPUT TIMING WITH $\overline{FSEN}$ = L

PARAMETER	SYMBOL	DF1750P/U MIN	DF1750P/U TYP	DF1750P/U MAX	UNIT
BCK Pulse Width	t_{OBCW}	140	1/128fs		ns
BCK Pulse Period	t_{OBCY}		1/64fs		ns
WDCK Pulse Width	t_{WDCW}		1/4fs		µs
WDCK Pulse Period	t_{WDCY}		1/2fs		µs
LRCK Pulse Width	t_{LRCW}		1/2fs		µs
LRCK Pulse Period	t_{LRCY}		1/fs		µs
Output Data Delay Time	t_{DHL}	–10		30	ns
	t_{DLH}	–10		30	ns



THEORY

According to the Nyquist Theorem, digital audio recordings sampled at a rate of 44.1kHz (CD) or 48kHz (DAT) should accurately reproduce the full 20kHz audio bandwidth. Unfortunately, if frequencies higher than1/2 the sample rate are seen at the input of an analog-to-digital converter, aliasing back into the baseband will occur. At these sample frequencies, the way to assure that aliasing does not occur is to use complicated high order filters at the input of the ADC . These filters can be expensive and they can also have undesirable phase characteristics. These problems can be avoided by using an oversampling ADC (such as the PCM1750) with a decimating filter, where a high order filter can be replaced with a low order filter which has very little phase distortion (Figure 1).

With the oversampling-decimating technique, the input signal (Figure 2a) is band limited by a low order analog low-pass filter as shown in Figure 2b. This signal is 4-times oversampled, with its spectra and foldover noise shown in Figure 2c. The DF1750 first rejects the high frequency components of the 4fs ADC output (Figure 2d). A 1/2 decimating filter then processes this data into a 2fs data stream. This output spectra is shown in Figure 2e. The high frequency components of the 2fs data are then removed, producing the output spectra shown in Figure 2f. A second 1/2 decimating filter processes the 2fs data to a final fs data stream and the original signal is restored without distortion (Figure 2g). Note, when operating in the 1/2 decimating mode the DF1750 processes data through the first LPF and a single 1/2 decimating filter only.

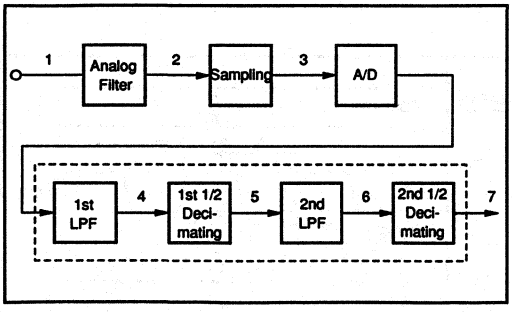


FIGURE 1. A Block Diagram of an Oversampling ADC Followed by Digital Decimation.

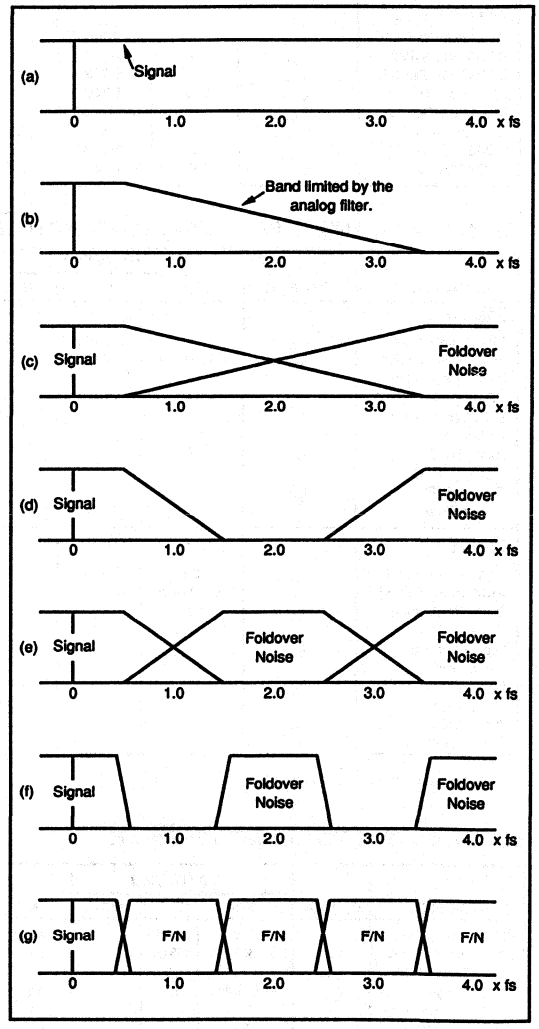
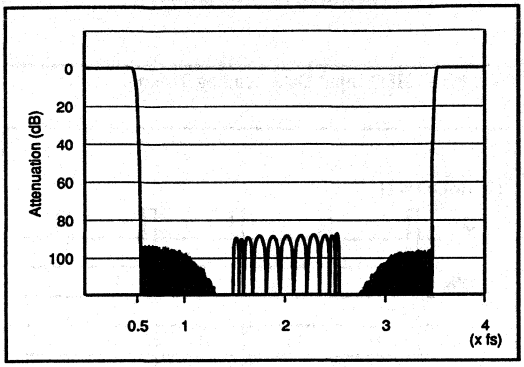


FIGURE 2. The Associated Spectra of the Oversampling-Decimating Technique.

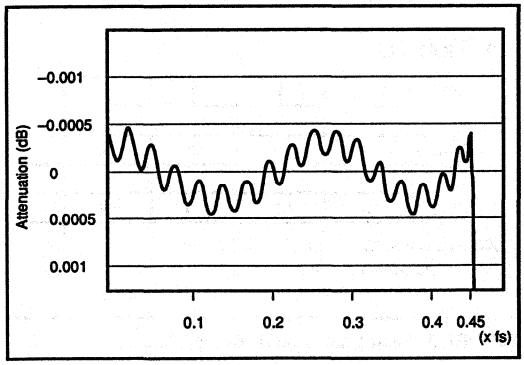
THEORETICAL FILTER CHARACTERISTICS

1/4 DECIMATING, INPUT DATA FREQUENCY = 4fs

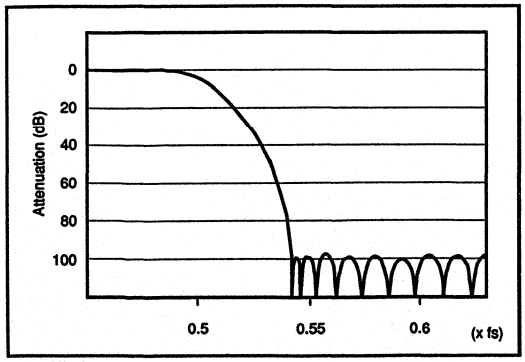
PARAMETER	CHARACTERISTICS
Passband	DC to 0.4583fs
Stopband	0.5417fs and Above
Passband Ripple	±0.0005 dB
Stopband Attenuation	95dB min, 0.5417fs to 1.4583fs 88dB min, 1.4583fs to 2.5417fs 95dB min, 2.5417fs to 3.4583fs
Group Delay Time	Constant, Linear Phase



DF1750 1/4 Decimating Filter Tranfer Characteristics.



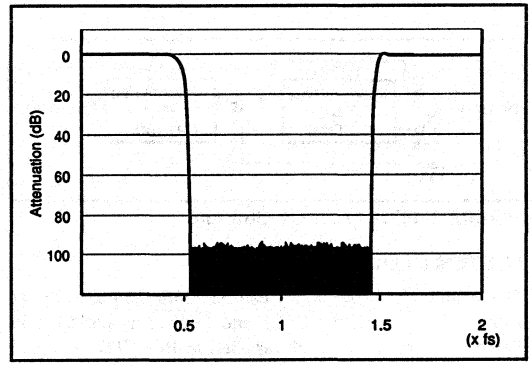
DF1750 1/4 Decimating Passband Frequency Response.



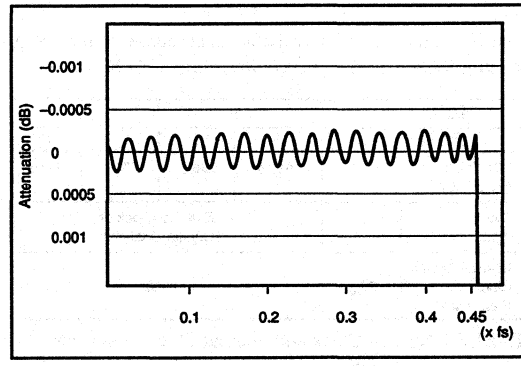
DF1750 1/4 Decimating Transitionband Frequency Response.

1/2 DECIMATING, INPUT DATA FREQUENCY = 2fs

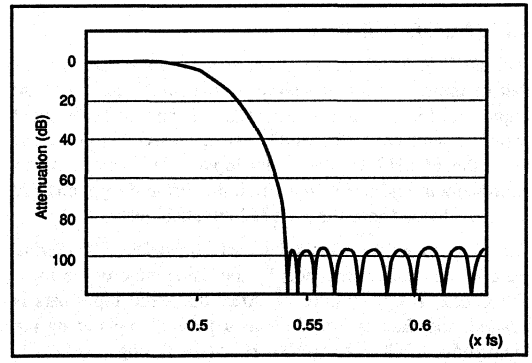
PARAMETER	CHARACTERISTICS
Passband	DC to 0.4583fs
Stopband	0.5417fs and above
Passband Ripple	±0.0002dB
Stopband Attenuation	95dB min, 0.5417fs to 1.4583fs
Group Delay Time	Constant, Linear Phase



DF1750 1/2 Decimating Filter Transfer Characteristics.



DF1750 1/2 Decimating Passband Frequency Response.



DF1750 1/2 Decimating Transitionband Frequency Response.

FUNCTIONAL DESCRIPTION

1/4 AND 1/2 DECIMATING FUNCTIONS

1/4 or 1/2 decimating filtering converts 4fs or 2fs oversampled data back to a sampling rate of fs data by a digital filtering algorithm. $\overline{2DS}$ is used to select 1/4 or 1/2 decimating.

$\overline{2DS}$ = H; 1/4 decimating (0.5417fs ~ 3.4583fs)
$\overline{2DS}$ = L; 1/2 decimating (0.5417fs ~ 1.4583fs)

The filter arithmetic block consists of two 1/2 decimating finite impulse response (FIR) filters as shown in Figure 3.

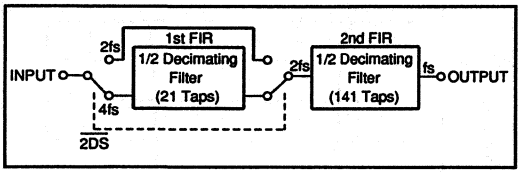


FIGURE 3. Filter Arithmetic Structure

SYSTEM CLOCK

The system clock frequency can be 256fs, 364fs, 512fs, or 768fs selectable with $\overline{SCSL1}$ and $\overline{SCSL2}$ as indicated in Table I. An external clock (applied to Pin XTI) or crystal oscillator (Pins XTI and XTO) can be employed. AC coupling is required for an external clock.

The XTI input clock is available as an output at pin CKO, when $\overline{CKEN}$ = L. CKO stays low when $\overline{CKEN}$ = H.

$\overline{SCSL1}$		H		L	
$\overline{SCSL2}$		H	L	H	L
XTI Clock Frequency	F_{xi}	512fs	256fs	768fs	384fs
Clock Input		External Clock or Crystal Oscillator			
Internal System Clock Frequency	F_{sys}	256fs			

TABLE I. System Clock and Internal Clock Frequency Selection.

SERIAL DATA INPUT

The DF1750 is programmed for accepting the correct number of input data bits per word by the $\overline{IMOD}$ pin. A 16-bit input word is selected with $\overline{IMOD}$ = L and an 18-bit input word is selected with $\overline{IMOD}$ = H. Set $\overline{IMOD}$ = H for use with the PCM1750. The serial input data format is two's complement and MSB first. Both the left and right channel data are loaded into the DF1750 simutaneously.

Each bit of the data is loaded to each channel's SIPO (Serial/parallel conversion register) by the rising edge of the Input Bit Clock, IBCK (Figure 4). After the serial input data is loaded, the data is latched into a parallel register by the rising edge of CC for $\overline{IMOD}$ = H and the falling edge of CC for $\overline{IMOD}$ = L (Figure 5).

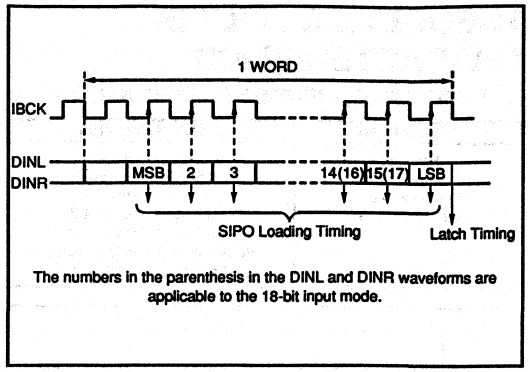


FIGURE 4. SIPO Input Data Loading Timing.

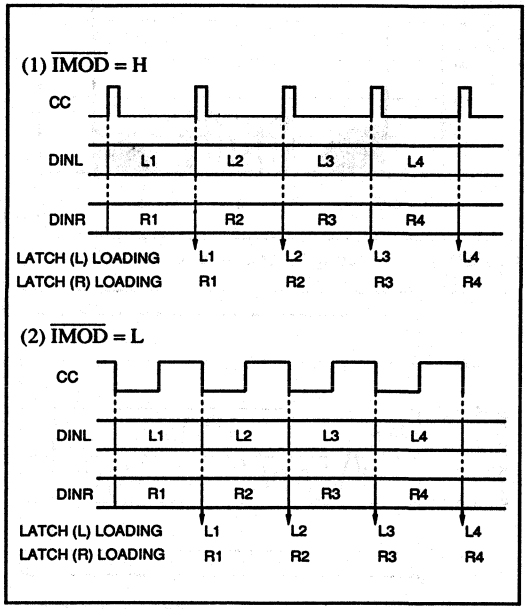


FIGURE 5. Input Data Latch/Loading Timing.

ADC CONTROL SIGNALS (CC, BBC, AND IBO) WITH $\overline{IMOD}$ = H

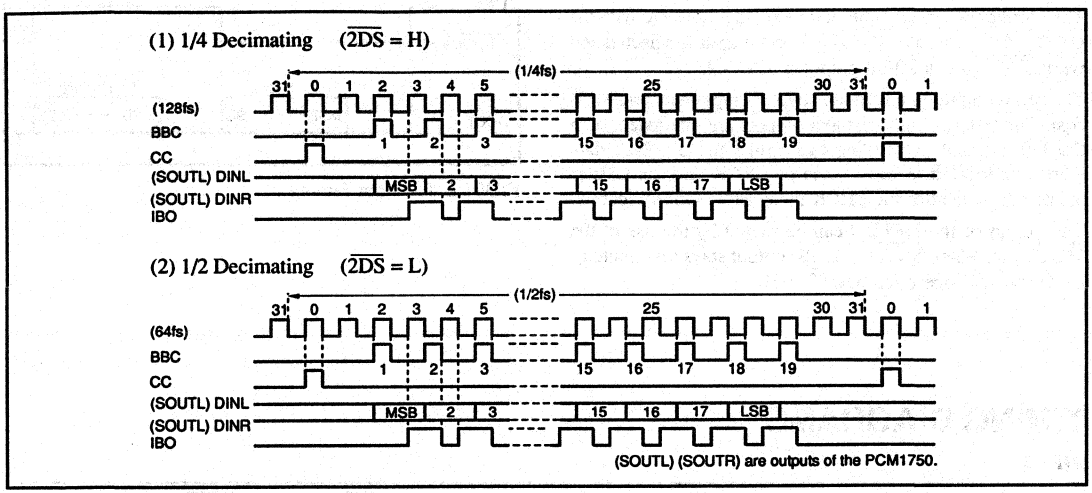


FIGURE 6. ADC Control Signals With $\overline{IMOD}$ = H. (Applicable for use with the Burr-Brown PCM1750 ADC).

ADC CONTROL SIGNALS (CC, BBC AND IBO) WITH $\overline{IMOD}$ = L

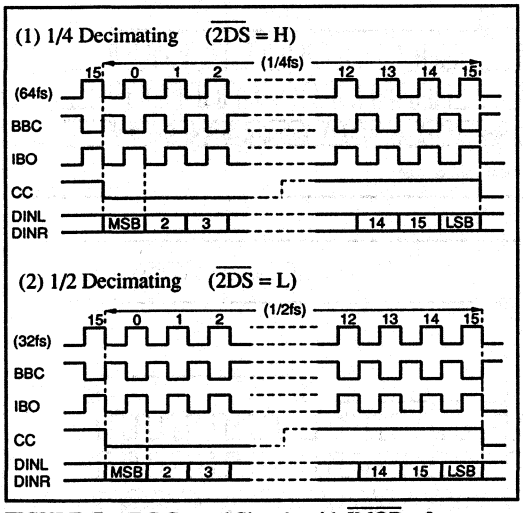


FIGURE 7. ADC Control Signals with $\overline{IMOD}$ = L

OUTPUT INTERFACE (BCK, WDCK, LRCK, $\overline{OBPOL}$, $\overline{LRPOL}$, $\overline{FSEN}$)

The output of the DF1750 can be interfaced to many different devices by programming the output interface pins. These pins provide the following functions:

a. Output control clocks, BCK, WDCK, LRCK I/O selection ($\overline{FSEN}$).
$\overline{FSEN}$ = H; BCK WDCK, LRCK = Input
$\overline{FSEN}$ = L; BCK WDCK, LRCK = Output

b. Sampling rate clock (LRCK)
When $\overline{FSEN}$ = H, apply a 50% duty cycle sampling frequency (fs) to pin LRCK.
When $\overline{FSEN}$ = L, a fs clock generated from the system clock is available at pin LRCK.

c. Word Clock (WDCK)
When $\overline{FSEN}$ = L, WDCK provides a 2fs clock that is derived from the system clock.

d. Output bit clock
When $\overline{FSEN}$ = H, apply a 64fs clock to pin BCK.
When $\overline{FSEN}$ = L, a 64fs clock generated from the system clock is available at pin BCK.

e. LRCK polarity selection ($\overline{LRPDL}$)
$\overline{LRPOL}$ = H; Lch/Rch = Low/High
$\overline{LRPOL}$ = L; Lch/Rch = High/Low
(Regardless of LRCK's I/O mode).

f. BCK polarity selection ($\overline{OBPOL}$)
$\overline{OBPOL}$ = H; DOUT changes state at rising edge of BCK.
$\overline{OBPOL}$ = L; DOUT changes state at falling edge of BCK.
(Regardless of BCK's I/O mode).

g. Timing relation between XTI and BCK, WDCK, LRCK clocks.
When $\overline{FSEN}$ = H, clocks to BCK and LRCK must be synchronized to XTI. However, there is no limit on their phase differences (between XTI and BCK, LRCK clocks).

SERIAL DATA OUTPUT

The number of bits per output data word is selected with the $\overline{OW20}$ pin. With $\overline{OW20}$ = H a 16-bit output is selected and with $\overline{OW20}$ = L a 20-bit output is selected.

The serial output data format is two's complement and MSB first. The left and right channel outputs are alternated, with the left channel preceeding the right channel. Each data word is allocated in each pulse of LRCK and the LSB is located at the end of the LRCK pulse as shown in Figure 8.

The output of the DF1750 can be muted by the use of the $\overline{MUTE}$ pin. When $\overline{MUTE}$ = L, the output stays low (muted). Under normal operation $\overline{MUTE}$ = H.

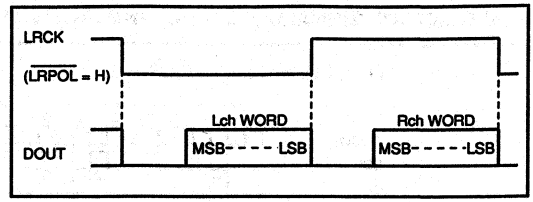
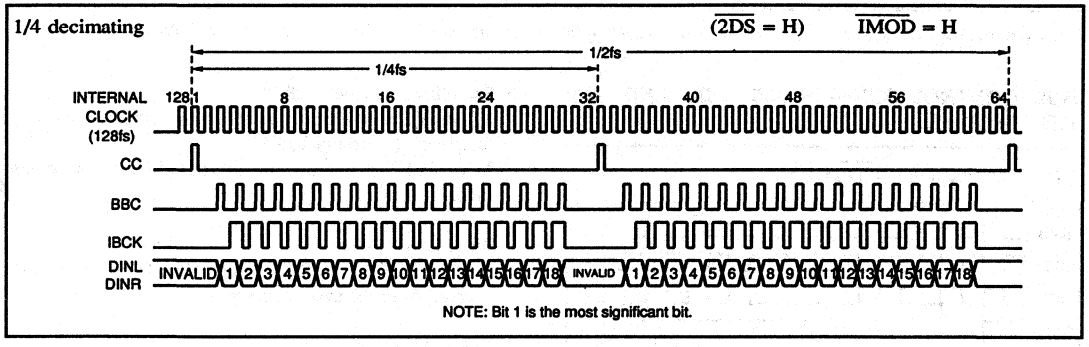
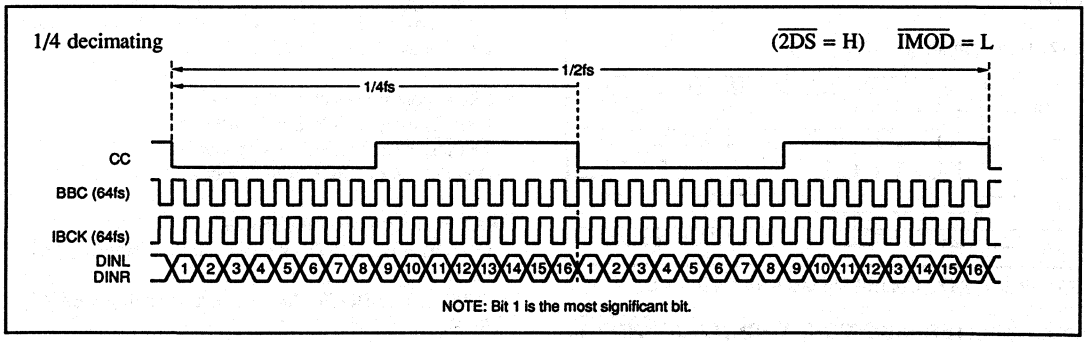


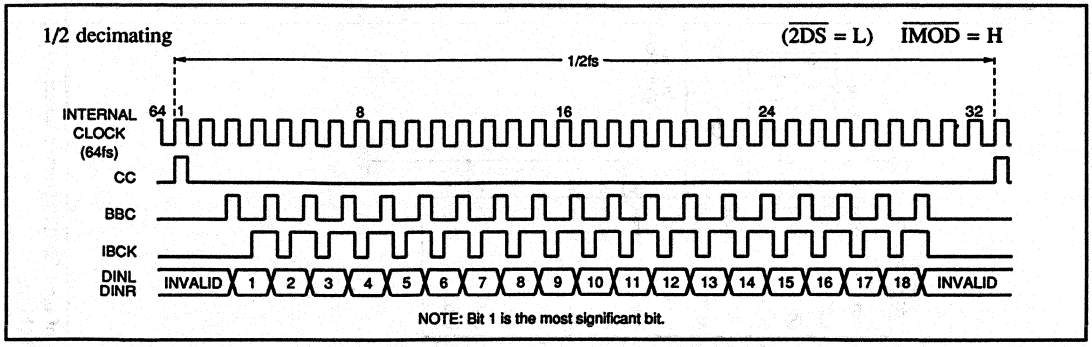
FIGURE 8. Output Timing.

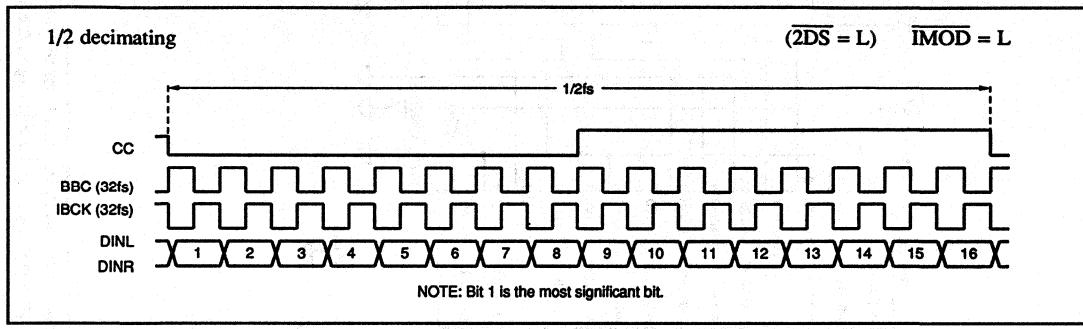
TIMING DIAGRAMS

INPUT

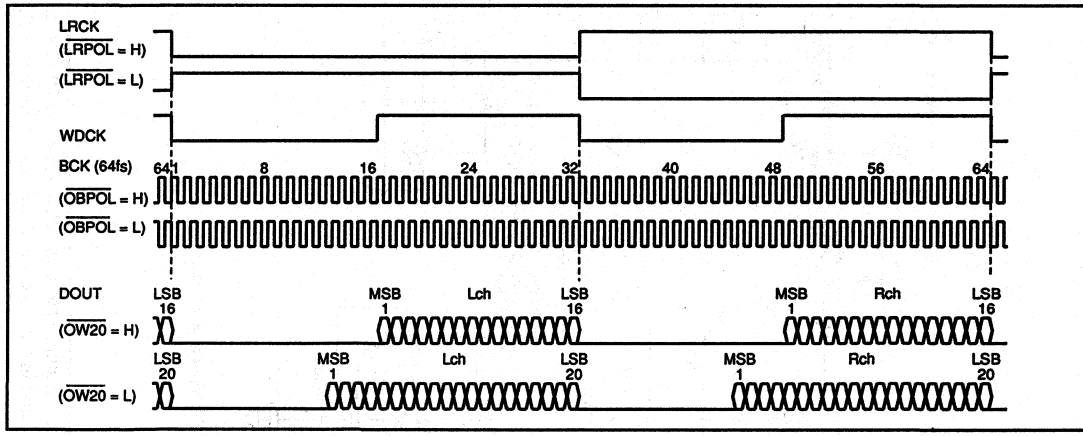








OUTPUT



APPLICATIONS

A typical circuit configuration for digital audio recording is shown in Figure 9. Each of the stereo input channels passes through a six pole Generalized Immitance Converter (GIC) low pass analog filter. This filter features extremely low distortion and negligible phase shift. The band limited signals are 4x oversampled by the dual-channel PCM1750 A/D converter. Clock and convert signals are provided to the PCM1750 by the DF1750. The 4fs oversampled data of the PCM1750 is filtered by the DF1750 to provide a data stream of fs. A PCM1750/DF1750 evaluation board, DEM1133, is available from Burr-Brown. This board incorporates the features mentioned above as well as an AES/EBU interface, test points for monitoring both the serial and parallel data outputs, and a breadboard area for user experimentation.

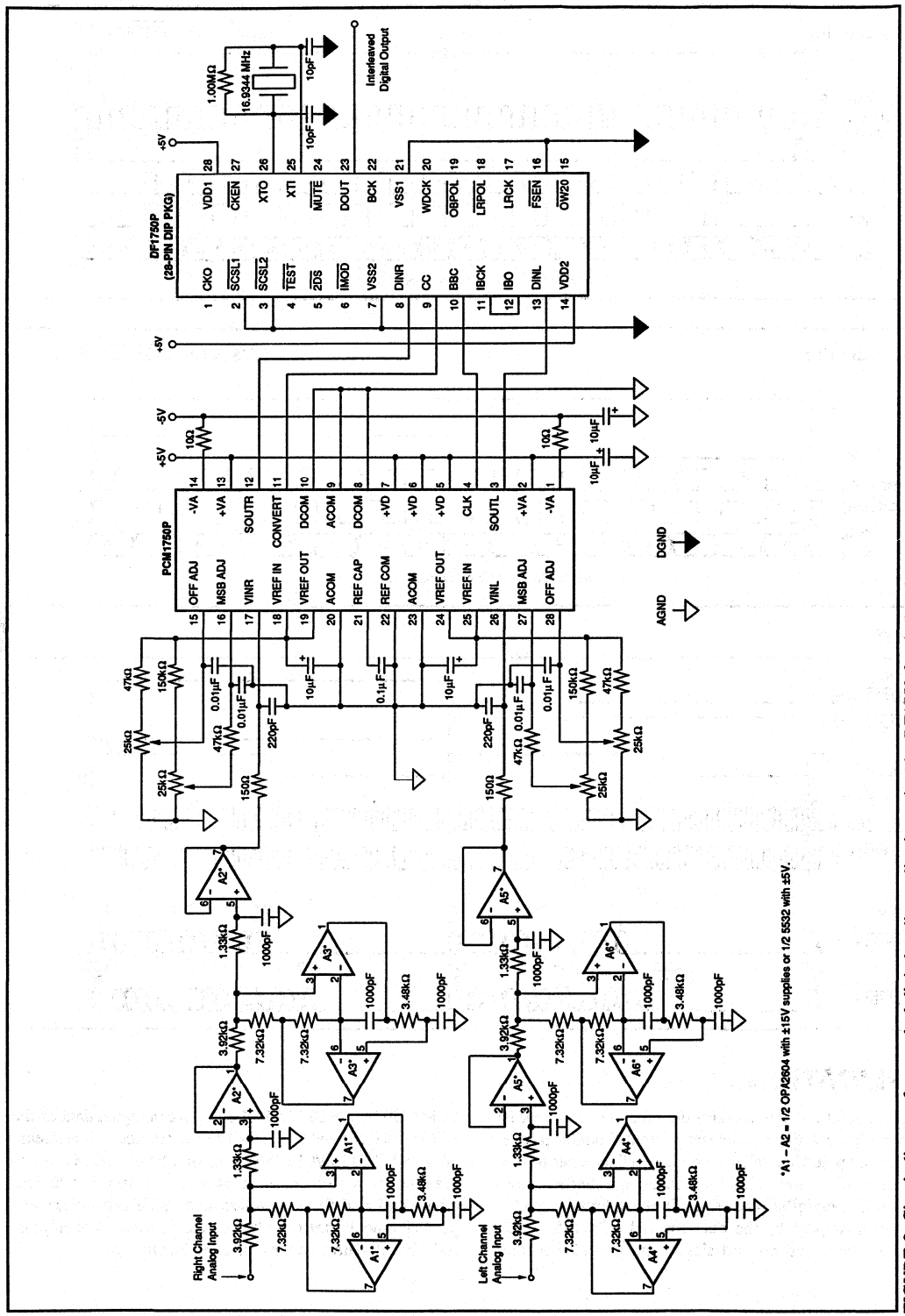
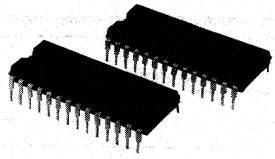


FIGURE 9. Circuit diagram for a typical digital audio application using the DF1750 for decimating oversampled data from the output of the PCM1750 dual channel ADC. The OPA2604s are configured in a generalized immittence converter (GIC) filter arrangement to avoid aliasing in the PCM1750.

BURR-BROWN®



PCM78P

16-Bit Audio ANALOG-TO-DIGITAL CONVERTER

FEATURES

- LOW COST/HIGH PERFORMANCE 16-BIT AUDIO A/D CONVERTER
- FAST 5µs MAX CONVERSION TIME (4µs TYP)
- VERY LOW THD+N (TYP –88dB AT FS; max –82dB)
- ±3V INPUT RANGE
- TWO SERIAL OUTPUT MODES PROVIDE VERSATILE INTERFACING
- COMPLETE WITH INTERNAL REFERENCE AND CLOCK IN 28-PIN PLASTIC DIP
- ±5V TO ±15V SUPPLY RANGE (600mW POWER DISSIPATION)

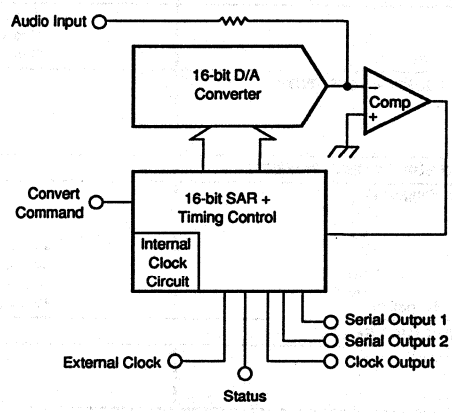
APPLICATIONS

- DSP DATA ACQUISTION
- TEST INSTRUMENTATION
- SAMPLING KEYBOARD SYNTHESIZERS
- DIGITAL AUDIO TAPE
- BROADCAST AUDIO PROCESSING
- TELECOMMUNICATIONS

DESCRIPTION

The PCM78P is a low-cost 16-bit A/D converter which is specifically designed and tested for dynamic applications. It features very fast, low distortion performance (4µs/–88dB THD+N typical) and is complete with internal clock and reference circuitry. The PCM78P is packaged in a reliable, low-cost 28-pin plastic DIP and data output is available in user-selectable serial output formats. The PCM78P is ideal for digital audio tape (DAT) recorders. Many similar applications such as digital signal processing and telecom applications are equally well served by the PCM78P.

The PCM78P uses a SAR technique. Analog and digital portions are efficiently partitioned into a high-speed, bipolar section and a low-power CMOS section. The PCM78P has been optimized for excellent dynamic performance and low cost.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL

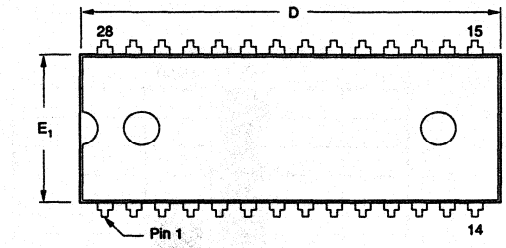
T_C = +25°C, $+V_{DD}$ = +5V, and $\pm V_{CC}$ = ±12V, and one minute warm-up in convection environment, unless otherwise noted.

PARAMETER	CONDITIONS	PCM78P MIN	PCM78P TYP	PCM78P MAX	UNITS
RESOLUTION				16	Bits
INPUT/OUTPUT					
ANALOG INPUT					
Input Range		–3		+3	V
Input Impedance			1.5		kΩ
DIGITAL INPUT/OUTPUT					
Logic Family			TTL Compatible CMOS		
Logic Level: V_{IH}	I_{IH} = +40µA	+2		+5.5	V
V_{IL}	I_{IL} = –100µA	0		+0.8	V
V_{OH}	I_{OH} = 2TTL Loads	+2.4			V
V_{OL}	I_{OL} = 2TTL Loads			+0.4	V
Data Format			Serial BOB or BTC		
Convert Command			Negative Edge [1]		
Pulse Width		25	50		ns
CONVERSION TIME			4	5	µs
DYNAMIC CHARACTERISTICS					
SIGNAL-TO-NOISE RATIO (SNR)[2]	f_S = 200kHz/T_{CONV} = 4µs[3]				
f = 1kHz (0dB)	BW = 20kHz		90		dB[4]
f = 10kHz (0dB)	BW = 100kHz		80		dB
TOTAL HARMONIC DISTORTION[5]	f_S = 200kHz/T_{CONV} = 4µs				
f = 1kHz (0dB)	BW = 20kHz		–91		dB
f = 19kHz (0dB)	BW = 20kHz		–90		dB
f = 10kHz (0dB)	BW = 100kHz		–90		dB
f = 90kHz (0dB)	BW = 100kHz		–89		dB
TOTAL HARMONIC DISTORTION + NOISE[6]	f_S = 200kHz/T_{CONV} = 4µs				
f = 1kHz (0dB)	BW = 20kHz		–88	–82	dB
f = 1kHz (–20dB)	BW = 20kHz		–74	–68	dB
f = 1kHz (–60dB)	BW = 20kHz		–34		dB
f = 19kHz (0dB)	BW = 20kHz		–87		dB
f = 10kHz (0dB)	BW = 100kHz		–82		dB
f = 90kHz (0dB)	BW = 100kHz		–81		dB
TRANSFER CHARACTERISTICS					
ACCURACY					
Gain Error			±2		%
Bipolar Zero Error			±20		mV
Differential Linearity Error			±0.002		% of FSR[7]
Integral Linearity Error			±0.003		% of FSR
Missing Codes			None		14 Bits[8]
DRIFT					
Gain	0°C to +70°C		±25		ppm/°C
Bipolar Zero	0°C to +70°C		±4		ppm of FSR/°C
POWER SUPPLY SENSITIVITY					
$+V_{CC}$			±0.008		%FSR/%V_{CC}
$-V_{CC}$			±0.003		%FSR/%V_{CC}
$+V_{DD}$			±0.003		%FSR/%V_{DD}
POWER SUPPLY REQUIREMENTS					
Voltage Range: $+V_{CC}$		+4.75		+15.6	V
$-V_{CC}$		–4.75		–15.6	V
$+V_{DD}$		+4.75		+5.25	V
Current: $+V_{CC}$	$+V_{CC}$ = +12V		+15		mA
$-V_{CC}$	$-V_{CC}$ = –12V		–21		mA
$+V_{DD}$	$+V_{DD}$ = +5V		+7		mA
Power Dissipation	$\pm V_{CC}$ = ±12V		575		mW
TEMPERATURE RANGE					
Specification		0		+70	°C
Storage		–50		+100	°C
Operating		–25		+85	°C

NOTES: (1) When convert command is high, converter is in a halt/reset mode. Actual conversion begins on negative edge. See detailed text on timing for convert command description when using external clock. (2) Ratio of Noise rms/Signal rms. (3) f = input frequency; f_S = sample frequency (PCM78P and SHC702 in combination); BW = bandwidth of output (based on FFT or actual analog reconstruction using a 20kHz low-pass filter). (4) Referred to input signal level. (5) Ratio of Distortion rms/Signal rms. (6) Ratio of Distortion rms + Noise rms/Signal rms. (7) FSR: Full-Scale Range = 6Vp-p. (8) Typically no missing Codes at 14-bit resolution.

MECHANICAL

P Package — 28-Pin Plastic DIP

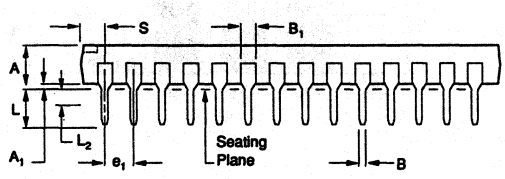


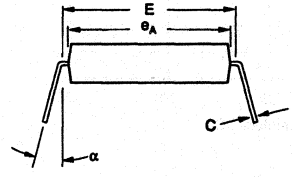
DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A (1)	.169	.200	4.29	5.08
A1 (1)	.015	.070	0.38	1.78
B	.015	.020	0.38	0.51
B1	.015	.055	0.38	1.40
C	.008	.012	0.20	0.30
D (1)	1.380	1.455	35.05	36.96
E	.600	.625	15.24	15.88
E1 (1)	.485	.550	12.32	13.97
e1	.100 BASIC		2.54 BASIC	
eA	.600 BASIC		15.24 BASIC	

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
L	.100	.200	2.54	5.08
L2	.000	.030	0.00	0.76
α	0°	15°	0°	15°
Q1	.020	.070	0.51	1.78
S1	.040	.080	1.02	2.03

(1) Not JEDEC Standard

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.





INPUT/OUTPUT RELATIONSHIPS

ANALOG INPUT	CONDITION	DIGITAL OUTPUT BTC	DIGITAL OUTPUT BOB
+2.999908V	+ Full Scale	7FFF Hex	FFFF Hex
–3.000000V	–Full Scale	8000 Hex	0000 Hex
0.000000V	Bipolar Zero	0000 Hex	8000 Hex
–0.000092V	Zero-1 LSB	FFFF Hex	7FFF Hex

ABSOLUTE MAXIMUM RATINGS

$+V_{CC}$ to Analog Common	0 to +16.5V
$-V_{CC}$ to Analog Common	0 to –16.5V
$-V_{DD}$ to Analog Common	0 to +7V
Analog Common to Digital Common	±0.5V
Logic Inputs to Digital Common	–0.3V to V_{DD} + 0.5V
Analog Inputs to Analog Common	±16.5V
Lead Temperature (soldering, 10s)	+300°C

Stresses above these ratings may permanently damage the device.

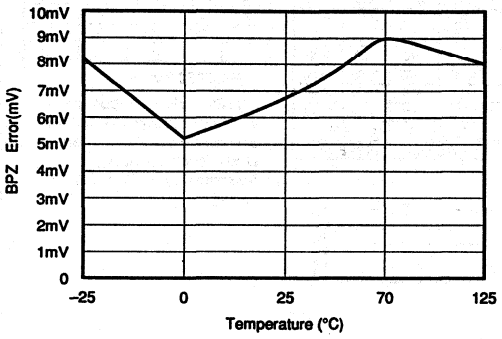
PIN ASSIGNMENTS

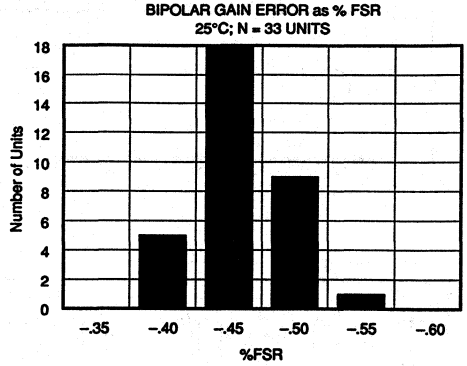
PIN	NAME	I/O	DESCRIPTIUON
1	Analog In	I	Analog Signal Input (1.5kΩ impedance).
2	$-V_{CC}$	I	Analog power supply (–5V to –15V).
3	MSB Adjust	I	Internal adjustment point to allow adjustment of MSB major carry.
4	$+V_{DD}$	I	Power connection for comparator (+5V).
5	No Connection	—	No internal connection.
6	Comparator Common	I	Comparator common connection. Connect to ground.
7	$\overline{MSB}$	O	Parallel output of bit 1 (MSB) inverted.
8	BTC/BOB Select	I	Two's complement (open) or straight binary (grounded) data output format selection.
9	Status	O	Output signal held high until conversion is complete.
10	Clock Out	O	Internal clock output generated from RC network on pins 11 and 12 (also present when external clock is used lagging external clock by ~24ns and same duty cycle).
11	R_1C_1	I	RC connection point used to generate internal clock. Sets clock high time. See text for details.
12	R_2C_2	I	RC connection point used to generate internal clock. Sets clock low time. See text for details.
13	S_{OUT2}	O	Internal shift register containing the previous conversion result. (Alternate latched data output mode).
14	$+V_{DD}$	I	Power connection for +5V logic supply.
15	S_{OUT1}	O	Primary real-time data output synchronized to clock out.
16	External Clock	I	External clock input point (internal clock must be disabled).
17	Int/Ext Clock Select	I	Selects either internal or external clock mode (low = internal; open = external).
18	Short Cycle	I	Terminates conversion at less than 16-bits (open for 16-bit mode). See text for details.
19	Convert Command	I	Starts conversion process (can optionally be generated internally).
20	S_{OUT2} Latch	I	Latches previous conversion result for readout (must be issued with the S_{OUT2} clock to initiate latch and an internal convert command).
21	S_{OUT2} Clock	I	Used to read out internally latched data from previous conversion.
22	Digital Common	I	Digital grounding pin.
23	$+V_{CC}$	I	Analog supply connection (+5V to +15V).
24	V_{POT}	O	Voltage output (~2.5V) for optional adjustment of MSB transition.
25	Reference Decouple	I	Reference decoupling point.
26	Analog Common	I	Analog grounding pin.
27	Reference Out	O	2V reference out. Should not be used except as shown in connection diagram.
28	Speed Up	I	Connection point for a capacitor to speed reference settling. See text for details.

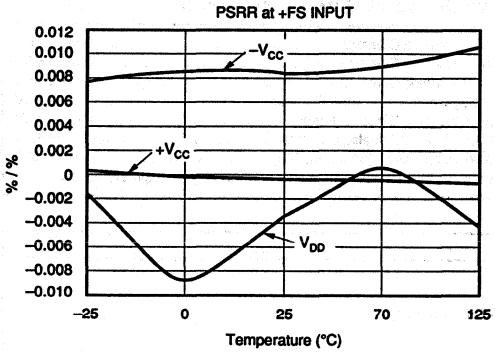
NOTE: Analog and digital commons are connected internally.

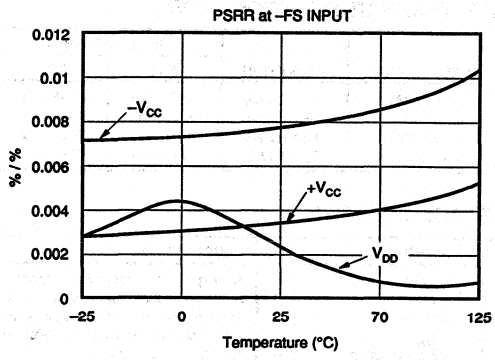
TYPICAL PERFORMANCE CURVES

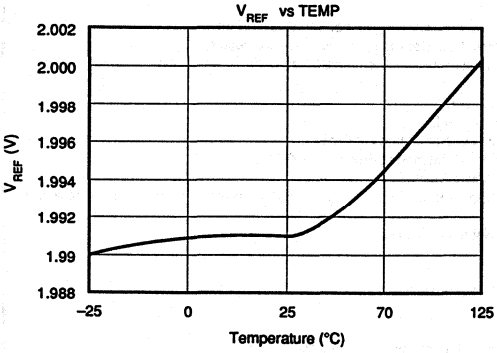
T_A = +25°C, V_{CC} = ±15V unless otherwise noted.

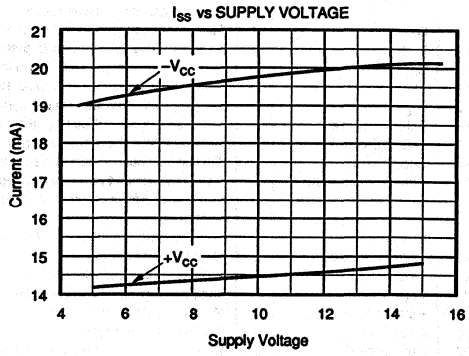








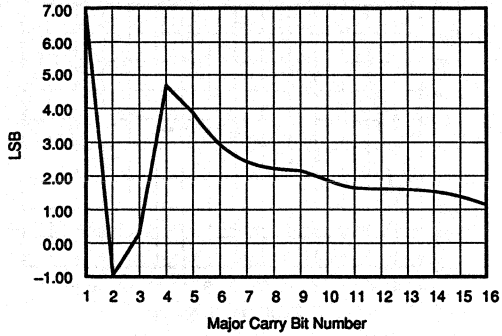




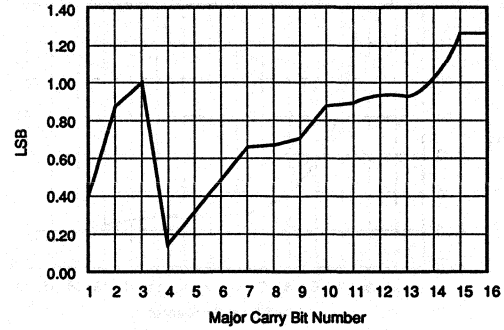
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_{CC} = ±15V unless otherwise noted.

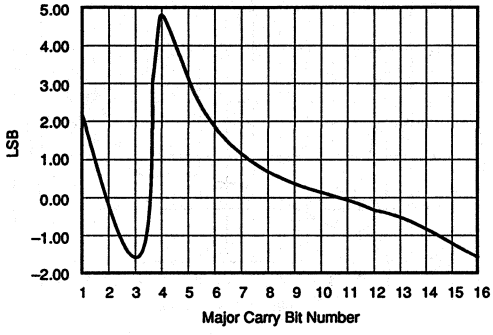
INTEGRAL NONLINEARITY
at –25°C



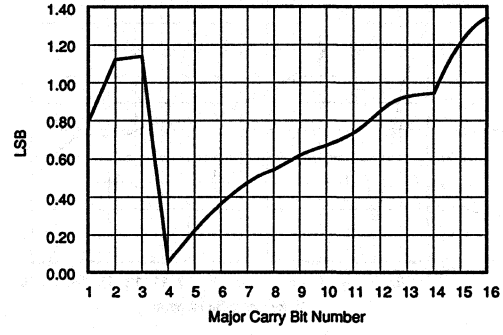
DIFFERENTIAL NONLINEARITY
at –25°C



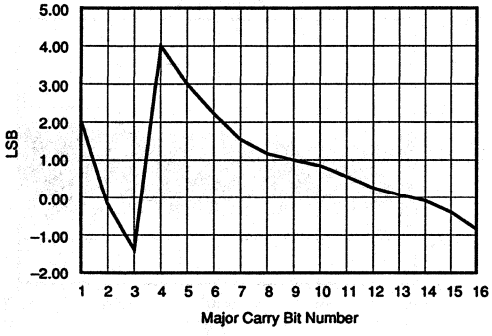
INTEGRAL NONLINEARITY
at 0°C



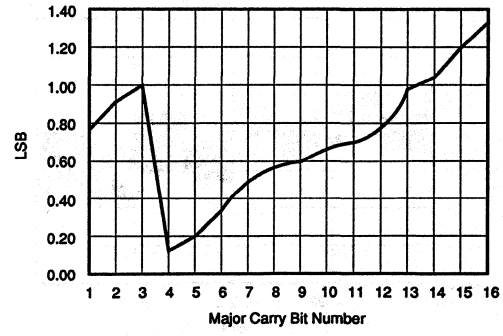
DIFFERENTIAL NONLINEARITY
at 0°C



INTEGRAL NONLINEARITY
at 25°C



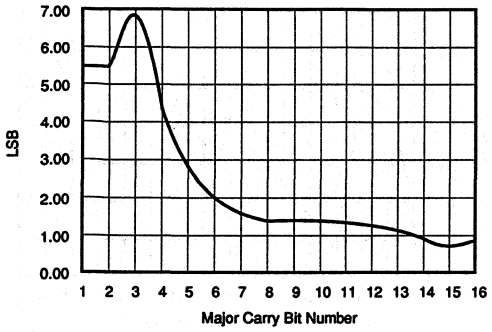
DIFFERENTIAL NONLINEARITY
at 25°C



TYPICAL PERFORMANCE CURVES (CONT)

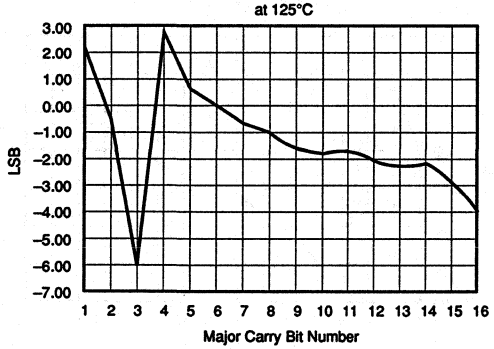
T_A = +25°C, V_{CC} = ±15V unless otherwise noted. Histograms done with conversion time = 8µs.

INTEGRAL NONLINEARITY
at 70°C

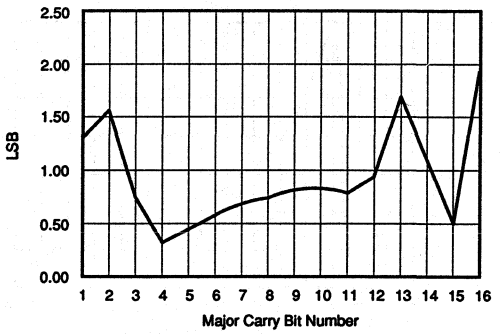


DIFFERENTIAL NONLINEARITY
at 70°C

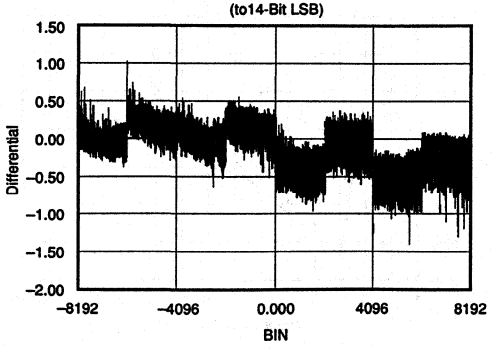
INTEGRAL NONLINEARITY
at 125°C



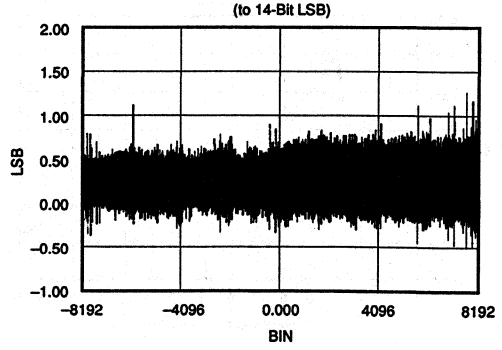
DIFFERENTIAL NONLINEARITY
at 125°C



INTEGRAL NONLINEARITY ERROR
(to14-Bit LSB)



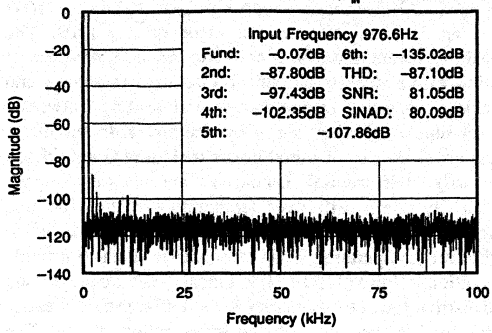
DIFFERENTIAL NONLINEARITY ERROR
(to 14-Bit LSB)



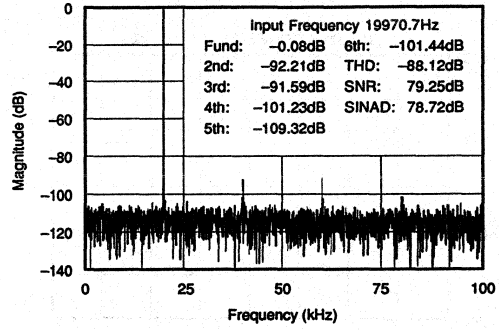
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_{CC} = ±15V unless otherwise noted. Histograms done with Conversion Time = 8µs.

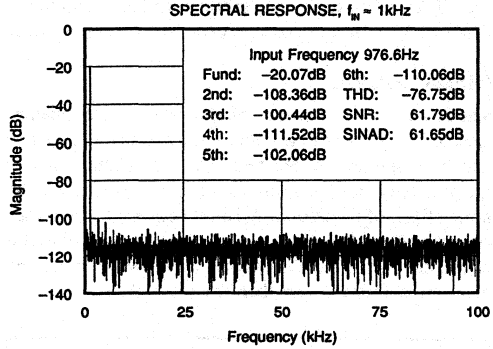
SPECTRAL RESPONSE, f_{IN} = 1kHz



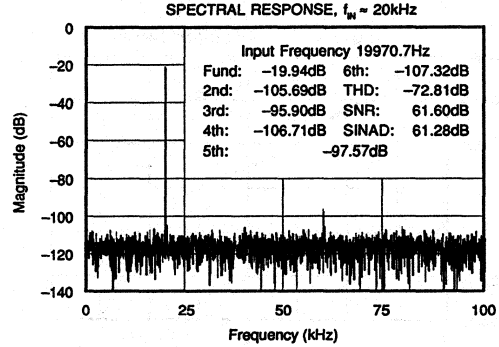
SPECTRAL RESPONSE, f_{IN} = 20kHz



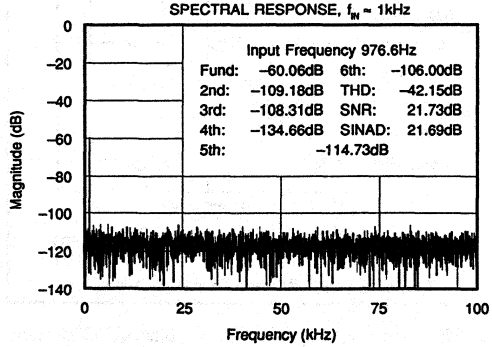
SPECTRAL RESPONSE, f_{IN} = 1kHz



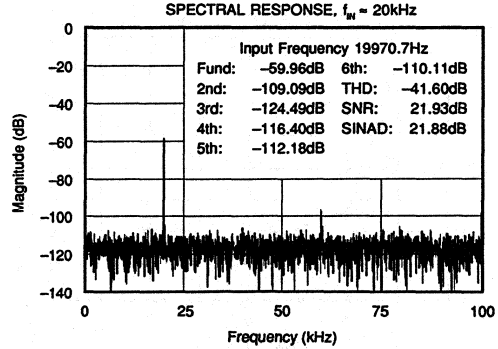
SPECTRAL RESPONSE, f_{IN} = 20kHz



SPECTRAL RESPONSE, f_{IN} = 1kHz

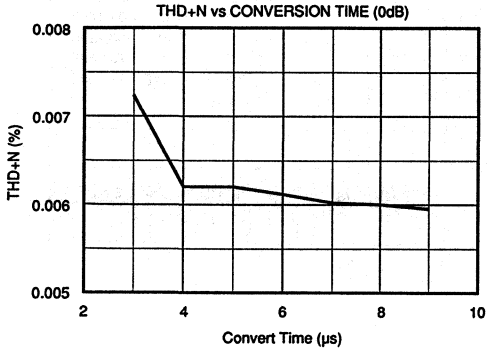


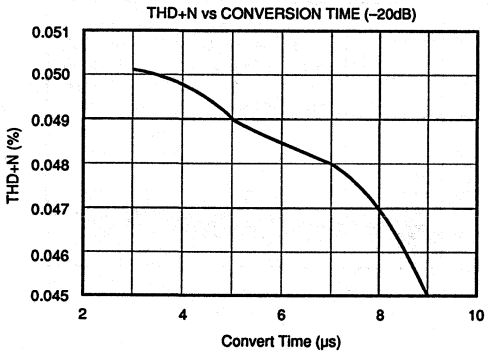
SPECTRAL RESPONSE, f_{IN} = 20kHz

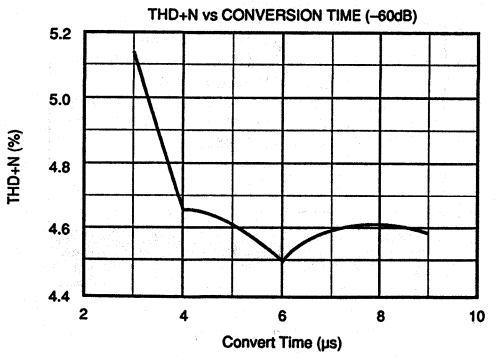


TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_{CC} = ±15V unless otherwise noted.







THEORY OF OPERATION

The PCM78P is a successive approximation A/D converter; this type of converter is well suited to high speed and resolution. The accuracy of a successive approximation converter is described by the transfer function shown in Figure 1. All successive-approximation A/D converters have an inherent quantization error of ±1/2LSB. The remaining errors in the A/D converter are combinations of analog errors due to the linear circuitry, matching and tracking properties of the ladder and scaling networks, power supply rejection, and reference errors. In summary, these errors consist of initial errors including Gain, Offset, Linearity, Differential Linearity, and Power Supply Sensitivity. Gain drift over temperature rotates the line (Figure 1) about zero, and Offset drift shifts the line left or right over the operating temperature range. Total Harmonic Distortion + Noise (THD + N) is a measure of the magnitude and distribution of the Linearity Error, Differential Linearity Error, and Noise, as well as quantization errors. The THD+N specification is most useful in audio or dynamic signal processing applications. To be useful, THD + N should be specified for both high level and low level input signals. This error is unadjustable and is the most meaningful indicator of A/D converter accuracy for dynamic applications.

DYNAMIC RANGE

Dynamic range is a measure of the ratio of the smallest signals the converter can resolve to the full scale range and is usually expressed in decibels. The theoretical dynamic range of a converter is approximately 6 x n, where n is the number of bits of resolution. A 16-bit converter would thus have a theoretical dynamic range of 96dB. The actual useful dynamic range is limited by noise and linearity errors and is therefore somewhat less than the theoretical limit.

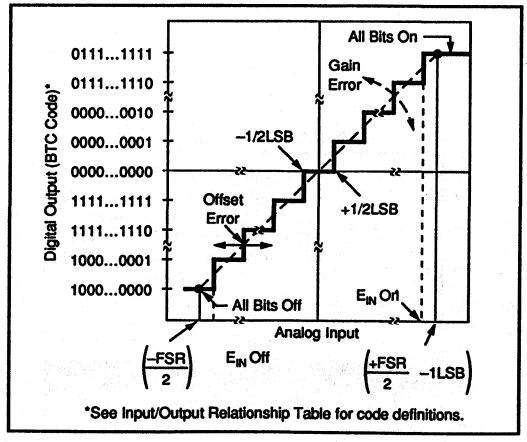


FIGURE 1. Input vs Output for Ideal Bipolar A/D Converter.

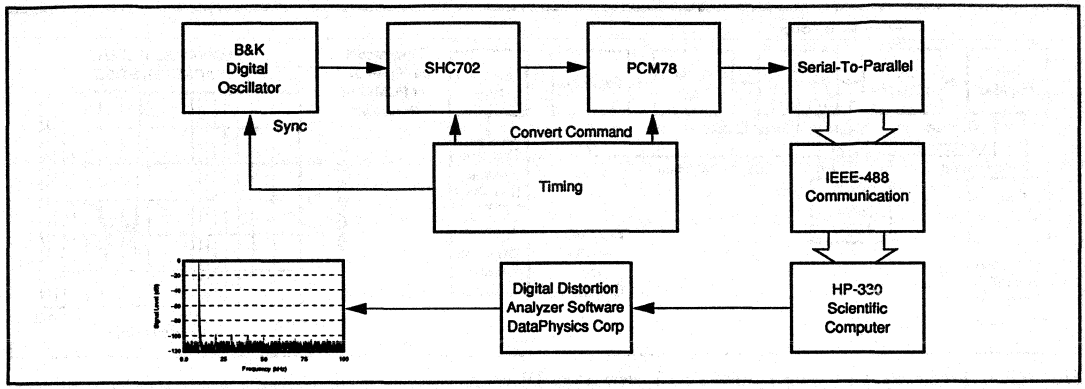


FIGURE 2. Block Diagram of Distortion Test Circuit.

DISCUSSION OF SPECIFICATIONS

TOTAL HARMONIC DISTORTION

Evaluating distortion specifications can be a difficult task, as distortion is often specified in different ways. Total Harmonic Distortion (THD) is defined as the ratio of the square root sum of the squares of the value of rms harmonics to the value of the rms fundamental and is expressed in percent or dB. Note that this measurement only includes energy present in those frequencies which would contain harmonics, and therefore is less than Total Harmonic Distortion plus Noise.

The Total Harmonic Distortion plus Noise (THD + N) is defined as the ratio of the square root of the sum of the squares of the value of the rms harmonics and rms noise to the value of the rms fundamental and is expressed in percent or dB. This is the most meaningful measurement of a dynamic converter's performance because it includes all energy present in the signal that is not fundamental. A block diagram of the test circuit used to measure the THD and THD + N of the PCM78 is shown in Figure 2. This digital system is capable of differentiating harmonic energy and noise; conventional distortion analyzers which operate on a tracking notch filter principle cannot distinguish this energy, and therefore only measure THD + N. Unfortunately, in the past, these systems were used for measuring distortion performance of converters, and the distortion was often simply specified as "THD", when in fact it was really THD + N. For this reason, it is often confusing to compare specifications of converters unless one knows exactly what was being measured.

If we assume that the error due to the test circuit of Figure 2 is negligible, then the rms value of the PCM78 error referred to the input can be shown to be

$$THD + N = \frac{\sqrt{\frac{1}{N}\sum_{i=1}^{N}\left[E_L(i) + E_Q(i) + E_N(i)\right]^2}}{E_{rms}} X\ 100\%$$

where N is the number of samples, $E_L(i)$ is the linearity error at each sample, $E_Q(i)$ is the quantization error at each

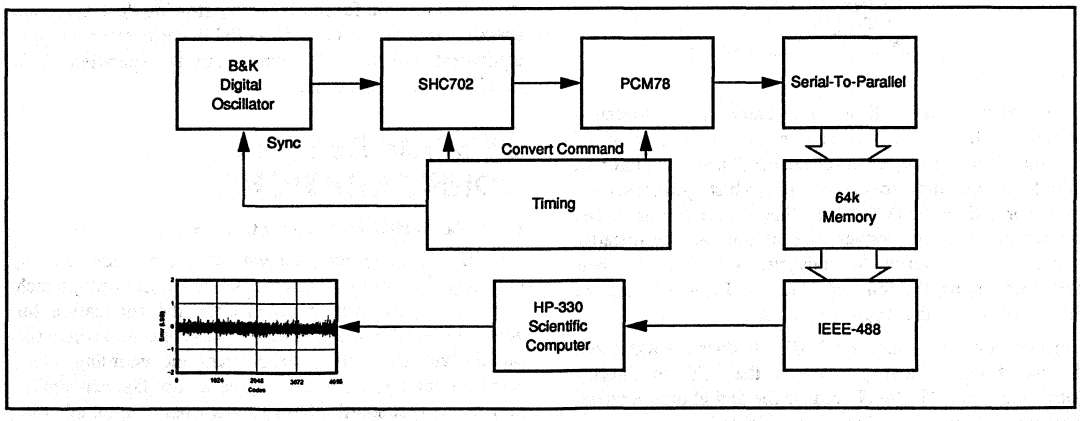


FIGURE 3. Block Diagram of Histogram Test .

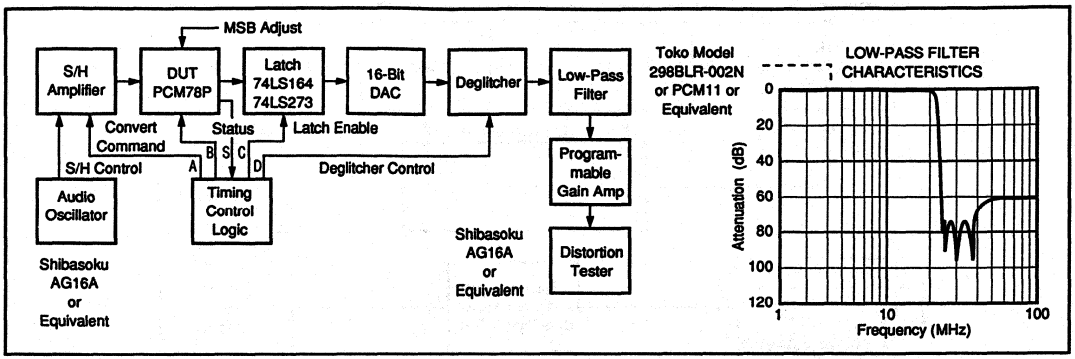


FIGURE 4. Production Distortion + Noise Test System Block Diagram.

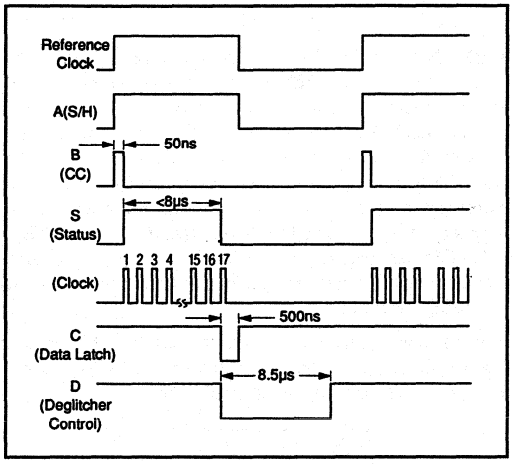


FIGURE 5. Timing Diagram for Figure 4.

sample, and $E_N(i)$ is the residual noise energy present at each sample. Similarly, THD alone can be expressed as

$$THD = \frac{\sqrt{\frac{1}{N}\sum_{i=1}^{N}[E_L(i)]^2}}{E_{rms}} X\ 100\%$$

These expressions indicate that there is a correlation between THD + N and the square root of the sum of the squares of the linearity errors at each digital word of interest. In order to find this error at each code, a histogram test must be performed on the PCM78, as illustrated in Figure 3. The histogram for every converter is unique, as the linearity errors from converter to converter will vary in their placement along the transfer function. Typical histogram data is shown in the Typical Curves.

However, this expression for THD + N does not mean that the worst case linearity error of the A/D is directly correlated to the THD + N because the digital output words from the A/D vary according to the amplitude and frequency of the sine wave input as well as the sampling frequency.

For the PCM78 the test sampling frequency was chosen to be 200kHz, near the PCM78's fastest rate of conversion. The test frequencies used vary within the audio range, and are stepped in amplitude from 0dB, to –20dB, to –60dB.

In manufacturing the PCM78, the test system shown in Figure 4 is used to test for guaranteed THD + N.

ACCURACY VS CONVERSION TIME AND INPUT SIGNAL LEVEL

The relationship of THD vs input signal level and THD vs conversion time is shown is the typical curves. Slowing the conversion time to more than 8µs results in little added benefit in terms of THD + N.

For applications which are not as concerned with dynamic performance but require DC accuracy and linearity, it is best to use the PCM78 at the longest conversion time possible for the system requirements. Slowing the PCM78 to 8µs-10µs conversion time results in a substantial improvement in linearity. The typical curves show DNL and INL plots for a typical device, at an 8µs conversion time. Due to the segmented architecture of the internal DAC used in the successive approximation conversion technique, significant differential linearity errors occur near bits 3 and 4. Allowing more settling time for the DAC (by slowing the conversion speed) will improve this differential linearity error and give equivalent performance to more costly DC-specified 12-bit to 14-bit A/D converters.

SYSTEM DESIGN CONSIDERATIONS

DIGITAL CIRCUIT CONNECTIONS

The PCM78 comes complete with an internal clock circuit, or it may be clocked by an external clock. Choosing which mode to operate with depends upon the application for which the PCM78 will be used. In an application where the sample rate may not be fixed (transient recording, etc.), using the internal clock set to give a very fast conversion may be the best solution. In systems where the sample rate is fixed, an external clock is probably the better choice since it will allow the digital system design to be synchronous.

In either case, the PCM78 requires 17 clock cycles to complete a conversion. To calculate the clock frequency necessary for a given conversion time, the following equation may be used:

$$f_{CLOCK} = \frac{17}{\text{Conversion Time}}$$

The internal clock operates only during a conversion, and is gated on by the falling edge of the convert command. See Figure 6. The internal clock is available on pin 10, Clock Out. The high and low time of this clock is set by R_1C_1 and R_2C_2 respectively. The duty cycle of the clock should be between 20% to 80%, and may be set to 50% for simplicity.

$$\text{Clock High Time (in ns)} = 1.32R_1C_1$$

$$\text{Clock Low Time (in ns)} = 1.32R_2C_2$$

$$R \text{ in } k\Omega;\ C \text{ in pF.}$$

These equations are approximate (±5%); they should be used for determining an initial part value which will then need to be "tweaked" for accurate timing. If highly accurate time bases are required, use of an external clock is recommended.

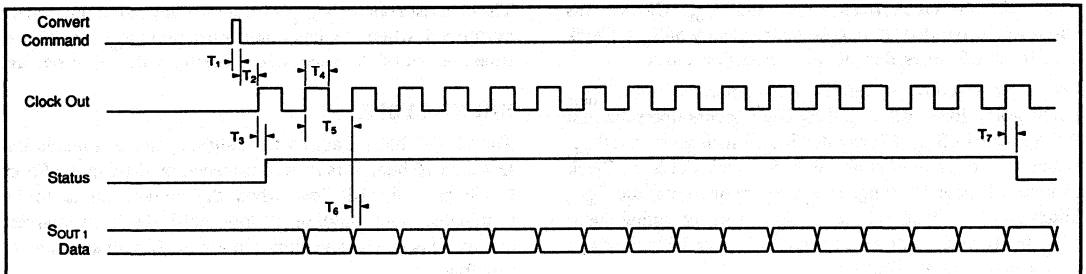
The external clock is applied at pin 16, and the Int/Ext Clock select (pin 17) should be left open (an internal pull-up resistor assures that the logical state of an open pin is "1"). Using the external clock requires careful placement in time of the convert command. Figure 7 diagrams the recommended timing with an external clock. A simple circuit which assures the proper timing of the convert command is shown in Figure 8.

Due to the design of the Clock/Logic chip in the PCM78, a conversion is begun inside the PCM78 by an asynchronous state machine. This places stringent requirements on the timing of the convert command, as improper timing can cause metastable states within this state machine. Using the circuitry shown in Figure 8, the user is assured of consistent operation, and these invalid states within the state machine are entirely avoided. (Note that this is not a consideration when using an internal clock, as nothing is being clocked when a convert command is presented to the PCM78).

The Clock Out function is a gated form of the external clock, i.e. the 17 clock cycles used in the conversion are present on this pin during conversion. This allows use of a continuous external clock, with Clock Out being the clock that the converter is actually using for conversion. Note that this is simply a delayed (~24ns) version of the external clock, and will have the same frequency and duty cycle.

The S_{OUT2} Latch enables the user to latch data from the previous conversion and read it out at a higher speed than the convert clock. This feature allows the converter to easily interface to digital filtering necessary for oversampling. See Figure 9 for timing information in this mode.

In this mode, the PCM78 generates its own internal convert command when the S_{OUT2} Clock goes high within ±50ns of S_{OUT2} Latch going low; the external convert command may not be used, and pin 19 must be grounded. The timing diagram shows the recommended timing for using this mode. After the S_{OUT2} Latch control signal goes low, data from the SAR is loaded into the S_{OUT2} latch on the next rising edge of the S_{OUT2} Clock. This clock edge should occur prior to the next rising edge of the conversion clock (internal or external), since the SAR will reset itself prior to the latching

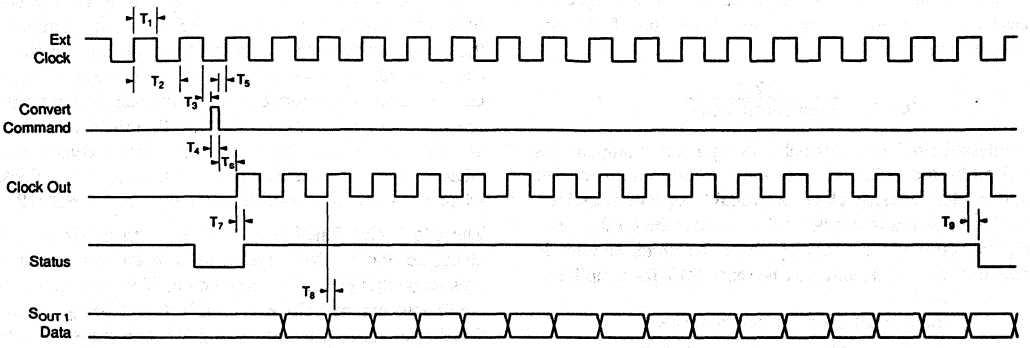


T_A = +25°C, V_{DD} = +5V, guaranteed by sample testing; these parameters are not 100% tested in production.

TIME	DESCRIPTION	TIME (ns) MIN	TYP	MAX
T_1	CONVERT COMMAND pulse width	25	50	(1)
T_2	Delay from falling edge of CONVERT COMMAND to rising edge of CLOCK OUT	60	70	85
T_3	Delay from rising edge of CLOCK OUT to rising edge of STATUS	8	10	30
T_4	INTERNAL CLOCK pulse width	50	125	450
T_5	INTERNAL CLOCK period	140	290	500
T_6	Delay from rising edge of CLOCK OUT to bit data valid	17	20	50
T_7	Delay from rising edge of 17th clock pulse to falling edge of STATUS	10	15	30

NOTE: (1) When using the internal clock, the clock does not operate until the Convert Command is low. It is therefore possible to keep the convert command high indefinitely, thereby keeping the PCM78 in a halt mode. The conversion cycle begins on the falling edge of convert command, and convert command must remain low during the entire conversion cycle in order to make the PCM78 operate properly.

FIGURE 6. Conversion Timing when using Internal Clock.



T_A = +25°C, V_{DD} = +5V, guaranteed by sample testing; these parameters are not 100% tested in production.

TIME	DESCRIPTION	TIME (ns) MIN	TYP	MAX
T_1	EXTERNAL CLOCK pulse width	50	125	(1)
T_2	EXTERNAL CLOCK period	140	290	(1)
T_3	Delay from falling edge of EXTERNAL CLOCK to rising edge of CONVERT COMMAND	–30	0	420
T_4	CONVERT COMMAND pulse width	10	50	200
T_5	Delay from falling edge of CONVERT COMMAND to rising edge of EXTERNAL CLOCK	20	50	430
T_6	Delay from falling edge of CONVERT COMMAND to rising edge of CLOCK OUT	40	75	460
T_7	Delay from rising edge of CLOCK OUT to rising edge of STATUS	6	10	30
T_8	Delay from rising edge of CLOCK OUT to bit data valid	15	17	20
T_9	Delay from rising edge of 17th clock pulse to falling edge of STATUS	8	10	30

NOTE: (1) The PCM78 does not contain dynamic digital circuitry, and can be clocked as slowly as the user wishes. In typical applications, the longest clock period may be as long as 1µs.

FIGURE 7. Conversion Timing when using External Clock.

if the convert clock rises before the S_{OUT2} Clock. This condition is avoided as long as the frequency of S_{OUT2} Clock is at least 1.5 times that of the conversion clock.

The internal convert command is generated upon S_{OUT2} Latch going low, and its falling edge occurs upon the first falling edge of S_{OUT2} Clock after S_{OUT2} Latch goes low. S_{OUT2} Latch should remain low for at least 2 cycles of S_{OUT2} Clock to insure proper latching. In many applications, the S_{OUT2} Latch can be the $2f_S$ signal present in many digital audio systems, typically known as WDCK. Figure 10 includes an example of this application.

The data read out on S_{OUT2} is from the conversion previously performed, while the data that is present on S_{OUT1} is the real time readout of the successive approximation as it occurs.

SHORT CYCLE

The PCM78 has the ability to be short cycled to a resolution less than 16 bits. This is accomplished by driving the Short Cycle pin (pin 18) low when the conversion is to be terminated, and holding it low until the next convert command is given. The circuit in Figure 11 will accomplish this function.

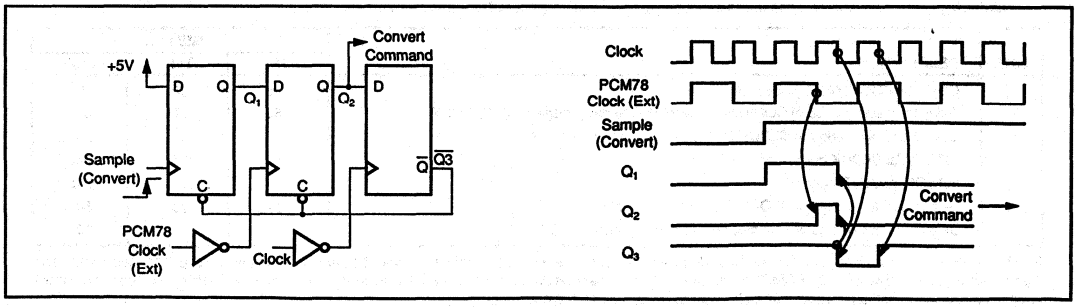
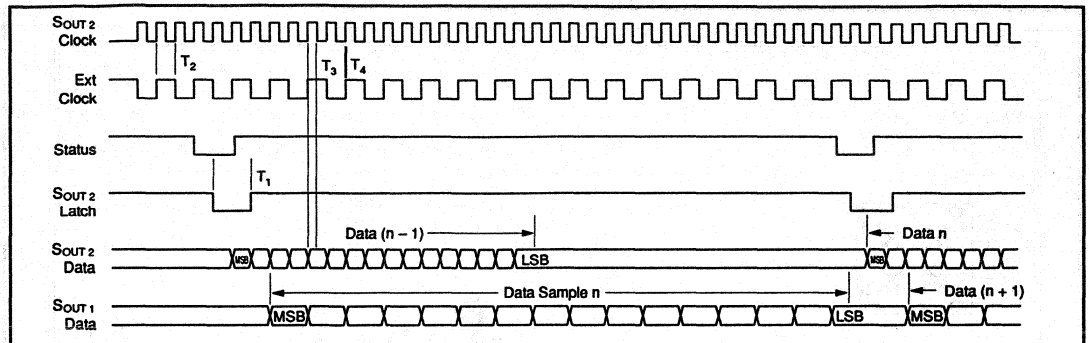


FIGURE 8. Convert Command Timing Circuit for Use with External Clock.



T_A = +25°C, V_{CC} = +5V, guaranteed by sample testing; these parameters are not 100% tested in production.

TIME	DESCRIPTION	TIME (ns) MIN	TYP	MAX
T_1	S_{OUT2} Latch pulse width	50	100	
T_2	S_{OUT2} Clock Cycle		24	
T_3	Delay from rising edge of CLOCK OUT to bit data valid		10	30
T_4	Delay from rising edge of S_{OUT2} Clock to rising edge of Ext Clock	50	125	

FIGURE 9. Timing when using S_{OUT2} Latch.

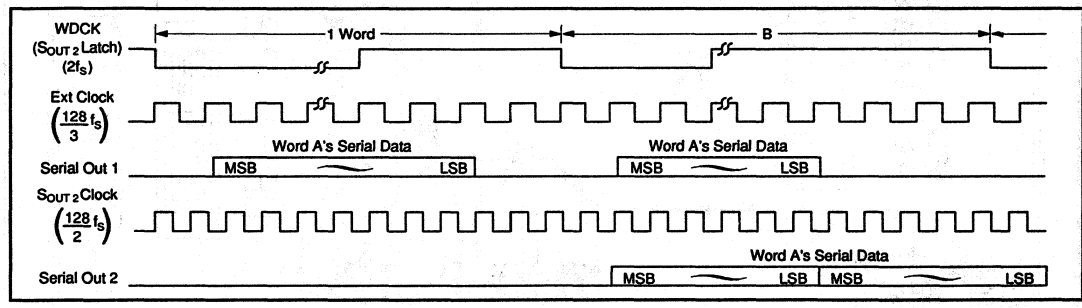
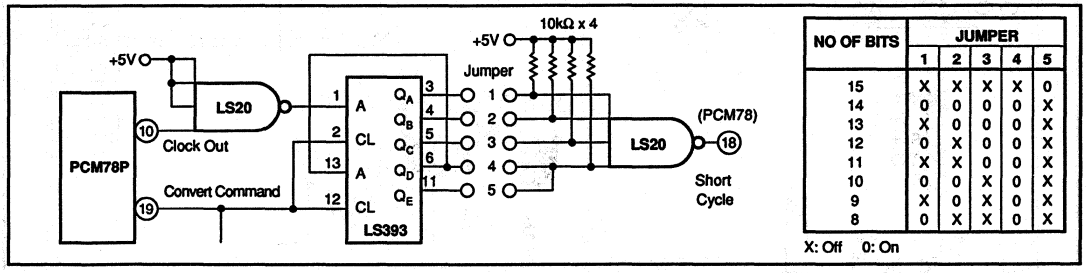


FIGURE 10. Application Example of S_{OUT2} Operation.



NO OF BITS	JUMPER 1	2	3	4	5
15	X	X	X	X	0
14	0	0	0	0	X
13	X	0	0	0	X
12	0	X	0	0	X
11	X	X	0	0	X
10	0	0	X	0	X
9	X	0	X	0	X
8	0	X	X	0	X

X: Off 0: On

FIGURE 11 . Short Cycle Circuit.

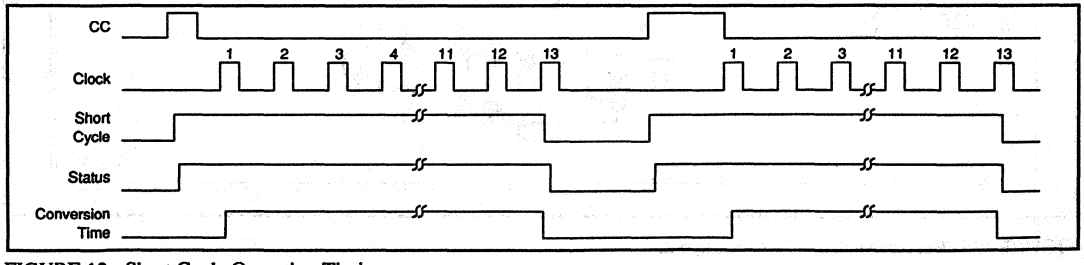


FIGURE 12. Short Cycle Operation Timing.

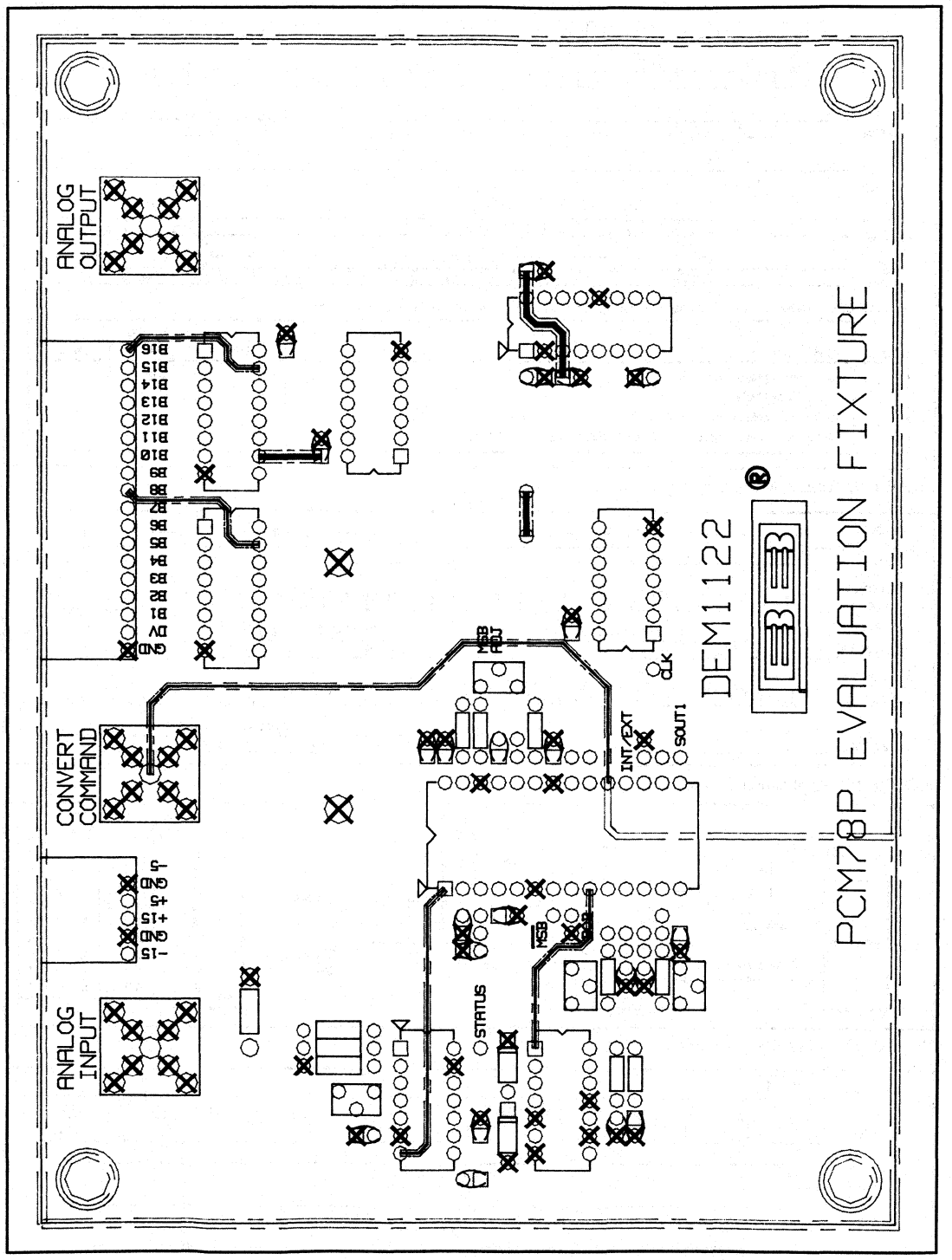


FIGURE 13a. Recommended PC Board Layout.

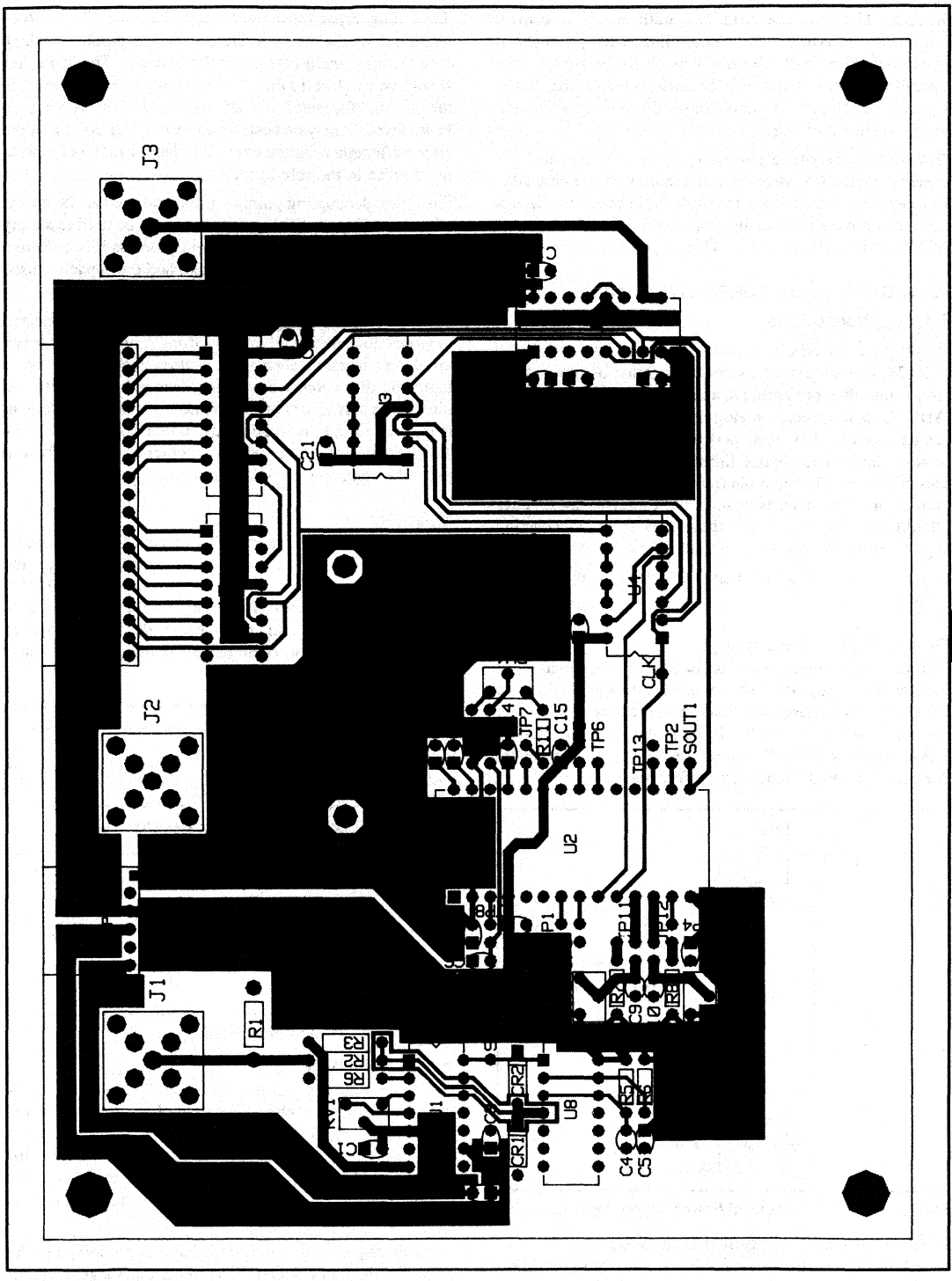


FIGURE 13b. Recommended PC Board Layout.

If Short Cycle is not held low until the next convert command is issued, the Status line will go high in synchronization with Short Cycle. This is because the operation of the Status line becomes invalid after Short Cycle is asserted. An example of the Short Cycle operation is shown in Figure 12.

In those systems where a user may not be using a continuous external clock, it is necessary to assure that a falling edge of external clock occurs after short cycle goes low. This is because conversion actually stops on the first falling edge of external clock after Short Cycle goes low.

ANALOG CIRCUIT CONSIDERATIONS

Layout Precautions

Analog and Digital Common are connected internally in the PCM78, and should be connected together as close to the unit as possible, preferably to a large ground plane under the ADC. Low impedance analog and digital common returns are essential for low noise performance. Coupling between analog inputs and digital lines should be minimized by careful layout. The input pin (pin 1) and the MSB adjust pin (pin 3) are both extremely sensitive to noise; digital lines should be kept away from these pins to avoid coupling digital noise into the sensitive analog circuitry.

Figure 13 shows a recommended PCB layout for the PCM78.

Power Supply Decoupling

The power supplies should be bypassed with tantalum or electrolytic capacitors as shown in Figure 14 to obtain noise free operation. These capacitors should be located as close to the ADC as possible. Bypass the 1µF electrolytic capacitors with 0.01µF ceramic or polystyrene capacitors for improved high frequency performance.

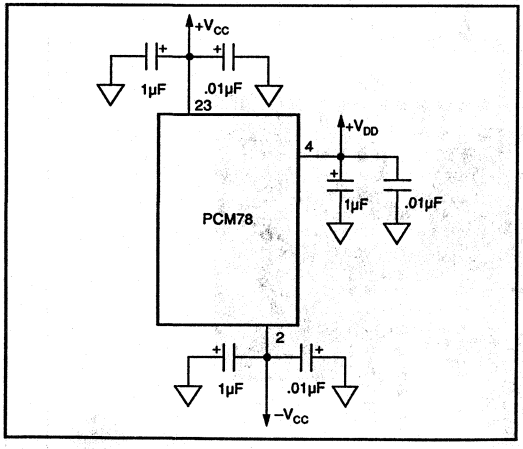


FIGURE 14. Recommended Power Supply Decoupling.

Reference Decoupling and Speed Up

In order to assure the lowest noise operation of the PCM78, the reference may be bypassed by three different capacitors. Pin 25 is a decoupling point for the reference to $-V_{CC}$. The decoupling capacitor should range from 0.1µF to 4.7µF; larger values can cause reference settling problems which may manifest themselves as missing codes. This capacitor should be as close to the PCM78 as possible, to minimize the potential for coupling noise into the device; with a good board layout it may be best to leave this capacitor out of the circuit altogether, as the extra lead length may only cause more noise in the reference.

Pin 27 is a decoupling point to ground, as well as the output of the 2V reference. This point should not be used to supply reference voltage to external circuitry unless it is buffered. A 2.2µF capacitor is recommended, and the capacitor used here should not exceed 4.7µF.

Pin 28, the Speed Up pin, allows a capacitor to be connected to ground to facilitate reference settling. This does not speed up the conversion time, but it does reduce odd order harmonic distortion. As with the decoupling capacitor on pin 25, this may also contribute to noise; if harmonic content is most important in an application, this capacitor (0.1µF - 10µF) should be connected. In all other cases, it is best to leave the capacitor out of the circuit.

Input Scaling

The analog input should be scaled as close to the maximum input signal range as possible in order to utilize the maximum signal resolution of the A/D converter. The DAC inside the PCM78 has a ±2mA range, and the nominal ±3V input is scaled by a 1.5kΩ resistor. In order to scale to other ranges, see Table I for recommended scaling resistor values, connected as shown in Figure 15.

INPUT RANGE	R
±10V	8.2kΩ
±5V	3.3kΩ
NOTE: R values shown assume use of 1k trim pot to adjust for scale accuracy.	

TABLE I. PCM78 Input Scaling Resistor Values.

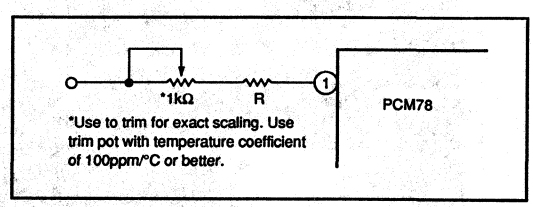


FIGURE 15. PCM78 Input Scaling Circuit.

INPUT IMPEDANCE

The input signal to the PCM78 should come from a low impedance source, such as the output of an op amp, to avoid any errors due to the dynamic input impedance that a successive-approximation converter presents to the the outside world because of the changing currents in this circuit during conversion as the converter steps through its approximations.

If the driving circuit output impedance is not low, a buffer amplifier should be added between the input signal and the direct input to the PCM78 as shown in Figure 16.

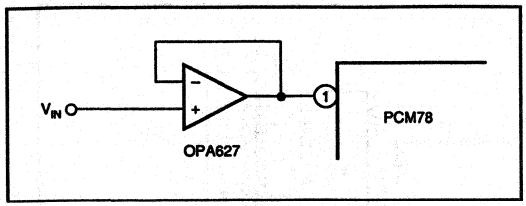


FIGURE 16. Buffer Amplifier for PCM78 Input.

MSB Adjustment

Differential Linearity errors at bipolar zero and THD are guaranteed to meet data sheet specifications without any external adjustment. However, a provision has been made for an optional adjustment of the MSB linearity point which makes it possible to eliminate DLE error at BPZ. This is important when the signal level is very low, because zero crossing noise (DLE at BPZ) becomes very significant when compared to the small codes changes occurring in the LSB portion of the converter.

The PCM78 is laser trimmed for best performance at the factory without the MSB adjust circuitry installed; if better performance can be obtained it would be by the addition of the MSB adjust circuitry shown in Figure 17.

The best method of adjusting the MSB is by using a real time FFT routine to monitor the levels of odd order harmonics when a sine-wave is being digitized by the PCM78. Adjusting the potentiometer in Figure 17 will allow the user to reduce the magnitude of odd-order harmonics.

An alternate method is to recontruct the data out of the PCM78 through a DAC, and measure THD+N on a conventional distortion analyzer. Adjust the potentiometer for minimum THD+N.

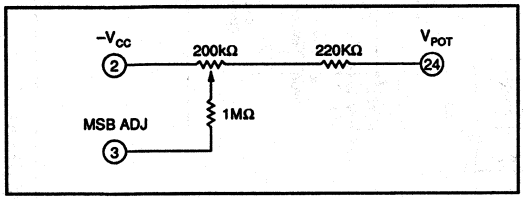


FIGURE 17. MSB Adjust Circuit.

APPLICATIONS INFORMATION

A typical digitization circuit, used on the demonstration board available for the PCM78, is shown in Figure 21. The connections and part values shown in this circuit have been optimized for the best THD+N performance at a 200kHz sample rate.

The PCM78 may be interfaced to many popular digital signal processors, such as the TMS320, DSP56001, and the DSP32. Suggested interface circuits for these processors are shown in Figures 18-20.

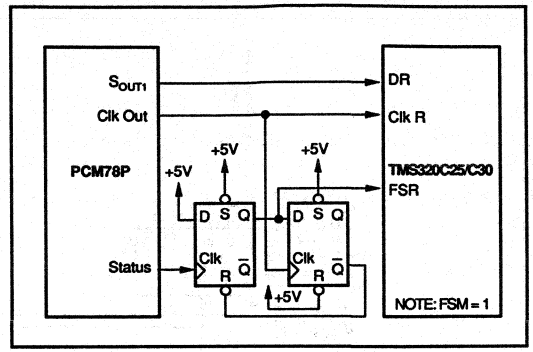


FIGURE 18. PCM78 Interface to TMS320C25/C30 DSP Processors.

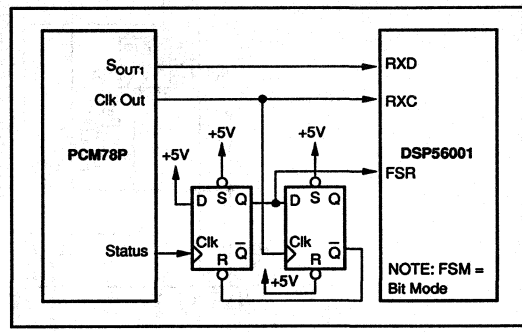


FIGURE 19. PCM78 Interface to Motorola DSP56001 DSP Processor.

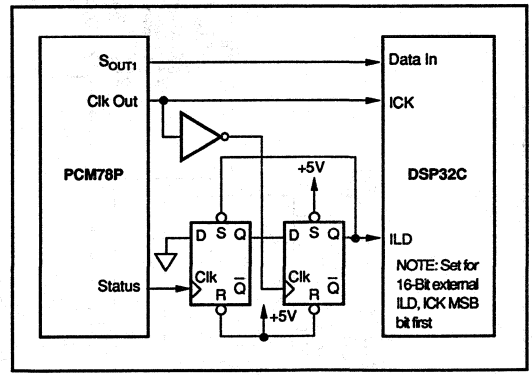


FIGURE 20. PCM78 Interface to AT&T DSP16 & DSP32C Processors.

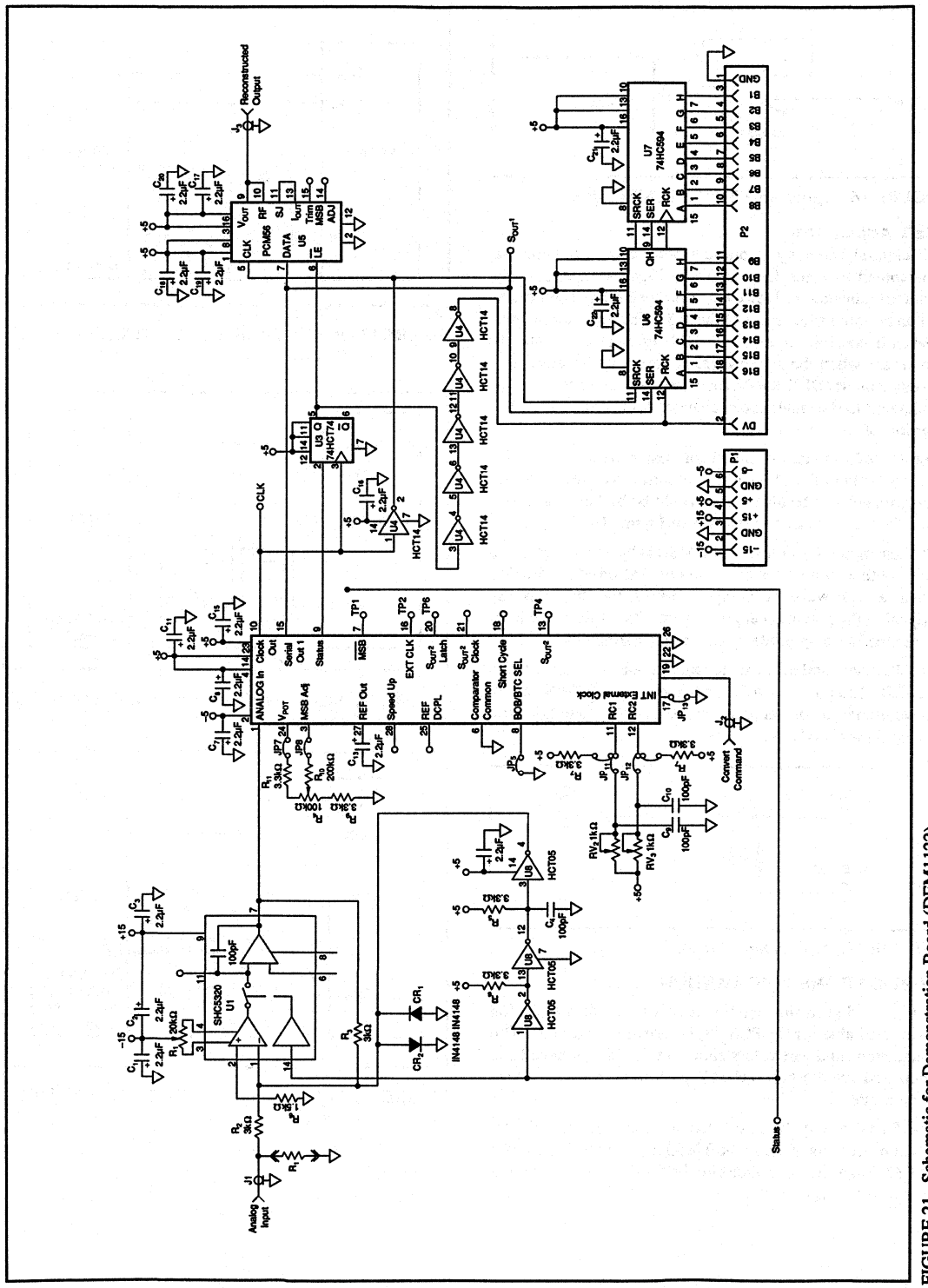


FIGURE 21. Schematic for Demonstration Board (DEM1122).

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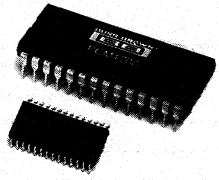


PCM1700U
PCM1700P

Dual 18-Bit Monolithic Audio DIGITAL-TO-ANALOG CONVERTER

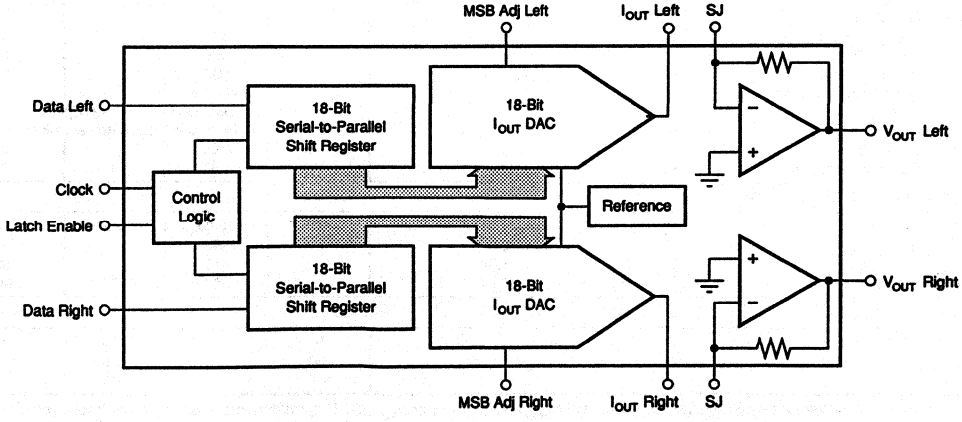
FEATURES

- DUAL 18-BIT LOW-POWER MONOLITHIC AUDIO D/A CONVERTER
- VERY LOW MAX THD+N: –92dB Without External Adjust
- CO-PHASE, GLITCH-FREE ±3V OR ±670µA AUDIO OUTPUTS
- CAPABLE OF 16X PER CHANNEL OVERSAMPLING RATE
- COMPLETE WITH INTERNAL REFERENCE
- SERIAL INPUT FORMAT 100% COMPATIBLE WITH INDUSTRY STD PCM56P
- RUNS ON ±5V SUPPLIES AND DISSIPATES 300mW MAX
- COMPACT 28-PIN PLASTIC DIP OR SOIC

DESCRIPTION

The PCM1700 is a low cost, high-performance, dual 18-bit digital-to-analog converter. The PCM1700 features true glitch-free, co-phase current and voltage outputs and only requires ±5V supplies. The PCM1700 comes complete with an internal reference and optional MSB adjustability for even greater THD performance. Total power dissipation is less than 400mW max. Low maximum Total Harmonic Distortion + Noise (–92dB max; PCM1700P-K) is 100% tested. The very fast PCM1700 is also capable of 16X oversampling rates on both channels simultaneously, providing freedom in output filter selection.

The PCM1700 comes in space-saving 28-pin plastic DIP and SOIC packages. PCM1700 accepts a serial data input format that is compatible with other Burr-Brown PCM products such as the industry standard PCM56P.



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Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL

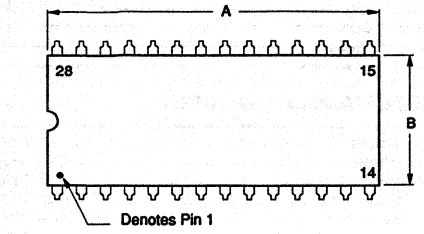
At 25°C, and $\pm V_{CC}$ = ±5.00V unless otherwise noted. Where relevant, specifications apply to both left and right input/output channels.

PARAMETER	CONDITIONS	PCM1700U/U-J/U-K, PCM1700P/P-J/P-K MIN	TYP	MAX	UNITS
RESOLUTION		18			Bits
DYNAMIC RANGE			+108		dB
INPUT					
DIGITAL INPUT					
Logic Family			TTL Compatible		
Logic Level: V_{IH}		+2		$+V_{CC}$	V
V_{IL}		0		–0.8	V
I_{IH}	V_{IH} = +2.7V			+1	µA
I_{IL}	V_{IL} = +0.4V			–50	µA
Data Format			Serial BTC[1]		
Input Clock Frequency				16.9	ns
DYNAMIC CHARACTERISTICS					
TOTAL HARMONIC DISTORTION + N[6]					
PCM1700_:					
f = 991kHz (0dB)	f_S = 705.6kHz[4]		–88	–82	dB
f = 991kHz (–20dB)	f_S = 705.6kHz		–74	–68	dB
f_{IN} = 991kHz (–60dB)	f_S = 705.6kHz		–34	–28	dB
PCM1700_-J:					
f = 991kHz (0dB)	f_S = 705.6kHz		–94	–88	dB
f = 991kHz (–20dB)	f_S = 705.6kHz		–76	–74	dB
f = 991kHz (–60dB)	f_S = 705.6kHz		–36	–34	dB
PCM1700_-K:					
f = 991kHz (0dB)	f_S = 705.6kHz		–98	–92	dB
f = 991kHz (–20dB)	f_S = 705.6kHz		–80	–74	dB
f = 991kHz (–60dB)	f_S = 705.6kHz		–40	–34	dB
CHANNEL SEPARATION		+96	+108		dB
SIGNAL-TO-NOISE RATIO[5]	20Hz to 20kHz at BPZ[6]		+108		dB
TRANSFER CHARACTERISTICS					
ACCURACY					
Gain Error			±1	±3	%
Gain Mismatch	Channel to Channel		±1	±3	%
Bipolar Zero Error			10		mV
BPZ Error Mismatch	Channel to Channel		5		mV
BPZ Differential Linearity Error[7]			±1		LSB
Gain Drift			100		ppm/°C
Bipolar Zero Drift			20		ppm of FSR/°C
Warm-up Time		1			minute
POWER SUPPLY REJECTION	$\pm V_{CC}$ TO V_{OUT}		+86		dB
ANALOG OUTPUT					
Voltage: Output Range			±3		V
Output Impedance			0.1		Ω
Current Output			±8		mA
Capacitive Load Drive	R_{LOAD} = 1.5kΩ		TBD		pF
Short Circuit Duration			Indefinite		
Settling Time			Sufficient to Meet THD + N Specs		
Glitch Energ			Meets All THD + N Specs Without External Output Deglitching		
Current: Output Range	(±2%)		±670		µA
Output Impedance	(±2%)		1.67		kΩ
POWER SUPPLY REQUIREMENTS					
$\pm V_{CC}$ Supply Voltage		+4.75	+5.00	+5.25	V
Supply Current: $+I_{CC}$	$+V_{CC}$ = +5.0V		–40		mA
$-I_{CC}$	$-V_{CC}$ = –5.0V		+16		mA
Power Dissipation	$\pm V_{CC}$ = ±5.0V		280	475	mW
TEMPERATURE RANGE					
Specification		0		+70	°C
Operating		–30		+70	°C
Storage		–60		+100	°C

NOTES: (1) Binary Two's Complement coding. (6) Ratio of (Distortion$_{RMS}$ + Noise$_{RMS}$) / Signal$_{RMS}$. (3) D/A converter input frequency/signal level on both left and right channels. (4) D/A converter sample frequency (8 X 44.1kHz; 8X oversampling per channel). (5) Ratio of Noise$_{RMS}$ / Signal$_{RMS}$. Measured using an A-weighted filter. (6) Bipolar zero. (7) Differential non-linearity at bipolar major carry input code. Measured in 16-bit LSBs. Adjustable to zero error.

MECHANICAL

P Package — 28-Pin Plastic DIP

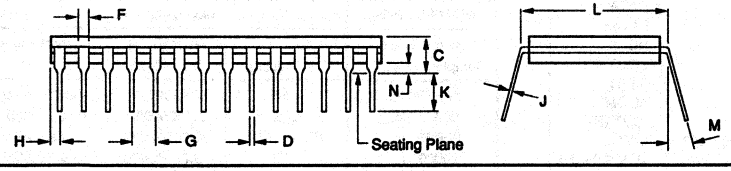


DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.360	1.470	34.54	37.34
B	.500	.550	12.70	13.97
C	—	.200	—	5.08
D	.015	.021	0.38	0.53
F	.030	.070	0.76	1.78
G	.100 BASIC		2.54 BASIC	
H	.030	.095	0.76	2.41
J	.007	.013	0.18	0.33
K	.100	—	2.54	—
L	.600 BASIC		15.24 BASIC	
M	—	15°	—	15°
N	.020	.090	0.51	2.29

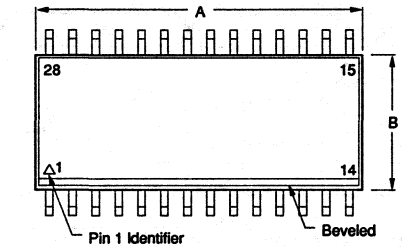
NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers are shown for reference only. Numbers may not be marked on package.

Case: Plastic

Weight: 4.3 grams (0.15oz.)

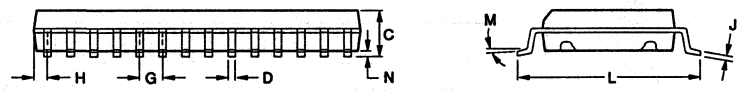


U Package — 28-Pin Plastic SOIC



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.700	.716	17.78	18.19
B	.286	.302	7.26	7.67
C	.093	.109	2.36	2.77
D	.016 BASIC		0.41 BASIC	
G	.050 BASIC		1.27 BASIC	
H	.022	.038	0.56	0.97
J	.008	.012	0.20	0.30
L	.398	.414	10.11	10.52
M	5° TYP		5° TYP	
N	.000	.012	0.00	0.30

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.



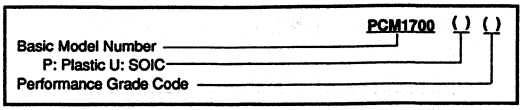
PIN ASSIGNMENTS (Plastic PKG)

PIN	DESCRIPTION	MNEMONIC
1	–5V Analog Supply	$-V_{CC}$
2	Left Channel Servo-Amp Decoupling Point	CAP
3	Left Channel MSB Adjustment	MSB ADJ (L)
4	No Connect	NC
5	Left Channel Bipolar Offset Decoupling Point	CAP
6	Left Channel Current Output	IOUT (L)
7	Left Channel Analog Common	ACOM
8	Left Channel Summing Junction	SJ (L)
9	Left Channel Voltage Output	VOUT (L)
10	No Connect	NC
11	+5V Digital Supply	$+V_{DD}$
12	Left Channel Data Input	DATA
13	Clock Input	CLOCK
14	–5V Logic Supply	$-V_{DD}$
15	Latch Enable Input	LE
16	Right Channel Data Input	DATA (R)
17	Digital Common	DCOM
18	No Connect	NC
19	Right Channel Voltage Output	VOUT (R)
20	Right Channel Summing Junction	SJ (R)
21	Right Channel Analog Common	ACOM
22	Right Channel Current Output	IOUT (R)
23	Right Channel Bipolar Offset Decoupling Point	CAP
24	Right Channel MSB Adjustment	MSB ADJ (R)
25	Right Channel Servo-Amp Decoupling Point	CAP
26	MSB Adjustment Potentiometer Voltage Output	VPOT
27	+5V Analog Supply	$+V_{CC}$
28	Reference Decoupling Point	CAP

PIN ASSIGNMENTS (SOIC PKG)

PIN	DESCRIPTION	MNEMONIC
9	–5V Analog Supply	$-V_{CC}$
10	Left Channel Servo-Amp Decoupling Point	CAP
11	Left Channel MSB Adjustment	MSB ADJ (L)
19	No Connect	NC
12	Left Channel Bipolar Offset Decoupling Point	CAP
13	Left Channel Current Output	I_{OUT} (L)
14	Left Channel Analog Common	ACOM
15	Left Channel Summing Junction	SJ (L)
16	Left Channel Voltage Output	V_{OUT} (L)
17	No Connect	NC
18	+5V Digital Supply	$+V_{DD}$
20	Left Channel Data Input	DATA
21	Clock Input	CLOCK
22	–5V Logic Supply	$-V_{DD}$
23	Latch Enable Input	LE
24	Right Channel Data Input	DATA (R)
25	Digital Common	DCOM
26	No Connect	NC
27	Right Channel Voltage Output	V_{OUT} (R)
28	Right Channel Summing Junction	SJ (R)
1	Right Channel Analog Common	ACOM
2	Right Channel Current Output	I_{OUT} (R)
3	Right Channel Bipolar Offset Decoupling Point	CAP
4	Right Channel MSB Adjustment	MSB ADJ (R)
5	Right Channel Servo-Amp Decoupling Point	CAP
6	MSB Adjustment Potentiometer Voltage Output	V_{POT}
7	+5V Analog Supply	$+V_{DD}$
8	Digital Common	DCOM

ORDERING INFORMATION



ABSOLUTE MAXIMUM RATINGS

DC Supply Voltages	±7.5VDC
Input Logic Voltage	–1V to $+V_{CC}$
Power Dissipation	500mW
Operating Temperature	–25°C to +70°C
Storage Temperature	–60°C to +100°C
Lead Temperature (soldering, 10s)	+300°C

DIGITAL INPUT	ANALOG OUTPUT		
Binary Two's Complement (BTC)	DAC Output	Voltage (V) V_{OUT} Mode	Current (mA) I_{OUT} Mode
1FFFF Hex	+ FS	+2.99997711	–0.66999489
00000 Hex	BPZ	0.00000000	0.00000000
3FFFF Hex	BPZ – 1LSB	–0.00002289	+0.00000511
20000 Hex	– FS	–3.00000000	+0.67000000

TABLE I. PCM1700 Input/Output Relationships.

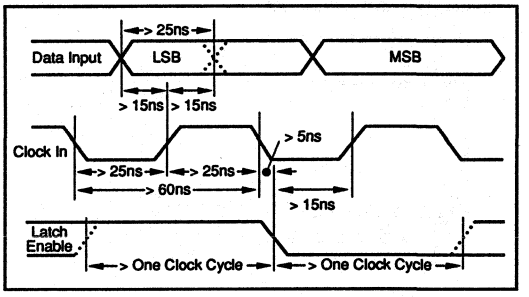


FIGURE 1. PCM1700P Setup and Hold Timing Diagram.

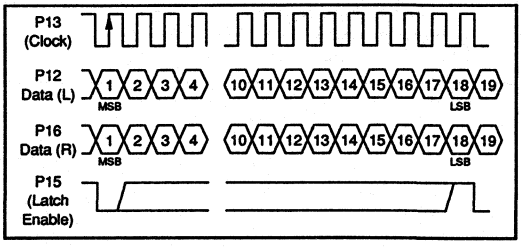


FIGURE 2. Timing Diagram.

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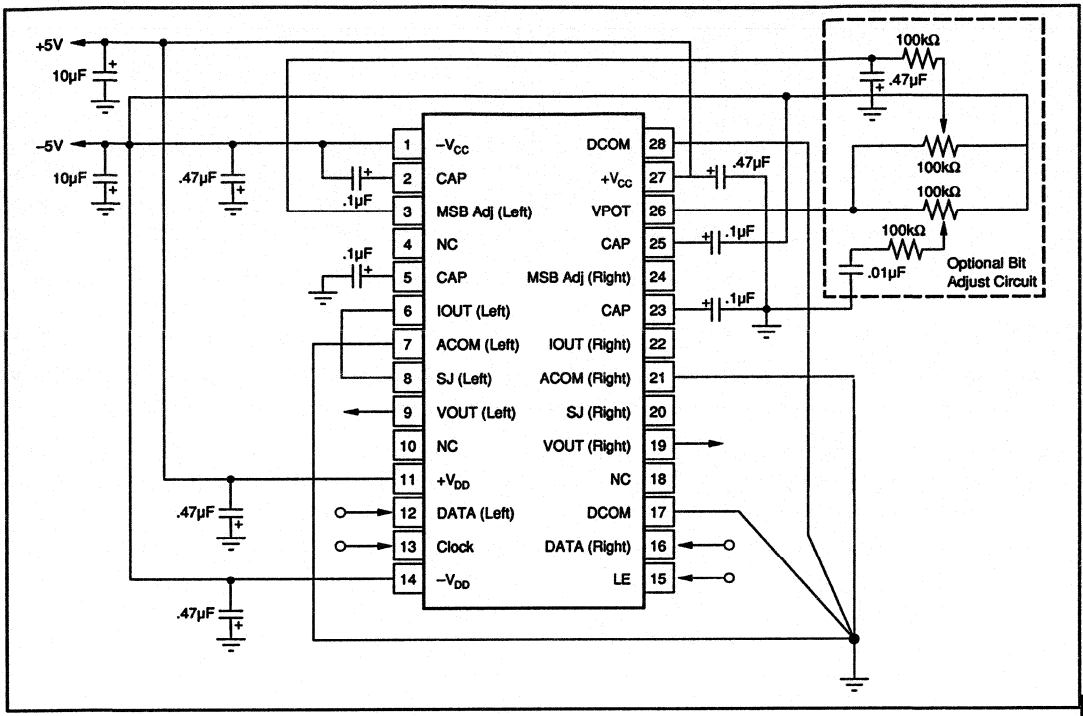

FIGURE 3. Voltage Output Connection Diagram (DIP Package Diagram.)

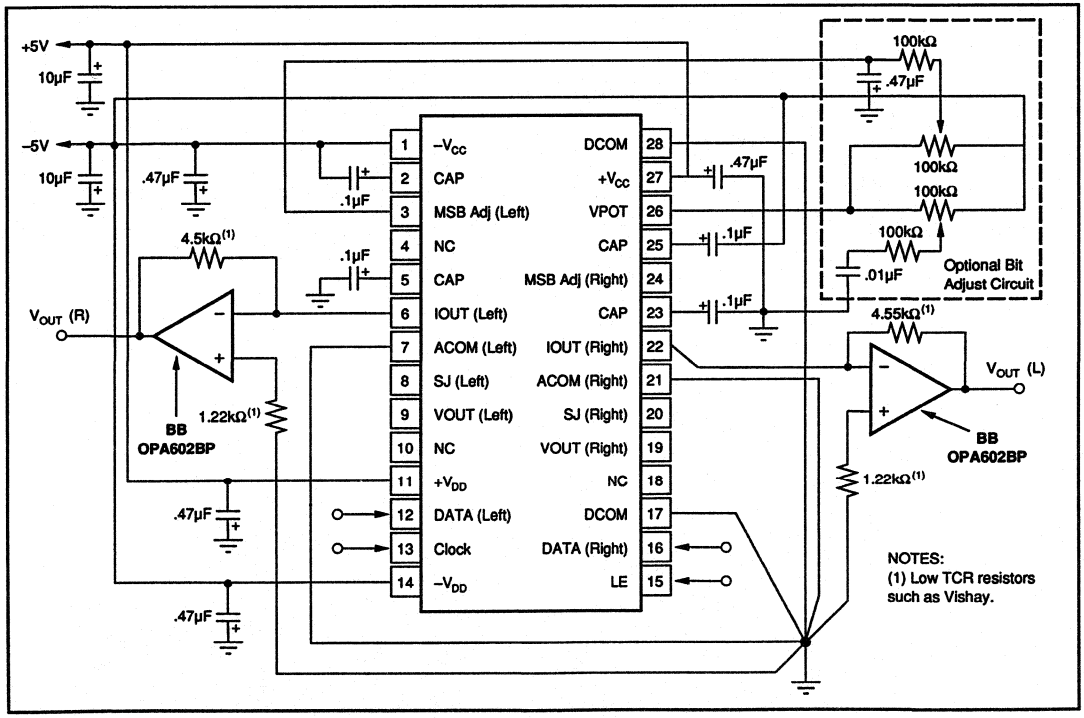

FIGURE 4. Current Output Connection Diagram (DIP Package Diagram.)

10 Voltage-to-Frequency Converters

Voltage-to-frequency converters provide a simple, low-cost way of converting analog signals into digital form. They provide an important alternative to other analog-to-digital conversion techniques. Their integrating input properties make them an appropriate choice when operating in noisy environments. The combination of high accuracy and linearity, low temperature drift, and monotonicity often provides performance characteristics unattainable with other techniques.

Since an analog quantity represented as a frequency is inherently serial data, it is easily handled in large multi-channel systems. Frequency information can be transmitted over long lines with excellent noise immunity using low cost digital line transmitters and receivers. Isolation can be accomplished with optical or transformer couplers without loss in accuracy. Outputs from multiple VFCs can be gated to common counter circuitry with simple digital logic. Low-cost isolation is obtained when a VFC is used together with a DC/DC converter and a single optical coupler.

Burr-Brown monolithic voltage-to-frequency converters provide industry-standard performance and reliability in such applications as precision test and measurement equipment, data acquisition systems, communications equipment, and process control.

The Selection Guide shows parameters for the high grade. Models shown in **boldface** are new products introduced since publication of the previous *Burr-Brown IC Data Book, or Vol. 33b Supplement.*

VOLTAGE-TO-FREQUENCY CONVERTERS

Description	Model	Frequency Range (kHz)	V_{IN} Range (V)	Linearity, max (% of FSR)	Tempco, max (ppm of FSR/°C)	Temp Range[1]	Pkg	Page
Low-Cost Monolithic	VFC32	User-selected 500kHz, max	User-selected	±0.01 at 10kHz ±0.05 at 100kHz	75 typ ±100	Com Ind	DIP, SOIC TO-100,	10-3 10-3
Low-Cost Complete	VFC42 VFC52	0 to 10 0 to 100	0 to +10 0 to +10	±0.01 ±0.05	±100 ±150	Ind Ind	DIP DIP	10-12 10-12
Precision Monolithic	VFC62 **VFC320**	User-selected **User-selected 1MHz max**	User-selected **1MHz max**	±0.002 at 10kHz **±0.002 at 10kHz**	±20 **±20**	Ind **Ind**	DIP, **TO-100**	10-18 **S-10.33**
Synchronized Monolithic	**VFC100**	**Clock Programmed 2MHz max**	**0 to +10**	**0.1 at 1MHz**	**±50**	**Ind**	**DIP**	**S-10.2**
	VFC101	Clock Programmed, 2MHz max	0 to +10, 0 to +5, 0 to +8, –5 to +5	±0.02 at 100kHz	±40	Ind	PLCC	10-41
High-Performance	**VFC110**	**User-selected 4MHz max**	**0 to +10**	**±0.05 at 1MHz**	**±50**	**Ind**	**DIP,**	**S-10.17**
Single Supply, Low Power	**VFC121**	**User-selected 1.5MHz max**	**User-selected**	**±0.03 at 100kHz**	**±40**	**Ind**	**DIP**	**S-10.25**

NOTES: (1) Com = 0°C to +70°C, Ind = –25°C to +85°C.

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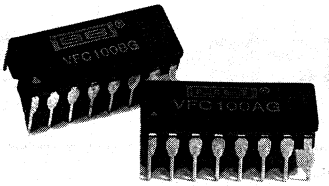


VFC100

Synchronized VOLTAGE-TO-FREQUENCY CONVERTER

FEATURES

- FULL-SCALE FREQUENCY SET BY SYSTEM CLOCK; NO CRITICAL EXTERNAL COMPONENTS REQUIRED
- PRECISION 10V FULL-SCALE INPUT, 0.5% max GAIN ERROR
- ACCURATE 5V REFERENCE VOLTAGE
- EXCELLENT LINEARITY:
  0.02% max at 100kHz FS
  0.1% max at 1MHz FS
- VERY LOW GAIN DRIFT: 50ppm/°C

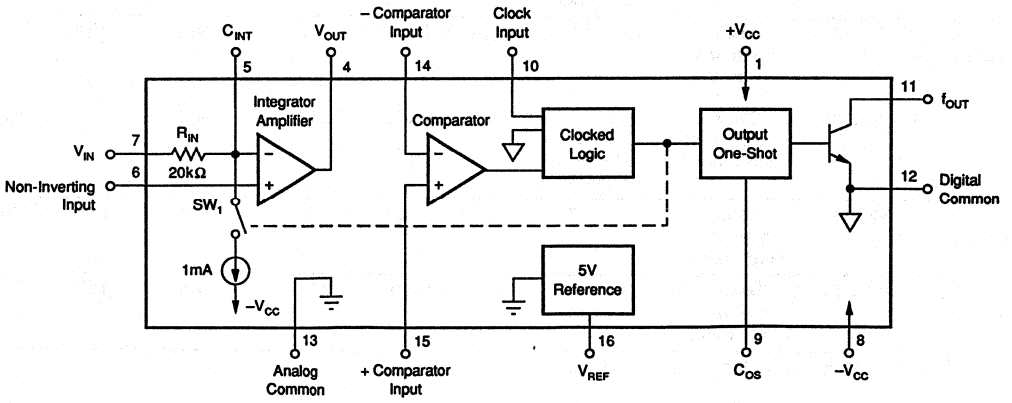
APPLICATIONS

- A/D CONVERSION
- PROCESS CONTROL
- DATA ACQUISITION
- VOLTAGE ISOLATION

DESCRIPTION

The VFC100 voltage-to-frequency converter is an important advance in VFCs. The well-proven charge balance technique is used; however, the critical reset integration period is derived from an external clock frequency. The external clock accurately sets an output full-scale frequency, eliminating error and drift from the external timing components required for other VFCs. A precision input resistor is provided which accurately sets a 10V full-scale input voltage. In many applications the required accuracy can be achieved without external adjustment.

The open collector active-low output provides fast fall time on the important leading edge of output pulses, and interfaces easily with TTL and CMOS circuitry. An output one-shot circuit is particularly uesful to provide optimum output pulse widths for optical couplers and transformers to achieve voltage isolation. An accurate 5V reference is also provided which is useful for applications such as offsetting for bipolar input voltages, exciting bridges and sensors, and autocalibration schemes.



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PDS-547E

SPECIFICATIONS

ELECTRICAL

At T_A = +25°C and ±15VDC supplies unless otherwise noted.

PARAMETER	CONDITIONS	VFC100AG MIN	VFC100AG TYP	VFC100AG MAX	VFC100BG MIN	VFC100BG TYP	VFC100BG MAX	UNITS
TRANSFER FUNCTION								
Voltage-to-Frequency Mode	$f_{OUT} = f_{CLOCK} \times (V_{IN}/20V)$							
Gain Error[1]	FSR = 100kHz		±0.5	±1		±0.2	±0.5	% of FSR[4]
Linearity Error	FSR = 100kHz, Over Temperature		±0.01	±0.025		*	±0.02	% of FSR
	FSR = 500kHz, C_{OS} = 60pF		±0.015			*	±0.05	% of FSR
	FSR = 1MHz, C_{OS} = 60pF		±0.025			*	±0.1	% of FSR
Gain Drift[2]	FSR = 100kHz		±70	±100		±30	±50	ppm of FSR/°C
Referred to Internal V_{REF}			±70	±100		±30	±50	ppm of FSR/°C
Offset Referred to Input			±1	±3		±1	±2	mV
Offset Drift			±12	±100		±6.5	±25	µV/°C
Power Supply Rejection	Full Supply Range			0.01			*	%/V
Response Time	To Step Input Change	One Period of New Output Frequency Plus One Clock Period						
Current-to-Frequency Mode	$f_{OUT} = f_{CLOCK} \times (I_{IN}/1mA)$							
Gain Error			±0.5	±1		±0.2	±0.5	% of FSR
Gain Drift[2]			±120	±200		±80	±140	ppm of FSR/°C
Frequency-to-Voltage Mode[3]	$V_{OUT} = 20V \times (f_{IN}/f_{CLOCK})$							
Gain Accuracy[1]	FSR = 100kHz		±0.5	±1		±0.2	±0.5	%
Linearity	FSR = 100kHz		±0.01	±0.025		*	±0.02	%
Input Resistor (R_{IN})								
Resistance		19.8	20	20.2	*	*	*	kΩ
Temperature Coefficient (T_C)[2]			±50	±100		*	*	ppm/°C
INTEGRATOR OP AMP								
V_{OS}[1]			±150	±1000		*	*	µV
V_{OS} Drift			±5			*		µV/°C
I_B			±50	±100		±25	±50	nA
I_{OS}			100	200		50	100	nA
A_{OL}	Z_{LOAD} = 5kΩ/10,000pF	100	120		*	*		dB
CMRR		80	105		*	*		dBV
CM Range		–7.5		+0.1	*		*	V
V_{OUT} Range	Z_{LOAD} = 5kΩ/10,000pF	–0.2		+12		*	*	V
Bandwidth			14			*		MHz
COMPARATOR INPUTS								
Input Current (Operating)	$-11V < V_{COMPARATOR} < +V_{CC} - 2V$			5			*	µA
CLOCK INPUT								
(Referred to Digital Common)								
Frequency (Maximum Operating)			4			*		MHz
Threshold Voltage			1.4			*		V
	Over Temperature	0.8		2	*		*	V
Voltage Range (Operating)		$-V_{CC}$ + 2V		$+V_{CC}$	*		*	V
Input Current	$-V_{CC} < V_{CLOCK} < +V_{CC}$		0.5	5		*	*	µA
Rise Time				2			*	µs
OPEN COLLECTOR OUTPUT								
(Referred to Digital Common)								
V_{OL}	I_{OUT} = 10mA			0.4			*	V
I_{OL}				15			*	mA
I_{OH} (Off Leakage)	V_{OH} = 30V		0.01	10		*	*	µA
Delay Time, Positive Clock Edge to Output Pulse			300			*		ns
Fall Time			100			*		ns
Output Capacitance			5			*		pF
OUTPUT ONE-SHOT	Nominal PW_{OUT} = (5ns/pF) x C_{OS} – 90ns							
Pulse Width Out	C_{OS} = 300pF	1	1.4	2	*	*	*	µs
REFERENCE VOLTAGE								
Accuracy	No Load	4.9	5	5.1	4.95	*	5.05	V
Drift[2]			±60	±150		±40	±100	ppm/°C
Current Output	Sourcing Capability	10				*		mA
Power Supply Rejection				0.015			0.015	%/V
Output Impedance			0.5	2		*	*	Ω

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ELECTRICAL (CONT)

At T_A = +25°C and ±15VDC supplies unless otherwise noted.

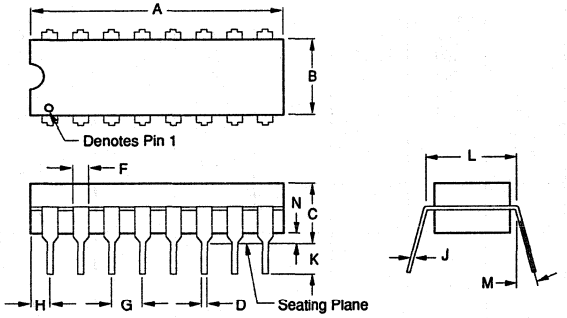
PARAMETER	CONDITIONS	VFC100AG MIN	VFC100AG TYP	VFC100AG MAX	VFC100BG MIN	VFC100BG TYP	VFC100BG MAX	UNITS
POWER SUPPLY								
Rated Voltage			±15			*		V
Operating Voltage Range (See Figure 9)	$+V_{CC}$	+7.5		+28.5	*		*	V
	$-V_{CC}$	–7.5		–28.5	*		*	V
Total Supply	$+V_{CC} - (-V_{CC})$	15		36	*		*	V
Digital Common		$-V_{CC}$ + 2		$+V_{CC}$ – 4	*		*	V
Quiescent Current: $+I_{CC}$	Over Temperature		10.6	15		*	*	mA
$-I_{CC}$			9.6	15		*	*	mA
TEMPERATURE RANGE								
Specification		–25		+85	*		*	°C
Storage		–65		+150	*		*	°C
θ_{JA}			150			*		°C/W
θ_{JC}			100			*		°C/W

* Specification same as AG grade.

NOTES: (1) Offset and gain error can be trimmed to zero. See text. (2) Specified by the box method: (max. – min.) + (FSR x ΔT). (3) Refer to detailed timing diagram in Figure 16 for frequency input signal timing requirements. (4) FSR = Full Scale Range.

MECHANICAL

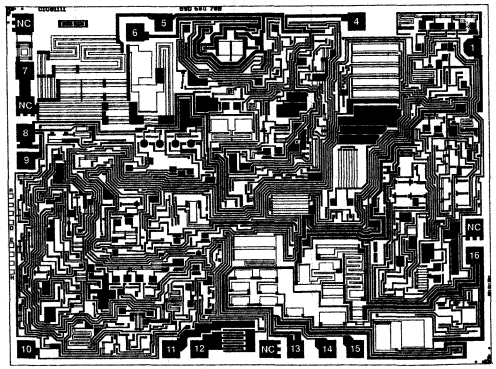
G Package — 16-Pin Ceramic DIP



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.760	.885	19.30	22.48
B	.220	.280	5.59	7.11
C	—	.200	—	5.08
D	.015	.023	0.38	0.58
F	.030	.070	0.76	1.78
G	.100 BASIC		2.54 BASIC	
H	.030	.095	0.76	2.41
J	.008	.015	0.20	0.38
K	.100	—	2.54	—
L	.300 BASIC		7.62 BASIC	
M	—	15°	—	15°
N	.020	.050	0.51	1.27

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

DICE INFORMATION



VFC100 DIE TOPOGRAPHY

PAD	FUNCTION	PAD	FUNCTION
1	$+V_{CC}$	9	C_{OS}
2	NC	10	Clock Input
3	NC	11	f_{OUT}
4	Integrator Out	12	Digital Common
5	C_{INT}	13	Analog Common
6	Noninverting In	14	–Comparator In
7	V_{IN}	15	+Comparator In
8	$-V_{CC}$	16	V_{REF}

NC: No Connection

Substrate Bias: Electrically connected to –V supply.

MECHANICAL INFORMATION

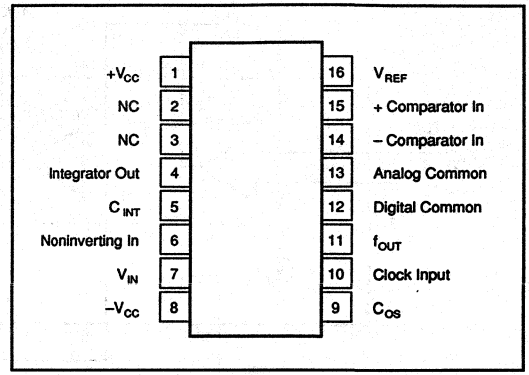
	MILS (0.001")	MILLIMETERS
Die Size	141 x 107 ±5	3.58 x 2.72 ±0.13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.1 x 0.1
Backing	Gold	

See "DICE PRODUCTS" Section 17 in Data Book Supplement Volume 33c, or contact Burr-Brown for current information.

ABSOLUTE MAXIMUM RATINGS

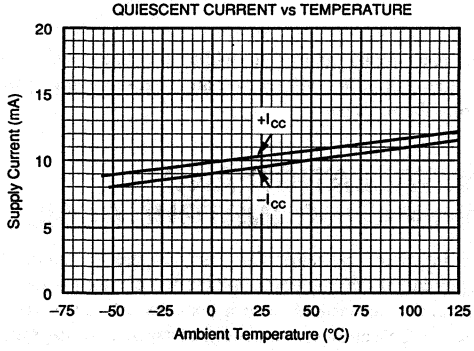
Power Supply Voltage ($+V_{CC}$ to $-V_{CC}$)	36V
$+V_{CC}$ to Analog Common	28V
$-V_{CC}$ to Analog Common	28V
Integrator Out Short-Circuit to Ground	Indefinite
Integrator Differential Input	±10V
Integrator Common-Mode Input	$-V_{CC}$ +5V to +2V
V_{IN} (pin 7)	$\pm V_{CC}$
Clock Input	$\pm V_{CC}$
V_{REF} Out Short-Circuit to Ground	Indefinite
Pin 9 (C_{OS})	0 to $+V_{CC}$
f_{OUT} (referred to digital common)	–0.5V to 36V
Digital Common	$\pm V_{CC}$
Storage Temperature Range	–65°C to +150°C
Lead Temperature (soldering, 10s)	300°C

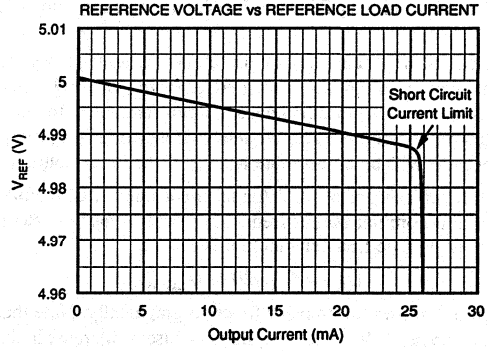
PIN CONFIGURATION



TYPICAL PERFORMANCE CURVES

At +25°C, $\pm V_{CC}$ = 15VDC, and in circuit of Figure 1.





THEORY OF OPERATION

The VFC100 monolithic voltage-to-frequency converter provides a digital pulse train output with an average frequency proportional to the analog input voltage. The output is an active low pulse of constant duration, with a repetition rate determined by the input voltage. Falling edges of the output pulses are synchronized with rising edges of the clock input.

Operation is similar to a conventional charge balance VFC. An input operational amplifier (Figure 1) is configured as an integrator so that a positive input voltage causes an input current to flow in R_{IN}. This forces the integrator output to ramp negatively. When the output of the integrator crosses the reference voltage (5V), the comparator trips, activating the clocked logic circuit. Once activated, the clocked logic awaits a falling edge of the clock input, followed by a rising edge (see Figure 2). On the rising edge, switch S_1 is closed for one complete clock cycle, causing the reset current, I_1, to switch to the integrator input. Since I_1 is larger than the input current, I_{IN}, the output of the integrator ramps positively during the one clock cycle reset period. The clocked logic circuitry also generates a VFC output pulse during the reset period.

Unlike conventional VFC circuits, the VFC100 accurately derives its reset period from an external clock frequency. This eliminates the critical timing capacitor required by other VFC circuits. One period (from rising edge to rising edge) of the clock input determines the integrator reset period.

When the negative-going integration of the input signal crosses the comparator threshold, integration of the input signal will continue until the reset period can start (awaiting

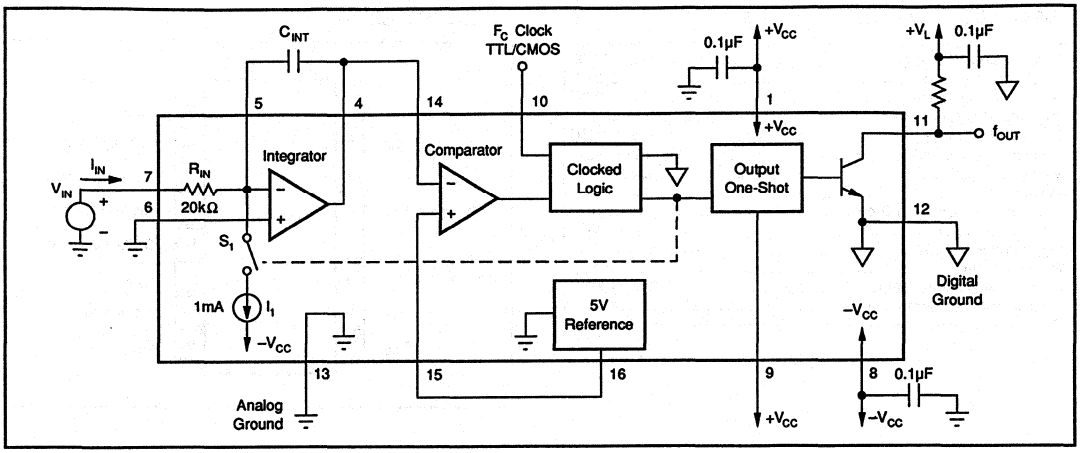


FIGURE 1. Circuit Diagram for Voltage-to-Frequency Mode.

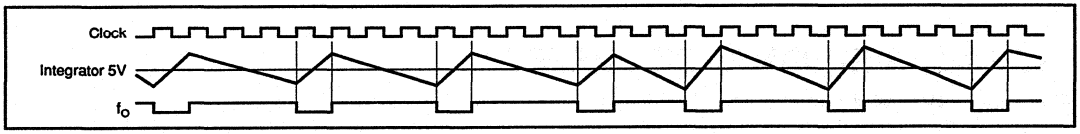


FIGURE 2. Timing Diagram for Voltage-to-Frequency Mode.

the necessary transitions of the clock). Output pulses are thus made to align with rising edges of the external clock. This causes the instantaneous output frequency to be a subharmonic of the clock frequency. The average frequency, however, will be an accurate analog of the input voltage.

A full scale input of 10V (or an input current of 0.5mA) causes a nominal output frequency equal to half the clock frequency. The transfer function is

$$f_{OUT} = (V_{IN}/20V)\ f_{CLOCK}.$$

Figure 3 shows the transfer function graphically. Note that inputs above 10V (or 0.5mA) do not cause an increase in the output frequency. This is an easily detectable indication of an overrange input. In the overrange condition, the integrator amplifier will ramp to its negative output swing limit. When the input signal returns to within the linear range, the integrator amplifier will recover and begin ramping upward during the reset period.

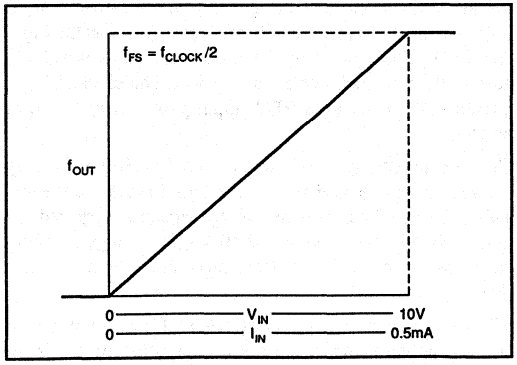


FIGURE 3. Transfer Function for Voltage-to-Frequency Mode.

INSTALLATION AND OPERATING INSTRUCTIONS

The integrator capacitor C_{INT} (see Figure 1) affects the magnitude of the integrator voltage waveform. Its absolute accuracy is not critical since it does not affect the transfer function. This allows a wide range of capacitance to produce excellent results. Figure 4 facilitates choosing an appropriate

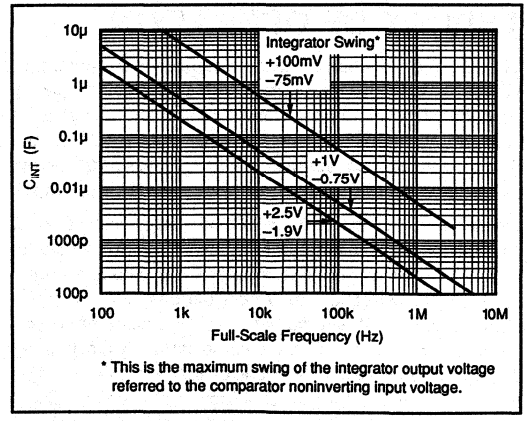


FIGURE 4. Integrator Capacitor Selection Graph.

standard value to assure that the integrator waveform voltage is within acceptable limits. Good dielectric absorption properties are required to achieve best linearity. Mylar®, polycarbonate, mica, polystyrene, Teflon® and glass types are appropriate choices. The choice in a given application will depend on the particular value and size considerations. Ceramic capacitors vary considerably from type to type and some produce significant nonlinearities. Polarized capacitors should not be used.

Deviation from the nominal recommended +1V to –0.75V integrator voltage (as controlled by the integrator capacitor value) is permissible and will have a negligible effect on VFC operation. Certain situations may make deviations from the suggested integrator swing highly desirable. Smaller integrator voltages, for instance, allow more "headroom" for averaging noisy input signals. The VFC is a fully integrating input converter, able to reject large levels of interfering noise. This ability is limited only by the output voltage swing range of the integrator amplifier. By setting a small integrator voltage swing using a large C_{INT} value, larger levels of noise can be integrated without integrator output saturation and loss of accuracy. For instance, with a 50kHz full-scale output and C_{INT} = 0.1µF, the circuit in Figure 1 can accurately average an input through the full 0 to 10V input range with 1Vp-p superimposed 60Hz noise.

The integrator output voltage should not be allowed to exceed +12V or –0.2V, otherwise saturation of the operational amplifier could cause inaccuracies. Operation with positive power supplies less than +15V will limit the output swing of the integrator operational amplifier. Smaller integrator voltage waveforms may be required to avoid output saturation of the integrator amplifier. See "Power Supply Considerations" for information on low voltage operation.

The maximum integrator voltage swing requirement is nearly symmetrical about the comparator threshold voltage (see Figure 12). One-third greater swing is required above the threshold than below it. Maximum demand on positive integrator swing occurs at low scale, while the negative swing is greatest just below full scale.

CLOCK INPUT

The clock input is TTL and CMOS-compatible. Its input threshold is approximately 1.4V (two diode voltage drops) referenced to digital ground (pin 12). The clock "high" input may be standard TLL or may be as high as $+V_{CC} - 2V$. A CMOS clock should be powered from a voltage source at least 2V below the VFC100's $+V_{CC}$ to prevent overdriving the clock input. Alternatively, a resistive voltage divider may be used to limit the clock voltage swing to $+V_{CC} - 2V$ maximum. The clock input has a high input impedance, so no special drivers are required. Rise time in the transition region from 0.8V to 2V must be less than 2µs for proper operation.

OUTPUT

The frequency output is an open collector current-sink transistor. Output pulses are active low such that the output transistor is on only during the reset integration period (see "Shortened Output Pulses"). This minimizes power dissipation over the full frequency range and provides the fastest logic edge at the beginning of the output pulse, where it is most desirable.

Interface to a logic circuit would normally be made using a pull-up resistor to the logic power supply. Selection of the pull-up resistor should be made such that no more than 15mA flows in the output transistor. The actual choice of the pull-up resistor may depend on the full-scale frequency and the stray capacitance on the output line. The rising edge of an output pulse is determined by the RC time constant of the pull-up resistor and the stray capacitance. Excessive capacitance will produce a rounding of the output pulse rising edge, which may create problems driving some logic circuits. If long lines must be driven, a buffer or digital line transmitter circuit should be used.

The synchronized nature of the VFC100 makes viewing its output on an oscilloscope somewhat tricky. Since all output pulses align with the clock, it is best to trigger and view the clock on one of the input channels; the output can then be viewed on another oscilloscope channel. Depending on the VFC input voltage, the output waveform may appear as if the oscilloscope is not properly triggered. The output might best be visualized by imagining a constant output frequency which is locked to a submultiple of the clock frequency with occasional extra pulses or missing pulses to create the necessary average frequency. It is these extra or missing pulses that make the output waveform appear as if the oscilloscope is not properly triggered. This is normal. Experimentation with the input voltage and oscilloscope triggering generally allows a stable view of the output and provides an understanding of its nature.

SHORTENED OUTPUT PULSES

In normal operation, the negative output pulse duration is equal to one period of the clock input. Shorter output pulses may be useful in driving optical couplers or transformers for voltage isolation or noise rejection. This can be accomplished by connecting capacitor C_{OS} as shown in Figure 5. Pin 9 may be connected to $+V_{CC}$, deactivating the output one-shot circuit. The value of C_{OS} is chosen according to the curve in Figure 6. Output pulses cannot be made to exceed one clock period in duration. Thus, a C_{OS} value which would create an output pulse which is longer than one period of the clock will have the same effect as disabling the one-shot, causing the output pulse to last one clock period. The minimum practical pulse width of the one-shot circuit is approximately 100ns. Using C_{OS} to generate shorter output pulses does not affect the output frequency or the gain equation.

REFERENCE VOLTAGE

Excellent gain drift is achieved by use of a precision internal 5V reference. This reference is brought to an external pin and can be used for a variety of purposes. It is used to offset the noninverting comparator input in voltage-to-frequency mode (although a precise voltage is not required for this function). The reference is very useful for handling bipolar

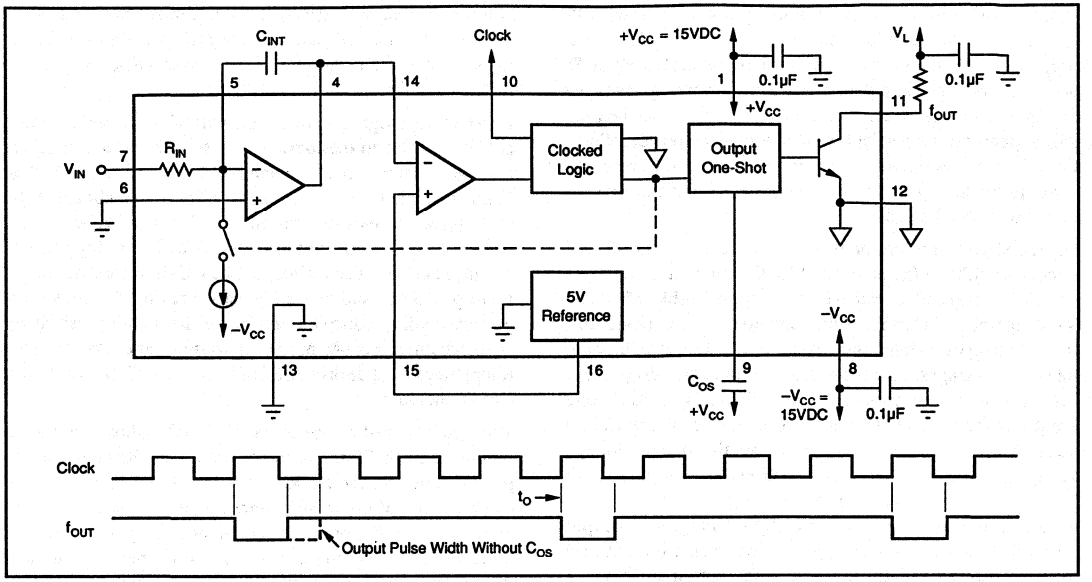


FIGURE 5. Circuit and Timing Diagram for Shortened Output Pulses.

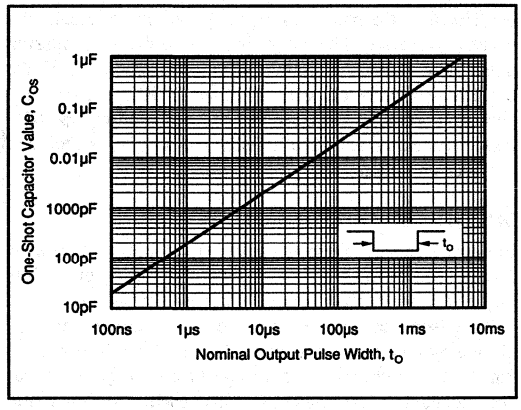


FIGURE 6. Output One-Shot Capacitor Selection.

input signals in many other applications, such as offsetting the input. It can source up to 10mA and sink 100µA. Heavy loading of the reference will change the gain of the VFC and affect the external reference voltage. For instance, a 10mA load interacting with a 0.5Ω typical output impedance will change the VFC gain equation and reference voltage by 0.1%.

Figure 7 shows the reference used to offset the VFC transfer function, to convert a –5V to +5V input to 0–500kHz output. The circuit in Figure 8 uses the reference to excite a 300Ω bridge transducer. R_1 provides the majority of the current to the bridge while the V_{REF} output supplies the balance and accurately controls the bridge voltage. The VFC gain is inversely proportional to the reference voltage, V_{REF}. Since the bridge gain is directly proportional to its excitation voltage, the two equal and opposite effects cancel the effect of reference voltage drift on gain.

The reference output amplifier is specifically designed for excellent transient response, to provide precision in a noisy environment.

OTHER INPUT VOLTAGE RANGES

The internal input resistor, R_{IN} = 20kΩ, sets a full-scale input of 10V. Other input ranges can be created by using an external gain set resistor connected to pin 5. Since the excellent temperature drifts of the VFC100 are achieved by careful matching of internal temperature coefficients, use of an external gain set resistor will generally degrade this drift. Using an external resistor to set the gain, the resulting gain drift would be equal to the sum of the external resistor drift and the specified current gain drift of the VFC100. Different voltage input ranges are best implemented by using the internal input resistor, R_{IN}, in series or parallel with a high quality external resistor, thus maintaining as much of the precision temperature tracking as possible.

For best drift performance, the adjustment range of a fine gain trim should be made as narrow as practical. R_1 and R_2 in Figure 9 allow gain adjustments over a ±1% range (adequate to trim the 100kHz FS gain error to zero) and will not significantly affect the drift performance of the VFC100. R_3, R_4 and R_5 allow trimming of the integrator amplifier input offset voltage. The adjustment range is determined by the ratio of R_4 to R_5. Accurate end-point calibration would be performed by first adjusting the offset trim so that zero volts input just causes all output pulses to cease. The gain trim is then adjusted for the proper full-scale output frequency with an accurate full-scale input voltage.

A different input voltage range could also be made by using only a portion of the normal input range of the VFC. For instance, a 2V full-scale input could be created by using the

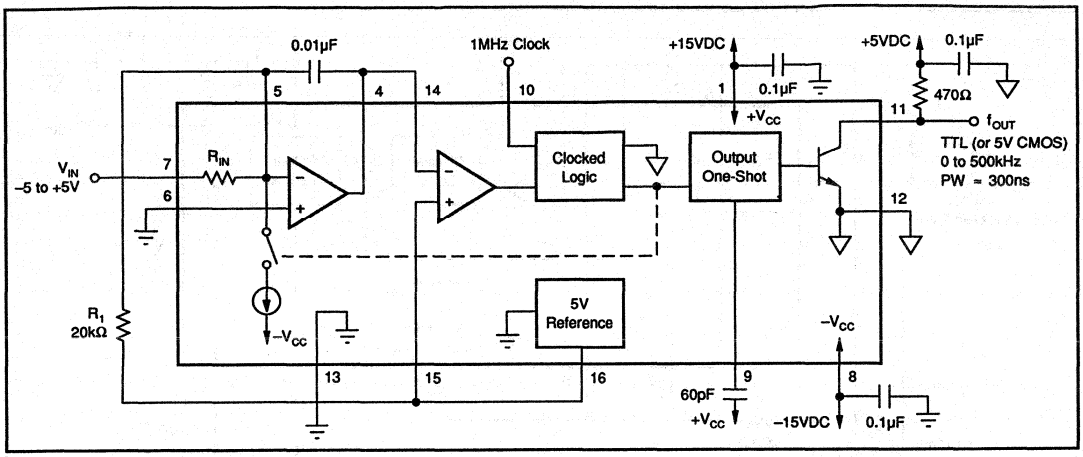


FIGURE 7. Circuit Diagram for Bipolar Input Voltages.

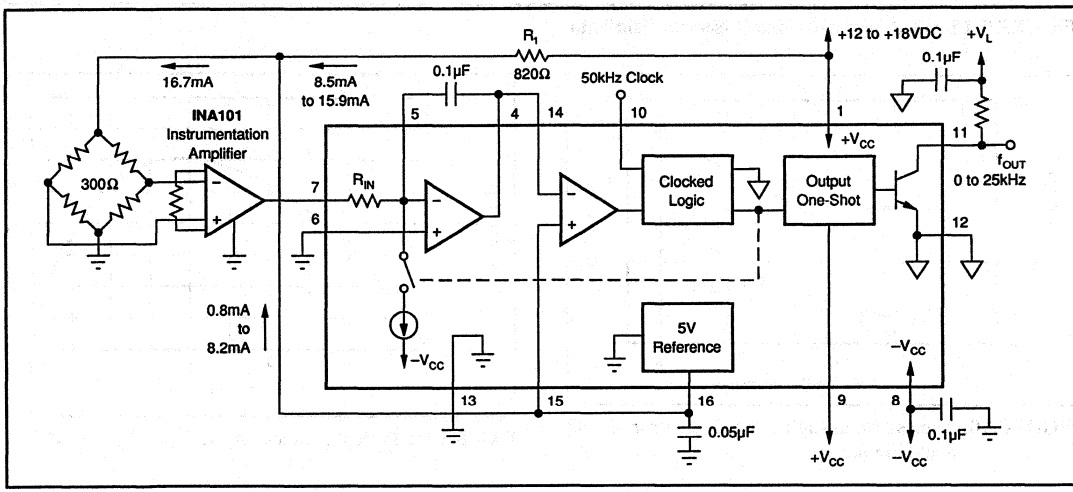


FIGURE 8. Circuit Diagram for Bridge Excitation Using V_{REF}.

internal input resistor and a clock frequency of 10 times the desired full-scale output frequency.

LINEARITY PERFORMANCE

The linearity of the VFC100 is specified as the worst-case deviation from a straight line defined by low scale and high scale end point measurements. This worst-case deviation is expressed as a percentage of the 10V full-scale input. All units are tested and guaranteed for the specified level of performance.

Linearity performance and gain error change with full-scale operating frequency as shown in Figure 10. Figure 11 shows the typical shape of the nonlinearity at 100kHz full scale. Integrator voltage swing (determined by C_{INT}) has a minor effect on linearity. A small integrator voltage swing typically leads to best linearity performance.

The best linearity performance at high full-scale frequencies (above 500kHz) is obtained by using short output pulses with a one-shot capacitor of 60pF. As with any high-frequency circuit, careful attention to good power supply bypassing techniques (see "Power Supplies and Grounding") is also required.

TEMPERATURE DRIFT

Conventional VFC circuits are affected significantly by external component temperature drift. Drift of the external input resistor and timing capacitor required with these devices may easily exceed the specified drift of the VFC itself.

When used with its internal input resistor, the gain drift of the complete VFC100 circuit is totally determined by the performance of the VFC100. Gain drift is specified at a full-scale output frequency of 100kHz. Conventional VFC circuits usually specify drift at 10kHz and degrade significantly

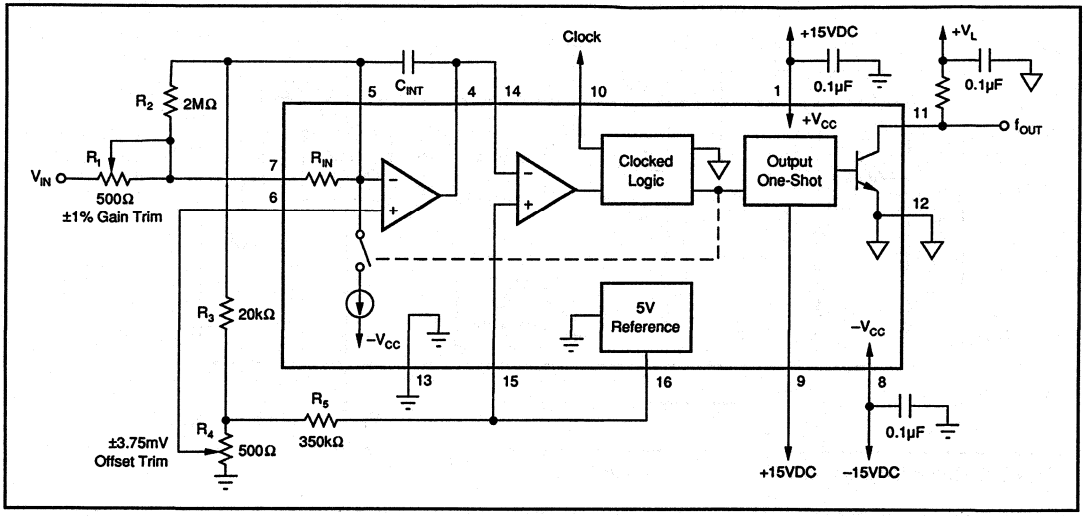


FIGURE 9. Circuit Diagram for Fine Offset and Gain Trim.

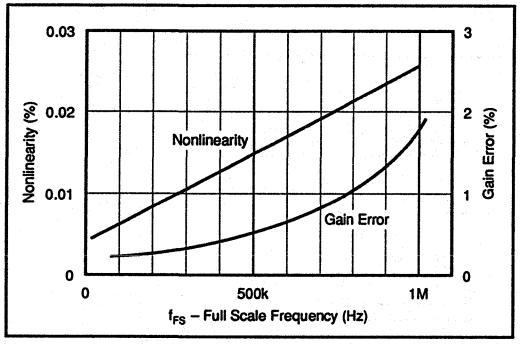


FIGURE 10. Typical Nonlinearity and Gain Error vs Full Scale Frequency.

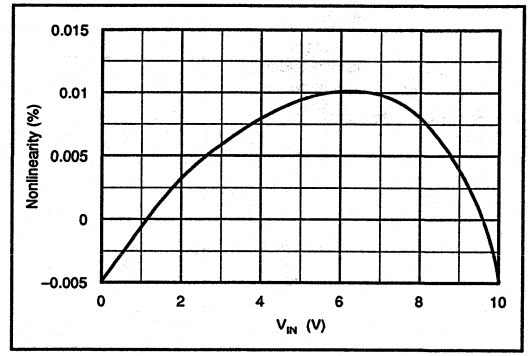


FIGURE 11. Typical Nonlinearity vs V_{IN}. (f_{FS} = 0.1MHz)

at higher operating frequency. The VFC100's gain drift remains excellent at higher operating frequency, typically remaining within specifications at f_{FS} = 1MHz.

Drift of the external clock frequency directly affects the output frequency, but by using a common clock for the VFC and counting circuitry, this drift can be cancelled (see "Counting the Output").

POWER SUPPLIES AND GROUNDING

Separate analog and digital grounds are provided on the VFC100 and it is important to separate these grounds to attain greatest accuracy. Logic sink current flowing in the f_{OUT} pin is returned to the digital ground. If this "noisy" current were allowed to flow in analog ground, errors could be created. Although analog and digital grounds may eventually be connected together at a common point in the circuitry, separate circuit connections to this common point can reduce the error voltages created by varying currents flowing through the ground return impedance. The +5V V_{REF} pin is referenced to analog ground.

The power supplies should be well bypassed using capacitors with low impedance at high frequency. A value of 0.1µF is adequate for most circuit layouts.

The VFC100 is specified for a nominal supply voltage of ±15V. Supply voltages ranging from ±7.5V to ±18V may be used. Either supply can be up to 28V as long as the total of both does not exceed 36V. Steps must be taken, however, to assure that the integrator output does not exceed its linear range. Although the integrator output is capable of 12V output swing with 15V power supplies, with 7.5V supplies, output swing will be limited to approximately 4.5V. In this case, the comparator input cannot be offset by directly connecting to the 5V reference output pin. The comparator input must be connected to a lower voltage point (approximately 2V). This allows the integrator output to operate around a lower voltage point, assuring linear operation. This threshold voltage does not affect the accuracy or drift of the VFC as long as it is not noisy. It should not be made too

small, however, or the negative output limitation of the integrator (–0.2V) may cause saturation. Additionally, a large integrator capacitor may be used to limit the required integrator waveform swing to approximately 100mV (see "Integrator Capacitor").

Figure 12 shows a circuit for operating from the minimum power supplies, avoiding saturation of the integrator amplifier and loss of accuracy. C_{INT} is chosen for a +100mV to –75mV integrator voltage swing (referred to the noninverting comparator input). The offset voltage applied to the comparator's noninverting input is derived from a resistive voltage divider from V_{REF}.

The relationship of the allowable operating voltage ranges on important pins is show in Figure 13. Note that the integrator amplifier output cannot swing more than 0.2V below ground. Although this is not "normal" for an operational amplifier, a special internal design of this type optimizes high frequency performance. It is this characteristic which necessitates the offsetting of the noninverting comparator input in voltage-to-frequency mode to avoid negative output swing.

COUNTING THE OUTPUT

In evaluation and use of the VFC100, you may want to measure the output frequency with a frequency counter. Since synchronization of the VFC100 causes it to await a clock edge for any given output pulse, the output frequency is essentially quantized. The quantized steps are equal to one clock period of the counting gate period. The quantizing error can be made arbitrarily small by counting with long gate times. For instance, a one-second counter gate period with a 100kHz full-scale frequency has a resolution of one part in 100,000. Many of the more sophisticated laboratory frequency counters, however, use period measurement schemes to count the input frequency quickly. These instruments work equally well, but the gate period must be set appropriately to achieve the desired count resolution. Short gate periods will produce many digits of "accuracy" in the display, but the results may be very inaccurate.

Figure 14 is a typical system application showing a basic counting technique. A 0 to 10V input is converted to a 0 to 100kHz frequency output. The VFC's clock is divided by M = 4000 to produce a gate period for the counter circuit. The resulting VFC count, N, is insensitive to variations in the actual clock frequency. The input voltage represented by the resulting count is V_{IN} = (N/M) 20V.

Resolution is related to the number of counts at full scale, or half the number of clock pulses in the gate period.

The integrating nature of the VFC is important in achieving accurate conversions. The integrating period is equal to the counting period. This can be used to great advantage to reject unwanted signals of a known frequency. Figure 15 shows that response nulls occur at the inverse of the integration period and its multiples. If 60Hz is to be rejected, for instance, the counting period should be made equal to, or a multiple of, 1/60 of a second.

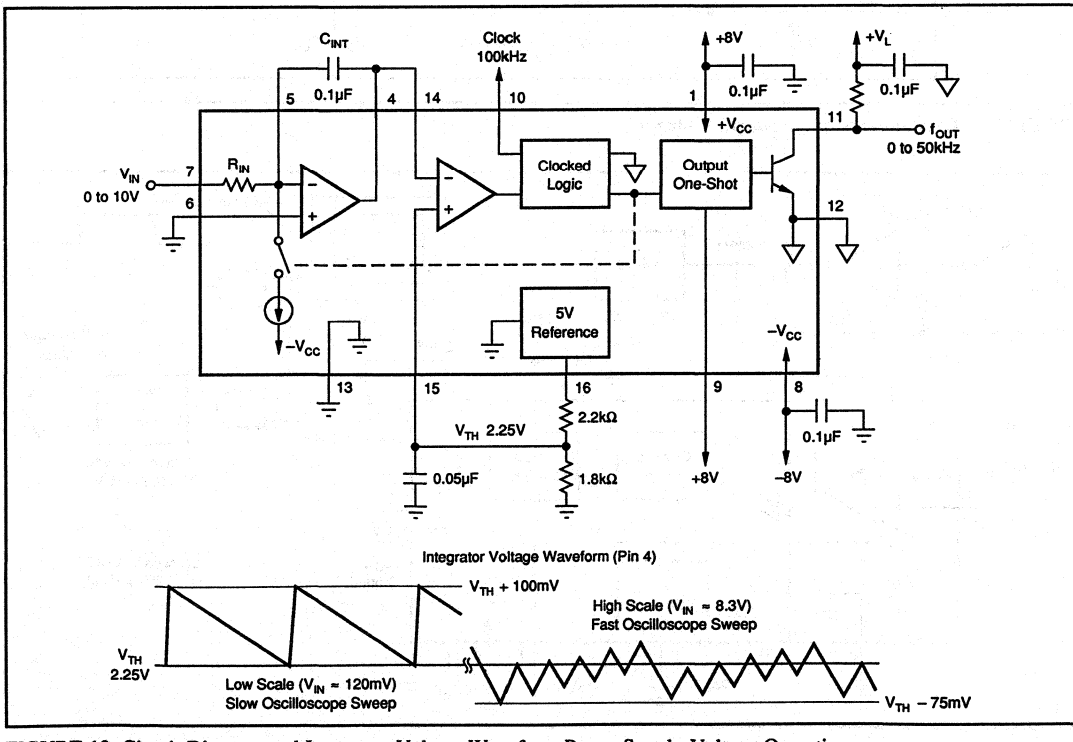


FIGURE 12. Circuit Diagram and Integrator Voltage Waveform Power Supply Voltage Operation.

FREQUENCY-TO-VOLTAGE MODE

The VFC100 can also function as a frequency-to-voltage converter by supplying an input frequency to the comparator input as shown in Figure 16. The input resistor, R_{IN}, is connected as a feedback resistor. The voltage at the integrator amp output is proportional to the ratio of the input frequency to the clock frequency. The transfer function is $V_{OUT} = (F_{IN}/f_{CLOCK})$ 20V.

This transfer function is complementary to the voltage-to-frequency mode transfer function, making voltage-to-frequency-to-voltage conversions simple and accurate.

Direct coupling of the input frequency to the comparator is easily accomplished by driving both comparators with complementary frequency input signals. Alternatively, one of the comparator inputs can be biased at half the logic voltage (using V_{REF} and a voltage divider) and the other input driven directly.

The proper timing of the input frequency waveform is shown in Figure 16. The input pulse should go low for one clock cycle, centered around a falling edge of the clock. The minimum acceptable input pulse width must fall no later than 200ns before a negative clock edge and rise no sooner

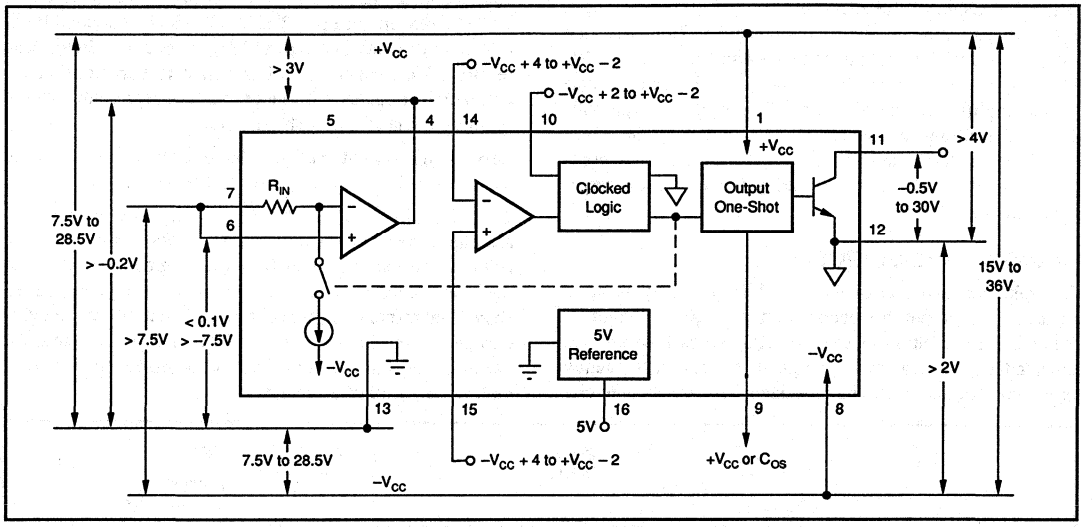


FIGURE 13. Relationships of Allowable Voltages.

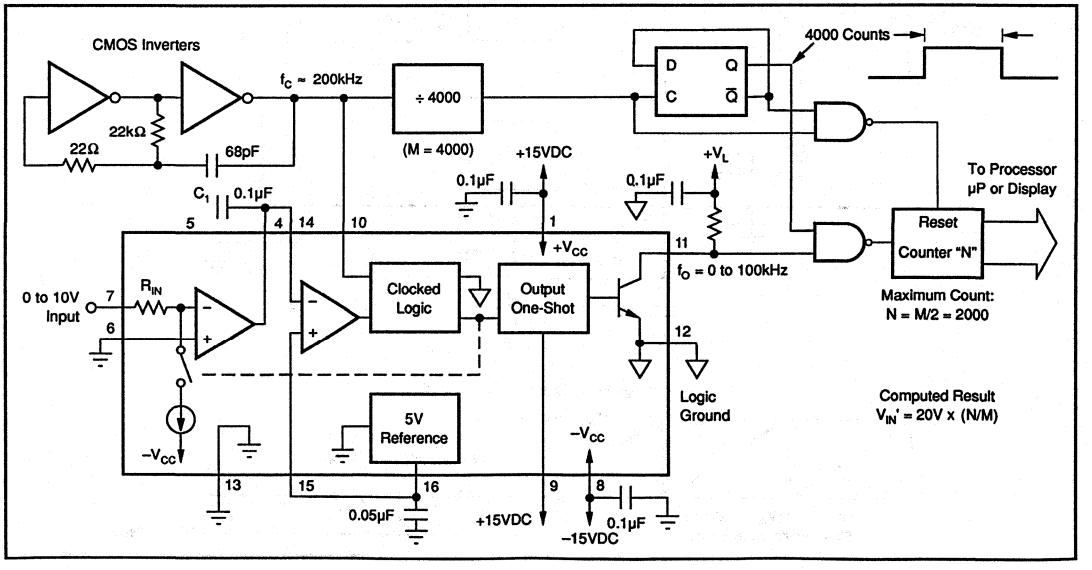


FIGURE 14. Diagram of a Voltage-to-Frequency Converter and Counter System.

than 200ns after the falling clock edge. An input pulse which remains low for more than one falling edge of the clock will produce incorrect output voltages. Positive (active high) input pulses can be accepted by reversing the connections to pins 14 and 15. Figure 17 shows a digital conditioning circuit which will accept any input duty cycle and provide the proper pulse width to the comparator. Each rising edge at this circuit's input generates the required negative pulse at the inverting comparator input. The noninverting comparator is driven by a complementary signal.

The integrator amplifier output is designed to drive up to 10,000pF and 5kΩ loads in frequency-to-voltage mode. This allows driving long lines in a large system.

Ripple voltage in the voltage output is unavoidable and is inversely proportional to the value of the integrator capacitor. Figure 18 shows the output ripple and settling time as a function of the C_{INT} value.

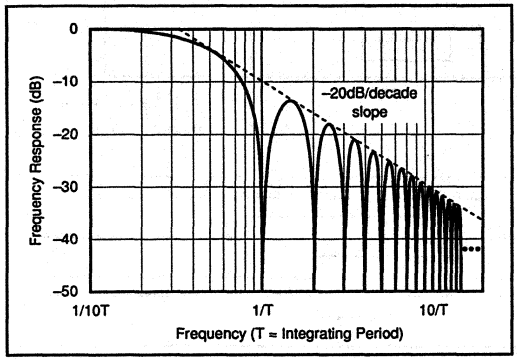


FIGURE 15. Frequency Response of an Integrating Analog-to-Digital Converter.

The ripple frequency is equal to the input frequency. Its magnitude can be reduced by using a large integrator capacitor value, but at the sacrifice of slow settling time at the voltage output in response to an input frequency change. The settling time constant is equal to $R_{IN} \times C_{INT}$. A better compromise between output ripple and settling time can be achieved by using a moderately low integrator capacitor value and adding a low-pass filter on the analog output. The cutoff frequency of the filter should be made below the lowest expected input frequency to the frequency-to-voltage converter.

The system in Figure 20 makes use of both voltage-to-frequency and frequency-to-voltage modes to send a signal across an optically isolated barrier. This technique is useful not only for providing safety in the presence of high voltages, but also for creating high noise rejection in electrically noisy environments. The use of a common clock frequency causes the two devices to have complementary transfer functions, which minimizes errors.

Optical coupling is facilitated by use of the output one-shot feature. The output pulse is shortened (see "Shortened Output Pulses") to allow for the relatively slow turn-off time of the LED. The timing diagram in Figure 19 shows how the accumulated delay of both optical couplers could produce too long an input pulse for the frequency-to-voltage converter, VFC_2, of Figure 20.

An output filter is used to reduce the ripple in the output of VFC_2. In order to most effectively filter the output, both input and output VFCs are offset. By connecting R_1 to V_{REF}-

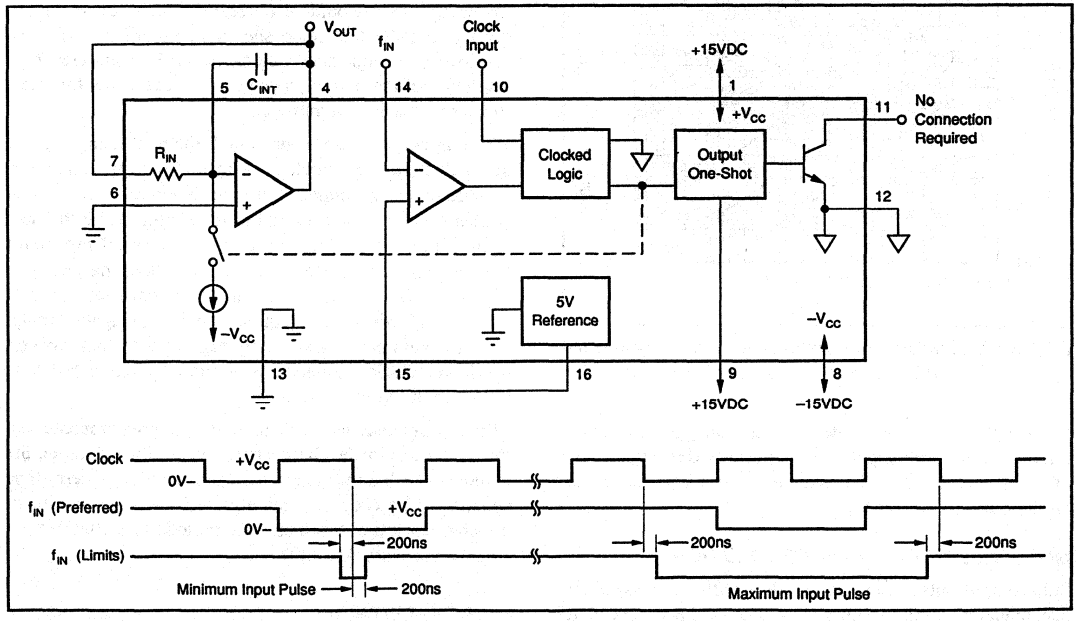


FIGURE 16. Circuit and Timing Diagram of a Frequency-to-Voltage Converter.

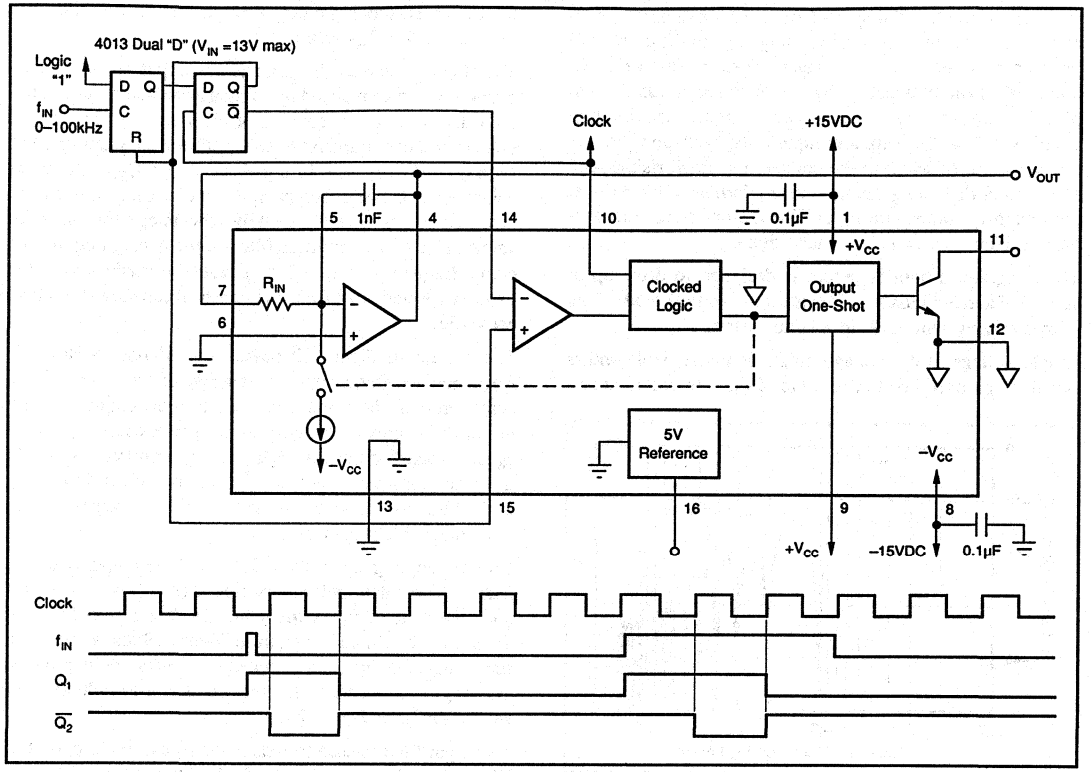


FIGURE 17. Digital Timing Input Conditioning Circuit for Frequency-to-Voltage Operation.

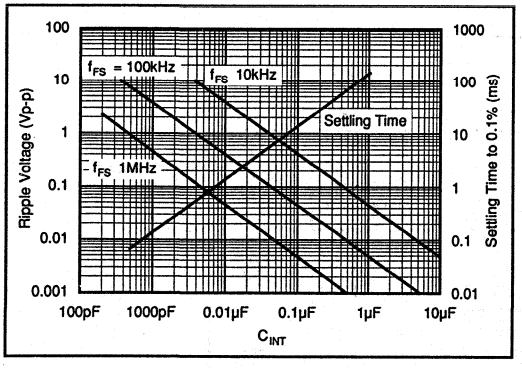


FIGURE 18. Frequency-to-Voltage Mode Output Ripple and Settling Time vs Integrator Capacitance.

an accurate offset is created in the voltage-to-frequency function. Zero volts input now creates a 10kHz output. This offset is subtracted in the frequency-to-voltage conversion on the output side, by V_{REF} and R_5.

MORE PULSE POSITION RESOLUTION

Since output pulses must always align with clock edges, the instantaneous output frequency is quantized and appears to have phase jitter. This effect can be greatly reduced by using a high speed clock so that available clock edges come more frequently. This would also create a high full-scale frequency, but the technique shown in Figure 21 offers an alternative. A high speed clock is used to produce high resolution of the output pulse position, but a low full-scale frequency can be programmed.

When an output pulse is generated, the next rising edge of the high frequency clock is delayed for a programmable number of clock counts. Since the integrator reset period (which sets the full-scale range) is determined by the time from rising edge to rising edge at the VFC's clock input once the comparator is tripped, the effective clock frequency is $f_{CLOCK}/16$. The circuit shown can be programmed for an N from 2 to 16. Since an output pulse must propagate through the VFC before the next rising edge of the clock arrives, maximum clock frequency is limited by the delay time shown in the timing diagram.

With output pulses now able to align with greater resolution, the output has lower phase jitter. Using this technique, the output is suitable for ratiometric (period measurement) type counting. This counting technique achieves the maximum possible resolution for short gate periods (see Burr-Brown Application Note AN-130).

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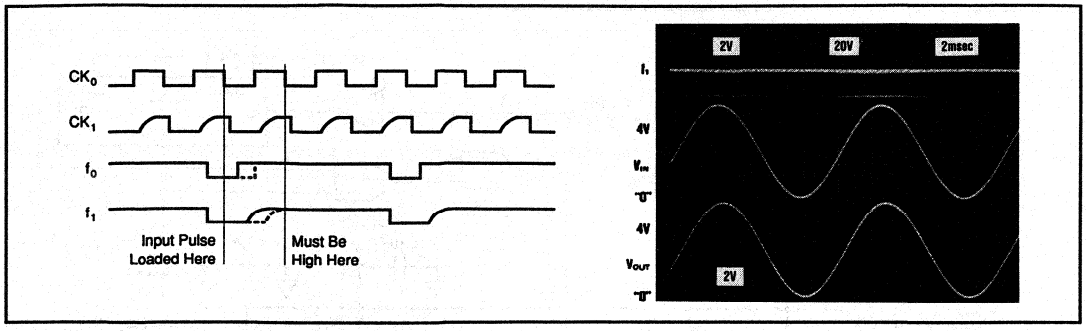

FIGURE 19. Timing Diagram and Oscilloscope Trace of Isolated Voltage-to-Frequency/Frequency-to-Voltage System.

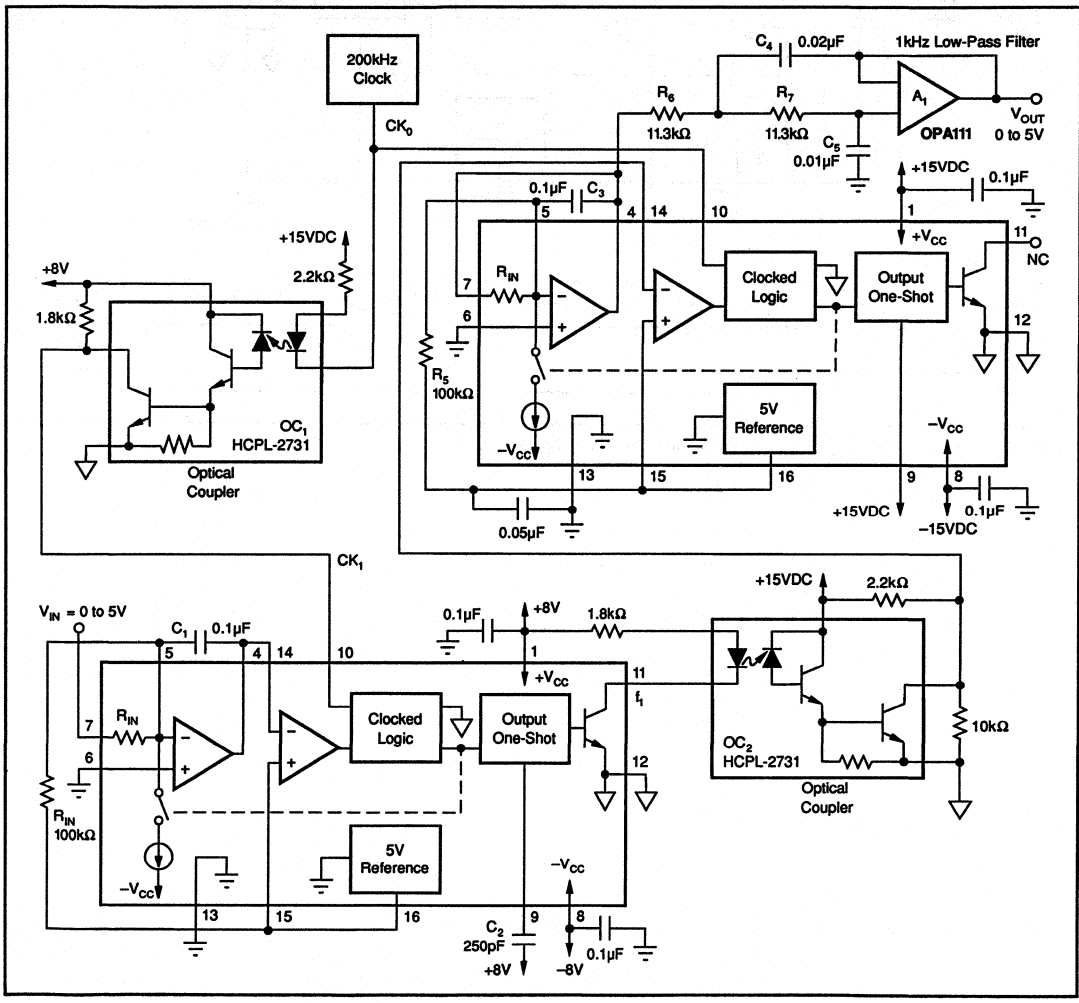

FIGURE 20. Circuit Diagram of Isolated Voltage-to-Frequency/Frequency-to-Voltage System.

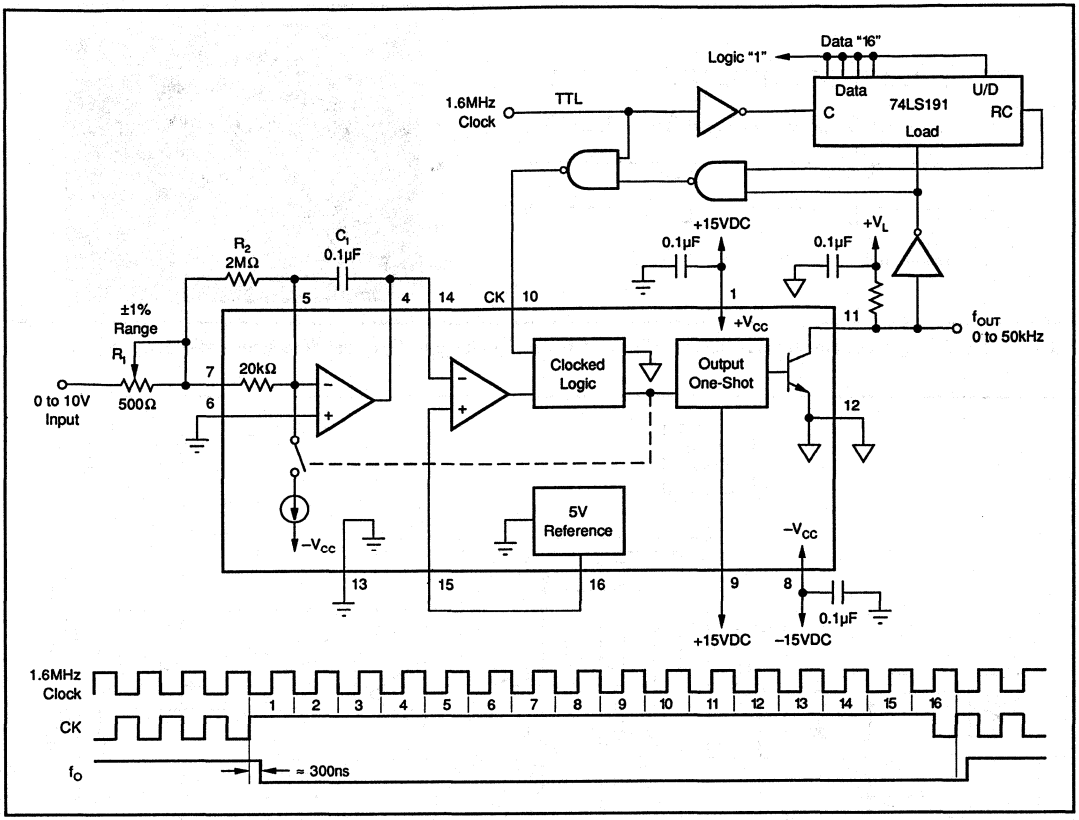

FIGURE 21. Circuit Diagram for Increased Pulse Position Resolution.

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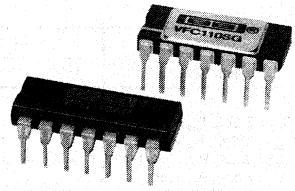


VFC110

High-Frequency VOLTAGE-TO-FREQUENCY CONVERTER

FEATURES

- HIGH-FREQUENCY OPERATION: 4MHz FS max
- EXCELLENT LINEARITY: ±0.02% typ at 2MHz
- PRECISION 5V REFERENCE
- DISABLE PIN
- LOW JITTER

APPLICATIONS

- INTEGRATING A/D CONVERSION
- PROCESS CONTROL
- VOLTAGE ISOLATION
- VOLTAGE-CONTROLLED OSCILLATOR
- FM TELEMETRY

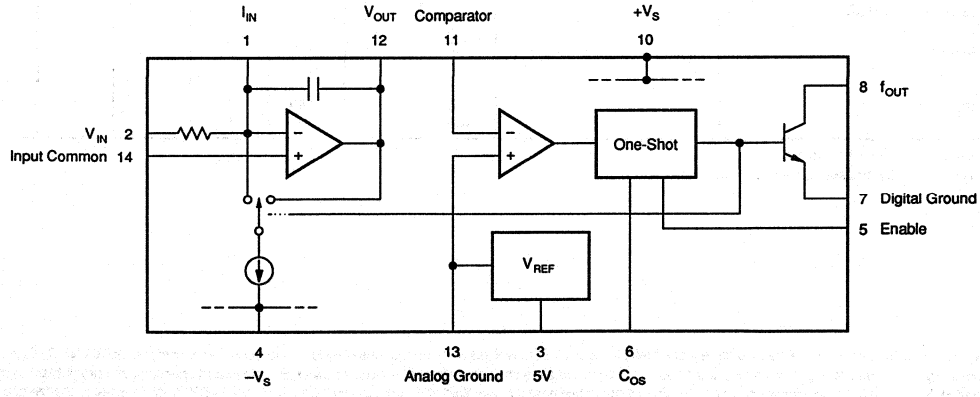
DESCRIPTION

The VFC110 voltage-to-frequency converter is a third-generation VFC offering improved features and performance. These include higher frequency operation, an on-board precision 5V reference and a Disable function.

The precision 5V reference can be used for offsetting the VFC transfer function, as well as exciting transducers or bridges. The Enable pin allows several VFCs' outputs to be paralleled, multiplexed, or simply to shut off the VFC. The open-collector frequency output is TTL/CMOS-compatible. The output may be isolated by using an opto-coupler or transformer.

Internal input resistor, one-shot and integrator capacitors simplify applications circuits. These components are trimmed for a full-scale output frequency of 4MHz at 10V input. No additional components are required for many applications.

The VFC110 is packaged in plastic and ceramic 14-pin DIPs. Industrial and military temperature range gradeouts are available.



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Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

At T_A = +25°C and V_S = ±15V unless otherwise noted.

PARAMETER	CONDITIONS	VFC110BG MIN	VFC110BG TYP	VFC110BG MAX	VFC110AG/SG/AP MIN	VFC110AG/SG/AP TYP	VFC110AG/SG/AP MAX	UNITS
VOLTAGE-TO-FREQUENCY OPERATION								
Nonlinearity[1]: f_{FS} = 100kHz	C_{OS} = 2.2nF, R_{IN} = 44kΩ		0.005	0.01		0.01	0.05	%FS
f_{FS} = 1MHz	C_{OS} = 150pF, R_{IN} = 40kΩ		0.01	0.05			0.1	%FS
f_{FS} = 2MHz	C_{OS} = 56pF, R_{IN} = 34kΩ		0.02			*		%FS
f_{FS} = 4MHz	C_{OS} = (Int), R_{IN} = (Int)		1			*		%FS
Gain Error, f = 1MHz	C_{OS} = 150pF, R_{IN} = 40kΩ			5			*	%
Gain Drift, f = 1MHz	Specified Temp Range			50			100	ppm/°C
Relative to V_{REF}	Specified Temp Range		50			100		ppm/°C
PSRR	V_S = ±8V to ±18V			0.05			0.1	%/V
INPUT								
Full Scale Input Current			250	500		*	*	µA
I_B– (Inverting Input)			15	60		20	100	nA
I_B+ (Non-Inverting Input)			250			*		nA
V_{OS}				3			3	mV
V_{OS} Drift	Specified Temp Range		35			*		µV/°C
INTEGRATOR AMPLIFIER OUTPUT								
Output Voltage Range	R_L = 2kΩ	–0.2		$+V_S - 4$	*		*	V
Output Current Drive		5	20		*	*		mA
Capacitive Load	No Oscillations		10			10		nF
COMPARATOR INPUT								
I_B (Input Bias Current)			–5			*		µA
Trigger Voltage			±50			*		mV
Input Voltage Range		–5		$+V_S$	*		*	V
OPEN COLLECTOR OUTPUT								
V_O Low				0.4			*	V
$I_{LEAKAGE}$			0.1	1		*	*	µA
Fall Time			25			*		ns
Delay to Rise			25			*		ns
Settling Time	To Specified Linearity for a Full-Scale Input Step		One Pulse of New Frequency Plus 1µs					
REFERENCE VOLTAGE								
Voltage		4.97	5	5.03	*	*	*	V
Voltage Drift				20			50	ppm/°C
Load Regulation	I_O = 0 to 10mA		2	10		*	*	mV
PSRR	V_S = ±8V to ±18V		5			*		mV/V
Current Limit	Short Circuit	15	20			*		mA
ENABLE INPUT								
V_{HIGH} (f_{OUT} Enabled)	Specified Temp Range	2			*			V
V_{LOW} (f_{OUT} Disabled)	Specified Temp Range			0.4			*	V
I_{HIGH}			0.1			*		µA
I_{LOW}			1			*		µA
POWER SUPPLY								
Voltage, ±V_S		±8	±15	±18	*	*	*	V
Current			13	16		*	*	mA
TEMPERATURE RANGE								
Specified								
AG, BG, AP		–25		+85	*		*	°C
SG		–55		+125				°C
Storage								
AG, BG, SG		–65		+150	*		*	°C
AP		–40		+125	*		*	°C

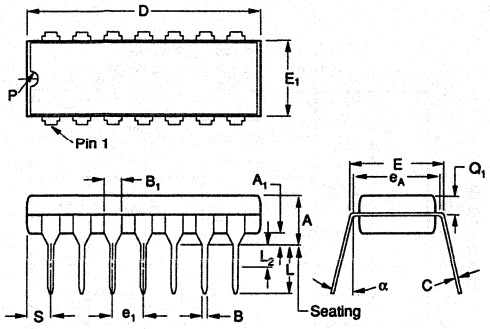
* Same specifications as VFC110BG.

NOTE: (1) Nonlinearity measured from 1V to 10V input.

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

MECHANICAL

P Package — 14-Pin Plastic DIP



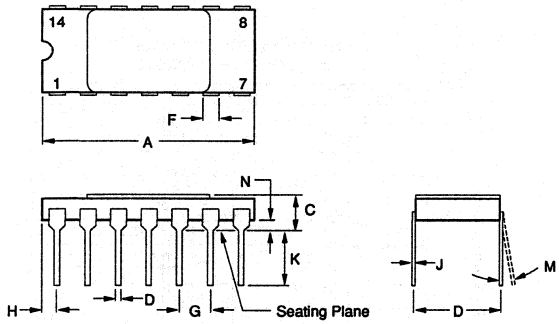
DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.120	.160	3.048	4.064
A1	.015	.065	.381	1.651
B	.014	.020	.355	.508
B1	.050	.065	1.270	1.651
C	.008	.012	.203	.304
D	.745	.770	18.923	19.558
E	.300	.325	7.620	8.255
E1	.240	.260	6.096	6.604
e1	.100 BASIC		2.540 BASIC	
eA	.300 BASIC		7.620 BASIC	
L	.125	.150	3.175	3.810

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
L2 (4)	0	.030	0	.762
α	0°	15°	0°	15°
N (1)	14		14	
N1 (2)	0		0	
P	—	.050	—	1.270
Q1	.050	.085	1.270	2.159
S (3)	.065	.090	1.651	2.286

(1) N = Total number of pins.
(2) N_1 = Total number of missing pins.
(3) Not per JEDEC Std.
(4) e_1 and e_A applies in zone L_2 when unit installed.

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

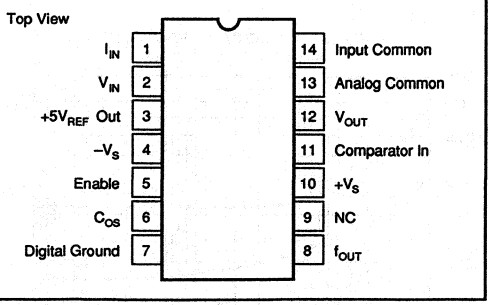
G Package — 14-Pin Hermetic DIP



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.670	.710	17.02	18.03
C	.065	.170	1.65	4.32
D	.015	.021	0.38	0.53
F	.045	.060	1.14	1.52
G	.100 BASIC		2.54 BASIC	
H	.025	.070	0.64	1.78
J	.008	.012	0.20	0.30
K	.120	.240	3.05	6.10
L	.300 BASIC		7.62 BASIC	
M	—	10°	—	10°
N	.009	.060	0.23	1.52

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Power Supply Voltages ($+V_S$ to $-V_S$) 40V
f_{OUT} Sink Current 50mA
Comparator In Voltage ..... $-5V$ to $+V_S$
Enable Input ..... $+V_S$ to $-V_S$
Integrator Common-Mode Voltage ..... –1.5V to +1.5V
Integrator Differential Input Voltage ..... +0.5V to –0.5V
Integrator Out (short-circuit) ..... Indefinite
V_{REF} Out (short-circuit) ..... Indefinite
Operating Temperature Range
  G Package ..... –55°C to +125°C
  P Package ..... –40°C to +85°C
Storage Temperature
  G Package ..... –60°C to +150°C
  P Package ..... –40°C to +125°C
Lead Temperature (soldering, 10s) ..... +300°C

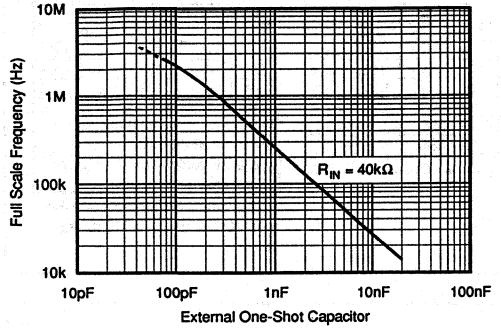
ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE
VFC110AG	Ceramic DIP	–25°C to +85°C
VFC110BG	Ceramic DIP	–25°C to +85°C
VFC110SG	Ceramic DIP	–55°C to +125°C
VFC110AP	Plastic DIP	–25°C to +85°C

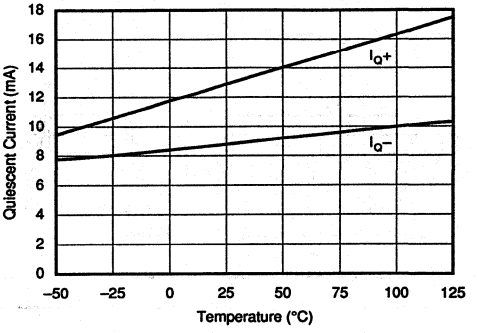
TYPICAL PERFORMANCE CURVES

At T_A = +25°C, V_S = ±15V unless otherwise noted.

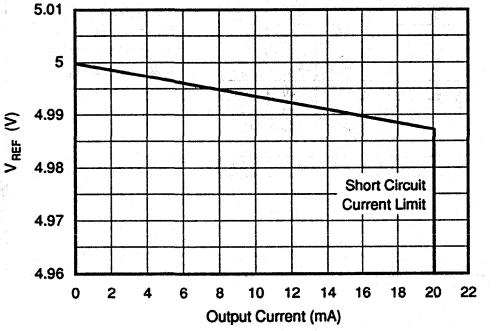
FULL-SCALE FREQUENCY vs EXTERNAL ONE-SHOT CAPACITOR



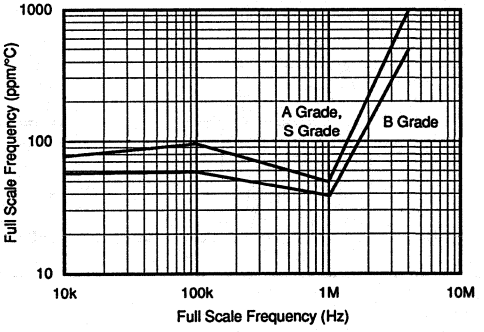
FULL-SCALE FREQUENCY vs EXTERNAL ONE-SHOT CAPACITOR



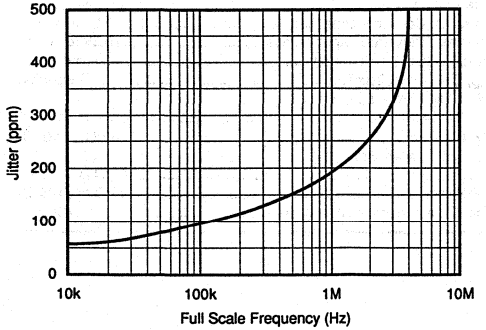
REFERENCE VOLTAGE vs REFERENCE LOAD CURRENT



TYPICAL FULL SCALE GAIN DRIFT vs FULL SCALE FREQUENCY

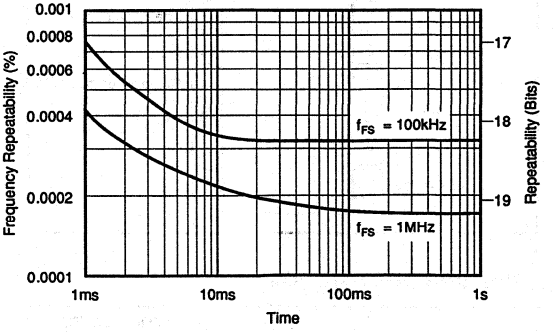


JITTER vs FULL SCALE FREQUENCY



Jitter is the ratio of the 1σ value of the distribution of the period ($1/f_{OUT}$, max) to the mean of the period.

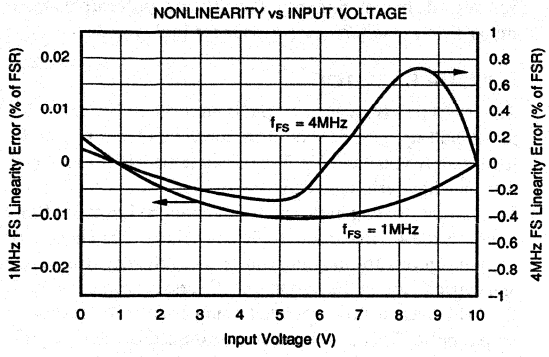
FREQUENCY COUNT REPEATABILITY vs COUNTER GATE TIME

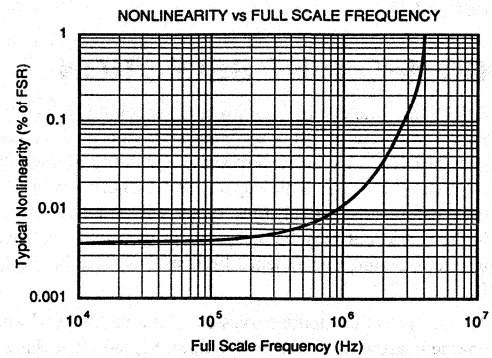


This graph describes the low frequency stability of the VFC110: the ratio of the 1σ point of the distribution of 100 runs (where each mean frequency came from 1000 readings for each gate time) to the overall mean frequency.

TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_S = ±15V unless otherwise noted.





OPERATION

Figure 1 shows the connections required for operation at a full-scale output frequency of 4MHz. Only power supply bypass capacitors and an output pull-up resistor, R_{PU}, are required for this mode of operation. A 0V to 10V input voltage produces a 0Hz to 4MHz output frequency. The internal input resistor, one-shot and integrator capacitors set the full-scale output frequency. The input is applied to the summing junction of the integrator amplifier through the 25kΩ internal input resistor. Pin 14 (the non-inverting amplifier input) should be referred directly to the negative side of V_{IN}. The common-mode range of the integrating amplifier is limited to approximately –1V to +1V referred to analog ground. This allows the non-inverting input to Kelvin-sense the common connection of V_{IN}, easily accommodating any ground-drop errors. The input impedance loading V_{IN} is equal to the input resistor—approximately 25kΩ.

OPERATION AT LOWER FREQUENCIES

The VFC110 can be operated at lower frequencies simply by limiting the input voltage to less than the nominal 10V full-scale input. To maintain a 10V FS input and highest accuracy, however, external components are required (see Table I). Small adjustments may be required in the nominal values indicated. Integrator and one-shot capacitors are added in parallel to internal capacitors. Figure 2 shows the connections required for 100kHz full scale output. The one-shot capacitor, C_{OS}, should be connected to logic ground. The one-shot connection (pin 6) is not short-circuit protected. Short-circuits to ground may damage the device.

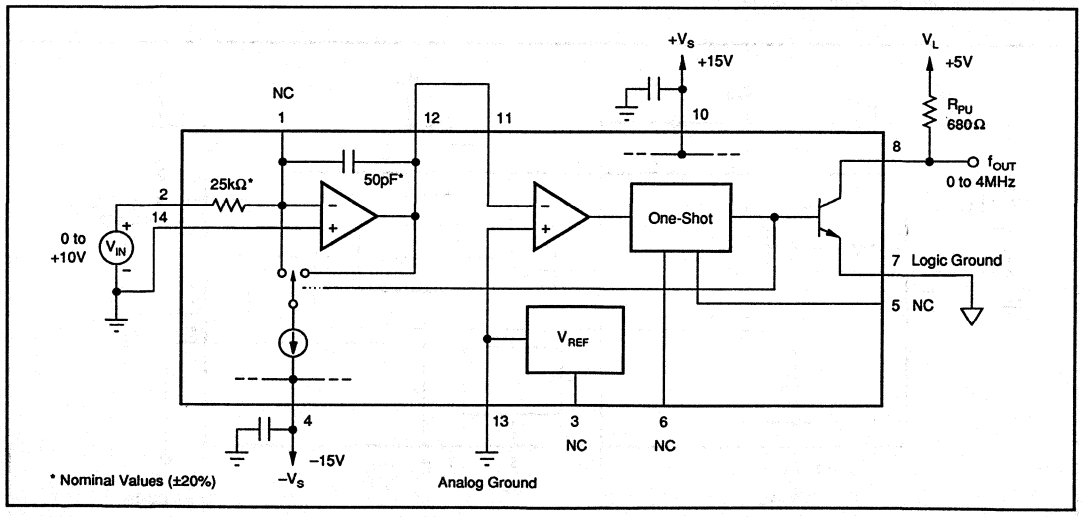


FIGURE 1. 4MHz Full-Scale Operation.

The integrator capacitor's value does not directly affect the output frequency, but determines the magnitude of the voltage swing on the integrator's output. Using a C_{INT} equal to C_{OS} provides an integrator output swing from 0V to approximately 1.5V.

COMPONENT SELECTION

Selection of the external resistor and capacitor type is important. Temperature drift of an external input resistor and one-shot capacitor will affect temperature stability of the output frequency. NPO ceramic capacitors will normally produce the best results. Silver-mica types will result in slightly higher drift, but may be adequate in many applications. A low temperature coefficient film resistor should be used for R_{IN}.

The integrator capacitor serves as a "charge bucket," where charge is accumulated from the input, V_{IN}, and that charge is drained during the one-shot period. While the size of the bucket (capacitor value) is not critical, it must not leak. Capacitor leakage or dielectric absorption can affect the linearity and offset of the transfer function. High-quality ceramic capacitors can be used for values less than 0.01µF. Use caution with higher value ceramic capacitors. High-k ceramic capacitors may have voltage nonlinearities which can degrade overall linearity. Polystyrene, polycarbonate, or mylar film capacitors are superior for high values.

FULL-SCALE FREQUENCY, f_{FS}	EXTERNAL COMPONENTS		
	R_{IN}	C_{OS}	C_{INT}
4MHz	*	*	*
2MHz	34kΩ	56pF	*
1MHz	40kΩ	150pF	*
500kHz	58kΩ	330pF	2nF
100kHz	44kΩ	2.2nF	10nF
50kHz	88kΩ	2.2nF	0.1µF
10kHz	44kΩ	22nF	0.1µF

* Use internal component only.
The values given were determined empirically to give the optimal performance, taking into consideration tradeoffs between linearity and jitter for each given full scale frequency of operation. The capacitors listed were chosen from standard values of NPO ceramic type capacitors while the resistor values were rounded off. Larger C_{INT} values may improve linearity, but may also increase frequency noise.

TABLE I. Component Selection Table.

PULL-UP RESISTOR

The VFC110's frequency output is an open-collector transistor. A pull-up resistor should be connected from f_{OUT} to the logic supply voltage, $+V_L$. The output transistor is On during the one-shot period, causing the output to be a logic Low. The current flowing in this resistor should be limited to 8mA to assure a 0.4V maximum logic Low. The value chosen for the pull-up resistor may depend on the full-scale frequency and capacitance on the output line. Excessive capacitance on f_{OUT} will cause a slow, rounded rising edge at the end of an output pulse. This effect can be minimized by using a pull-up resistor which sets the output current to its maximum of 8mA. The logic power supply can be any positive voltage up to $+V_S$.

ENABLE PIN

If left unconnected, the Enable input will assume a logic High level, enabling operation. Alternatively, the Enable input may be connected directly to $+V_S$. Since an internal pull-up current is included, the Enable input may be driven by an open-collector logic signal.

A logic Low at the Enable input causes output pulses to cease. This is accomplished by interrupting the signal path through the one-shot circuitry. While disabled, all circuitry remains active and quiescent current is unchanged. Since no reset current pulses can occur while disabled, any positive input voltage will cause the integrator op amp to ramp negatively and saturate at its most negative output swing of approximately –0.7V.

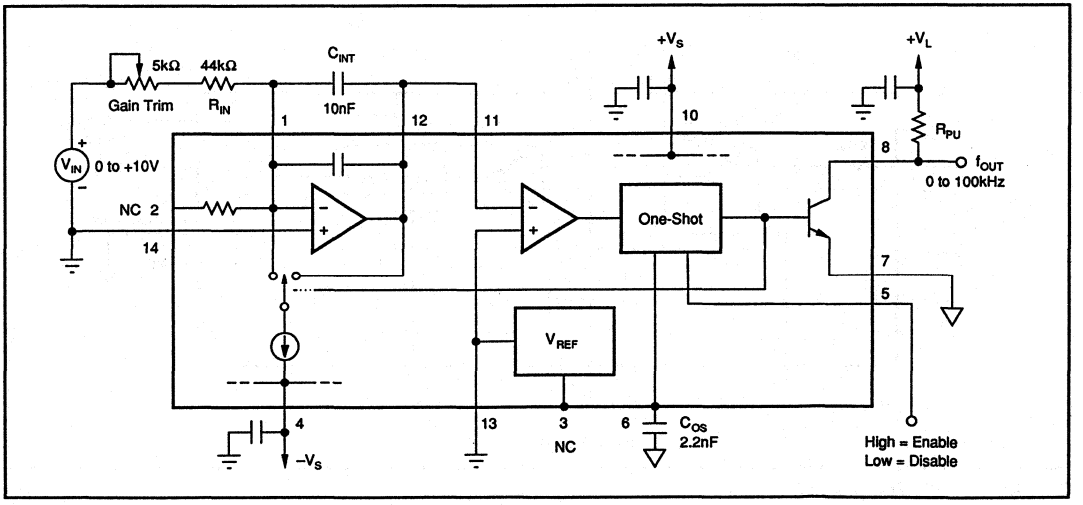


FIGURE 2. 100kHz Full-Scale Operation.

PRINCIPLE OF OPERATION

The VFC110 uses a charge-balance technique to achieve high accuracy. The heart of this technique is an analog integrator formed by the integrator op amp, feedback capacitor C_{INT}, and input resistor R_{IN}. The integrator's output voltage is proportional to the charge stored in C_{INT}. An input voltage develops an input current of V_{IN}/R_{IN}, which is forced to flow through C_{INT}. This current charges C_{INT}, causing the integrator output voltage to ramp negatively.

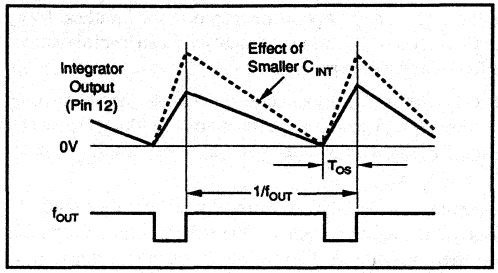
When the output of the integrator ramps to 0V, the comparator trips, triggering the one-shot. This connects the reference current, I_{REF}, to the integrator input during the one-shot period, T_{OS}. This switched current causes the integrator output to ramp positively until the one-shot period ends. Then the cycle starts again.

The oscillation is regulated by the balance of current (or charge) between the input current and the time-averaged reset current. The equation of current balance is

$$I_{IN} = I_{REF} \cdot \text{Duty Cycle}$$

$$V_{IN}/R_{IN} = I_{REF} \cdot f_{OUT} \cdot T_O$$

where T_O is the one-shot period and f_{OUT} is the oscillation frequency.



When the Enable input receives a logic High (greater than +2V), a reset current cycle is initiated (causing f_{OUT} to go Low). The integrator ramps positively and normal operation is established. The time required for the output frequency to stabilize is equal to approximately one cycle of the final output frequency plus 1µs.

Using the Enable input, several VFCs' outputs can be connected to a single output line. All disabled VFCs will have a high output impedance; one active VFC can then transmit on the output line. Since the disabled VFCs are not oscillating, they cannot interfere or "lock" with the operating VFC. Locking can occur when one VFC operates at nearly the same frequency as—or a multiple of—a nearby VFC. Coupling between the two may cause them to lock to the same or exact multiple frequency. It then takes a small incremental input voltage change to unlock them. Locking cannot occur when unneeded VFCs are disabled.

REFERENCE VOLTAGE

The V_{REF} output is useful for offsetting the transfer function and exciting sensors. Figure 3 shows V_{REF} used to offset the transfer function of the VFC110 to achieve a bipolar input voltage range. Sub-surface zener reference circuitry is used for low noise and excellent temperature drift. Output current is specified to 10mA and current-limited to approximately 20mA. Excessive or variable loads on V_{REF} can decrease frequency stability due to internal heating.

MEASURING THE OUTPUT FREQUENCY

To complete an integrating A/D conversion, the output frequency of the VFC110 must be counted. Simple frequency counting is accomplished by counting output pulses for a reference time (usually derived from a crystal oscillator).

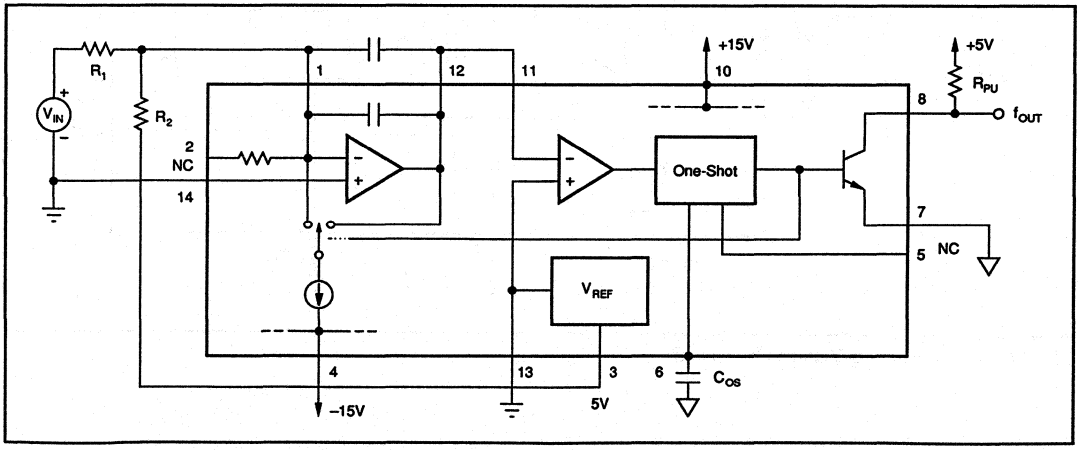


FIGURE 3. Offsetting the Frequency Output.

This can be implemented with counter/timer peripheral chips available for many popular microprocessor families. Many micro-controllers have counter inputs that can be programmed for frequency measurement.

Since f_{OUT} is an open-collector device, the negative-going edge provides the fastest logic transition. Clocking the counter on the falling edge will provide the best results in noisy environments.

Frequency can also be measured by accurately timing the period of one or more cycles of the VFC's output. Frequency must then be computed since it is inversely proportional to the measured period. This measurement technique can provide higher measurement resolution in short conversion times. It is the method used in most high-performance laboratory frequency counters. It is usually necessary to offset the transfer function so 0V input causes a finite frequency out. Otherwise the output period (and therefore the conversion time) approaches infinity.

FREQUENCY NOISE

Frequency noise (small random variation in the output frequency) limits the useful resolution of fast frequency measurement techniques. Long measurement time averages the effect of frequency noise and achieves the maximum useful resolution. The VFC110 is designed to minimize frequency noise and allows improved useful resolution with short measurement times. The typical curve "Frequency Count Repeatability vs Counter Gate Time" shows the effect of noise as the counter gate time is varied. It shows the one standard deviation (1σ) count variation (as a percentage of FS counts) versus counter gate time.

FREQUENCY-TO-VOLTAGE CONVERSION

The VFC110 can also be connected as a frequency-to-voltage converter (Figure 4). Input frequency pulses are applied to the comparator input. A negative-going pulse crossing 0V initiates a reference current pulse which is averaged by the integrator op amp. The values of the one-shot capacitor and feedback resistor (same as R_{IN}) are determined with Table I. The input frequency pulse must not remain negative for longer than the duration of the one-shot period. Figure 4 shows the required timing to assure this. If the negative-going input frequency pulses are longer in duration, the capacitive coupling circuit shown can be used. Level shift or capacitive coupling circuitry should not provide pulses which go lower than –5V or damage to the comparator input may occur.

This frequency-to-voltage converter operates by averaging (filtering) the reference current pulses triggered on every falling edge at the frequency input. Voltage ripple with a frequency equal to the input will be present in the output voltage. The magnitude of this ripple voltage is inversely proportional to the integrator capacitor. The ripple can be made arbitrarily small with a large capacitor, but at the sacrifice of settling time. The R-C time constant of C_{INT} and R_{IN} determine the settling behavior. A better compromise between output ripple and settling time can be achieved by adding a low-pass filter following the voltage output.

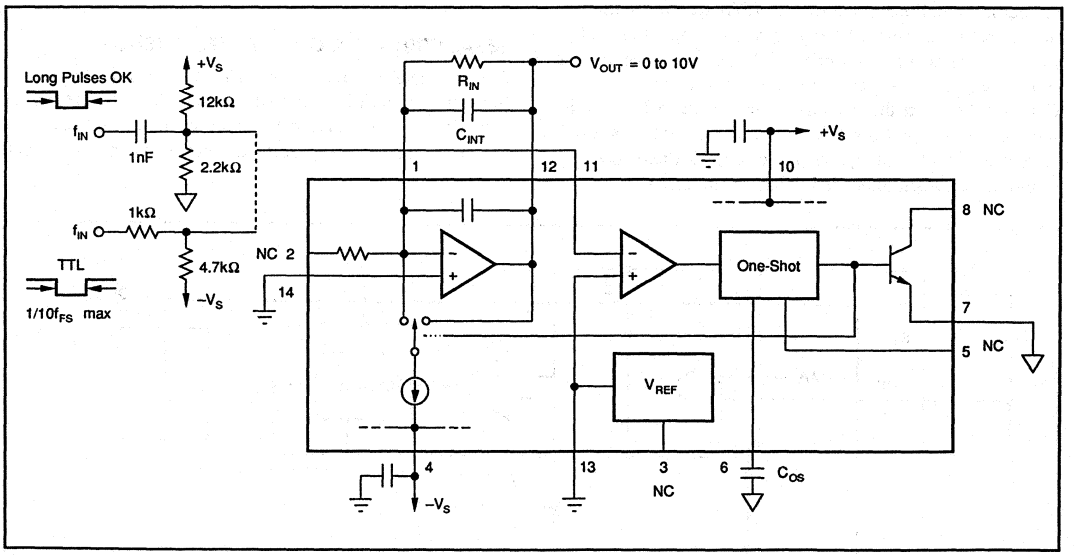
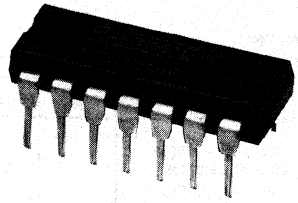


FIGURE 4. Frequency-to-Voltage Conversion.

BURR-BROWN®



VFC121

Precision Single Power Supply VOLTAGE-TO-FREQUENCY CONVERTER

FEATURES

- SINGLE SUPPLY OPERATION: +4.5V to +36V
- f_o = 1.5MHz max
- LOW NONLINEARITY: 0.03% max at 100kHz, 0.1% max at 1MHz
- HIGH INPUT IMPEDANCE
- VOLTAGE REFERENCE OUTPUT
- THERMOMETER OUTPUT: 1mV/°K

APPLICATIONS

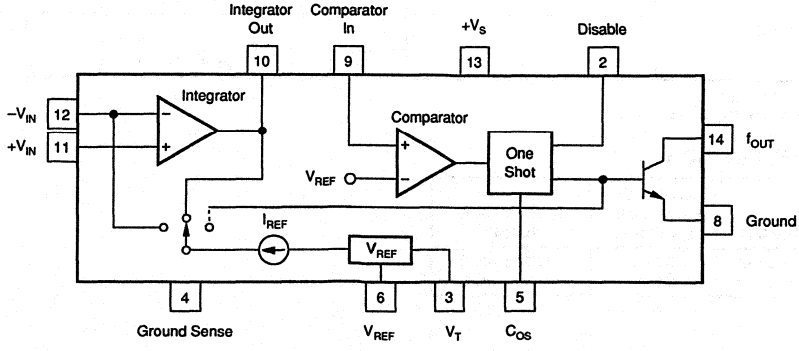
- INTEGRATING A/D CONVERSION
- ANALOG SIGNAL TRANSMISSION
- PHASE-LOCKED LOOP VCO
- GALVANICALLY ISOLATED SYSTEMS

DESCRIPTION

The VFC121 is a monolithic voltage-to-frequency converter consisting of an integrating amplifier, voltage reference, and one-shot charge pump circuitry. High-frequency complementary NPN/PNP circuitry is used to implement the charge-balance technique, achieving speed and accuracy far superior to previous single power supply VFCs.

The high-impedance input accepts signals from ground potential to V_S – 2.5V. Power supplies from 4.5V to 36V may be used. A 2.6V reference voltage output may be used to excite sensors or bias external circuitry. A thermometer output voltage proportional to absolute temperature (°K) may be used as a temperature sensor or for temperature compensation of applications circuits.

Frequency output is an open-collector transistor. A disable pin forces the output to the high impedance state, allowing multiple VFCs to share a common transmission path.



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SPECIFICATIONS

ELECTRICAL

At T_A = +25°C, V_S = +5V, and R_{IN} = 8kΩ unless otherwise noted.

PARAMETER	CONDITIONS	VFC121AP MIN	VFC121AP TYP	VFC121AP MAX	VFC121BP MIN	VFC121BP TYP	VFC121BP MAX	UNITS
ACCURACY								
Nonlinearity: f_{FS} = 100kHz	C_{OS} 1200pF, C_{INT} = 2700pF			0.05			0.03	%FS
f_{FS} = 1MHz	C_{OS} 68pF, C_{INT} = 270pF		0.1				0.1	%FS
Gain Error: f_{FS} = 100kHz	C_{OS} 1200pF, C_{INT} = 2700pF			10			*	%FS
Gain Drift: f_{FS} = 100kHz	T_{MIN} to T_{MAX}			80			40	ppm/°C
Relative to V_{REF}	+V_S = +5V to +36V			100			40	ppm/°C
PSRR				0.025			*	%/V
INPUT								
Minimum Input Voltage				0			*	V
Maximum Input Voltage		V_S – 2.5	V_S – 2		*	*		V
Impedance		10	100		*	*		MΩ
I_{BIAS}			150	300		*	*	nA
V_{OS}			300	800		100	400	µV
V_{OS} Drift	T_{MIN} to T_{MAX}		10			*		µV/°C
OPEN COLLECTOR OUTPUT								
V_{SAT}	$I_{PULL\ UP}$ = 10mA			0.4			*	V
$I_{LEAKAGE}$	$V_{PULL\ UP}$ = 5V			1			*	µA
	$V_{PULL\ UP}$ = 36V			10			*	µA
Fall Time				100			*	ns
Delay to Rise	$R_{PULL\ UP}$ = 470Ω			100			*	ns
Settling Time	To Specified Linearity for Full Scale Input Step	(1)						
REFERENCE VOLTAGE								
Voltage		2.59	2.6	2.61	*	*	*	V
Voltage Drift				100			50	ppm/°C
Load Regulation	I_O = 0 to 10mA			10			*	mV
PSRR	V_S = +5V to +36V			10			*	mV
Current Limit		Short Circuit Protected						
INTEGRATOR AMPLIFIER OUTPUT								
Output Voltage Range	R_L = 100kΩ	0.8		2.9	*		*	V
COMPARATOR INPUT								
I_{BIAS}			+1			*		µA
Trigger Voltage			2.6			*		V
Input Voltage Range		0		2.9	*		*	V
THERMOMETER								
V_T	T_A = +25°C		298			*		mV
V_T Slope	T_{MIN} to T_{MAX}		1			*		mV/°K
DISABLE INPUT								
V_{HIGH} (Disabled)		2			*			V
V_{LOW}				0.8			*	V
I_{HIGH} (Disabled)	V_{HIGH} = 2V		10			*		µA
I_{LOW}	V_{LOW} = 0.8V		10			*		µA
POWER SUPPLY								
Voltage		4.5	5	36	*	*	*	V
Current			7.5	10		*	*	mA
TEMPERATURE RANGE								
Specified		–25		+85	*		*	°C
Storage		–40		+125	*		*	°C

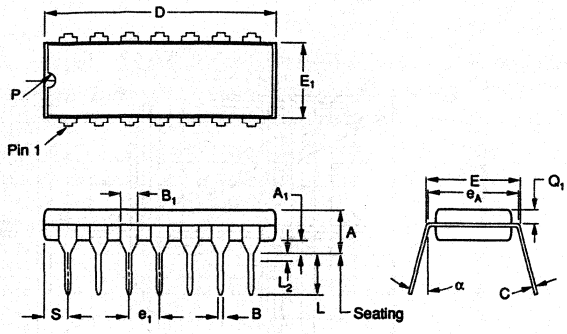
* Same specification as VFC121AP.
NOTE: (1) One pulse of new frequency plus 1µs.

ORDERING INFORMATION

MODEL	PACKAGE	LINEARITY ERROR, MAX (f_S = 100kHz)	TEMPERATURE RANGE
VFC121AP	Plastic DIP	0.05%	–25°C to +85°C
VFC121BP	Plastic DIP	0.03%	–25°C to +85°C

MECHANICAL

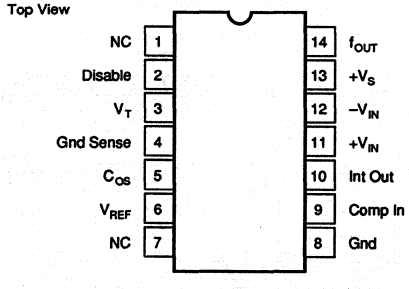
P Package — 14-Pin Plastic DIP



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.120	.160	3.048	4.064
A1	.015	.065	.381	1.651
B	.014	.020	.355	.508
B1	.050	.065	1.270	1.651
C	.008	.012	.203	.304
D	.745	.770	18.923	19.558
E	.300	.325	7.620	8.255
E1	.240	.260	6.096	6.604
e1	.100 BASIC		2.540 BASIC	
eA	.300 BASIC		7.620 BASIC	
L	.125	.150	3.175	3.810
L2(1)	0	.030	0	.762
α	0°	15°	0°	15
P	—	.050	—	1.270
Q1	.050	.085	1.270	2.159
S(2)	.065	.090	1.651	2.286

NOTES: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.
(1) e_1 and e_A apply in zone L_2 when unit is installed.
(2) Not per JEDEC.

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage ($+V_S$) 40V
f_{OUT} Sink Current 20mA
Comparator In Voltage ..... –0.5V to +3V
Enable Input ..... –0.3V to $+V_S$
Integrator Common-Mode Voltage ..... 0V to $+V_S$ – 2V
Integrator Differential Input Voltage ..... –0.3V to +0.3V
V_{REF} Out (short-circuit) ..... Indefinite
Operating Temperature Range ..... –40°C to +85°C
Storage Temperature ..... –40°C to +125°C
Lead Temperature (soldering, 10s) ..... +300°C

Stresses above these ratings may permanently damage the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN CONFIGURATION

PIN #	NAME	DESCRIPTION
1	NC	Not Connected
2	Disable	Input logic Low for normal operation. Input logic High to disable the VFC121. Has internal pull-down, for normal operation if not connected.
3	V_T	Temperature compensation voltage proportional to absolute temperature. Typically 298mV at room temperature (298°K), with a change of 1mV per °C (°K).
4	Gnd Sense	Defines ground for the internal voltage reference.
5	C_{OS}	One-shot capacitor is connected between here and ground to set full scale output frequency.
6	V_{REF}	Output from the internal band-gap voltage reference, typically 2.6V. Can be used externally to set levels or excite sensors.
7	NC	Not Connected
8	Gnd	Ground
9	Comp In	Comparator In
10	Int Out	Integrator Out
11	$+V_{IN}$	Non-inverting input of the integrating op amp. The input signal is applied here.
12	$–V_{IN}$	Inverting input of the integrating op amp. C_{INT} is connected between here and the integrator output (pin 10), and R_{IN} is connected between here and ground.
13	$+V_S$	Supply voltage connected here. Range is +4.5V to +36V.
14	f_{OUT}	Frequency output pin. This is the output of an open-collector transistor, and an external pull-up circuit should be used to generate the appropriate logic levels.

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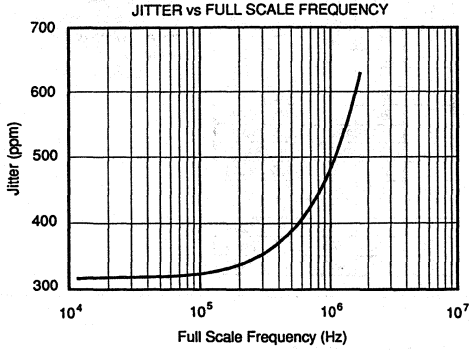
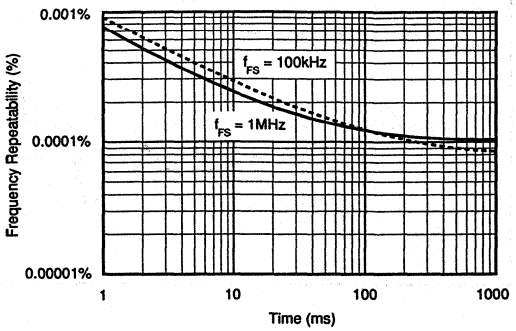
TYPICAL PERFORMANCE CURVES

At T_A = +25°C, V_S = +5V, and R_{IN} = 8kΩ unless otherwise noted.

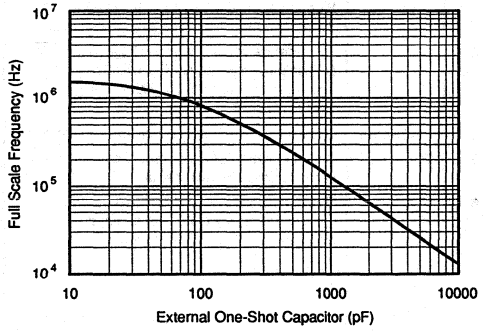
JITTER vs FULL SCALE FREQUENCY



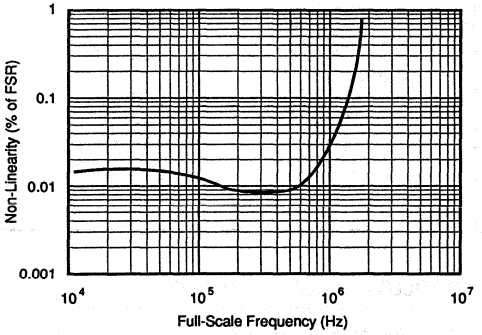
FREQUENCY COUNT REPEATABILITY vs COUNTER GATE TIME



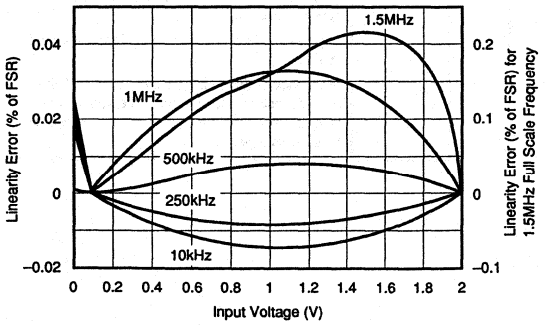
FULL SCALE FREQUENCY vs EXTERNAL ONE-SHOT CAPACITOR



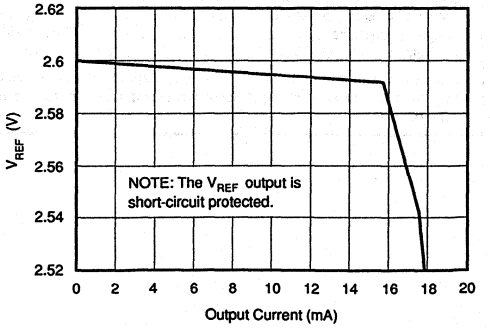
NON-LINEARITY vs FULL-SCALE FREQUENCY



NON-LINEARITY vs INPUT VOLTAGE

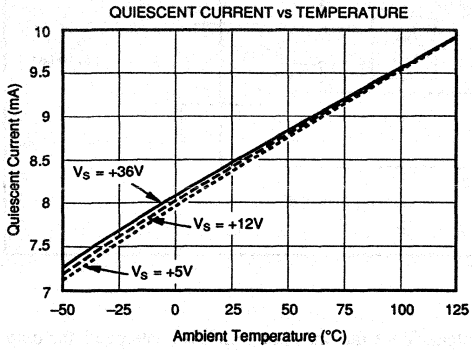


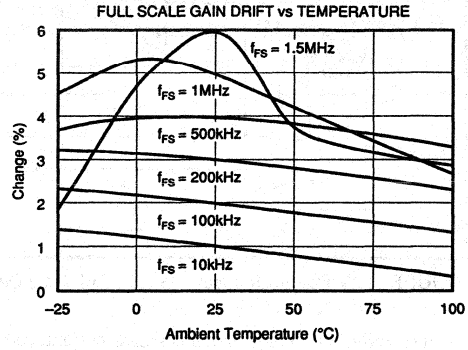
REFERENCE VOLTAGE vs REFERENCE LOAD CURRENT



TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C, V_S = +5V, and R_{IN} = 8kΩ unless otherwise noted.





THEORY OF OPERATION

The VFC121 uses a charge-balance technique to achieve high accuracy. The basic architecture is shown in Figure 1. An analog integrator at the front end, consisting of a precision op amp and a feedback capacitor, C_{INT}, provides a true integrating approach for improved noise immunity. Use of the non-inverting input of the op amp for the analog input provides a high input impedance to the user.

The integrator's output is proportional to the charge stored on C_{INT} plus the analog input voltage. An input voltage, V_{IN}, forces a current through R_{IN} of V_{IN}/R_{IN}, which also flows through C_{INT}. This current through C_{INT} causes the integrator output to ramp positive. (Refer to the timing diagram in Figure 2.)

When the output of the integrator ramps to V_{REF}, the comparator trips, driving the output of the VFC121 Low, and triggering the one-shot. The tripping of the comparator also connects the reference current, I_{REF}, to the integrator input for the duration of the one-shot period, T_{OS}. This switched current causes the output of the integrator to ramp negative.

When the one-shot times out, the output of the VFC121 is reset High, the one-shot is reset, and I_{REF} is switched to the output of the integrating op amp. (This causes the output of

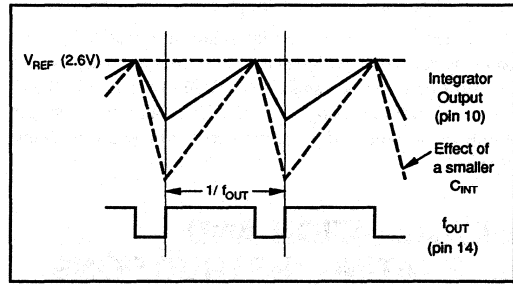


FIGURE 2. Timing Diagram.

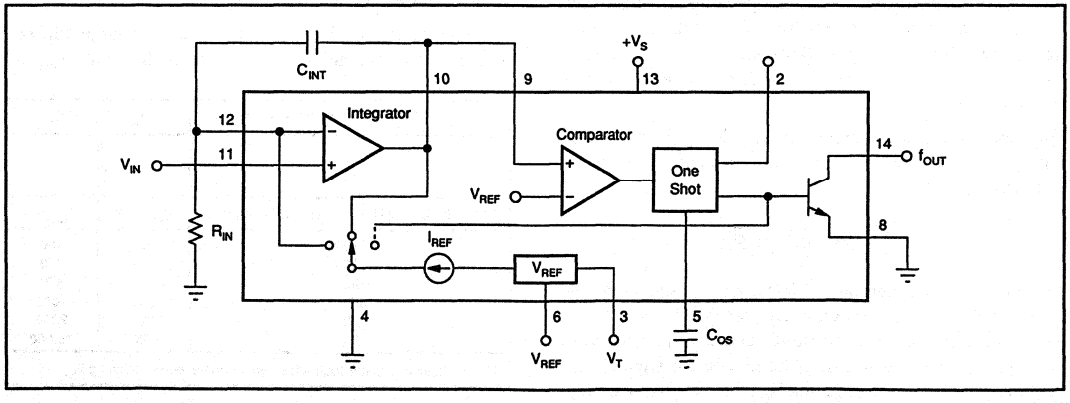


FIGURE 1. VFC121 Architecture.

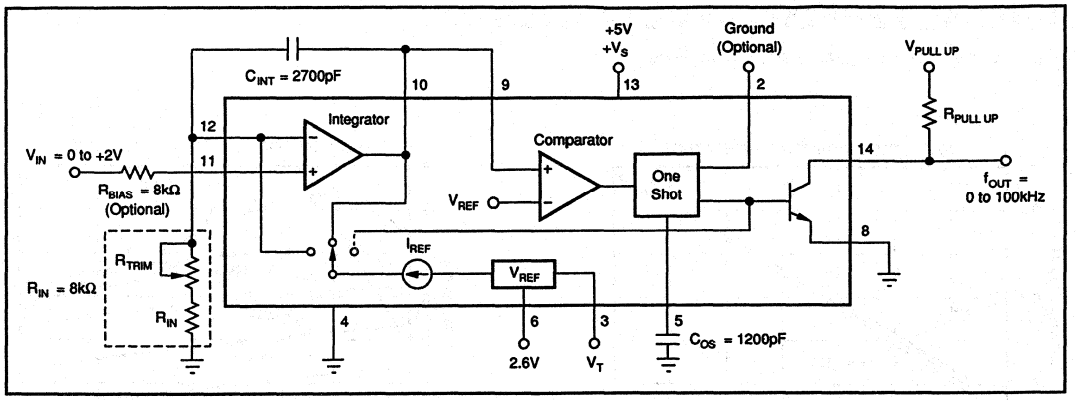


FIGURE 3. 2V Full Scale Input, 100kHz Full Scale Output.

the integrating op amp to see a constant current, reducing errors that might occur if the load were unbalanced.) In this state, the output of the integrator resumes a positive ramp, restarting the cycle.

The output frequency is regulated by the balance of current (or charge) between the current V_{IN}/R_{IN} and the time-averaged reset current. The size of the integrating capacitor, C_{INT}, determines the slew rate of the integrator, and thus how far down the integrator ramps during the one-shot period, but has no effect on the output frequency of the VFC121.

The reference voltage used internally is generated from a bandgap reference, which is actively trimmed to achieve the low drift characteristics of the VFC121. To maximize flexibility of designs using the VFC121, both the bandgap reference voltage and a thermometer voltage are available externally.

INSTALLATION AND OPERATING INSTRUCTIONS

BASIC OPERATION

The VFC121 allows users a wide range of input voltages and supply voltages, and easy control of the full scale output frequency. The basic connections are shown in Figure 3, with components that generate a 100kHz output with a 2V full scale input.

For other input and output ranges, the full scale input voltages and full scale output frequencies can be calculated as follows:

$$f_{FS} = \frac{V_{FS}}{2(R_{IN})(C_{OS} + 60)}$$

The full scale input current of 250µA was chosen to provide a 25% duty cycle in the output frequency. The VFC121 is designed to give optimum linearity under these conditions, but other current levels can be used without significantly degrading linearity. By reducing R_{IN}, the integrating current is increased, increasing the positive ramp rate of the integrator output. Since the one-shot period is unchanged, the duty cycle of the output increases.

Stray capacitance at the C_{OS} pin typically adds about 60pF to the capacitance of the external C_{OS}, which accounts for the adjustment in the above equation. This usually becomes negligible as the required output frequency is reduced, and C_{OS} is increased.

R_{BIAS} is included in the circuit in Figure 3 to compensate for the effects of bias currents at the input of the integrating op amp. It is optional in most applications, but when needed, R_{BIAS} should equal R_{IN}.

Table 1 indicates standard external component values for common input voltage ranges and output frequency ranges.

COMPONENT SELECTION

Selection of the external resistor and capacitor type is important. Temperature drift of the external input resistor and one-shot capacitor will affect temperature stability of the output frequency. NPO ceramic capacitors will normally produce the best results. Silver-mica types will result in slightly higher drift, but may be adequate in many applications. A low temperature coefficient film resistor should be used for R_{IN}.

The integrator capacitor, C_{INT}, serves as a "charge bucket," where charge accumulation is induced by the input, V_{IN}, and

FULL SCALE INPUT RANGE (V)	$R_{IN} + R_{TRIM}$ (kΩ)	
2	8	
5	20	
10	40	
FULL SCALE OUTPUT FREQUENCY (kHz)	**C_{OS} (pF)**	**C_{INT} (pF)**
1500	22	150
1000	68	270
500	180	470
250	470	1000
125	1000	2200
25	4700	10,000
NOTE: Higher output frequencies can be achieved by reducing R_{IN}.		

TABLE 1. Standard External Component Values

repeatedly reduced during the one-shot period. The size of the bucket (the capacitor value) is not critical, since it primarily determines how far below V_{REF} the output of the integrator ramps during the one-shot period. At the same time, the capacitor used must not leak since capacitor leakage or dielectric absorption can affect the linearity and offset of the transfer function. High-quality ceramic capacitors can be used for values less than 0.01µF, but caution should be used with higher value ceramic capacitors. High-k ceramic capacitors may have voltage non-linearities which can degrade overall linearity. Polystyrene, polycarbonate, or mylar film capacitors are superior for higher capacitance values.

During the one-shot period, the output of the integrator is ramping down. To prevent the integrating op amp from being saturated at its minimum output of 0.8V, C_{INT} should be kept at least 1.7 x C_{OS}.

OUTPUT FREQUENCY ADJUSTMENT

The full scale output frequency of the VFC121 can be adjusted using a trim-pot, R_{TRIM} in Figure 3, in series with R_{IN}. For optimum drift vs temperature, a low temperature coefficient fixed resistor of approximately 90% of the calculated R_{IN} requirement should be used in series with a trim-pot approximately 20% of the size of the calculated R_{IN}. The low-drift fixed resistor contributes most of the final R_{IN} resistance, so that the effect of higher drift from the trim-pot is attenuated in the total R_{IN}.

PULL-UP RESISTOR

The VFC121's frequency output is an open-collector transistor. A pull-up resistor should be connected from f_{OUT} to the logic supply, $+V_L$. The output transistor is On during the one-shot period, causing the output to be logic Low. The current flowing in this resistor should be limited to 10mA to assure a 0.4V maximum logic Low. The value chosen for the pull-up resistor may depend on the full-scale frequency and capacitance on the output line. Excessive capacitance on f_{OUT} will cause a slow, rounded rising edge at the end of an output pulse. This effect can be minimized by using a pull-up resistor which sets the output current to its maximum of 10mA. The logic power supply can be any positive voltage up to +36V.

ENABLE PIN

If left unconnected, the Enable input will assume a logic Low level, enabling the output stage, Alternatively, the Enable input may be connected directly to ground. This pin can also be driven by standard TTL or CMOS logic.

A logic High at the Enable input causes output pulses to cease. This is accomplished by interrupting the signal path through the one-shot circuitry. While disabled, all circuitry remains active and quiescent current is unchanged. Since no reset current pulses can occur while disabled, any positive input voltage will cause the integrator op amp to ramp positive and saturate at its most positive output swing of approximately V_{REF} + 0.7V.

When the Enable input receives a logic Low (less than 0.8V), a reset current cycle is initiated, (causing f_{OUT} to go Low). The integrator ramps negatively and normal operation is established. The time required for the output frequency to stabilize is equal to approximately one cycle of the final output frequency plus 1µs.

Using the Enable input, the outputs from several VFCs can be connected to a single line. All disabled VFCs will have a high output impedance; one active VFC can then transmit on the line. Since disabled VFCs are not oscillating, they cannot interfere or "lock" with the operating VFC. Locking can occur when one VFC operates at nearly the same frequency, or a multiple, as a nearby VFC. Coupling between the two may cause them to lock to the same frequency or an exact multiple. It then takes a small incremental input voltage change on one of the VFCs to unlock them. Locking cannot occur when unneeded VFCs are disabled.

APPLICATION INFORMATION

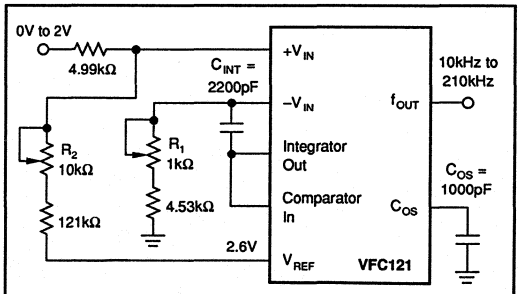
OPERATION FROM 10kHz TO 210kHz

The VFC121 is designed to provide an output frequency starting at 0Hz for a 0V input and increasing linearly to the full scale output frequency, f_{FS}, at the full scale input voltage, V_{FS}. For applications where low level inputs, near 0V, are critical, it may be inconvenient to have an output frequency approaching 0Hz. Figure 4 shows a circuit which transforms a 0V to 2V input level into output frequencies from 10kHz to 210kHz, by placing a resistor divider network between the input source and the V_{REF} output of the VFC121. This produces a positive voltage at $+V_{IN}$ when the input to the circuit is grounded. This circuit makes use of the high input impedance at $+V_{IN}$.

The transfer function of this circuit is:

$$V_{IN} = \frac{f_{OUT} - 10kHz}{100kHz} V$$

To trim the circuit, first apply 2V to the analog input, and adjust R_1 to give a full scale output frequency of 210kHz. Then apply 0V to the analog input, and adjust R_2 until the output frequency is 10kHz. For absolute precision, it may be necessary to make several iterations trimming R_1 and R_2. In most cases, one iteration will be enough, since the effect of R_2 on



NOTE: Use 1% metal film fixed resistors, Cermet® trim pots, and NPO ceramic capacitors.

FIGURE 4. Offsetting the Output Frequency.

full scale output frequency is attenuated by the divider network, which sees only a 0.6V total delta at full scale (2.6V at V_{REF} minus 2V full scale input) as compared with a 2.6V delta at a 0V input level.

USING THE VFC121 THERMOMETER VOLTAGE

Because of the high input impedance of the VFC121 (which results from using the non-inverting input to the integrating op amp), it is relatively simple to use a standard multiplexer in front of the VFC121. One of the possible reason to multiplex the input to the VFC121 is to use it to track temperature changes in the operating environment of the electronics in a system, in addition to using the VFC121 in its normal mode to measure an analog signal.

Figure 5 shows a way to do this. In this circuit, the normal analog input signals to be multiplexed through the VFC121 have a full scale voltage of 2V, and generate a full scale output frequency of 100kHz. To measure the electronics system temperature, the user selects the multiplexer channel connected to the thermometer voltage on pin 3. A measured output frequency from the VFC121, with the multiplexer on channel 8, now corresponds to the temperature of the electronics as follows:

$$\text{Temp (°C)} = \frac{\text{Output Frequency} - 13{,}650}{50}$$

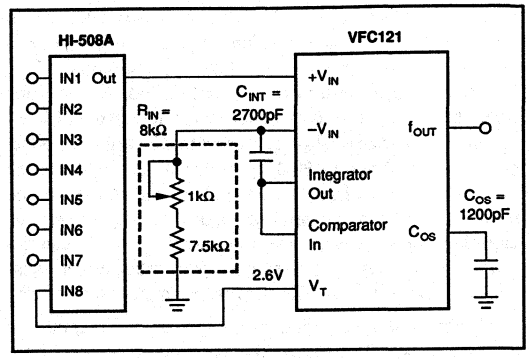


FIGURE 5. Measuring System Temperature.

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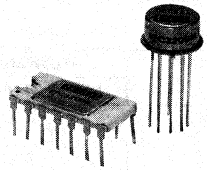


VFC320

AVAILABLE IN DIE

Voltage-to-Frequency and Frequency-to-Voltage CONVERTER

FEATURES

- HIGH LINEARITY, 12 to 14 bits
  ±0.005% max at 10kHz FS
  ±0.03% max at 100kHz FS
  ±0.1% typ at 1MHz FS
- V/F OR F/V CONVERSION
- 6-DECADE DYNAMIC RANGE
- 20ppm/°C max GAIN DRIFT
- OUTPUT TTL/CMOS COMPATIBLE

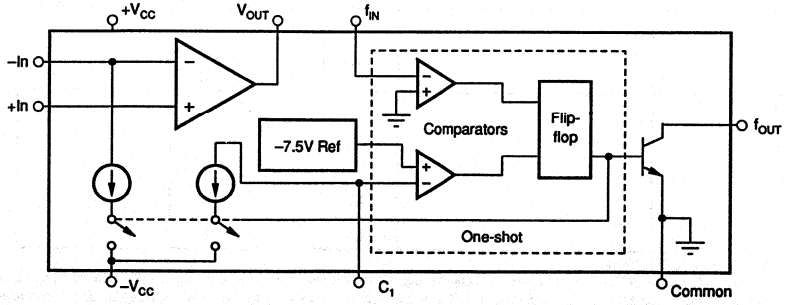
APPLICATIONS

- INEXPENSIVE A/D AND D/A CONVERTER
- DIGITAL PANEL METERS
- TWO-WIRE DIGITAL TRANSMISSION WITH NOISE IMMUNITY
- FM MOD/DEMOD OF TRANSDUCER SIGNALS
- PRECISION LONG TERM INTEGRATOR
- HIGH RESOLUTION OPTICAL LINK FOR ISOLATION
- AC LINE FREQUENCY MONITOR
- MOTOR SPEED MONITOR AND CONTROL

DESCRIPTION

The VFC320 monolithic voltage-to-frequency and frequency-to-voltage converter provides a simple low cost method of converting analog signals into digital pulses. The digital output is an open collector and the digital pulse train repetition rate is proportional to the amplitude of the analog input voltage. Output pulses are compatible with TTL, and CMOS logic families.

High linearity (0.005%, max at 10kHz FS) is achieved with relatively few external components. Two external resistors and two external capacitors are required to operate. Full scale frequency and input voltage are determined by a resistor in series with –In and two capacitors (one-shot timing and input amplifier integration). The other resistor is a non-critical open collector pull-up (f_{OUT} to $+V_{CC}$). The VFC320 is available in three performance/temperature grades and two package configurations. The TO-100 versions are hermetically sealed, and specified for the –25°C to +85°C and –55°C to +125°C ranges, and the dual-in-line units are specified from –25°C to +85°C.



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Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

At T_A = +25°C and ±15VDC power supply, unless otherwise noted.

PARAMETER	CONDITIONS	VFC320BG/BM/SM MIN	VFC320BG/BM/SM TYP	VFC320BG/BM/SM MAX	VFC320CG/CM MIN	VFC320CG/CM TYP	VFC320CG/CM MAX	UNITS
V/F CONVERTER $f_{OUT} = V_{IN}/7.5\ R_1C_1$, Figure 4								
INPUT TO OP AMP								
Voltage Range[1]	Fig. 4 with $e_2 = 0$	>0		Note 2				V
	Fig. 4 with $e_1 = 0$	<0		–10				V
Current Range[1]	$I_{IN} = V_{IN}/R_{IN}$	+0.25		+750	*		*	µA
Bias Current								
Inverting Input			4	8		*	*	nA
Noninverting Input			10	30		*	*	nA
Offset Voltage[3]				±0.15			*	mV
Offset Voltage Drift			±5			*		µV/°C
Differential Impedance		300 || 5	650 || 5		*	*		kΩ || pF
Common-Mode Impedance		300 || 3	500 || 3		*	*		kΩ || pF
ACCURACY								
Linearity Error[1][4][5]	Fig. 4 with $e_2 = 0$[6]							
	0.01Hz ≤ f_{OUT} ≤ 10kHz		±0.004	±0.005		±0.0015	±0.002	% FSR
	0.1Hz ≤ f_{OUT} ≤ 100kHz		±0.008	±0.030		*	*	% FSR
	1Hz ≤ f_{OUT} ≤ 1MHz		±0.1			*		% FSR
Offset Error Input Offset Voltage[3]				±15			*	ppm FSR
Offset Drift[7]			±0.5			*		ppm FSR/°C
Gain Error[3]			±5	±10		*	*	% FSR
Gain Drift[7]	f = 10kHz			50			20	ppm FSR/°C
Full Scale Drift (Offset Drift and Gain Drift)[7][8][9]	f = 10kHz			50			20	ppm FSR/°C
Power Supply Sensitivity	±V_{CC} = 14VDC to 18VDC			±0.015			*	% FSR%
DYNAMIC RESPONSE								
Full Scale Frequency	C_{LOAD} ≤ 50pF			1			*	MHz
Dynamic Range		6			*			Decades
Settling Time	(V/F) to Specified Linearity For a Full Scale Input Step		Note 10			*		
Overload Recovery	<50% Overload		Note 10			*		
OPEN COLLECTOR OUTPUT								
Voltage, Logic "0"	I_{SINK} = 8mA, max			0.4			*	V
Leakage Current, Logic "1"	V_O = 15V		0.01	1.0		*	*	µA
Voltage, Logic "1"	External Pull-up Resistor Required (See Figure 4)			V_{PU}			*	V
Duty Cycle at FS	For Best Linearity		25			*		%
Fall Time	I_{OUT} = 5mA, C_{LOAD} = 500pF		100			*		ns
F/V CONVERTER $V_{OUT} = 7.5\ R_1C_1\ f_{IN}$, Figure 9								
INPUT TO COMPARATOR								
Impedance		50 || 10	150 || 10		*	*		kΩ || pF
Logic "1"		+1.0		+V_{CC}	*		*	V
Logic "0"		–V_{CC}		–0.05	*		*	V
Pulse-width Range		0.25			*			µs
OUTPUT FROM OP AMP								
Voltage	I_O = 6mA	0 to +10			*			V
Current	V_O = 7VDC	+10			*			mA
Impedance	Closed-Loop			0.1			*	Ω
Capacitive Load	Without Oscillation			100			*	pF
POWER SUPPLY								
Rated Voltage			±15			*		V
Voltage Range		±13		±20	*		*	V
Quiescent Current			±6.5	±7.5		*	*	mA
TEMPERATURE RANGE								
Specification								
B and C Grades		–25		+85	*		*	°C
S Grade		–55		+125				°C
Operating								
B and C Grades		–25		+85	*		*	°C
S Grade		–55		+125				°C
Storage		–65		+150	*		*	°C

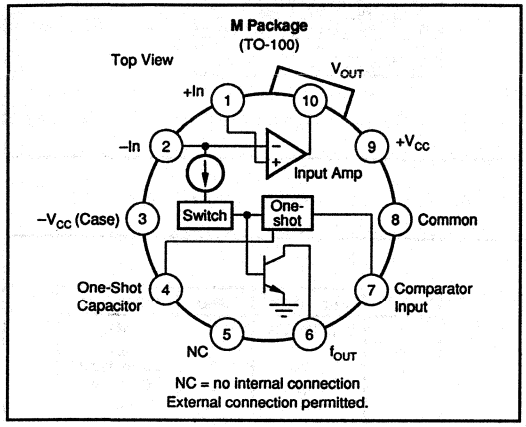
* Specification the same as for VFC320BG/BM/SM.

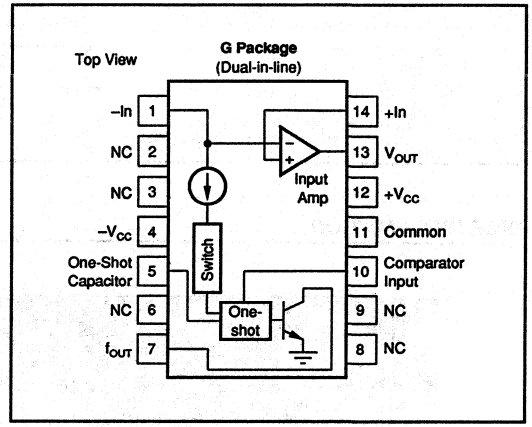
NOTES: (1) A 25% duty cycle at full scale (0.25mA input current) is recommended where possible to achieve best linearity. (2) Determined by R_{IN} and full scale current range constraints. (3) Adjustable to zero. See Offset and Gain Adjustment section. (4) Linearity error at any operating frequency is defined as the deviation from a straight line drawn between the full scale frequency and 0.1% of full scale frequency. See Discussion of Specifications section. (5) When offset and gain errors are nulled, at an operating temperature, the linearity error determines the final accuracy. (6) For e_1 = 0 typical linearity errors are: 0.01% at 10kHz, 0.2% at 100kHz, 0.1% at 1MHz. (7) Exclusive of external components' drift. (8) FSR = Full Scale Range (corresponds to full scale and full scale input voltage.) (9) Positive drift is defined to be increasing frequency with increasing temperature. (10) One pulse of new frequency plus 50ns typical.

ABSOLUTE MAXIMUM RATINGS

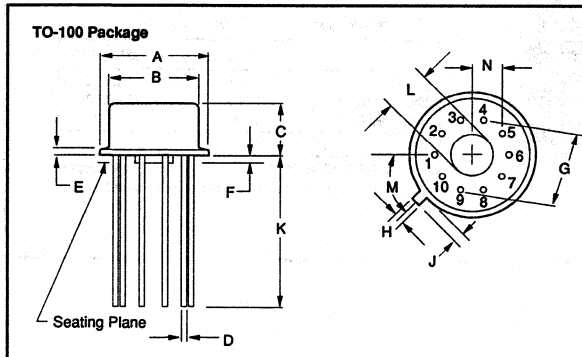
Supply Voltage	±20V
Output Sink Current at f_{OUT}	50mA
Output Current at V_{OUT}	+20mA
Input Voltage, –Input	$\pm V_{CC}$
Input Voltage, +Input	$\pm V_{CC}$
Storage Temperature Range	–65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C

CONNECTION DIAGRAM





MECHANICAL



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.335	.370	8.51	9.40
B	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.230 BASIC		5.84 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500	—	12.70	—
L	.120	.160	3.05	4.06
M	36° BASIC		36° BASIC	
N	.110	.120	2.79	3.05

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only.

ORDERING INFORMATION

MODEL	DESCRIPTION	TEMPERATURE RANGE
VFC320BG	Ceramic DIP	–25°C to +85°C
VFC320BM	TO-100	–25°C to +85°C
VFC320SM	TO-100	–55°C to +125°C
VFC320CG	Ceramic DIP	–25°C to +85°C
VFC320CM	TO-100	–25°C to +85°C

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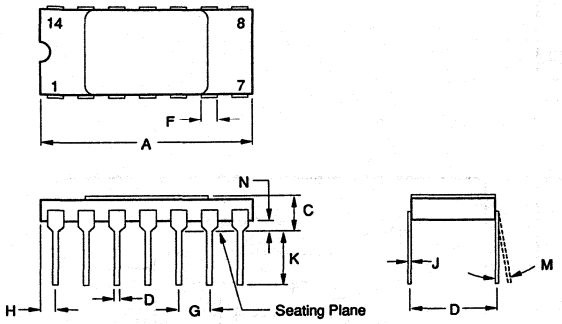
MECHANICAL

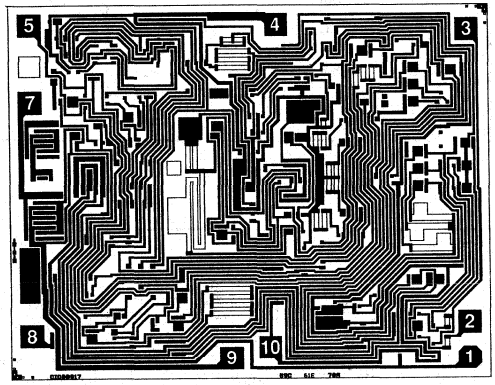
G Package — 14-Pin Hermetic DIP



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	.670	.710	17.02	18.03
C	.065	.170	1.65	4.32
D	.015	.021	0.38	0.53
F	.045	.060	1.14	1.52
G	.100 BASIC		2.54 BASIC	
H	.025	.070	0.64	1.78
J	.008	.012	0.20	0.30
K	.120	.240	3.05	6.10
L	.300 BASIC		7.62 BASIC	
M	—	10°	—	10°
N	.009	.060	0.23	1.52

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.

DICE INFORMATION



VCF320 DIE TOPOGRAPHY

PAD	FUNCTION	PAD	FUNCTION
1	V_{OUT} (Int. Out)	6	NC
2	+In	7	f_{OUT}
3	–In	8	Comp. Input
4	$-V_{CC}$	9	Common
5	One-Shot Cap.	10	$+V_{CC}$

NC: No Connection.
Substrate Bias: Electrically connected to $-V_S$ supply.

MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	109 x 87 ±5	2.77 x 2.21 ±0.13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.1 x 0.1
Backing	Gold	

See "DICE PRODUCTS" Section 17 in Data Book Supplement Volume 33c, or contact Burr-Brown for current information.

DISCUSSION OF SPECIFICATIONS

LINEARITY

Linearity is the maximum deviation of the actual transfer function from a straight line drawn between the end points (100% full scale input or frequency and 0.1% of full scale called zero.) Linearity is the most demanding measure of voltage-to-frequency converter performance, and is a function of the full scale frequency. Refer to Figure 1 to determine typical linearity error for your application. Once the full scale frequency is chosen, the linearity is a function of operating frequency as it varies between zero and full scale. Examples for 10kHz full scale are shown in Figure 2. Best linearity is achieved at lower gains ($\Delta f_{OUT}/\Delta_{VIN}$) with operation as close to the chosen full scale frequency as possible

The high linearity of the VFC320 makes the device an excellent choice for use as the front end of A/D converters with 12- to 14-bit resolution, and for highly accurate transfer of analog data over long lines in noisy environments (2-wire digital transmission.)

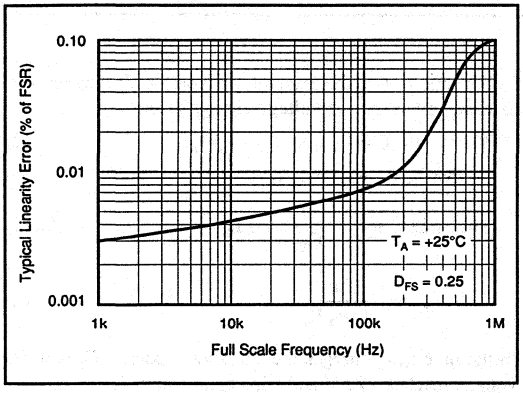


Figure 1. Linearity Error vs Full Scale Frequency.

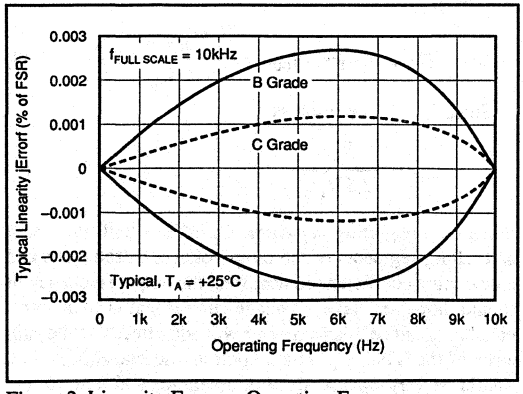


Figure 2. Linearity Error vs Operating Frequency.

FREQUENCY STABILITY VS TEMPERATURE

The full scale frequency drift of the VFC320 versus temperature is expressed as parts per million of full scale range per °C. As shown in Figure 3, the drift increases above 10kHz. To determine the total accuracy drift over temperature, the drift coefficients of external components (especially R_1 and C_1) must be added to the drift of the VFC320.

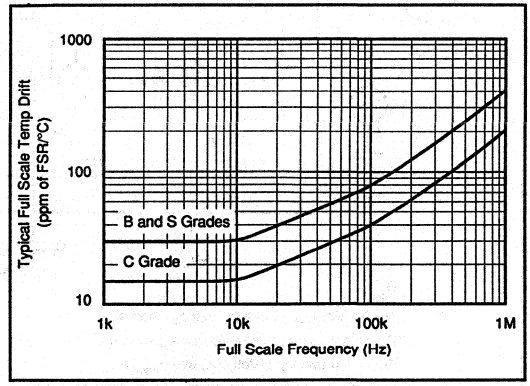


Figure 3. Full Scale Drift vs Full Scale Frequency.

RESPONSE

Response of the VFC320 to changes in input signal level is specified for a full scale step, and is 50ns plus 1 pulse of the new frequency. For a 10V input signal step with the VFC320 operating at 100kHz full scale, the settling time to within ±0.01% of full scale is 10µs.

THEORY OF OPERATION

The VFC320 monolithic voltage-to-frequency converter provides a digital pulse train output whose repetition rate is directly proportional to the analog input voltage. The circuit shown in Figure 4 is composed of an input amplifier, two comparators and a flip-flop (forming a on-shot), two switched current sinks, and an open collector output transistor stage. Essentially the input amplifier acts as an integrator that produces a two-part ramp. The first part is a function of the input voltage, and the second part is dependent on the input voltage and current sink. When a positive input voltage is applied at V_{IN}, a current will flow through the input resistor, causing the voltage at V_{OUT} to ramp down toward zero, according to $dV/dt = V_{IN}/R_1C_1$. During this time the constant current sink is disabled by the switch. Note, this period is only dependent on V_{IN} and the integrating components.

When the ramp reaches a voltage close to zero, comparator A sets the flip-flop. This closes the current sink switches as well as changing f_{OUT} from logic 0 to logic 1. The ramp now begins to ramp up, and 1mA charges through C_1 until V_{C1} = –7.5V. Note this ramp period is dependent on the 1mA current sink, connected to the negative input of the op amp, as well as the input voltage. At this –7.5V threshold point C_1, comparator B resets the flip-flop, and the ramp voltage

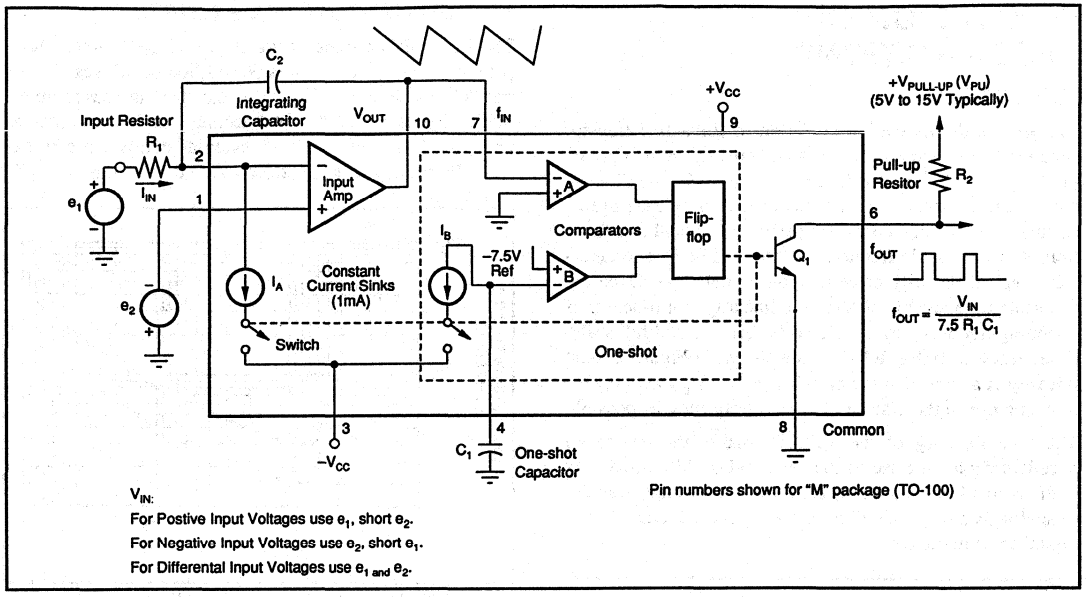


FIGURE 4. Functional Block Diagram of the VFC320.

begins to ramp down again before the input amplifier has a chance to saturate. In effect the comparators and flip-flop form a one-shot whose period is determined by the internal reference and a 1mA current sink plus the external capacitor, C_1. After the one-shot resets, f_{OUT} changes back to logic 0 and the cycle begins again.

The transfer function for the VFC320 is derived for the circuit shown in Figure 4. Detailed waveforms are shown in Figure 5.

$$f_{OUT} = \frac{1}{t_1 + t_2} \qquad (1)$$

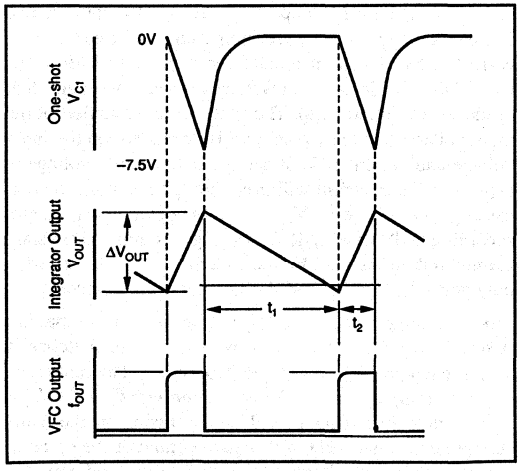


FIGURE 5. Integrator and VFC Output Timing.

In the time $t_1 + t_2$ the integrator capacitor C_2 charges and discharges but the net voltage change is zero.

Thus $\Delta Q = 0 = I_{IN}\, t_1 + (I_{IN} - I_A)\, t_2$ (2)

So that $I_{IN}\,(t_1 + t_2) = I_A\, t_2$ (3)

But since $t_1 + t_2 = \dfrac{1}{f_{OUT}}$ and $I_{IN} = \dfrac{V_{IN}}{R_1}$ (4), (5)

$$f_{OUT} = \frac{V_{IN}}{I_A R_2 R_2} \qquad (6)$$

In the time t_1, I_B charges the one-shot capacitor C_1 until its voltage reaches –7.5V and trips comparator B.

Thus $t_2 = \dfrac{C_{IN} 7.5}{I_B}$ (7)

Using (7) in (6) yield $f_{OUT} = \dfrac{V_{IN}}{7.5\, R_1\, C_1} \times \dfrac{I_B}{I_A}$ (8)

Since $I_A = I_B$ the result is

$$f_{OUT} = \frac{V_{IN}}{7.5\, R_1\, C_1} \qquad (9)$$

Since the integrating capacitor, C_2, affects both the rising and falling segments of the ramp voltage, its tolerance and temperature coefficient do not affect the output frequency. It should, however, have a leakage current that is small compared to I_{IN}, since this parameter will add directly to the gain error of the VFC. C_1, which controls the one-shot period, should be very precise since its tolerance and temperature coefficient add directly to the errors in the transfer function.

The operation of the VFC320 as a highly linear frequency-to-voltage converter, follows the same theory of operation as the voltage-to-frequency converter. e_1 and e_2 are shorted and F_{IN} is disconnected from V_{OUT}. F_{IN} is then driven with a signal which is sufficient to trigger comparator A. The one-shot period will then be determined by C_1 as before, but the cycle repetition frequency will be dictated by the digital input at F_{IN}.

DUTY CYCLE

The duty cycle (D) of the VFC is the ratio of the one-shot period (t_2) or pulse width, PW, to the total VFC period ($t_1 + t_2$). For the VFC320, t_2 is fixed and $t_1 + t_2$ varies as the input voltage. Thus the duty cycle, D, is a function of the input voltage. Of particular interest is the duty cycle at full scale frequency, D_{FS}, which occurs at full scale input. D_{FS} is a user determined parameter which affects linearity.

$$D_{FS} = \frac{t_2}{t_1 + t_2} = PW \times f_{FS}$$

Best linearity is achieved when D_{FS} is 25%. By reducing equations (7) and (9) it can be shown that

$$D_{FS} = \frac{V_{IN}\,max / R_1}{1mA} = \frac{I_{IN}\,max}{1mA}$$

Thus $D_{FS} = 0.25$ corresponds to I_{IN} max = 0.25mA.

INSTALLATION AND OPERATING INSTRUCTIONS

VOLTAGE-TO-FREQUENCY CONVERSION

The VCF320 can be connected to operate as a V/F converter that will accept either positive or negative input voltages, or an input current. Refer to Figures 6 and 7.

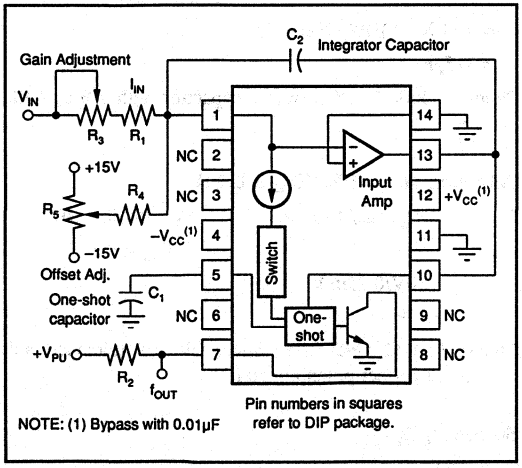


FIGURE 6. Connection Diagram for V/F Conversion, Positive Input Voltages.

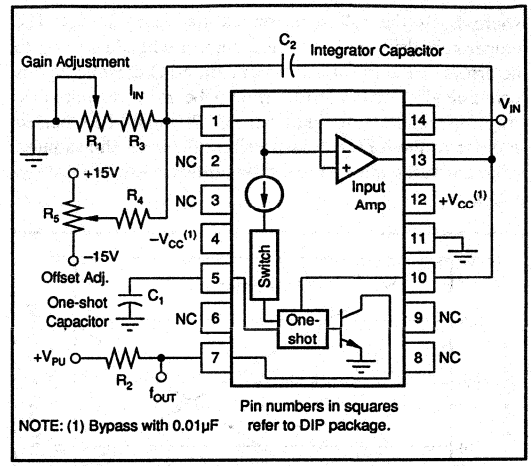


FIGURE 7. Connection Diagram for V/F Conversion, Negative Input Voltages.

EXTERNAL COMPONENT SELECTION

In general, the design sequence consists of: (1) choosing f_{MAX}, (2) choosing the duty cycle at full scale ($D_{FS} = 0.25$ typically), (3) determining the input resistor, R_1 (Figure 4), (4) calculating the one-shot capacitor, C_1, (5) selecting the integrator capacitor C_2, and (6) selecting the output pull-up resistor, R_2.

Input Resistors R_1 and R_3

The input resistance (R_1 and R_3 in Figures 6 and 7) is calculated to set the desired input current at full scale input voltage. This is normally 0.25mA to provide a 25% duty cycle at full scale input and output. Values other than $D_{FS} = 0.25$ may be used but linearity will be affected.

The nominal value is R_1 is

$$R_1 = \frac{V_{IN}max}{0.25mA} \qquad (10)$$

If gain trimming is to be done, the nominal value is reduced by the tolerance of C_1 and the desired trim range. R_1 should have a very-low temperature coefficient since its drift adds directly to the errors in the transfer function.

One-Shot Capacitor, C_1

This capacitor determines the duration of the one-shot pulse. From equation (9) the nominal value is

$$C_{1\,NOM} = \frac{V_{IN}}{7.5\,R_1\,f_{OUT}} \qquad (11)$$

For the usual 25% duty at $f_{MAX} = V_{IN}/R_1 = 0.25mA$ there is approximately 15pF of residual capacitance so that the design value is

$$C_1(pF) = \frac{33 \times 10^6}{f_{FS}} - 15 \qquad (12)$$

where f_{FS} is the full scale output frequency in Hz. The temperature drift of C_1 is critical since it will add directly to the errors of the transfer function. An NPO ceramic type is recommended. Every effort should be made to minimize stray capacitance associated with C_1. It should be mounted as close to the VFC320 as possible. Figure 8 shows pulse width and full scale frequency for various values of C_1 at D_{FS} = 25%.

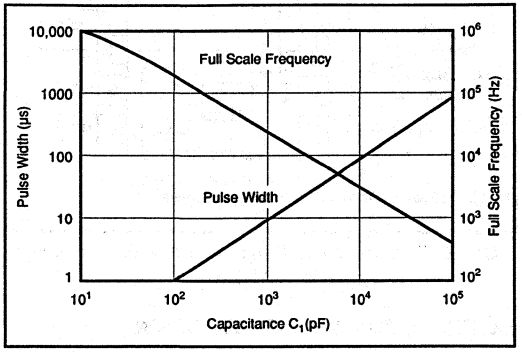


FIGURE 8. Output Pulse Width (D_{FS} = 0.25) and Full Scale Frequency vs External One-shot Capacitance.

Integrating Capacitor, C_2

Since C_2 does not occur in the V/F transfer function equation (9), its tolerance and temperature stability are not important; however, leakage current in C_2 causes a gain error. A ceramic type is sufficient for most applications. The value of C_2 determines the amplitude of V_{OUT}. Input amplifier saturation, noise levels for the comparators and slew rate limiting of the integrator determine a range of acceptable values,

$$C_2\ (\mu F) = \begin{cases} 100/f_{FS};\ \text{if } f_{FS} \le 100\text{kHz} \\ 0.001;\ \text{if } 100\text{kHz} < f_{FS} \le 500\text{kHz} \\ 0.0005;\ \text{if } f_{FS} > 500\text{kHz} \end{cases} \quad (13)$$

Output Pull Up Resistor R_2

The open collector output can sink up to 8mA and still be TTL-compatible. Select R_2 according to this equation:

$$R_2\ \text{min}\ (\Omega)\ V_{PULLUP}/(8\text{mA} - I_{LOAD})$$

A 10% carbon film resistor is suitable for use as R_2.

Trimming Components R_3, R_4, R_5

R_5 nulls the offset voltage of the input amplifier. It should have a series resistance between 10kΩ and 100kΩ and a temperature coefficient less than 100ppm/°C. R_4 can be a 10% carbon film resistor with a value of 10MΩ.

R_3 nulls the gain errors of the converter and compensates for initial tolerances of R_1 and C_1. Its total resistance should be at least 20% of R_1, if R_1 is selected 10% low. Its temperature coefficient should be no greater than five times that of R_1 to maintain a low drift of the R_3 - R_1 series combination.

OFFSET AND GAIN ADJUSTMENT PROCEDURES

To null errors to zero, follow this procedure:

1. Apply an input voltage that should produce an output frequency of 0.001 X full scale.
2. Adjust R_5 for proper output.
3. Apply the full scale input voltage.
4. Adjust R_3 for proper output.
5. Repeat stems 1 through 4.

If nulling is unnecessary for the application, delete R_4 and R_5, and replace R_3 with a short circuit.

POWER SUPPLY CONSIDERATIONS

The power supply rejection ratio of the VFC320 is 0.015% of FSR/% max. To maintain ±0.015% conversion, power supplies which are stable to within ±1% are recommended. These supplies should be bypassed as close as possible to the converter with 0.01µF capacitors.

Internal circuitry causes some current to flow in the common connection (pin 11 on DIP package). Current flowing into the f_{OUT} pin (logic sink current) will also contribute to this current. It is advisable to separate this common lead ground from the analog ground associated with the integrator input to avoid errors produced by these currents flowing through any ground return impedance.

DESIGN EXAMPLE

Given a full scale input of +10V, select the values of R_1, R_2, R_3, C_1, and C_2 for a 25% duty cycle at 100kHz maximum operation into one TTL load. See Figure 6.

Selecting C_1 (D_{FS} = 0.25)

$C_1 = [(33 \text{ X } 10^6)/f_{MAX}] - 15$ $\quad [(66 \text{ X } 10^6)/f_{MAX}] - 15$ if D_{FS} = 0.5

$= [(33 \text{ X } 10^6)/100\text{kHz}] - 15$

$= 315\text{pF}$

Choose a 300pF NPO ceramic capacitor with 1% to 10% tolerance.

Selecting R_1 and R_3 (D_{RS} = 0.25)

$R_1 + R_3 = V_{IN}$ max/0.25mA $\quad V_{IN}$ max/0.5mA if D_{FS} = 0.5

$= 10\text{V}/0.25\text{mA}$

$= 40\text{k}\Omega$

Choose 32.4kΩ metal film resistor with 1% tolerance and R_3 = 10kΩ cermet potentiometer.

Selecting C_2

$C_2 = 10^2/F_{MAX}$

$= 10^2/100\text{kHz}$

$= 0.001\mu\text{F}$

Choose a 0.001µF capacitor with ±5% tolerance.

Selecting R_2

$R_2 = V_{PULLUP}/(8mA - I_{LOAD})$

$=5V/(8mA - 1.6mA)$, one TTL-load = 1.6mA

$=781\Omega$

Choose a 750Ω 1/4-watt carbon compensation resistor with ±5% tolerance.

FREQUENCY-TO-VOLTAGE CONVERSION

To operate the VFC320 as a frequency-to-voltage converter, connect the unit as shown in Figure 9. To interface with TTL-logic, the input should be coupled through a capacitor, and the input to pin 10 biased near +2.5V. The converter will detect the falling edges of the input pulse train as the voltage at pin 10 crosses zero. Choose C_3 to make t = 0.1t (see Figure 9). For input signals with amplitudes less than 5V, pin 10 should be biased closer to zero to insure that the input signal at pin 10 crosses the zero threshold.

Errors are nulled using 0.001 X full scale frequency to null offset, and full scale frequency to null the gain error. The procedure is given on this page. Use equations from V/F calculations to find R_1, R_3, R_4, C_1 and C_2.

TYPICAL APPLICATIONS

Excellent linearity, wide dynamic range, and compatible TTL, DTL, and CMOS digital output make the VFC320 ideal for a variety of VFC applications. High accuracy allows the VFC320 to be used where absolute or exact readings must be made. It is also suitable for systems requiring high resolution up to 14 bits

Figures 10-14 show typical applications of the VFC320.

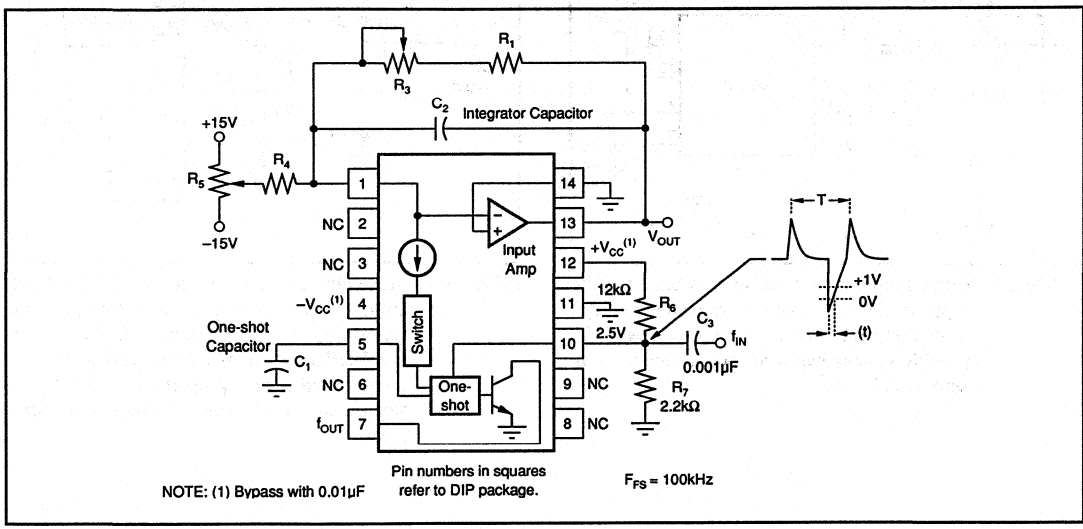


FIGURE 9. Connection Diagram for F/V Conversion.

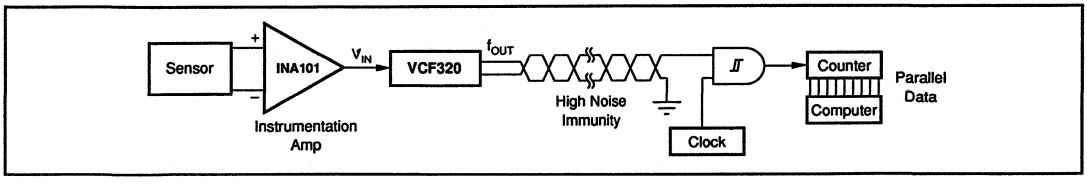


FIGURE 10. Inexpensive A/D with Two-Wire Digital Transmission Over Twisted Pair.

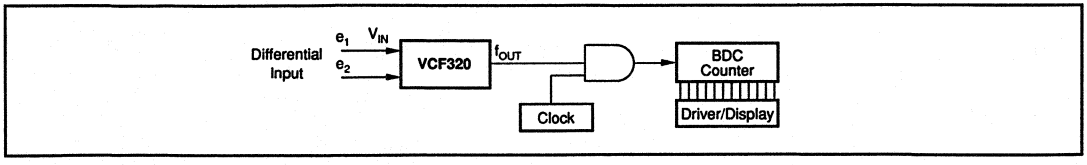


FIGURE 11. Inexpensive Digital Panel Meter.

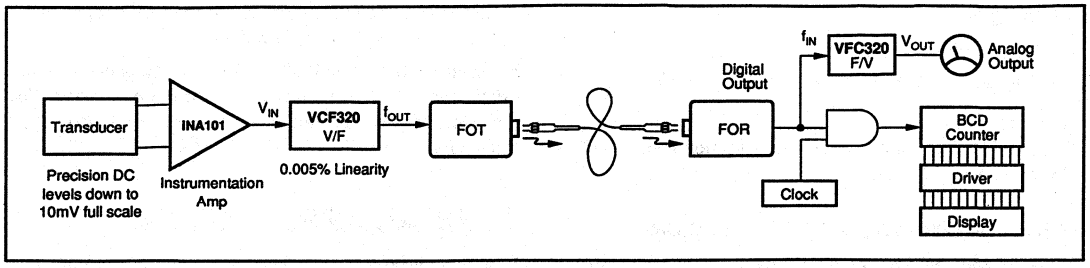


FIGURE 12. Remote Transducer Readout via Fiber Optic Link (Analog and Digital Output).

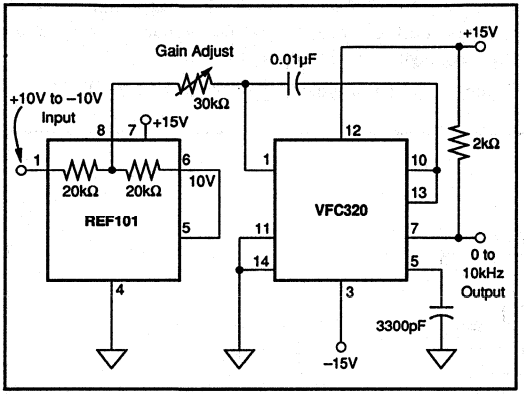


FIGURE 13. Bipolar input is accomplished by offsetting the input to the VFC with a reference voltage. Accurately matched resistors in the REF101 provide a stable half-scale output frequency at zero volts input.

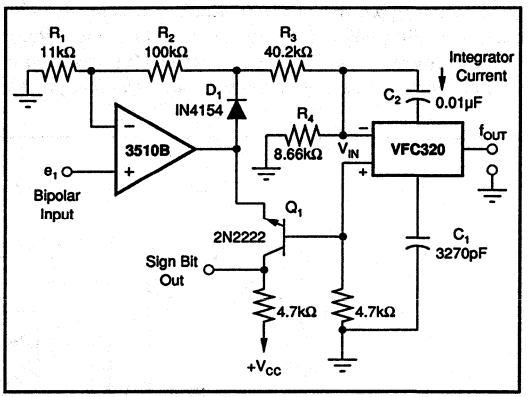


FIGURE 14. Absolute value circuit with the VFC320. Op amp, D_1 and Q_1 (its base-emitter junction funtioning as a diode) provide full-wave rectification of bipolar input voltages. VFC output frequency is proportional to $|e_1|$. The sign bit output provides indication of the input polarity.

11 Data Acquisition Components

If your system requires data acquisition and conversion, you may want to consider one of our system data modules (SDM). These products contain a multiplexer, A/D converter, and timing and control logic, with instrumentation amplifiers and sample/hold circuits also available.

As with all Burr-Brown conversion products, these units are designed to provide a total solution. They are very popular in applications requiring rapid design turnaround because they offer a fully optimized analog circuit layout. Typical applications include industrial measurement and control (such as process monitoring), test equipment, and any other application requiring total guaranteed performance with a minimum of utilized space.

The Selection Guide shows parameters for the high grade. Models shown in **boldface** are products included in this supplement.

DATA ACQUISITION COMPONENTS — **Boldface = NEW**

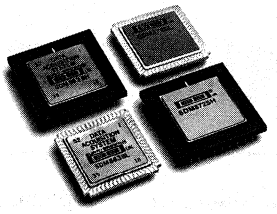
Model	Channels	Resolution (Bits)	Linearity Error (%FSR)	Input Range (V)[1]	Throughput Rate (kHz)	Temp Range[2]	Pkg[3]	Page No.
SDM862	**16 single ended**	**12**	**±0.012**	**±5, ±10, +10**	**33**	**Com, Ind, Mil**	**LCC, PGA**	**S-11.2**
SDM863	**8 differential**	**12**	**±0.012**	**±5, ±10, +10**	**33**	**Com, Ind, Mil**	**LCC, PGA**	**S-11.2**
SDM872	**16 single ended**	**12**	**±0.012**	**±5, ±10, +10**	**50**	**Com, Ind, Mil**	**LCC, PGA**	**S-11.2**
SDM873	**8 differential**	**12**	**±0.012**	**±5, ±10, +10**	**50**	**Com, Ind, Mil**	**LCC, PGA**	**S-11.2**

NOTES: (1) Internal instrumentation amplifier can be pin programmed for G = 1, 10, 100. (2) Temperature Range: Com = 0°C to +70°C, Ind = –25°C to +85°C, Mil = –55°C to +125°C. (3) LCC = Hermetic 0.95" (typ) square Leadless Chip Carrier, PGA = Hermetic 1.1" (typ) square Pin Grid Array

MODELS STILL AVAILABLE BUT NOT FEATURED IN IC DATA BOOK OR SUPPLEMENT

SDM854AG
SDM854BG
SDM856JG
SDM856KG
SDM857JG
SDM857KG

BURR-BROWN®



SDM862
SDM863
SDM872
SDM873

16 Single Ended/8 Differential Input 12-BIT DATA ACQUISITION SYSTEMS

FEATURES

- COMPLETE 12-BIT DATA ACQUISITION SYSTEM IN A MINIATURE PACKAGE
- INPUT RANGES SELECTABLE FOR UNIPOLAR OR BIPOLAR OPERATION
- THROUGHPUT RATES:

	862/3	872/3
8-BIT ACCURACY:	45kHz	67kHz
12-BIT ACCURACY:	33kHz	50kHz

- SELECTABLE GAINS OF 1, 10, AND 100
- FULL MICROPROCESSOR COMPATIBLE INTERFACE
- GUARANTEED NO MISSING CODES OVER TEMPERATURE
- SURFACE-MOUNT OR PIN GRID ARRAY PACKAGE OPTIONS
- HIGH RELIABILITY SCREENED VERSIONS AVAILABLE
- FULL SPECIFICATION OVER THREE TEMPERATURE RANGES: 0 to +70°C, –25 to +85°C, –55 to +125°C
- EVERY UNIT SUPPLIED WITH ELECTRICAL TEST DATA

APPLICATIONS

- INDUSTRIAL PROCESS MONITORING
- AIRBORNE SYSTEMS MONITORING
- ENGINE MONITORING
- POWER PLANT MONITORING
- SECURITY SYSTEMS MONITORING
- AUTOMATIC TEST EQUIPMENT

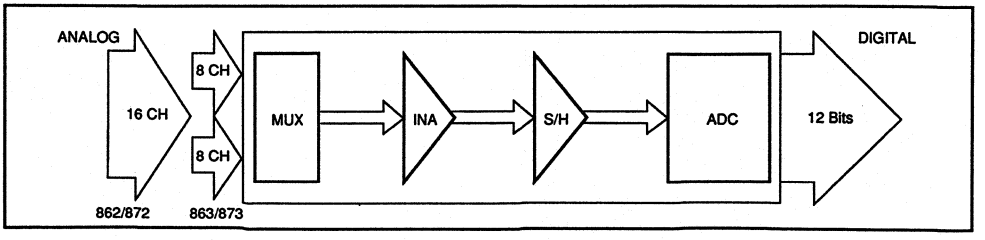
DESCRIPTION

16 Single-Ended Inputs:	SDM862	SDM872
8 Differential Inputs:	SDM863	SDM873
33kHz Throughput Rate:	SDM862	SDM863
50kHz Throughput Rate:	SDM872	SDM873

The SDM components are complete, pin-compatible, data acquisition systems housed in a hermetically sealed 1"-square leadless chip carrier or a 1.1"-square pin grid array. The small package outlines and low power consumption provide an ideal data acquisition solution when space is at a premium.

The devices comprise of an input multiplexer, instrumentation amplifier with selectable gains, sample/hold amplifier and A/D converter with microprocessor interface and three-state buffers.

The SDM family will accept unipolar or bipolar voltage inputs in the range 0 to +10V, ±5V and ±10V. For low-level signals, jumper-selectable gains of 10 or 100 can be applied. The number of input channels can be expanded by the addition of multiplexers. System integration is simplified by the microprocessor interface and the facility of the sample/hold amplifier being controlled directly by the A/D converter.



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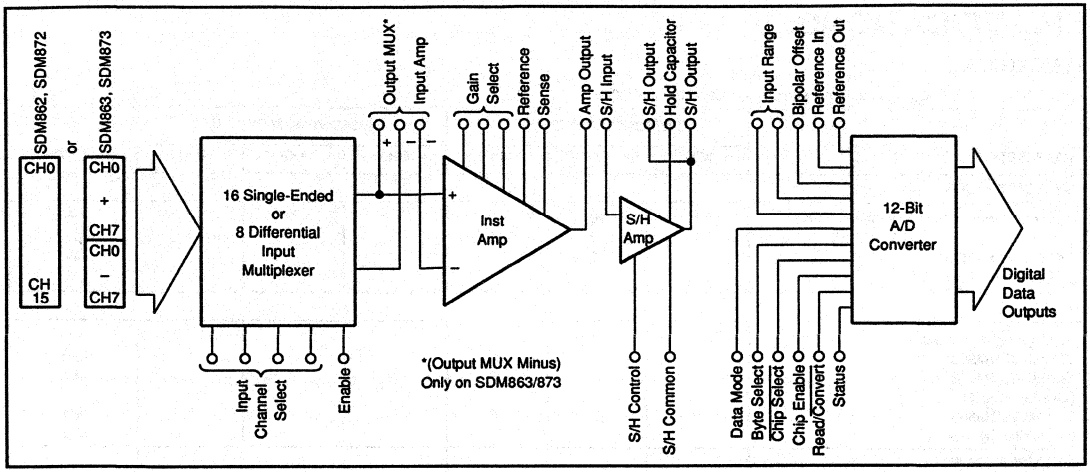


SPECIFICATIONS

ELECTRICAL

At +25°C, V_{CC} = ±15V, V_{DD} = 5V, external sample/hold capacitor of 4700pF. **All grades are burned-in at +125°C for 48 hours min.**

PARAMETER	SDM862/863/872/873 J, A, R MIN	SDM862/863/872/873 J, A, R TYP	SDM862/863/872/873 J, A, R MAX	SDM862/863/872/873 K, B, S MIN	SDM862/863/872/873 K, B, S TYP	SDM862/863/872/873 K, B, S MAX	UNITS
RESOLUTION			12			*	BITS
INPUT							
ANALOG							
Voltage Ranges: Bipolar			±5, ±10				V
Unipolar			0-10				V
Input Impedance: On Channel		10^{10}			*		Ω
Off Channel		10^{10}			*		Ω
Input Capacitance: On Channel		20			*		pF
Off Channel		20			*		pF
CMRR (20VDC to 1kHz)	80	85		*	*		dB
Crosstalk (20Vp-p, 1kHz) [1]		–85	–80		*	*	dB
Feedthrough (at 1kHz) [1]		–85	–80		*	*	dB
Offset (channel to channel) G = 1 [2]		30	100		*	*	µV
Input Bias Current/Channel		1	5		*	*	nA
Input Voltage Range [3]	+10	+11		*	*		V
	–10	–15		*	*		V
DIGITAL							
MUX Input Channel Select: Logic '1'		5	30		*	*	µA
Logic '0'		5	30		*	*	µA
MUX Input: Logic High	4.0			*			V
Logic Low			0.8			*	V
S/H Command: Logic '1'		0.2			*		nA
Logic '0'		5	30		*	*	µA
ADC Section: Logic '1'			10			*	µA
Logic '0'			10			*	µA
TRANSFER CHARACTERISTICS							
ACCURACY							
Integral Linearity [4]			±0.024			±0.012	%FSR
Differential Linearity [4]			±0.024			*	%FSR
No Missing Codes		Over Operating Temperature Range					
Gain Error [5]: G = 1			0.5			*	%
G = 100		0.9			*		%
Unipolar Offset Error [5]		16			*		mV
Bipolar Offset Error [5]			50			*	mV
Noise Error							
(Measured at S/H Output) G = 1		0.5	1		*	*	mVp-p
Droop Rate		50	500		*	*	µV/ms
Temperature Coefficients:							
Unipolar Offset			20			15	ppm of FSR/°C
Bipolar Offset			30			25	ppm of FSR/°C
Full-Scale Calibration			60			35	ppm of FSR/°C

SPECIFICATIONS

ELECTRICAL

At +25°C, V_{CC} = ±15V, V_{DD} = 5V, external sample/hold capacitor of 4700pF.

PARAMETERS	SDM862/863/872/873 J, A, R			SDM862/863/872/873 K, B, S			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	
SYSTEM TIMINGS							
ADC Conversion Time: SDM862/SDM863	9	20	25	*	*	*	µs
SDM872/SDM873	9	12	15	*	*	*	µs
S/H Aperture Delay		50			*		ns
S/H Aperture Uncertainty		2			*		ns
TIMING							
Throughput (Serial Mode)							
SDM862/SDM863			22			*	kHz
SDM872/SDM873			28			*	kHz
(Overlap Mode):							
SDM862/SDM863			33			*	kHz
SDM872/SDM873			50			*	kHz
MULTIPLEXER (6)							
Switching Time (between channels)		+1.5			*		µs
Settling Time (10V step to 0.02%)		2.5			*		µs
Enable Time 'ON'		1	2		*	*	µs
'OFF'		0.25	0.5		*	*	µs
INSTRUMENTATION AMPLIFIER (6)							
Settling Time (20V step to 0.01%)							
G = 1		5	12.5		*	*	µs
G = 10		3	7.5		*	*	µs
G = 100		4	7.5		*	*	µS
Slew Rate	12	17		*	*		V/µs
S/H AMPLIFIER (6)							
Acquisition (10V step to 0.01%)		5			*		µS
Aperture Delay		50			*		nS
Hold Mode Settling Time		1.5			*		µS
Slew Rate		10			*		V/µS
OUTPUT							
DIGITAL DATA							
Output Codes: Unipolar			Unipolar Straight Binary (USB)				
Bipolar			Bipolar Offset Binary (BOB)				
Logic Levels: Logic 0 (Sink = 1.6mA)			+0.4			*	V
Logic 1 (Source = 500µA)	+2.4			*			V
Leakage (Data Bits Only), High-Z State	–5	0.1	+5	*	*	*	µA
POWER SUPPLY REQUIREMENTS							
Rated Voltage: Analog (±V_{CC})	14.25	15	15.75	*	*	*	VDC
Digital (V_{DD})	4.5	5	5.5	*	*	*	VDC
Supply Drain: +15V		13	22		*	*	mA
–15V		22	30		*	*	mA
+5V		11	15		*	*	mA
Power Dissipation		580	855		*	*	mW
TEMPERATURE RANGE							
Operating Temperature Range							
JH, KH/JL, KL	0		70	*		*	°C
AH, BH/AL, BL	–25		+85	*		*	°C
RH, SH/RL, SL	–55		+125	*		*	°C
Storage Temperature Range	–65		+150	*		*	°C

* Specification same as SDM862/863/872/873J, A, R grades.

NOTES: (1) Measured at the same and hold output. (2) Measured with all input channels grounded. (3) The range of voltage on any input with respect to common over which accuracy and leakage current is guaranteed. (4) Applicable over full operating temperature range. NO MISSING CODES GUARANTEED OVER TEMPERATURE RANGE. (5) Adjustable to zero using external potentiometer or select-on-test resistor. (6) Specifications are at +25°C and measured at 50% level of transition.

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

DIGITAL TIMING

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
CONVERT MODE					
tdsc	Status Delay from CE		100	200	ns
thec	CE Pulse Width	50	30		ns
tssc	$\overline{CS}$ to CE Setup	50	20		ns
thsc	$\overline{CS}$ Low During CE High	50	20		ns
tsrc	R/$\overline{C}$ to CE Setup	50	0		ns
thrc	R/$\overline{C}$ Low During CE High	50	20		ns
tsac	Byte Select to CE Setup	0	0		ns
thac	Byte Selected Valid During CE High	50	20		ns
tc 86X	Conversion Time: 12 Bit Cycle	9	20	25	µs
	8 Bit Cycle	6	13	17	µs
tc 87X	Conversion Time: 12 Bit Cycle	9	12	15	µs
	8 Bit Cycle	6	8	10	µs
READ MODE					
tdd	Access Time from CE		75	150	ns
thd	Data Valid after CE Low	25	35		ns
thl	Output Float Delay		100	150	ns
tssr	$\overline{CS}$ to CE Setup	50	0		ns
tsrr	R/$\overline{C}$ to CE Setup	0	0		ns
tsar	Byte Select to CE Setup	50	25		ns
thsr	$\overline{CS}$ Valid after CE Low	0	0		ns
thrr	R/$\overline{C}$ High after CE Low	0	0		ns
thar	Byte Select Valid after CE Low	50	25		ns
ths 86X	Status Delay after Data Valid	100	500	1000	ns
ths 87X	Status Delay after Data Valid	100	300	600	ns

ABSOLUTE MAXIMUM RATINGS[1]

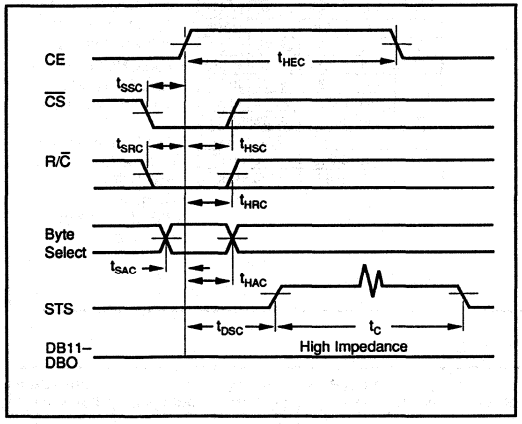
$+V_{CC}$ to ACOM	−0.5V to +16V
$-V_{CC}$ to ACOM	+0.5 to −16V
$+V_{DD}$ to DCOM	−0.5V to +7.0V
Analog Input Signal Range	$+V_{CC}$ +20V to $-V_{CC}$ −20V
Digital Input Signal	−0.5V to $+V_{DD}$
ACOM to DCOM	±1V

NOTE: (1) Absolute maximum ratings are limiting values applied individually, beyond which the serviceability of the circuit may be impaired. Functions operation under any of these conditions is not necessarily implied.

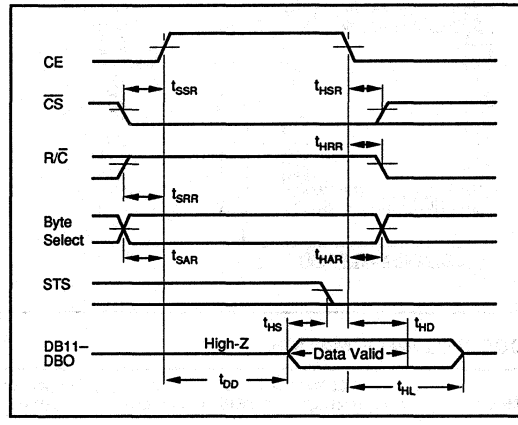
/QM HIGH RELIABILITY SCREENING

High Power Internal	
Visual Inspection	Burr-Brown Spec. QC2010
Stabilization Bake	24Hr at +150°C
Temperature Cycling	10 Cycles −65°C to +150°C
Constant Acceleration	30kG, Y1 axis
Hermeticity Fine Leak	Helium 5 x 10^{-8}cc/s
Hermeticity Gross Leak	Fluorocarbon
Burn-In	160Hr at +125°C

CONVERSION CYCLE TIMING

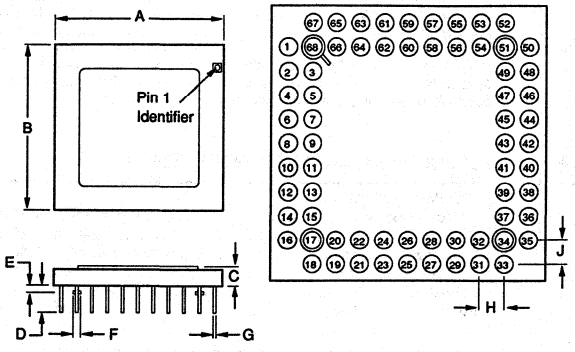


READ CYCLE TIMING



MECHANICAL (P.G.A.)

H Package

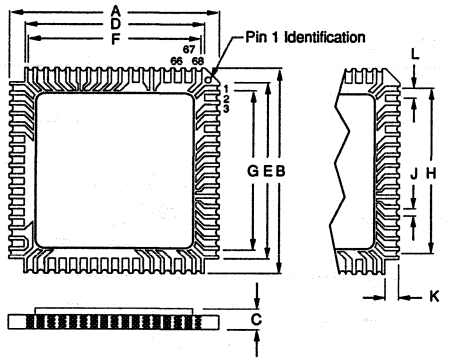


DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.087	1.109	27.610	28.169
B	1.087	1.109	27.610	28.169
C	.095	.120	2.413	3.048
D	.162	.198	4.115	5.029
E	.045	.055	1.143	1.397
F	.045	.055	1.143	1.397
G	.016	.020	.406	.508
H	.100 BASIC		2.540 BASIC	
J	.100 BASIC		2.540 BASIC	

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.
TERMINATION: Gold plated KOVAR.
CASE: Ceramic with gold plated nickel lid.
HERMETICITY: Gross leak test.
WEIGHT: 9 grms (0.32 oz)

MECHANICAL (L.C.C.)

TOP VIEW



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.945	.965	24.003	24.511
B	.945	.965	24.003	24.511
C	.076	.094	1.934	2.388
D	.841	.859	21.361	21.819
E	.841	.859	21.361	21.819
F	.755	.785	19.177	19.939
G	.755	.785	19.177	19.939
H	.800 BASIC		20.320 BASIC	
J	.027	.033	.686	.838
K	.045 BASIC		1.143 BASIC	
L	.050 BASIC		1.270 BASIC	

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only.
TERMINATION: Gold plated nickel on refractory metallization.
CASE: Ceramic with gold plated nickel lid.
HERMETICITY: Gross leak test.
WEIGHT: 4.37 grms (0.124 oz)

ODERING INFORMATION [1]

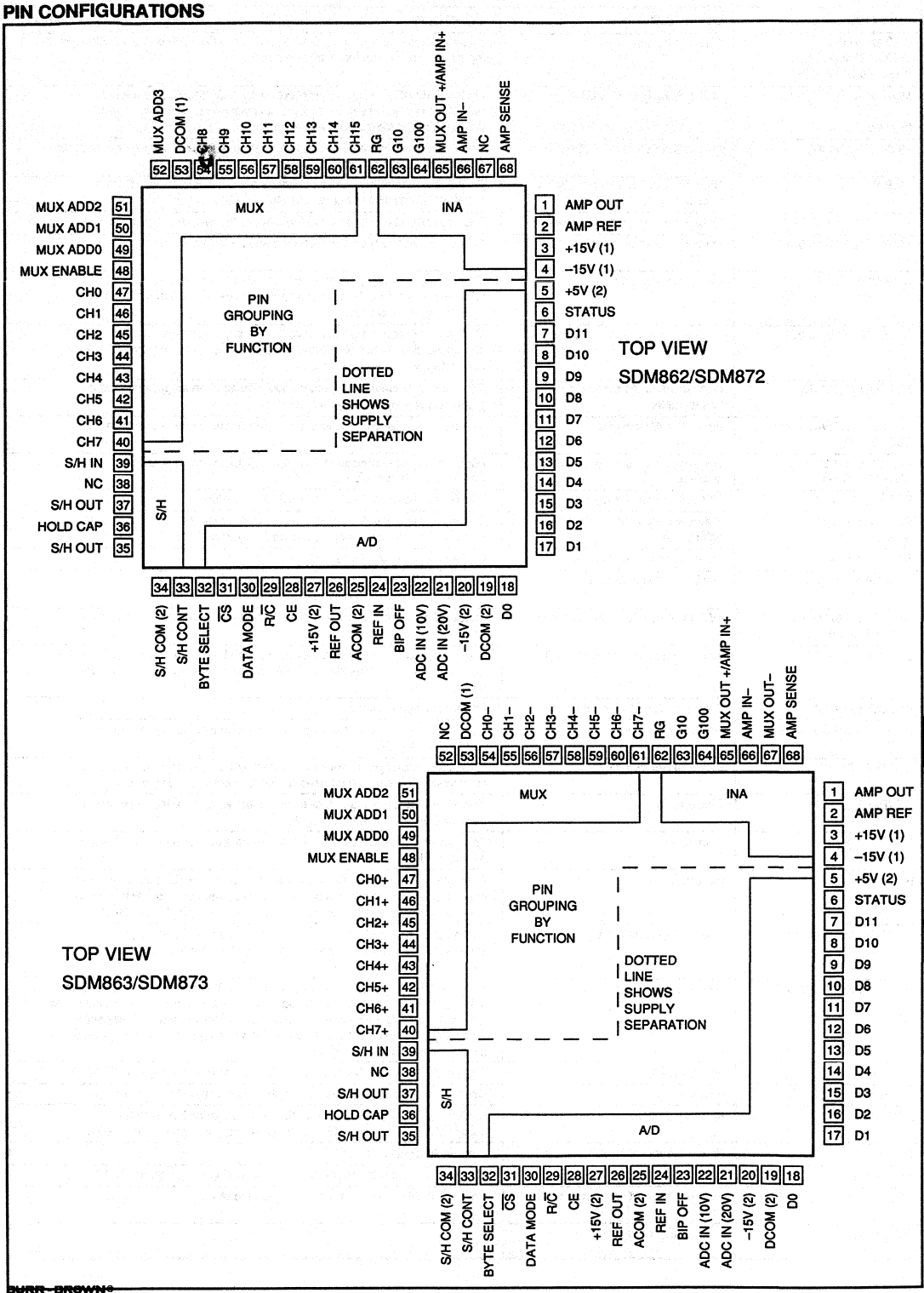
Model	Input	LCC, PGA Package	Accuracy (% FSR)	Throughput	Temperature Range (°C)	Model	Input	LCC, PGA Package	Accuracy (% FSR)	Throughput	Temperature Range (°C)
SDM862J	16SE	L,H	±0.024	33kHz	0 to +70	SDM863J	8DIF	L, H	±0.024	33kHz	0 to +70
SDM862K	16SE	L,H	±0.012	33kHz	0 to +70	SDM863K	8DIF	L, H	±0.012	33kHz	0 to +70
SDM862A	16SE	L,H	±0.024	33kHz	–25 to +85	SDM863A	8DIF	L, H	±0.024	33kHz	–25 to +85
SDM862B	16SE	L,H	±0.012	33kHz	–25 to +85	SDM863B	8DIF	L, H	±0.012	33kHz	–25 to +85
SDM862R	16SE	L,H	±0.024	33kHz	–55 to +125	SDM863R	8DIF	L, H	±0.024	33kHz	–55 to +125
SDM862S	16SE	L,H	±0.012	33kHz	–55 to +125	SDM863S	8DIF	L, H	±0.012	33kHz	–55 to +125
SDM872J	16SE	L,H	±0.024	50kHz	0 to +70	SDM873J	8DIF	L,H	±0.024	50kHz	0 to +70
SDM872K	16SE	L,H	±0.012	50kHz	0 to +70	SDM873K	8DIF	L,H	±0.012	50kHz	0 to +70
SDM872A	16SE	L,H	±0.024	50kHz	–25 to +85	SDM873A	8DIF	L,H	±0.024	50kHz	–25 to +85
SDM872B	16SE	L,H	±0.012	50kHz	–25 to +85	SDM873B	8DIF	L,H	±0.012	50kHz	–25 to +85
SDM872R	16SE	L,H	±0.024	50kHz	–55 to +125	SDM873R	8DIF	L,H	±0.024	50kHz	–55 to +125
SDM872S	16SE	L,H	±0.012	50kHz	–55 to +125	SDM873S	8DIF	L,H	±0.012	50kHz	–55 to +125

NOTE: 16 single-ended inputs, LCC package, with accuracy of 0.24% FSR. Temp Range of 0°C to +70°C and throughput of 33kHz = SDM862JL.

MODEL	DESCRIPTION
PC862/863-1	LCC (Socketed) Evaluation PCB*
PC862/863-2	PGA Evaluation PCB

* Switches socket is MC0068.

PIN CONFIGURATIONS



PIN DESIGNATION	DEFINITION	COMMENTS SDM8X2 = SDM862 OR SDM872
CH0 to CH15 CH0 to CH7 (+, –) (PINS 40 to 47, 54 to 61)	Channel Inputs	Analog Inputs (Total 16) for single-ended and differential operation. Unused inputs must be connected to analog common.
MUX OUT+/AMP IN+ (PIN 65)	MULTIPLEXER "HI" OUTPUT	On the SDM8X2 this is the multiplexer output. On the SDM8X3 it is the output of the positive selected inputs. It is connected internally to the positive input of the instrumentation amplifier.
MUXOUT (Pin 67)	MULTIPLEXER "LO" OUTPUT	This pin is used on the SDM8X3 only. It should be connected to the negative input of the instrumentation amplifier.
AMP IN (Pin 66)	Negative input of instrumentation amplifier	On the SDM8X2 this should be connected to analog common. On the SDM8X3 it should be connected to Muxout—(Pin 67).
AMP OUT (Pin 1)	Output of instrumentation amplifier	This pin should be connected to the input of the S/H amplifier (Pin 39).
AMP SENSE (Pin 68)	Output sense line of instrumentation amplifier	This pin will normally be connected direct to AMP OUT (Pin 1).
AMP REF (Pin 2)	Reference for amplifier output	This pin will normally be connected to analog common. Care should be taken to minimize tracking and contact resistance to analog common to optimize system accuracy.
S/H OUT (Pins 35/37)	Output of sample/hold amplifier	Two pins are provided to facilitate a guard ring around the hold capacitor pin. These pins should be connected to either ADC in (20V) or ADC in (10V) depending on the desired range.
HOLD CAP (Pin 36)	Connection for hold capacitor on S/H amplifier	The tracking to the hold capacitor should be as short as possible and a guard ring employed using Pins 35 and 37.
ADC IN (20V); ADC IN (10V) (Pins 21, 22)	Inputs to A/D converter	Connect to S/H amplifier output. Use appropriate pin for desired range.
RG, G10, G100 (Pins 62, 63, 64)	Gain settling pins on instrumentation amplifer	For Gain = 1, no connections. For Gain = 10, connect G10 to RG. For Gain = 100, connect G100 to RG.
REF OUT (PIN 26)	10V Reference voltage	This is the reference voltage for the A/D converter.
REF IN, BIP OFF (Pins 24, 23)	Reference input and offset input to A/D converter	Connect trim potentiometers (or select-on-test resistors) to these pins for unipolar or bipolar operation as shown in Figures 12, 13.
S/H IN (Pin 39)	Input to sample/hold amplifier	Connect to amp out (Pin 1).
MUX ENABLE (Pin 48)	Multiplex enable/disable	Logic '1' on this pin will enable a selected channel on the internal multiplexer. Logic '0' de-selects all channels.
MUX ADD0 to MUX ADD3 (Pins 49 to 52)	Address inputs for channel selection	These address lines select a particular channel as specified in Figure 24.
S/H CONT (Pin 33)	Track/Hold control on S/H amplifer	Logic '1' holds an analog value for conversion by the A/D converter. This line may be controlled by the status (Pin 6) of the converter to simplify external timing control.
S/H COM (Pin 34)	Reference for S/H logic control	Connect to digital common.
D0 to D11 (Pins 7 to 18)	3-state digital outputs	The 12- or 8-bit result of a conversion is available as output on these pins (D0-LSB, D11-MSB).
STATUS (Pin 6)	Status of A/D conversion	This output is at logic '1' while the internal A/D converter is carrying out a conversion. This pin may be used to directly control the S/H amplifier.
CE (Pin 28)	Chip enable	This input must be at logic '1' to either initiate a conversion or read output data (see Figures 10, 17, 18, 19, 20).
$\overline{CS}$ (Pin 31)	Chip select	This input must be at logic '0' to either initiate a conversion or read output data (see Figures 10, 17, 18, 19, 20).
R/$\overline{C}$ (Pin 29)	Read/convert	Data can be read when this pin is logic '1' or a conversion can be initiated when this pin is logic '0'. This pin is typically connected to the R/$\overline{W}$ control line of a microprocessor-based system (see Figures 10, 17, 18, 19, 20).
DATA MODE (Pin 30)	Select 12 or 8 Bit Data	When data mode is at logic '1' all 12 output data bits are enabled simultaneously. When data mode is at logic '0' MSBs and LSBs are controlled by byte select (Pin 32).
BYTE SELECT (Pin 32)	Byte address, short cycle	When reading output data, byte select at logic '0' enables the 8 MSBs. Byte select at logic '1' enables the 4 LSBs. The 4 LSBs can therefore be connected to four of the MSB lines for inter-connection to an 8-bit bus. In start convert mode, logic '0' enables a 12-bit conversion while logic '1' will short cycle the conversion to 8 bits (see Figure 10).
+15V(1), +15V(2)(Pins 3, 27)	Power Supply	Connect to +15V supply using decoupling as indicated in Figures 15, 16.
–15V(1), –15V(2)(Pins 4, 20)	Power Supply	Connect to –15V supply using decoupling as indicated in Figures 15, 16.
ACOM(2) (Pin 25)	Analog Common	Analog common connection. Note that a common (including digital common) should be connected together at one point close to the device.
DCOM (1) (Pin 53)	Reference for MUX logic control.	Connect to digital common.
+5V (Pin 5)	Logic power supply	Connect to +5V digital supply line with decoupling as in Figures 15, 16.
DCOM(2) (Pin 19)	Reference for A/D converter control lines	Connect to S/H common at one point close to device.
NC (Pin38)	No internal connection	

SYSTEM DESCRIPTION

The SDM comprises four circuit elements—an input-protected multiplexer, an instrumentation amplifier, a sample/hold amplifier, and an analog-to-digital converter.

INSTALLATION

MULTIPLEXER

The SDM family has a choice of input multiplexers (MUX).

SDM862 and SDM872: 16 single-ended inputs
SDM863 and SDM873: 8 differential inputs

The select inputs are designed for use with TTL and CMOS logic levels and do not require pull-up resistors to ensure break-before-make operation.

On all models, the analog inputs may be expanded using the enable control. See Figure 1. When the enable is at a logic "0," the internal MUX is disabled, allowing additional multiplexers to be connected in parallel. The limiting factor for the number of additional multiplexers is the cumulative effect of leakage current flowing in the signal source impedance, causing offset errors.

Differential inputs will generally eliminate the noise associated with common system grounds, but care must be taken to ensure that neither of the differential inputs exceed the maximum input range. Otherwise, signal distortion will result. A return path for the input bias currents must always be provided. This prevents the charging of stray capacitances in applications using floating sources, such as transformers and thermocouples. Multiplexer inputs are protected from overvoltage, as indicated in the electrical specifications, and should be current limited to 20mA. To avoid signal distortion on the selected channel, MUX inputs that are not selected should have their input voltages limited to between—V_{CC} and $+V_{CC}$–4V, as voltages outside of these values can turn on the non-selected channel. A graph of this characteristic is shown in Figure 2 with a possible circuit solution where it is known that the input voltages will exceed the above values.

Where high-speed operation is required and channels require rapid sampling, then it is important to buffer the inputs

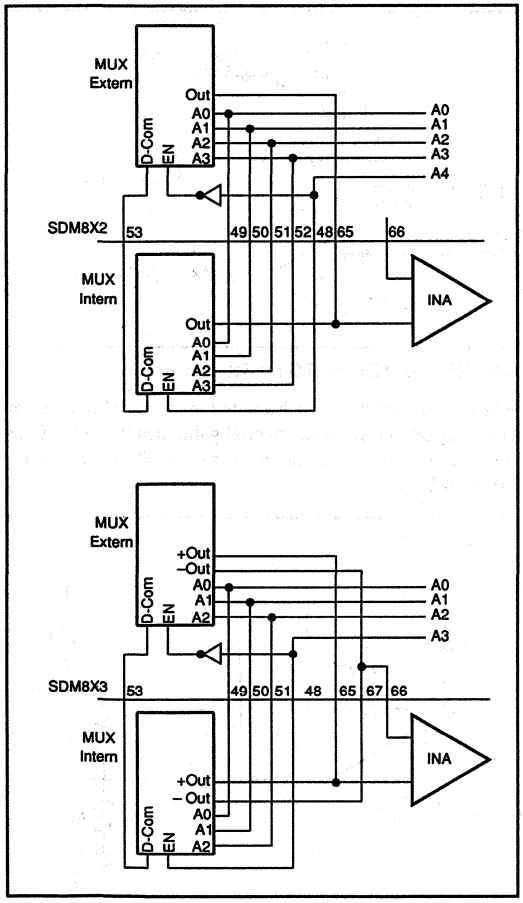


FIGURE 1. External Multiplexer Connections for Differential and Single-Ended Operation.

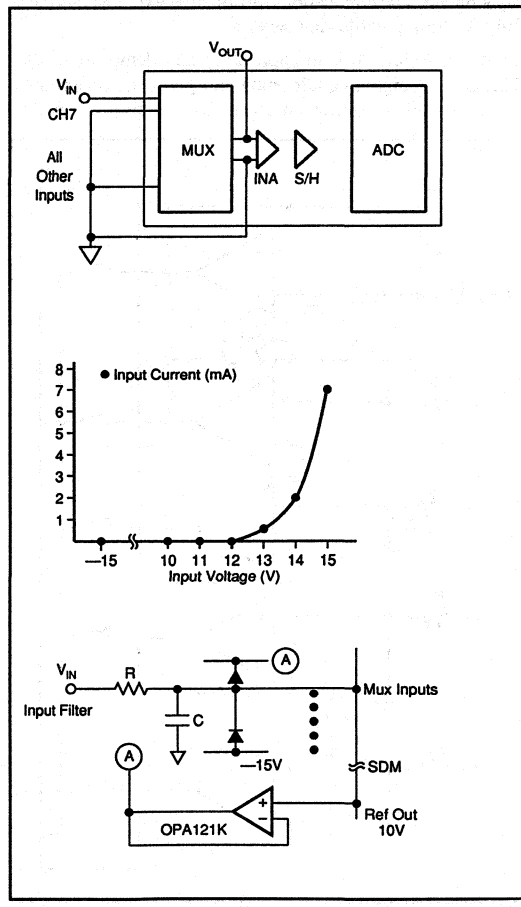


FIGURE 2. MUX Inputs With Limited Input Voltages and Possible Circuit Solution for Non-limited Cases.

against the effect of current sharing between the MUX output capacitance and the input filter capacitance. See Figure 3.

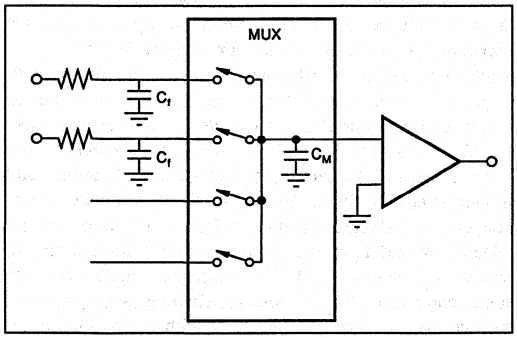


FIGURE 3. Filter and MUX Capacitance.

All data acquisition systems using a MUX require consideration of the errors that may be introduced by MUX output capacitance. The applications information explains this more fully in the input filtering section.

Shown in Figure 4 is an application that demonstrates the flexibility of signal conditioning and gives the opportunity to use a higher bandwidth filter. Diodes shown are low leakage types (1na). The low output impedance of the amplifiers reduces the time taken to charge MUX capacitance C_M.

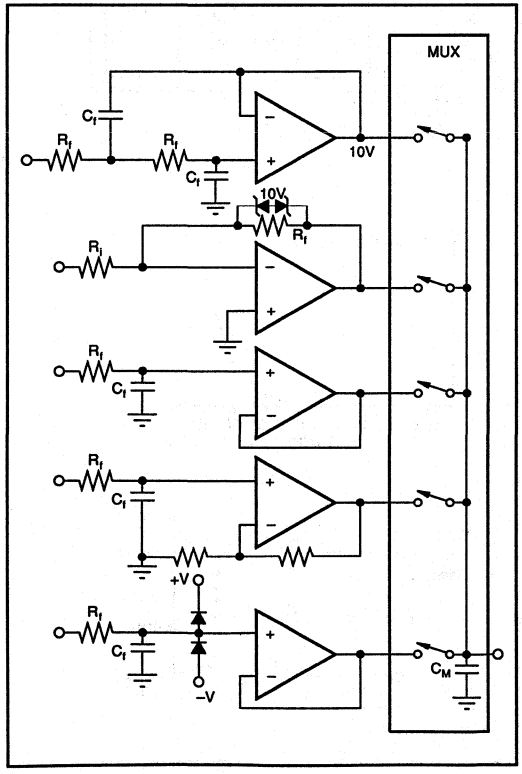


FIGURE 4. Example Application Illustrating Flexible Signal Conditioning.

INSTRUMENT AMPLIFIER

The instrument amplifier (INA) presents a very high input impedance to the signal source, eliminating gain errors introduced by voltage divider action between the source output impedance and SDM input impedance. Where the differential models are used, the INA performs the differential to single-ended conversion required to drive the sample/hold amplifier. Gains may be set by using external jumpers,to values of 1 (no jumper), 10 and 100. For gains other than these presets, the following formula may be used to find an external resistor value to add in series with the G = 10 or G = 100 jumpers.

$$R_{ext} = \frac{40k\Omega}{G-1} - Ri$$

Where Ri = 4444Ω, G = 10 input.
404Ω, G = 100 input.

It should be noted that the internal gain set resistors have a ±20% tolerance and ±20ppm/°C drift.

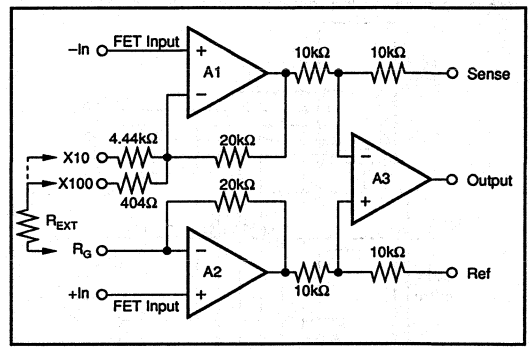


FIGURE 5. Use External Gain Set Resistor.

Where it is necessary to keep the input amplifiers from saturating or increasing the overall gain, then the gain of the output amplifier can be increased from unity by using the circuit in Figure 6.

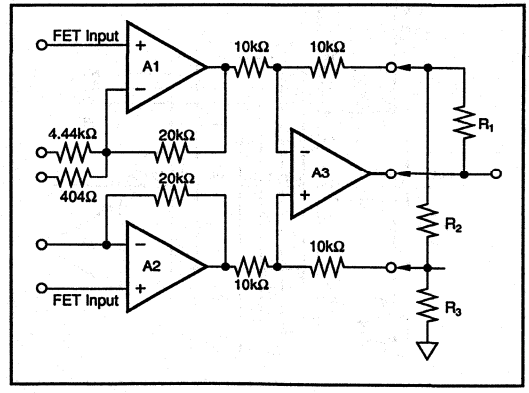


FIGURE 6. Increasing Output Amplifier Gain.

The values of the resistors in Figure 6 are in the following table.

O/P GAIN	R_1 & R_3 Ω	R_2 Ω
2	1200	2740
5	1000	511
10	1500	340

Matching of R_1 and R_3 is required to maintain high common-mode rejection (CMR), R_2 sets the gain and may be varied without effect on CMR.

To ensure that the effects of temperature are minimized when altering the gain with external components, it is very important to use low tempco resistors. When connecting the output sense, ensure that series resistance is minimized because resistance present will degrade CMR.

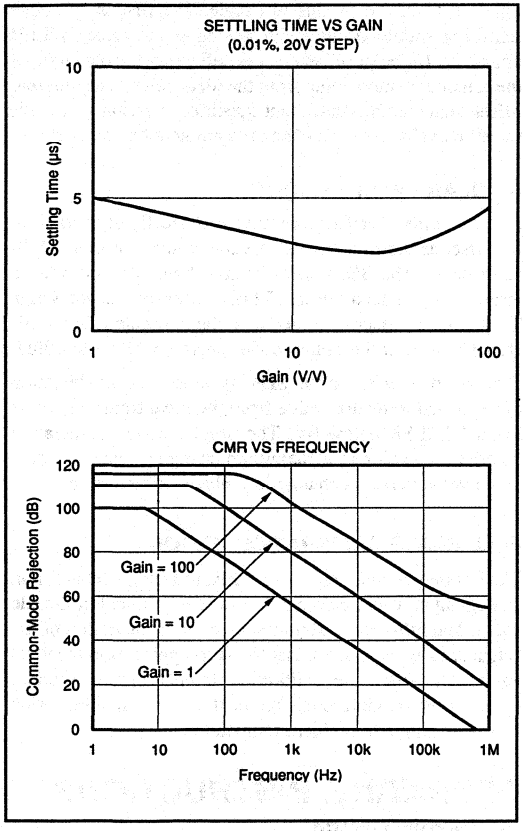


FIGURE 7. Typical INA Settling Time and CMR.

Some applications may require programmable gains. This may be realized with Figure 8.

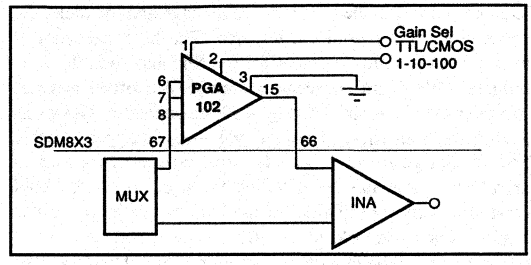


FIGURE 8. Setting Programmable Gains.

SAMPLE/HOLD AMPLIFIER

The Sample/Hold amplifier (S/H) is used to track the incoming signal and "hold" the required instantaneous value so that it does not change while the ADC is carrying out its conversion. Timing for the S/H may be derived from the STATUS output of the ADC, with care being taken to comply with the SDM timing considerations.

Capacitors with high insulation resistance and low dielectric absorption such as Teflon™, polystyrene or polypropylene should be used as storage elements. (Polystyrene should not be used above +80°C.) Teflon™ is recommended for high temperature operation. Care should be taken in the printed circuit layout to minimize stray capacitance and leakage currents from the capacitor to minimize charge offset and droop errors. The use of a guard ring driven by the S/H output around the pin connecting to the hold capacitor is recommended. (Refer to the application board layout for an example of this.)

The value of the external hold capacitor determines the droop rate, charge offset and acquisition time of the S/H, Figure 9. Droop rate for the SDM is specified with a hold capacitor value of 4700pf. There is a trade-off between acquisition time and droop rate, as the hold capacitor is increased in value it takes longer to charge, and hence there

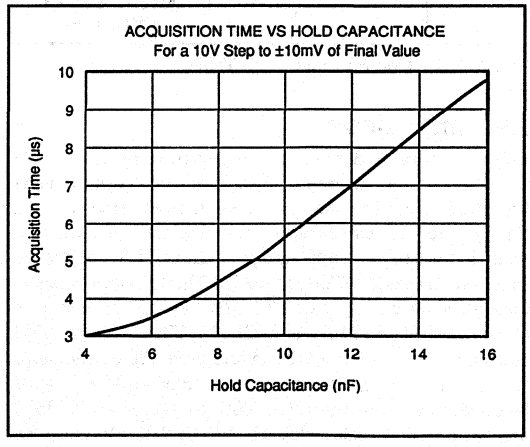


FIGURE 9. Acquisition Time vs Hold Capacitance for a 10V Step Settling to ±10mV of Final Value.

is a corresponding increase in acquisition time and reduction in droop rate. The droop rate is determined by the amount of leakage present in the SDM, board leakage and the dielectric absorption of the hold capacitance. The hold capacitor is also a compensation element for the S/H and should not be reduced below 2nf for good stability. The offset error in sample mode is not affected by the hold capacitor. However, during the transition to hold mode there is approximately 5pC of charge injected into the hold capacitor, causing an offset error that has been nulled for use with a 5nf hold capacitor. Any other value for the hold capacitor will cause a minor but fixed hold mode offset to be introduced, and is proportional to the change in value from 5nf. Therefore, the SDM should be offset nulled with the S/H in hold mode.

ANALOG-TO-DIGITAL CONVERTER

This circuit element converts the analog voltage presented by the sample/hold amplifier to a digital number in binary format under control of the digital signals detailed in Figure 10. The converter can convert unipolar and bipolar signals in the range 10V and 20V. It can be calibrated to remove gain and offset errors from the entire system. The converter contains its own clock, voltage reference, and microprocessor interface with 3-state outputs. The converter will normally be used to digitize signals to 12-bit resolution, but it can be short-cycled to provide 8-bit resolution at higher speed. The digital output is compatible with 8- or 16-bit data buses, the data format being selected by control signals as detailed in Figure 10.

CE	$\overline{CS}$	R/$\overline{C}$	DATA MODE	BYTE SELECT	OPERATION
0	X	X	X	X	None
X	1	X	X	X	None
↑	0	0	X	0	Initiate 12-bit conversion
↑	0	0	X	1	Initiate 8-bit conversion
1	↓	0	X	0	Initiate 12-bit conversion
1	↓	0	X	1	Initiate 8-bit conversion
1	0	↓	X	0	Initiate 12-bit conversion
1	0	↓	X	1	Initiate 8-bit conversion
1	0	1	1	X	Enable 12-bit output
1	0	1	0	0	Enable 8 MSBs only
1	0	1	0	1	Enable 4 LSBs plus 4 trailing zeros

FIGURE 10. Control Input Truth Table.

LINEARITY ERROR

Linearity error is defined as the deviation of actual code transition values from the ideal transition values. Ideal transition values lie on a line drawn through zero (or minus full scale for bipolar operation) and plus full scale. The zero value is located at an analog input value 1/2LSB before the first code transition (000_H to 001_H). The full-scale value is located at an analog value 3/2LSB beyond the last code transition (FFE_H to FFF_H) (see Figure). Thus, with the SDM connected for bipolar operation and with a full-scale range (or span) of 20V (±10V), the zero value of –10V is 2.44mV below the first code transition (000_H to 001_H at –9.99756V) and the plus full-scale value of +10V is 7.32mV above the last code transition (FFE_H to FFF_H at +9.99268) (see Figure 14).

NO MISSING CODES (DIFFERENTIAL LINEARITY ERROR)

A specification which guarantees no missing codes requires that every code combination appear in a monotonically-increasing sequence as the analog input is increased throughout the range. Thus, every input code width (quantum) must have a finite width. If an input quantum has a value of zero (a differential linearity error of –1LSB), a missing code will occur.

The SDM is guaranteed to have no missing codes to 12-bit resolution over it's respective specification temperature ranges.

UNIPOLAR OFFSET ERROR

An SDM connected for unipolar operation has an analog input range of 0V to plus full scale. The first output code transition should occur at an analog input value 1/2LSB above 0V. Unipolar offset error is defined as the deviation of the actual transition value from the ideal value. The unipolar offset temperature coefficient specifies the change of this transition value versus a change in ambient temperature.

BIPOLAR OFFSET ERROR

A/D converter specifications have historically defined bipolar offset as the first transition value above the minus full-scale value. The SDM specification, however, follows the terminology defined for the 574 converter several years ago. Thus, bipolar offset is located near the midscale value of 0V (bipolar zero) at the output code transition 7FFH to 800H.

Bipolar offset error for the SDM is defined as the deviation of the actual transition value from the ideal transition value located 1/2LSB below 0V. The bipolar offset temperature coefficient specifies the maximum change of the code transition value versus a change in ambient temperature.

FULL SCALE CALIBRATION ERROR

The last output code transition (FFE_H to FFF_H) occurs for an analog input value 3/2LSB below the nominal full-scale value. The full-scale calibration error is the deviation of the actual analog value at the last transition point from the ideal value. The full-scale calibration temperature coefficient specifies the maximum change of the code transition value versus a change in ambient temperature.

OPERATING INSTRUCTIONS

OPERATING MODES

The SDM can operate in one of two modes, namely serial and overlap, as shown in Figure 11. In serial mode, control of the device is such that a multiplexer channel X is first selected, time is then allowed for the instrumentation amplifier to settle, the sample/hold amplifier is set to HOLD mode and finally a conversion is carried out. This procedure is then repeated for channel Y. Faster throughput can be obtained using overlap mode. While a conversion is being carried out by the ADC on a voltage from channel X held on

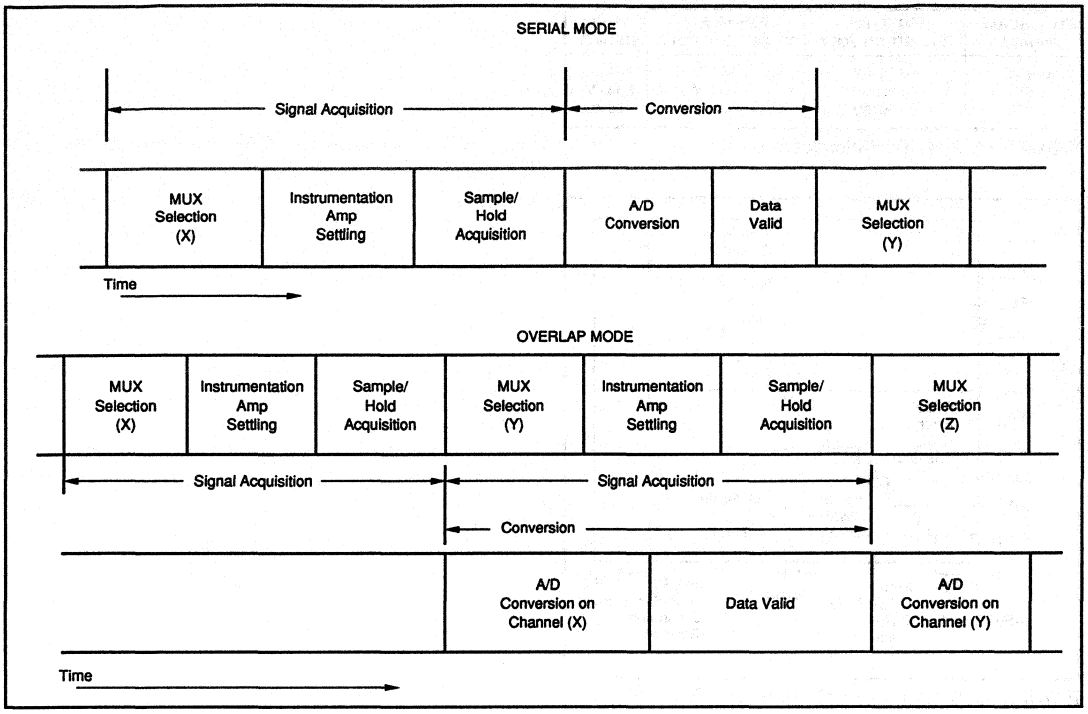


FIGURE 11. Serial and Overlap Modes of Operation.

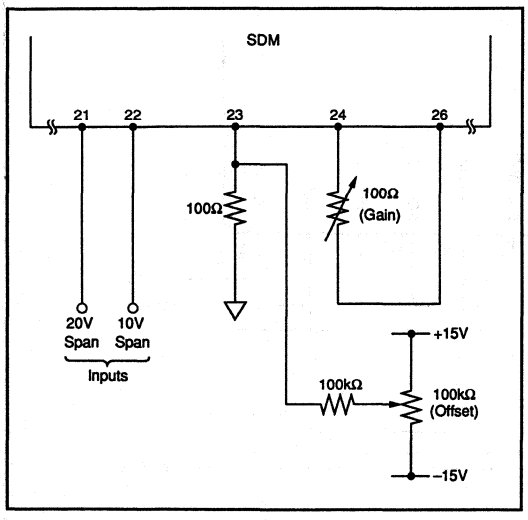


FIGURE 12. Unipolar Calibration.

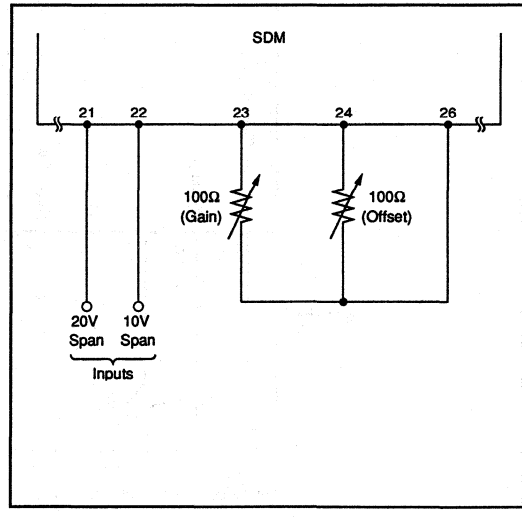


FIGURE 13. Bipolar Calibration.

FULL-SCALE RANGE	000 TO 001 TRANSITION VOLT.	FFE TO FFF TRANSITION VOLT.	1LSB EQUALS
0–10V	+0.0012V	+9.9963V	2.44mV
±5V	–4.9988V	+4.9963V	2.44mV
±10V	–9.9976V	+9.9927V	4.88mV

FIGURE 14. Code Transition Ranges.

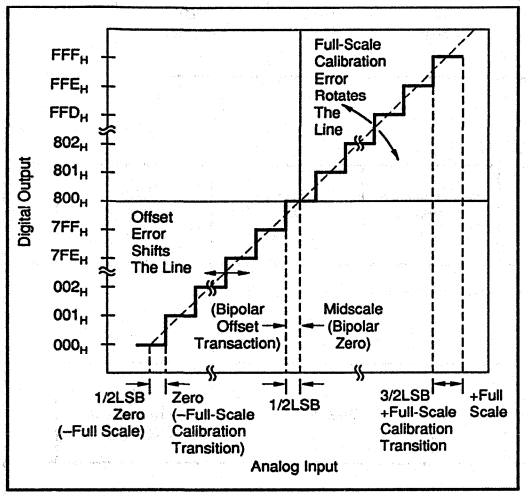


FIGURE 15. SDM Transfer Characteristic Terminology.

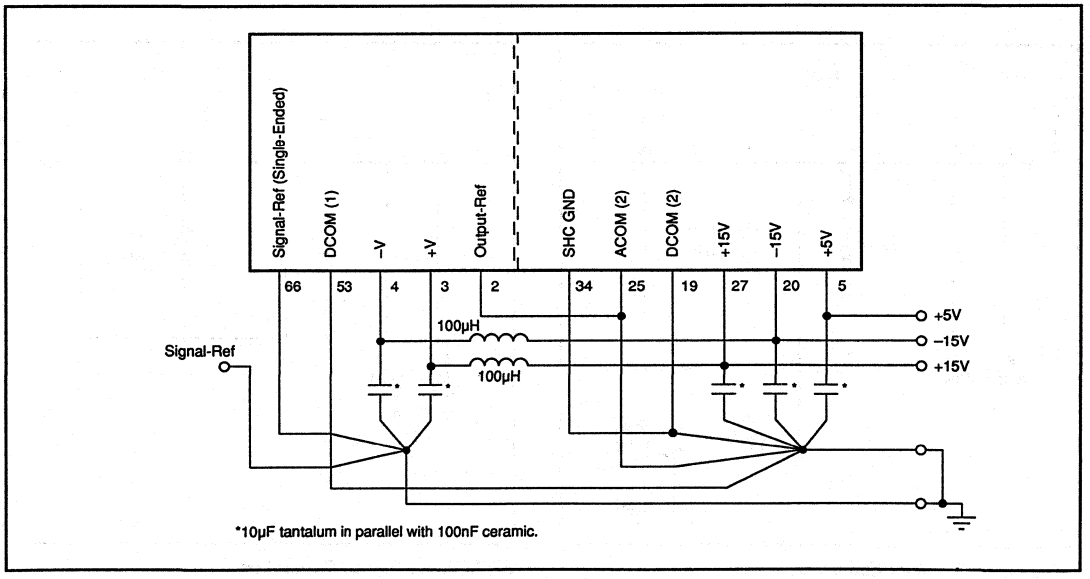


FIGURE 16. Recommended Decoupling of Power Supplies.

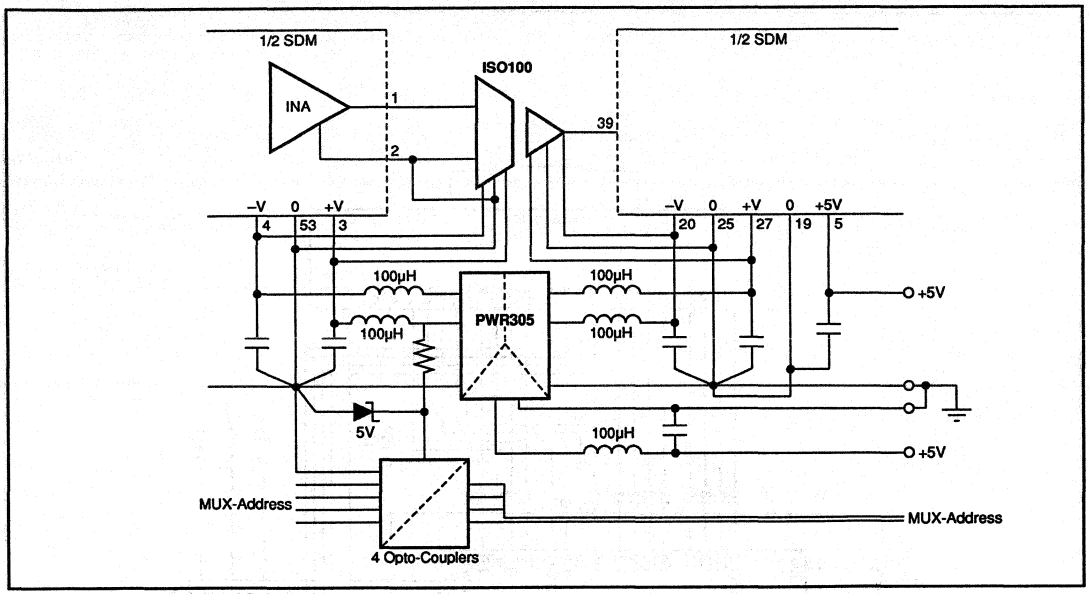


FIGURE 17. Galvanic Isolation Between Analog and Digital Signals.

the sample/hold, channel Y is selected and the multiplexer and instrumentation amplifier allowed to settle. In this way, the total throughput time is limited only by the sum of the sample/hold acquisition time and the ADC conversion time.

CALIBRATION – UNIPOLAR

If adjustment of unipolar offset and gain are not required, then the gain set potentiometer in Figure 12 (Unipolar operation) may be replaced with a 50Ω, 1% metal film resistor, and the offset network replaced with a connection from pin 23 to ground.

CALIBRATION - BIPOLAR

If adjustment of bipolar offset and gain are not required then the gain set and offset potentiometers in Figure 13 (Bipolar operation) may both be replaced with 50Ω, 1% metal film resistors.

CALIBRATION - GENERAL

The input voltage ranges of the ADC are 0-10V, ±5V and ±10V. Calibration in all ranges is achieved by adjusting the offset and gain potentiometers (indicated in Figures 12 and 13) such that the 000 to 001 code transition takes place at +1/2LSB from full-scale negative (–FS) and the FFE to FFF transition takes place at –3/2LSB from full-scale positive (+FS). The procedure is therefore to select the required range from Figure 14, apply the specified (–FS+1/2LSB) voltage to any selected input channel and adjust the offset potentiometer for the 000 to 001 transition. The (+FS–3/2LSB) voltage should then be applied to the same channel and the gain potentiometer adjusted for the FFE to FFF transition. The offset should always be made before the gain adjustment.

GROUNDING, DECOUPLING AND LAYOUT CONSIDERATIONS

It should be noted that the multiplexer/instrumentation amplifier section and sample/hold plus ADC section of the SDM have separate power connections. This is to enable more flexible grounding techniques to be implemented, Figures 16, 17. It also facilitates the use of independent decoupling of the analog front-end power supply, and the ADC plus associated digital circuitry power supply if desired. In this way, a separately decoupled analog front-end can be made to be substantially more immune to power supply noise generated by the ADC circuitry than if the power supplies to the two sections were directly connected. This feature is important where low-level signals are in use or high input signal noise immunity is desired.

The output section has three grounds:

Pin 25 Analog Common, A/D Converter
Pin 34 S/H Amp Digital Input Reference
Pin 19 Digital Common, A/D Converter

The input section has one ground:

Pin 53 Common for digital MUX-inputs and power supply decoupling.

All grounds have to be interconnected externally to the SDM, and it is recommended that all grounds are connected via one track to a single point as close as possible to the SDM. To check that the grounding structure is correct, the ground tracking should be sketched and a grounding "tree" should result whereby all grounds route to a central point.

In general, layout should be such that analog and digital tracks are separated as much as possible with coupling between analog and digital lines minimized by careful lay-

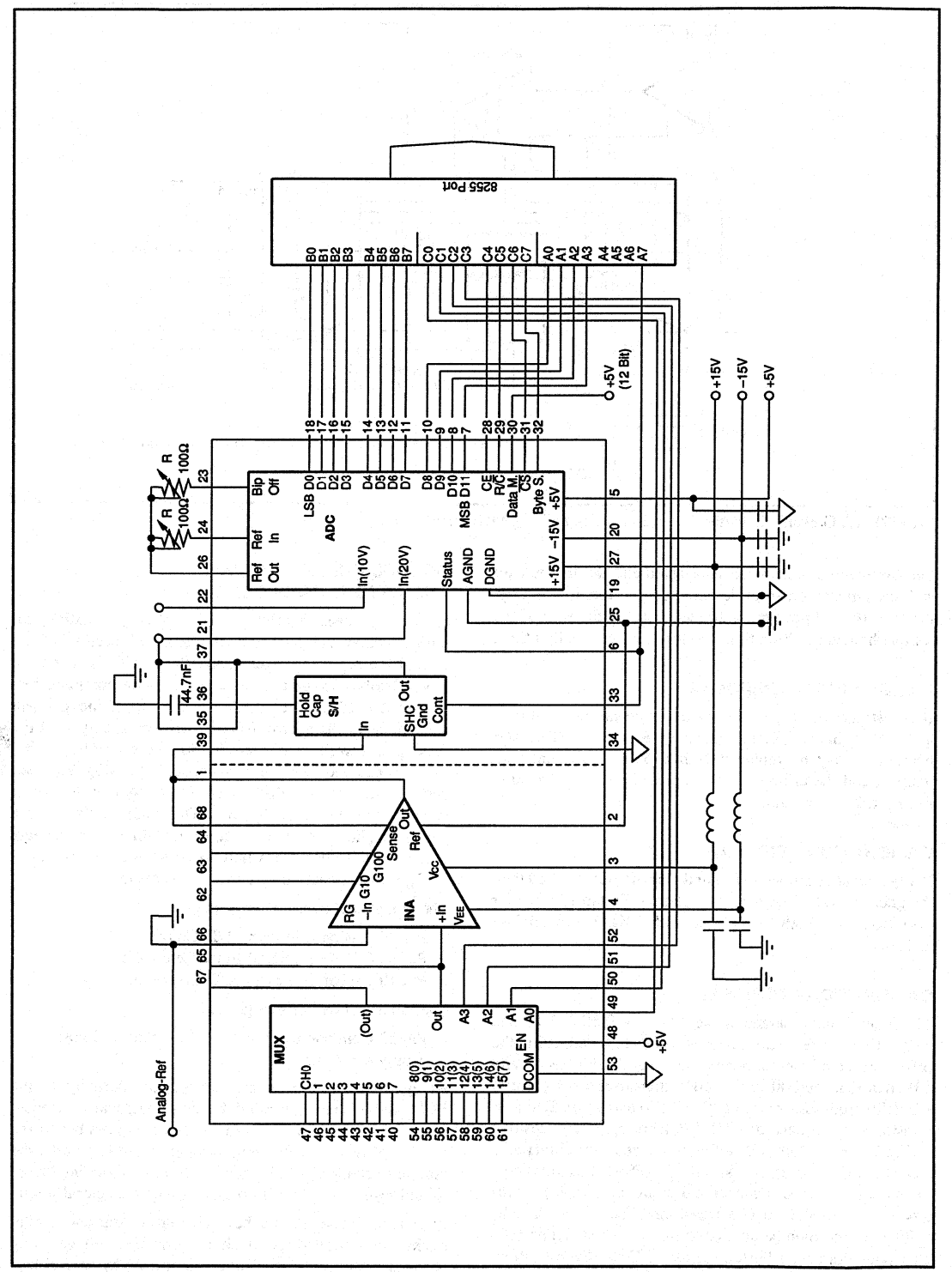


FIGURE 18. The SDM Connected to an Input/Output Port.

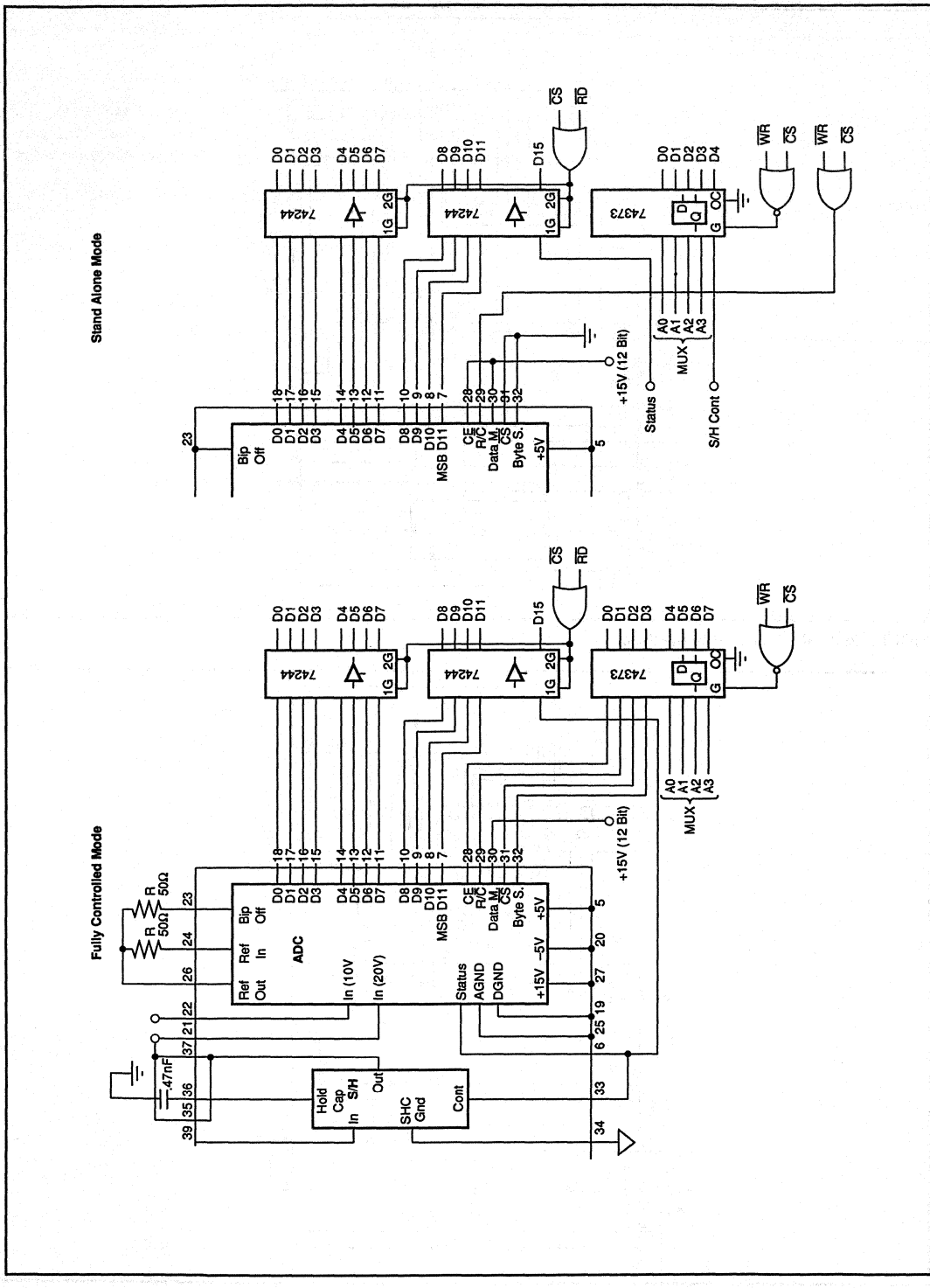


FIGURE 19. The SDM Connected to a 16-Bit-BUS.

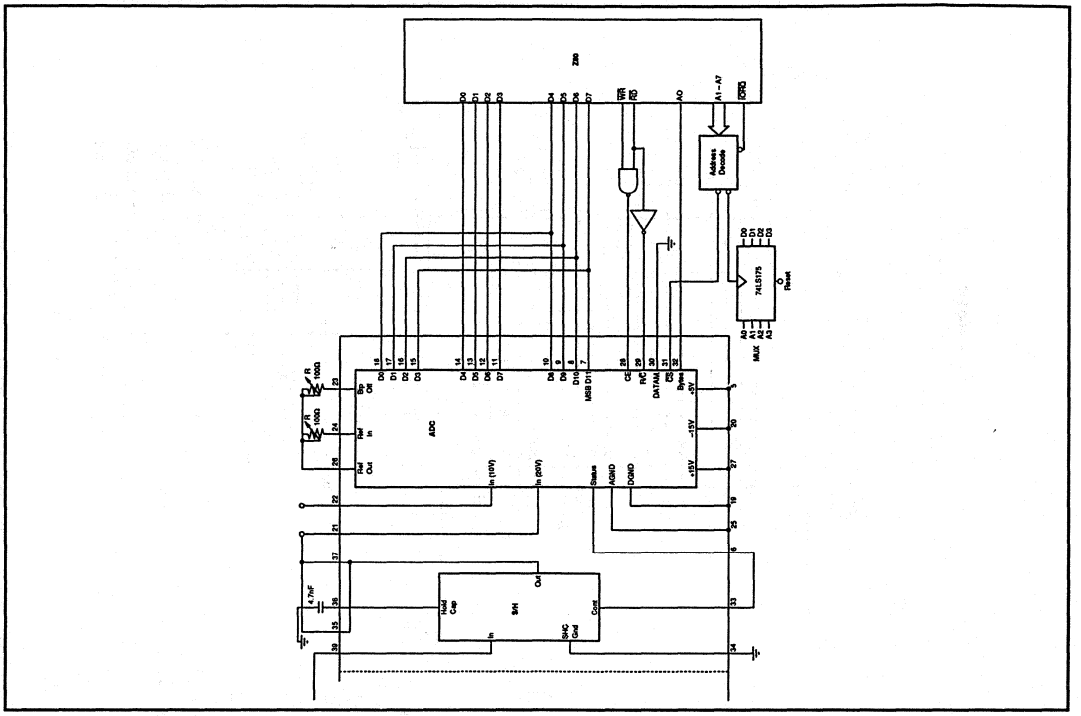


FIGURE 20A. SDM on the Z80 Interface.

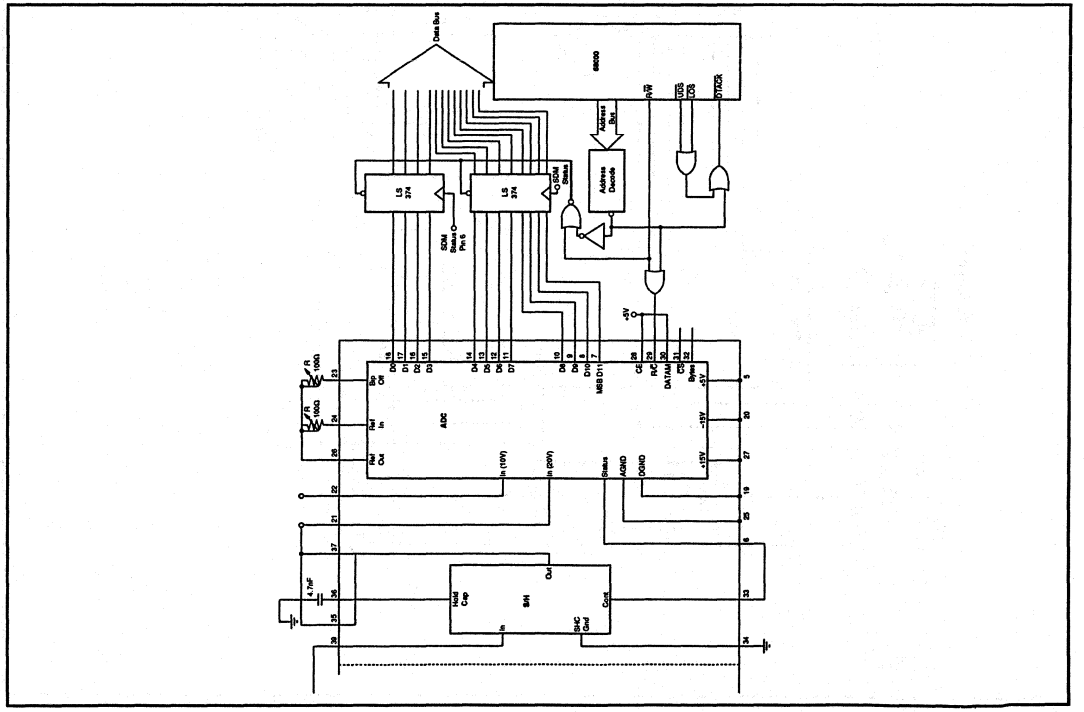


FIGURE 20B. 68000/SDM Interface.

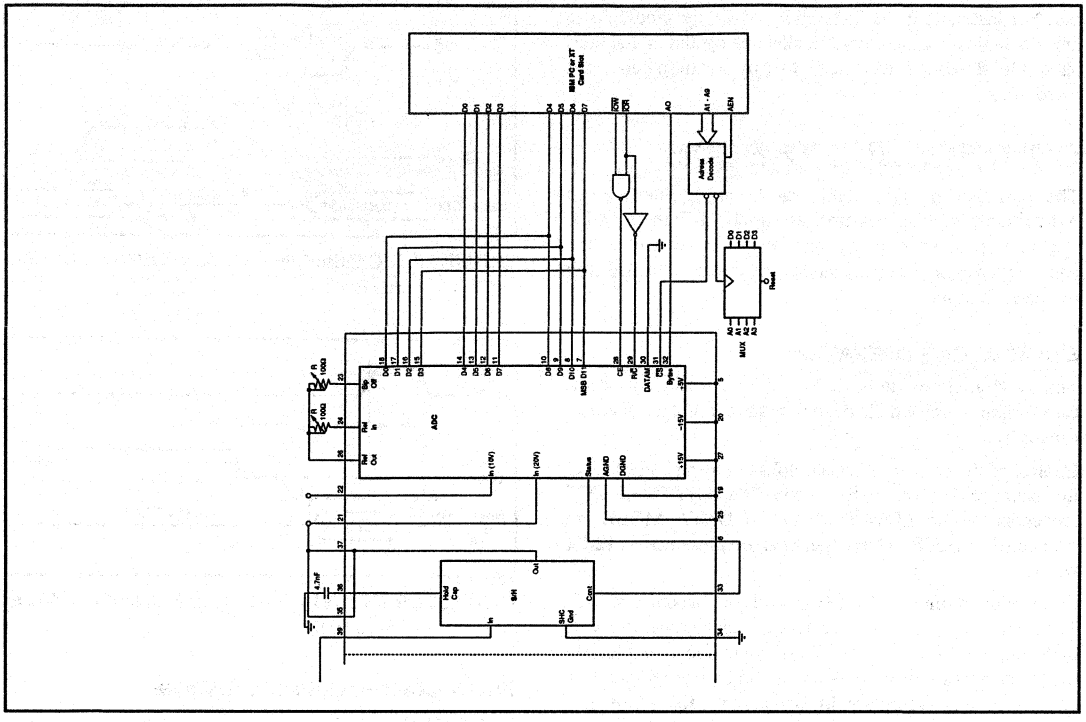


FIGURE 20C. IBM PC SDM Interface.

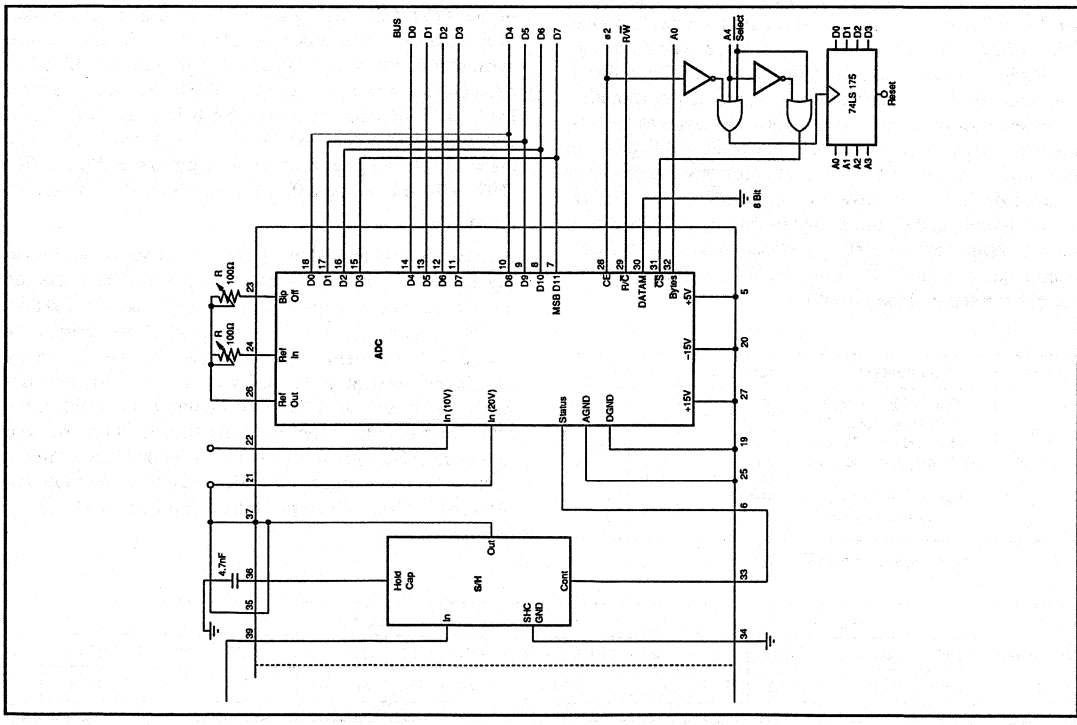


FIGURE 21. SDM on the 6502 BUS.

out. For instance, if the lines must cross they should do so at right angles to each other. Parallel analog and digital lines should be separated from each other by a pattern connected to common.

CONTROLLING THE SDM

The Burr-Brown SDM family can be easily interfaced to most microprocessor systems, as shown in Figures 18-21. The microprocessor may control each conversion, or the converter may operate in a stand-alone mode controlled only by the R/$\overline{C}$ input.

STAND-ALONE OPERATION

The stand-alone mode is used in systems containing dedicated input ports which do not require full bus interface capability.

Control of the converter is accomplished by a single control line connected to R/$\overline{C}$. In this mode $\overline{CS}$ and BYTE SELECT are connected to LOW and CE and DATA MODE are connected to HIGH. The output data are presented as 12-bit words.

Conversion is initiated by a High-to-Low transition of R/$\overline{C}$. The three-state data output buffers are enabled when R/$\overline{C}$ is high and STATUS is low. Thus, there are two possible modes of operation; conversion can be initiated with either positive or negative pulses. In each case the R/$\overline{C}$ pulse must remain low for a minimum of 50ns.

Figure 22 illustrates timing when conversion is initiated by an R/$\overline{C}$ pulse which goes low and returns to the high state during the conversion. In this case, the three-state outputs go to the high-impedance state in response to the falling edge of R/$\overline{C}$ and are enabled for external access of the data after completion of the conversion. Figure 23 illustrates the timing when conversion is initiated by a positive R/$\overline{C}$ pulse. In this mode the output data from the previous conversion is enabled during the positive portion of R/$\overline{C}$. A new conversion is started on the falling edge of R/$\overline{C}$, and the three-state outputs return to the high impedance state until the next occurrence of a high R/$\overline{C}$ pulse. Table I lists timing specifications for stand-alone operation.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
t_{HRL}	Low R/$\overline{C}$ Pulse Width	50			ns
t_{DS}	STS Delay from R/$\overline{C}$			200	ns
t_{HDR}	Data Valid After R/$\overline{C}$ Low	25			ns
t_{HS} 86X	STS Delay After Data Valid	300	500	1000	ns
t_{HS} 87X		100	300	600	ns
t_{HRH}	High R/$\overline{C}$ Pulse Width	150			ns
t_{DDR}	Data Access Time			150	ns

TABLE I. Stand-Alone Mode Timing.

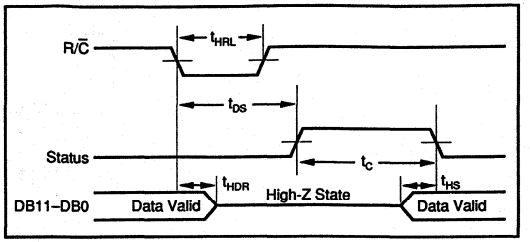


FIGURE 22. R/C Pulse Low—Outputs Enabled After Conversion.

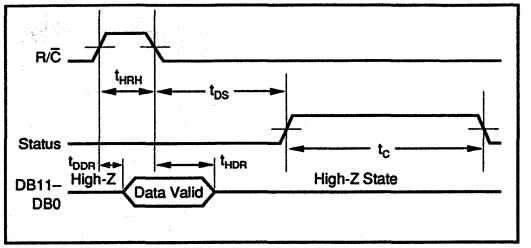


FIGURE 23. R/$\overline{C}$ Pulse High—Outputs Enabled Only Where R/$\overline{C}$ is High.

FULLY CONTROLLED OPERATION

Conversion Length

Conversion length (8-bit or 12-bit) is determined by the state of the BYTE SELECT input, which is latched upon receipt of a conversion start transition. BYTE SELECT is latched because it is also involved in enabling the output buffers. No other control inputs are latched. If BYTE SELECT is latched high, the conversion continues for 8 bits. The full 12-bit conversion will occur if BYTE SELECT is low. If all 12 bits are read following an 8-bit conversion, the 3LSBs (DB0-DB2) will be low (logic 0) and DB3 will be high (logic 1).

Conversion Start

A conversion is initiated by a transition on any of three logic inputs (CE, CS, and R/C)—refer to Figure 10. The last of the three to reach the required state start the conversion and thus all three may be dynamically controlled. If necessary, they may change state simultaneously, and the nominal delay time is independent of which input actually starts the conversion. If it is desired that a particular input establish the actual start of conversion, the other two should be stable a minimum of 50ns prior to the transition of that input. Timing relationships for start of conversion timing are illustrated in Conversion Cycle Timing of the Digital Specifications.

	Word 1								Word 2							
Processor	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
SDM	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	0	0	0	0

FIGURE 24. 12-Bit Data Format for 8-Bit Systems (connected as Figures 19 and 20).

The STATUS output indicates the state of the converter by being high only during a conversion. During this time the three-state output buffers remain in a high-impedance state, and therefore, data is not valid. During this period additional transitions of the three control inputs will be ignored, so that conversion cannot be prematurely terminated or restarted. However, if BYTE SELECT changes state after the beginning of conversion, any additional start conversion transition will latch the new state of BYTE SELECT, possibly resulting in an incorrect conversion length (8 bit versus 12 bits) for that conversion.

READING OUTPUT DATA

After conversion is initiated, the output data buffers remain in a high-impedance state until the following four conditions are met: R/$\overline{C}$ high, STATUS low, CE high, and $\overline{CS}$ low. In this condition the data lines are enabled according to the state of the inputs DATA MODE and BYTE SELECT. See Read Cycle Timing for timing relationships and specification.

In most applications the DATA MODE input will be hardwired in either the high or low condition, although it is fully TTL- and CMOS-compatible and may be actively driven if desired. When DATA MODE is high, all 12 outputs lines (DB0-DB11) are enabled simultaneously for full data word transfer to a 12-bit or 16-bit bus and the state of the BYTE SELECT is ignored.

When DATA MODE is low, the data is presented in the form of two 8-bit bytes, with selection of each byte by the state of BYTE SELECT during the read cycle.

The BYTE SELECT input is usually driven by the least significant bit of the address bus, allowing storage of the output data word in two consecutive memory locations.

When BYTE SELECT is low, the byte addressed contains the 8MSBs. When BYTE SELECT is high, the byte addressed contains the 4LSBs from the conversion followed by four zeros that have been forced by the control logic. The left-justified formats of the two 8-bit bytes are shown in Figure 24. The design of the SDM guarantees that the BYTE SELECT input may be toggled at any time without damage to the output buffers occuring.

In the majority of applications, the read operation will be attempted only after the conversion is complete and the status output has gone low. In those situations requiring the fastest possible access to the data, the read may be started as much as (t_{DD} max + t_{HS} max) before STATUS goes low. Refer to Read Cycle Timing for these timing relationships.

APPLICATIONS INFORMATION

ASSEMBLY OF SURFACE MOUNT PACKAGES

There are several assembly methods for the LCC versions of the SDM8XX. The associated advantages and disadvantages of three methods are outlined below.

1. DIRECT SURFACE MOUNT ONTO PCB

ADVANTAGES	DISADVANTAGES
Ease of assembly Low cost Low weight Small footprint size	Difficult to inspect solder joints Difficult to clean Choice of board material important in wide temperature range applications

In wide temperature applications it is important to match the coefficients of thermal expansion of the board and the SDM8XXL. Below is a list of materials and their approximate coefficients of linear thermal expansion.

MATERIAL	(ppm/°C)
Alumina (96%) - SDM Package	6-7
Copper-clad-Invar (50% Cu)	9
(30% Cu)	6
(10% Cu)	3
Epoxy-Kevlar (60% Kevlar)	6
Polyimide-Kevlar (40% Kevlar)	6
Beryllia	5
Polyimide-glass (x-axis)	12
(y-axis)	14

Kevlar™ E.I. du Pont de Nemours & Co.

2. ATTACHMENT OF SURFACE MOUNT EDGE CLIPS

ADVANTAGES	DISADVANTAGES
Ease of Inspection Easy cleaning Thermal expansion taken up by the flexing of the edge clips	Extra cost Extra assembly

ASSEMBLY

The edge clips are attached to the edges of the SDM8XXL as in Figure 25 before the device is mounted on to the board.

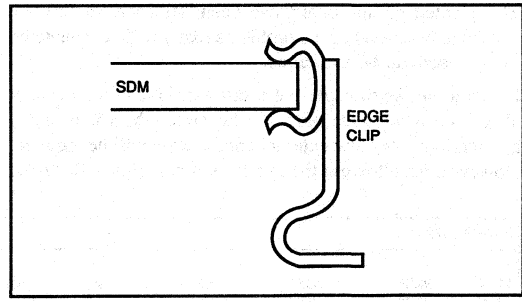


FIGURE 25. Edge Clip Assembly.

SUPPLIERS OF EDGE CLIPS

USA	USA
DIE-TECH INC., R.D. 1, Sipe Road, York Haven, PA 17370 USA PHONE: (717) 938-6771	NAS Electronics, 381 Park St., Hackensack, NJ 07602 USA PHONE: (201) 343-3156
EUROPE	**EUROPE**
SEMI-DICE (UK) Ltd, Buckingham House, Mineral Lane, Chesham, Bucks. HP5 2AU UK PHONE: 0494 771275	NASBRIT Ltd, Wester Goudi Ind. Est. Dundee DD2 4UX UK PHONE: 0382 622222

3. SURFACE MOUNT SOCKET

ADVANTAGES	DISADVANTAGES
Board thermal expansion not so critical Ease of component replacement	Cost Extra height (if critical)

Below is the name and address of a supplier of a 68-pin surface mountable socket.

The part number is: Socket 212-068-012
Spring cover CCS-004

USA	EUROPE
Methode Electronics INC, Interconnect Products Div. 1700 Hick Road, Roling Meadows, TX 75050 USA PHONE: (312) 392-3500	Lucas Methode Connectors Ltd, Halifax Road Ingrow Bridge, Keighley, Yorkshire BD21 5HR UK PHONE: 0535 603282

General Comments

The advantages and disadvantages of all the methods mentioned above are for general use of surface mount components. Every user will find that the importance of these factors will depend on his application and situation.

EVALUATION BOARD

For the engineer who wishes to evaluate the SDM family, Burr-Brown has designed printed circuit boards on a single 'Eurocard' (shown here for LCC only). These boards enable the design engineer to experiment with various accuracy improvement techniques which are described below. Special consideration has been given to the grounding and circuit layout techniques required when dealing with 12-bit analog signals.

The printed circuit board has been designed so that the solutions to several of the problems likely to be encountered by the user can be examined.

It should not be thought that every user is required to adopt all of the techniques used on the circuit board. In many applications very few external components will be required. However, in following the application guidelines illustrated by the circuitry and accompanying notes, the designer will be able to select and adapt the solutions most suited to their won particular application or problem area.

Provisions for the following are made on the LCC PC board:

—68 pin LCC socket (Burr-Brown Part No. MC0068).
—8 differential or 16 single-ended inputs.
—Input filtering with overvoltage protection for each channel.
—Socket for quad D-type flip-flop 74175 (MUX address latches).
—7 additional I.C. sockets for easy interfacing to various BUS systems (connection by wire wrap techniques).
—2 voltage regulators (15V).
—LC power supply decoupling.

The layout pays particluar attention to the requirements when operating with precision analog signals. This requires strict separation of the analog and digital areas. Analog and digital commons are totally separated and connected together only at the commons of the supply voltage. All common lines are low resistance and low inductance.

SUPPLY VOLTAGES

In order to avoid coupling between the external supply voltage 15V supplies, 2 voltage regulators (78M15, 79L15) are provided on the PC board. The unregulated supply voltage may vary from ±17V to ±25V.

The MUX/INA section and SHC/ADC section of the SDM have separate supply lines which can be inductively decoupled. This is recommended in order to suppress the high frequency noise which comes from the ADC during conversion.

The power supply rejection of the instrumentation amplifier reduces with increasing frequency. If high frequency noise on the supplies is not decoupled it will be injected into the signal path and cause errors. This effect can be particularly pronounced when using the 'overlap' mode since the instrumentation amplifier is settling to a new analog value while the ADC is still carrying out the previous conversion.

SDM862/872						SDM863/873				
MUX ADD3	MUX ADD2	MUX ADD1	MUX ADD0	MUX Enable	Channel Selected	MUX ADD2	MUX ADD1	MUX ADD0	MUX Enable	Channel Pair Selected
X	X	X	X	L	NONE	X	X	X	L	NONE
L	L	L	L	H	0	L	L	L	H	0
L	L	L	H	H	1	L	L	H	H	1
L	L	H	L	H	2	L	H	L	H	2
L	L	H	H	H	3	L	H	H	H	3
L	H	L	L	H	4	H	L	L	H	4
L	H	L	H	H	5	H	L	H	H	5
L	H	H	L	H	6	H	H	L	H	6
L	H	H	H	H	7	H	H	H	H	7
H	L	L	L	H	8			–		
H	L	L	H	H	9			–		
H	L	H	L	H	10			–		
H	L	H	H	H	11			–		
H	H	L	L	H	12			–		
H	H	L	H	H	13			–		
H	H	H	L	H	14			–		
H	H	H	H	H	15			–		

FIGURE 26. Channel Select Truth Table.

The digital supply voltage is +5V and is also LC-filtered.

All supply lines are bypassed with a 10µF tantalum and a 100nF ceramic capacitor situated **as close as possible** to the package.

If the voltage regulators for the ±15V are not used, small inductors for decoupling of the supply voltages are recommended. If inductors are not fitted a dynamic ground loop will be created from supply lines via bypass capacitors to analog common.

INPUT PROTECTION

The multiplexer is protected up to an input voltage which can exceed the supply voltage by a maximum of 20V. This means, that with ±15V supply voltage, the input voltage can be ±35V without damage. This is also the case when the supply voltages are switched off (0V). The maximum input voltage can then be ±20V. For higher overvoltage protection a series resistor has to be used. The current via the multiplexer should be limited to 20mA absolute maximum, 1mA is preferred. For example, a 10kΩ series resistor would give an additional 10V overprotection.

For much higher overvoltages (e.g. 100V), high value series resistors cannot be used as offset errors would result. In practice, a combination of series resistors and diodes is used. The diodes are connected to ±15V and will conduct whenever the input voltage exceeds the ±15V supply voltage. The diodes are selected by signal source impedance, as well as filter resistance, as the diode leakage current across the series resistor can cause offset and linearity errors. In this circuit, IN4148 together with 10kΩ are used.

INPUT FILTER

Processor noise can be induced in the analog ground. Input filtering is therefore recommended for analog data aquisition. Such high frequency noise signals can cause dynamic overload of the instrumentation amplifier resulting in non-linear behavior. This leads directly to digitizing errors.

The design of the filter takes into account the characteristics of the SDM and of the signal source.

The following points have to be considered:

—The stray capacitance, output capacitance of the multiplexer and input capacitance of the instrument amplifier (up to 80pf in some cases) has to be discharged in order to minimize errors caused by 'charge sharing.'

—The series resistor limits the current in the protection diodes, but it also has to be selected for the required filter time constant.

—The noise rejection of the filter has to be >80db in order to satisfy a 12-bit A/D conversion.

As well as considering the above, different calculations have to be carried out for single and differential input signals.

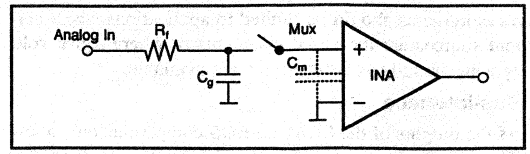


FIGURE 27.

Single-Ended Measurement

R_f limits the maximum input current through the protection diodes. In this case, R_f has been chosen as 10kΩ and together with the capacitor C_g, forms the input filter time constant (C_g = 0.47µF). The time constant must be chosen according to the requirements of the input signal bandwidth and noise rejection. The multiplexer capacitance (C_m) is discharged mainly by C_g. This means C_g has to be sufficiently large compared with C_m or charged via R_f prior to re-sampling of the signal.

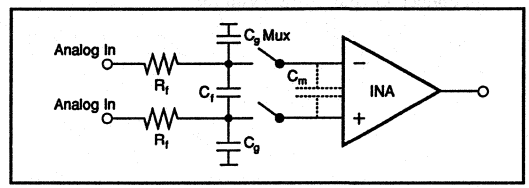


FIGURE 28.

Differential Measurement

Capacitor C_f, is used for limiting the input signal frequency. The bandwidth is calculated as follows:

$$F_f = \frac{1}{4\pi R_f C_f} \quad \text{IF } C_f >> C_g$$

When selecting the value of C_f, it should be noted that C_m has to be discharged when switching the multiplexer channels. This means that the voltage error of C_f (induced by 'charge sharing' with C_m) has to be smaller than 1LSB. Therefore, C_f should have a minimum value of a 0.47µF. The resistors R_f, together with the source impedance, have to be sufficiently small in order to recharge C_f prior to signal sampling. This prevents errors in the signal value caused by the charge stored on C_m by the previously selected channel.

The 2 capacitors C_g form together with R_f a common-mode filter. This filter greatly improves accuracy in a noisy environment (decrease of common-mode rejection of instrumentation amplifier with increasing frequency).

For good common-mode filter operation, both time constants R_f and C_g should match each other within 2%. Additional errors will be induced by a mismatch.

Selected values are: C_f = 0.47µF, C_g = 10nF, R_f = 10kΩ. The filter reduces the signal slew rate so that the instrumentation amplifier can follow the voltage variation of the signal with the noise component eliminated.

In general, all measurements which require more than a gain of 10 should be done in differential mode. Single ended

measurements should be limited to applications where current sources are measured via shunts or where signal voltages in the range of some volts are available.

Bus-Interface

As the outputs of the SDM are BUS compatible, only a few ICs are necessary to interface to various BUS systems. For such interfacing, 20-pin IC sockets are provided. Wiring is by wire wrap to the BUS connector.

Setting of Various Modes

Circuit Board positions are provided for the connection of 'jumpers' as follows:

J1, J2—ADC analog input voltage settings.
J3—Set for differential (SDM8X3) or single ended (SMD8X2) operation.
J4—Instrumentation amplifier gain settings.

(a) 16 input channels, single ended:
—Use SDM8X2
—Consider single-ended filtering
—Connect J3 (pin 66) to common

(b) Differential inputs
—Use SDM8X3
—Consider differential filtering
—Connect J3 (pin 66) to pin 67

(c) Analog input

±10V	Connect J1 to pin 21
	Connect J2 to pot P2 (100Ω)
±5V	Connect J1 to pin 22
	Connect J2 to pot P2 (100Ω)
0 to +10V:	Connect J1 to pin 22
	Connect J2 to junction of R_1/R_2

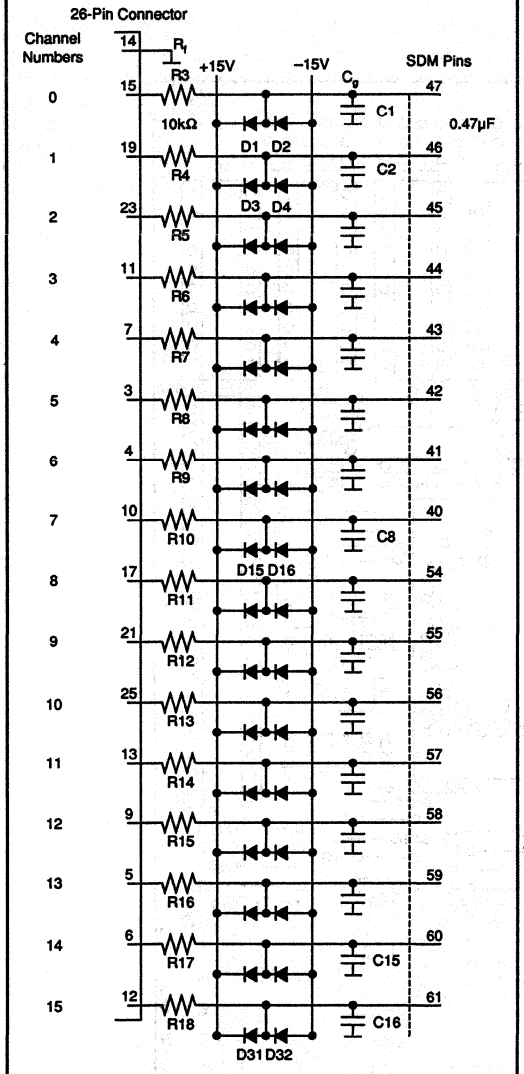
(d) Gain of instrumentation amplifier

G = 1	Jumper J4 open
G = 10	Jumper J4 to pin 63
G = 100	Jumper J4 to pin 64

Other gains: use additional resistor between pin 62 and pin 63 (see section on Instrumentation Amplifier) as low tempco resistor is recommended in order to minimize gain drift.

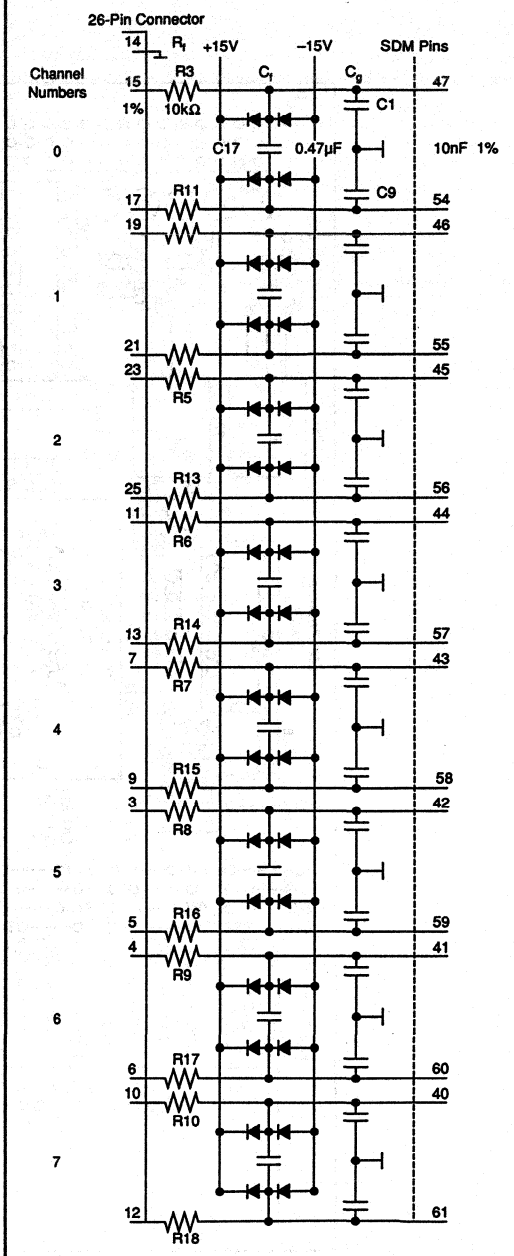
INPUT FILTER AND PROTECTION CIRCUITRY

SINGLE-ENDED



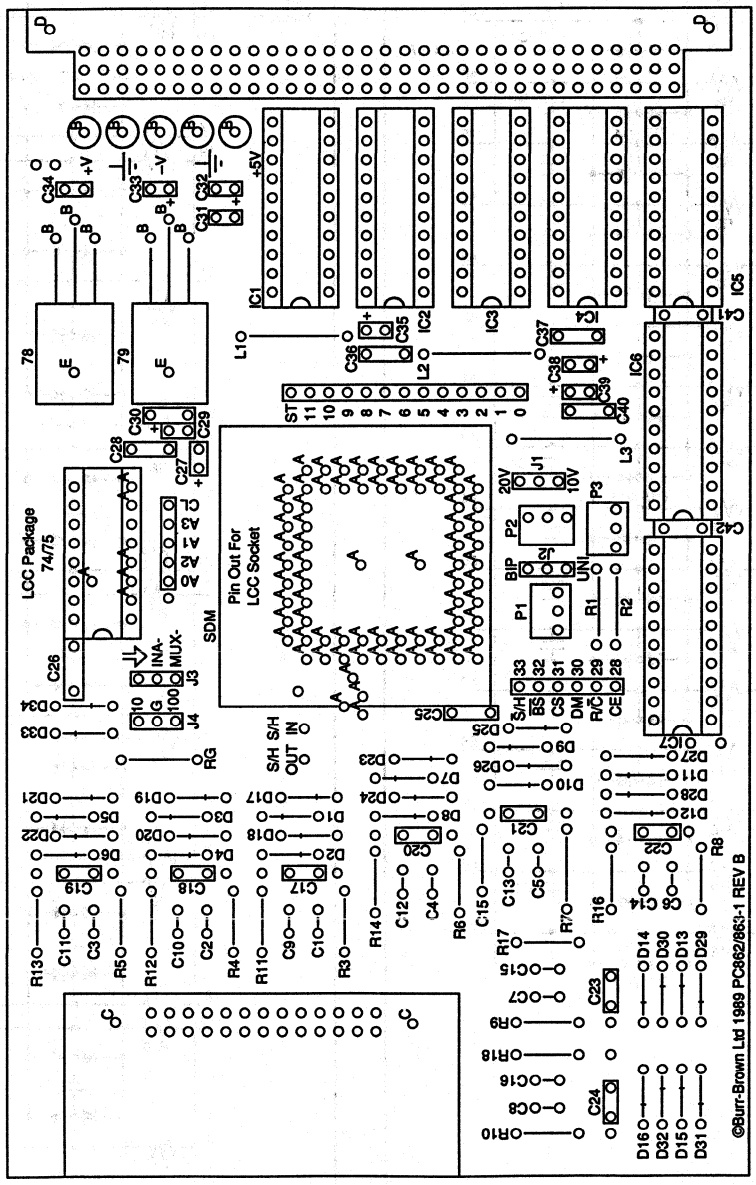
Pins 1, 2, 8, 14, 16, 18, 20, 22, 24 and 26 are Connected to Common

DIFFERENTIAL



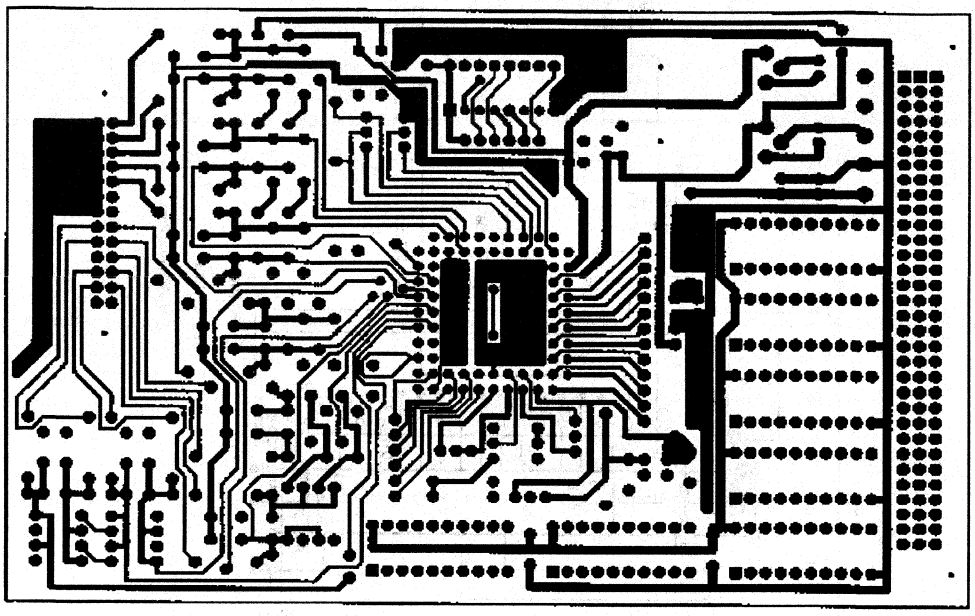
Pins 1, 2, 8, 14, 16, 18, 20, 22, 24 and 26 are Connected to Common

PCB COMPONENT LAYOUT

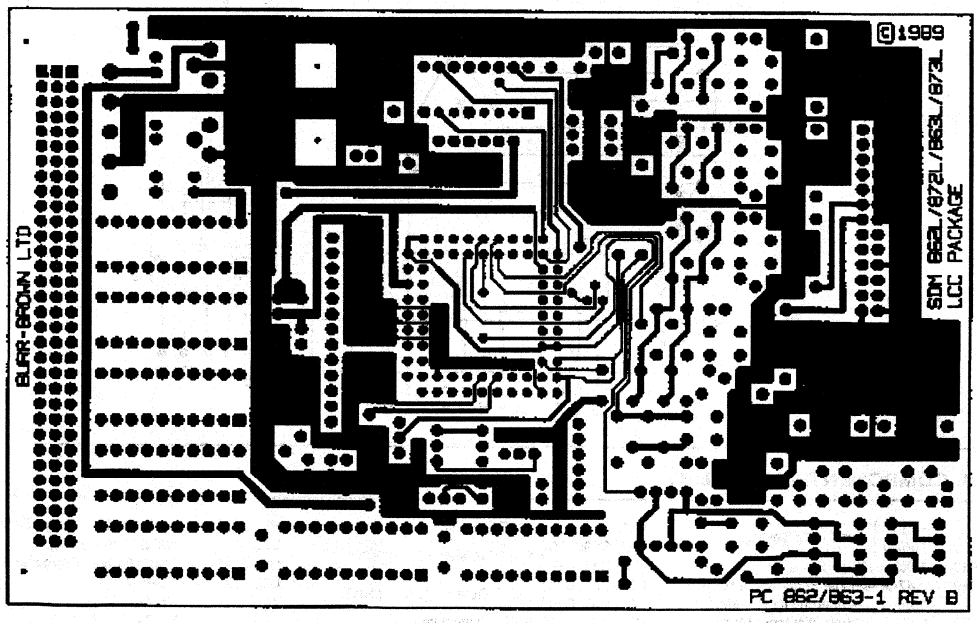


NOTE: (1) NOT SUITABLE FOR PGA PACKAGE SEE PC862/863-2
(2) NOT DRAWN TO SCALE

P.C.B. LAYOUT

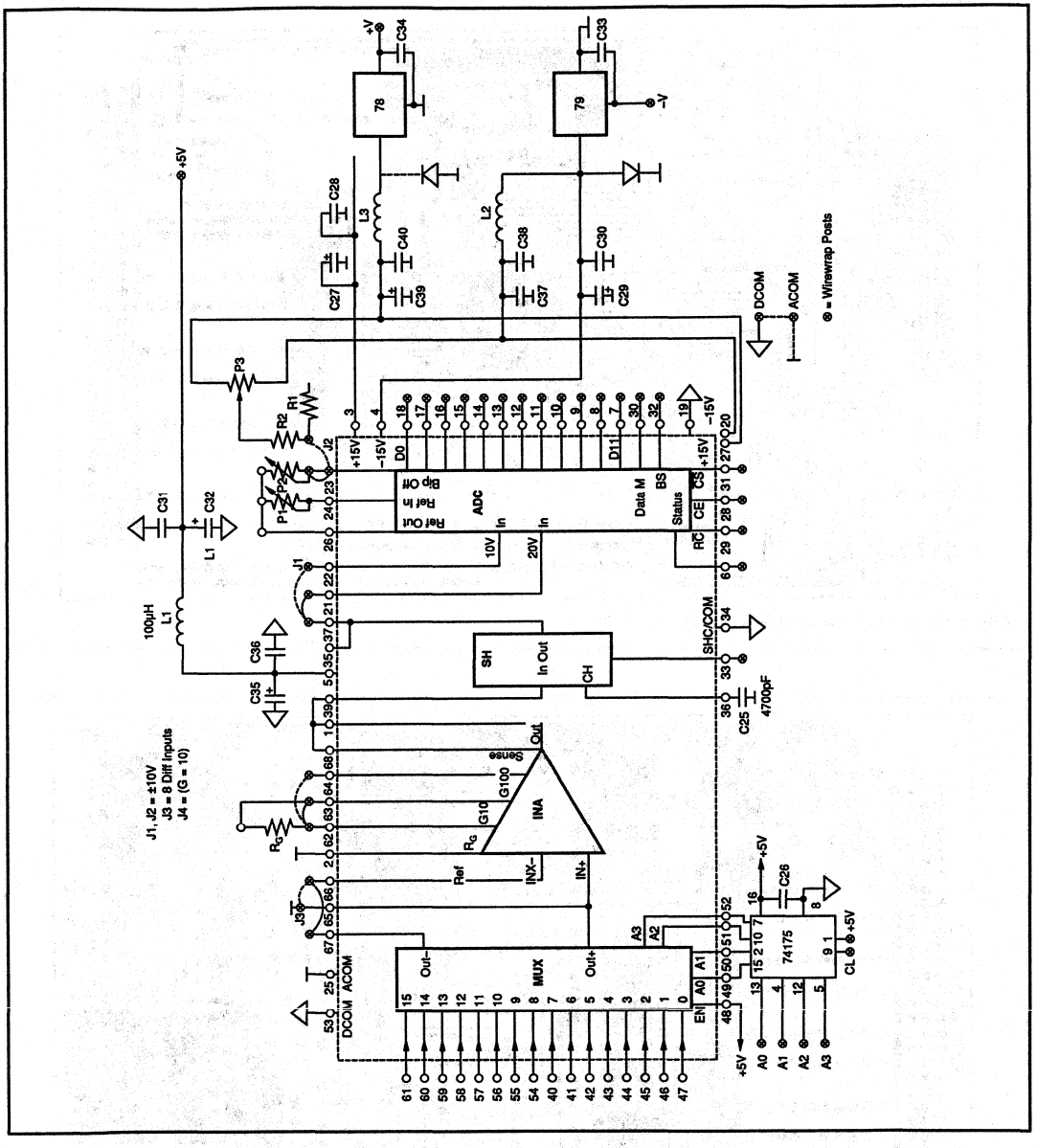


NOTE: NOT SUITABLE FOR PGA PACKAGE SEE PC862/863-2



NOTE: NOT SUITABLE FOR PGA PACKAGE SEE PC862/863-2

CIRCUIT DIAGRAM—SDM PC BOARD



P.C.B. COMPONENTS PARTS LIST

R1	100Ω } For 0–10V Settling	C26	10nF Ceramic	P3	100kΩ **0–10V Range Only**
R2	100kΩ } For 0–10V Settling	C27, C29, C35	10µF Tantalum (Decoupling)	L1...L3	100µH (Decoupling)
R3...R18	10kΩ 1%	C32, C38, C39		D1...D32	1N4148 (Input Protection Diodes)
C1...C16	0.47µF—Single Ended Input Mode	C28, C30, C31	100nF Ceramic (Decoupling)	D33, D34	1N4007
	10nF 1%—Differential Input Mode	C36, C37, C40		78	MC78M15CG
C17...C24	0.47µF—Differential Input Mode	C33, C34	0.33µF Tantalum	79	MC79L15CG
C25	4.700pF (Polypropylene, Polystyrene or Teflon™)	P1	100Ω	74175	74LS175
		P2	100Ω **±5V, ±10V Range Only**	LCC Socket	MC0068

UNLESS OTHERWISE MARKED—RESISTORS ARE 1/4W, 5%, CAPACITORS ARE 10%

Teflon™ E.I. du Pont de Nemours & Co.

14 Other Burr-Brown Products

Burr-Brown's world of digital signal processing solutions emphasizes ease of use and ranges from DIP-packaged analog input and analog output components all the way to complete DSP-based systems. The product line includes development and code generation software, dedicated processors, and analog I/O products. Easy-to-use and cost efficient, these products carry the user all the way from simulation to integration.

Other DSP design and integration tools are currently in development. If you need to find the shortest route from DSP development to integration, call the Product Information Center at 1-800-548-6132.

ANALOG DSP COMPONENTS AND TEST SYSTEMS

Function	Model	Description	Sample Rate	Resolution	Package	Page
Analog-to-Digital Converters	DSP101	Low-cost, high resolution A-to-D with zero-chip interface to DSP IC's from ADI, AT&T, Motorola and TI	200kHz	16/18 bits	28-pin DIP	S-9.1.89
	DSP102	Two channel, low-cost, high resolution A-to-D with zero-chip interface to DSP IC's from ADI, AT&T, Motorola and TI	200kHz	16/18 bits	28-pin DIP	S-9.1.89
Digital-to-Analog Converters	DSP201	Low-cost, high resolution D-to-A with zero-chip interface to DSP IC's from ADI, AT&T, Motorola and TI	500kHz	16/18 bits	28-pin DIP	S-6.2.139
	DSP202	Two channel, low-cost, high resolution D-to-A with zero-chip interface to DSP IC's from ADI, AT&T, Motorola and TI	200kHz	16/18 bits	28-pin DIP	S-6.2.139

BURR-BROWN POWER SUPPLIES AND THE POWER CONVERTIBLES HANDBOOK

Burr-Brown offers a wide selection of power conversion products. Hundreds of standard and unique DC/DC converters ranging from DIP sizes through high wattage, wide-range modular packages are available. They are summarized in tables on the following three pages. All of these models carry Burr-Brown's guarantee of high quality and reliability and are included in their own publication, *Burr-Brown Power Convertibles Handbook.*

The Burr-Brown Power Convertibles Handbook contains detailed Product Data Sheets for the best of Burr-Brown's power conversion products. In addition, it includes supplementary data, such as an extensive selection guide, discussion of the advanced reliability programs available, a glossary of power conversion terminology, and application notes for effective use of these products. Information on obtaining modified and custom models is also included.

POWER CONVERTIBLES

SERIES	POWER (WATTS)	INPUT VOLTAGES (PLUS OR MINUS)						OUTPUT VOLTAGES							# OF CHANNELS	OUTPUTS PER CHANNEL	REGULATION	ISOLATION VOLTAGE	SHIELDING	SHORT CIRCUIT PROTECTION
								PLUS OR MINUS				PLUS AND MINUS								
HPR1XX	0.75	5	12	15	24			5		12	15	5	12	15	1	S/D	U	750	NO	Momentary
HPR4XX	0.75	5	12	15	24			5		12	15	5	12	15	1	S/D	U	1000	NO	Momentary
PWR59XX	1.00	5	12	15	24			5	9	12	15	5	12	15	1	S/D	R	750	NO	Continuous
PWR11XX	1.50	5	12	15	24			5	9	12	15	5	12	15	1	S/D	U	500	NO	Momentary
PWR13XX	1.50	5	12	15				5		12	15	5	12	15	1	S/D	U	4000	NO	5 Seconds
PWR1726	1.50			15										15	1	D	U	5000	NO	Continuous
PWR60XX	1.80	5	12	15	24			5					12	15	1	S/D	R	500	NO	Continuous
PWR3XX	2.00	5	12	15	24	28	48	5		12	15	5	12	15	2	S/D	U	1000	YES	Continuous
LPR3XX	2.25	5	12						9						1	S	U	500	NO	Momentary
PWR1017	3.00			15										15	4	D	U	1000	YES	Momentary
PWR12XX	3.00	5	12	15	24			5	9	12	15	5	12	15	1	S/D	U	500	NO	Momentary
HPR2XX	3.00	5	12	15	24							5	12	15	4	D	U	750	NO	Momentary
WPR4XX	3.00			18-36		36-72		5					12	15	1	S/D	R	500	NO	10 Seconds
PWR40XX	4.00	5	12	15	24			5		12			12	15	1	S/D	U	1000	NO	Momentary
PWR5XX	4.00	5	12	15	24	28	48	5		12	15	5	12	15	4	S/D	U	750	YES	Momentary
HPR7XX	5.00	5	12	15				5				5	12	15	1	S/D	U	500	YES	Momentary
PWR1546A	5.00	5												15	1	D	R	750	YES	Continuous
PWR70XX	5.00	5	12	15	24		48	5				5	12	15	1	S/D	R	500	YES	Continuous
PWR8XX	5.00	5	12	15	24	28	48	5					12	15	2	T	U	1000	YES	Momentary
PWR62XX	5.20	5	12	15	24	28	48	-5.2							1	S	R	500	YES	Continuous
PWR16XX	6.00	5	12	15	24			5		12			12	15	1	S/D	U	500	YES	Momentary
PWR51XX	9.00	5											12	15	1	D	R	750	YES	15 Seconds
PWR53XX	15.00	9-18		18-36		36-72		5		12	15	5	12	15	1	S/D/T	R	500	YES	Continuous

UNREGULATED POWER CONVERTIBLES

Model	Rated Power (Watts)	Features
HPR1XX	0.75	Miniature SIP
HPR4XX	0.75	High Isolation, Miniature SIP
PWR11XX	1.50	Low Cost, DIP
PWR13XX	1.50	High Isolation, DIP
PWR1726	1.50	Very High Isolation
PWR3XX	2.00	Multichannel
LPR3XX	2.25	LAN Applications (9 volt output)
PWR1017	3.00	Multichannel
PWR12XX	3.00	Low Cost, DIP
HPR2XX	3.00	Multichannel, SIP
PWR40XX	4.00	Low Cost
PWR5XX	4.00	Multichannel
HPR7XX	5.00	Low Cost, SIP
PWR8XX	5.00	Triple Output
PWR16XX	6.00	Low Cost

REGULATED POWER CONVERTIBLES

Model	Rated Power (Watts)	Regulation Line (%)	Regulation Load (%)	Features
PWR59XX	1.00	±0.3	0.4	DIP, Low Cost
PWR60XX	1.80	±0.2	0.5	Low Noise, Low Cost
PWR1546A	5.00	±0.02	0.02	Ultra Low Noise
PWR70XX	5.00	±0.02	0.04	Standard Pinout, Low Cost
PWR62XX	5.20	±0.04	0.06	ECL Power (5.2V output)
PWR51XX	9.00	±0.02	0.04	High Power Density
PWR53XX	15.00	±0.2	1.0	Wide Input Voltage Range, Triple Output

SPECIAL OUTPUT VOLTAGE POWER CONVERTIBLES

Model	Total Rated (Watts)	Special Voltage	Features
PWR59XX	1.00	–9 Volts	Regulated, DIP, LAN
LPR3XX	2.25	–9 Volts	Low Cost, DIP,LAN
PWR62XX	5.20	–5.2 Volts	ECL Power Supply

SPECIAL OUTPUT VOLTAGE POWER CONVERTIBLES

Model	Total Rated (Watts)	Special Voltage	Features
PWR59XX	1.00	–9 Volts	Regulated, DIP, LAN
LPR3XX	2.25	–9 Volts	Low Cost, DIP,LAN
PWR62XX	5.20	–5.2 Volts	ECL Power Supply

MULTICHANNEL POWER CONVERTIBLES

Model	Total Rated Power (Watts)	Number of Channels	Outputs per Channel	Total Number of Outputs
PWR3XX	2.00	2	Single or Dual	2, 3, or 4
PWR1017	3.00	4	Dual	8
HPR2XX	3.00	4	Dual	8
PWR5XX	4.00	4	Single or Dual	4, 5, 6, 7, or 8
PWR8XX	5.00	2	Single + Dual	3

HIGH ISOLATION POWER CONVERTIBLES

Model	Rated Power (Watts)	Test Voltage (AC, Vpeak 60Hz,60s)	Rated Voltage (VDC)
HPR4XX	0.75	3000	1000
PWR13XX	1.50	8000	4000
PWR1726	1.50	8000	5000
PWR3XX	2.00	3000	1000
PWR60XX-HV	2.00	3000	1000
PWR1017	3.00	3000	1000
PWR40XX	4.00	3000	1000
PWR8XX	5.00	3000	1000

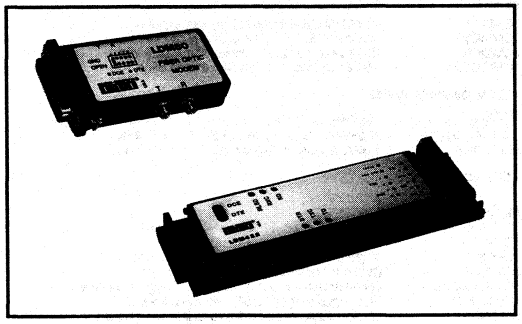
LOW NOISE POWER CONVERTIBLES

Model	Rated Power (Watts)	Noise Out (mVp-p) Typ	Max	Features
PWR59XX	1.00	50		Low Cost, DIP
PWR1546A	5.00	0.6	1.0	Ultra Low Noise
PWR70XX	5.00	30		Standard Pinout, Low Cost
PWR51XX	9.00	6	35	High Power Density
PWR53XX	15.00	40	75	Wide Input Voltage Range Triple Output

STD BUS AND DATA COMMUNICATIONS PRODUCTS

The Burr-Brown STD Bus products provide the most cost-effective tool for solving the applications-oriented problems of process control and system integration.

The modularity and simplicity offered by this well-defined standard have led to the development of a complete line of STD Bus products. The line includes a 32-channel 12-bit A/D converter, two CRT controllers, and IEEE-488 interface card, and two types of discrete I/O cards.



DATA COMMUNICATIONS PRODUCTS

Burr-Brown Data Communications products provide the most cost-effective tool for solving the local data communications problems for industrial and institutional facilities.

Limited Distance and Fiber Optic Modems provide extension of RS-232 ports up to several miles. In addition, electrical isolation for wire units is provided by transformers and optical couplers, eliminating ground loops, equipment damage, and noise pickup. Surge suppresion devices are internally mounted on all field inputs and outputs. The LDM422 (right) serv es as a Limited Distance Modem and as an RS-232-to-RS-422 converter with multipoint capability. It has two complete high speed transmit and receive channels for data and handshake. It features 1000V isolation and surge protection.

Fiber optic modems offer the maximum in isolation and EMI/RFI immunity. The LDM80 (left) is signal powered from RS-232 ports and transmits up to 3.5km at 19.2Kbits per second. The LDM85 is a unique multipoint-capable modem with data rates to 5Mbits per second.

Other products include:

LDM30—Low Cost Limited-Distance Modem.

LDM35—Signal-Powered Limited-Distance Modem.

LDM70—High Speed Ruggedized Limited-Distance Modem.

LDM485—RS-485 Compatible Limited-Distance Modem.

SCM5B ISOLATED SIGNAL CONDITIONING PRODUCTS

Burr-Brown now offers cost-effective, improved replacements for popular industrial signal conditioning modules. The new SCM5B analog modules are form, fit, and functional equivalents to similar products from other manufacturers. The SCM digital line replaces similar I/O products from industry's leading suppliers. Both lines include a very complete selection of backpanel options, interface cables, racks, fuses, jumpers, power supplies, and other accessory items.

These signal conditioning modules are essential components of safe data acquisition system design. Isolation barriers in each module prevent damage to expensive control room equipment from hazardous voltages and lightning surges usually present in industrial applications. Isolation also prevents troublesome ground loops which disrupt the measured signal.

Filter circuits on the input modules eliminate electrical noise in the measured signal. Overall, the SCM product line of analog and digital signal conditioners and accessories create a more cost effective and manageable method for system, design, expansion, and repair.

Key Specifications:

SCM5B Analog Modules

- 1500V Isolation
- Accuracy, 0.05%
- CMR, 160dB
- NMR, 95dB
- Transient Protection, IEEE-472
- ±1µV/°C Drift
- Output noise as low as 150µVrms
- Input protection, 240VAC
- Operating temp range, –25°C to +85°C

SCM Digital Modules

- 4000V Isolation
- Certification, UL/CSA
- Operating temp range, –30°C to +70°C

For Immediate Assistance, Contact Your Local Salesperson

SELECTION GUIDE FOR SCM ISOLATED SIGNAL CONDITIONING PRODUCTS

ANALOG mV, V INPUT MODULES, LOW BANDWIDTH (4Hz BW)

MODEL	INPUT	OUTPUT
SCM5B30-01	±10mV	±5V
SCM5B30-02	±50mV	±5V
SCM5B30-03	±100mV	±5V
SCM5B30-04	±10mV	0 to +5V
SCM5B30-05	±50mV	0 to +5V
SCM5B30-06	±100mV	0 to +5V
SCM5B31-01	±1V	±5V
SCM5B31-02	±5V	±5V
SCM5B31-03	±10V	±5V
SCM5B31-04	±1V	0 to +5V
SCM5B31-05	±5V	0 to +5V
SCM5B31-06	±10V	0 to +5V

ANALOG CURRENT INPUT MODULES, LOW BANDWIDTH (4Hz BW)

MODEL	INPUT	OUTPUT
SCM5B32-01	4 to 20mA	0 to +5V
SCM5B32-02	0 to 20mA	0 to +5V

RTD INPUT MODULES (ALL 0 to +5V OUTPUT, 4Hz BW)

MODEL	TYPE	INPUT RANGE
SCM5B34-01	100Ω Pt	–100 to +100°C (–148 to +212°F)
SCM5B34-02	100Ω Pt	0 to +100°C (+32 to +212°F)
SCM5B34-03	100Ω Pt	0 to +200°C (+32 to +392°F)
SCM5B34-04	100Ω Pt	0 to +600°C (+32 to + 1112°F)
SCM5B34C-01	10Ω Cu at 0°C	0 to +120°C (+32 to +248°F)
SCM5B34C-02	10Ω Cu at 25°C	0 to 120°C (+32 to +248°F)
SCM5B34N-01	120Ω Ni	0 to +300°C (+32 to +572°F)

THERMOCOUPLE INPUT MODULES (ALL 0 to +5V OUTPUT, 4Hz BW)

MODEL	TYPE	INPUT RANGE
SCM5B37J	J	–100 to +760°C (–148 to +1400°F)
SCM5B37K	K	–100 to +1350°C (–148 to +2462°F)
SCM5B37T	T	–100 to +400°C (–148 to +752°F)
SCM5B37E	E	0 to +900°C (+32 to +1652°F)
SCM5B37R	R	0 to +1750°C (+32 to +3182°F)
SCM5B37S	S	0 to +1750°C (+32 to +3182°F)
SCM5B37B	B	0 to +1800°C (+32 to +3272°F)

STRAIN GAGE INPUT MODULES, (ALL ±5V OUTPUT, 10kHz BW)

MODEL	EXCITATION	INPUT RANGE
SCM5B38-02	+10.0V at 3mV/V	300 to 10kΩ, Full Bridge
SCM5B38-04	+10.0V at 3mV/V	300 to 10kΩ, Half Bridge
SCM5B38-05	+10.0V at 2mV/V	300 to 10kΩ, Full Bridge

CURRENT OUTPUT MODULE (400Hz BW)

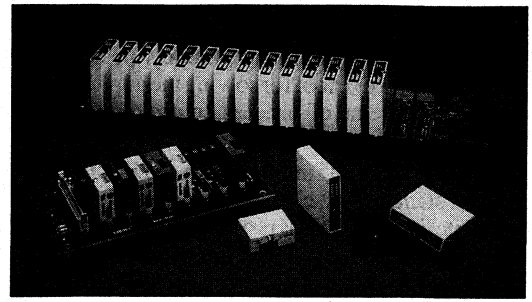
MODEL	INPUT	OUTPUT
SCM5B39-01	0 to +5V	4 to 20mA
SCM5B39-02	±5V	4 to 20mA
SCM5B39-03	0 to +5V	0 to 20mA
SCM5B39-04	±5V	0 to 20mA

ANALOG VOLTAGE INPUT MODULES, WIDE BANDWIDTH (10kHz BW)

MODEL	INPUT	OUTPUT
SCM5B40-01	±10mV	±5V
SCM5B40-02	±50mV	±5V
SCM5B40-03	±100mV	±5V
SCM5B40-04	±10mV	0 to +5V
SCM5B40-05	±50mV	0 to +5V
SCM5B40-06	±100mV	0 to +5V
SCM5B41-01	±1V	±5V
SCM5B41-02	±5V	±5V
SCM5B41-03	±10V	±5V
SCM5B41-04	±1V	0 to +5V
SCM5B41-05	±5V	0 to +5V
SCM5B41-06	±10V	0 to +5V

LINEARIZED THERMOCOUPLE INPUT MODULES, (ALL 0 to +5V OUTPUT, 4Hz BW)

MODEL	TYPE	INPUT RANGE
SCM5B47J-01	J	0 to +760°C (+32 to +1400°F)
SCM5B47J-02	J	–100 to +300°C (–148 to +572°F)
SCM5B47J-03	J	0 to +500°C (+32 to +932°F)
SCM5B47K-04	K	0 to +1000°C (+32 to +1832°F)
SCM5B47K-05	K	0 to +500°C (+32 to +932°F)
SCM5B47T-06	T	–100 to +400°C (–148 to +752°F)
SCM5B47T-07	T	0 to +200°C (+32 to +392°F)
SCM5B47E-08	E	0 to +1000°C (+32 to +1832°F)
SCM5B47R-09	R	+500 to +1750°C (+932 to +3182°F)
SCM5B47S-10	S	+500 to +1750°C (+932 to +3182°F)
SCM5B47B-11	B	+500 to +1800°C (+932 to +3272°F)



DIGITAL INPUT MODULES

MODEL	INPUT
SCMIAC5	90-140 VAC/DC Input, 11mA Max Input I
SCMIAC5A	180-280 VAC/DC Input, 6.5mA Max Input I
SCMIDC5	12-32 VAC, 10-32 VDC Input, 25mA Max Input I
SCMIDC5D	2.5-28 VDC Input, 30mA Max Input I, High Speed

DIGITAL OUTPUT MODULES

MODEL	OUTPUT
SCMOAC5A	24-280VAC Output, 3A at 45°C Output I Rating
SCMODC5	5-60VDC Output, 3A at 45°C Output I Rating

ACCESSORIES

ANALOG

MODEL	DESCRIPTION
SCMPB01	Non-multiplexed, 16 channel backpanel.
SCMPB02	Multiplexed, 16 channel backpanel.
SCMPB03	Single channel backpanel, DIN rail mount.
SCMPB04	Dual channel backpanel, DIN rail mount.
SCMXCA004-xx	System interface cable for both analog backpanels.
SCMXCA005	Daisy-chain cable for SCMPB02 backpanel.
SCMXIF	Ribbon cable to screw terminal interface board.
SCMXJP-003	Package of 10 jumpers.
SCMXFS-003	Package of 10, 4A fuses.
SCMXEV	Single channel SCM5B evaluation board.
SCMXRK-002	19 inch metal rack for mounting analog backpanels.
SCMXCS	Blank SCM5B module case and mounting screw.
SCMXPRT-003	Power supply, 3A, 5VDC, 120VAC U.S.
SCMXPRE-003	Power supply, 3A, 5VDC, 220VAC European.
SCMXR1	Precision 20Ω R for SCM5B32.

DIGITAL

MODEL	DESCRIPTION
SCMPB8H	8 channel backpanel.
SCMPB16H	16 channel backpanel.
SCMPB24	24 channel backpanel.
SCMXJP-001	Package of 10, 2 position barrier-strip jumpers.
SCMXJP-002	Package of 10, 8 position barrier-strip jumpers.
SCMXFS-001	Package of 10, 1A fuses.
SCMXFS-002	Package of 10, 5A fuses.
SCMX-INPUT	Input test module.
SCMX-OUTPUT	Output test module.
SCMXRK-001	19 inch metal rack for mounting digital backpanels.
SCMXPRT-001	Power supply, 0.5A, 5VDC, 120VAC U.S.
SCMXPRE-001	Power supply, 0.5A, 5VDC, 220VAC European.
SCMXCA001-xx	System interface cable for all digital backpanels.
SCMXCA002-xx	System interface cable for all digital backpanels.
SCMXCA003-xx	System interface cable for SCMPB24 backpanel.

MANUAL

SCMXMA-001	User's manual for all SCM digital and analog products.

16 Demo Board Products

Burr-Brown offers pre-designed demonstration boards for quick and easy evaluation of many products at your own site. The layout of these boards can also be used as a guideline for your own design. Schematics and CAD layouts are included with the fixtures. Evaluation fixtures are designed to connect to test equipment via BNC connectors. Application boards are designed with edge connectors instead of BNC connectors to allow the user to use the board as a daughter board.

MODEL	PRODUCT	DESCRIPTION
DEM-ACF2101BP-C	ACF2101BP	Evaluation Fixture with Programmable Timing Generator
DEM-ADC614-A	ADC603/614	Application Board Kit—Digital Output Only (Formerly DEM 1145)
DEM-ADC614-E	ADC603/614	Evaluation Fixture—Digital/Analog Output (Formerly DEM 1123)
DEM-ADC700-GC	ADC700	Evaluation Fixture—Digital/Analog Output
DEM-ADC701-E	ADC701/SHC702	Evaluation Fixture—Digital/Analog Output (Formerly DEM 1113)
DEM-ADC7802-GC	ADC7802	Evaluation Fixture—4 Input channels with +5V, ±5V, +10V and ±10V input voltage range
DEM-ADS602-A	ADS602	Application Board Kit—Digital Output Only (Formerly DEM 1146)
DEM-ADS7800-GC	ADS7800	Evaluation fixture—Dynamic and static 12-bit analog data acquisition system with two anti aliasing filters
DEM-BUF600-1GC	BUF600AP	Evaluation fixture—Buffer Amplifier
DEM-BUF601-1GC	BUF601AP	Evaluation Fixture—Buffer Amplifier
DEM-DSP102/202C	DSP102/202	Evaluation Fixture—DSP Interface with Programmable Timing Generator
DEM-FIFO-RAM-GC		Digital acquisition system up to 20 bit bus with 20MHz sampling rate 16k words
DEM-ISO122-GC	ISO122/HPR117	Evaluation fixture—8 channels isolated output (voltage and current)
DEM-ISO212-4-GC	ISO212	Evaluation Fixture—4 Input Channels, Tri-port isolation
DEM-ISO212-8-GC	ISO212	Evaluation fixture—8 Input Channels, Tri-port isolation
DEM-MPC100-GC	MPC100AU	Evaluation Fixture
	BUF601AU	4 to 1 video Multiplexer and Output Buffer
DEM-OPA541-GC	OPA541P	Evaluation Fixture—Contains current limitation resistor and protection circuitry
DEM-OPA620G/P-C	OPA620/621	Evaluation Fixture Kit for DIP packages—Generic Op Amp Configurations (Formerly DEM 1135)
DEM-OPA620U-C	OPA620/621	Evaluation Fixture Kit for SOIC packages—Generic Op Amp Configurations (Formerly DEM 1136)
DEM-PCM1700P-C	PCM1700	Evaluation Fixture—Serial/SPDIF Inputs (Formerly DEM 1143)
DEM-PCM1750P-C	PCM1750	Evaluation Fixture—Serial/Parallel Output, SPDF Out (Formerly DEM 1133)
DEM-PCM63P-C	PCM63P	Evaluation Fixture—Dual PCM63s, SPDIF Input
DEM-PCM67P-C	PCM67P	Evaluation Fixture—Dual PCM67s (single/dual supply operation), SPDIF Input
DEM-PCM78P-C	PCM78	Evaluation Fixture—Serial/Parallel Output Analog Reconstruction (Formerly DEM 1122)
DEM-OPA660-XXX	OPA660	Evaluation Fixture—Five boards are offered for five different configurations. DEM-OPA660-1GC: Diamond transistor and buffer; DEM-OPA660-2GC: Current-feedback operational amplifier; DEM-OPA660-3C: Direct-feedback amplifier; DEM-OPA660-4G: Layouts for all applications using SOIC (unassembled); DEM-OPA660-5G: Layouts for all applications using DIP packages (unassembled).

17 Die Products

HIGH PERFORMANCE CHIPS

HIGH PERFORMANCE DICE BACKED BY BURR-BROWN'S TRADITION OF QUALITY

Many of Burr-Brown's high-performance monolithic products are available in die form.

All Burr-Brown dice products are the same as those used in our high quality, high performance monolithic and hybrid devices and are proven in demanding applications throughout the world. The dice are manufactured and tested using the most advanced equipment and methods available, assuring the utmost in quality and reliability for every product.

The state-of-the-art performance achieved by these precision monolithic products reflects Burr-Brown's unmatched technical capabilities in:

Low-noise processing/High-stability nichrome
Thin-film resistors/Active laser trimming
Dielectric isolation/Patented circuit design

At Burr-Brown, concern for quality is a fundamental part of wafer processing.

INTEGRATED CIRCUIT DICE

Quality

Visual Inspection: All dice and wafers are 100% visually inspected to MIL-STD-883, Method, Method 2010, Condition B.

Probe Tests: All dice are electrically probe tested at the wafer level. The dice performance will typically be equivalent to its corresponding packaged device. Due to possible parametric shifts during die separation and assembly, these specifications are not guaranteed after assembly.

Package: Dice are packaged face-up in individually compartmented anti-static plastic carriers (waffle packs) and are oriented for automatic assembly. Carriers are heat sealed in plastic bags.

Lot Acceptance Testing: Lot Acceptance Testing is available on selected models. Consult the factory for availability.

Marking: Each die carrier is marked with:

1. Burr-Brown part number
2. Lot number
3. Wafer number
4. QA seal and date
5. Quantity
6. QC identification number

If required, customer part number and order number can be marked on each package.

Storage: High humidity and corrosive atmospheres can cause oxidation or corrosion of the metalization on wire bond pads. Dice should be protected from static damage and stored in a dry nitrogen atmosphere.

DIE HANDLING PRECAUTIONS

Handling: Although each die is protected by a glassivation layer, care should be taken to keep from scratching the surface of the die. Anti-static protection is recommended whenever dice are handled. All integrated circuits can suffer damage from electrostatic discharge. Precision devices can suffer subtle parametric damage (increased offset voltage, drift, noise, etc.) if precautions are not adequate. Anti-static work stations are recommended for the handling and assembly of precision semiconductor devices.

HYBRID CIRCUIT ASSEMBLY RECOMMENDATIONS

Die Attach: Die attach with silver conductive epoxy or polyimide is recommended to minimize assembly shifts and preserve the accuracy and precision inherent in the die.

Gold backed die can be eutectically die-attached using 98/2 gold/silicon preform and a die/substrate temperature of 400°C to 430°C. Exposure time to die attach temperatures should be minimized as permanent parametric shifts can occur.

Consult the device data sheet to determine the composition of the die backing.

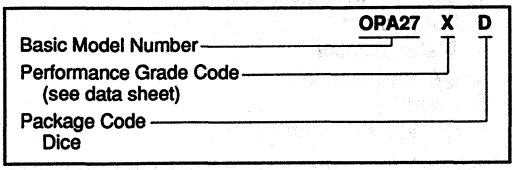
Wire Bond: Wire bonding may be done with ultrasonic bonders using 1.25 mil 99/1 aluminum/ silicon wire or by 1.25 mil 99.99% pure gold wire using thermo-sonic techniques. Wire bond pad size is 4 X 4 mils minimum.

Packaging: Assembly in hermetic packages using processes designed to provide an internal moisture content of less than 5000ppm is recommended in order to preserve parametric performance and stability.

Minimum Order: Dice are subject to minimum order quantities. Quantities ordered are to be multiples of the minimum pack count. See the accompanying table. Consult your local sales office for pricing.

Returns: Returns must be authorized by Burr-Brown. The entire lot must be returned in the original carriers along with detailed documentation showing reason for rejection.

ORDERING INFORMATION



DIE MODEL NUMBERS AND MINIMUM PACKAGE COUNT

DIE MODEL	MINIMUM PACK QTY	DIE MODEL	MINIMUM PACK QTY	DIE MODEL	MINIMUM PACK QTY
ACF2101D	100	INA102AD	50	OPA621AD	100
ADC574KD	50	INA103AD	100	OPA621SD	100
ADC674KD	25	INA105AD	100	OPA627AD	100
ADC774KD	25	INA110AD	100	OPA633AD	100
ADC80KD	25	INA110SD	100	OPA633KD	100
ADS574D	25	INA117KD	100	OPA633SD	100
ADS774D	25	MPY100AD	100	OPA637AD	100
ADS7800D	25	MPY534AD	100	OPA675JD	100
DAC702D	25	OPA111AD	100	OPA675SD	100
DAC703D	25	OPA128JD	100	OPA676JD	100
DAC703D	100	OPA2107AD	100	OPA676SD	100
DAC7541AD	100	OPA2111AD	100	PCM56D	50
DAC7545D	100	OPA27GD	100	PCM64D	25
DAC7800D	100	OPA37GD	100	PGA102KD	100
DAC7801D	100	OPA404AD	100	REF102D	100
DAC7802D	100	OPA445AD	100	REF200D	100
DAC80KD-I	100	OPA541AD	25	UAF42AD	50
DAC80KD-V	100	OPA541SD	25	VFC100AD	100
DAC811JD	100	OPA602AD	100	VFC320BD	100
DAC813D	25	OPA603AD	100	VFC32BD	100
INA101AD	100	OPA606KD	100	XTR101AD	25
INA101SD	25	OPA620AD	100	XTR110AD	100
		OPA620SD	100		

NOTE: Quantities ordered must be multiples of the minimim pack quantity.

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